

FINAL PROJECT

DESIGN OF MINI STEREO DIGITAL AUDIO PROCESSOR

EEDG 6306: Application Specific Integrated Circuit Design

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1. Introduction

Digital signal and audio processing is one of the major industry which largely depend on the advanced Digital Signal Processor (DSP) chips. Most of the modern multimedia systems require the implementation of audio processors which are highly accurate and efficient being the first priority. These DSP chips highly rely on the embedded high-performance multipliers for carrying out the filtering operation (be it FIR filter or IIR filter). But to achieve this, the cost becomes invariably high. So, when it comes to use such processors for battery powered, portable devices or household applications such as audio systems, cost of the audio processor and power consumption are of major concern. Most of the similar audio processing designs are implemented using the Digital Signal Processing (DSP) chips with separate left and right channel processing that performs the basic function of Finite Impulse Response (FIR) Digital Filter.

This project aims to create a Mini Stereo Digital Audio Processor (MSDAP) chip. For small audio applications like the hearing aid devices, such high performance is not required compared to the other audio applications like record studios. A new approach ‘Mini Stereo Digital Audio Processor (MSDAP)’ is proposed. This chip, instead of using large and power hungry multipliers, uses a single bit shifter and single bit adder. The proposed chip can do all the small audio operations which are done by any regular audio processor. The report starts with an overview of ASIC design flow model and briefly explains all the steps involved in the process. The rest of the report explains how all the steps from the design flow model are performed to create an MSDAP chip.

2. ASIC Design Flow

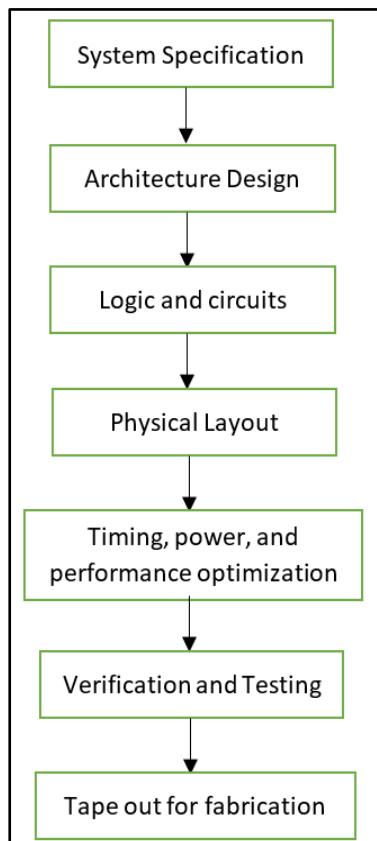


Figure 1: ASIC Design flow

designer can also choose to come up with full custom design to deploy his/her own optimizations by directly skipping to next step.

2.4. Physical Layout

In this step, initially floor-planning is for the chip is done according to the area and aspect ratio requirements. Later, placement and routing of the physical cells is done onto a 2 dimensional surface. The netlist obtained in the previous step is used to make these placements and connecting them.

2.5. Timing, power, and performance optimization

Even though the software simulation was successful in the step 2, it is not necessary that it will be successful after doing the physical layout. This is because, the physical layout represents the actual physical implementation of the design, and thus it will have the real-time signal delays, crosstalk, and similar issues which may cause malfunctioning of the design. The power consumption also needs to be checked with the target maximum power. For this, it is very necessary to optimize the physical layout for the required timing, power and performance optimization.

2.6. Verification and timing

This step is more or less performed throughout the whole ASIC design flow. This is to ensure that the defects are not introduced during the manufacture process. Even for this step, CAD tools such as HSPICE, PrimTime, etc. are very helpful to ensure the correct functionality and timing of the circuit.

2.7. Tape out for fabrication

The design is finally sent for the actual fabrication only after it has passed all the tests which are carried out during as well as after the previous steps.

2.1. System Specification

This is the first and the important most step in the ASIC design flow. In the real-world ASIC design process, it is very important to fully decompose and understand the application which needs to be implemented. Once the application is understood, clear and complete specifications needs to be written in fully technical terms such as number and name of I/O pins, clock frequency, operating modes, etc.

2.2. Architecture Design

This second step in the ASIC design flow deals with the high-level design of the system once all the required specifications are defined. This specification definition is already done in the first step. In this step, the detailed flow of the system is defined in terms of Finite State Machine. This step includes the design of the system in RTL code such as Verilog HDL or VHDL.

After developing the RTL, its functional verification needs to be done before proceeding to next step. This is to assure that this RTL description is giving the desired output

2.3. Logic and circuits

In this step, the RTL which was developed in the previous step is synthesized with the standard cell library. This translates the RTL description into a netlist file. This step in most cases can be automated using CAD tool like Synopsys Design Compiler or the

This project deals with all the ASIC design flow steps except for the last one. In the first half of the project, we will be dealing with the steps such as system specification for the proposed MSDAP chip, architectural design, and its functional verification. To implement this system, we are using Verilog HDL.

In the later stages of the project, we will use our RTL design to synthesize and then we will go through the other steps discussed above (such as physical layout, functional and timing verification, etc.)

3. Mini Stereo Digital Audio Processor (MSDAP)

In this project we are going to implement the MSDAP, an audio filter, from the paper provided. This system is implemented using an FIR filter and as discussed in next sections, it is implemented in such a way that there will be only single shift and then addition every clock cycle. This is done to increase the simplicity of the hardware. In order to implement this, the input files to the system are:

1. Actual 16 bit input data.
2. Coefficient data that provides an offset (K) for the input.
3. RJ values which represents the number of addition/subtractions to be performed before one shift

First, let's see the common approach of designing a digital filter and then we'll discuss the simpler approach i.e. the method given in the MSDAP paper.

3.1. Common approach

Normally, for implementing any kind of the digital filter, a common approach would be to use the linear convolution method. In this method the signal which needs to be filtered is convolved with the filter coefficient. The figure 2 shows an abstract of general convolution approach.

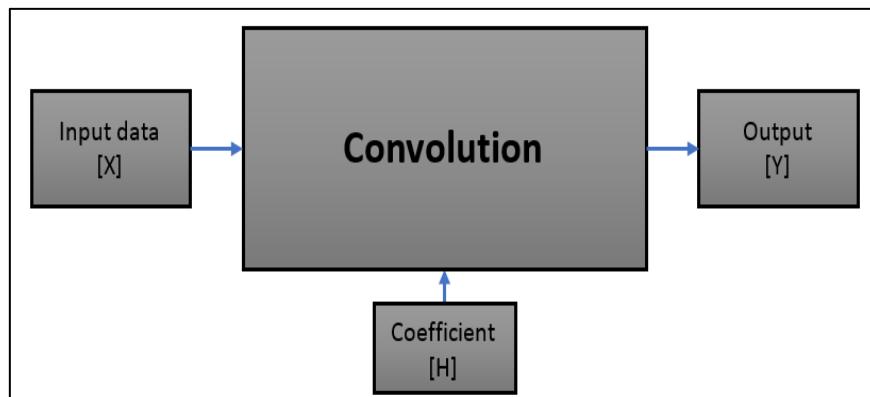


Figure 2: General convolution approach

Here, the convolution block will receive the digital input continuously. This input will be convolved with the filter coefficient H to generate the filtered output Y . This process is mathematically represented as follows:

$$Y(n) = \sum_{k=0}^N x(n-k) \times h(k)$$

where,

$x(n)$ is the input audio sequence and $y(n)$ is the output corresponding to $x(n)$. The filter coefficient is represented by $h(k)$ for the filter of the order N .

Careful observation at this equation makes it clear that it requires $N+1$ multiplications and N additions. To implement this filter, usually a DSP chip can be used which has a high-speed multiplier embedded onto it. But since this application needs to perform only linear convolution, it would be wise to use a simpler hardware that to use a DSP chip.

For an instance, let's take an example of filter coefficient as below.

$$h(k) = 2^{-3} - 2^{-7} + 2^{-16}$$

Putting it into the equation of $Y(n)$ above, after expanding the equation, it becomes as follows:

$$h(k).x(n-k) = 2^{-3}.x(n-k) - 2^{-7}.x(n-k) + 2^{-16}.x(n-k)$$

The above equation shows that it will use only three shifts and three additions/subtraction operations instead of using multiplier from DSP chip. One problem with this approach is that for a 4-bit filter coefficient function, the power-of-two (POT) digit can be 16 at max (i.e. 2-16). This implies that we need a big 16-bit shifter. This type of shifter will need to be programmed to perform dynamic shifting operation from 1-bit to 16-bits. This can increase the area requirement as well as it will reduce the overall system performance. This might destroy the whole purpose of making this design simpler. An excellent idea of using only one single bit shifter is proposed in the MSDAP paper.

3.2 Simpler approach

The simpler way to reduce the hardware complexity of an FIR filter is to expand the equation above fully and combine all the $\pm x(n-k)$ terms which share the common POT coefficients such that,

$$y(n) = 2^{-1}(\dots 2^{-1}(2^{-1}(2^{-1}u_1 + u_2) + u_3) + \dots) + u_{16}$$

and

$$U[r] = \sum_{i=1}^{rj} X_i(n-k), \quad 0 \leq r \leq 15 \text{ and } 0 \leq k \leq 255$$

where,

- rj : # of terms to be shifted ($16-r$) times.
- 2^{-1} represents one right shift.

The proposed system will divide the operation into series of addition/subtraction and one bit shift. The above equations mean that we will only need single and small 1-bit shift register. This will reduce the area and complexity of hardware by significant amount.

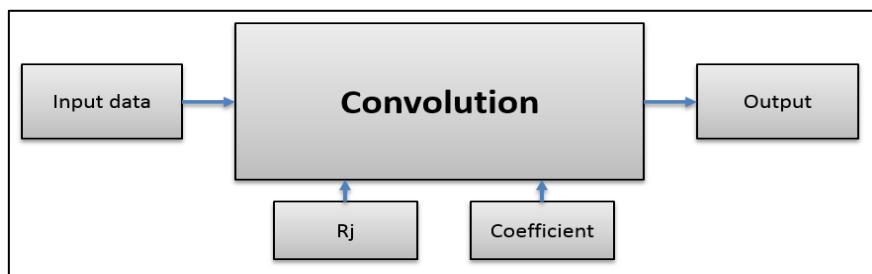


Figure 3: High-level schematic of the system

Figure 3 shows High level abstract of the MSDAP filter. It takes actual input data, R_j terms and coefficients as input. R_j terms are used to decide how many coefficients to be selected for the operation. Using this data, an array U_j ($j: 1 \rightarrow 16$) is created where $U[1]$ stores terms to be shifted 16 times, $U[2]$ stores terms to be shifted 15 times, till $U[16]$ that stores terms which needs to be shifted 1 time and added to generate output $Y[n]$ as shown in the equation below:

$$Y(n) = 2^{-1} \left(U[16] + \dots + 2^{-1} \left(U[4] + 2^{-1} \left(U[3] + 2^{-1} \left(U[2] + 2^{-1} \left(U[1] + 2^{-1} U[0] \right) \right) \right) \right) \right)$$

4. Input data formats

There are 3 kinds of input to the system of different bit widths. But when accepting them, all are accepted as 16 bit inputs. The frame format of each input data are discussed below.

4.1. Format of rj data

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Unused/ 0 Padded bits								MSB	Rj data				LSB		

Figure 4: Format of rj data

Figure 4 shows the format of the rj data frame. The value given by LSB 8 bit represents the number of coefficients to be selected from the coefficient memory.

4.2. Format of coefficient data

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Unused/ 0 Padded bits								Sign bit	MSB	Coefficient data				LSB	

Figure 5: Format of the coefficient data

Figure 5 shows the format of the coefficient data. The idea was to separate the sign bit from address bits. The sign bit is 9th bit (bit 8) and if it is one then it means that the digit created by LSB 8 bits is negative. The LSB 8-bits represents K value.

4.3. Format of the input data

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSB data														LSB	

Figure 6: Format of the input data

Figure 6 shows the format of the input data frame. Input data is 16 bit hence all bits in the frame are relevant.

5. System Specification and Pin interface

5.1. Pin Interface

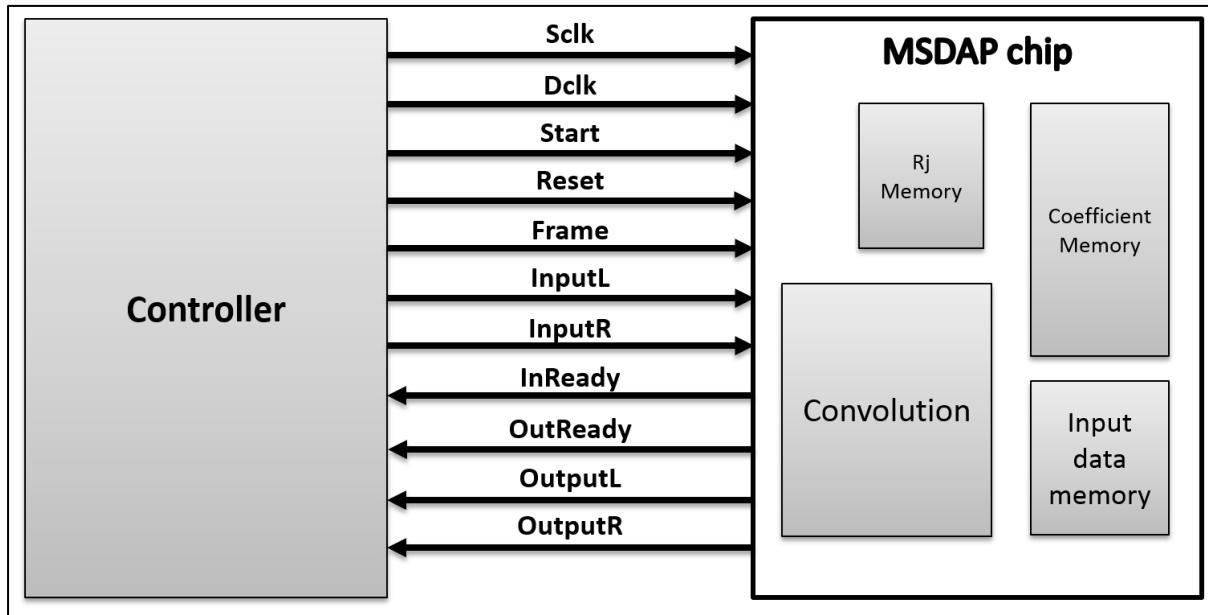


Figure 7: Interface and communication of MSDAP with controller

Figure 7 shows the interface of the MSDAP chip with the controller. Below is the brief description of each I/O pin that is connected to the chip

- Sclk: System clock for internal computation and output transmission.
- Dclk: Data clock for accepting serial input data.
- Start: Indicates the initial power on.
- Reset: A reset input.
- Frame: Indicates the beginning of the new relevant input.
- InputL/InputR: Input pins to accept the inputs on Left and Right channel.
- InReady: Signal to indicate the readiness of chip to accept the input.
- OutReady: Signal to indicate the readiness of the computed output.
- OutputL/OutputR: Output pins to send the serial outputs on Left and Right channel.

5.2. System specifications

1. FIR filter of the order of 256.
2. clocks:

The design is using two separate clocks.

- a. System clock of 26.88MHz.
 - System clock is used by controller to perform its internal operations. The system clock greatly helps in synchronization and overcome the issues related to synchronising. System clock is also used to send the output data (if ready) to the controller from the chip at every rising edge.
 - b. Data clock of 768kHz.
 - The sole purpose of data clock is to accept the inputs from the controller at each falling edge of after the 'Frame'.
3. An active high 'Start'
 - When high, this signal completely initializes the whole system for the first time when it is powered on.

4. Active low 'Reset'.
-Whenever a low signal is detected at the reset pin, the chip immediately resets. It comes out of the reset state only when high is detected at the same pin.
5. Active high InReady and OutReady signals.
-When the chip is ready to accept the input, it sets a high signal on InReady pin. Similarly when the chip has an output ready to be sent, it sets a high on the OutReady pin. OutReady signal is aligned with the rising edge of the Frame.
6. Dual channel input and output with LSB-first and MSB-last format.
-There are two separate pins to receive the inputs for left channel and right channel. Inputs are accepted serially in a format such that LSB is accepted first and MSB is accepted last. LSB is synchronized with rising edge of the Frame signal which is synchronized with data clock by controller. Frame signal is set high by the controller when it is sending the LSB of the data and it lasts for 1 data clock cycle.

6. Working

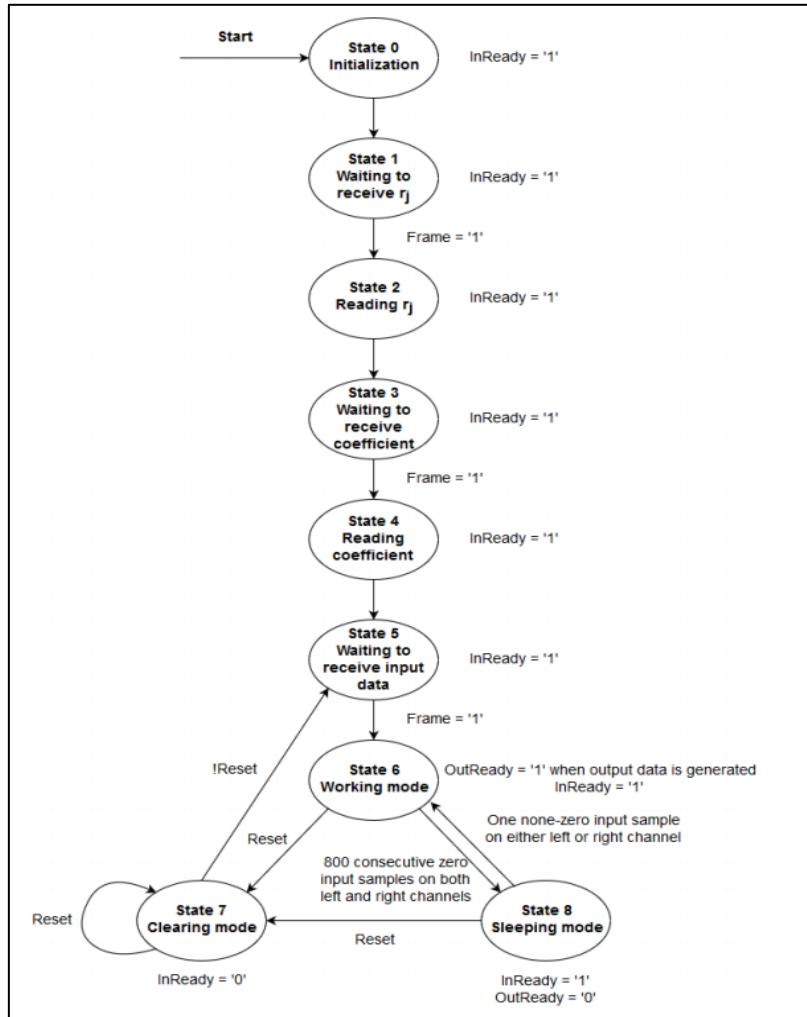


Figure 8: State Diagram

Figure 8 shows the internal state diagram of the MSDAP chip.

State0:

Upon reception of start signal, the system enters in state0 and clears Input, Rj and Coefficient memories. The clearing operation is performed in parallel and system enters into state1 after all memories are clear.

State1:

In state1, InReady signal goes high to indicate that the system is ready to receive Rj data and waits for the Frame signal from the controller. As soon as Frame signal goes high, the system changes its state to state2.

State2:

In state2, Inready signal is held high and the system starts accepting the incoming bits on left and right channel on every rising edge of the data clock cycle and stores them into Rj memory. As the input data is of 16 bits, this step is repeated 16 times before incrementing the pointer to accept next input on next Frame signal. Once all 16 Rj inputs are received on left and right channels, the system enters in state3.

State3:

In state3, InReady signal goes high (if it is low) to indicate that the system is ready to receive coefficient data and waits for the Frame signal from the controller. As soon as Frame signal goes high, the system changes its state to state4.

State4:

In state4, Inready signal is held high and the system starts accepting the incoming bits on left and right channel on every rising edge of the data clock cycle and stores them into coefficient memory. As the input data is of 16 bits, this step is repeated 16 times before incrementing the pointer to accept next input on next Frame signal. Once all 512 coefficient inputs are received on left and right channels, the system enters in state5.

State5:

In state5, InReady signal goes high (if it is low) to indicate that the system is ready to receive input data and waits for the Frame signal from the controller. As soon as Frame signal goes high, the system changes its state to state6.

State6:

In state6, Inready signal is held high and the system starts accepting the incoming bits on left and right channel on every rising edge of the data clock cycle and stores them into Input memory. As the input data is of 16 bits, this step is repeated 16 times before incrementing the pointer to accept next input on next Frame signal. While accepting the Inputs, the system also starts computation on the previously accepted input and if any output is ready to be sent, the OutReady signal is set high and the output which was computed while receiving the previous input is sent.

Table 1: Pipelining of accept, compute and send operations

Receive	Compute on	Send output of
X(n)		
X(n+1)	X(n)	
X(n+2)	X(n+1)	X(n)

The Table 1 shows pipelining of accept, compute and send operations, the system is accepting the input $x(n)$, while accepting this input the computation on $x(n-1)$ and sending of output $y(n-2)$ starts in parallel (Discussed later in section 8). The output is sent serially at the rate of system clock frequency with LSB first format as mentioned in the specification.

State7:

State7 is reset state, the system enters into this state on reception of a low signal on Reset pin regardless of the clock. In this state, the system suspends every operation what it was doing before coming to this state. The system disregards all the previously accepted inputs except R_j and coefficient data.

The system exits this state upon reception of a High signal on Reset pin and enters in state5 to initialize itself to accept input data as if it is accepting it for the first time.

State8:

The system enters into this state when 800 consecutive inputs are received on both left and right channel. In this state, InReady signal is held high and new inputs are continued to be accepted but not stored until a non-zero input is encountered on either channel. As soon as a non-zero input is detected, the system enters into state6 and accepts current input complete.

7. Architecture:

The behaviour of MSDAP was defined in section 5 and section 6 describes the whole operation of the chip in terms of a state machine. This whole operation is broken down into small modules each performing a definite unique task. A controller was designed to control the operations of all these modules and integrate them in such a way that all discrete modules work in synchronization.

The list of modules is as follows:

1. Serial-in Parallel-Out (SIPO) block
2. RJ memory
3. H memory
4. X memory
5. Arithmetic and Logic Unit(ALU)
6. Parallel-In Serial-Out (PISO)
7. Controller

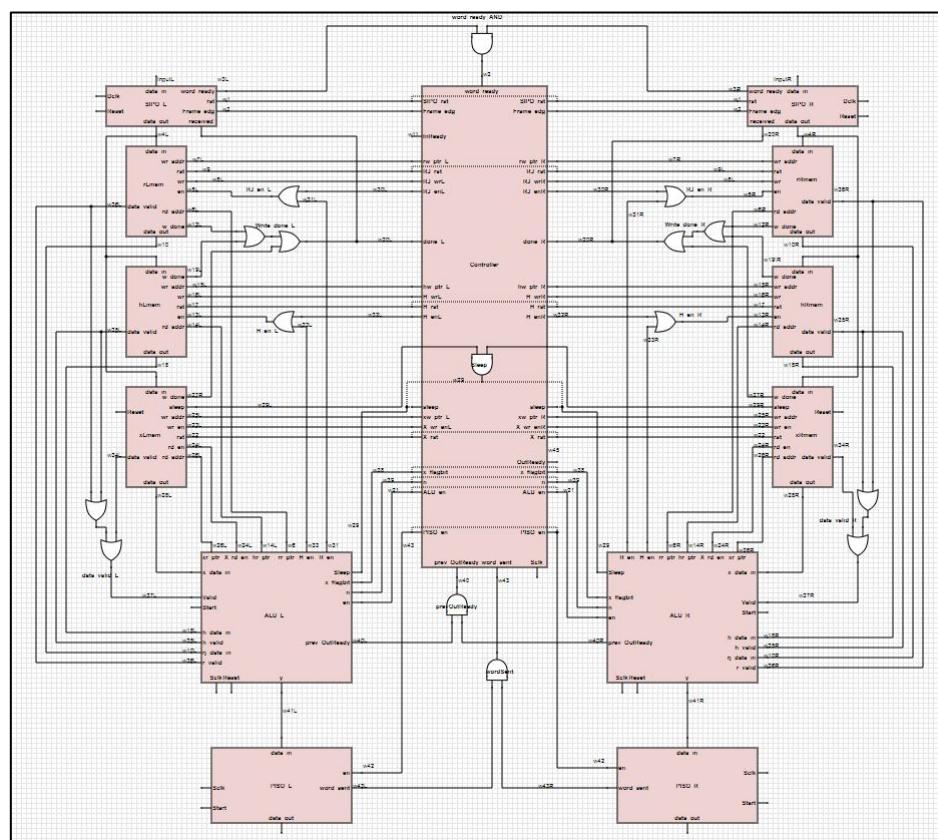


Figure 9: Complete architecture of MSDAP

Figure 13 shows the complete Architecture of the MSDAP. And table 2 shows all primary inputs and primary outputs of MSDAP. The primary inputs and outputs are used for integrating the chip to the outside world but, there are many internal signals that the modules use for internal communication. The main controller controls all these internal communications between modules and makes sure that all the operations are performed in synchronization.

Table 2: Primary input and outputs of MSDAP

Primary Inputs							Primary Outputs				
Sclk	Dclk	Start	Frame	Reset	InputL	InputR	InReady	OutReady	OutputL	OutputR	

7.1. Serial Input Parallel Output (SIPO):

Figure 14 shows SIPO module. This block serves as an interface for outside world to the MSDAP. MSDAP uses two SIPO modules for left and right channels. The primary inputs InputL and InputR are connected to left and right SIPOs respectively as shown in figure 14.

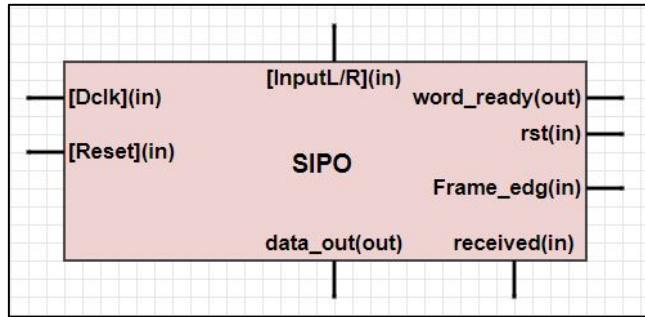


Figure 10: Serial in Parallel out (SIPO) module

Pin description:

- Dclk: This is a single bit clock pin.
- Reset: This is a single bit input pin. The reset signal of the complete system is connected to this pin.
- rst: This is a single bit input pin serves as local reset for SIPO.
- Frame_edg: This is a single bit pin serves as enable for SIPO.
- InputL/R: This is a single bit input data pin to accept input data.
- word_ready: This is a single bit output pin to indicate availability of a complete word.
- data_out: This is a 16 bit output data port to send the output data.
- received: This is a single bit input pin to acknowledge the reception of the data.

Operation:

SIPO module is used for serial to parallel conversion of the input data. The Frame_edg signal serves as an enable signal. As long as this signal is high, SIPO samples data on the input pin at every falling edge of Dclk, the data is in LSB-first and MSB-last format. Once all 16 bits of the data are received, the data is kept on output buffer and word_ready signal is made high to indicate availability of complete data. This signal stays high until a high on received pin is detected. A low on 'Reset' pin initializes the SIPO module and a high on 'rst' pin clears the internal data register as well as output buffer.

7.2. RJmem (RJ memory):

A 16x16 memory is used to store the RJ data. MSDAP uses two RJ memory blocks, RJmemL and RJmemR to store the RJ data for left and right channels respectively. Figure 15 shows RJ memory module.

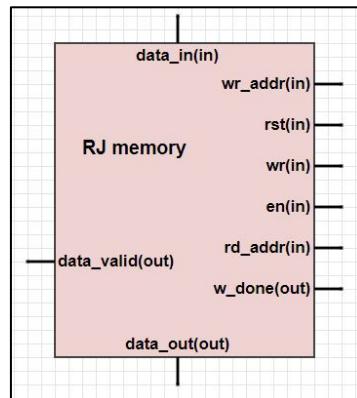


Figure 11: RJ memory

Pin description:

- rst: This is a single bit reset pin.
- en: This is a single bit input pin serves as enable.
- wr: This is a single bit input pin to control the read/write operation
- wr_addr: This is a 4 bit input port to get a memory location to write the data.
- data_in: This is a 16 bit input data port to receive the input data.
- w_done: This is a single bit output pin to indicate completion of a write operation.
- rd_addr: This is a 4 bit input port to get a memory location to read the data.
- data_out: This is a 16 bit output data port to send the output data.
- data_valid: This is a single bit output pin to indicate validity of the data on the output port.

Operation

The RJ memory is used for storing the RJ data. When a high on the enable (en) pin is detected, the RJ memory starts its operation depending upon the condition specified by wr and rst signals. When 'wr' is high, the data present on the data_in port is written to the memory location indicated by the 'wr_addr' port and 'w_done' signal is made high to indicate the completion of the write operation. When wr is low, the data from the memory location indicated by 'rd_addr' port is made available on the 'data_out' port and 'data_valid' signal is made high to indicate the availability of valid data on the 'data_out' port. When 'rst' is high, the memory location indicated by the 'wr_addr' is cleared and 'w_done' signal is made high. The 'data_valid' and 'w_done' signals are made low when enable goes down.

7.3. Hmem (H coefficient memory):

A 16x512 memory is used to store the H coefficient data. MSDAP uses two H memory blocks, HmemL and HmemR to store the H data for left and right channels respectively. Figure 16 shows H memory module.

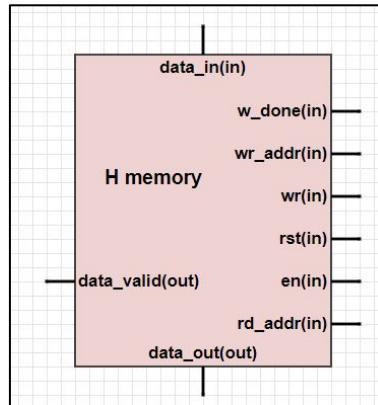


Figure 12: H coefficient memory

Pin description:

- rst: This is a single bit reset pin.
- en: This is a single bit input pin serves as enable.
- wr: This is a single bit input pin to control the read/write operation
- wr_addr: This is a 4 bit input port to get a memory location to write the data.
- data_in: This is a 16 bit input data port to receive the input data.
- w_done: This is a single bit output pin to indicate completion of a write operation.
- rd_addr: This is a 4 bit input port to get a memory location to read the data.
- data_out: This is a 16 bit output data port to send the output data.
- data_valid: This is a single bit output pin to indicate validity of the data on the output port.

Operation:

The H memory is used for storing the H coefficient data. When a high on the enable (en) pin is detected, the H memory starts its operation depending upon the condition specified by wr and rst signals. When 'wr' is high, the data present on the data_in port is written to the memory location indicated by the 'wr_addr' port and 'w_done' signal is made high to indicate the completion of the write operation. When wr is low, the data from the memory location indicated by 'rd_addr' port is made available on the 'data_out' port and 'data_valid' signal is made high to indicate the availability of valid data on the 'data_out' port. When 'rst' is high, the memory location indicated by the 'wr_addr' is cleared and 'w_done' signal is made high. The 'data_valid' and 'w_done' signals are made low when enable goes down.

7.4. Xmem (X memory):

A 16x256 memory is used to store the X input data. MSDAP uses two X memory blocks, XmemL and XmemR to store the X input data for left and right channels respectively. Figure 17 shows X memory module.

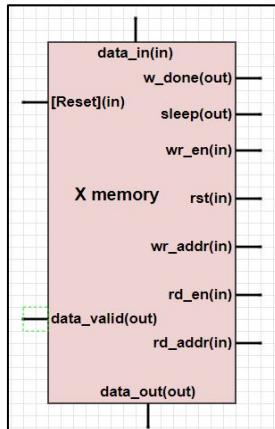


Figure 13: X memory

Pin description:

- Reset: This is a single bit system reset pin.
- rst: This is a single bit local reset pin.
- wr_en: This is a single bit input pin serves as enable for write operation.
- wr_addr: This is an 8 bit input port to get a memory location to write the data.
- data_in: This is a 16 bit input data port to receive the input data.
- w_done: This is a single bit output pin to indicate completion of a write operation.
- sleep: This is a single bit output pin to indicate sleep condition.
- rd_en: This is a single bit input pin serves as enable for read operation.
- rd_addr: This is an 8 bit input port to get a memory location to read the data.
- data_out: This is a 16 bit output data port to send the output data.
- data_valid: This is a single bit output pin to indicate validity of the data on the output port.

Operation:

The X memory is used for storing the X input data. This module is designed slightly differently as compared to other two memories discussed before. There are two individual enable signals for read and write operations therefore enable parallel read and write operation. When a high on the 'wr_en' pin is detected, the X memory starts write operation and the data present on the 'data_in' port is written to the memory location indicated by the 'wr_addr' port and 'w_done' signal is made high to indicate the completion of the write operation. The consecutive 800 zero inputs enable the sleep condition and sleep signal is made high along with 'w_done'. Sleep signal stays high until a non-zero input is received. When a high on 'rd_en' pin is detected, the data from the memory location indicated by 'rd_addr' port is made available on the 'data_out' port and 'data_valid' signal is made high to indicate the availability of valid data on the 'data_out' port. When 'rst' is high, the memory location indicated by the 'wr_addr' is cleared and 'w_done' signal is made high. The 'data_valid' and 'w_done' signals are made low when enable goes down.

7.5. ALU (Arithmetic Logic Unit):

An ALU module is used to perform mathematical and logical operations. MSDAP uses two ALU blocks, ALU_L and ALU_R to operate on inputs on left and right channels respectively. Figure 18 shows ALU module.

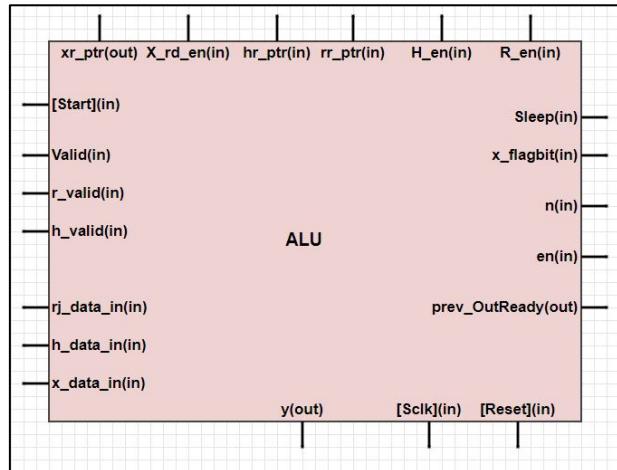


Figure 14: Arithmetic and Logic unit (ALU)

Pin description:

- Start: This is a single bit input pin to initialize the system.
- Reset: This is a single bit system reset pin.
- Sclk: Single bit clock pin connected to Sclk
- en: This is a single bit input pin serves as enable signal.
- rr_ptr: This is a 4 bit output port to provide a RJ memory location to read the data.
- R_en: This is a single bit output pin to enable RJ memory.
- r_valid: This is a single bit input pin to check validity of data at the output of RJ memory.
- rj_data_in: This is a 16 bit input port to read RJ data.
- hr_ptr: This is a 9 bit output port to provide an H memory location to read the data.
- H_en: This is a single bit output pin to enable H memory.
- h_valid: This is a single bit input pin to check validity of data at the output of H memory.
- h_data_in: This is a 16 bit input port to read H data.
- x_flagbit: This is a single bit input pin to recognize more than 256 Xs have been read.
- n: This is an 8 bit input port pointing to the address of the most recent X data.
- xr_ptr: This is an 8 bit output port to provide an X memory location to read the data.
- X_rd_en: This is a single bit output pin to enable X memory for reading.
- x_data_in: This is a 16 bit input port to read X data.
- Valid: This is a single bit input signal for memory enable control.
- y: This is a 40 bit output data port to provide output of ALU.
- prev_OutReady: This is a single bit output port to indicate a valid output is ready at ALU.
- sleep: This is a single bit input port to acknowledge the sleep mode.

Operation:

The ALU initializes at 'Start' and 'Reset' signal and normally operates at 'Sclk' frequency. When a high at 'en' and a low at 'sleep' is detected, a command to read first RJ data is sent by making 'rr_ptr' point at 0th location and 'RJ_en' high. After reading first RJ, required number of H coefficients are read at every positive edge of Sclk cycle by making 'hr_ptr' point at 0th location (and incrementing by 1 before each Sclk cycle) of H memory and 'H_en' high. Once, required number read on H memory, new RJ data is read and this process continues as long as valid RJ and H data are available. After each 'H_data' read, an address of X memory is calculated using 'H_data' and 'n' and X data is read by making 'xr_ptr' to

point at this address and ‘X_rd_en’ high. Of course, a validity check for ‘xr_ptr’ is done prior to this and X data is read only if this address is valid. The ‘add and shift’ operations are performed on this ‘x_data’ and final output is sent on ‘y’ port. ‘prev_OutReady’ is made high to indicate a valid output is ready at the output of ALU. When a high is detected at ‘sleep’ input, ALU does none of the above operations and keeps ‘prev_OutReady’ low if ‘en’ is high.

7.6. Parallel In Serial Out (PISO):

Figure 19 shows PISO module. This block serves as an interface for outside world from the MSDAP. MSDAP uses two PISO modules for left and right channels. The primary outputs OutputL and OutputR are connected to left and right PISOs respectively as shown in figure 19.

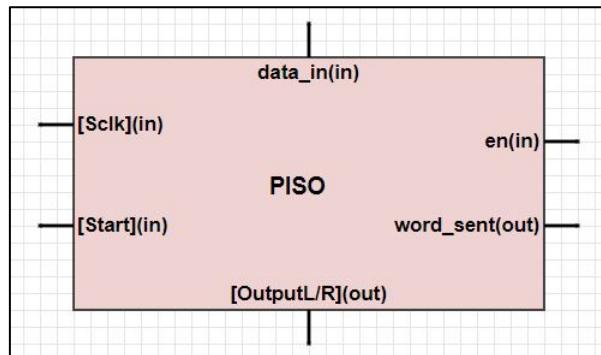


Figure 15: Parallel In Serial Out (PISO) module

Pin description:

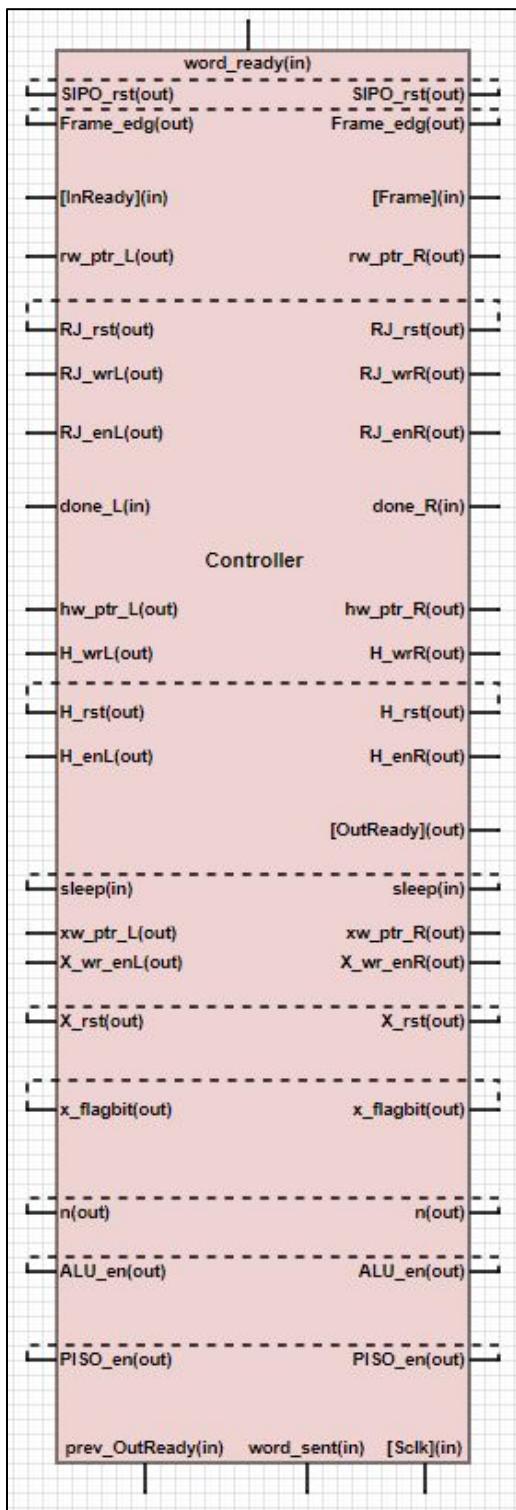
- Start: This is a single bit input pin to initialize the PISO.
- Sclk: This is a single bit clock pin.
- en: This is a single bit input pin serves as enable for PISO.
- data_in: This is a 16 bit output data port to accept input data.
- word_sent: This is a single bit output pin to indicate end of transmission of a complete word.
- OutputL/R: This is a single bit output data port to send the output data.

Operation:

PISO module is used for parallel to serial conversion of the input data. A high on ‘Start’ pin initializes the PISO module. As long as the signal on ‘en’ pin is high, PISO registers the data present on the input pin, the data is registered in parallel fashion i.e. all bits at once. PISO sends this data from the output pin serially at every positive edge of ‘Sclk’. This data is sent in LSB-first and MSB-last format. Once all 16 bits of the data are sent, ‘word_sent’ signal is made high to indicate the completion of transmission of complete data. This signal stays high until a low on ‘en’ pin is detected. The controller makes sure that enable ‘en’ signal of PISO goes low as soon as it receives ‘word_sent’.

7.7. Controller:

A controller module is required to control the operations of all the other modules discussed in this section. The state machine discussed in section 6 is present inside the controller and it makes sure that the sequence of operations performed by the system is right by triggering right module in right state in proper sequence. Figure 20 shows the only controller module present in MSDAP.



Pin description

- Sclk: Single bit clock pin connected to Sclk
- Start: This is a single bit input pin to initialize the system.
- Reset: This is a single bit system reset pin.
- InReady: This is a single bit output pin to indicate the system is ready to take inputs
- Frame: This is a single bit input pin to recognize the start of a valid word
- SIPO_rst: This is a single bit output pin to reset the SIPO module.
- Frame_edg: This is a single bit output pin to enable the SIPO module
- word_ready: This is a single bit input pin to recognize the word is ready at the output of SIPO
- RJ_rst: This is a single bit output pin to clear RJ memory.
- RJ_enL and RJ_enR: These are two single bit output pins to enable the two RJ memories.
- RJ_wrL and RJ_wrR: These are the two single bit output pins to control read and write operations on two RJ memories.
- rw_ptr_L and rw_ptr_R: These are the two 4 bit output ports to provide an RJ memory address location for write operation.
- H_rst: This is a single bit output pin to clear H memory.
- H_enL and H_enR: These are two single bit output pins to enable the two H memories.
- H_wrL and H_wrR: These are the two single bit output pins to control read and write operations on two H memories.
- hw_ptr_L and hw_ptr_R: These are the two 9 bit output ports to provide an H memory address location for write operation.
- X_rst: This is a single bit output pin to clear X memory.
- xw_ptr_L and xw_ptr_R: These are the two 8 bit output ports to provide an X memory address location for write operation.

Figure 16: Controller module

X_wr_enL and **X_wr_enR**: These are the two single bit output pins to enable a write operation on X memory
done_L and **done_R**: These are the two single bit input pins to recognize the completion of write operation on memories.
ALU_en: This is a single bit output pin to enable the ALU.
x_flagbit: This is a single bit output pin to indicate more than 256 Xs have been read.
n: This is an 8 bit output port pointing to the address of most recent X data.
Prev_OutReady: This is a single bit input pin to recognize the availability of the output at the output port of ALU.
OutReady: This is a single bit primary output pin to indicate the availability of the output to be sent.
PISO_en: This is a single bit output pin to enable the PISO module.
word_sent: This is a single bit input pin to recognize the end of transmission of a complete word.
sleep: This is a single bit input port to acknowledge the sleep mode.

Operation:

As mentioned earlier, the controller controls the operation of the complete system using a state machine discussed in section 6. The controller initializes all the internal registers at ‘Start’ signal and normally operates at ‘Sclk’ frequency. The controller makes sure that the system will start from ‘State0’ after ‘Start’ signal goes low. In this state ‘SIP0_rst’ signal, and all the memory clear signals (**RJ_rst**, **H_rst**, **X_rst**) are held high. All the memory address pointers (**rw_ptrL/R**, **hw_ptrL/R**, **xw_ptrL/R**) are incremented at every rising edge of the ‘Sclk’ sequentially from 0 to the final value. All the memory enable signals ‘**RJ_enL/R**, **H_enL/R**, **X_wr_enL/R**’ are made high at every rising edge of ‘Sclk’ to enable the memories to perform the memory clear operations. The memory enable signals are made low as soon as the memory location specified in that clock cycle is cleared. After clearing all the memories, the controller puts a high on ‘InReady’ pin to indicate that the system has been initialized and ready to receive the inputs. The controller makes the system enters into ‘State1’ and waits for the ‘Frame’ signal. Once a high on ‘Frame’ is recognized, ‘Frame_edg’ signal is made high to enable the SIPO to start its operation. The system is made to enter into state two and waits for ‘word_ready’ signal from both SIPO_L and SIPO_R. The ‘**RJ_wrL/R**’ and ‘**RJ_enL/R**’ signals are made high when a high on ‘word_ready’ is detected. This enables the RJ memories to write the word which is present at the output of SIPOL/R to the memory location specified by ‘**rw_ptrL/R**’. The controller makes sure that ‘**rw_ptrL/R**’ starts from 0 and increments before each write operation. ‘Frame_edg’ is made low as soon as ‘word_ready’ is detected and ‘**Rj_enL/R**’ are made low as soon as a high on ‘doneL/R’ is detected. Once all the RJ values are written, the system is made to enter into ‘State3’. In this state, ‘**RJ_wrL/R**’ signals are made low and system waits for ‘Frame’ signal. Once ‘Frame’ is detected, the system enters into ‘State4’ where the acceptance of H coefficient starts. The H memory is written in the same fashion as RJ memory in ‘State2’, with the help of all H memory related pins i.e. ‘**H_enL/R**’, ‘**H_wrL/R**’, and ‘**hw_ptrL/R**’. Once all the H coefficients are written, the system enters into ‘State5’. In this state, ‘**H_wrL/R**’ is made low and the system waits for the ‘Frame’ signal. Once a high on ‘Frame’ is detected, the system enters into ‘State6’ where the acceptance of X data starts. Again this X data is written in same fashion as RJ values in ‘State2’ and H coefficients in ‘State4’ with the help of all the X memory related pins i.e. ‘**xw_enL/R**’, and ‘**xw_ptr_I/R**’. ‘**x_flagbit**’ goes high after accepting 257 X data to indicate more than 256 X data have been accepted and ‘n’ points to the address of the most recent X data available in X memory. As discussed in section 6, computation can be started after accepting at least one complete input, therefore ‘**ALU_en**’ is set high on the rising edge of second ‘Frame’ signal. ALU module starts its operation based on the address pointed by ‘n’ and the condition of ‘**x_flagbit**’ pin. ALU completes its operation before next ‘Frame’ where controller checks for ‘**prev_OutReady**’ signal. If a high is detected on ‘**prev_OutReady**’ then ‘**OutReady**’ signal is set high by the controller along with ‘**PISO_en**’ signal. This informs the test bench that a valid output is ready at

the primary output pins ‘OutputL/R’ and PISO starts its operation due to ‘PISO_en’ signal. The ‘OutReady’ and ‘PISO_en’ signals go low on detection of ‘word_sent’ from PISO. In ‘State6’, if a high is detected on ‘sleep’ pin, then the system enters into ‘State8’. In this state, the system keep accepting the input but won’t calculate anything i.e. ‘Frame_edg’ is set high on every ‘Frame’ but ‘ALU_en’ will be low. A low on ‘sleep’ pin makes the system to enter into ‘State5’ from ‘State8’ and normal operation continues as if it is entering ‘State5’ for the first time. When a ‘low’ is detected on ‘Reset’ pin, then the system enters into ‘State7’ which is Reset state and the complete system gets re-initialized. A high on ‘Reset’ puts the system into ‘State5’ and normal operation will be continued as if it is coming to ‘State5’ for the first time.

8. RTL design Simulation:

Following the ASIC design flow explained in section 2 the next step after architecture design is, RTL design. We developed a RTL level Verilog code for the whole MSDAP discussed above. The functional correctness of this RTL code can be verified in terms of waveforms.

Transition to ‘State0’:

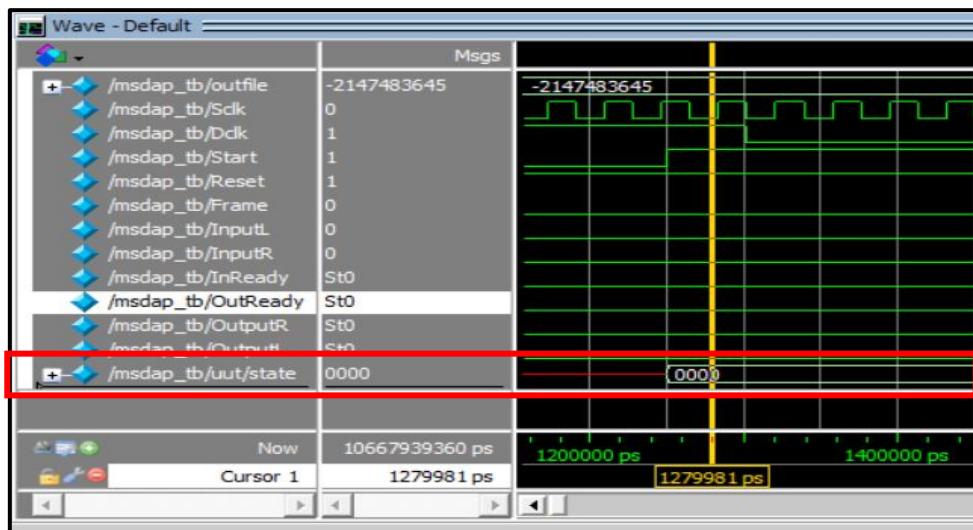


Figure 17: Transition to ‘State0’

As discussed in section 6 system enters into ‘State0’ on reception of ‘Start’ signal. The figure 17 shows the transition to ‘State0’.

Transition from ‘State0’ to ‘State1’ and ‘State1’ to ‘State2’:

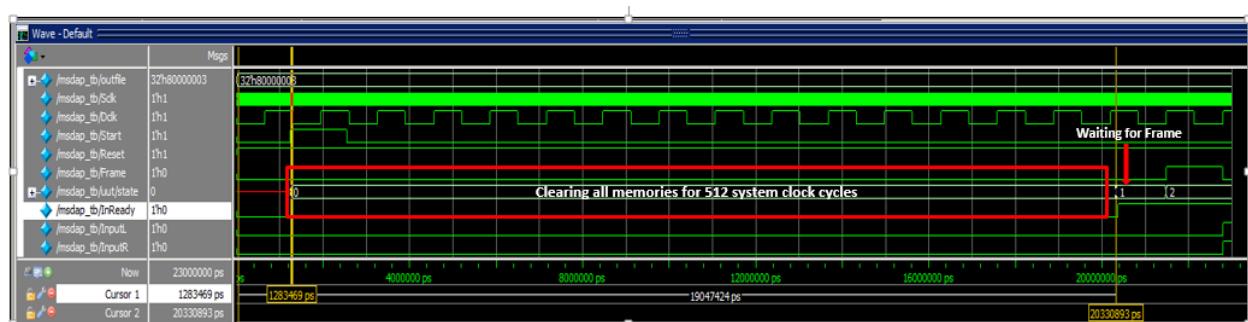


Figure 18: Transition from ‘State0’ to ‘State1’ and ‘State1’ to ‘State2’

The system clears all the memories in ‘State0’. ‘InReady’ signal goes high after clearing all the memories and the system enters into ‘State1’ to wait for the Frame signal. The state changes to ‘State2’ when ‘Frame’ signal goes high. This transition is shown in figure 18.

Transition from ‘State2’ to ‘State3’ and ‘State3’ to ‘State4’:

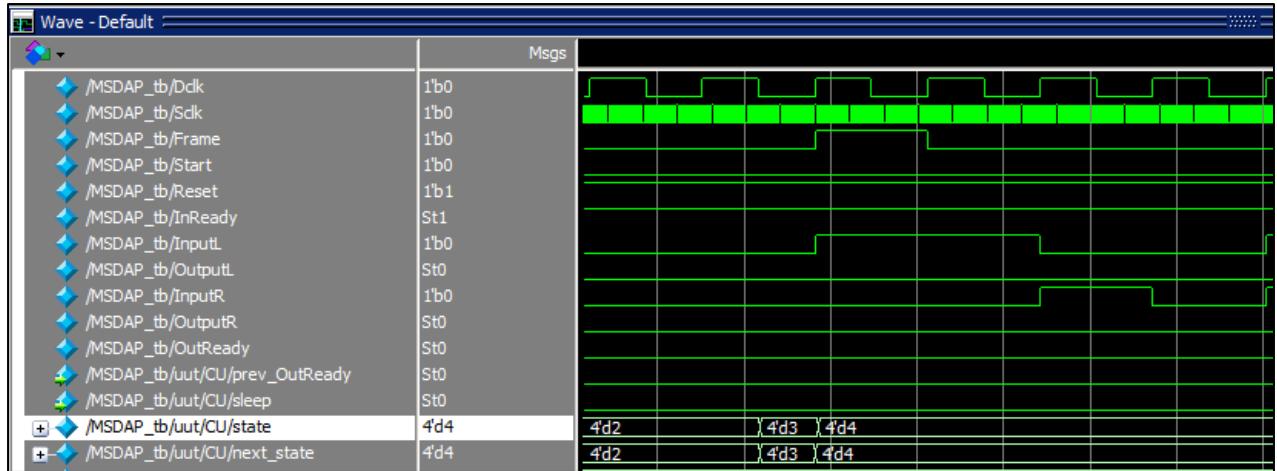


Figure 19: Transition from ‘State2’ to ‘State3’ and ‘State3’ to ‘State4’

In ‘State2’, the system accepts RJ values and after accepting all 16 RJ values, the system enters into ‘State3’ to wait for next ‘Frame’. The system enters into ‘State4’ as soon as ‘Frame’ is detected. This transition is shown in figure 19.

Transition from ‘State4’ to ‘State5’ and ‘State5’ to ‘State6’:

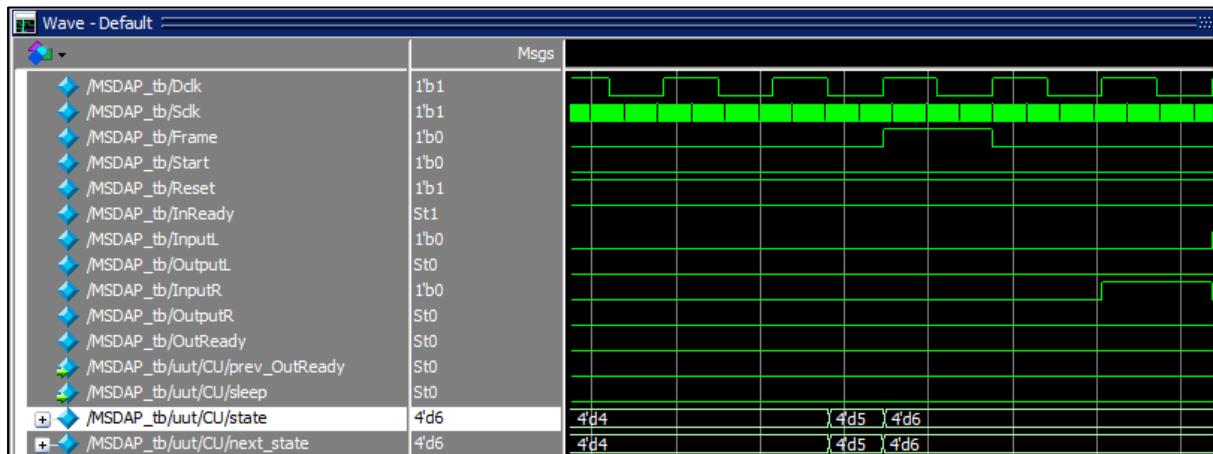


Figure 20: Transition from ‘State4’ to ‘State5’ and ‘State5’ to ‘State6’:

In ‘State4’, the system accepts H coefficients and after accepting all 512 H coefficients, the system enters into ‘State5’ to wait for next frame. The system enters into ‘State6’ as soon as ‘Frame’ is detected. This transition is shown in figure 20.

Computation and parallel operations:

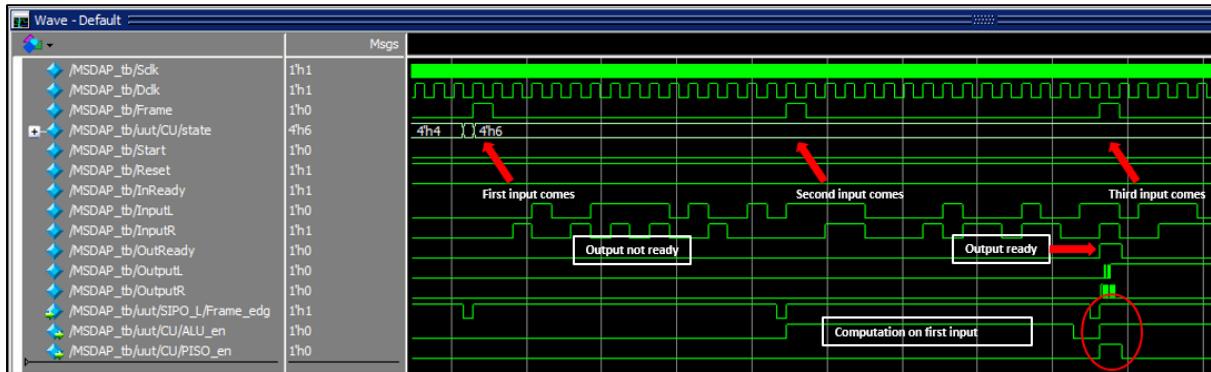


Figure 21: Parallelization of operations

The figure 21 shows transitions on ‘Frame_edg’, ‘ALU_en’, and ‘PISO_en’ signals to enable SIPO, ALU and PISO modules. It can be seen that SIPO is enabled at every ‘Frame’ signal to accept the inputs on ‘InputL/R’. ALU is not enabled until the acceptance of at least one complete input. ALU does its computation on X(0) while accepting the second input X(1). PISO is enabled to send the output Y(0) along with ALU to operate on X(1) while accepting the third input X(2). All these are now parallelized from third input as all modules are enabled at the same time.

Reset state:

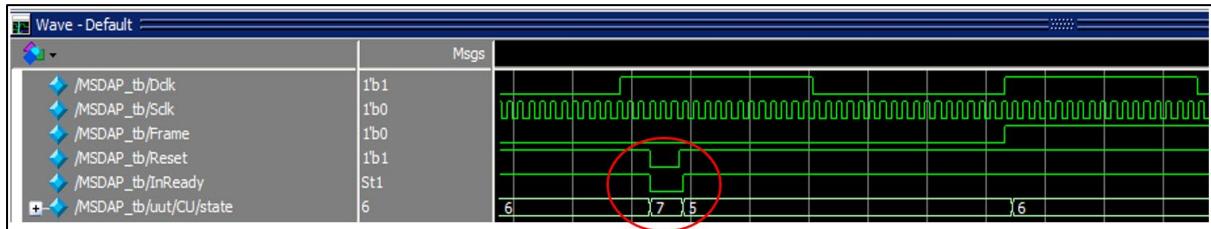


Figure 22: Transition to reset state

‘State7’ is a synchronous active low reset state, the system enters into ‘State7’ as soon as the signal on the ‘Reset’ pin goes low. The system enters into ‘State5’ when reset goes high again. This transition is shown in figure 22.

Sleep mode:

The system enters into sleep mode i.e. ‘State8’ when ‘sleep’ signal on the controller goes high. The sleep signal on the controller is the logical ‘and’ of sleep signals coming from X memories of both the channels as shown in figure 9. This ‘and’ operation makes sure, the sleep mode is entered if and only if both memories have detected 800 consecutive zero inputs. The system wakes up from sleep mode when any one of the memories receive a non-zero input. Figure 23 shows desirable situation and figures 24, 25 show undesirable situations to enter into sleep mode respectively. Figure 26 shows wake up behaviour of the system.

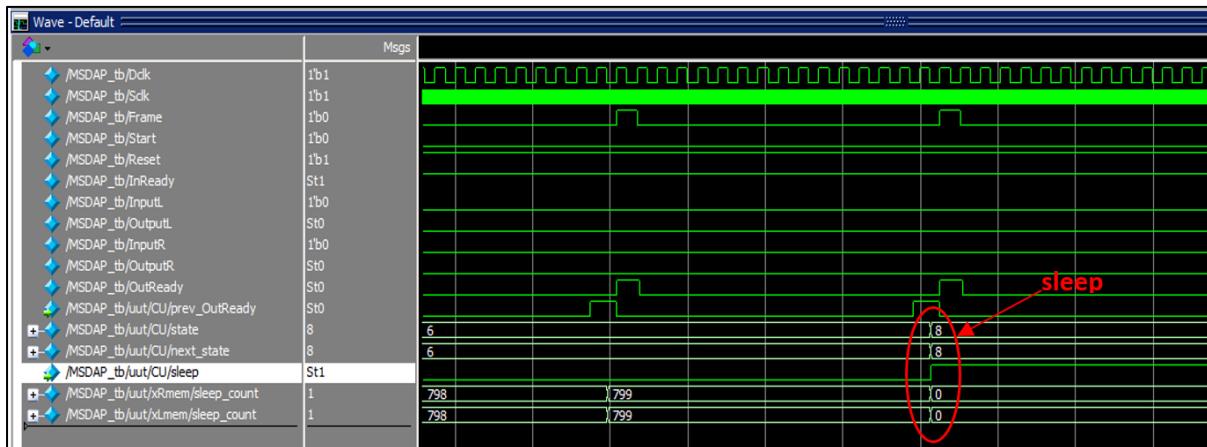


Figure 23: Both memories count 800 zeros at the inputs

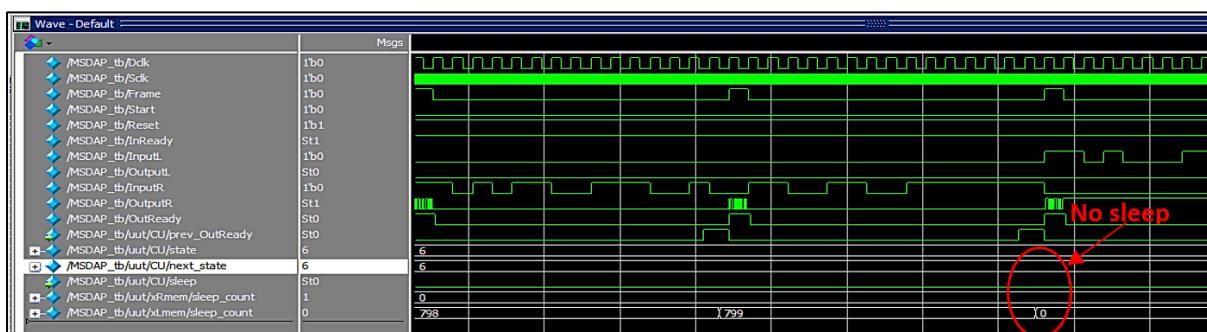


Figure 24: Only Left channel memory counts 800 zeros at the input

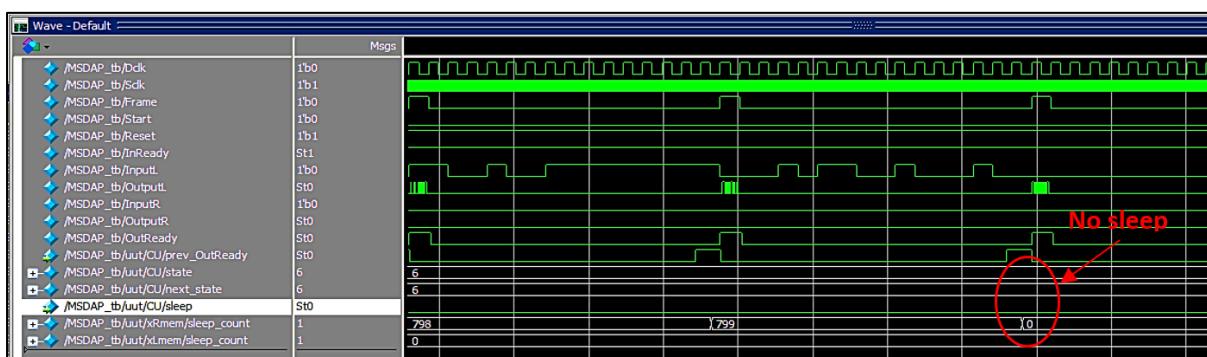


Figure 25: Only right channel memory counts 800 zeros at the input

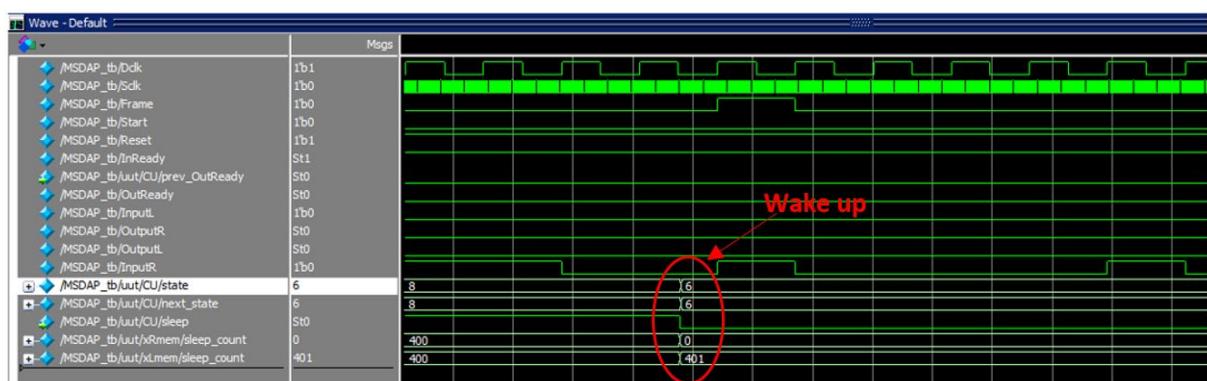


Figure 26: Right channel memory receives a non-zero input, wake up!

9. RTL design synthesis:

After verifying the functionality of the system, the RTL code is synthesized to generate a gate level netlist. This synthesis is performed using a design compiler, which takes the RTL code and target library as input and maps the functionality of the entire system using the cells present inside the library. A netlist is generated which describes this entire mapping as another verilog code. A part of the synthesis report is shown in figure 27 to show that the synthesis was successful. Complete synthesis report is attached in Appendix A.

```
Optimization Complete
-----
1
Current design is 'top_level'.
design_vision>
```

Figure 27: Completion of Synthesis

The figure 28 shows the top level schematic of complete system. It can be seen that all the primary input and out pins have been synthesized correctly.

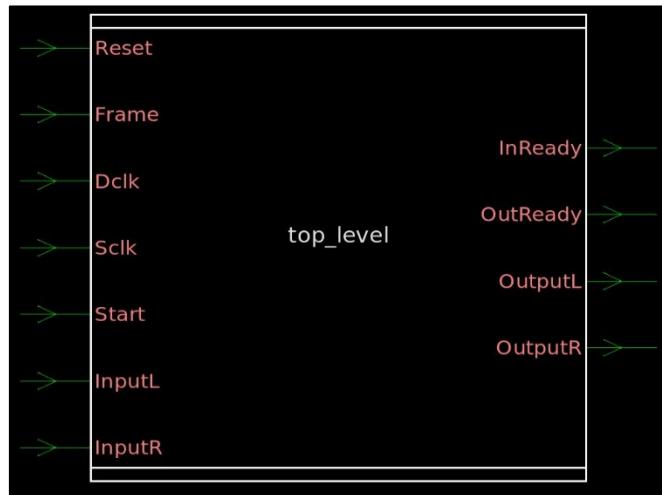


Figure 28: Top level schematic of MSDAP

The figure 29 shows complete architecture of MSDAP after synthesis. It can be seen that the schematic discussed in section 7 matches exactly with the schematic generated by design compiler.

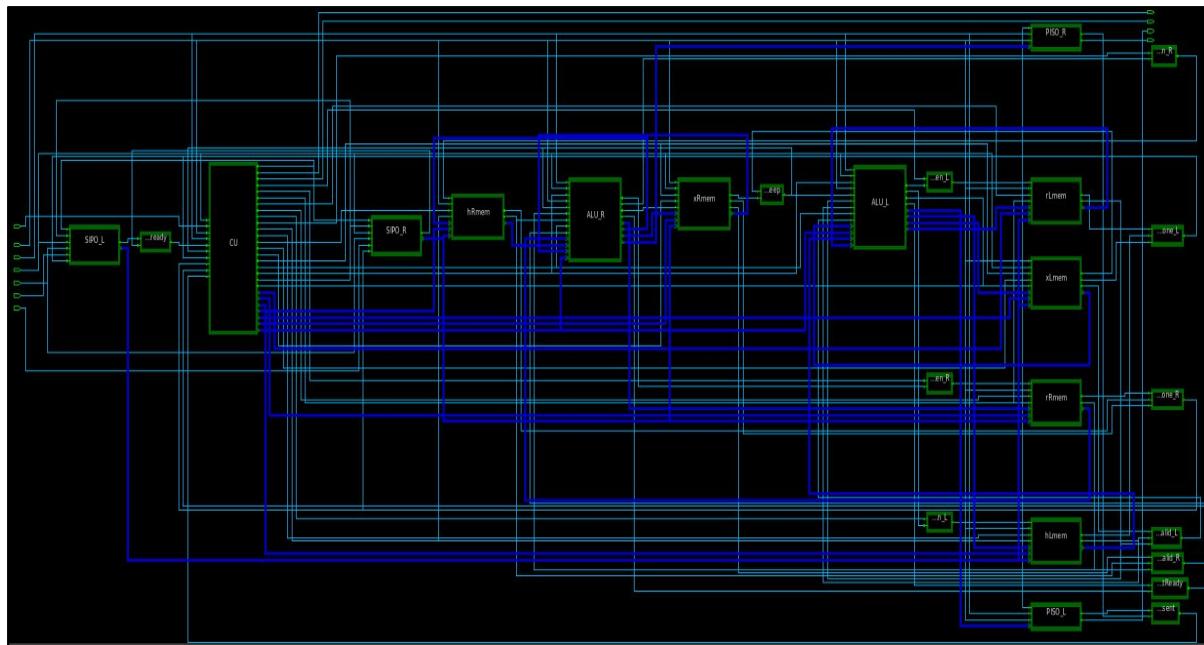


Figure 29: architecture of complete MSDAP after synthesis

To show the correct synthesis of each functional block, the top level schematics of all individual blocks are shown below in figures 30 to 36. These schematics match exactly with the blocks discussed in section 7. The internal circuitry of each of these block is attached in Appendix B.



Figure 30: Top Level Schematic of SIPO



Figure 31: Top Level Schematic of R memory



Figure 32: Top level Schematic of H memory



Figure 33: Top Level Schematic of X memory



Figure 34: Top level Schematic of PISO

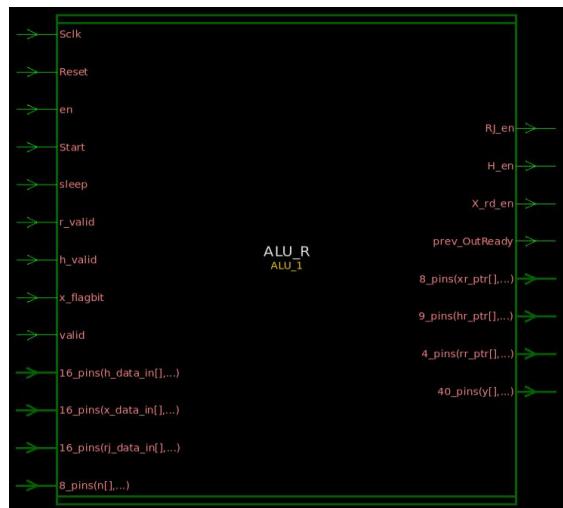


Figure 35: Top level Schematic of ALU

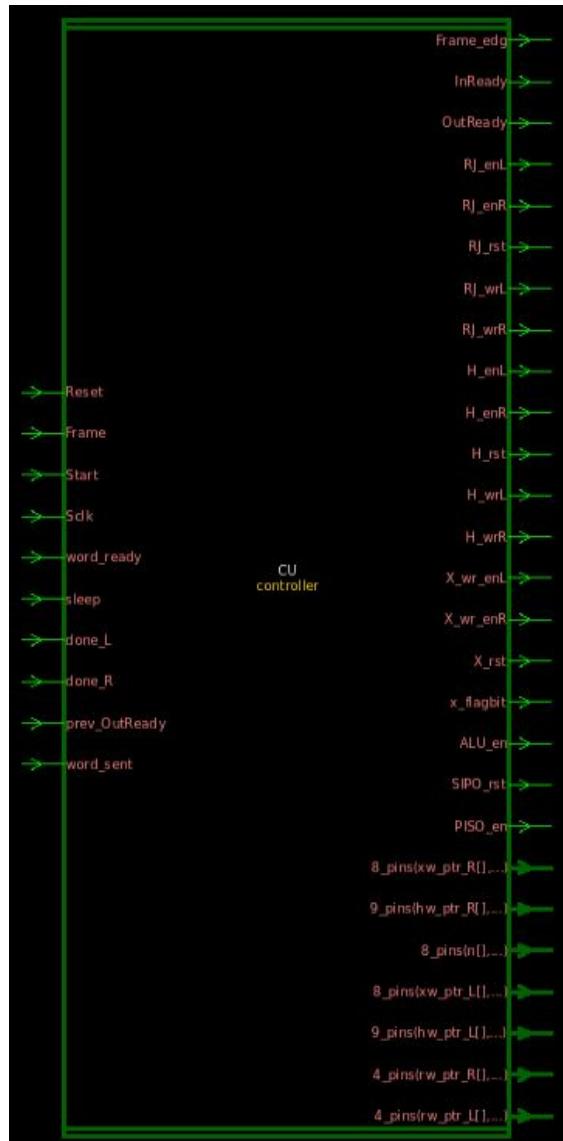


Figure 36: Top Level Schematic of Controller

10 Critical Path Delay

Critical path is the longest delay path in the circuit. This delay defines the operating clock frequency of the entire system. After synthesis, design compiler can provide this critical path and the delay of this path. The figure 37 shows critical path generated by design compiler (DC) for our version of MSDAP architecture. A complete quality of report generated by DC is shown in figure 38 and it can be seen that the slack for both the clocks is positive and the design is meeting all the timing constraints. All timing, cell, and area reports are provided in Appendix C.

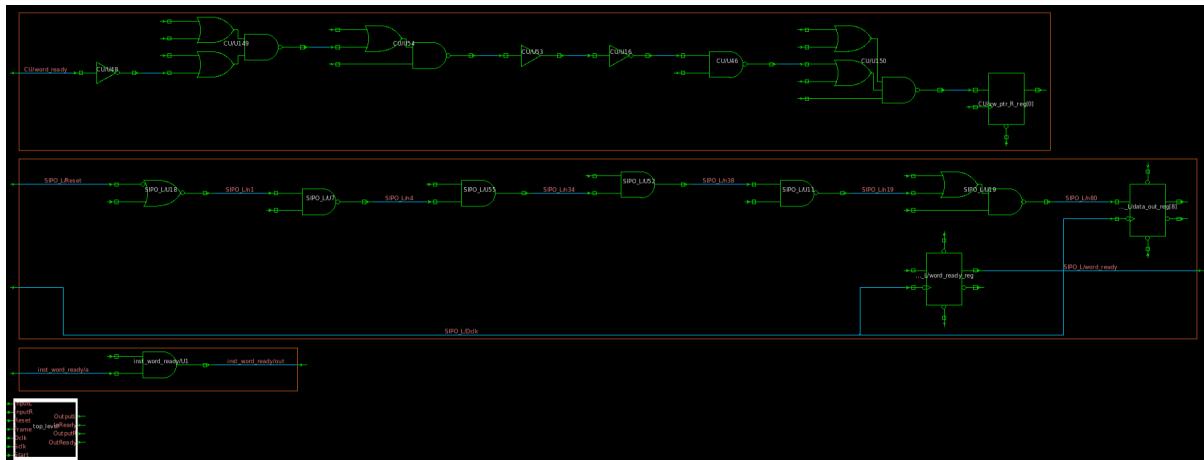


Figure 37: Critical path in MSDAP

```
1 ****
2 ****
3 Report : gqr
4 Design : top_level
5 Version: O-2018.06-SP1
6 Date   : Thu Dec 13 20:38:38 2018
7 ****
8
9
10 Timing Path Group 'Dclk'
11 -----
12 Levels of Logic:          6.00
13 Critical Path Length:    1.32
14 Critical Path Slack:     15.74
15 Critical Path Clk Period: 1302.08
16 Total Negative Slack:    0.00
17 No. of Violating Paths:  0.00
18 Worst Hold Violation:   0.00
19 Total Hold Violation:   0.00
20 No. of Hold Violations: 0.00
21
22
23 Timing Path Group 'Sclk'
24 -----
25 Levels of Logic:          8.00
26 Critical Path Length:    2.49
27 Critical Path Slack:     15.83
28 Critical Path Clk Period: 37.20
29 Total Negative Slack:    0.00
30 No. of Violating Paths:  0.00
31 Worst Hold Violation:   0.00
32 Total Hold Violation:   0.00
33 No. of Hold Violations: 0.00
34
35
36
37 Cell Count
38 -----
39 Hierarchical Cell Count:  41
40 Hierarchical Port Count: 1572
41 Leaf Cell Count:        54275
42 Buf/Inv Cell Count:    6990
43 Buf Cell Count:         6549
44 Inv Cell Count:         441
45 CT Buf/Inv Cell Count: 0
46 Combinational Cell Count: 28548
47 Sequential Cell Count: 25727
48 Macro Count:            0
49
50
51
52 Area
53 -----
54 Combinational Area: 339573.287809
55 Noncombinational Area: 745162.824894
56 Buf/Inv Area: 60409.707876
57 Total Buffer Area: 57505.46
58 Total Inverter Area: 2904.25
59 Macro/Black Box Area: 0.000000
60 Net Area: 0.000000
61
62
63 Cell Area: 1084736.112703
64 Design Area: 1084736.112703
65
66
67 Design Rules
68 -----
69 Total Number of Nets: 54604
70 Nets With Violations: 0
71 Max Trans Violations: 0
72 Max Cap Violations: 0
73
74
75
76 Hostname: engnx11.utdallas.edu
77
78 Compile CPU Statistics
79 -----
80 Resource Sharing: 32.53
81 Logic Optimization: 69.64
82 Mapping Optimization: 89.29
83
84 Overall Compile Time: 229.15
85 Overall Compile Wall Clock Time: 230.24
86
```

Figure 38: Complete QOR report by DC

11. Physical Design of MSDAP

After the synthesis part is done, the next step in the ASIC design flow is Physical Design. In this step, netlist of the circuit is created in the form of physical cell block. The geometric locations of each cell and the wiring between them determines the total area and the timing correctness of the design. Following are the steps that are involved in the complete Physical Design Flow:

1. Design Entry
2. Circuit Partitioning
3. Floor planning
4. Placement
5. Clock Tree Synthesis
6. Routing
7. Parasitic extraction and post layout timing checks

11.1. Design Entry

This step requires the importing of 3 main files.

- a) Gate netlist: The netlist generated by the synthesis step that has all the necessary information about the internal gates and the interconnection between them. This file is a Verilog/VHDL file.
- b) Cell library file: This library file contains the information of the basic combinational gates/cell such as Inverter, AND, NAND, XOR, etc. This file may also include some sequential gates such as Flip-flops. This information include the geometric properties such as dimensions, height and width, and timing information. Timing information that it contains is a function of various input and output loads and delays.

Figure 39 shows the layout window after importing the MSDAP design

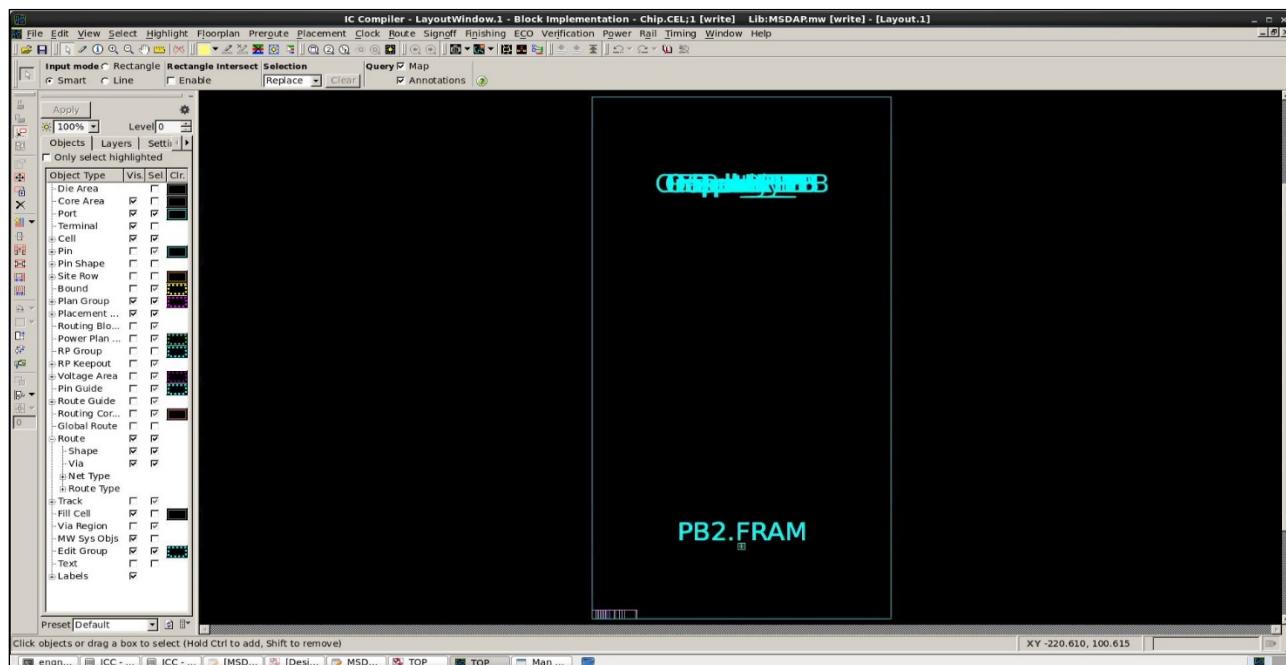


Figure 39: Design entry

11.2. Circuit Partitioning

Partitioning is the process of dividing a chip into different functional blocks and aim is to keep the frequently communicating blocks together. This reduces the cost and efforts of further design stages. The aim of the partitioning process is to divide the design in such a way that, the interconnection between the blocks are minimized. If the interconnections between two partitions are not minimized, then the functional blocks which are supposed to be together will be pushed away from each other which will affect the overall performance of the system. This will increase the total number of required interconnects in the design which will increase the complexity of the circuit overall. The partitioning problem takes in a netlist and divides the circuit represented by the netlist into two parts with a target to minimize the interconnection between them.

11.3. Floor planning

Once the circuit is partitioned properly so that the cells connected to each other are brought together, the design is ready for the floor plan. The floor plan aims to reduce the cross talks, potential timing violations, and the total chip area. During floor planning, the important things that are kept in mind are aspect ratio of the chip, core utilization, distance between core and I/O pins, and distance between two adjacent cell rows.

Figure 41 shows the layout window in IC compiler after floor plan of MSDAP was done.

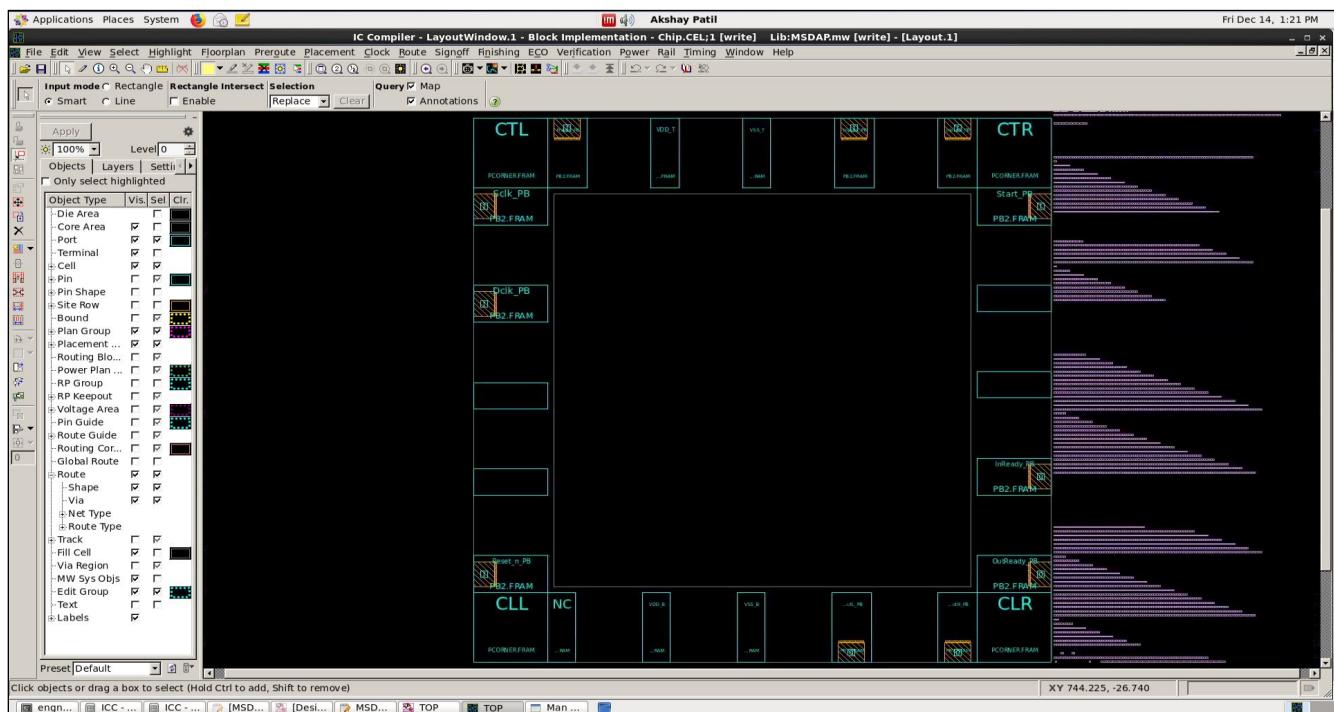


Figure 40: Floorplan of MSDAP

The figures 42-44 shows the floorplan after inserting pad fillers, VDD/VSS rings and VDD/VSS strips respectively.

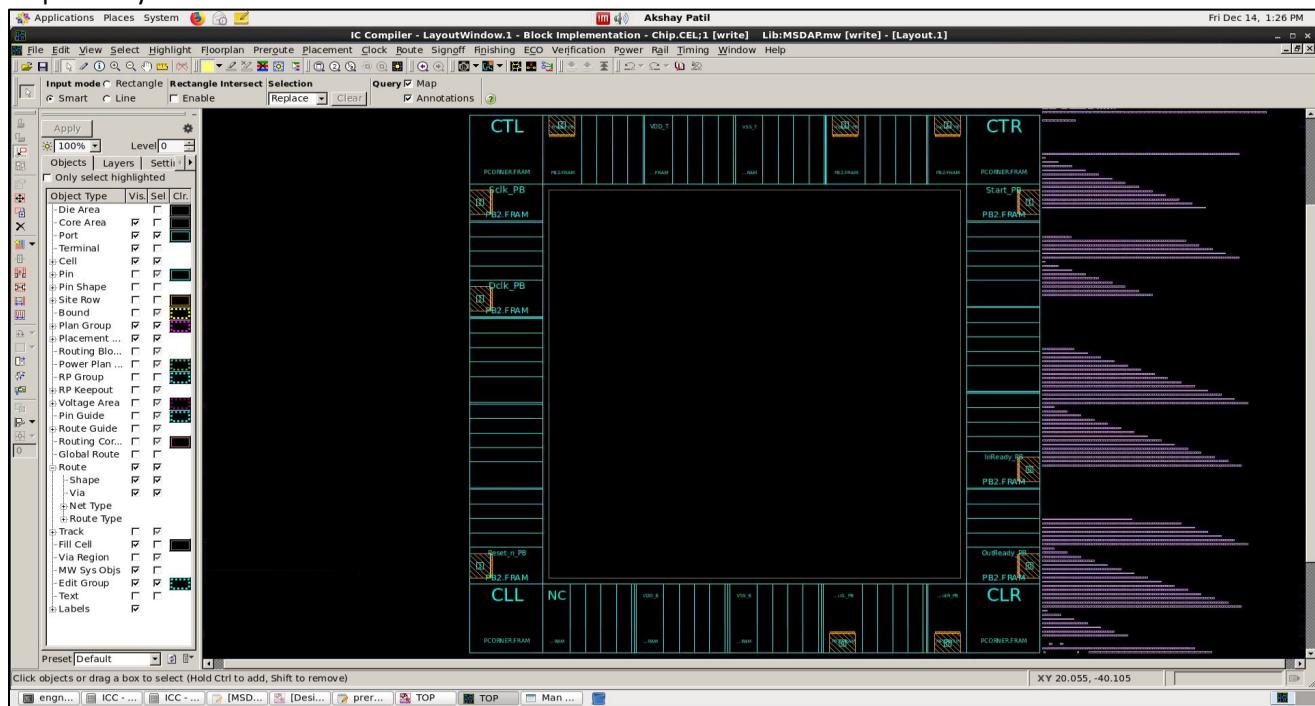


Figure 41: Insertion of PAD fillers

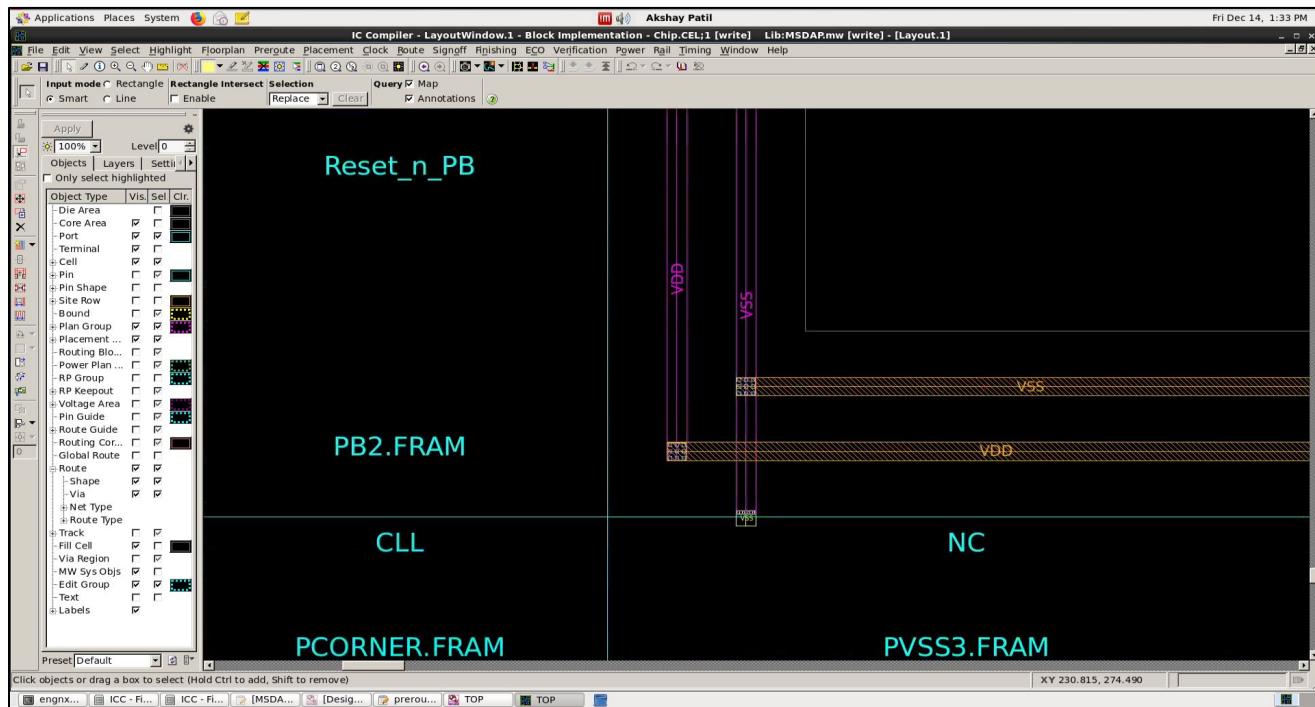


Figure 42: Insertion of VDD/VSS rings

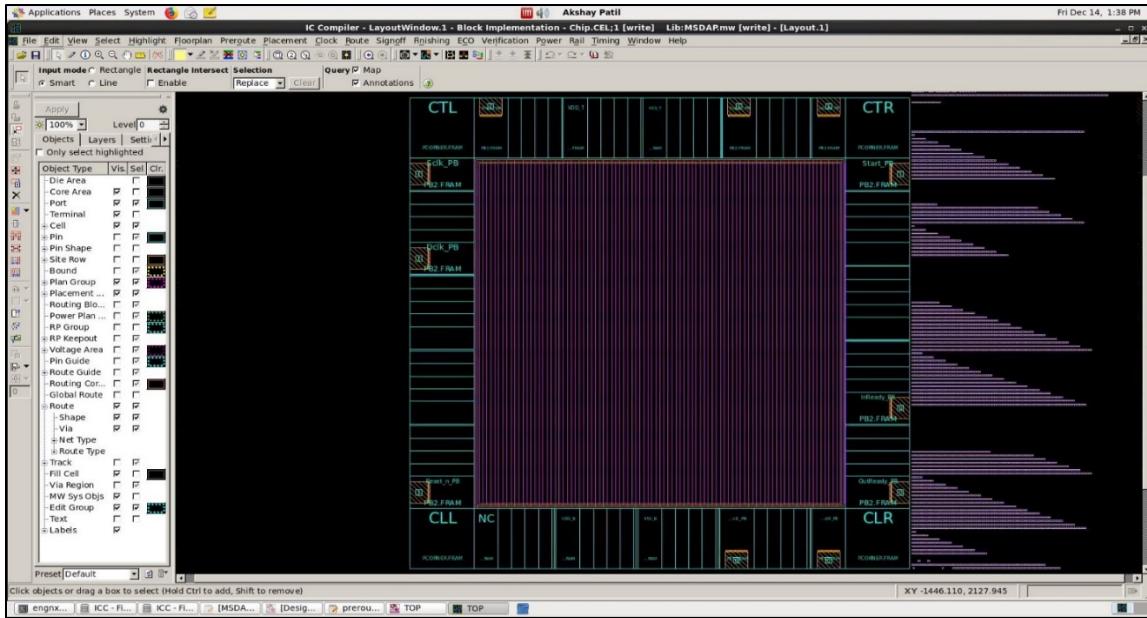


Figure 43: Insertion of VDD/VSS strips

This step of creating VDD/VSS rails basically provides the supply power to the whole chip. Therefore, this step is also called Power planning.

11.4. Placement

Placement is another very important stage in physical design. In this stage, the geometrical locations are assigned to each cell in the circuit. The factors taken into consideration for placement mainly involves, interconnections between the cells e.g. nets. The aim of the placement is to ensure that every cell in the circuit is connected to the other cell through minimum required wire length which will minimize the total wire length of the circuit. Minimum wire length reduces the routing area which will reduce the cost of the system. It will also reduce the complexity for the routing stage of physical design process. Figure 45 shows the layout after placement of all cells is done.

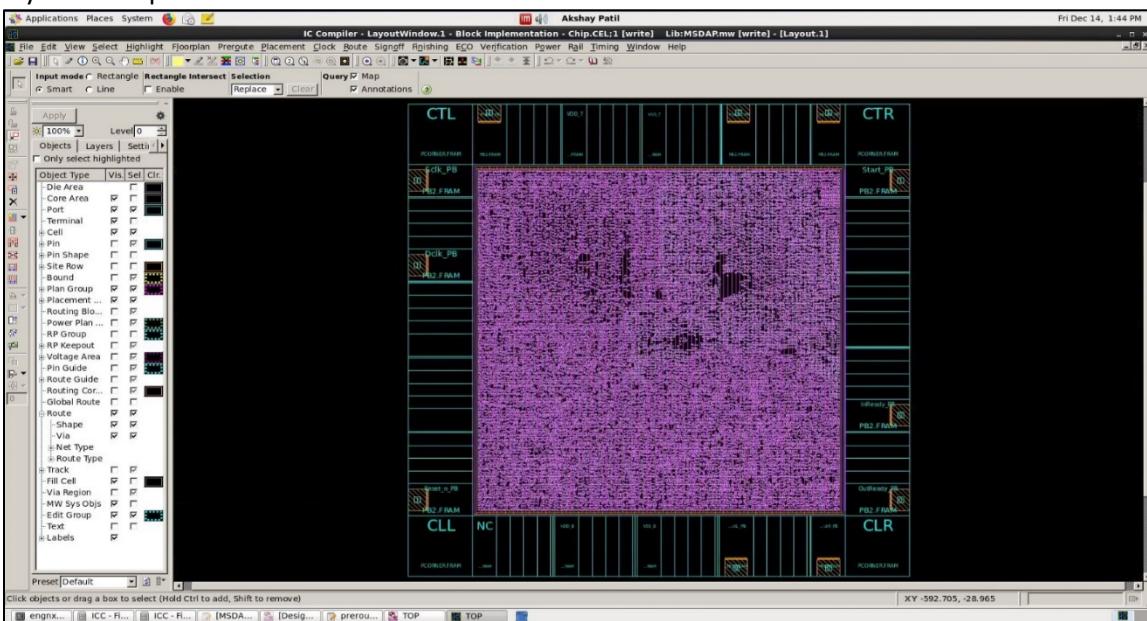


Figure 44: Placement

11.5. Clock Tree Synthesis

Clock net is the most critical net in any design. If the timing constraints are not met, then the circuit may give wrong results or no result at all. To avoid this timing violations, it is very important to supply the clock to each clocked device in such a way that all the cells which are at the same stage in the dataflow will receive the clock exactly at the same time. If there is a difference in these cells, then this difference is called 'skew'. The aim of the CTS is to re arrange the cells after placement step to minimize this skew. The layout after doing the CTS is shown in the figure 46.

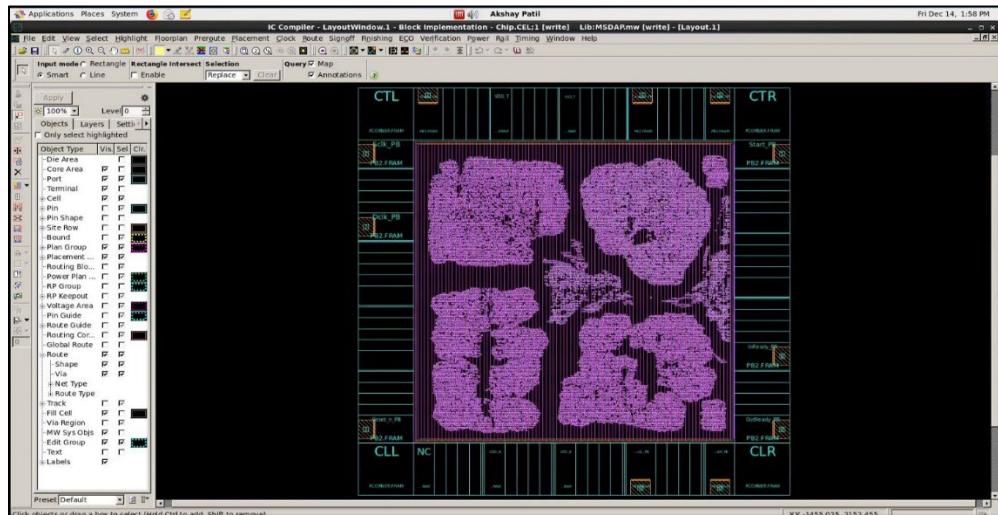


Figure 45: Clock tree Synthesis

11.6. Routing

Routing is a connection of the various standard cells using wires. There are two types of routing.
Global routing : This method first partitions the routing into tiles and then decides tile-to-tile paths for all nets while attempting to optimize some of the objective functions such as circuit timing and the lengths etc.

Detailed routing: This method uses the paths obtained by global routing and assigns tracks and vias for nets.

Figure 47 shows the closer look of the MSDAP after the routing step was complete.

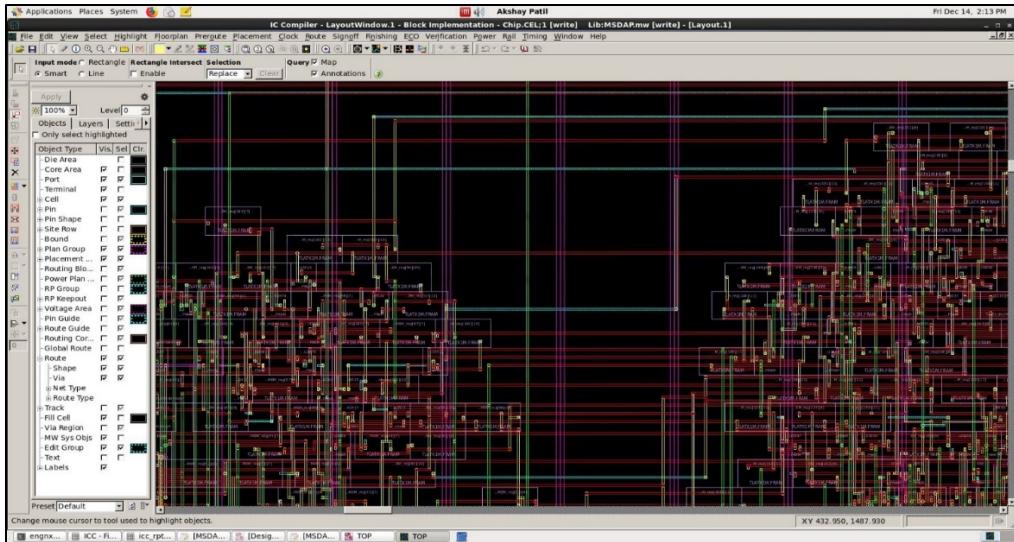


Figure 46: Routing

After routing, it is very important to verify the routing done by tool. It can happen that there are some un-routed nets left behind. It may also happen that the routed nets are violating some DRC rules. Once the verification is done, the design is ready for further steps. Figure shows the image of verification report.

```

Total double via conversion rate = 0.00% (0 / 316492 vias)

Layer VIA12      = 0.00% (0 / 137492 vias)
Layer VIA23      = 0.00% (0 / 141114 vias)
Layer VIA34      = 0.00% (0 / 34011 vias)
Layer VIA45      = 0.00% (0 / 3237 vias)
Layer VIA56      = 0.00% (0 / 638 vias)

The optimized via conversion rate based on total routed via count = 0.00% (0 / 316492 vias)

Layer VIA12      = 0.00% (0 / 137492 vias)
    Un-optimized = 100.00% (137492 vias)
Layer VIA23      = 0.00% (0 / 141114 vias)
    Un-optimized = 100.00% (141114 vias)
Layer VIA34      = 0.00% (0 / 34011 vias)
    Un-optimized = 100.00% (34011 vias)
Layer VIA45      = 0.00% (0 / 3237 vias)
    Un-optimized = 100.00% (3237 vias)
Layer VIA56      = 0.00% (0 / 638 vias)
    Un-optimized = 100.00% (638 vias)

Verify Summary:

Total number of nets = 36698, of which 0 are not extracted
Total number of open nets = 0, of which 0 are frozen
Total number of excluded ports = 0 ports of 0 unplaced cells connected to 0 nets
                                         0 ports without pins of 0 cells connected to 0 nets
                                         0 ports of 0 cover cells connected to 0 non-pg nets
Total number of DRCS = 0
Total number of antenna violations = no antenna rules defined
Total number of voltage-area violations = no voltage-areas defined
Total number of tie to rail violations = not checked
Total number of tie to rail directly violations = not checked

1
icc shell>

```

Figure 47: Screenshot of DRC verification report

11.7. Parasitic extraction and post layout timing checks

The transistors used for designing of the system, the wires used for interconnects between the cells are not ideal in nature. They have their own capacitances and resistances. These RC components are not

unavoidable and their effect has to be accounted while doing any ASIC design. When the effects of these parasitic components are accounted, it may disturb the timing checks. Therefore it is very important to do the post-layout timing checks which also accounts for the parasitic mentioned above. The reports for this utilization, power and the post-layout timing are provided in Appendix D.

12. Optimization of the layout

The layout in figure 46 shown during the discussion of Clock Tree synthesis shows the complete layout of MSDAP with 60% target core utilization. After performing the placement and CTS, the actual core utilization reduced to ~43%. If the wiring complexity of the design is not high, then such low core utilization is not good as it wastes a lot of area on the chip. Therefore, one more design was made with the 90% of target core utilization. After complete placement and route, this yielded to the layout of ~64% actual core utilization. Figures 49 and 50 shows the layouts after placement and routing of this design.

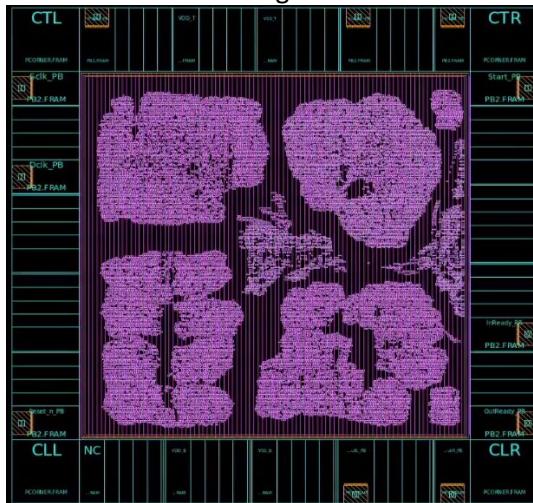


Figure 48: Layout with 43% core utilization

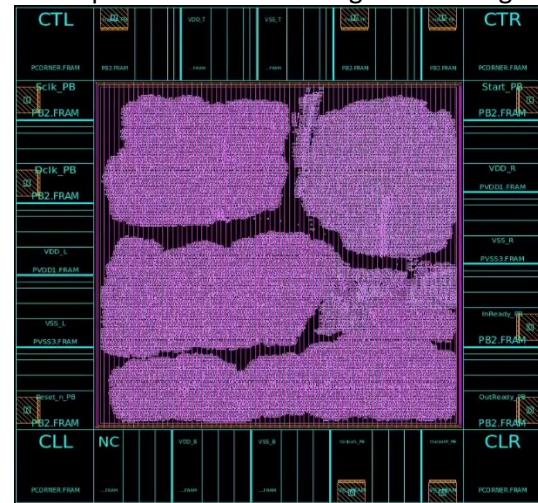


Figure 49: Layout with 64% actual core utilization

The table 3 shows the summary of physical design report. Please see Appendix D for details

Table 3: Summary of physical design report

Core Utilization	60%	90%
Actual core utilization	43.99%	64.23%
Chip Area	823543 sites	548800 sites
Standard cell area	362270 sites	352507 sites
Library cell count	137	114
Total dynamic power	1.4691 mW	1.4869 mW
Cell leakage power	28.5806 uW	30.6297 uW
Slack	MET	MET
Frequency of Sclk	26.88MHz	26.88MHz

13. Issues of physical design

In general, the normal signal nets may undergo in iterative routing steps such as, Global routing and detailed routing. In global routing, the design is first partitioned in small section also known as islands. (Because these sections looks like islands on the chip. See figure 10 and 11). Global routing aims to make the connections between these islands first. In detailed routing, the connections inside each island is handled to minimize the total routing cost. But the most important than doing the signal routing is routing of critical/sensitive nets. In ASIC, the most sensitive nets are power nets and clock nets. It is advised to do perform the routing of these critical nets first before proceeding to global and detailed routing.

13.1. Clock network layout

In synchronous systems, the performance of the design highly depends on the quality of the clock network. Without the precise routing of these nets, the path length from the entry point of the clock signal in the chip till the actual feed points will vary. This is shown in the figure 51.

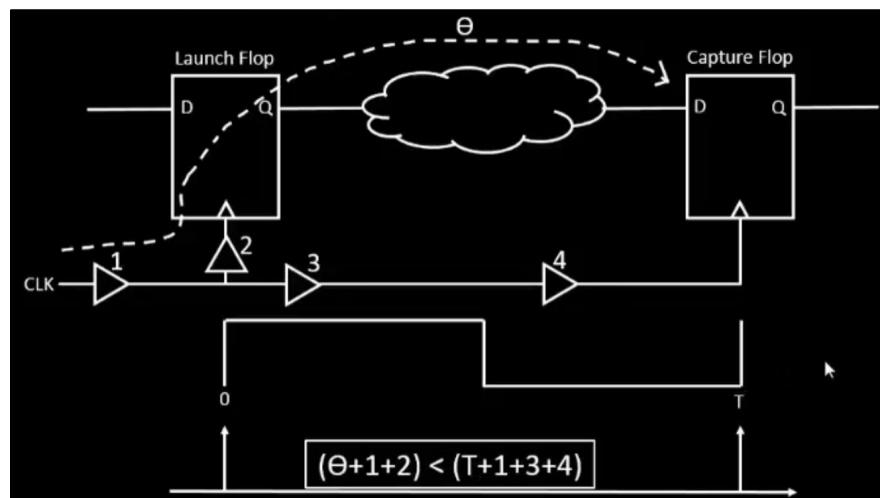


Figure 50: Structure of clock network

In the figure above, we can see that there is a difference in the clock arrival times at launch flop and capture flop. The clock signal takes delay of 2 buffers (Buffer 1 & 2) to arrive at launch flop. To arrive at capture flop, the clock signal takes the delay of 3 buffers (Buffers 1, 3, and 4). This scenario is very common to happen in all the ASIC chip. Ideally it is required that both flip-flops should be triggered at the same time. But due to the scenarios like shown in the figure, this cannot happen. The difference between the arrival edges at two flip-flop is known as 'Skew'. If the skew is too high in the design, then the design will not work at the desired clock frequency which is undesirable. Because of this reason, the clock routing plays very important part in the layout.

To tackle the issues related to clock routing, designers have come up with various techniques. One of these technique include H-tree algorithm

H-tree clocking:

This is one of the widely used technique for clock trees. This method found to be very effective for regular structure like FPGAs and is somewhat effective in the ASIC design as well. In this method, clock net is attempted to bring at the equidistant point from all the feeding points. This is illustrated in figures 52, 53.

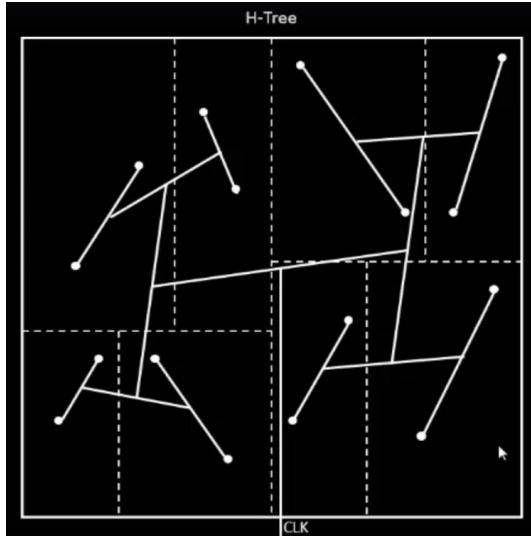


Figure 51: H-tree clock design

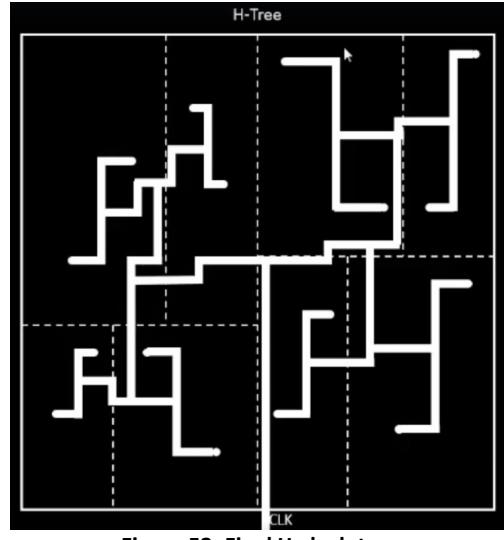


Figure 52: Final H-clock-tree

As we can see in the figure 52 that instead of providing the clock directly to the feeding points, it is brought as close to the centre as possible. Because the angle routing is not allowed in the VLSI world, the clock scheme in the figure 52 is then converted to the practical routing as shown in the figure 53.

Other problems, apart from clock skew, associated with the clock network are,

- **Power consumption:** Clock is the most power hungry net in the whole design because it switches at every half clock cycle. Clock contributes to approximately 70% of the total dynamic power consumption. This increases total dynamic power consumption in the system. To tackle this problem, a concept called ‘clock gating’ is used. In this, the part of the network which runs on the clock but may not need the clock all the time is provided with the gated clock. Whenever this part does not need the clock, the supply of the clock is stopped in that part. This is done using a simple technique depicted in the figure 54.

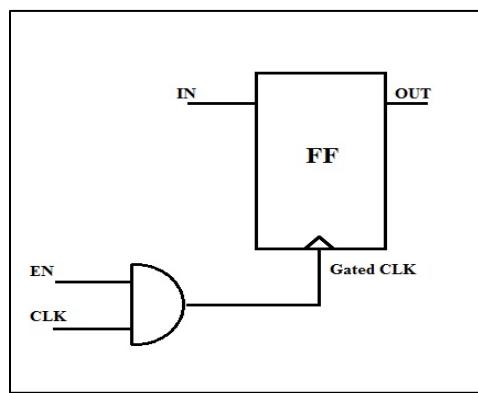


Figure 53: Illustration of a gated clock

- **Noise:** All the nets that carry signals and clock, are not ideal nets in real circuit. They have their own parasitic resistance and capacitances. The capacitors get short circuited during the high frequency activities. In digital systems, the switching part in any signal is the highest frequency component. As we know that clock makes the switching at every half clock cycle, the capacitors between the clock net and neighbouring net can get short circuited causing the crosstalk between these nets. In such cases, the signal on the neighbouring net (victim net) can get affected by the signal from clock net (aggressor

net). This situation is illustrated in the figure 55. It is normally avoided by making the clock network on a different metal layer. If that is not possible then the clock nets are shielded by ground net in between the aggressor and victim net. The red net in figure represents the aggressor net, and the white net represents victim net.

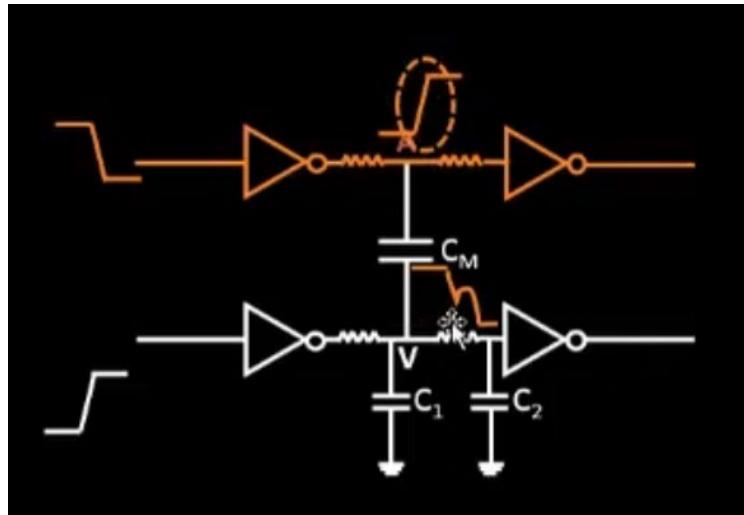


Figure 54: Crosstalk

13.2. Power network layout

Almost all of the cells in the design requires the two nets. They are power nets and ground nets. As the demand of these signals is high, they undoubtedly contribute to very huge network on the chip. As power is demanded by each cell in the network, the size of these power nets must be more than a regular net to make sure that the resistivity is reduced and current carrying capacity is increased. Therefore, it is very critical to manage the area resource distribution n in power/ground, clock, and signal nets. The two important issues related to the power nets are, voltage drop and ground bump.

- **Voltage drop:** Consider the figure 56. Suppose that all the 16 nets shown in the figure are driven by inverters. When all these inverters make a switching at the same time, the capacitors discharged with the 0V starts charging towards voltage VDD. During switching, there is a direct path between the VDD and VSS/GND. In such cases, if the current carrying capacity of the VDD net is low then there can be a voltage drop at this net as shown in the figure. This reduces the total supply voltage which makes the system slow in response.

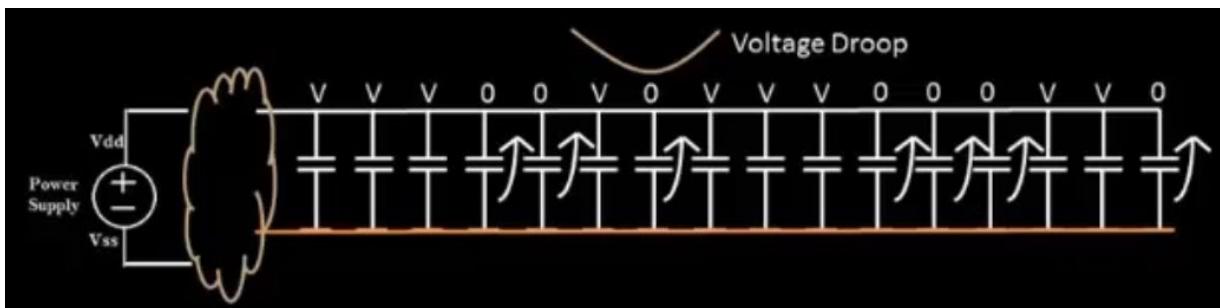


Figure 55: Voltage drop due to switching

- **Ground bump:** Consider the similar scenario but for the ground net this time. In figure we can see that when all the inverters switches, the capacitors which were charged to VDD previously starts to discharge towards GND. If the number of discharging capacitors is so high that the ground net cannot

with stand this, then there can be a bump on the ground net. This increases the minimum voltage that can be provided as a ground to the system.

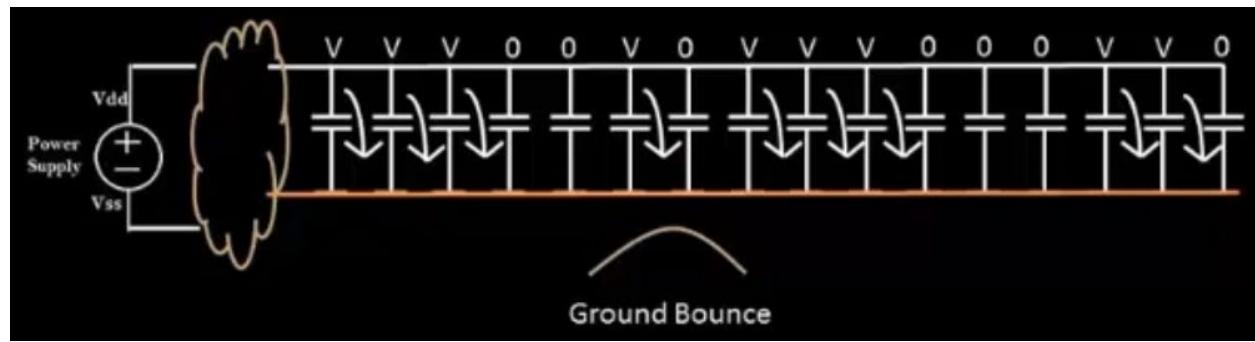


Figure 56: Ground bump due to switching

14. Physical verification

The primary objective of physical design verification is to check whether the layout created in the physical design step is following all the rules provided by the foundry. This is to make sure that the design is manufacturable and will function as it should even after manufacturing. Even though the design has passed all the checks, it is not fully ready to be taped out after its physical layout. This process is highly automated because of the number of components involved in the modern designs. In general, the physical verification is carried out in a same tool in which the physical layout is done. Once the physical layout is done it has to undergo various check such as,

- Design Rule Check (DRC)
- Antenna Effect checking
- Electric Rule check (ERC)
- Layout versus Schematic (LVS)
- Critical path timing check

If any of these check fails, the designer has to go back in the design steps in a sequential manner. Upon failure, first the designer need to go back to the physical design steps such as floor planning, placement, and routing. By re-doing these steps, the designer has to come up with a new layout which will again go through the post-layout verification checks, if the changes in the layout design step doesn't help, then the designer is forced to go back to the RTL design step. Designer has to make the changes in RTL design in such a way that the design remains synthesizable and the problems that caused in the post-layout verification are solved. Once the new RTL is synthesized, it has to go through all the physical design steps mentioned in the section 11.

14.1. Design Rule Check (DRC)

DRC check is the fundamental check which needs to be done on any layout design. This check is carried out using the information in a file called 'DRC deck'. DRC deck is provided by the semiconductor fabrication company. It contains the rules for the minimum geometric separation between the different layers that are used while laying out the design. If these rules are not obeyed then it can lead to an improper manufacturing of an Integrated Circuit Chip. This reduces the probability of yield.

If the DRC deck are designed in more conservative way, then it ensures the high probability of the yield because the manufacturing of design verified with these decks have enough spacing between the layers. But it is important to keep in mind that this will lead to a considerably large area design. On the other hand, if the DRC deck is designed in very optimistic manner, then it provides relatively compact circuit. However, this results in low probability of yield. Apart from the minimum distance, the DRC rules includes the rules for,

- Minimum area enclosure
- Minimum width of layers and regions
- Enclosure rule for two different layers to specify the margin between their adjacent boundaries.
- Rule that check the ratio of area of metals used at different layers

In ICC, the DRC verification option is available in the '*Verification > DRC*' menu

14.2. Layout versus Schematic (LVS)

The LVS checks for the equivalence of the physical layout that of the design and its transistor level schematic. If the layout and the transistor level schematic represents the same system, then the number of transistor present in both of them, the number of connections, and connectivity in the designs should be same. This can be considered as the most basic test to check the correctness of the functionality of the

layout. According to the Moore's law, the number of transistor in ICs multiplies by 1.5 times each two years and the modern ASIC design have millions of transistor in it. This make it impossible to check for LVS manually. In such cases the LVS check tool comes in handy. Even though the LVS check software are very fast, they can consume high amount of memory during the check. This is overcome by doing the hierarchical approach for LVS check. This approach reduces the amount of data to be checked. In this approach, the L VS check is done at every stage during the design. For example, in the standard cell based design, instead of checking the final design at the transistor level, it is made sure that each gate in the cell library has undergone LVS check. This enables the designer to perform the gate level LVS check in the final design.

The EDA tools performs LVS in 3 steps. They are,

- Extraction – Process of determining the components present by analyzing the layers that are drawn during physical layout design step.
- Reduction – Generation of a netlist with the help of information obtained after extraction step. It also generated the netlist from the transistor level schematic file.
- Comparison – Comparison of two netlists created in Reduction step.

In ICC, the LVS verification option is available in the '*Verification > LVS*' menu

14.3. Electric Rule check (ERC)

The Electric Rule Check might seem to be very similar to LVS check, but the carry a minute difference. Unlike LVS, which verifies the equivalence in the transistor count and interconnections present in layout and schematic, the ERC rules check for the electrical correctness of the design. This includes checking for conflicting output cases such as race conditions, floating inputs and outputs, etc. The circuit which has passed the LVS check does not necessarily would pass ERC. Consider an example where the schematic and the layout of a system both contains a floating pin. This system will pass the LVS check because they both are electrically equivalent but it will not pass the ERC rules because they are not electrically correct.

ERC rules are usually not generic in nature and can be modified by designer as per requirement. Apart from the cases mentioned above, ERC may also check for the cases like potential places to for latch ups, and ESD.

14.4. Antenna Effect checking

Antenna rule are designed by the IC manufacturing companies to make sure that the transistor is not destroyed during its manufacturing process itself. While manufacturing of the transistors, ion implantation is done. These ions need a path from the wafer to the substrate as well as active layers which are present at the bottom. This check mainly concerns the manufacturing of the gate area of transistor.

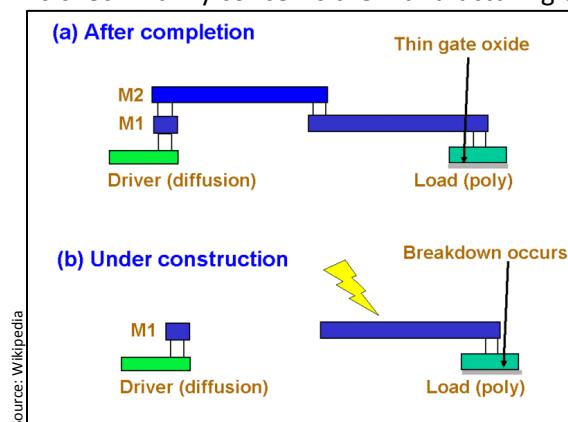


Figure 57: Antenna Effect

Figure 58.a shows the desired connection that has to be done in the design. Here the Source/Drain of one device connected to the Gate of another device. This connection is made via Metal 2 layer. But the fabrication of transistor is done layer by layer. Hence while fabricating the gate area of the 2nd transistor, there is no connection of it between the Source/Drain of first transistor. This is shown in the figure 58.b. The yellow lightning bolt in the figure b represents the ion implantation. The only way for the ions to reach the substrate is through gate poly and gate oxide. In such case, the ions will force their way down the gate oxide and this might destroy the oxide. Once the oxide layer is destroyed, the transistor no longer remains functional.

Antenna effects are overcome by adding small antenna diode to discharge the ions or by changing the order of routing layers. In ICC, Antenna check is performed from '*Route > Verify Route*' menu.

14.5. Critical path

The critical path obtained after the synthesis step and the timing check done at that point of time is not enough because that timing check does not account for the routing delay and the delay due to routing net parasitic. Once the complete layout is done and all the interconnections are made, it is necessary to do the parasitic extraction/ RC extraction.

The wires used to connect the cell in the layout has their own resistance, capacitance and inductance. Longer the wire runs, greater the resistance and capacitance it introduces.

Even the transistor used in the design have their parasitic capacitances. These parasitic components cannot be removed from the circuit and hence their effect must be considered.

For this, the EDA tools provides the option to do the RC extraction. In ICC, it is available under the menu '*Route > Extract RC*'. Using these extracted RC values, the delays associated with wires, transistors and other components is calculated. This information is stored in the SDF (Standard Delay Format) file. During the simulation of netlist, the delays from this SDF file is pulled out. This process is known as 'Back-Annotation'. The EDA tools use this delay information to re-calculate the critical path and its delay. This path and delay is more accurate than the one evaluated after the synthesis step.

Appendix

Appendix A: Synthesis Report

```
design_vision> compile -exact_map
Information: There are 26 potential problems in your design. Please run
'check_design' for more information. (LINT-99)
```

Beginning Pass 1 Mapping

```
-----  
Processing 'controller'  
Processing 'PISO_0'  
Processing 'ALU_0'  
Processing 'Xmem_0'  
Processing 'Hmem_0'  
Processing 'RJmem_0'  
Processing 'SIPO_0'  
Processing 'and2_0'  
Processing 'or3_0'  
Processing 'or2_0'  
Processing 'top_level'
```

Updating timing information

```
Information: Updating design information... (UID-85)
```

Beginning Implementation Selection

```
-----  
Processing 'controller_DW01_cmp6_0'  
Processing 'controller_DW01_inc_0'  
Processing 'controller_DW01_inc_1'  
Processing 'controller_DW01_inc_2'  
Processing 'controller_DW01_inc_3'  
Processing 'controller_DW01_inc_4'  
Processing 'controller_DW01_inc_5'  
Processing 'PISO_1_DW01_cmp6_0'  
Processing 'PISO_1_DW01_inc_0'  
Processing 'PISO_0_DW01_cmp6_0'  
Processing 'PISO_0_DW01_inc_0'  
Processing 'ALU_1_DW01_inc_0'  
Processing 'ALU_1_DW01_inc_1'  
Processing 'ALU_1_DW01_cmp6_0'  
Processing 'ALU_1_DW01_inc_2'  
Processing 'ALU_1_DW01_cmp6_1'  
Processing 'ALU_1_DW01_sub_0'  
Processing 'ALU_1_DW01_sub_1'  
Processing 'ALU_1_DW01_add_0'  
Processing 'ALU_0_DW01_inc_0'  
Processing 'ALU_0_DW01_inc_1'  
Processing 'ALU_0_DW01_cmp6_0'  
Processing 'ALU_0_DW01_inc_2'  
Processing 'ALU_0_DW01_cmp6_1'  
Processing 'ALU_0_DW01_sub_0'  
Processing 'ALU_0_DW01_sub_1'  
Processing 'ALU_0_DW01_add_0'  
Processing 'Xmem_1_DW01_inc_0'  
Processing 'Xmem_0_DW01_inc_0'  
Processing 'SIPO_1_DW01_inc_0'  
Processing 'SIPO_0_DW01_inc_0'
```

Beginning Mapping Optimizations (Medium effort)

ELAPSED TIME	AREA	WORST NEG SLACK	TOTAL COST	DESIGN RULE COST	ENDPOINT
-----------------	------	--------------------	---------------	---------------------	----------

```

-----
0:02:30 1966826.8      0.00      0.0      0.0
0:02:30 1966826.8      0.00      0.0      0.0
0:02:30 1966826.8      0.00      0.0      0.0
0:02:30 1966826.8      0.00      0.0      0.0
0:02:31 1966826.8      0.00      0.0      0.0
0:03:02 1085840.3      0.00      0.0      0.0
0:03:03 1085840.3      0.00      0.0      0.0
0:03:04 1085840.3      0.00      0.0      0.0
0:03:05 1085840.3      0.00      0.0      0.0
0:03:05 1085840.3      0.00      0.0      0.0
0:03:06 1085840.3      0.00      0.0      0.0
0:03:06 1085840.3      0.00      0.0      0.0
0:03:06 1085840.3      0.00      0.0      0.0

```

Beginning Delay Optimization Phase

ELAPSED TIME	AREA	TOTAL			ENDPOINT
		WORST SLACK	NEG	SETUP COST	
0:03:06	1085840.3	0.00	0.0	0.0	
0:03:06	1085840.3	0.00	0.0	0.0	
0:03:06	1085840.3	0.00	0.0	0.0	

Beginning Area-Recovery Phase (cleanup)

ELAPSED TIME	AREA	TOTAL			ENDPOINT
		WORST SLACK	NEG	SETUP COST	
0:03:06	1085840.3	0.00	0.0	0.0	
0:03:07	1085840.3	0.00	0.0	0.0	
0:03:38	1085513.2	0.00	0.0	0.0	
0:03:38	1085405.6	0.00	0.0	0.0	
0:03:38	1085328.8	0.00	0.0	0.0	
0:03:39	1085291.5	0.00	0.0	0.0	
0:03:39	1085271.7	0.00	0.0	0.0	
0:03:39	1085271.7	0.00	0.0	0.0	
0:03:40	1085271.7	0.00	0.0	0.0	
0:03:40	1085271.7	0.00	0.0	0.0	
0:03:40	1085271.7	0.00	0.0	0.0	
0:03:41	1085271.7	0.00	0.0	0.0	
0:03:41	1085271.7	0.00	0.0	0.0	
0:03:41	1085271.7	0.00	0.0	0.0	
0:03:42	1085271.7	0.00	0.0	0.0	

Loading db file '/home/eng/x/xxw122030/synopsys/ss_1v62_125c.db'
 Loading db file '/home/eng/x/xxw122030/synopsys/ff_1v98_0c.db'
 Loading db file '/home/eng/x/xxw122030/synopsys/tt_1v8_25c.db'

Note: Symbol # after min delay cost means estimated hold TNS across all active scenarios

Optimization Complete

1
 Current design is 'top_level'.
 design_vision>

Appendix B: Schematic of each function block

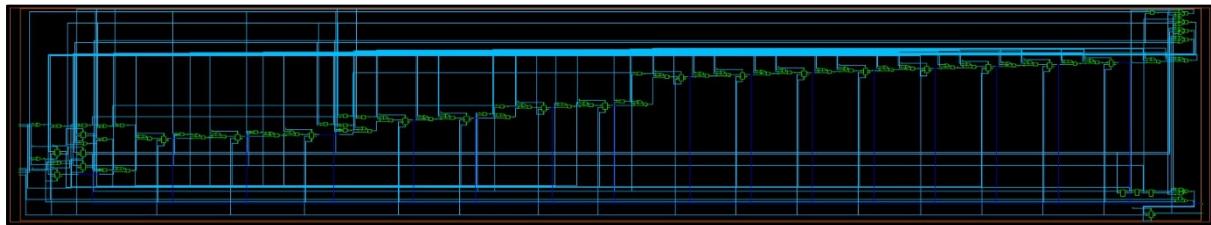


Figure 58: Schematic of SIPO module

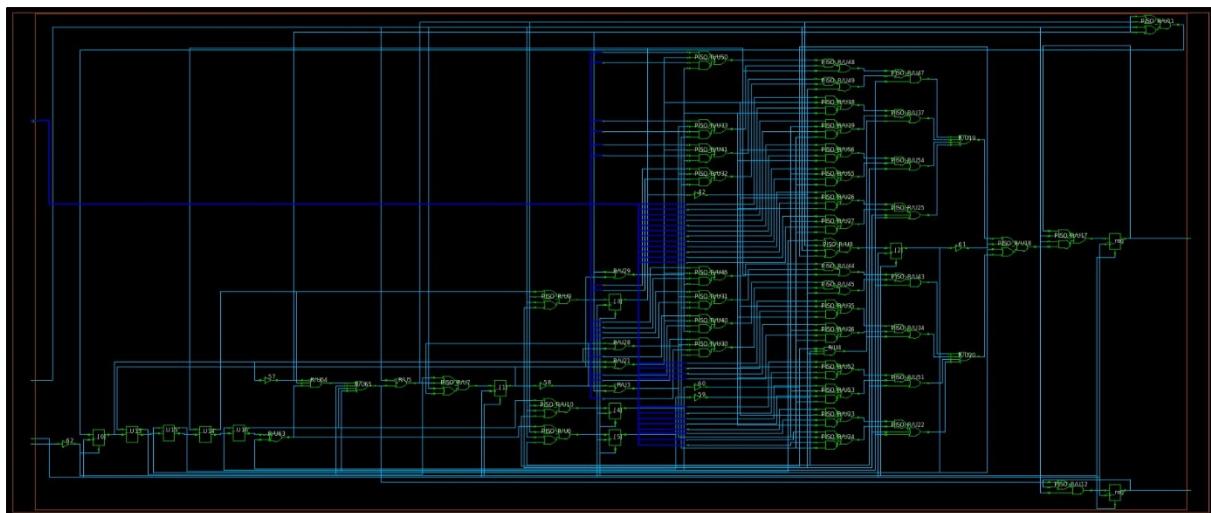


Figure 59: Schematic of PISO module

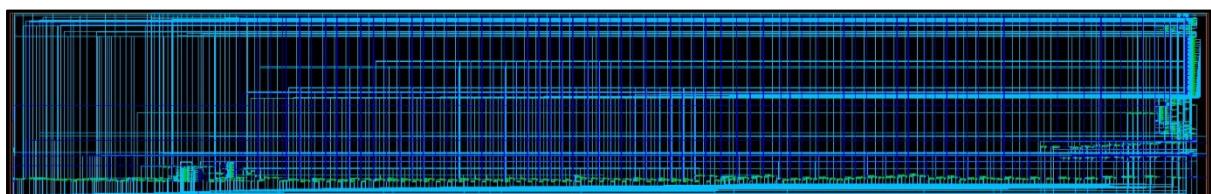


Figure 60: Schematic of ALU module

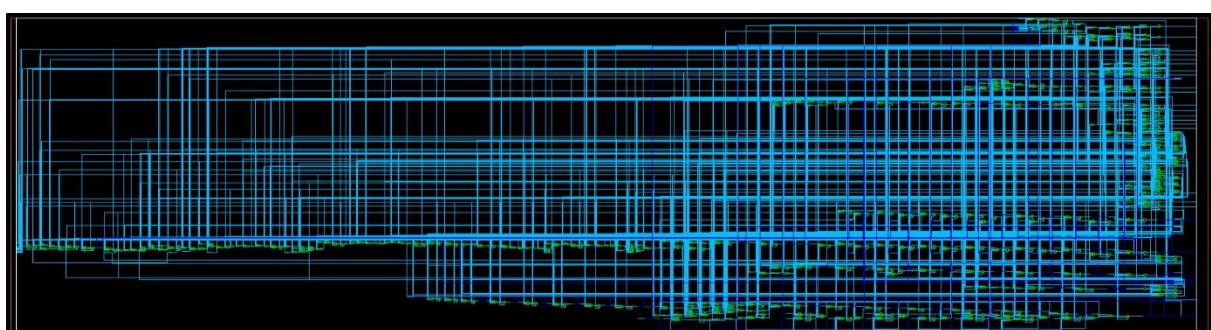


Figure 61: Schematic of controller module

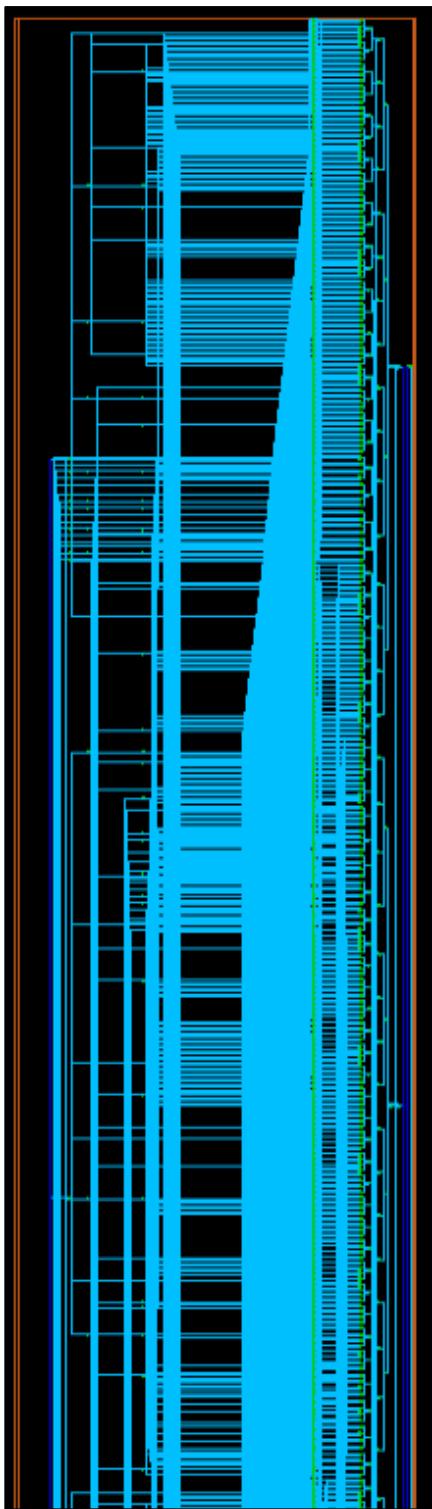


Figure 62: Schematic of X memory module



Figure 63: Schematic of RJ memory module

*Note: Schematics of H memory block is not provided since it is too big to be opened by DC

Appendix C: Timing, Cell, and Area reports.

```
*****
Report : timing
    -path full
    -delay max
    -max_paths 1
Design : top_level
Version: O-2018.06-SP1
Date   : Thu Dec 13 20:38:38 2018
*****
```

Operating Conditions: ss_lv62_125c Library: ss_lv62_125c
Wire Load Model Mode: top

Startpoint: Reset (input port clocked by Sclk)
Endpoint: SIPO_L/data_out_reg[8]
(falling edge-triggered flip-flop clocked by Dclk)
Path Group: Dclk
Path Type: max

Point	Incr	Path
clock Sclk (rise edge)	37091.11	37091.11
clock network delay (ideal)	0.00	37091.11
input external delay	1.00	37092.11 r
Reset (in)	0.00	37092.11 r
SIPO_L/Reset (SIPO_0)	0.00	37092.11 r
SIPO_L/U18/Y (NOR2BX2M)	0.34	37092.44 r
SIPO_L/U7/Y (NAND2X2M)	0.26	37092.70 f
SIPO_L/U55/Y (AND2X2M)	0.26	37092.96 f
SIPO_L/U52/Y (AND2X2M)	0.21	37093.17 f
SIPO_L/U11/Y (NAND2X2M)	0.12	37093.29 r
SIPO_L/U19/Y (OAI21X1M)	0.14	37093.42 f
SIPO_L/data_out_reg[8]/D (DFFNSRHX1M)	0.00	37093.42 f
data arrival time		37093.42
clock Dclk (fall edge)	37109.28	37109.28
clock network delay (ideal)	0.00	37109.28
SIPO_L/data_out_reg[8]/CKN (DFFNSRHX1M)	0.00	37109.28 f
library setup time	-0.11	37109.16
data required time		37109.16
data required time		37109.16
data arrival time		-37093.42
slack (MET)		15.74

Startpoint: SIPO_L/word_ready_reg
(falling edge-triggered flip-flop clocked by Dclk)
Endpoint: CU/xw_ptr_R_reg[0]
(rising edge-triggered flip-flop clocked by Sclk)
Path Group: Sclk
Path Type: max

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (ideal)	0.00	651.04
SIPO_L/word_ready_reg/CKN (DFFNSRHX1M)	0.00	651.04 f
SIPO_L/word_ready_reg/Q (DFFNSRHX1M)	0.65	651.69 r
SIPO_L/word_ready (SIPO_0)	0.00	651.69 r
inst_word_ready/a (and2_0)	0.00	651.69 r
inst_word_ready/U1/Y (AND2X2M)	0.33	652.02 r

inst_word_ready/out (and2_0)	0.00	652.02	r
CU/word_ready (controller)	0.00	652.02	r
CU/U48/Y (INVX2M)	0.20	652.22	f
CU/U149/Y (OAI22X1M)	0.26	652.48	r
CU/U54/Y (OAI21X1M)	0.15	652.63	f
CU/U53/Y (BUFX2M)	0.33	652.96	f
CU/U16/Y (INVX2M)	0.12	653.08	r
CU/U46/Y (NAND2X2M)	0.20	653.28	f
CU/U150/Y (OAI221X1M)	0.25	653.53	r
CU/xw_ptr_R_reg[0]/D (DFFRQX2M)	0.00	653.53	r
data arrival time		653.53	
clock Sclk (rise edge)	669.64	669.64	
clock network delay (ideal)	0.00	669.64	
CU/xw_ptr_R_reg[0]/CK (DFFRQX2M)	0.00	669.64	r
library setup time	-0.28	669.36	
data required time		669.36	
data required time		669.36	
data arrival time		-653.53	
slack (MET)		15.83	
1			

Report : cell
Design : top_level
Version: 0-2018.06-SP1
Date : Thu Dec 13 20:38:38 2018

Attributes:

- b - black box (unknown)
- h - hierarchical
- n - noncombinational
- r - removable
- u - contains unmapped logic

Cell	Reference	Library	Area	Attributes
<hr/>				
ALU_L	ALU_0		18255.283329	h, n
ALU_R	ALU_1		18255.283329	h, n
CU	controller		10892.582449	h, n
PISO_L	PISO_0		1202.969597	h, n
PISO_R	PISO_1		1202.969597	h, n
SIFO_L	SIFO_0		2329.107244	h, n
SIFO_R	SIFO_1		2329.107244	h, n
hLmem	Hmem_0		334291.636490	h, n
hRmem	Hmem_1		334291.636490	h, n
inst_H_en_L	or2_2		10.976000	h
inst_H_en_R	or2_1		10.976000	h
inst_RJ_en_L	or2_0		10.976000	h
inst_RJ_en_R	or2_3		10.976000	h
inst_Write_Done_L	or3_0		13.171200	h
inst_Write_Done_R	or3_3		13.171200	h
inst_data_valid_L	or3_2		13.171200	h
inst_data_valid_R	or3_1		13.171200	h

inst_prev_OutReady	and2_2	10.976000 h
inst_sleep	and2_3	10.976000 h
inst_word_ready	and2_0	10.976000 h
inst_word_sent	and2_1	10.976000 h
rLmem	RJmem_0	11085.759832 h, n
rRmem	RJmem_1	11085.759832 h, n
xLmem	Xmem_0	169686.762236 h, n
xRmem	Xmem_1	169686.762236 h, n
<hr/>		<hr/>
Total 25 cells		1084736.112703
1		

Report : area
Design : top_level
Version: O-2018.06-SP1
Date : Thu Dec 13 20:38:38 2018

Library(s) Used:

ss_1v62_125c (File: /home/eng/x/xxw122030/synopsys/ss_1v62_125c.db)

Number of ports:	1583
Number of nets:	56058
Number of cells:	54404
Number of combinational cells:	28548
Number of sequential cells:	25815
Number of macros/black boxes:	0
Number of buf/inv:	6990
Number of references:	25
Combinational area:	339573.287809
Buf/Inv area:	60409.707876
Noncombinational area:	745162.824894
Macro/Black Box area:	0.000000
Net Interconnect area:	undefined (No wire load specified)
Total cell area:	1084736.112703
Total area:	undefined
1	

Appendix D: Utilization, power and timing report by ICC

D.1. Utilization and cell report

```
*****
Report : Chip Summary
Design : Chip
Version: O-2018.06-SP2
Date   : Fri Dec 14 16:33:28 2018
*****
Std cell utilization: 64.23% (352507/(548800-0))
(Non-fixed + Fixed)
Std cell utilization: 64.23% (352507/(548800-0))
(Non-fixed only)
Chip area:      548800 sites, bbox (258.00 258.00 1355.60 1355.60) um
Std cell area:  352507 sites, (non-fixed:352507 fixed:0)
                 36410  cells, (non-fixed:36410 fixed:0)
Macro cell area: 0 sites
                  0 cells
Placement blockages: 0 sites, (excluding fixed std cells)
                      0 sites, (include fixed std cells & chimney area)
                      0 sites, (complete p/g net blockages)
Routing blockages:  0 sites, (partial p/g net blockages)
                     0 sites, (routing blockages and signal pre-route)
Lib cell count:    114
Avg. std cell width: 4.91 um
Site array:        unit (width: 0.56 um, height: 3.92 um, rows: 280)
Physical DB scale: 1000 db_unit = 1 um
```

```
*****
Report : pnet options
Design : Chip
Version: O-2018.06-SP2
Date   : Fri Dec 14 16:33:28 2018
*****
```

Layer	Blockage	Min_width	Min_height	Via_additive	Density
METAL1	none	---	---	via additive	---
METAL2	none	---	---	via additive	---
METAL3	none	---	---	via additive	---
METAL4	none	---	---	via additive	---
METAL5	none	---	---	via additive	---
METAL6	none	---	---	via additive	---

```
*****
Sub-Region Utilization
*****
Number of regions with placement utilization 0 - 0.125 is 0 (0.00%)
Number of regions with placement utilization 0.125 - 0.25 is 0 (0.00%)
Number of regions with placement utilization 0.25 - 0.375 is 0 (0.00%)
Number of regions with placement utilization 0.375 - 0.5 is 238 (7.59%)
Number of regions with placement utilization 0.5 - 0.625 is 1300 (41.45%)
Number of regions with placement utilization 0.625 - 0.75 is 1008 (32.14%)
Number of regions with placement utilization 0.75 - 0.875 is 565 (18.02%)
Number of regions with placement utilization 0.875 - 1 is 25 (0.80%)
```

1

D.2. Power report

```
***** POWER REPORT*****
Warning: Cell 'Frame_PB' is being marked as "dont_touch" because it has
        a fixed_placement attribute. (PSYN-040)
Warning: Cell 'InputL_PB' is being marked as "dont_touch" because it has
        a fixed_placement attribute. (PSYN-040)
Warning: Cell 'InputR_PB' is being marked as "dont_touch" because it has
        a fixed_placement attribute. (PSYN-040)
Warning: Cell 'InReady_PB' is being marked as "dont_touch" because it has
        a fixed_placement attribute. (PSYN-040)
Warning: Cell 'OutReady_PB' is being marked as "dont_touch" because it has
        a fixed_placement attribute. (PSYN-040)
Warning: Cell 'OutputL_PB' is being marked as "dont_touch" because it has
        a fixed_placement attribute. (PSYN-040)
Warning: Cell 'OutputR_PB' is being marked as "dont_touch" because it has
        a fixed_placement attribute. (PSYN-040)
Warning: Cell 'Sclk_PB' is being marked as "dont_touch" because it has
        a fixed_placement attribute. (PSYN-040)
Warning: Cell 'Dclk_PB' is being marked as "dont_touch" because it has
        a fixed_placement attribute. (PSYN-040)
Warning: Cell 'Start_PB' is being marked as "dont_touch" because it has
        a fixed_placement attribute. (PSYN-040)
Warning: Cell 'Reset_n_PB' is being marked as "dont_touch" because it has
        a fixed_placement attribute. (PSYN-040)
Warning: The following library cells don't have power description:PFILL50  PFILL20
PFILL2  PFILL01  PFILL001  PCORNER  PFILL1  (PWR-682)
Information: Updating design information... (UID-85)
Information: Input delay ('rise') on clock port 'Sclk' will be added to the clock's
propagated skew. (TIM-112)
Information: Input delay ('fall') on clock port 'Sclk' will be added to the clock's
propagated skew. (TIM-112)
Information: Input delay ('rise') on clock port 'Dclk' will be added to the clock's
propagated skew. (TIM-112)
Information: Input delay ('fall') on clock port 'Dclk' will be added to the clock's
propagated skew. (TIM-112)
Information: Propagating switching activity (low effort zero delay simulation).
(PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)
Warning: The following physical-only library cells don't have power description
that matches design's operation condition:PVSS3  PVDD1  (PWR-681)

*****
Report : power
        -analysis_effort low
Design : Chip
Version: 0-2018.06-SP2
Date   : Fri Dec 14 16:43:27 2018
*****
```

Library(s) Used:

```
SP018EE_V0p5_max (File: /home/eng/z/zxb107020/synopsys/io_max.db)
ss_1v62_125c (File: /home/eng/z/zxb107020/synopsys/ss_1v62_125c.db)
```

Operating Conditions: ss_1v62_125c Library: ss_1v62_125c
Wire Load Model Mode: top

```
Global Operating Voltage = 1.62
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW      (derived from V,C,T units)
```

```

Leakage Power Units = 1pW

Cell Internal Power = 906.3206 uW (61%)
Net Switching Power = 580.5493 uW (39%)
-----
Total Dynamic Power = 1.4869 mW (100%)
Cell Leakage Power = 30.6297 uW



| Power Group %          | Internal Power | Switching Power | Leakage Power | Total Power  |
|------------------------|----------------|-----------------|---------------|--------------|
| ) Attrs                |                |                 |               | (            |
| io_pad (31.53%)        | 0.1319         | 0.3461          | 3.7675e+05    | 0.4785 (     |
| memory (0.00%)         | 0.0000         | 0.0000          | 0.0000        | 0.0000 (     |
| black_box (0.00%)      | 0.0000         | 0.0000          | 0.0000        | 0.0000 (     |
| clock_network (12.30%) | 2.8223e-02     | 0.1584          | 3.5752e+04    | 0.1866 (     |
| register (46.30%)      | 0.6968         | 5.2161e-03      | 5.8503e+05    | 0.7026 (     |
| sequential (3.97%)     | 3.4843e-02     | 2.4217e-03      | 2.2906e+07    | 6.0170e-02 ( |
| combinational (5.91%)  | 1.4479e-02     | 6.8412e-02      | 6.7264e+06    | 8.9617e-02 ( |
| Total 1                | 0.9063 mW      | 0.5805 mW       | 3.0630e+07 pW | 1.5175 mW    |


```

D.3. Setup time report:

```

Information: Updating design information... (UID-85)
Information: Input delay ('rise') on clock port 'Sclk' will be added to the clock's
propagated skew. (TIM-112)
Information: Input delay ('fall') on clock port 'Sclk' will be added to the clock's
propagated skew. (TIM-112)
Information: Input delay ('rise') on clock port 'Dclk' will be added to the clock's
propagated skew. (TIM-112)
Information: Input delay ('fall') on clock port 'Dclk' will be added to the clock's
propagated skew. (TIM-112)
Warning: Clock network timing may not be up-to-date since only 83.333336 percentage
of clock nets are routed. (TIM-233)
*****
```

```

Report : timing
    -path full
    -delay max
    -max_paths 20
Design : Chip
Version: 0-2018.06-SP2
Date   : Fri Dec 14 16:39:41 2018
*****
```

* Some/all delay information is back-annotated.

```

Operating Conditions: ss_lv62_125c Library: ss_lv62_125c
    Parasitic source : LPE
    Parasitic mode   : RealRVirtualC
    Extraction mode  : MIN_MAX
    Extraction derating : 125/125/125
```

Information: Percent of Arnoldi-based delays = 0.33%

Startpoint: P_MSDAP/CU/SIPO_rst_reg
 (rising edge-triggered flip-flop clocked by Sclk)
 Endpoint: P_MSDAP/SIPO_L/data_out_reg[10]
 (falling edge-triggered flip-flop clocked by Dclk)
 Path Group: Dclk
 Path Type: max

Point	Incr	Path
clock Sclk (rise edge)	37091.11	37091.11
clock network delay (propagated)	2.47	37093.58
P_MSDAP/CU/SIPO_rst_reg/CK (DFFSQX2M)	0.00	37093.58 r
P_MSDAP/CU/SIPO_rst_reg/Q (DFFSQX2M)	0.76	37094.34 f
P_MSDAP/CU/SIPO_rst (controller)	0.00	37094.34 f
P_MSDAP/SIPO_L/rst (SIPO_0)	0.00	37094.34 f
P_MSDAP/SIPO_L/U18/Y (NOR2BX2M)	0.50 *	37094.84 r
P_MSDAP/SIPO_L/U7/Y (NAND2X2M)	0.39 *	37095.22 f
P_MSDAP/SIPO_L/U55/Y (AND2X2M)	0.32 *	37095.55 f
P_MSDAP/SIPO_L/U52/Y (AND2X2M)	0.22 *	37095.77 f
P_MSDAP/SIPO_L/U4/Y (NAND2X2M)	0.15 *	37095.92 r
P_MSDAP/SIPO_L/U21/Y (OAI21X1M)	0.18 *	37096.11 f
P_MSDAP/SIPO_L/data_out_reg[10]/D (DFFNSRHX1M)	0.00 *	37096.11 f
data arrival time		37096.11
clock Dclk (fall edge)	37109.28	37109.28
clock network delay (propagated)	1.60	37110.88
P_MSDAP/SIPO_L/data_out_reg[10]/CKN (DFFNSRHX1M)	0.00	37110.88 f
library setup time	-0.09	37110.79
data required time		37110.79
data required time		37110.79
data arrival time		-37096.11
slack (MET)		14.68

Startpoint: P_MSDAP/CU/SIPO_rst_reg
 (rising edge-triggered flip-flop clocked by Sclk)
 Endpoint: P_MSDAP/SIPO_L/data_out_reg[15]
 (falling edge-triggered flip-flop clocked by Dclk)
 Path Group: Dclk
 Path Type: max

Point	Incr	Path
clock Sclk (rise edge)	37091.11	37091.11
clock network delay (propagated)	2.47	37093.58
P_MSDAP/CU/SIPO_rst_reg/CK (DFFSQX2M)	0.00	37093.58 r
P_MSDAP/CU/SIPO_rst_reg/Q (DFFSQX2M)	0.76	37094.34 f
P_MSDAP/CU/SIPO_rst (controller)	0.00	37094.34 f
P_MSDAP/SIPO_L/rst (SIPO_0)	0.00	37094.34 f
P_MSDAP/SIPO_L/U18/Y (NOR2BX2M)	0.50 *	37094.84 r
P_MSDAP/SIPO_L/U7/Y (NAND2X2M)	0.39 *	37095.22 f
P_MSDAP/SIPO_L/U55/Y (AND2X2M)	0.32 *	37095.55 f
P_MSDAP/SIPO_L/U14/Y (NOR2BX2M)	0.21 *	37095.75 f
P_MSDAP/SIPO_L/U5/Y (NAND2X2M)	0.15 *	37095.91 r
P_MSDAP/SIPO_L/U49/Y (OAI21X1M)	0.18 *	37096.08 f
P_MSDAP/SIPO_L/data_out_reg[15]/D (DFFNSRHX1M)	0.00 *	37096.08 f
data arrival time		37096.08
clock Dclk (fall edge)	37109.28	37109.28
clock network delay (propagated)	1.60	37110.88
P_MSDAP/SIPO_L/data_out_reg[15]/CKN (DFFNSRHX1M)	0.00	37110.88 f
library setup time	-0.09	37110.79
data required time		37110.79

data required time	37110.79
data arrival time	-37096.08

slack (MET)	14.70

Startpoint: P_MSDAP/CU/SIPO_rst_reg
 (rising edge-triggered flip-flop clocked by Sclk)
 Endpoint: P_MSDAP/SIPO_L/data_out_reg[13]
 (falling edge-triggered flip-flop clocked by Dclk)
 Path Group: Dclk
 Path Type: max

Point	Incr	Path
clock Sclk (rise edge)	37091.11	37091.11
clock network delay (propagated)	2.47	37093.58
P_MSDAP/CU/SIPO_rst_reg/CK (DFFSQX2M)	0.00	37093.58 r
P_MSDAP/CU/SIPO_rst_reg/Q (DFFSQX2M)	0.76	37094.34 f
P_MSDAP/CU/SIPO_rst (controller)	0.00	37094.34 f
P_MSDAP/SIPO_L/rst (SIPO_0)	0.00	37094.34 f
P_MSDAP/SIPO_L/U18/Y (NOR2BX2M)	0.50 *	37094.84 r
P_MSDAP/SIPO_L/U7/Y (NAND2X2M)	0.39 *	37095.22 f
P_MSDAP/SIPO_L/U55/Y (AND2X2M)	0.32 *	37095.55 f
P_MSDAP/SIPO_L/U14/Y (NOR2BX2M)	0.21 *	37095.75 f
P_MSDAP/SIPO_L/U9/Y (NAND2X2M)	0.16 *	37095.92 r
P_MSDAP/SIPO_L/U47/Y (OAI21X1M)	0.16 *	37096.08 f
P_MSDAP/SIPO_L/data_out_reg[13]/D (DFFNSRHX1M)	0.00 *	37096.08 f
data arrival time		37096.08

clock Dclk (fall edge)	37109.28	37109.28
clock network delay (propagated)	1.60	37110.88
P_MSDAP/SIPO_L/data_out_reg[13]/CKN (DFFNSRHX1M)	0.00	37110.88 f
library setup time	-0.09	37110.79
data required time		37110.79

data required time		37110.79
data arrival time		-37096.08

slack (MET)		14.71

Startpoint: P_MSDAP/CU/SIPO_rst_reg
 (rising edge-triggered flip-flop clocked by Sclk)
 Endpoint: P_MSDAP/SIPO_L/data_out_reg[9]
 (falling edge-triggered flip-flop clocked by Dclk)
 Path Group: Dclk
 Path Type: max

Point	Incr	Path
clock Sclk (rise edge)	37091.11	37091.11
clock network delay (propagated)	2.47	37093.58
P_MSDAP/CU/SIPO_rst_reg/CK (DFFSQX2M)	0.00	37093.58 r
P_MSDAP/CU/SIPO_rst_reg/Q (DFFSQX2M)	0.76	37094.34 f
P_MSDAP/CU/SIPO_rst (controller)	0.00	37094.34 f
P_MSDAP/SIPO_L/rst (SIPO_0)	0.00	37094.34 f
P_MSDAP/SIPO_L/U18/Y (NOR2BX2M)	0.50 *	37094.84 r
P_MSDAP/SIPO_L/U7/Y (NAND2X2M)	0.39 *	37095.22 f
P_MSDAP/SIPO_L/U55/Y (AND2X2M)	0.32 *	37095.55 f
P_MSDAP/SIPO_L/U52/Y (AND2X2M)	0.22 *	37095.77 f
P_MSDAP/SIPO_L/U11/Y (NAND2X2M)	0.14 *	37095.91 r
P_MSDAP/SIPO_L/U43/Y (OAI21X1M)	0.16 *	37096.08 f
P_MSDAP/SIPO_L/data_out_reg[9]/D (DFFNSRHX1M)	0.00 *	37096.08 f
data arrival time		37096.08

clock Dclk (fall edge)	37109.28	37109.28
clock network delay (propagated)	1.60	37110.88

P_MSDAP/SIPO_L/data_out_reg[9]/CKN (DFFNSRHX1M)	0.00	37110.88	f
library setup time	-0.09	37110.79	
data required time		37110.79	

data required time		37110.79	
data arrival time		-37096.08	

slack (MET)		14.71	

Startpoint: P_MSDAP/CU/SIPO_rst_reg
 (rising edge-triggered flip-flop clocked by Sclk)
 Endpoint: P_MSDAP/SIPO_L/data_out_reg[11]
 (falling edge-triggered flip-flop clocked by Dclk)
 Path Group: Dclk
 Path Type: max

Point	Incr	Path
clock Sclk (rise edge)	37091.11	37091.11
clock network delay (propagated)	2.47	37093.58
P_MSDAP/CU/SIPO_rst_reg/CK (DFFSQX2M)	0.00	37093.58 r
P_MSDAP/CU/SIPO_rst_reg/Q (DFFSQX2M)	0.76	37094.34 f
P_MSDAP/CU/SIPO_rst (controller)	0.00	37094.34 f
P_MSDAP/SIPO_L/rst (SIPO_0)	0.00	37094.34 f
P_MSDAP/SIPO_L/U18/Y (NOR2BX2M)	0.50 *	37094.84 r
P_MSDAP/SIPO_L/U7/Y (NAND2X2M)	0.39 *	37095.22 f
P_MSDAP/SIPO_L/U55/Y (AND2X2M)	0.32 *	37095.55 f
P_MSDAP/SIPO_L/U52/Y (AND2X2M)	0.22 *	37095.77 f
P_MSDAP/SIPO_L/U4/Y (NAND2X2M)	0.15 *	37095.92 r
P_MSDAP/SIPO_L/U45/Y (OAI21X1M)	0.16 *	37096.08 f
P_MSDAP/SIPO_L/data_out_reg[11]/D (DFFNSRHX1M)	0.00 *	37096.08 f
data arrival time		37096.08

clock Dclk (fall edge)	37109.28	37109.28
clock network delay (propagated)	1.60	37110.88
P_MSDAP/SIPO_L/data_out_reg[11]/CKN (DFFNSRHX1M)	0.00	37110.88 f
library setup time	-0.08	37110.79
data required time		37110.79

data required time		37110.79
data arrival time		-37096.08

slack (MET)		14.71

Startpoint: P_MSDAP/CU/SIPO_rst_reg
 (rising edge-triggered flip-flop clocked by Sclk)
 Endpoint: P_MSDAP/SIPO_L/data_out_reg[12]
 (falling edge-triggered flip-flop clocked by Dclk)
 Path Group: Dclk
 Path Type: max

Point	Incr	Path
clock Sclk (rise edge)	37091.11	37091.11
clock network delay (propagated)	2.47	37093.58
P_MSDAP/CU/SIPO_rst_reg/CK (DFFSQX2M)	0.00	37093.58 r
P_MSDAP/CU/SIPO_rst_reg/Q (DFFSQX2M)	0.76	37094.34 f
P_MSDAP/CU/SIPO_rst (controller)	0.00	37094.34 f
P_MSDAP/SIPO_L/rst (SIPO_0)	0.00	37094.34 f
P_MSDAP/SIPO_L/U18/Y (NOR2BX2M)	0.50 *	37094.84 r
P_MSDAP/SIPO_L/U7/Y (NAND2X2M)	0.39 *	37095.22 f
P_MSDAP/SIPO_L/U55/Y (AND2X2M)	0.32 *	37095.55 f
P_MSDAP/SIPO_L/U14/Y (NOR2BX2M)	0.21 *	37095.75 f
P_MSDAP/SIPO_L/U9/Y (NAND2X2M)	0.16 *	37095.92 r
P_MSDAP/SIPO_L/U23/Y (OAI21X1M)	0.16 *	37096.08 f
P_MSDAP/SIPO_L/data_out_reg[12]/D (DFFNSRHX1M)	0.00 *	37096.08 f

data arrival time		37096.08
clock Dclk (fall edge)	37109.28	37109.28
clock network delay (propagated)	1.60	37110.88
P_MSDAP/SIPO_L/data_out_reg[12]/CKN (DFFNSRHX1M)	0.00	37110.88 f
library setup time	-0.09	37110.79
data required time		37110.79

data required time		37110.79
data arrival time		-37096.08

slack (MET)		14.71

Startpoint: P_MSDAP/CU/SIPO_rst_reg
 (rising edge-triggered flip-flop clocked by Sclk)
 Endpoint: P_MSDAP/SIPO_L/data_out_reg[0]
 (falling edge-triggered flip-flop clocked by Dclk)
 Path Group: Dclk
 Path Type: max

Point	Incr	Path
clock Sclk (rise edge)	37091.11	37091.11
clock network delay (propagated)	2.47	37093.58
P_MSDAP/CU/SIPO_rst_reg/CK (DFFSQX2M)	0.00	37093.58 r
P_MSDAP/CU/SIPO_rst_reg/Q (DFFSQX2M)	0.76	37094.34 f
P_MSDAP/CU/SIPO_rst (controller)	0.00	37094.34 f
P_MSDAP/SIPO_L/rst (SIPO_0)	0.00	37094.34 f
P_MSDAP/SIPO_L/U18/Y (NOR2BX2M)	0.50 *	37094.84 r
P_MSDAP/SIPO_L/U7/Y (NAND2X2M)	0.39 *	37095.22 f
P_MSDAP/SIPO_L/U55/Y (AND2X2M)	0.32 *	37095.55 f
P_MSDAP/SIPO_L/U52/Y (AND2X2M)	0.22 *	37095.77 f
P_MSDAP/SIPO_L/U11/Y (NAND2X2M)	0.14 *	37095.91 r
P_MSDAP/SIPO_L/U25/Y (OAI21X1M)	0.15 *	37096.07 f
P_MSDAP/SIPO_L/data_out_reg[0]/D (DFFNSRHX1M)	0.00 *	37096.07 f
data arrival time		37096.07

clock Dclk (fall edge)	37109.28	37109.28
clock network delay (propagated)	1.60	37110.88
P_MSDAP/SIPO_L/data_out_reg[0]/CKN (DFFNSRHX1M)	0.00	37110.88 f
library setup time	-0.09	37110.79
data required time		37110.79

data required time		37110.79
data arrival time		-37096.07

slack (MET)		14.72

Startpoint: P_MSDAP/CU/SIPO_rst_reg
 (rising edge-triggered flip-flop clocked by Sclk)
 Endpoint: P_MSDAP/SIPO_L/data_out_reg[2]
 (falling edge-triggered flip-flop clocked by Dclk)
 Path Group: Dclk
 Path Type: max

Point	Incr	Path
clock Sclk (rise edge)	37091.11	37091.11
clock network delay (propagated)	2.47	37093.58
P_MSDAP/CU/SIPO_rst_reg/CK (DFFSQX2M)	0.00	37093.58 r
P_MSDAP/CU/SIPO_rst_reg/Q (DFFSQX2M)	0.76	37094.34 f
P_MSDAP/CU/SIPO_rst (controller)	0.00	37094.34 f
P_MSDAP/SIPO_L/rst (SIPO_0)	0.00	37094.34 f
P_MSDAP/SIPO_L/U18/Y (NOR2BX2M)	0.50 *	37094.84 r
P_MSDAP/SIPO_L/U7/Y (NAND2X2M)	0.39 *	37095.22 f
P_MSDAP/SIPO_L/U55/Y (AND2X2M)	0.32 *	37095.55 f

P_MSDAP/SIPO_L/U52/Y (AND2X2M)	0.22	*	37095.77	f
P_MSDAP/SIPO_L/U4/Y (NAND2X2M)	0.15	*	37095.92	r
P_MSDAP/SIPO_L/U27/Y (OAI21X1M)	0.15	*	37096.07	f
P_MSDAP/SIPO_L/data_out_reg[2]/D (DFFNSRHX1M)	0.00	*	37096.07	f
data arrival time				37096.07
 clock Dclk (fall edge)	37109.28		37109.28	
clock network delay (propagated)	1.60		37110.88	
P_MSDAP/SIPO_L/data_out_reg[2]/CKN (DFFNSRHX1M)	0.00		37110.88	f
library setup time	-0.09		37110.79	
data required time			37110.79	

data required time			37110.79	
data arrival time			-37096.07	

slack (MET)			14.71	

Startpoint: P_MSDAP/CU/SIPO_rst_reg
 (rising edge-triggered flip-flop clocked by Sclk)
 Endpoint: P_MSDAP/SIPO_L/data_out_reg[8]
 (falling edge-triggered flip-flop clocked by Dclk)
 Path Group: Dclk
 Path Type: max

Point	Incr	Path		
 clock Sclk (rise edge)	37091.11	37091.11		
clock network delay (propagated)	2.47	37093.58		
P_MSDAP/CU/SIPO_rst_reg/CK (DFFSQX2M)	0.00	37093.58 r		
P_MSDAP/CU/SIPO_rst_reg/Q (DFFSQX2M)	0.76	37094.34 f		
P_MSDAP/CU/SIPO_rst (controller)	0.00	37094.34 f		
P_MSDAP/SIPO_L/rst (SIPO_0)	0.00	37094.34 f		
P_MSDAP/SIPO_L/U18/Y (NOR2BX2M)	0.50	*	37094.84 r	
P_MSDAP/SIPO_L/U7/Y (NAND2X2M)	0.39	*	37095.22 f	
P_MSDAP/SIPO_L/U55/Y (AND2X2M)	0.32	*	37095.55 f	
P_MSDAP/SIPO_L/U52/Y (AND2X2M)	0.22	*	37095.77 f	
P_MSDAP/SIPO_L/U11/Y (NAND2X2M)	0.14	*	37095.91 r	
P_MSDAP/SIPO_L/U19/Y (OAI21X1M)	0.16	*	37096.07 f	
P_MSDAP/SIPO_L/data_out_reg[8]/D (DFFNSRHX1M)	0.00	*	37096.07 f	
data arrival time			37096.07	
 clock Dclk (fall edge)	37109.28	37109.28		
clock network delay (propagated)	1.60	37110.88		
P_MSDAP/SIPO_L/data_out_reg[8]/CKN (DFFNSRHX1M)	0.00	37110.88 f		
library setup time	-0.08	37110.79		
data required time			37110.79	

data required time			37110.79	
data arrival time			-37096.07	

slack (MET)			14.72	

Startpoint: P_MSDAP/CU/SIPO_rst_reg
 (rising edge-triggered flip-flop clocked by Sclk)
 Endpoint: P_MSDAP/SIPO_L/data_out_reg[5]
 (falling edge-triggered flip-flop clocked by Dclk)
 Path Group: Dclk
 Path Type: max

Point	Incr	Path
 clock Sclk (rise edge)	37091.11	37091.11
clock network delay (propagated)	2.47	37093.58
P_MSDAP/CU/SIPO_rst_reg/CK (DFFSQX2M)	0.00	37093.58 r
P_MSDAP/CU/SIPO_rst_reg/Q (DFFSQX2M)	0.76	37094.34 f
P_MSDAP/CU/SIPO_rst (controller)	0.00	37094.34 f

P_MSDAP/SIPO_L/rst (SIPO_0)	0.00	37094.34	f	
P_MSDAP/SIPO_L/U18/Y (NOR2BX2M)	0.50	*	37094.84	r
P_MSDAP/SIPO_L/U7/Y (NAND2X2M)	0.39	*	37095.22	f
P_MSDAP/SIPO_L/U55/Y (AND2X2M)	0.32	*	37095.55	f
P_MSDAP/SIPO_L/U14/Y (NOR2BX2M)	0.21	*	37095.75	f
P_MSDAP/SIPO_L/U9/Y (NAND2X2M)	0.16	*	37095.92	r
P_MSDAP/SIPO_L/U37/Y (OAI21X1M)	0.14	*	37096.06	f
P_MSDAP/SIPO_L/data_out_reg[5]/D (DFFNSRHX1M)	0.00	*	37096.06	f
data arrival time			37096.06	
clock Dclk (fall edge)	37109.28	37109.28		
clock network delay (propagated)	1.60	37110.88		
P_MSDAP/SIPO_L/data_out_reg[5]/CKN (DFFNSRHX1M)	0.00	37110.88	f	
library setup time	-0.09	37110.79		
data required time		37110.79		

data required time		37110.79		
data arrival time		-37096.06		

slack (MET)		14.72		

Startpoint: P_MSDAP/CU/SIPO_rst_reg
 (rising edge-triggered flip-flop clocked by Sclk)
 Endpoint: P_MSDAP/SIPO_L/data_out_reg[4]
 (falling edge-triggered flip-flop clocked by Dclk)
 Path Group: Dclk
 Path Type: max

Point	Incr	Path		
clock Sclk (rise edge)	37091.11	37091.11		
clock network delay (propagated)	2.47	37093.58		
P_MSDAP/CU/SIPO_rst_reg/CK (DFFSQX2M)	0.00	37093.58 r		
P_MSDAP/CU/SIPO_rst_reg/Q (DFFSQX2M)	0.76	37094.34 f		
P_MSDAP/CU/SIPO_rst (controller)	0.00	37094.34 f		
P_MSDAP/SIPO_L/rst (SIPO_0)	0.00	37094.34 f		
P_MSDAP/SIPO_L/U18/Y (NOR2BX2M)	0.50	*	37094.84	r
P_MSDAP/SIPO_L/U7/Y (NAND2X2M)	0.39	*	37095.22	f
P_MSDAP/SIPO_L/U55/Y (AND2X2M)	0.32	*	37095.55	f
P_MSDAP/SIPO_L/U14/Y (NOR2BX2M)	0.21	*	37095.75	f
P_MSDAP/SIPO_L/U9/Y (NAND2X2M)	0.16	*	37095.92	r
P_MSDAP/SIPO_L/U29/Y (OAI21X1M)	0.14	*	37096.06	f
P_MSDAP/SIPO_L/data_out_reg[4]/D (DFFNSRHX1M)	0.00	*	37096.06	f
data arrival time		37096.06		
clock Dclk (fall edge)	37109.28	37109.28		
clock network delay (propagated)	1.60	37110.88		
P_MSDAP/SIPO_L/data_out_reg[4]/CKN (DFFNSRHX1M)	0.00	37110.88	f	
library setup time	-0.09	37110.79		
data required time		37110.79		

data required time		37110.79		
data arrival time		-37096.06		

slack (MET)		14.73		

Startpoint: P_MSDAP/CU/SIPO_rst_reg
 (rising edge-triggered flip-flop clocked by Sclk)
 Endpoint: P_MSDAP/SIPO_L/data_out_reg[7]
 (falling edge-triggered flip-flop clocked by Dclk)
 Path Group: Dclk
 Path Type: max

Point	Incr	Path
clock Sclk (rise edge)	37091.11	37091.11

clock network delay (propagated)	2.47	37093.58
P_MSDAP/CU/SIPO_rst_reg/CK (DFFSQX2M)	0.00	37093.58 r
P_MSDAP/CU/SIPO_rst_reg/Q (DFFSQX2M)	0.76	37094.34 f
P_MSDAP/CU/SIPO_rst (controller)	0.00	37094.34 f
P_MSDAP/SIPO_L/rst (SIPO_0)	0.00	37094.34 f
P_MSDAP/SIPO_L/U18/Y (NOR2BX2M)	0.50 *	37094.84 r
P_MSDAP/SIPO_L/U7/Y (NAND2X2M)	0.39 *	37095.22 f
P_MSDAP/SIPO_L/U55/Y (AND2X2M)	0.32 *	37095.55 f
P_MSDAP/SIPO_L/U14/Y (NOR2BX2M)	0.21 *	37095.75 f
P_MSDAP/SIPO_L/U5/Y (NAND2X2M)	0.15 *	37095.91 r
P_MSDAP/SIPO_L/U39/Y (OAI21X1M)	0.15 *	37096.05 f
P_MSDAP/SIPO_L/data_out_reg[7]/D (DFFNSRHX1M)	0.00 *	37096.06 f
data arrival time		37096.06
clock Dclk (fall edge)	37109.28	37109.28
clock network delay (propagated)	1.60	37110.88
P_MSDAP/SIPO_L/data_out_reg[7]/CKN (DFFNSRHX1M)	0.00	37110.88 f
library setup time	-0.09	37110.79
data required time		37110.79
data required time		37110.79
data arrival time		-37096.06
slack (MET)		14.73

Startpoint: P_MSDAP/CU/SIPO_rst_reg
 (rising edge-triggered flip-flop clocked by Sclk)
 Endpoint: P_MSDAP/SIPO_L/data_out_reg[6]
 (falling edge-triggered flip-flop clocked by Dclk)
 Path Group: Dclk
 Path Type: max

Point	Incr	Path
clock Sclk (rise edge)	37091.11	37091.11
clock network delay (propagated)	2.47	37093.58
P_MSDAP/CU/SIPO_rst_reg/CK (DFFSQX2M)	0.00	37093.58 r
P_MSDAP/CU/SIPO_rst_reg/Q (DFFSQX2M)	0.76	37094.34 f
P_MSDAP/CU/SIPO_rst (controller)	0.00	37094.34 f
P_MSDAP/SIPO_L/rst (SIPO_0)	0.00	37094.34 f
P_MSDAP/SIPO_L/U18/Y (NOR2BX2M)	0.50 *	37094.84 r
P_MSDAP/SIPO_L/U7/Y (NAND2X2M)	0.39 *	37095.22 f
P_MSDAP/SIPO_L/U55/Y (AND2X2M)	0.32 *	37095.55 f
P_MSDAP/SIPO_L/U14/Y (NOR2BX2M)	0.21 *	37095.75 f
P_MSDAP/SIPO_L/U5/Y (NAND2X2M)	0.15 *	37095.91 r
P_MSDAP/SIPO_L/U31/Y (OAI21X1M)	0.15 *	37096.05 f
P_MSDAP/SIPO_L/data_out_reg[6]/D (DFFNSRHX1M)	0.00 *	37096.05 f
data arrival time		37096.05
clock Dclk (fall edge)	37109.28	37109.28
clock network delay (propagated)	1.60	37110.88
P_MSDAP/SIPO_L/data_out_reg[6]/CKN (DFFNSRHX1M)	0.00	37110.88 f
library setup time	-0.09	37110.79
data required time		37110.79
data required time		37110.79
data arrival time		-37096.05
slack (MET)		14.73

Startpoint: P_MSDAP/CU/SIPO_rst_reg
 (rising edge-triggered flip-flop clocked by Sclk)
 Endpoint: P_MSDAP/SIPO_L/data_out_reg[3]
 (falling edge-triggered flip-flop clocked by Dclk)
 Path Group: Dclk
 Path Type: max

Point	Incr	Path
clock Sclk (rise edge)	37091.11	37091.11
clock network delay (propagated)	2.47	37093.58
P_MSDAP/CU/SIPO_rst_reg/CK (DFFSQX2M)	0.00	37093.58 r
P_MSDAP/CU/SIPO_rst_reg/Q (DFFSQX2M)	0.76	37094.34 f
P_MSDAP/CU/SIPO_rst (controller)	0.00	37094.34 f
P_MSDAP/SIPO_L/rst (SIPO_0)	0.00	37094.34 f
P_MSDAP/SIPO_L/U18/Y (NOR2BX2M)	0.50	* 37094.84 r
P_MSDAP/SIPO_L/U7/Y (NAND2X2M)	0.39	* 37095.22 f
P_MSDAP/SIPO_L/U55/Y (AND2X2M)	0.32	* 37095.55 f
P_MSDAP/SIPO_L/U52/Y (AND2X2M)	0.22	* 37095.77 f
P_MSDAP/SIPO_L/U4/Y (NAND2X2M)	0.15	* 37095.92 r
P_MSDAP/SIPO_L/U35/Y (OAI21X1M)	0.13	* 37096.05 f
P_MSDAP/SIPO_L/data_out_reg[3]/D (DFFNSRHX1M)	0.00	* 37096.05 f
data arrival time		37096.05
clock Dclk (fall edge)	37109.28	37109.28
clock network delay (propagated)	1.60	37110.88
P_MSDAP/SIPO_L/data_out_reg[3]/CKN (DFFNSRHX1M)	0.00	37110.88 f
library setup time	-0.09	37110.79
data required time		37110.79
data required time		37110.79
data arrival time		-37096.05
slack (MET)		14.74

Startpoint: P_MSDAP/CU/SIPO_rst_reg
(rising edge-triggered flip-flop clocked by Sclk)
Endpoint: P_MSDAP/SIPO_L/data_out_reg[1]
(falling edge-triggered flip-flop clocked by Dclk)
Path Group: Dclk
Path Type: max

Point	Incr	Path
clock Sclk (rise edge)	37091.11	37091.11
clock network delay (propagated)	2.47	37093.58
P_MSDAP/CU/SIPO_rst_reg/CK (DFFSQX2M)	0.00	37093.58 f
P_MSDAP/CU/SIPO_rst_reg/Q (DFFSQX2M)	0.76	37094.34 f
P_MSDAP/CU/SIPO_rst (controller)	0.00	37094.34 f
P_MSDAP/SIPO_L/rst (SIPO_0)	0.00	37094.34 f
P_MSDAP/SIPO_L/U18/Y (NOR2BX2M)	0.50	* 37094.84 r
P_MSDAP/SIPO_L/U7/Y (NAND2X2M)	0.39	* 37095.22 f
P_MSDAP/SIPO_L/U55/Y (AND2X2M)	0.32	* 37095.55 f
P_MSDAP/SIPO_L/U52/Y (AND2X2M)	0.22	* 37095.77 f
P_MSDAP/SIPO_L/U11/Y (NAND2X2M)	0.14	* 37095.91 r
P_MSDAP/SIPO_L/U33/Y (OAI21X1M)	0.14	* 37096.05 f
P_MSDAP/SIPO_L/data_out_reg[1]/D (DFFNSRHX1M)	0.00	* 37096.05 f
data arrival time		37096.05
clock Dclk (fall edge)	37109.28	37109.28
clock network delay (propagated)	1.60	37110.88
P_MSDAP/SIPO_L/data_out_reg[1]/CKN (DFFNSRHX1M)	0.00	37110.88 f
library setup time	-0.09	37110.79
data required time		37110.79
data required time		37110.79
data arrival time		-37096.05
slack (MET)		14.74

Startpoint: P_MSDAP/CU/SIPO_rst_reg
(rising edge-triggered flip-flop clocked by Sclk)

Endpoint: P_MSDAP/SIPO_L/data_out_reg[14]
 (falling edge-triggered flip-flop clocked by Dclk)
 Path Group: Dclk
 Path Type: max

Point	Incr	Path
clock Sclk (rise edge)	37091.11	37091.11
clock network delay (propagated)	2.47	37093.58
P_MSDAP/CU/SIPO_rst_reg/CK (DFFSQX2M)	0.00	37093.58 r
P_MSDAP/CU/SIPO_rst_reg/Q (DFFSQX2M)	0.76	37094.34 f
P_MSDAP/CU/SIPO_rst (controller)	0.00	37094.34 f
P_MSDAP/SIPO_L/rst (SIPO_0)	0.00	37094.34 f
P_MSDAP/SIPO_L/U18/Y (NOR2BX2M)	0.50 *	37094.84 r
P_MSDAP/SIPO_L/U7/Y (NAND2X2M)	0.39 *	37095.22 f
P_MSDAP/SIPO_L/U55/Y (AND2X2M)	0.32 *	37095.55 f
P_MSDAP/SIPO_L/U14/Y (NOR2BX2M)	0.21 *	37095.75 f
P_MSDAP/SIPO_L/U5/Y (NAND2X2M)	0.15 *	37095.91 r
P_MSDAP/SIPO_L/U41/Y (OAI21X1M)	0.13 *	37096.04 f
P_MSDAP/SIPO_L/data_out_reg[14]/D (DFFNSRHX1M)	0.00 *	37096.04 f
data arrival time		37096.04
clock Dclk (fall edge)	37109.28	37109.28
clock network delay (propagated)	1.60	37110.88
P_MSDAP/SIPO_L/data_out_reg[14]/CKN (DFFNSRHX1M)	0.00	37110.88 f
library setup time	-0.09	37110.79
data required time		37110.79
data required time		37110.79
data arrival time		-37096.04
slack (MET)		14.75

Startpoint: P_MSDAP/CU/SIPO_rst_reg
 (rising edge-triggered flip-flop clocked by Sclk)
 Endpoint: P_MSDAP/SIPO_R/data_out_reg[13]
 (falling edge-triggered flip-flop clocked by Dclk)
 Path Group: Dclk
 Path Type: max

Point	Incr	Path
clock Sclk (rise edge)	37091.11	37091.11
clock network delay (propagated)	2.47	37093.58
P_MSDAP/CU/SIPO_rst_reg/CK (DFFSQX2M)	0.00	37093.58 r
P_MSDAP/CU/SIPO_rst_reg/Q (DFFSQX2M)	0.76	37094.34 f
P_MSDAP/CU/SIPO_rst (controller)	0.00	37094.34 f
P_MSDAP/SIPO_R/rst (SIPO_1)	0.00	37094.34 f
P_MSDAP/SIPO_R/U18/Y (NOR2BX2M)	0.47 *	37094.81 r
P_MSDAP/SIPO_R/U7/Y (NAND2X2M)	0.35 *	37095.16 f
P_MSDAP/SIPO_R/U55/Y (AND2X2M)	0.31 *	37095.47 f
P_MSDAP/SIPO_R/U14/Y (NOR2BX2M)	0.20 *	37095.67 f
P_MSDAP/SIPO_R/U9/Y (NAND2X2M)	0.16 *	37095.83 r
P_MSDAP/SIPO_R/U47/Y (OAI21X1M)	0.18 *	37096.01 f
P_MSDAP/SIPO_R/data_out_reg[13]/D (DFFNSRHX1M)	0.00 *	37096.01 f
data arrival time		37096.01
clock Dclk (fall edge)	37109.28	37109.28
clock network delay (propagated)	1.60	37110.88
P_MSDAP/SIPO_R/data_out_reg[13]/CKN (DFFNSRHX1M)	0.00	37110.88 f
library setup time	-0.09	37110.79
data required time		37110.79
data required time		37110.79
data arrival time		-37096.01
slack (MET)		14.77

Startpoint: P_MSDAP/CU/SIPO_rst_reg
 (rising edge-triggered flip-flop clocked by Sclk)
 Endpoint: P_MSDAP/SIPO_R/data_out_reg[15]
 (falling edge-triggered flip-flop clocked by Dclk)
 Path Group: Dclk
 Path Type: max

Point	Incr	Path
clock Sclk (rise edge)	37091.11	37091.11
clock network delay (propagated)	2.47	37093.58
P_MSDAP/CU/SIPO_rst_reg/CK (DFFSQX2M)	0.00	37093.58 r
P_MSDAP/CU/SIPO_rst_reg/Q (DFFSQX2M)	0.76	37094.34 f
P_MSDAP/CU/SIPO_rst (controller)	0.00	37094.34 f
P_MSDAP/SIPO_R/rst (SIPO_1)	0.00	37094.34 f
P_MSDAP/SIPO_R/U18/Y (NOR2BX2M)	0.47 *	37094.81 r
P_MSDAP/SIPO_R/U7/Y (NAND2X2M)	0.35 *	37095.16 f
P_MSDAP/SIPO_R/U55/Y (AND2X2M)	0.31 *	37095.47 f
P_MSDAP/SIPO_R/U14/Y (NOR2BX2M)	0.20 *	37095.67 f
P_MSDAP/SIPO_R/U5/Y (NAND2X2M)	0.15 *	37095.82 r
P_MSDAP/SIPO_R/U49/Y (OAI21X1M)	0.18 *	37096.00 f
P_MSDAP/SIPO_R/data_out_reg[15]/D (DFFNSRHX1M)	0.00 *	37096.00 f
data arrival time		37096.00
clock Dclk (fall edge)	37109.28	37109.28
clock network delay (propagated)	1.60	37110.88
P_MSDAP/SIPO_R/data_out_reg[15]/CKN (DFFNSRHX1M)	0.00	37110.88 f
library setup time	-0.09	37110.79
data required time		37110.79
data required time		37110.79
data arrival time		-37096.00
slack (MET)		14.78

Startpoint: P_MSDAP/CU/SIPO_rst_reg
 (rising edge-triggered flip-flop clocked by Sclk)
 Endpoint: P_MSDAP/SIPO_R/data_out_reg[6]
 (falling edge-triggered flip-flop clocked by Dclk)
 Path Group: Dclk
 Path Type: max

Point	Incr	Path
clock Sclk (rise edge)	37091.11	37091.11
clock network delay (propagated)	2.47	37093.58
P_MSDAP/CU/SIPO_rst_reg/CK (DFFSQX2M)	0.00	37093.58 r
P_MSDAP/CU/SIPO_rst_reg/Q (DFFSQX2M)	0.76	37094.34 f
P_MSDAP/CU/SIPO_rst (controller)	0.00	37094.34 f
P_MSDAP/SIPO_R/rst (SIPO_1)	0.00	37094.34 f
P_MSDAP/SIPO_R/U18/Y (NOR2BX2M)	0.47 *	37094.81 r
P_MSDAP/SIPO_R/U7/Y (NAND2X2M)	0.35 *	37095.16 f
P_MSDAP/SIPO_R/U55/Y (AND2X2M)	0.31 *	37095.47 f
P_MSDAP/SIPO_R/U14/Y (NOR2BX2M)	0.20 *	37095.67 f
P_MSDAP/SIPO_R/U5/Y (NAND2X2M)	0.15 *	37095.82 r
P_MSDAP/SIPO_R/U31/Y (OAI21X1M)	0.18 *	37096.00 f
P_MSDAP/SIPO_R/data_out_reg[6]/D (DFFNSRHX1M)	0.00 *	37096.00 f
data arrival time		37096.00
clock Dclk (fall edge)	37109.28	37109.28
clock network delay (propagated)	1.60	37110.88
P_MSDAP/SIPO_R/data_out_reg[6]/CKN (DFFNSRHX1M)	0.00	37110.88 f
library setup time	-0.10	37110.78
data required time		37110.78

data required time	37110.78	
data arrival time	-37096.00	
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slack (MET)	14.78	
 Startpoint: P_MSDAP/CU/SIPO_rst_reg (rising edge-triggered flip-flop clocked by Sclk)		
Endpoint: P_MSDAP/SIPO_R/data_out_reg[10]	(falling edge-triggered flip-flop clocked by Dclk)	
Path Group:	Dclk	
Path Type:	max	
Point	Incr	Path
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clock Sclk (rise edge)	37091.11	37091.11
clock network delay (propagated)	2.47	37093.58
P_MSDAP/CU/SIPO_rst_reg/CK (DFFSQX2M)	0.00	37093.58 r
P_MSDAP/CU/SIPO_rst_reg/Q (DFFSQX2M)	0.76	37094.34 f
P_MSDAP/CU/SIPO_rst (controller)	0.00	37094.34 f
P_MSDAP/SIPO_R/rst (SIPO_1)	0.00	37094.34 f
P_MSDAP/SIPO_R/U18/Y (NOR2BX2M)	0.47 *	37094.81 r
P_MSDAP/SIPO_R/U7/Y (NAND2X2M)	0.35 *	37095.16 f
P_MSDAP/SIPO_R/U55/Y (AND2X2M)	0.31 *	37095.47 f
P_MSDAP/SIPO_R/U52/Y (AND2X2M)	0.21 *	37095.69 f
P_MSDAP/SIPO_R/U4/Y (NAND2X2M)	0.14 *	37095.82 r
P_MSDAP/SIPO_R/U21/Y (OAI21X1M)	0.18 *	37096.00 f
P_MSDAP/SIPO_R/data_out_reg[10]/D (DFFNSRHX1M)	0.00 *	37096.00 f
data arrival time		37096.00
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clock Dclk (fall edge)	37109.28	37109.28
clock network delay (propagated)	1.60	37110.88
P_MSDAP/SIPO_R/data_out_reg[10]/CKN (DFFNSRHX1M)	0.00	37110.88 f
library setup time	-0.09	37110.79
data required time		37110.79
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data required time	37110.79	
data arrival time	-37096.00	
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slack (MET)	14.79	
 Startpoint: P_MSDAP/SIPO_R/word_ready_reg (falling edge-triggered flip-flop clocked by Dclk)		
Endpoint: P_MSDAP/CU/hw_ptr_R_reg[2]	(rising edge-triggered flip-flop clocked by Sclk)	
Path Group:	Sclk	
Path Type:	max	
Point	Incr	Path
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clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.60	652.64
P_MSDAP/SIPO_R/word_ready_reg/CKN (DFFNSRHX1M)	0.00	652.64 f
P_MSDAP/SIPO_R/word_ready_reg/Q (DFFNSRHX1M)	0.82	653.45 r
P_MSDAP/SIPO_R/word_ready (SIPO_1)	0.00	653.45 r
P_MSDAP/inst_word_ready/b (and2_0)	0.00	653.45 r
P_MSDAP/inst_word_ready/U1/Y (AND2X2M)	0.45 *	653.90 r
P_MSDAP/inst_word_ready/out (and2_0)	0.00	653.90 r
P_MSDAP/CU/word_ready (controller)	0.00	653.90 r
P_MSDAP/CU/U19/Y (INVX1M)	0.36 *	654.26 f
P_MSDAP/CU/U13/Y (NOR2X2M)	0.26 *	654.52 r
P_MSDAP/CU/U42/Y (NOR2X2M)	0.15 *	654.67 f
P_MSDAP/CU/U41/Y (OAI21X1M)	0.13 *	654.80 r
P_MSDAP/CU/U40/Y (OAI21X1M)	0.71 *	655.51 f
P_MSDAP/CU/U12/Y (NAND2BX2M)	0.61 *	656.12 f
P_MSDAP/CU/U196/Y (OAI2BB2X1M)	0.23 *	656.35 r
P_MSDAP/CU/hw_ptr_R_reg[2]/D (DFFRQX2M)	0.00 *	656.35 r

data arrival time		656.35
clock Sclk (rise edge)	669.64	669.64
clock network delay (propagated)	2.47	672.11
P_MSDAP/CU/hw_ptr_R_reg[2]/CK (DFFRQX2M)	0.00	672.11 r
library setup time	-0.26	671.85
data required time		671.85

data required time		671.85
data arrival time		-656.35

slack (MET)		15.50

Startpoint: P_MSDAP/SIPO_R/word_ready_reg
 (falling edge-triggered flip-flop clocked by Dclk)
 Endpoint: P_MSDAP/CU/hw_ptr_R_reg[8]
 (rising edge-triggered flip-flop clocked by Sclk)
 Path Group: Sclk
 Path Type: max

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.60	652.64
P_MSDAP/SIPO_R/word_ready_reg/CKN (DFFNSRHX1M)	0.00	652.64 f
P_MSDAP/SIPO_R/word_ready_reg/Q (DFFNSRHX1M)	0.82	653.45 r
P_MSDAP/SIPO_R/word_ready (SIPO_1)	0.00	653.45 r
P_MSDAP/inst_word_ready/b (and2_0)	0.00	653.45 r
P_MSDAP/inst_word_ready/U1/Y (AND2X2M)	0.45 *	653.90 r
P_MSDAP/inst_word_ready/out (and2_0)	0.00	653.90 r
P_MSDAP/CU/word_ready (controller)	0.00	653.90 r
P_MSDAP/CU/U19/Y (INVX1M)	0.36 *	654.26 f
P_MSDAP/CU/U13/Y (NOR2X2M)	0.26 *	654.52 r
P_MSDAP/CU/U42/Y (NOR2X2M)	0.15 *	654.67 f
P_MSDAP/CU/U41/Y (OAI21X1M)	0.13 *	654.80 r
P_MSDAP/CU/U40/Y (OAI21X1M)	0.71 *	655.51 f
P_MSDAP/CU/U12/Y (NAND2BX2M)	0.61 *	656.12 f
P_MSDAP/CU/U190/Y (OAI2BB2X1M)	0.22 *	656.35 r
P_MSDAP/CU/hw_ptr_R_reg[8]/D (DFFRQX2M)	0.00 *	656.35 r
data arrival time		656.35

clock Sclk (rise edge)	669.64	669.64
clock network delay (propagated)	2.47	672.11
P_MSDAP/CU/hw_ptr_R_reg[8]/CK (DFFRQX2M)	0.00	672.11 r
library setup time	-0.26	671.85
data required time		671.85

data required time		671.85
data arrival time		-656.35

slack (MET)		15.51

Startpoint: P_MSDAP/SIPO_R/word_ready_reg
 (falling edge-triggered flip-flop clocked by Dclk)
 Endpoint: P_MSDAP/CU/hw_ptr_R_reg[3]
 (rising edge-triggered flip-flop clocked by Sclk)
 Path Group: Sclk
 Path Type: max

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.60	652.64
P_MSDAP/SIPO_R/word_ready_reg/CKN (DFFNSRHX1M)	0.00	652.64 f
P_MSDAP/SIPO_R/word_ready_reg/Q (DFFNSRHX1M)	0.82	653.45 r
P_MSDAP/SIPO_R/word_ready (SIPO_1)	0.00	653.45 r

P_MSDAP/inst_word_ready/b (and2_0)	0.00	653.45	r
P_MSDAP/inst_word_ready/U1/Y (AND2X2M)	0.45 *	653.90	r
P_MSDAP/inst_word_ready/out (and2_0)	0.00	653.90	r
P_MSDAP/CU/word_ready (controller)	0.00	653.90	r
P_MSDAP/CU/U19/Y (INVX1M)	0.36 *	654.26	f
P_MSDAP/CU/U13/Y (NOR2X2M)	0.26 *	654.52	r
P_MSDAP/CU/U42/Y (NOR2X2M)	0.15 *	654.67	f
P_MSDAP/CU/U41/Y (OAI21X1M)	0.13 *	654.80	r
P_MSDAP/CU/U40/Y (OAI21X1M)	0.71 *	655.51	f
P_MSDAP/CU/U12/Y (NAND2BX2M)	0.61 *	656.12	f
P_MSDAP/CU/U195/Y (OAI2BB2X1M)	0.22 *	656.34	r
P_MSDAP/CU/hw_ptr_R_reg[3]/D (DFFRQX2M)	0.00 *	656.34	r
data arrival time		656.34	

clock Sclk (rise edge)	669.64	669.64	
clock network delay (propagated)	2.47	672.11	
P_MSDAP/CU/hw_ptr_R_reg[3]/CK (DFFRQX2M)	0.00	672.11	r
library setup time	-0.26	671.85	
data required time		671.85	

data required time		671.85	
data arrival time		-656.34	

slack (MET)		15.51	

Startpoint: P_MSDAP/SIPO_R/word_ready_reg
 (falling edge-triggered flip-flop clocked by Dclk)
 Endpoint: P_MSDAP/CU/hw_ptr_R_reg[1]
 (rising edge-triggered flip-flop clocked by Sclk)
 Path Group: Sclk
 Path Type: max

Point	Incr	Path

clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.60	652.64
P_MSDAP/SIPO_R/word_ready_reg/CKN (DFFNSRHX1M)	0.00	652.64 f
P_MSDAP/SIPO_R/word_ready_reg/Q (DFFNSRHX1M)	0.82	653.45 r
P_MSDAP/SIPO_R/word_ready (SIPO_1)	0.00	653.45 r
P_MSDAP/inst_word_ready/b (and2_0)	0.00	653.45 r
P_MSDAP/inst_word_ready/U1/Y (AND2X2M)	0.45 *	653.90 r
P_MSDAP/inst_word_ready/out (and2_0)	0.00	653.90 r
P_MSDAP/CU/word_ready (controller)	0.00	653.90 r
P_MSDAP/CU/U19/Y (INVX1M)	0.36 *	654.26 f
P_MSDAP/CU/U13/Y (NOR2X2M)	0.26 *	654.52 r
P_MSDAP/CU/U42/Y (NOR2X2M)	0.15 *	654.67 f
P_MSDAP/CU/U41/Y (OAI21X1M)	0.13 *	654.80 r
P_MSDAP/CU/U40/Y (OAI21X1M)	0.71 *	655.51 f
P_MSDAP/CU/U12/Y (NAND2BX2M)	0.61 *	656.12 f
P_MSDAP/CU/U197/Y (OAI2BB2X1M)	0.22 *	656.34 r
P_MSDAP/CU/hw_ptr_R_reg[1]/D (DFFRQX2M)	0.00 *	656.34 r
data arrival time		656.34

clock Sclk (rise edge)	669.64	669.64
clock network delay (propagated)	2.47	672.11
P_MSDAP/CU/hw_ptr_R_reg[1]/CK (DFFRQX2M)	0.00	672.11 r
library setup time	-0.26	671.85
data required time		671.85

data required time		671.85
data arrival time		-656.34

slack (MET)		15.51

Startpoint: P_MSDAP/SIPO_R/word_ready_reg
 (falling edge-triggered flip-flop clocked by Dclk)

Endpoint: P_MSDAP/CU/hw_ptr_R_reg[5]
 (rising edge-triggered flip-flop clocked by Sclk)
 Path Group: Sclk
 Path Type: max

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.60	652.64
P_MSDAP/SIPO_R/word_ready_reg/CKN (DFFNSRHX1M)	0.00	652.64 f
P_MSDAP/SIPO_R/word_ready_reg/Q (DFFNSRHX1M)	0.82	653.45 r
P_MSDAP/SIPO_R/word_ready (SIPO_1)	0.00	653.45 r
P_MSDAP/inst_word_ready/b (and2_0)	0.00	653.45 r
P_MSDAP/inst_word_ready/U1/Y (AND2X2M)	0.45 *	653.90 r
P_MSDAP/inst_word_ready/out (and2_0)	0.00	653.90 r
P_MSDAP/CU/word_ready (controller)	0.00	653.90 r
P_MSDAP/CU/U19/Y (INVX1M)	0.36 *	654.26 f
P_MSDAP/CU/U13/Y (NOR2X2M)	0.26 *	654.52 r
P_MSDAP/CU/U42/Y (NOR2X2M)	0.15 *	654.67 f
P_MSDAP/CU/U41/Y (OAI21X1M)	0.13 *	654.80 r
P_MSDAP/CU/U40/Y (OAI21X1M)	0.71 *	655.51 f
P_MSDAP/CU/U12/Y (NAND2BX2M)	0.61 *	656.12 f
P_MSDAP/CU/U193/Y (OAI2BB2X1M)	0.21 *	656.33 r
P_MSDAP/CU/hw_ptr_R_reg[5]/D (DFFRQX2M)	0.00 *	656.33 r
data arrival time		656.33
clock Sclk (rise edge)	669.64	669.64
clock network delay (propagated)	2.47	672.11
P_MSDAP/CU/hw_ptr_R_reg[5]/CK (DFFRQX2M)	0.00	672.11 r
library setup time	-0.26	671.85
data required time		671.85
data required time		671.85
data arrival time		-656.33
slack (MET)		15.52

Startpoint: P_MSDAP/SIPO_R/word_ready_reg
 (falling edge-triggered flip-flop clocked by Dclk)
 Endpoint: P_MSDAP/CU/hw_ptr_R_reg[4]
 (rising edge-triggered flip-flop clocked by Sclk)
 Path Group: Sclk
 Path Type: max

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.60	652.64
P_MSDAP/SIPO_R/word_ready_reg/CKN (DFFNSRHX1M)	0.00	652.64 f
P_MSDAP/SIPO_R/word_ready_reg/Q (DFFNSRHX1M)	0.82	653.45 r
P_MSDAP/SIPO_R/word_ready (SIPO_1)	0.00	653.45 r
P_MSDAP/inst_word_ready/b (and2_0)	0.00	653.45 r
P_MSDAP/inst_word_ready/U1/Y (AND2X2M)	0.45 *	653.90 r
P_MSDAP/inst_word_ready/out (and2_0)	0.00	653.90 r
P_MSDAP/CU/word_ready (controller)	0.00	653.90 r
P_MSDAP/CU/U19/Y (INVX1M)	0.36 *	654.26 f
P_MSDAP/CU/U13/Y (NOR2X2M)	0.26 *	654.52 r
P_MSDAP/CU/U42/Y (NOR2X2M)	0.15 *	654.67 f
P_MSDAP/CU/U41/Y (OAI21X1M)	0.13 *	654.80 r
P_MSDAP/CU/U40/Y (OAI21X1M)	0.71 *	655.51 f
P_MSDAP/CU/U12/Y (NAND2BX2M)	0.61 *	656.12 f
P_MSDAP/CU/U194/Y (OAI2BB2X1M)	0.21 *	656.33 r
P_MSDAP/CU/hw_ptr_R_reg[4]/D (DFFRQX2M)	0.00 *	656.33 r
data arrival time		656.33
clock Sclk (rise edge)	669.64	669.64
clock network delay (propagated)	2.47	672.11

P_MSDAP/CU/hw_ptr_R_reg[4]/CK (DFFRQX2M)	0.00	672.11 r
library setup time	-0.26	671.85
data required time		671.85

data required time		671.85
data arrival time		-656.33

slack (MET)		15.52

Startpoint: P_MSDAP/SIPO_R/word_ready_reg
 (falling edge-triggered flip-flop clocked by Dclk)
 Endpoint: P_MSDAP/CU/hw_ptr_R_reg[0]
 (rising edge-triggered flip-flop clocked by Sclk)
 Path Group: Sclk
 Path Type: max

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.60	652.64
P_MSDAP/SIPO_R/word_ready_reg/CKN (DFFNSRHX1M)	0.00	652.64 f
P_MSDAP/SIPO_R/word_ready_reg/Q (DFFNSRHX1M)	0.82	653.45 r
P_MSDAP/SIPO_R/word_ready (SIPO_1)	0.00	653.45 r
P_MSDAP/inst_word_ready/b (and2_0)	0.00	653.45 r
P_MSDAP/inst_word_ready/U1/Y (AND2X2M)	0.45 *	653.90 r
P_MSDAP/inst_word_ready/out (and2_0)	0.00	653.90 r
P_MSDAP/CU/word_ready (controller)	0.00	653.90 r
P_MSDAP/CU/U19/Y (INVX1M)	0.36 *	654.26 f
P_MSDAP/CU/U13/Y (NOR2X2M)	0.26 *	654.52 r
P_MSDAP/CU/U42/Y (NOR2X2M)	0.15 *	654.67 f
P_MSDAP/CU/U41/Y (OAI21X1M)	0.13 *	654.80 r
P_MSDAP/CU/U40/Y (OAI21X1M)	0.71 *	655.51 f
P_MSDAP/CU/U12/Y (NAND2BX2M)	0.61 *	656.12 f
P_MSDAP/CU/U198/Y (OAI2BB2X1M)	0.21 *	656.33 r
P_MSDAP/CU/hw_ptr_R_reg[0]/D (DFFRQX2M)	0.00 *	656.33 r
data arrival time		656.33

clock Sclk (rise edge)	669.64	669.64
clock network delay (propagated)	2.47	672.11
P_MSDAP/CU/hw_ptr_R_reg[0]/CK (DFFRQX2M)	0.00	672.11 r
library setup time	-0.26	671.85
data required time		671.85

data required time		671.85
data arrival time		-656.33

slack (MET)		15.53

Startpoint: P_MSDAP/SIPO_R/word_ready_reg
 (falling edge-triggered flip-flop clocked by Dclk)
 Endpoint: P_MSDAP/CU/hw_ptr_R_reg[7]
 (rising edge-triggered flip-flop clocked by Sclk)
 Path Group: Sclk
 Path Type: max

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.60	652.64
P_MSDAP/SIPO_R/word_ready_reg/CKN (DFFNSRHX1M)	0.00	652.64 f
P_MSDAP/SIPO_R/word_ready_reg/Q (DFFNSRHX1M)	0.82	653.45 r
P_MSDAP/SIPO_R/word_ready (SIPO_1)	0.00	653.45 r
P_MSDAP/inst_word_ready/b (and2_0)	0.00	653.45 r
P_MSDAP/inst_word_ready/U1/Y (AND2X2M)	0.45 *	653.90 r
P_MSDAP/inst_word_ready/out (and2_0)	0.00	653.90 r
P_MSDAP/CU/word_ready (controller)	0.00	653.90 r

P_MSDAP/CU/U19/Y (INVX1M)	0.36 *	654.26 f
P_MSDAP/CU/U13/Y (NOR2X2M)	0.26 *	654.52 r
P_MSDAP/CU/U42/Y (NOR2X2M)	0.15 *	654.67 f
P_MSDAP/CU/U41/Y (OAI21X1M)	0.13 *	654.80 r
P_MSDAP/CU/U40/Y (OAI21X1M)	0.71 *	655.51 f
P_MSDAP/CU/U12/Y (NAND2BX2M)	0.61 *	656.12 f
P_MSDAP/CU/U191/Y (OAI2BB2X1M)	0.20 *	656.32 r
P_MSDAP/CU/hw_ptr_R_reg[7]/D (DFFRQX2M)	0.00 *	656.32 r
data arrival time		656.32
clock Sclk (rise edge)	669.64	669.64
clock network delay (propagated)	2.47	672.11
P_MSDAP/CU/hw_ptr_R_reg[7]/CK (DFFRQX2M)	0.00	672.11 r
library setup time	-0.26	671.85
data required time		671.85

data required time		671.85
data arrival time		-656.32

slack (MET)		15.53

Startpoint: P_MSDAP/SIPO_R/word_ready_reg
 (falling edge-triggered flip-flop clocked by Dclk)
 Endpoint: P_MSDAP/CU/hw_ptr_R_reg[6]
 (rising edge-triggered flip-flop clocked by Sclk)
 Path Group: Sclk
 Path Type: max

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.60	652.64
P_MSDAP/SIPO_R/word_ready_reg/CKN (DFFNSRHX1M)	0.00	652.64 f
P_MSDAP/SIPO_R/word_ready_reg/Q (DFFNSRHX1M)	0.82	653.45 r
P_MSDAP/SIPO_R/word_ready (SIPO_1)	0.00	653.45 r
P_MSDAP/inst_word_ready/b (and2_0)	0.00	653.45 r
P_MSDAP/inst_word_ready/U1/Y (AND2X2M)	0.45 *	653.90 r
P_MSDAP/inst_word_ready/out (and2_0)	0.00	653.90 r
P_MSDAP/CU/word_ready (controller)	0.00	653.90 r
P_MSDAP/CU/U19/Y (INVX1M)	0.36 *	654.26 f
P_MSDAP/CU/U13/Y (NOR2X2M)	0.26 *	654.52 r
P_MSDAP/CU/U42/Y (NOR2X2M)	0.15 *	654.67 f
P_MSDAP/CU/U41/Y (OAI21X1M)	0.13 *	654.80 r
P_MSDAP/CU/U40/Y (OAI21X1M)	0.71 *	655.51 f
P_MSDAP/CU/U12/Y (NAND2BX2M)	0.61 *	656.12 f
P_MSDAP/CU/U192/Y (OAI2BB2X1M)	0.20 *	656.32 r
P_MSDAP/CU/hw_ptr_R_reg[6]/D (DFFRQX2M)	0.00 *	656.32 r
data arrival time		656.32
clock Sclk (rise edge)	669.64	669.64
clock network delay (propagated)	2.47	672.11
P_MSDAP/CU/hw_ptr_R_reg[6]/CK (DFFRQX2M)	0.00	672.11 r
library setup time	-0.26	671.85
data required time		671.85

data required time		671.85
data arrival time		-656.32

slack (MET)		15.53

Startpoint: P_MSDAP/SIPO_R/word_ready_reg
 (falling edge-triggered flip-flop clocked by Dclk)
 Endpoint: P_MSDAP/CU/hw_ptr_L_reg[8]
 (rising edge-triggered flip-flop clocked by Sclk)
 Path Group: Sclk
 Path Type: max

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.60	652.64
P_MSDAP/SIPO_R/word_ready_reg/CKN (DFFNSRHX1M)	0.00	652.64 f
P_MSDAP/SIPO_R/word_ready_reg/Q (DFFNSRHX1M)	0.82	653.45 r
P_MSDAP/SIPO_R/word_ready (SIPO_1)	0.00	653.45 r
P_MSDAP/inst_word_ready/b (and2_0)	0.00	653.45 r
P_MSDAP/inst_word_ready/U1/Y (AND2X2M)	0.45 *	653.90 r
P_MSDAP/inst_word_ready/out (and2_0)	0.00	653.90 r
P_MSDAP/CU/word_ready (controller)	0.00	653.90 r
P_MSDAP/CU/U19/Y (INVX1M)	0.36 *	654.26 f
P_MSDAP/CU/U13/Y (NOR2X2M)	0.26 *	654.52 r
P_MSDAP/CU/U42/Y (NOR2X2M)	0.15 *	654.67 f
P_MSDAP/CU/U41/Y (OAI21X1M)	0.13 *	654.80 r
P_MSDAP/CU/U11/Y (OAI2B1X1M)	0.58 *	655.38 f
P_MSDAP/CU/U3/Y (NAND2BX2M)	0.59 *	655.97 f
P_MSDAP/CU/U199/Y (OAI2BB2X1M)	0.24 *	656.21 r
P_MSDAP/CU/hw_ptr_L_reg[8]/D (DFFRQX2M)	0.00 *	656.21 r
data arrival time		656.21
clock Sclk (rise edge)	669.64	669.64
clock network delay (propagated)	2.47	672.11
P_MSDAP/CU/hw_ptr_L_reg[8]/CK (DFFRQX2M)	0.00	672.11 r
library setup time	-0.26	671.85
data required time		671.85
data required time		671.85
data arrival time		-656.21
slack (MET)		15.64

Startpoint: P_MSDAP/SIPO_R/word_ready_reg
 (falling edge-triggered flip-flop clocked by Dclk)
 Endpoint: P_MSDAP/CU/hw_ptr_L_reg[7]
 (rising edge-triggered flip-flop clocked by Sclk)
 Path Group: Sclk
 Path Type: max

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.60	652.64
P_MSDAP/SIPO_R/word_ready_reg/CKN (DFFNSRHX1M)	0.00	652.64 f
P_MSDAP/SIPO_R/word_ready_reg/Q (DFFNSRHX1M)	0.82	653.45 r
P_MSDAP/SIPO_R/word_ready (SIPO_1)	0.00	653.45 r
P_MSDAP/inst_word_ready/b (and2_0)	0.00	653.45 r
P_MSDAP/inst_word_ready/U1/Y (AND2X2M)	0.45 *	653.90 r
P_MSDAP/inst_word_ready/out (and2_0)	0.00	653.90 r
P_MSDAP/CU/word_ready (controller)	0.00	653.90 r
P_MSDAP/CU/U19/Y (INVX1M)	0.36 *	654.26 f
P_MSDAP/CU/U13/Y (NOR2X2M)	0.26 *	654.52 r
P_MSDAP/CU/U42/Y (NOR2X2M)	0.15 *	654.67 f
P_MSDAP/CU/U41/Y (OAI21X1M)	0.13 *	654.80 r
P_MSDAP/CU/U11/Y (OAI2B1X1M)	0.58 *	655.38 f
P_MSDAP/CU/U3/Y (NAND2BX2M)	0.59 *	655.97 f
P_MSDAP/CU/U200/Y (OAI2BB2X1M)	0.23 *	656.20 r
P_MSDAP/CU/hw_ptr_L_reg[7]/D (DFFRQX2M)	0.00 *	656.20 r
data arrival time		656.20
clock Sclk (rise edge)	669.64	669.64
clock network delay (propagated)	2.47	672.11
P_MSDAP/CU/hw_ptr_L_reg[7]/CK (DFFRQX2M)	0.00	672.11 r
library setup time	-0.26	671.85
data required time		671.85

data required time	671.85
data arrival time	-656.20
slack (MET)	15.65

Startpoint: P_MSDAP/SIPO_R/word_ready_reg
 (falling edge-triggered flip-flop clocked by Dclk)
 Endpoint: P_MSDAP/CU/hw_ptr_L_reg[3]
 (rising edge-triggered flip-flop clocked by Sclk)
 Path Group: Sclk
 Path Type: max

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.60	652.64
P_MSDAP/SIPO_R/word_ready_reg/CKN (DFFNSRHX1M)	0.00	652.64 f
P_MSDAP/SIPO_R/word_ready_reg/Q (DFFNSRHX1M)	0.82	653.45 r
P_MSDAP/SIPO_R/word_ready (SIPO_1)	0.00	653.45 r
P_MSDAP/inst_word_ready/b (and2_0)	0.00	653.45 r
P_MSDAP/inst_word_ready/U1/Y (AND2X2M)	0.45 *	653.90 r
P_MSDAP/inst_word_ready/out (and2_0)	0.00	653.90 r
P_MSDAP/CU/word_ready (controller)	0.00	653.90 r
P_MSDAP/CU/U19/Y (INVX1M)	0.36 *	654.26 f
P_MSDAP/CU/U13/Y (NOR2X2M)	0.26 *	654.52 r
P_MSDAP/CU/U42/Y (NOR2X2M)	0.15 *	654.67 f
P_MSDAP/CU/U41/Y (OAI21X1M)	0.13 *	654.80 r
P_MSDAP/CU/U11/Y (OAI2B1X1M)	0.58 *	655.38 f
P_MSDAP/CU/U3/Y (NAND2BX2M)	0.59 *	655.97 f
P_MSDAP/CU/U204/Y (OAI2BB2X1M)	0.22 *	656.19 r
P_MSDAP/CU/hw_ptr_L_reg[3]/D (DFFRQX2M)	0.00 *	656.19 r
data arrival time		656.19
clock Sclk (rise edge)	669.64	669.64
clock network delay (propagated)	2.46	672.10
P_MSDAP/CU/hw_ptr_L_reg[3]/CK (DFFRQX2M)	0.00	672.10 r
library setup time	-0.26	671.84
data required time		671.84
data arrival time		-656.19
slack (MET)		15.65

Startpoint: P_MSDAP/SIPO_R/word_ready_reg
 (falling edge-triggered flip-flop clocked by Dclk)
 Endpoint: P_MSDAP/CU/hw_ptr_L_reg[5]
 (rising edge-triggered flip-flop clocked by Sclk)
 Path Group: Sclk
 Path Type: max

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.60	652.64
P_MSDAP/SIPO_R/word_ready_reg/CKN (DFFNSRHX1M)	0.00	652.64 f
P_MSDAP/SIPO_R/word_ready_reg/Q (DFFNSRHX1M)	0.82	653.45 r
P_MSDAP/SIPO_R/word_ready (SIPO_1)	0.00	653.45 r
P_MSDAP/inst_word_ready/b (and2_0)	0.00	653.45 r
P_MSDAP/inst_word_ready/U1/Y (AND2X2M)	0.45 *	653.90 r
P_MSDAP/inst_word_ready/out (and2_0)	0.00	653.90 r
P_MSDAP/CU/word_ready (controller)	0.00	653.90 r
P_MSDAP/CU/U19/Y (INVX1M)	0.36 *	654.26 f
P_MSDAP/CU/U13/Y (NOR2X2M)	0.26 *	654.52 r
P_MSDAP/CU/U42/Y (NOR2X2M)	0.15 *	654.67 f
P_MSDAP/CU/U41/Y (OAI21X1M)	0.13 *	654.80 r

P_MSDAP/CU/U11/Y (OAI2B1X1M)	0.58 *	655.38 f
P_MSDAP/CU/U3/Y (NAND2BX2M)	0.59 *	655.97 f
P_MSDAP/CU/U202/Y (OAI2BB2X1M)	0.22 *	656.20 r
P_MSDAP/CU/hw_ptr_L_reg[5]/D (DFFRQX2M)	0.00 *	656.20 r
data arrival time		656.20
clock Sclk (rise edge)	669.64	669.64
clock network delay (propagated)	2.47	672.11
P_MSDAP/CU/hw_ptr_L_reg[5]/CK (DFFRQX2M)	0.00	672.11 r
library setup time	-0.26	671.85
data required time		671.85
data required time		671.85
data arrival time		-656.20
slack (MET)		15.65

Startpoint: P_MSDAP/SIPO_R/word_ready_reg
 (falling edge-triggered flip-flop clocked by Dclk)
 Endpoint: P_MSDAP/CU/hw_ptr_L_reg[4]
 (rising edge-triggered flip-flop clocked by Sclk)
 Path Group: Sclk
 Path Type: max

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.60	652.64
P_MSDAP/SIPO_R/word_ready_reg/CKN (DFFNSRHX1M)	0.00	652.64 f
P_MSDAP/SIPO_R/word_ready_reg/Q (DFFNSRHX1M)	0.82	653.45 r
P_MSDAP/SIPO_R/word_ready (SIPO_1)	0.00	653.45 r
P_MSDAP/inst_word_ready/b (and2_0)	0.00	653.45 r
P_MSDAP/inst_word_ready/U1/Y (AND2X2M)	0.45 *	653.90 r
P_MSDAP/inst_word_ready/out (and2_0)	0.00	653.90 r
P_MSDAP/CU/word_ready (controller)	0.00	653.90 r
P_MSDAP/CU/U19/Y (INVX1M)	0.36 *	654.26 f
P_MSDAP/CU/U13/Y (NOR2X2M)	0.26 *	654.52 r
P_MSDAP/CU/U42/Y (NOR2X2M)	0.15 *	654.67 f
P_MSDAP/CU/U41/Y (OAI21X1M)	0.13 *	654.80 r
P_MSDAP/CU/U11/Y (OAI2B1X1M)	0.58 *	655.38 f
P_MSDAP/CU/U3/Y (NAND2BX2M)	0.59 *	655.97 f
P_MSDAP/CU/U203/Y (OAI2BB2X1M)	0.22 *	656.20 r
P_MSDAP/CU/hw_ptr_L_reg[4]/D (DFFRQX2M)	0.00 *	656.20 r
data arrival time		656.20
clock Sclk (rise edge)	669.64	669.64
clock network delay (propagated)	2.47	672.11
P_MSDAP/CU/hw_ptr_L_reg[4]/CK (DFFRQX2M)	0.00	672.11 r
library setup time	-0.26	671.85
data required time		671.85
data required time		671.85
data arrival time		-656.20
slack (MET)		15.66

Startpoint: P_MSDAP/SIPO_R/word_ready_reg
 (falling edge-triggered flip-flop clocked by Dclk)
 Endpoint: P_MSDAP/CU/hw_ptr_L_reg[2]
 (rising edge-triggered flip-flop clocked by Sclk)
 Path Group: Sclk
 Path Type: max

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04

clock network delay (propagated)	1.60	652.64
P_MSDAP/SIPO_R/word_ready_reg/CKN (DFFNSRHX1M)	0.00	652.64 f
P_MSDAP/SIPO_R/word_ready_reg/Q (DFFNSRHX1M)	0.82	653.45 r
P_MSDAP/SIPO_R/word_ready (SIPO_1)	0.00	653.45 r
P_MSDAP/inst_word_ready/b (and2_0)	0.00	653.45 r
P_MSDAP/inst_word_ready/U1/Y (AND2X2M)	0.45 *	653.90 r
P_MSDAP/inst_word_ready/out (and2_0)	0.00	653.90 r
P_MSDAP/CU/word_ready (controller)	0.00	653.90 r
P_MSDAP/CU/U19/Y (INVX1M)	0.36 *	654.26 f
P_MSDAP/CU/U13/Y (NOR2X2M)	0.26 *	654.52 r
P_MSDAP/CU/U42/Y (NOR2X2M)	0.15 *	654.67 f
P_MSDAP/CU/U41/Y (OAI21X1M)	0.13 *	654.80 r
P_MSDAP/CU/U11/Y (OAI2B1X1M)	0.58 *	655.38 f
P_MSDAP/CU/U3/Y (NAND2BX2M)	0.59 *	655.97 f
P_MSDAP/CU/U205/Y (OAI2BB2X1M)	0.22 *	656.19 r
P_MSDAP/CU/hw_ptr_L_reg[2]/D (DFFRQX2M)	0.00 *	656.19 r
data arrival time		656.19

clock Sclk (rise edge)	669.64	669.64
clock network delay (propagated)	2.47	672.11
P_MSDAP/CU/hw_ptr_L_reg[2]/CK (DFFRQX2M)	0.00	672.11 r
library setup time	-0.26	671.85
data required time		671.85

data required time		671.85
data arrival time		-656.19

slack (MET)		15.66

Startpoint: P_MSDAP/SIPO_R/word_ready_reg
 (falling edge-triggered flip-flop clocked by Dclk)
 Endpoint: P_MSDAP/CU/hw_ptr_L_reg[1]
 (rising edge-triggered flip-flop clocked by Sclk)
 Path Group: Sclk
 Path Type: max

Point	Incr	Path

clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.60	652.64
P_MSDAP/SIPO_R/word_ready_reg/CKN (DFFNSRHX1M)	0.00	652.64 f
P_MSDAP/SIPO_R/word_ready_reg/Q (DFFNSRHX1M)	0.82	653.45 r
P_MSDAP/SIPO_R/word_ready (SIPO_1)	0.00	653.45 r
P_MSDAP/inst_word_ready/b (and2_0)	0.00	653.45 r
P_MSDAP/inst_word_ready/U1/Y (AND2X2M)	0.45 *	653.90 r
P_MSDAP/inst_word_ready/out (and2_0)	0.00	653.90 r
P_MSDAP/CU/word_ready (controller)	0.00	653.90 r
P_MSDAP/CU/U19/Y (INVX1M)	0.36 *	654.26 f
P_MSDAP/CU/U13/Y (NOR2X2M)	0.26 *	654.52 r
P_MSDAP/CU/U42/Y (NOR2X2M)	0.15 *	654.67 f
P_MSDAP/CU/U41/Y (OAI21X1M)	0.13 *	654.80 r
P_MSDAP/CU/U11/Y (OAI2B1X1M)	0.58 *	655.38 f
P_MSDAP/CU/U3/Y (NAND2BX2M)	0.59 *	655.97 f
P_MSDAP/CU/U206/Y (OAI2BB2X1M)	0.21 *	656.19 r
P_MSDAP/CU/hw_ptr_L_reg[1]/D (DFFRQX2M)	0.00 *	656.19 r
data arrival time		656.19

clock Sclk (rise edge)	669.64	669.64
clock network delay (propagated)	2.47	672.11
P_MSDAP/CU/hw_ptr_L_reg[1]/CK (DFFRQX2M)	0.00	672.11 r
library setup time	-0.26	671.85
data required time		671.85

data required time		671.85
data arrival time		-656.19

slack (MET)		15.67

Startpoint: P_MSDAP/SIPO_R/word_ready_reg
 (falling edge-triggered flip-flop clocked by Dclk)
 Endpoint: P_MSDAP/CU/hw_ptr_L_reg[6]
 (rising edge-triggered flip-flop clocked by Sclk)
 Path Group: Sclk
 Path Type: max

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.60	652.64
P_MSDAP/SIPO_R/word_ready_reg/CKN (DFFNSRHX1M)	0.00	652.64 f
P_MSDAP/SIPO_R/word_ready_reg/Q (DFFNSRHX1M)	0.82	653.45 r
P_MSDAP/SIPO_R/word_ready (SIPO_1)	0.00	653.45 r
P_MSDAP/inst_word_ready/b (and2_0)	0.00	653.45 r
P_MSDAP/inst_word_ready/U1/Y (AND2X2M)	0.45 *	653.90 r
P_MSDAP/inst_word_ready/out (and2_0)	0.00	653.90 r
P_MSDAP/CU/word_ready (controller)	0.00	653.90 r
P_MSDAP/CU/U19/Y (INVX1M)	0.36 *	654.26 f
P_MSDAP/CU/U13/Y (NOR2X2M)	0.26 *	654.52 r
P_MSDAP/CU/U42/Y (NOR2X2M)	0.15 *	654.67 f
P_MSDAP/CU/U41/Y (OAI21X1M)	0.13 *	654.80 r
P_MSDAP/CU/U11/Y (OAI2B1X1M)	0.58 *	655.38 f
P_MSDAP/CU/U3/Y (NAND2BX2M)	0.59 *	655.97 f
P_MSDAP/CU/U201/Y (OAI2BB2X1M)	0.21 *	656.18 r
P_MSDAP/CU/hw_ptr_L_reg[6]/D (DFFRQX2M)	0.00 *	656.18 r
data arrival time		656.18
clock Sclk (rise edge)	669.64	669.64
clock network delay (propagated)	2.47	672.11
P_MSDAP/CU/hw_ptr_L_reg[6]/CK (DFFRQX2M)	0.00	672.11 r
library setup time	-0.26	671.85
data required time		671.85
data required time		671.85
data arrival time		-656.18
slack (MET)		15.67

Startpoint: P_MSDAP/SIPO_R/word_ready_reg
 (falling edge-triggered flip-flop clocked by Dclk)
 Endpoint: P_MSDAP/CU/hw_ptr_L_reg[0]
 (rising edge-triggered flip-flop clocked by Sclk)
 Path Group: Sclk
 Path Type: max

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.60	652.64
P_MSDAP/SIPO_R/word_ready_reg/CKN (DFFNSRHX1M)	0.00	652.64 f
P_MSDAP/SIPO_R/word_ready_reg/Q (DFFNSRHX1M)	0.82	653.45 r
P_MSDAP/SIPO_R/word_ready (SIPO_1)	0.00	653.45 r
P_MSDAP/inst_word_ready/b (and2_0)	0.00	653.45 r
P_MSDAP/inst_word_ready/U1/Y (AND2X2M)	0.45 *	653.90 r
P_MSDAP/inst_word_ready/out (and2_0)	0.00	653.90 r
P_MSDAP/CU/word_ready (controller)	0.00	653.90 r
P_MSDAP/CU/U19/Y (INVX1M)	0.36 *	654.26 f
P_MSDAP/CU/U13/Y (NOR2X2M)	0.26 *	654.52 r
P_MSDAP/CU/U42/Y (NOR2X2M)	0.15 *	654.67 f
P_MSDAP/CU/U41/Y (OAI21X1M)	0.13 *	654.80 r
P_MSDAP/CU/U11/Y (OAI2B1X1M)	0.58 *	655.38 f
P_MSDAP/CU/U3/Y (NAND2BX2M)	0.59 *	655.97 f
P_MSDAP/CU/U207/Y (OAI2BB2X1M)	0.21 *	656.18 r
P_MSDAP/CU/hw_ptr_L_reg[0]/D (DFFRQX2M)	0.00 *	656.18 r

data arrival time		656.18
clock Sclk (rise edge)	669.64	669.64
clock network delay (propagated)	2.47	672.11
P_MSDAP/CU/hw_ptr_L_reg[0]/CK (DFFRQX2M)	0.00	672.11 r
library setup time	-0.26	671.85
data required time		671.85

data required time		671.85
data arrival time		-656.18

slack (MET)		15.67

Startpoint: P_MSDAP/SIPO_R/word_ready_reg
 (falling edge-triggered flip-flop clocked by Dclk)
 Endpoint: P_MSDAP/CU/xw_ptr_R_reg[7]
 (rising edge-triggered flip-flop clocked by Sclk)
 Path Group: Sclk
 Path Type: max

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.60	652.64
P_MSDAP/SIPO_R/word_ready_reg/CKN (DFFNSRHX1M)	0.00	652.64 f
P_MSDAP/SIPO_R/word_ready_reg/Q (DFFNSRHX1M)	0.82	653.45 r
P_MSDAP/SIPO_R/word_ready(SIPO_1)	0.00	653.45 r
P_MSDAP/inst_word_ready/b (and2_0)	0.00	653.45 r
P_MSDAP/inst_word_ready/U1/Y (AND2X2M)	0.45 *	653.90 r
P_MSDAP/inst_word_ready/out (and2_0)	0.00	653.90 r
P_MSDAP/CU/word_ready(controller)	0.00	653.90 r
P_MSDAP/CU/U355/Y (OAI21X1M)	0.22 *	654.12 f
P_MSDAP/CU/U356/Y (OAI21X1M)	0.21 *	654.32 r
P_MSDAP/CU/U357/Y (AOI32X1M)	0.15 *	654.48 f
P_MSDAP/CU/U358/Y (OAI21X1M)	0.15 *	654.62 r
P_MSDAP/CU/U359/Y (AOI22X1M)	0.22 *	654.84 f
P_MSDAP/CU/U360/Y (OAI21X1M)	0.14 *	654.97 r
P_MSDAP/CU/U141/Y (NAND2X2M)	0.33 *	655.30 f
P_MSDAP/CU/U34/Y (NOR2X2M)	0.45 *	655.76 r
P_MSDAP/CU/U158/Y (AOI22X1M)	0.30 *	656.06 f
P_MSDAP/CU/U157/Y (OAI2BB1X2M)	0.12 *	656.18 r
P_MSDAP/CU/xw_ptr_R_reg[7]/D (DFFRQX2M)	0.00 *	656.18 r
data arrival time		656.18

clock Sclk (rise edge)	669.64	669.64
clock network delay (propagated)	2.47	672.11
P_MSDAP/CU/xw_ptr_R_reg[7]/CK (DFFRQX2M)	0.00	672.11 r
library setup time	-0.25	671.86
data required time		671.86

data required time		671.86
data arrival time		-656.18

slack (MET)		15.68

Startpoint: P_MSDAP/SIPO_R/word_ready_reg
 (falling edge-triggered flip-flop clocked by Dclk)
 Endpoint: P_MSDAP/CU/xw_ptr_R_reg[0]
 (rising edge-triggered flip-flop clocked by Sclk)
 Path Group: Sclk
 Path Type: max

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.60	652.64

P_MSDAP/SIPO_R/word_ready_reg/CKN (DFFNSRHX1M)	0.00	652.64	f
P_MSDAP/SIPO_R/word_ready_reg/Q (DFFNSRHX1M)	0.82	653.45	r
P_MSDAP/SIPO_R/word_ready (SIPO_1)	0.00	653.45	r
P_MSDAP/inst_word_ready/b (and2_0)	0.00	653.45	r
P_MSDAP/inst_word_ready/U1/Y (AND2X2M)	0.45 *	653.90	r
P_MSDAP/inst_word_ready/out (and2_0)	0.00	653.90	r
P_MSDAP/CU/word_ready (controller)	0.00	653.90	r
P_MSDAP/CU/U355/Y (OAI21X1M)	0.22 *	654.12	f
P_MSDAP/CU/U356/Y (OAI21X1M)	0.21 *	654.32	r
P_MSDAP/CU/U357/Y (AOI32X1M)	0.15 *	654.48	f
P_MSDAP/CU/U358/Y (OAI21X1M)	0.15 *	654.62	r
P_MSDAP/CU/U359/Y (AOI22X1M)	0.22 *	654.84	f
P_MSDAP/CU/U360/Y (OAI21X1M)	0.14 *	654.97	r
P_MSDAP/CU/U141/Y (NAND2X2M)	0.33 *	655.30	f
P_MSDAP/CU/U34/Y (NOR2X2M)	0.45 *	655.76	r
P_MSDAP/CU/U144/Y (AOI22X1M)	0.29 *	656.05	f
P_MSDAP/CU/U143/Y (OAI2BB1X2M)	0.13 *	656.18	r
P_MSDAP/CU/xw_ptr_R_reg[0]/D (DFFRQX2M)	0.00 *	656.18	r
data arrival time		656.18	
clock Sclk (rise edge)	669.64	669.64	
clock network delay (propagated)	2.47	672.11	
P_MSDAP/CU/xw_ptr_R_reg[0]/CK (DFFRQX2M)	0.00	672.11	r
library setup time	-0.25	671.86	
data required time		671.86	
data required time		671.86	
data arrival time		-656.18	
slack (MET)		15.68	

1

D.4. Hold timing report

Warning: Clock network timing may not be up-to-date since only 83.333336 percentage of clock nets are routed. (TIM-233)

```
*****
Report : timing
    -path full
    -delay min
    -max_paths 20
Design : Chip
Version: O-2018.06-SP2
Date   : Fri Dec 14 16:39:41 2018
*****
```

* Some/all delay information is back-annotated.

Operating Conditions: ff_1v98_0c Library: ff_1v98_0c
Parasitic source : LPE
Parasitic mode : RealRVirtualC
Extraction mode : MIN MAX
Extraction derating : 125/125/125

Information: Percent of Arnoldi-based delays = 0.33%

Startpoint: P_MSDAP/SIPO_R/bt_reg[0]
(falling edge-triggered flip-flop clocked by Dclk)
Endpoint: P_MSDAP/SIPO_R/bt_reg[0]
(falling edge-triggered flip-flop clocked by Dclk)
Path Group: Dclk
Path Type: min

Point	Incr	Path
-------	------	------

clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_R/bt_reg[0]/CKN (DFFNSRHX1M)	0.00	652.27 f
P_MSDAP/SIPO_R/bt_reg[0]/Q (DFFNSRHX1M)	0.76	653.03 f
P_MSDAP/SIPO_R/U16/Y (OAI2B2X2M)	0.18 *	653.21 r
P_MSDAP/SIPO_R/bt_reg[0]/D (DFFNSRHX1M)	0.00 *	653.21 r
data arrival time		653.21
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_R/bt_reg[0]/CKN (DFFNSRHX1M)	0.00	652.27 f
library hold time	0.16	652.44
data required time		652.44
data required time		652.44
data arrival time		-653.21
slack (MET)		0.77

Startpoint: P_MSDAP/SIPO_L/bt_reg[0]
 (falling edge-triggered flip-flop clocked by Dclk)

Endpoint: P_MSDAP/SIPO_L/bt_reg[0]
 (falling edge-triggered flip-flop clocked by Dclk)

Path Group: Dclk

Path Type: min

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_L/bt_reg[0]/CKN (DFFNSRHX1M)	0.00	652.27 f
P_MSDAP/SIPO_L/bt_reg[0]/Q (DFFNSRHX1M)	0.76	653.04 f
P_MSDAP/SIPO_L/U16/Y (OAI2B2X2M)	0.19 *	653.23 r
P_MSDAP/SIPO_L/bt_reg[0]/D (DFFNSRHX1M)	0.00 *	653.23 r
data arrival time		653.23
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_L/bt_reg[0]/CKN (DFFNSRHX1M)	0.00	652.27 f
library hold time	0.16	652.44
data required time		652.44
data required time		652.44
data arrival time		-653.23
slack (MET)		0.79

Startpoint: P_MSDAP/SIPO_L/bt_reg[2]
 (falling edge-triggered flip-flop clocked by Dclk)

Endpoint: P_MSDAP/SIPO_L/bt_reg[2]
 (falling edge-triggered flip-flop clocked by Dclk)

Path Group: Dclk

Path Type: min

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_L/bt_reg[2]/CKN (DFFNSRHX1M)	0.00	652.27 f
P_MSDAP/SIPO_L/bt_reg[2]/Q (DFFNSRHX1M)	0.60	652.88 f
P_MSDAP/SIPO_L/U61/S (ADDHX1M)	0.17 *	653.05 r
P_MSDAP/SIPO_L/U15/Y (OAI2BB2X1M)	0.22 *	653.26 r
P_MSDAP/SIPO_L/bt_reg[2]/D (DFFNSRHX1M)	0.00 *	653.26 r
data arrival time		653.26

clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_L/bt_reg[2]/CKN (DFFNSRHX1M)	0.00	652.27 f
library hold time	0.17	652.44
data required time		652.44

data required time		652.44
data arrival time		-653.26

slack (MET)		0.82

Startpoint: P_MSDAP/SIPO_L/word_ready_reg
 (falling edge-triggered flip-flop clocked by Dclk)
 Endpoint: P_MSDAP/SIPO_L/word_ready_reg
 (falling edge-triggered flip-flop clocked by Dclk)
 Path Group: Dclk
 Path Type: min

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_L/word_ready_reg/CKN (DFFNSRHX1M)	0.00	652.27 f
P_MSDAP/SIPO_L/word_ready_reg/Q (DFFNSRHX1M)	0.78	653.06 r
P_MSDAP/SIPO_L/U54/Y (AO2B2X2M)	0.22 *	653.28 r
P_MSDAP/SIPO_L/word_ready_reg/D (DFFNSRHX1M)	0.00 *	653.28 r
data arrival time		653.28

clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_L/word_ready_reg/CKN (DFFNSRHX1M)	0.00	652.27 f
library hold time	0.17	652.44
data required time		652.44

data required time		652.44
data arrival time		-653.28

slack (MET)		0.83

Startpoint: P_MSDAP/SIPO_R/bt_reg[2]
 (falling edge-triggered flip-flop clocked by Dclk)
 Endpoint: P_MSDAP/SIPO_R/bt_reg[2]
 (falling edge-triggered flip-flop clocked by Dclk)
 Path Group: Dclk
 Path Type: min

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_R/bt_reg[2]/CKN (DFFNSRHX1M)	0.00	652.27 f
P_MSDAP/SIPO_R/bt_reg[2]/Q (DFFNSRHX1M)	0.60	652.88 f
P_MSDAP/SIPO_R/U61/S (ADDHX1M)	0.18 *	653.06 r
P_MSDAP/SIPO_R/U15/Y (OAI2BB2X1M)	0.22 *	653.28 r
P_MSDAP/SIPO_R/bt_reg[2]/D (DFFNSRHX1M)	0.00 *	653.28 r
data arrival time		653.28

clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_R/bt_reg[2]/CKN (DFFNSRHX1M)	0.00	652.27 f
library hold time	0.17	652.44
data required time		652.44

data required time		652.44
data arrival time		-653.28

slack (MET) 0.84

Startpoint: P_MSDAP/SIPO_R/word_ready_reg
(falling edge-triggered flip-flop clocked by Dclk)
Endpoint: P_MSDAP/SIPO_R/word_ready_reg
(falling edge-triggered flip-flop clocked by Dclk)
Path Group: Dclk
Path Type: min

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_R/word_ready_reg/CKN (DFFNSRHX1M)	0.00	652.27 f
P_MSDAP/SIPO_R/word_ready_reg/Q (DFFNSRHX1M)	0.80	653.08 r
P_MSDAP/SIPO_R/U54/Y (AO2B2X2M)	0.23 *	653.30 r
P_MSDAP/SIPO_R/word_ready_reg/D (DFFNSRHX1M)	0.00 *	653.30 r
data arrival time		653.30
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_R/word_ready_reg/CKN (DFFNSRHX1M)	0.00	652.27 f
library hold time	0.17	652.44
data required time		652.44
data required time		652.44
data arrival time		-653.30
slack (MET)		0.86

Startpoint: P_MSDAP/SIPO_R/bt_reg[3]
(falling edge-triggered flip-flop clocked by Dclk)
Endpoint: P_MSDAP/SIPO_R/bt_reg[3]
(falling edge-triggered flip-flop clocked by Dclk)
Path Group: Dclk
Path Type: min

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_R/bt_reg[3]/CKN (DFFNSRHX1M)	0.00	652.27 f
P_MSDAP/SIPO_R/bt_reg[3]/Q (DFFNSRHX1M)	0.71	652.99 f
P_MSDAP/SIPO_R/U62/S (ADDHX1M)	0.20 *	653.19 r
P_MSDAP/SIPO_R/U17/Y (OAI2BB2X1M)	0.22 *	653.41 r
P_MSDAP/SIPO_R/bt_reg[3]/D (DFFNSRHX1M)	0.00 *	653.41 r
data arrival time		653.41
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_R/bt_reg[3]/CKN (DFFNSRHX1M)	0.00	652.27 f
library hold time	0.17	652.44
data required time		652.44
data required time		652.44
data arrival time		-653.41
slack (MET)		0.96

Startpoint: P_MSDAP/SIPO_R/bt_reg[0]
(falling edge-triggered flip-flop clocked by Dclk)
Endpoint: P_MSDAP/SIPO_R/bt_reg[1]
(falling edge-triggered flip-flop clocked by Dclk)
Path Group: Dclk
Path Type: min

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_R/bt_reg[0]/CKN (DFFNSRHX1M)	0.00	652.27 f
P_MSDAP/SIPO_R/bt_reg[0]/Q (DFFNSRHX1M)	0.76	653.03 f
P_MSDAP/SIPO_R/U60/S (ADDHX1M)	0.16 *	653.19 r
P_MSDAP/SIPO_R/U12/Y (OAI2BB2X1M)	0.22 *	653.41 r
P_MSDAP/SIPO_R/bt_reg[1]/D (DFFNSRHX1M)	0.00 *	653.41 r
data arrival time		653.41
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_R/bt_reg[1]/CKN (DFFNSRHX1M)	0.00	652.27 f
library hold time	0.17	652.44
data required time		652.44
data required time		652.44
data arrival time		-653.41
slack (MET)		0.97

Startpoint: P_MSDAP/SIPO_L/bt_reg[3]
 (falling edge-triggered flip-flop clocked by Dclk)
 Endpoint: P_MSDAP/SIPO_L/bt_reg[3]
 (falling edge-triggered flip-flop clocked by Dclk)
 Path Group: Dclk
 Path Type: min

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_L/bt_reg[3]/CKN (DFFNSRHX1M)	0.00	652.27 f
P_MSDAP/SIPO_L/bt_reg[3]/Q (DFFNSRHX1M)	0.72	652.99 f
P_MSDAP/SIPO_L/U62/S (ADDHX1M)	0.20 *	653.20 r
P_MSDAP/SIPO_L/U17/Y (OAI2BB2X1M)	0.22 *	653.42 r
P_MSDAP/SIPO_L/bt_reg[3]/D (DFFNSRHX1M)	0.00 *	653.42 r
data arrival time		653.42
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_L/bt_reg[3]/CKN (DFFNSRHX1M)	0.00	652.27 f
library hold time	0.17	652.44
data required time		652.44
data required time		652.44
data arrival time		-653.42
slack (MET)		0.97

Startpoint: P_MSDAP/SIPO_L/bt_reg[0]
 (falling edge-triggered flip-flop clocked by Dclk)
 Endpoint: P_MSDAP/SIPO_L/bt_reg[1]
 (falling edge-triggered flip-flop clocked by Dclk)
 Path Group: Dclk
 Path Type: min

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_L/bt_reg[0]/CKN (DFFNSRHX1M)	0.00	652.27 f
P_MSDAP/SIPO_L/bt_reg[0]/Q (DFFNSRHX1M)	0.76	653.04 f
P_MSDAP/SIPO_L/U60/S (ADDHX1M)	0.17 *	653.21 r

P_MSDAP/SIPO_L/U12/Y (OAI2BB2X1M)	0.22 *	653.43	r
P_MSDAP/SIPO_L/bt_reg[1]/D (DFFNSRHX1M)	0.00 *	653.43	r
data arrival time		653.43	
clock Dclk (fall edge)	651.04	651.04	
clock network delay (propagated)	1.23	652.27	
P_MSDAP/SIPO_L/bt_reg[1]/CKN (DFFNSRHX1M)	0.00	652.27	f
library hold time	0.17	652.44	
data required time		652.44	

data required time		652.44	
data arrival time		-653.43	

slack (MET)		0.99	

Startpoint: P_MSDAP/SIPO_R/data_out_reg[15]
 (falling edge-triggered flip-flop clocked by Dclk)
 Endpoint: P_MSDAP/SIPO_R/data_out_reg[15]
 (falling edge-triggered flip-flop clocked by Dclk)
 Path Group: Dclk
 Path Type: min

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_R/data_out_reg[15]/CKN (DFFNSRHX1M)	0.00	652.27 f
P_MSDAP/SIPO_R/data_out_reg[15]/Q (DFFNSRHX1M)	0.90	653.18 r
P_MSDAP/SIPO_R/U50/Y (OAI21X1M)	0.19 *	653.36 f
P_MSDAP/SIPO_R/U49/Y (OAI21X1M)	0.10 *	653.47 r
P_MSDAP/SIPO_R/data_out_reg[15]/D (DFFNSRHX1M)	0.00 *	653.47 r
data arrival time		653.47
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_R/data_out_reg[15]/CKN (DFFNSRHX1M)	0.00	652.27 f
library hold time	0.17	652.44
data required time		652.44

data required time		652.44
data arrival time		-653.47

slack (MET)		1.03

Startpoint: P_MSDAP/SIPO_R/data_out_reg[10]
 (falling edge-triggered flip-flop clocked by Dclk)
 Endpoint: P_MSDAP/SIPO_R/data_out_reg[10]
 (falling edge-triggered flip-flop clocked by Dclk)
 Path Group: Dclk
 Path Type: min

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.24	652.27
P_MSDAP/SIPO_R/data_out_reg[10]/CKN (DFFNSRHX1M)	0.00	652.27 f
P_MSDAP/SIPO_R/data_out_reg[10]/Q (DFFNSRHX1M)	0.92	653.20 r
P_MSDAP/SIPO_R/U22/Y (OAI21X1M)	0.18 *	653.38 f
P_MSDAP/SIPO_R/U21/Y (OAI21X1M)	0.10 *	653.48 r
P_MSDAP/SIPO_R/data_out_reg[10]/D (DFFNSRHX1M)	0.00 *	653.48 r
data arrival time		653.48
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.24	652.27
P_MSDAP/SIPO_R/data_out_reg[10]/CKN (DFFNSRHX1M)	0.00	652.27 f
library hold time	0.17	652.44

data required time	652.44

data required time	652.44
data arrival time	-653.48

slack (MET)	1.04

Startpoint: P_MSDAP/SIPO_R/bt_reg[1]
 (falling edge-triggered flip-flop clocked by Dclk)
 Endpoint: P_MSDAP/SIPO_R/data_out_reg[14]
 (falling edge-triggered flip-flop clocked by Dclk)
 Path Group: Dclk
 Path Type: min

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_R/bt_reg[1]/CKN (DFFNSRHX1M)	0.00	652.27 f
P_MSDAP/SIPO_R/bt_reg[1]/Q (DFFNSRHX1M)	0.87	653.14 r
P_MSDAP/SIPO_R/U5/Y (NAND2X2M)	0.17 *	653.32 f
P_MSDAP/SIPO_R/U41/Y (OAI21X1M)	0.18 *	653.49 r
P_MSDAP/SIPO_R/data_out_reg[14]/D (DFFNSRHX1M)	0.00 *	653.49 r
data arrival time		653.49

clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.24	652.27
P_MSDAP/SIPO_R/data_out_reg[14]/CKN (DFFNSRHX1M)	0.00	652.27 f
library hold time	0.17	652.44
data required time		652.44

data required time		652.44
data arrival time		-653.49

slack (MET)		1.05

Startpoint: P_MSDAP/SIPO_L/bt_reg[3]
 (falling edge-triggered flip-flop clocked by Dclk)
 Endpoint: P_MSDAP/SIPO_L/data_out_reg[8]
 (falling edge-triggered flip-flop clocked by Dclk)
 Path Group: Dclk
 Path Type: min

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_L/bt_reg[3]/CKN (DFFNSRHX1M)	0.00	652.27 f
P_MSDAP/SIPO_L/bt_reg[3]/Q (DFFNSRHX1M)	0.72	652.99 f
P_MSDAP/SIPO_L/U58/Y (NAND3X2M)	0.27 *	653.27 r
P_MSDAP/SIPO_L/U20/Y (OAI21X1M)	0.14 *	653.40 f
P_MSDAP/SIPO_L/U19/Y (OAI21X1M)	0.09 *	653.49 r
P_MSDAP/SIPO_L/data_out_reg[8]/D (DFFNSRHX1M)	0.00 *	653.49 r
data arrival time		653.49

clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_L/data_out_reg[8]/CKN (DFFNSRHX1M)	0.00	652.27 f
library hold time	0.17	652.44
data required time		652.44

data required time		652.44
data arrival time		-653.49

slack (MET)		1.05

Startpoint: P_MSDAP/SIPO_L/bt_reg[3]
 (falling edge-triggered flip-flop clocked by Dclk)
 Endpoint: P_MSDAP/SIPO_L/data_out_reg[12]
 (falling edge-triggered flip-flop clocked by Dclk)
 Path Group: Dclk
 Path Type: min

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_L/bt_reg[3]/CKN (DFFNSRHX1M)	0.00	652.27 f
P_MSDAP/SIPO_L/bt_reg[3]/Q (DFFNSRHX1M)	0.72	652.99 f
P_MSDAP/SIPO_L/U58/Y (NAND3X2M)	0.27 *	653.27 r
P_MSDAP/SIPO_L/U24/Y (OAI21X1M)	0.14 *	653.40 f
P_MSDAP/SIPO_L/U23/Y (OAI21X1M)	0.09 *	653.50 r
P_MSDAP/SIPO_L/data_out_reg[12]/D (DFFNSRHX1M)	0.00 *	653.50 r
data arrival time		653.50
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_L/data_out_reg[12]/CKN (DFFNSRHX1M)	0.00	652.27 f
library hold time	0.17	652.44
data required time		652.44
data required time		652.44
data arrival time		-653.50
slack (MET)		1.05

Startpoint: P_MSDAP/SIPO_R/data_out_reg[9]
 (falling edge-triggered flip-flop clocked by Dclk)
 Endpoint: P_MSDAP/SIPO_R/data_out_reg[9]
 (falling edge-triggered flip-flop clocked by Dclk)
 Path Group: Dclk
 Path Type: min

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_R/data_out_reg[9]/CKN (DFFNSRHX1M)	0.00	652.27 f
P_MSDAP/SIPO_R/data_out_reg[9]/Q (DFFNSRHX1M)	0.94	653.21 r
P_MSDAP/SIPO_R/U44/Y (OAI21X1M)	0.19 *	653.41 f
P_MSDAP/SIPO_R/U43/Y (OAI21X1M)	0.09 *	653.50 r
P_MSDAP/SIPO_R/data_out_reg[9]/D (DFFNSRHX1M)	0.00 *	653.50 r
data arrival time		653.50
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_R/data_out_reg[9]/CKN (DFFNSRHX1M)	0.00	652.27 f
library hold time	0.17	652.44
data required time		652.44
data required time		652.44
data arrival time		-653.50
slack (MET)		1.05

Startpoint: P_MSDAP/SIPO_R/bt_reg[1]
 (falling edge-triggered flip-flop clocked by Dclk)
 Endpoint: P_MSDAP/SIPO_R/data_out_reg[11]
 (falling edge-triggered flip-flop clocked by Dclk)
 Path Group: Dclk
 Path Type: min

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_R/bt_reg[1]/CKN (DFFNSRHX1M)	0.00	652.27 f
P_MSDAP/SIPO_R/bt_reg[1]/Q (DFFNSRHX1M)	0.87	653.14 r
P_MSDAP/SIPO_R/U4/Y (NAND2X2M)	0.17 *	653.32 f
P_MSDAP/SIPO_R/U45/Y (OAI21X1M)	0.19 *	653.50 r
P_MSDAP/SIPO_R/data_out_reg[11]/D (DFFNSRHX1M)	0.00 *	653.50 r
data arrival time		653.50
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_R/data_out_reg[11]/CKN (DFFNSRHX1M)	0.00	652.27 f
library hold time	0.17	652.44
data required time		652.44
data required time		652.44
data arrival time		-653.50
slack (MET)		1.06

Startpoint: P_MSDAP/SIPO_R/bt_reg[3]
 (falling edge-triggered flip-flop clocked by Dclk)
 Endpoint: P_MSDAP/SIPO_R/data_out_reg[12]
 (falling edge-triggered flip-flop clocked by Dclk)
 Path Group: Dclk
 Path Type: min

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_R/bt_reg[3]/CKN (DFFNSRHX1M)	0.00	652.27 f
P_MSDAP/SIPO_R/bt_reg[3]/Q (DFFNSRHX1M)	0.71	652.99 f
P_MSDAP/SIPO_R/U58/Y (NAND3X2M)	0.28 *	653.27 r
P_MSDAP/SIPO_R/U24/Y (OAI21X1M)	0.14 *	653.40 f
P_MSDAP/SIPO_R/U23/Y (OAI21X1M)	0.10 *	653.50 r
P_MSDAP/SIPO_R/data_out_reg[12]/D (DFFNSRHX1M)	0.00 *	653.50 r
data arrival time		653.50
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_R/data_out_reg[12]/CKN (DFFNSRHX1M)	0.00	652.27 f
library hold time	0.17	652.44
data required time		652.44
data required time		652.44
data arrival time		-653.50
slack (MET)		1.06

Startpoint: P_MSDAP/SIPO_L/bt_reg[3]
 (falling edge-triggered flip-flop clocked by Dclk)
 Endpoint: P_MSDAP/SIPO_L/data_out_reg[9]
 (falling edge-triggered flip-flop clocked by Dclk)
 Path Group: Dclk
 Path Type: min

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_L/bt_reg[3]/CKN (DFFNSRHX1M)	0.00	652.27 f
P_MSDAP/SIPO_L/bt_reg[3]/Q (DFFNSRHX1M)	0.72	652.99 f

P_MSDAP/SIPO_L/U59/Y (NAND3X2M)	0.28 *	653.27 r
P_MSDAP/SIPO_L/U44/Y (OAI21X1M)	0.14 *	653.41 f
P_MSDAP/SIPO_L/U43/Y (OAI21X1M)	0.09 *	653.50 r
P_MSDAP/SIPO_L/data_out_reg[9]/D (DFFNSRHX1M)	0.00 *	653.50 r
data arrival time		653.50
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_L/data_out_reg[9]/CKN (DFFNSRHX1M)	0.00	652.27 f
library hold time	0.17	652.44
data required time		652.44
data required time		652.44
data arrival time		-653.50
slack (MET)		1.06

Startpoint: P_MSDAP/SIPO_L/bt_reg[3]
 (falling edge-triggered flip-flop clocked by Dclk)
 Endpoint: P_MSDAP/SIPO_L/data_out_reg[11]
 (falling edge-triggered flip-flop clocked by Dclk)
 Path Group: Dclk
 Path Type: min

Point	Incr	Path
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_L/bt_reg[3]/CKN (DFFNSRHX1M)	0.00	652.27 f
P_MSDAP/SIPO_L/bt_reg[3]/Q (DFFNSRHX1M)	0.72	652.99 f
P_MSDAP/SIPO_L/U59/Y (NAND3X2M)	0.28 *	653.27 r
P_MSDAP/SIPO_L/U46/Y (OAI21X1M)	0.15 *	653.42 f
P_MSDAP/SIPO_L/U45/Y (OAI21X1M)	0.09 *	653.51 r
P_MSDAP/SIPO_L/data_out_reg[11]/D (DFFNSRHX1M)	0.00 *	653.51 r
data arrival time		653.51
clock Dclk (fall edge)	651.04	651.04
clock network delay (propagated)	1.23	652.27
P_MSDAP/SIPO_L/data_out_reg[11]/CKN (DFFNSRHX1M)	0.00	652.27 f
library hold time	0.17	652.44
data required time		652.44
data required time		652.44
data arrival time		-653.51
slack (MET)		1.06

Startpoint: Start (input port clocked by Sclk)
 Endpoint: P_MSDAP/CU/state_reg[2]
 (rising edge-triggered flip-flop clocked by Sclk)
 Path Group: Sclk
 Path Type: min

Point	Incr	Path
clock Sclk (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
input external delay	1.00	1.00 f
Start (in)	0.00	1.00 f
Start_PB/PAD (PB2)	0.09 *	1.09 f
Start_PB/C (PB2)	0.83	1.92 f
P_MSDAP/Start (top_level)	0.00	1.92 f
P_MSDAP/CU/IN4 (controller)	0.00	1.92 f
P_MSDAP/CU/U243/Y (NOR2X2M)	0.17 *	2.09 r
P_MSDAP/CU/U385/Y (AOI22X1M)	0.15 *	2.24 f
P_MSDAP/CU/U386/Y (OAI21X1M)	0.09 *	2.33 r

P_MSDAP/CU/U219/Y (OAI2BB2X1M)	0.21 *	2.54 r
P_MSDAP/CU/state_reg[2]/D (DFFSRHQX2M)	0.00 *	2.54 r
data arrival time		2.54
 clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.08	2.08
P_MSDAP/CU/state_reg[2]/CK (DFFSRHQX2M)	0.00	2.08 r
library hold time	-0.08	2.00
data required time		2.00

data required time		2.00
data arrival time		-2.54

slack (MET)		0.54

Startpoint: Start (input port clocked by Sclk)
 Endpoint: P_MSDAP/CU/state_reg[1]
 (rising edge-triggered flip-flop clocked by Sclk)
 Path Group: Sclk
 Path Type: min

Point	Incr	Path

clock Sclk (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
input external delay	1.00	1.00 f
Start (in)	0.00	1.00 f
Start_PB/PAD (PB2)	0.09 *	1.09 f
Start_PB/C (PB2)	0.83	1.92 f
P_MSDAP/Start (top_level)	0.00	1.92 f
P_MSDAP/CU/IN4 (controller)	0.00	1.92 f
P_MSDAP/CU/U246/Y (NOR2X2M)	0.17 *	2.09 r
P_MSDAP/CU/U379/Y (AOI22X1M)	0.13 *	2.22 f
P_MSDAP/CU/U380/Y (OAI21X1M)	0.11 *	2.33 r
P_MSDAP/CU/U220/Y (OAI2BB2X1M)	0.21 *	2.55 r
P_MSDAP/CU/state_reg[1]/D (DFFSRHQX2M)	0.00 *	2.55 r
data arrival time		2.55

clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.09	2.09
P_MSDAP/CU/state_reg[1]/CK (DFFSRHQX2M)	0.00	2.09 r
library hold time	-0.08	2.00
data required time		2.00

data required time		2.00
data arrival time		-2.55

slack (MET)		0.55

Startpoint: Start (input port clocked by Sclk)
 Endpoint: P_MSDAP/CU/state_reg[0]
 (rising edge-triggered flip-flop clocked by Sclk)
 Path Group: Sclk
 Path Type: min

Point	Incr	Path

clock Sclk (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
input external delay	1.00	1.00 f
Start (in)	0.00	1.00 f
Start_PB/PAD (PB2)	0.09 *	1.09 f
Start_PB/C (PB2)	0.83	1.92 f
P_MSDAP/Start (top_level)	0.00	1.92 f
P_MSDAP/CU/IN4 (controller)	0.00	1.92 f
P_MSDAP/CU/U244/Y (NOR2X2M)	0.17 *	2.09 r

P_MSDAP/CU/U372/Y (AOI22X1M)	0.13 *	2.22 f
P_MSDAP/CU/U373/Y (OAI2BB1X1M)	0.11 *	2.33 r
P_MSDAP/CU/U222/Y (AO2B2X2M)	0.23 *	2.57 r
P_MSDAP/CU/state_reg[0]/D (DFFSRHQX2M)	0.00 *	2.57 r
data arrival time		2.57
clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.08	2.08
P_MSDAP/CU/state_reg[0]/CK (DFFSRHQX2M)	0.00	2.08 r
library hold time	-0.08	2.00
data required time		2.00
data required time		2.00
data arrival time		-2.57
slack (MET)	0.56	

Startpoint: P_MSDAP/ALU_R/rj_data_reg[7]
 (rising edge-triggered flip-flop clocked by Sclk)

Endpoint: P_MSDAP/ALU_R/rj_data_reg[7]
 (rising edge-triggered flip-flop clocked by Sclk)

Path Group: Sclk

Path Type: min

Point	Incr	Path
clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.09	2.09
P_MSDAP/ALU_R/rj_data_reg[7]/CK (DFFRX2M)	0.00	2.09 r
P_MSDAP/ALU_R/rj_data_reg[7]/QN (DFFRX2M)	0.46	2.54 r
P_MSDAP/ALU_R/U101/Y (OAI22X1M)	0.13 *	2.67 f
P_MSDAP/ALU_R/rj_data_reg[7]/D (DFFRX2M)	0.00 *	2.67 f
data arrival time		2.67
clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.09	2.09
P_MSDAP/ALU_R/rj_data_reg[7]/CK (DFFRX2M)	0.00	2.09 r
library hold time	0.01	2.10
data required time		2.10
data required time		2.10
data arrival time		-2.67
slack (MET)	0.58	

Startpoint: P_MSDAP/ALU_R/rj_data_reg[3]
 (rising edge-triggered flip-flop clocked by Sclk)

Endpoint: P_MSDAP/ALU_R/rj_data_reg[3]
 (rising edge-triggered flip-flop clocked by Sclk)

Path Group: Sclk

Path Type: min

Point	Incr	Path
clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.09	2.09
P_MSDAP/ALU_R/rj_data_reg[3]/CK (DFFRX2M)	0.00	2.09 r
P_MSDAP/ALU_R/rj_data_reg[3]/QN (DFFRX2M)	0.46	2.54 r
P_MSDAP/ALU_R/U97/Y (OAI22X1M)	0.13 *	2.67 f
P_MSDAP/ALU_R/rj_data_reg[3]/D (DFFRX2M)	0.00 *	2.67 f
data arrival time		2.67
clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.09	2.09
P_MSDAP/ALU_R/rj_data_reg[3]/CK (DFFRX2M)	0.00	2.09 r
library hold time	0.01	2.10

data required time	2.10

data required time	2.10
data arrival time	-2.67

slack (MET)	0.58

Startpoint: P_MSDAP/ALU_L/rj_data_reg[6]
 (rising edge-triggered flip-flop clocked by Sclk)
 Endpoint: P_MSDAP/ALU_L/rj_data_reg[6]
 (rising edge-triggered flip-flop clocked by Sclk)
 Path Group: Sclk
 Path Type: min

Point	Incr	Path
clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.09	2.09
P_MSDAP/ALU_L/rj_data_reg[6]/CK (DFFRX2M)	0.00	2.09 r
P_MSDAP/ALU_L/rj_data_reg[6]/QN (DFFRX2M)	0.46	2.55 r
P_MSDAP/ALU_L/U99/Y (OAI22X1M)	0.13 *	2.68 f
P_MSDAP/ALU_L/rj_data_reg[6]/D (DFFRX2M)	0.00 *	2.68 f
data arrival time		2.68

clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.09	2.09
P_MSDAP/ALU_L/rj_data_reg[6]/CK (DFFRX2M)	0.00	2.09 r
library hold time	0.01	2.10
data required time		2.10

data required time		2.10
data arrival time		-2.68

slack (MET)		0.58

Startpoint: P_MSDAP/ALU_L/h_data_reg[3]
 (rising edge-triggered flip-flop clocked by Sclk)
 Endpoint: P_MSDAP/ALU_L/h_data_reg[3]
 (rising edge-triggered flip-flop clocked by Sclk)
 Path Group: Sclk
 Path Type: min

Point	Incr	Path
clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.10	2.10
P_MSDAP/ALU_L/h_data_reg[3]/CK (DFFRX2M)	0.00	2.10 r
P_MSDAP/ALU_L/h_data_reg[3]/QN (DFFRX2M)	0.47	2.57 r
P_MSDAP/ALU_L/U128/Y (OAI22X1M)	0.13 *	2.69 f
P_MSDAP/ALU_L/h_data_reg[3]/D (DFFRX2M)	0.00 *	2.69 f
data arrival time		2.69

clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.10	2.10
P_MSDAP/ALU_L/h_data_reg[3]/CK (DFFRX2M)	0.00	2.10 r
library hold time	0.02	2.11
data required time		2.11

data required time		2.11
data arrival time		-2.69

slack (MET)		0.58

Startpoint: P_MSDAP/ALU_R/rj_data_reg[1]
 (rising edge-triggered flip-flop clocked by Sclk)

Endpoint: P_MSDAP/ALU_R/rj_data_reg[1]
 (rising edge-triggered flip-flop clocked by Sclk)
 Path Group: Sclk
 Path Type: min

Point	Incr	Path
clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.09	2.09
P_MSDAP/ALU_R/rj_data_reg[1]/CK (DFFRX2M)	0.00	2.09 r
P_MSDAP/ALU_R/rj_data_reg[1]/QN (DFFRX2M)	0.45	2.54 r
P_MSDAP/ALU_R/U95/Y (OAI22X1M)	0.14 *	2.68 f
P_MSDAP/ALU_R/rj_data_reg[1]/D (DFFRX2M)	0.00 *	2.68 f
data arrival time		2.68
clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.09	2.09
P_MSDAP/ALU_R/rj_data_reg[1]/CK (DFFRX2M)	0.00	2.09 r
library hold time	0.01	2.09
data required time		2.09
data required time		2.09
data arrival time		-2.68
slack (MET)		0.58

Startpoint: P_MSDAP/ALU_R/rj_data_reg[2]
 (rising edge-triggered flip-flop clocked by Sclk)
 Endpoint: P_MSDAP/ALU_R/rj_data_reg[2]
 (rising edge-triggered flip-flop clocked by Sclk)
 Path Group: Sclk
 Path Type: min

Point	Incr	Path
clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.09	2.09
P_MSDAP/ALU_R/rj_data_reg[2]/CK (DFFRX2M)	0.00	2.09 r
P_MSDAP/ALU_R/rj_data_reg[2]/QN (DFFRX2M)	0.46	2.54 r
P_MSDAP/ALU_R/U96/Y (OAI22X1M)	0.13 *	2.68 f
P_MSDAP/ALU_R/rj_data_reg[2]/D (DFFRX2M)	0.00 *	2.68 f
data arrival time		2.68
clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.09	2.09
P_MSDAP/ALU_R/rj_data_reg[2]/CK (DFFRX2M)	0.00	2.09 r
library hold time	0.01	2.10
data required time		2.10
data required time		2.10
data arrival time		-2.68
slack (MET)		0.58

Startpoint: P_MSDAP/ALU_L/rj_data_reg[5]
 (rising edge-triggered flip-flop clocked by Sclk)
 Endpoint: P_MSDAP/ALU_L/rj_data_reg[5]
 (rising edge-triggered flip-flop clocked by Sclk)
 Path Group: Sclk
 Path Type: min

Point	Incr	Path
clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.09	2.09
P_MSDAP/ALU_L/rj_data_reg[5]/CK (DFFRX2M)	0.00	2.09 r

P_MSDAP/ALU_L/rj_data_reg[5]/QN (DFFRX2M)	0.46	2.55 r
P_MSDAP/ALU_L/U98/Y (OAI22X1M)	0.13 *	2.68 f
P_MSDAP/ALU_L/rj_data_reg[5]/D (DFFRX2M)	0.00 *	2.68 f
data arrival time		2.68
clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.09	2.09
P_MSDAP/ALU_L/rj_data_reg[5]/CK (DFFRX2M)	0.00	2.09 r
library hold time	0.01	2.10
data required time		2.10

data required time		2.10
data arrival time		-2.68

slack (MET)	0.58	

Startpoint: P_MSDAP/ALU_R/h_data_reg[2]
 (rising edge-triggered flip-flop clocked by Sclk)
 Endpoint: P_MSDAP/ALU_R/h_data_reg[2]
 (rising edge-triggered flip-flop clocked by Sclk)
 Path Group: Sclk
 Path Type: min

Point	Incr	Path
clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.09	2.09
P_MSDAP/ALU_R/h_data_reg[2]/CK (DFFRX2M)	0.00	2.09 r
P_MSDAP/ALU_R/h_data_reg[2]/QN (DFFRX2M)	0.46	2.55 r
P_MSDAP/ALU_R/U128/Y (OAI22X1M)	0.13 *	2.68 f
P_MSDAP/ALU_R/h_data_reg[2]/D (DFFRX2M)	0.00 *	2.68 f
data arrival time		2.68
clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.09	2.09
P_MSDAP/ALU_R/h_data_reg[2]/CK (DFFRX2M)	0.00	2.09 r
library hold time	0.01	2.10
data required time		2.10

data required time		2.10
data arrival time		-2.68

slack (MET)	0.58	

Startpoint: P_MSDAP/ALU_R/rj_data_reg[6]
 (rising edge-triggered flip-flop clocked by Sclk)
 Endpoint: P_MSDAP/ALU_R/rj_data_reg[6]
 (rising edge-triggered flip-flop clocked by Sclk)
 Path Group: Sclk
 Path Type: min

Point	Incr	Path
clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.09	2.09
P_MSDAP/ALU_R/rj_data_reg[6]/CK (DFFRX2M)	0.00	2.09 r
P_MSDAP/ALU_R/rj_data_reg[6]/QN (DFFRX2M)	0.46	2.55 r
P_MSDAP/ALU_R/U100/Y (OAI22X1M)	0.13 *	2.68 f
P_MSDAP/ALU_R/rj_data_reg[6]/D (DFFRX2M)	0.00 *	2.68 f
data arrival time		2.68
clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.09	2.09
P_MSDAP/ALU_R/rj_data_reg[6]/CK (DFFRX2M)	0.00	2.09 r
library hold time	0.01	2.10
data required time		2.10

data required time	2.10
data arrival time	-2.68
slack (MET)	0.58

Startpoint: P_MSDAP/ALU_R/rj_data_reg[5]
 (rising edge-triggered flip-flop clocked by Sclk)
 Endpoint: P_MSDAP/ALU_R/rj_data_reg[5]
 (rising edge-triggered flip-flop clocked by Sclk)
 Path Group: Sclk
 Path Type: min

Point	Incr	Path
clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.09	2.09
P_MSDAP/ALU_R/rj_data_reg[5]/CK (DFFRX2M)	0.00	2.09 r
P_MSDAP/ALU_R/rj_data_reg[5]/QN (DFFRX2M)	0.46	2.55 r
P_MSDAP/ALU_R/U99/Y (OAI22X1M)	0.13 *	2.68 f
P_MSDAP/ALU_R/rj_data_reg[5]/D (DFFRX2M)	0.00 *	2.68 f
data arrival time		2.68
clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.09	2.09
P_MSDAP/ALU_R/rj_data_reg[5]/CK (DFFRX2M)	0.00	2.09 r
library hold time	0.01	2.10
data required time		2.10
data required time		2.10
data arrival time		-2.68
slack (MET)		0.58

Startpoint: P_MSDAP/ALU_L/h_data_reg[1]
 (rising edge-triggered flip-flop clocked by Sclk)
 Endpoint: P_MSDAP/ALU_L/h_data_reg[1]
 (rising edge-triggered flip-flop clocked by Sclk)
 Path Group: Sclk
 Path Type: min

Point	Incr	Path
clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.10	2.10
P_MSDAP/ALU_L/h_data_reg[1]/CK (DFFRX2M)	0.00	2.10 r
P_MSDAP/ALU_L/h_data_reg[1]/QN (DFFRX2M)	0.47	2.57 r
P_MSDAP/ALU_L/U126/Y (OAI22X1M)	0.13 *	2.70 f
P_MSDAP/ALU_L/h_data_reg[1]/D (DFFRX2M)	0.00 *	2.70 f
data arrival time		2.70
clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.10	2.10
P_MSDAP/ALU_L/h_data_reg[1]/CK (DFFRX2M)	0.00	2.10 r
library hold time	0.02	2.11
data required time		2.11
data required time		2.11
data arrival time		-2.70
slack (MET)		0.58

Startpoint: P_MSDAP/ALU_R/rj_data_reg[0]
 (rising edge-triggered flip-flop clocked by Sclk)
 Endpoint: P_MSDAP/ALU_R/rj_data_reg[0]

(rising edge-triggered flip-flop clocked by Sclk)
Path Group: Sclk
Path Type: min

Point	Incr	Path
clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.09	2.09
P_MSDAP/ALU_R/rj_data_reg[0]/CK (DFFRX2M)	0.00	2.09 r
P_MSDAP/ALU_R/rj_data_reg[0]/QN (DFFRX2M)	0.46	2.55 r
P_MSDAP/ALU_R/U94/Y (OAI22X1M)	0.13 *	2.68 f
P_MSDAP/ALU_R/rj_data_reg[0]/D (DFFRX2M)	0.00 *	2.68 f
data arrival time		2.68
clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.09	2.09
P_MSDAP/ALU_R/rj_data_reg[0]/CK (DFFRX2M)	0.00	2.09 r
library hold time	0.01	2.10
data required time		2.10
data required time		2.10
data arrival time		-2.68
slack (MET)		0.58

Startpoint: P_MSDAP/ALU_L/rj_data_reg[7]
(rising edge-triggered flip-flop clocked by Sclk)
Endpoint: P_MSDAP/ALU_L/rj_data_reg[7]
(rising edge-triggered flip-flop clocked by Sclk)
Path Group: Sclk
Path Type: min

Point	Incr	Path
clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.09	2.09
P_MSDAP/ALU_L/rj_data_reg[7]/CK (DFFRX2M)	0.00	2.09 r
P_MSDAP/ALU_L/rj_data_reg[7]/QN (DFFRX2M)	0.46	2.55 r
P_MSDAP/ALU_L/U100/Y (OAI22X1M)	0.13 *	2.68 f
P_MSDAP/ALU_L/rj_data_reg[7]/D (DFFRX2M)	0.00 *	2.68 f
data arrival time		2.68
clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.09	2.09
P_MSDAP/ALU_L/rj_data_reg[7]/CK (DFFRX2M)	0.00	2.09 r
library hold time	0.01	2.10
data required time		2.10
data required time		2.10
data arrival time		-2.68
slack (MET)		0.58

Startpoint: P_MSDAP/ALU_L/rj_data_reg[4]
(rising edge-triggered flip-flop clocked by Sclk)
Endpoint: P_MSDAP/ALU_L/rj_data_reg[4]
(rising edge-triggered flip-flop clocked by Sclk)
Path Group: Sclk
Path Type: min

Point	Incr	Path
clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.09	2.09
P_MSDAP/ALU_L/rj_data_reg[4]/CK (DFFRX2M)	0.00	2.09 r
P_MSDAP/ALU_L/rj_data_reg[4]/QN (DFFRX2M)	0.46	2.55 r

P_MSDAP/ALU_L/U97/Y (OAI22X1M)	0.13 *	2.68 f
P_MSDAP/ALU_L/rj_data_reg[4]/D (DFFRX2M)	0.00 *	2.68 f
data arrival time		2.68
 clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.09	2.09
P_MSDAP/ALU_L/rj_data_reg[4]/CK (DFFRX2M)	0.00	2.09 r
library hold time	0.01	2.10
data required time		2.10

data required time		2.10
data arrival time		-2.68

slack (MET)		0.58

Startpoint: P_MSDAP/ALU_L/rj_data_reg[2]
 (rising edge-triggered flip-flop clocked by Sclk)
 Endpoint: P_MSDAP/ALU_L/rj_data_reg[2]
 (rising edge-triggered flip-flop clocked by Sclk)
 Path Group: Sclk
 Path Type: min

Point	Incr	Path
 clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.09	2.09
P_MSDAP/ALU_L/rj_data_reg[2]/CK (DFFRX2M)	0.00	2.09 r
P_MSDAP/ALU_L/rj_data_reg[2]/QN (DFFRX2M)	0.46	2.55 r
P_MSDAP/ALU_L/U95/Y (OAI22X1M)	0.14 *	2.68 f
P_MSDAP/ALU_L/rj_data_reg[2]/D (DFFRX2M)	0.00 *	2.68 f
data arrival time		2.68
 clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.09	2.09
P_MSDAP/ALU_L/rj_data_reg[2]/CK (DFFRX2M)	0.00	2.09 r
library hold time	0.01	2.10
data required time		2.10

data required time		2.10
data arrival time		-2.68

slack (MET)		0.58

Startpoint: P_MSDAP/ALU_L/rj_data_reg[0]
 (rising edge-triggered flip-flop clocked by Sclk)
 Endpoint: P_MSDAP/ALU_L/rj_data_reg[0]
 (rising edge-triggered flip-flop clocked by Sclk)
 Path Group: Sclk
 Path Type: min

Point	Incr	Path
 clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.09	2.09
P_MSDAP/ALU_L/rj_data_reg[0]/CK (DFFRX2M)	0.00	2.09 r
P_MSDAP/ALU_L/rj_data_reg[0]/QN (DFFRX2M)	0.46	2.55 r
P_MSDAP/ALU_L/U93/Y (OAI22X1M)	0.14 *	2.69 f
P_MSDAP/ALU_L/rj_data_reg[0]/D (DFFRX2M)	0.00 *	2.69 f
data arrival time		2.69
 clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.09	2.09
P_MSDAP/ALU_L/rj_data_reg[0]/CK (DFFRX2M)	0.00	2.09 r
library hold time	0.01	2.10
data required time		2.10

data required time		2.10
data arrival time		-2.69

slack (MET)		0.59
 Startpoint: P_MSDAP/ALU_L/rj_data_reg[3] (rising edge-triggered flip-flop clocked by Sclk)		
Endpoint: P_MSDAP/ALU_L/rj_data_reg[3] (rising edge-triggered flip-flop clocked by Sclk)		
Path Group: Sclk		
Path Type: min		
 Point	Incr	Path

clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.09	2.09
P_MSDAP/ALU_L/rj_data_reg[3]/CK (DFFRX2M)	0.00	2.09 r
P_MSDAP/ALU_L/rj_data_reg[3]/QN (DFFRX2M)	0.46	2.55 r
P_MSDAP/ALU_L/U96/Y (OAI22X1M)	0.14 *	2.69 f
P_MSDAP/ALU_L/rj_data_reg[3]/D (DFFRX2M)	0.00 *	2.69 f
data arrival time		2.69
 clock Sclk (rise edge)	0.00	0.00
clock network delay (propagated)	2.09	2.09
P_MSDAP/ALU_L/rj_data_reg[3]/CK (DFFRX2M)	0.00	2.09 r
library hold time	0.01	2.10
data required time		2.10

data required time		2.10
data arrival time		-2.69

slack (MET)		0.59