TOP SHEET

Revision 1

Mipi PCB guidelines on Page 203/347 of UG 583

Voltages for SOM240-2
HPB, HPC, and HDB are tied to VADJ, which goes from 1.2V to 1.8V
(Note if using FRAMOS connector, use 1.8V)

HPC is 3.3V, and used for some I/O

For High Speed PCB Guidelines
Refer to page 315/347 of ug583
TI:Dr Jog outs recommended for length matching
GTH DP0, and DP1 is for SLVS-EC RX, TX is available on HPC connector

Sheet: Displayport
File: DisplayPort.sch

Sheet: USB-3_0
File: USB-3_0.sch

Sheet: Micro_SD
File: Micro_SD.sch

Sheet: UART_JTAG
File: UART_JTAG.sch

Sheet: SATA
File: SATA.sch

Sheet: PL Power
File: PL_Power.sch

Sheet: PS Power
File: PS_Power.sch

Sheet: System Power Kria
File: Power_Kria.sch

Sheet: Buttons_Shutdown_MODE
File: Buttons_Shutdown_MODE.sch

Sheet: SOM240_1
File: SOM240_1.sch

C2M is RX (GTR 0 and 1 for Displayport)

GTR Refclk 2 not used

Sheet: MIPI_Conn
File: MIPI_Conn.sch

To ensure no conflicts with SOM I2C
ADDR_use other MIO for I2C

Sheet: Kria_Reset
File: Kria_Reset.sch

Sheet: Baro_IMU
File: Baro_IMU.sch

Sheet: FMC_PWR
File: FMC_PWR.sch

Sheet: WD_EEPROM_PWR_LED
File: WD_EEPROM_PWR_LED.sch

Sheet: Clocks_All
File: PS_Clocks.sch

Sheet: SOM240_2
File: SOM240_2.sch

Sheet: FMC_Carrier_Conn
File: FMC_Carrier_Conn.sch

Sheet: FRAMOS_PixelMate(TM)_Connector_-_SLVS-EC
File: SLVS-EC_FRAMOS.sch

FMC Mounting Holes

H13 Mounting Hole
H14 Mounting Hole

FSM/FSA Mounting Holes

H1 Mounting Hole
H3 Mounting Hole
H2 Mounting Hole
H4 Mounting Hole

Mounting Holes

H5 Mounting Hole
H7 Mounting Hole
H6 Mounting Hole
H8 Mounting Hole

Kria JSOM mounting Hole

H9 JSOM-0515-01
H11 JSOM-0515-01
H10 JSOM-0515-01
H12 JSOM-0515-01

Test Points

TP2 TestPoint
TP3 TestPoint
TP5 TestPoint
TP7 TestPoint
TP8 TestPoint
TP9 TestPoint
TP10 TestPoint
TP1 TestPoint
TP4 TestPoint
TP6 TestPoint

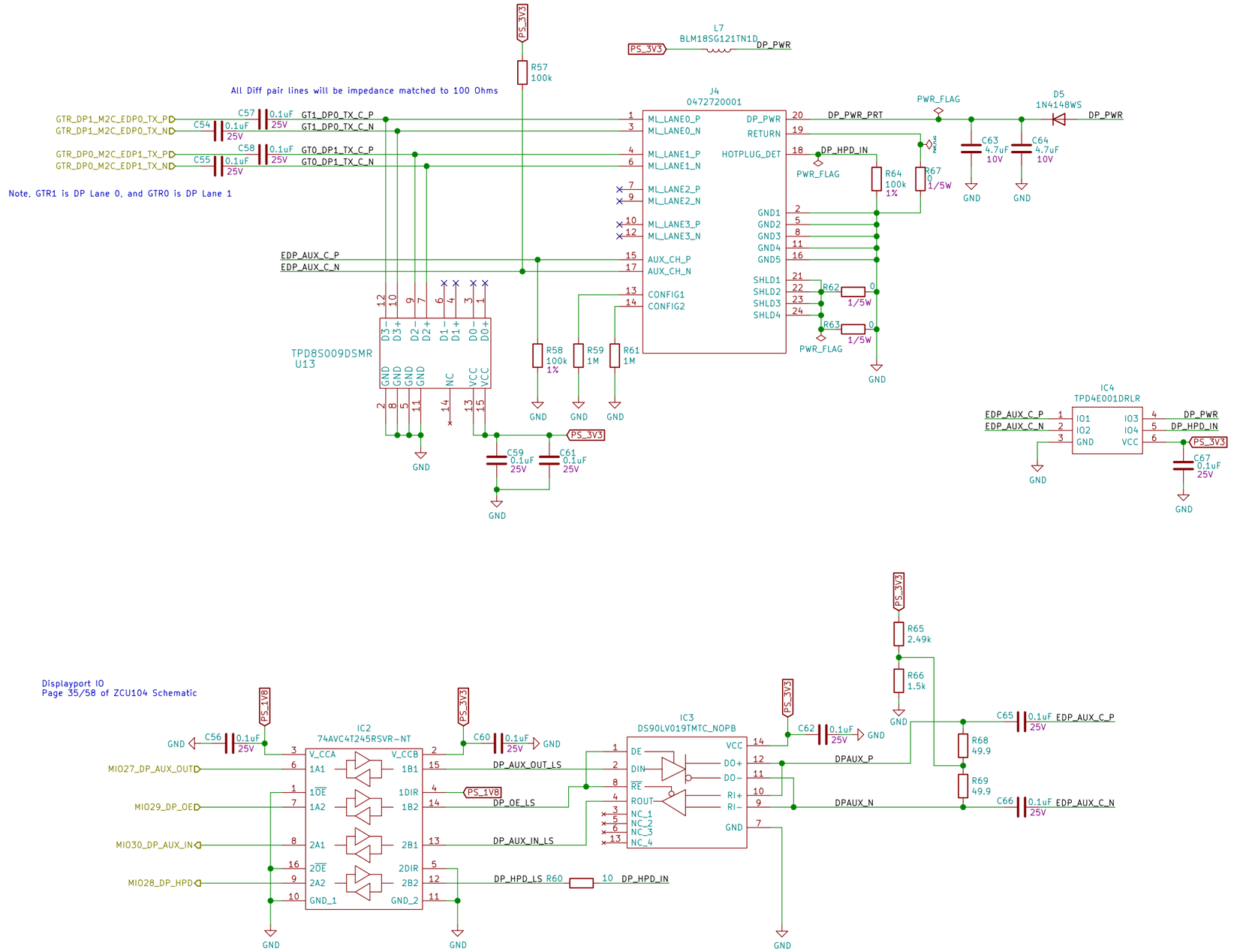
SYM4 SYM1 SYM2 SYM3

Author: Chance Reimer
SCH: APT-KRIA-FMC
ApotheoTech LLC
Sheet: /
File: APT-KRIA-FMC.sch

Title: Top Sheet

Size: A2 | Date: 2022-01-04 | **Rev: 1.00**
KiCad E.D.A. kicad (5.1.10)-1 | Id: 1/20

DisplayPort GTR



Author: Chance Reimer
SCH: APT−KRIA−FMC
ApotheoTech LLC

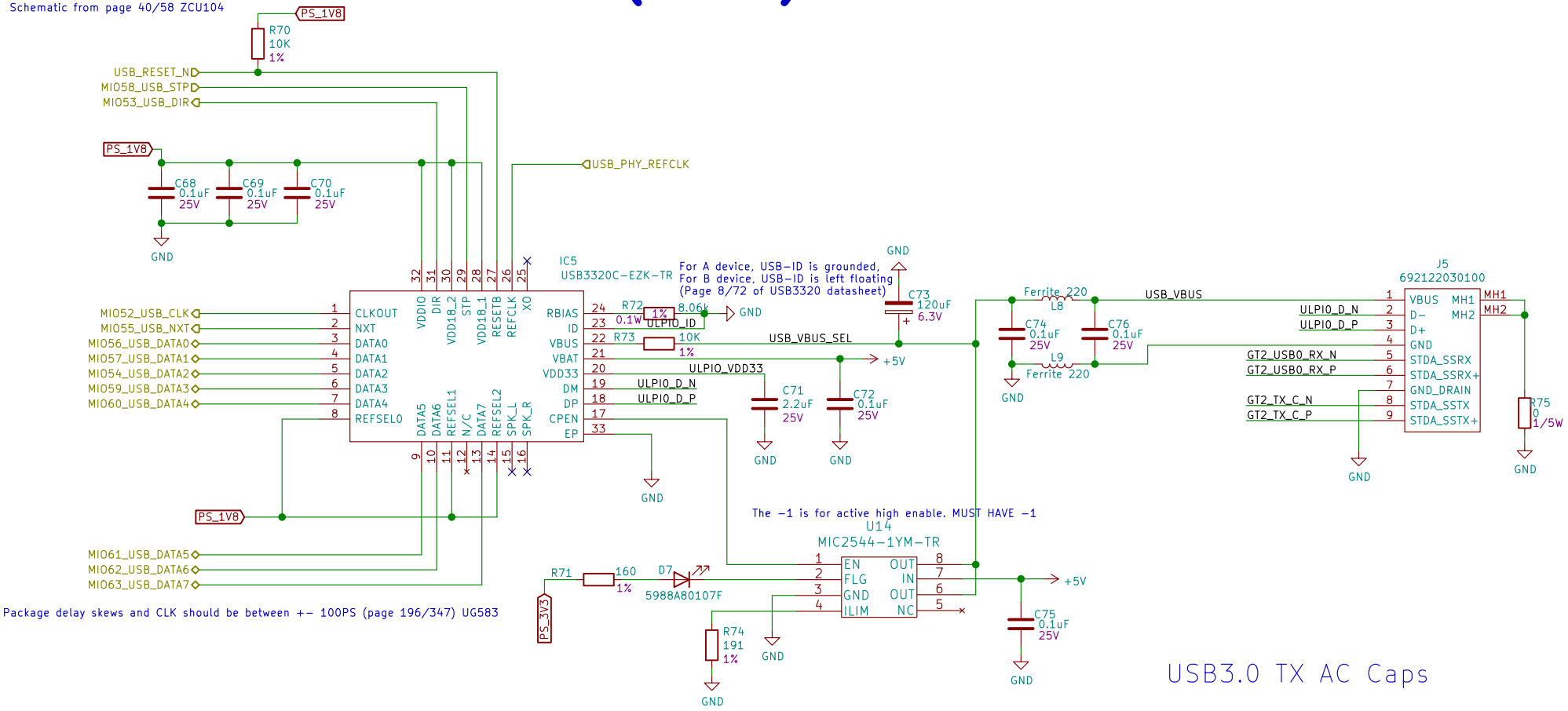
Sheet: /Displayport/
File: DisplayPort.sch

Title: Mini DisplayPort Layout

Size: A3	Date: 2022−01−04	**Rev: 1.00**
KiCad E.D.A. kicad (5.1.10)−1		Id: 2/20

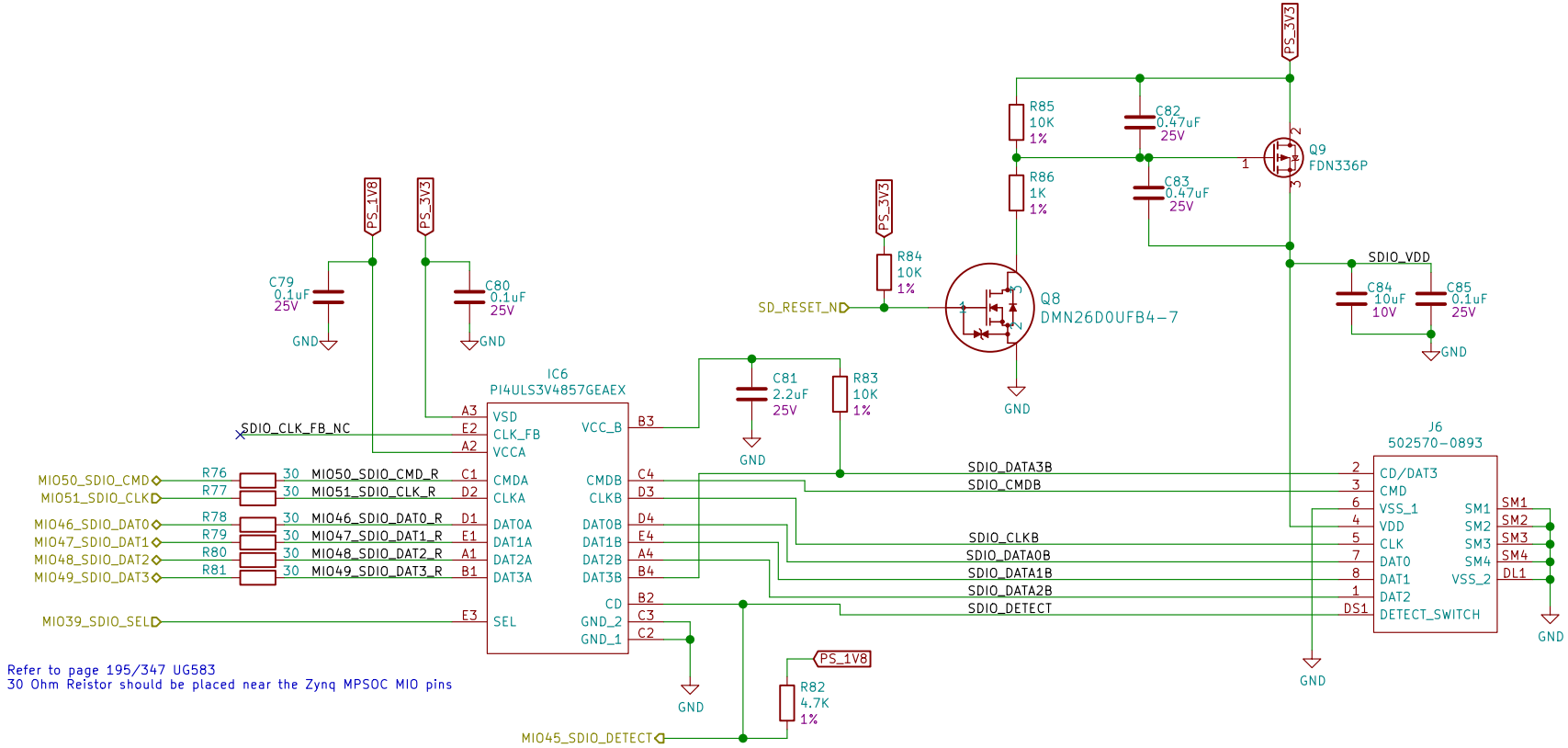
USB 3.0 and USB 2.0 (HOST)

Schematic from page 40/58 ZCU104



Author: Chance Reimer		
SCH: APT-KRIA-FMC		
ApotheoTech LLC		
Sheet: /USB-3_0/		
File: USB-3_0.sch		
Title: USB3.0 and 2.0		
Size: A4	Date: 2022-01-04	**Rev: 1.00**
KiCad E.D.A. kicad (5.1.10)-1		Id: 3/20

SD 3.0

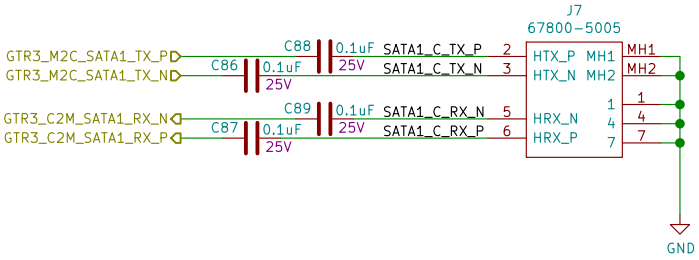


Author: Chance Reimer
SCH: APT-KRIA-FMC
ApotheoTech LLC
Sheet: /Micro_SD/
File: Micro_SD.sch

Title: SD 3.0 Card

Size: A4	Date: 2022-01-04	**Rev: 1.00**
KiCad E.D.A. kicad (5.1.10)-1		Id: 4/20

SATA



Author: Chance Reimer
SCH: APT-KRIA-FMC
ApotheoTech LLC

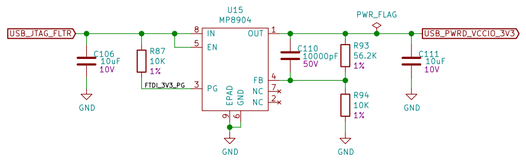
Sheet: /SATA/
File: SATA.sch

Title: SATA 1 lane

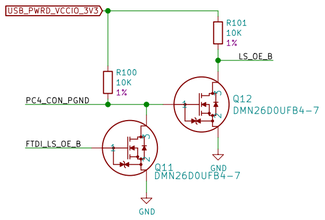
Size: A4	Date: 2022-01-04	**Rev: 1.00**
KiCad E.D.A. kicad (5.1.10)-1		Id: 5/20

JTAG, USB DBG

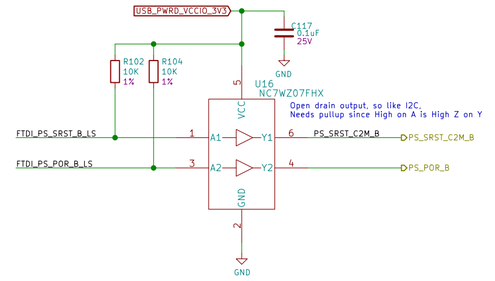
LDO for 5V VBUS to 3.3V VCCIO



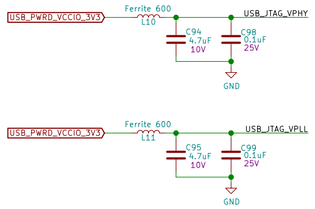
Reset Sequence for JTAG



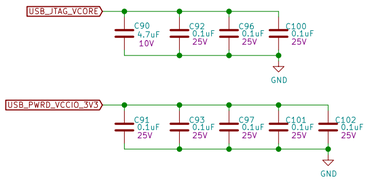
FTDI USB Reset to Board



FT4232HL PLL and PHY filtering

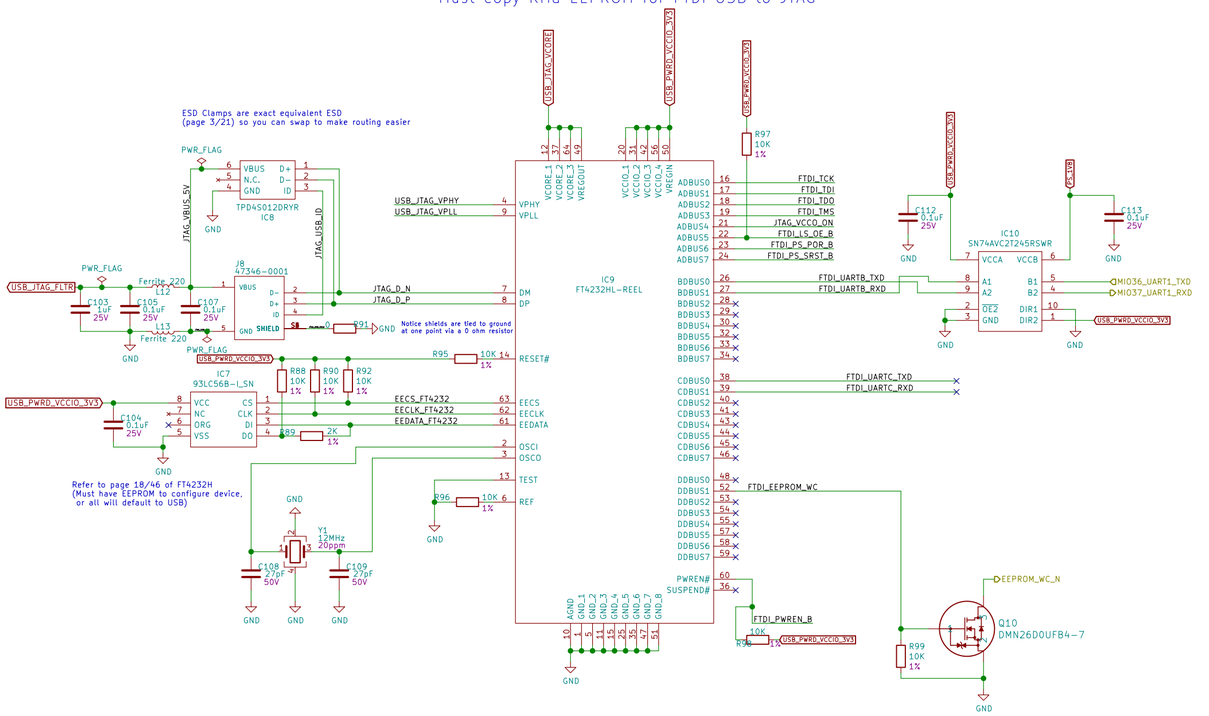


FT4232HL Decoupling Caps

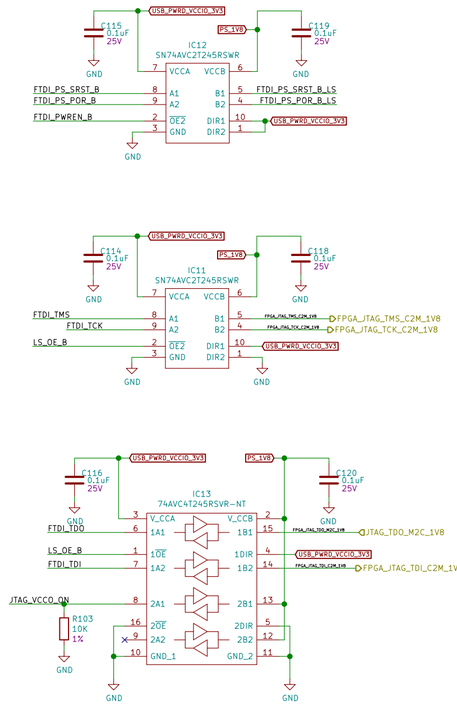


FT4232, refer to page 9 of Kria Carrier Board

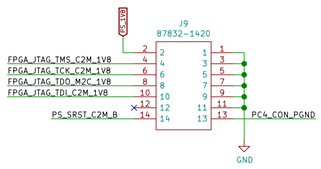
Must copy Kria EEPROM for FTDI USB to JTAG



Voltage level converters for JTAG and Status



Kria JTAG Connector



Note DS593 page 17, Note 5
Pin 13 is grounded on legacy Xilinx USB cables,
they need to be detached from 2mm connector
if FT4232H wants to communicate via JTAG

Author: Chance Reimer
SCH: APT-KRIA-FMC
ApotheoTech LLC

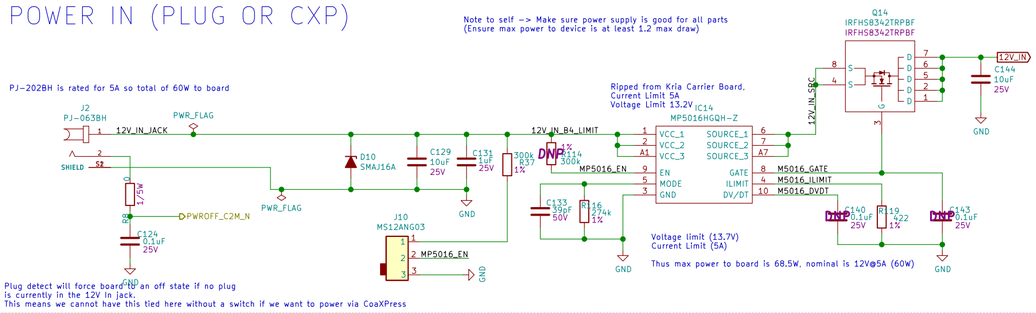
Sheet: /UART_JTAG/
File: UART_JTAG.sch

Title: JTAG for Kria and USB

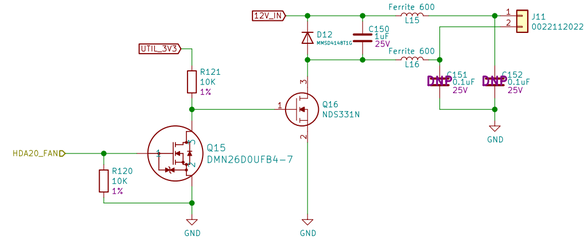
Size: A2	Date: 2022-01-04	**Rev: 1.00**
KiCad E.D.A. kicad (5.1.10)-1		Id: 6/20

Kria System Power

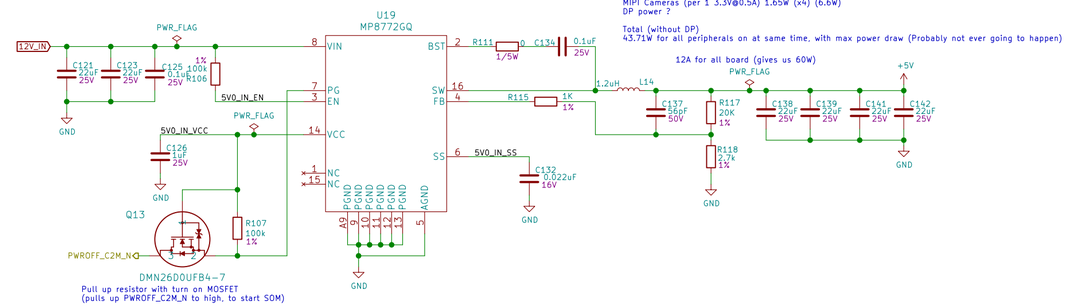
POWER IN (PLUG OR CXP)



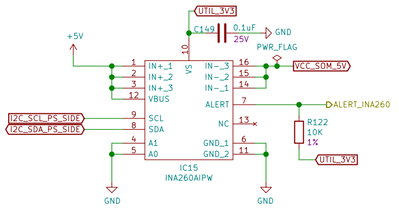
12V Fan Header Kria Heatsink



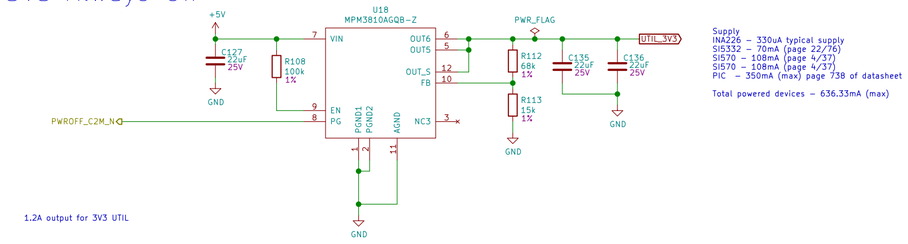
5V Always On



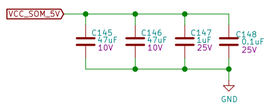
SOM_5V0 Current Monitor



3V3 Always On



SOM_5V0 Decoupling Caps



Author: Chance Reimer
SCH: APT-KRIA-FMC
ApotheoTech LLC

Sheet: /System Power Kria/
File: Power_Kria.sch

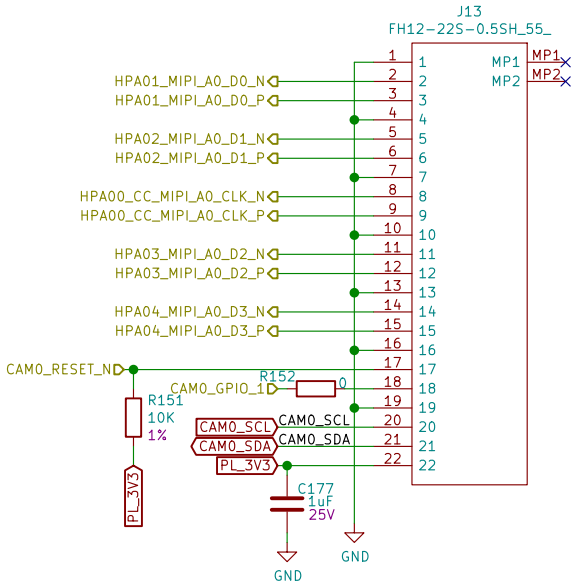
Title: System Power for Kria SOM

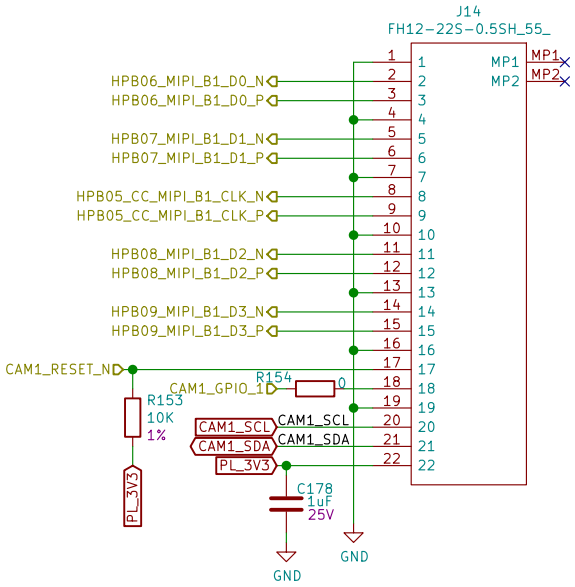
Size: A2	Date: 2022-01-04	**Rev: 1.00**
KiCad E.D.A. kicad (5.1.10)-1		Id: 7/20

ALL MIPI CONNECTORS

MIPI CSI-2 Connectors

Mipi PCB guidelines on Page 203/347 of UG 583





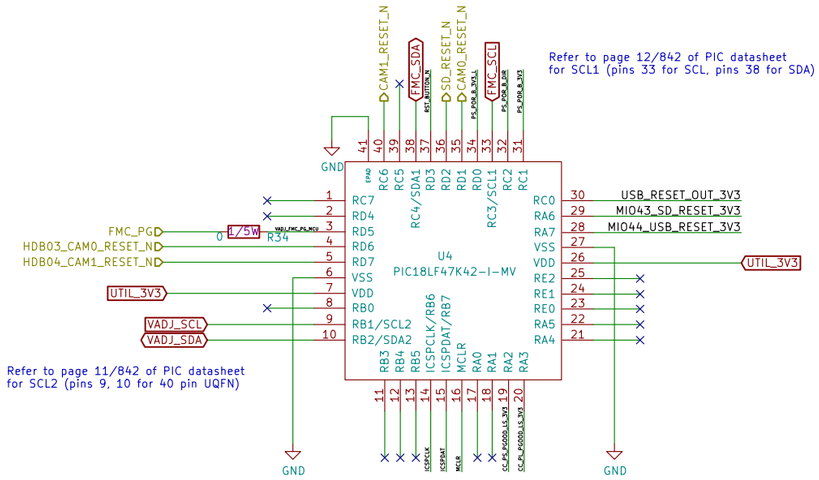
Author: Chance Reimer
SCH: APT-KRIA-FMC
ApotheoTech LLC
Sheet: /MIPI_Conn/
File: MIPI_Conn.sch

Title: MIPI DSI and CSI-2 Connectors

Size: A4	Date: 2022-01-04	**Rev: 1.00**
KiCad E.D.A. kicad (5.1.10)-1		Id: 8/20

PIC18LF47K42-I/MV Reset for Kria Carrier

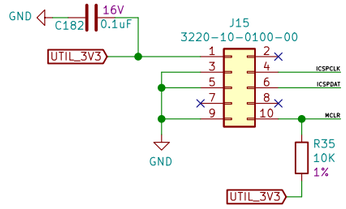
PIC18LF47K42-I/MV Reset Pinout



Refer to page 12/842 of PIC datasheet
for SCL1 (pins 33 for SCL, pins 38 for SDA)

Refer to page 11/842 of PIC datasheet
for SCL2 (pins 9, 10 for 40 pin UQFN)

CORTEX JTAG/SWD (10 pin mini)

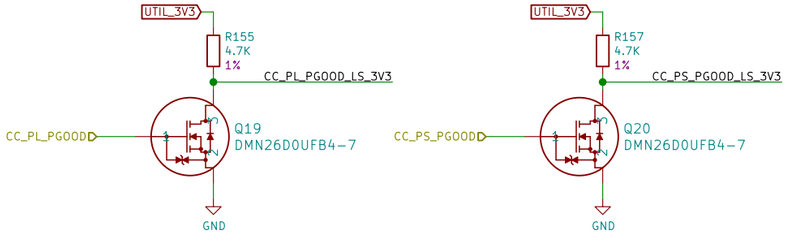


Refer to ICD4/PICkit 4 Target Adapter Board
Cortex JTAG/SWD (10 pin mini) which this is based off of

Does PGC mean ICSPCLK?
Does PGD mean ICSPDAT?

Refering to sheet 8/9 for Curiosity HPC for a reference pinout (RB7 for data, RB6 for clock)

CC_PL Voltage Changes

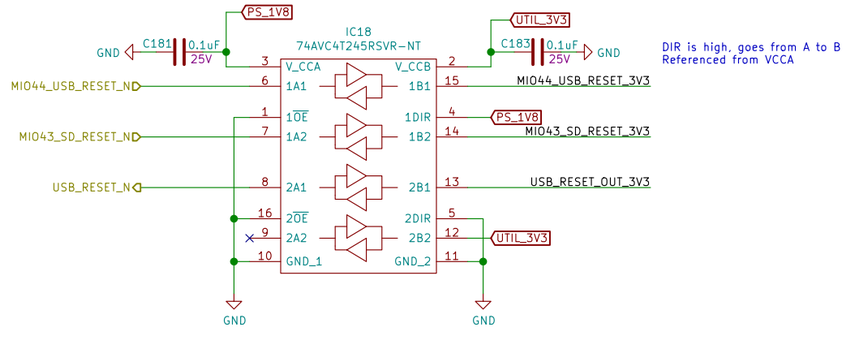


Note CC_P*_PGOOD is 5V high (when high CC_P*_PGOOD_LS is low
(inverse relationship with CC_PL_GOOD)

Voltage Level Conversion

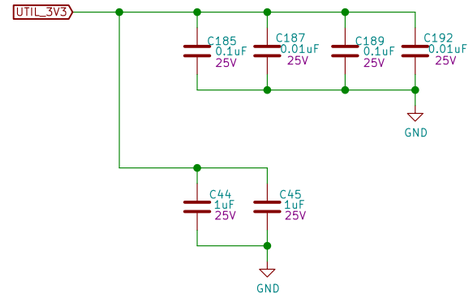
* SD reset is 3.3V nominal, no change
* Raspberry Pi Resets are 3.3V nominal, no change
* USB reset is 1.8V nominal,

Kria MIO Banks are fixed at 1.8V
Use 1.8V from PS voltage supply for reference voltage conversion

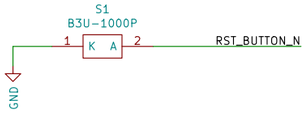


DIR is high, goes from A to B
Referenced from VCCA

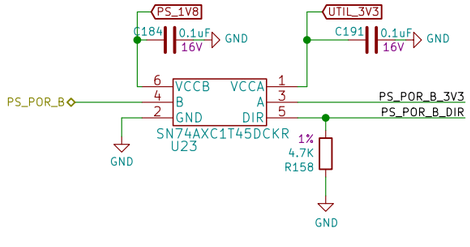
Decoupling Caps

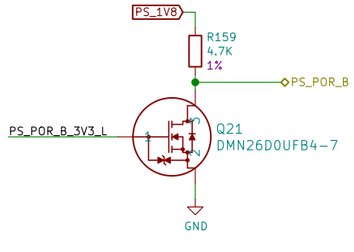


Reset Button



PS_POR_B





Pull up, DIR high is translation from A to B
Want POR_B to be controlled by carrier card,
it is held in reset until PS side is good
Refer to p age 24 of UG1089
Once CC_PS is good, check the PS_POR_B
to reset all PS reliant domains

Author: Chance Reimer
SCH: APT-KRIA-FMC
ApotheoTech LLC

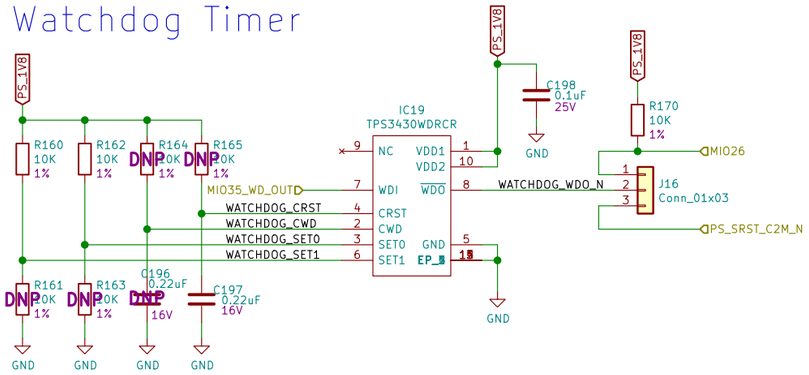
Sheet: /Kria_Reset/
File: Kria_Reset.sch

Title: IGLOO nano Reset for Kria Carrier

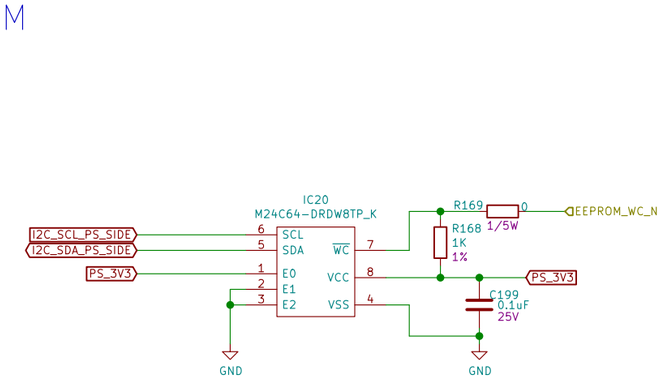
Size: A3	Date: 2022-01-04	**Rev: 1.00**
KiCad E.D.A. kicad (5.1.10)-1		Id: 9/20

WatchDog Timer, EEPROM, and Power LED Signals

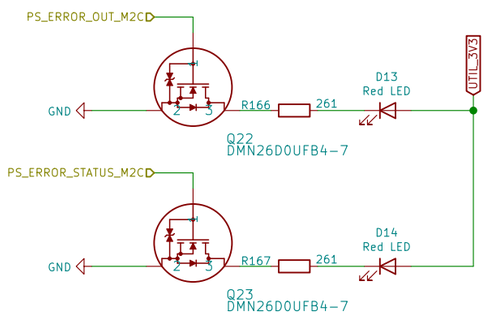
Watchdog Timer



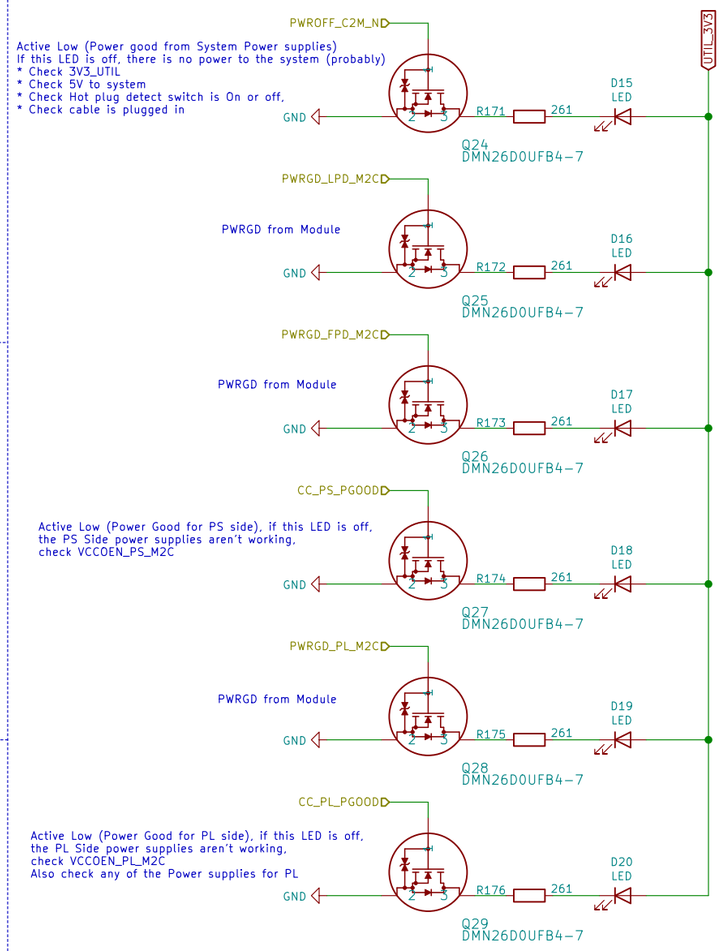
EEPROM



PS Error Status



Power Status LEDs



Author: Chance Reimer
SCH: APT-KRIA-FMC
ApotheoTech LLC

Sheet: /WD_EEPROM_PWR_LED/
File: WD_EEPROM_PWR_LED.sch

Title: WatchDog, EEPROM, Power LED

Size: A3	Date: 2022-01-04	**Rev: 1.00**
KiCad E.D.A. kicad (5.1.10)-1		Id: 10/20

Kria SOM240-1 GTR, HPIO Banks 66, MIO banks, HDIO bank 45

Remember Chance, We are the Carrier on this design

C2M -> RX for Kria module

M2C -> TX for Kria module

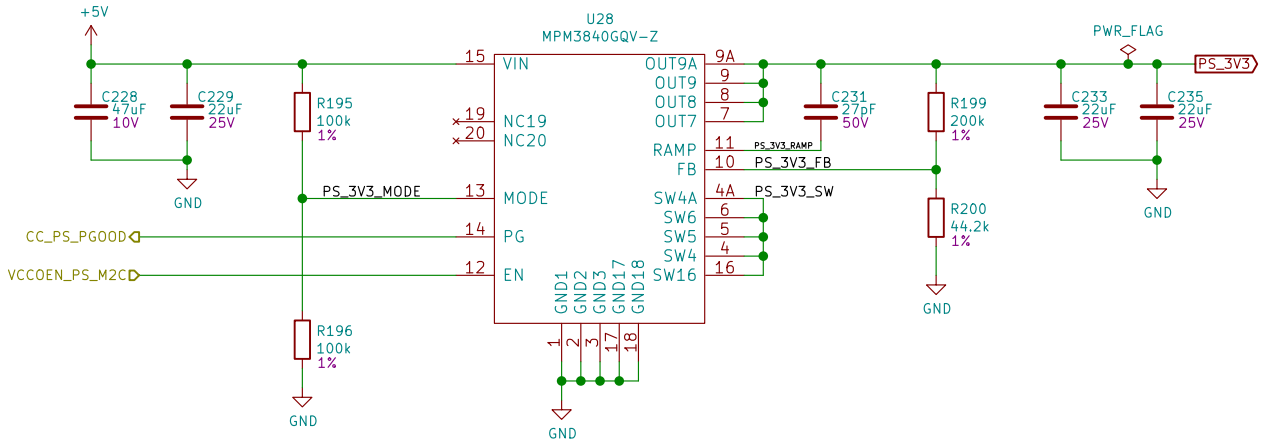
Note, to support MIPI pin standard,
VCCO must be 1.2V
(Page 143, UG571)

SOM 5V0 Decoupling

Author: Chance Reimer	
SCH: APT-KRIA-FMC	
ApotheoTech LLC	
Sheet: /SOM240_1/	
File: SOM240_1.sch	
Title: SOM240-1	
Size: A3	Date: 2022-01-04 **Rev: 1.00**
KiCad E.D.A. kicad (5.1.10)-1	Id: 11/20

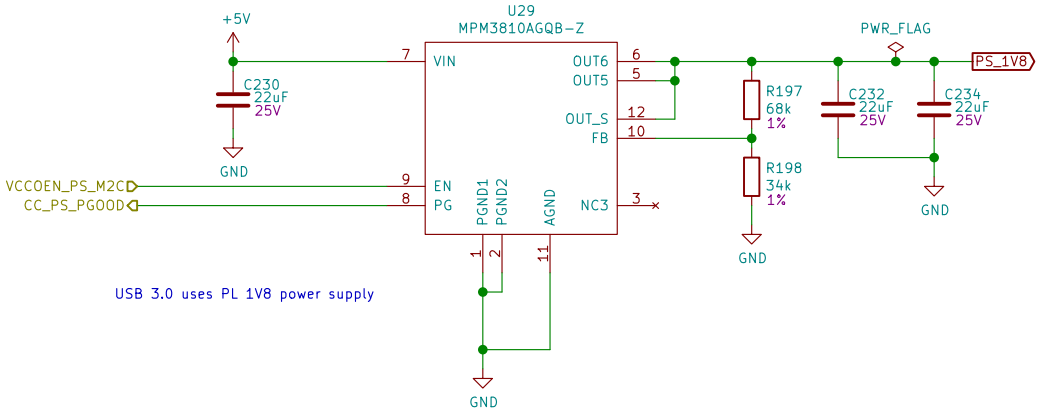
Kria PS Power

PS 3V3



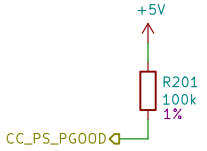
4A output for PS 3V3 for DisplayPort

PS 1V8



USB 3.0 uses PL 1V8 power supply

Pull Up Resistor for CC_PS_PGOOD



Author: Chance Reimer
SCH: APT-KRIA-FMC
ApotheoTech LLC

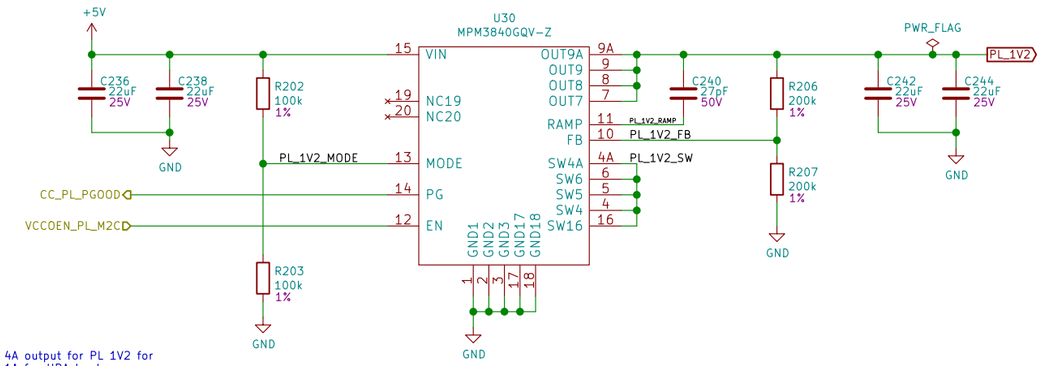
Sheet: /PS Power/
File: PS_Power.sch

Title: PS Power for Kria SOM

Size: A4	Date: 2022-01-04	**Rev: 1.00**
KiCad E.D.A. kicad (5.1.10)-1		Id: 12/20

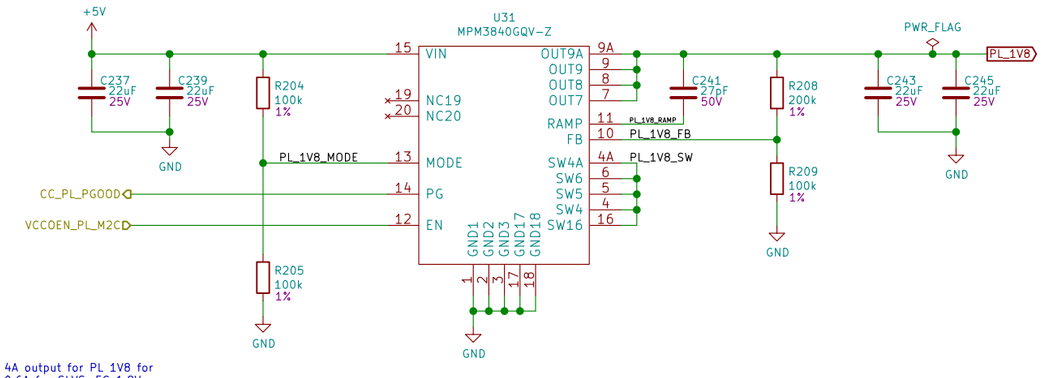
Kria PL Power

PL 1V2



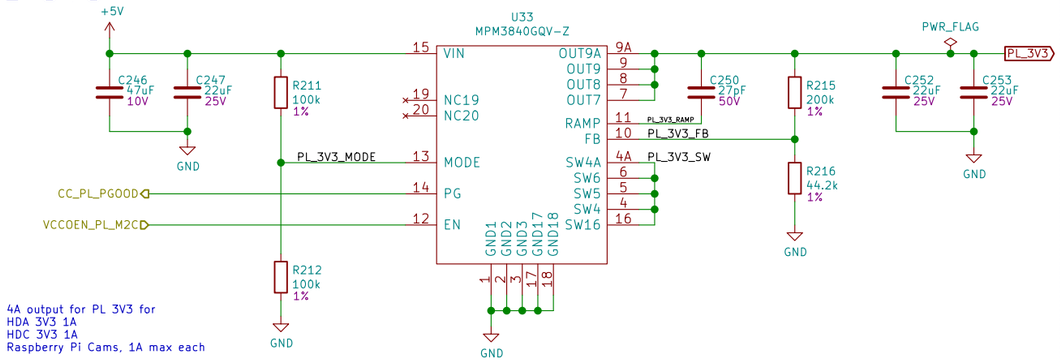
4A output for PL 1V2 for
1A for HPA bank
3A overhead for accessories

PL 1V8



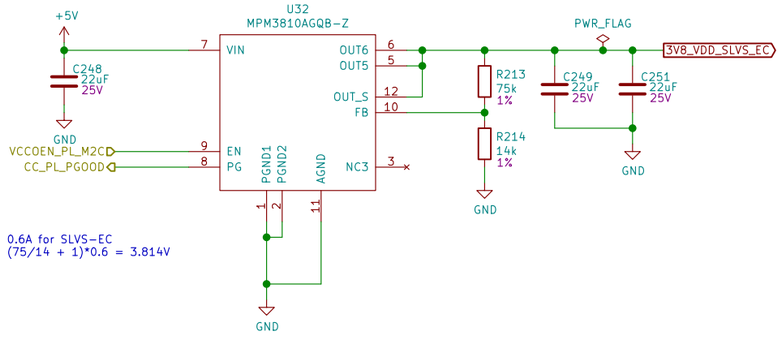
4A output for PL 1V8 for
0.6A for SLVS-EC 1.8V

PL 3V3



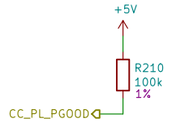
4A output for PL 3V3 for
HDA 3V3 1A
HDC 3V3 1A
Raspberry Pi Cams, 1A max each

SLVS-EC 3V8 for FRAMOS



0.6A for SLVS-EC
(75/14 + 1)*0.6 = 3.814V

Pull Up Resistor for CC_PL_PGOOD



Author: Chance Reimer
SCH: APT-KRIA-FMC
ApotheoTech LLC

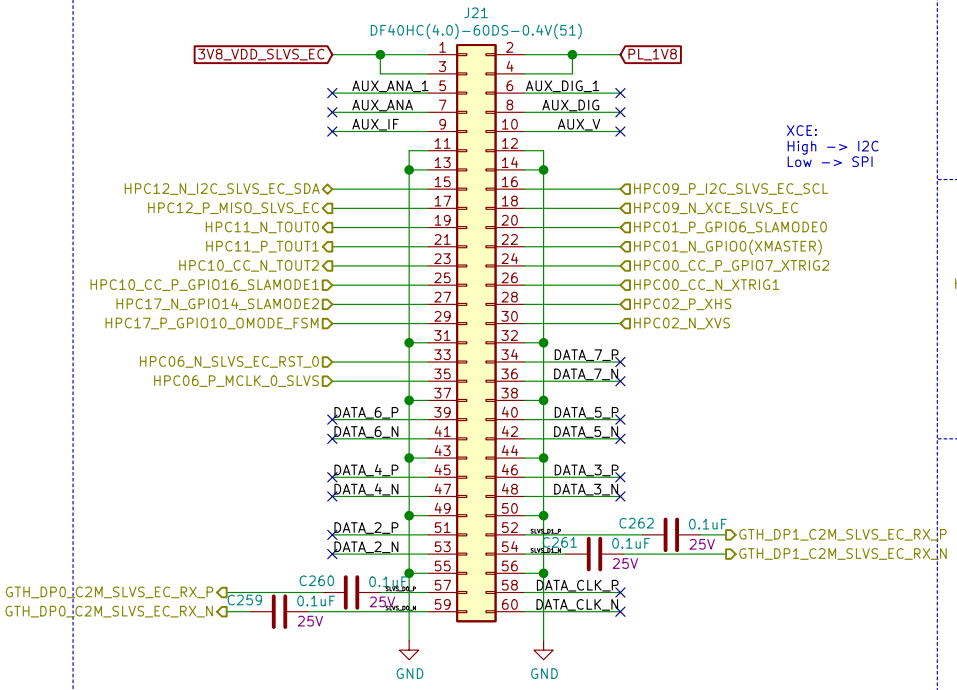
Sheet: /PL Power/
File: PL_Power.sch

Title: PL Power Kria

Size: A3	Date: 2022-01-04	**Rev: 1.00**
KiCad E.D.A. kicad (5.1.10)-1		Id: 13/20

FRAMOS PixelMate(TM) Connector – SLVS-EC

FRAMOS PixelMate(TM) Pinout SLVS-EC



Info about FRAMOS nomenclature:
FSM: Sensor Module
FSA: Sensor Module Adapter (has voltage specific for sensor)
FPA: Processing Board Adapter

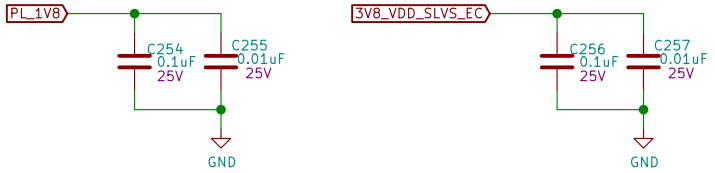
FSA for SLVS-EC is on page 30/62
(Connector J1 to FPA, which is this board)

Page 32 includes Amp draw
3V8VDD has 0.3A draw per pin, max 0.6A
1V8VDD has 0.3A draw per pin, max 0.6A

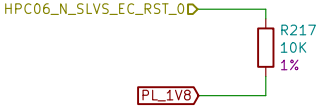
All GPIO and connection pins are
LVCMOS18 (1.8V)

SLVS-EC has no clock line
Stands for SLVS- Embedded Clock

Decoupling Caps



Pull up Resistors



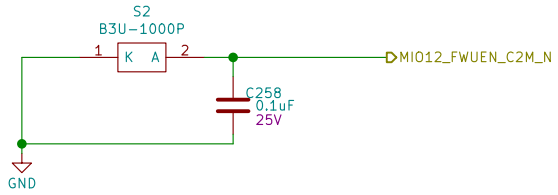
Author: Chance Reimer
SCH: APT-KRIA-FMC
ApotheoTech LLC
Sheet: /FRAMOS PixelMate(TM) Connector – SLVS-EC/
File: SLVS-EC_FRAMOS.sch

Title: FRAMOS PixelMate(TM) Connector – SLVS-EC

Size: A4	Date: 2022-01-04	**Rev: 1.00**
KiCad E.D.A. kicad (5.1.10)-1		Id: 14/20

Buttons, Shutdown, and Mode switch

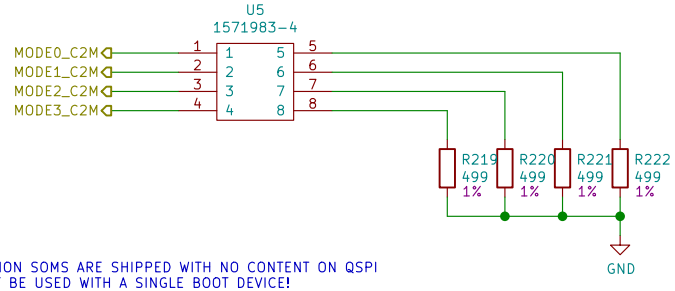
FWUEN BUTTON



SHUTDOWN

MODE SWITCH

Read Page 30 UG1091, MODE pins are tied to 1.8V on SOM,
Switches will leave the pins floating, and ground them when turned "on"



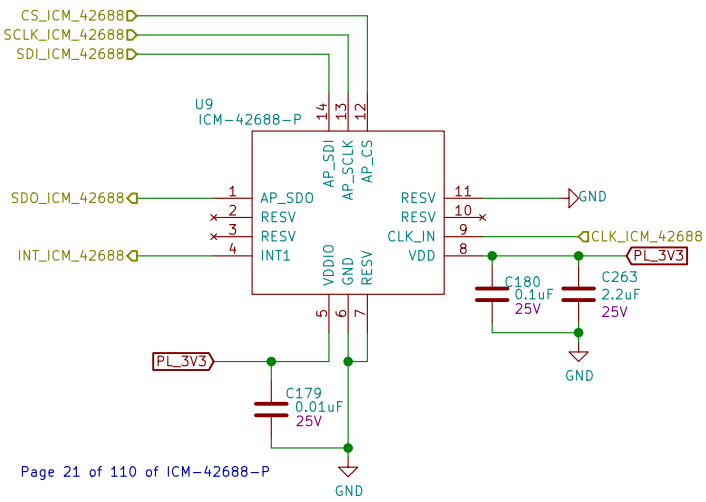
NOTE: PRODUCTION SOMS ARE SHIPPED WITH NO CONTENT ON QSPI
THUS BSP MUST BE USED WITH A SINGLE BOOT DEVICE!
(Source: https://xilinx-wiki.atlassian.net/wiki/spaces/A/pages/1641152513/Kria+K26+SOM#SD-Card-Images)
Go to Petalinux board support Packages Table

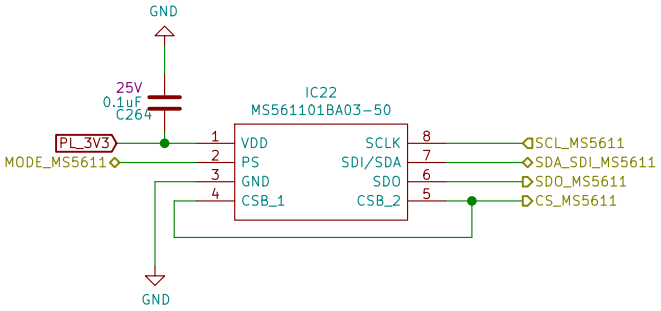
Note Boot Mode in UG1091 references UG1283, and UG1283 describes how to create boot image for EITHER QSPI or SD CARD.
Must use Mode pins to select which device to boot from

Note Boot Mode from Mode Pins
We are Interested in
boot_mode <= 4'b0, (JTAG)
boot_mode <= 4'b0010 (QSPI 32bit)
boot_mode <= 4'b0101(MIO[51:43])

Author: Chance Reimer SCH: APT-KRIA-FMC **ApotheoTech LLC**		
Sheet: /Buttons_Shutdown_MODE/ File: Buttons_Shutdown_MODE.sch		
Title: Buttons, Mode pins, Shutdown		
Size: A4	Date: 2022-01-04	**Rev: 1.00**
KiCad E.D.A. kicad (5.1.10)-1		Id: 15/20

Barometer and IMU





Author: Chance Reimer
SCH: APT-KRIA-FMC
ApotheoTech LLC

Sheet: /Baro_IMU/
File: Baro_IMU.sch

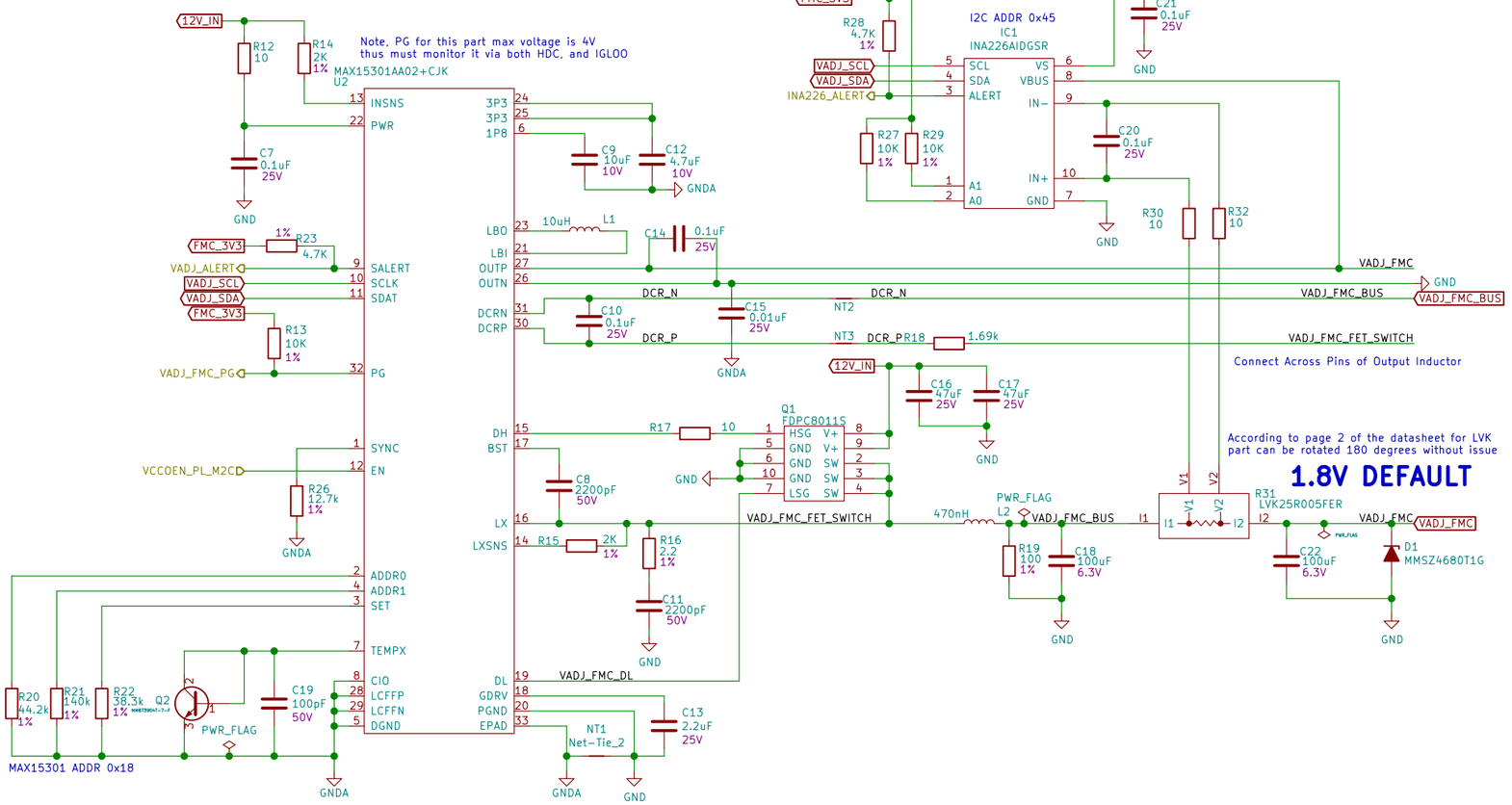
Title:

Size: A4	Date: 2022-01-04	**Rev: 1.00**
KiCad E.D.A. kicad (5.1.10)-1		Id: 16/20

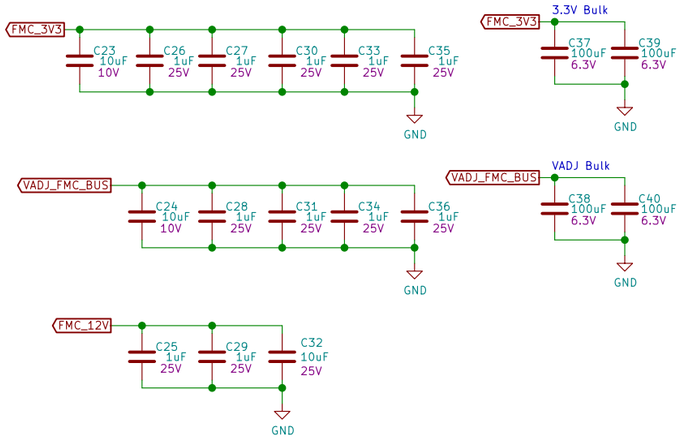
FMC POWER

(VADJ, 3.3V, and 12V lines from Kria SOM)

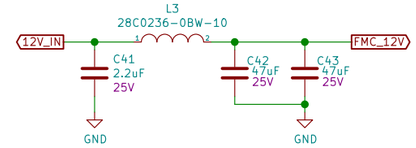
FMC VADJ (1.2, 1.5, 1.8V)



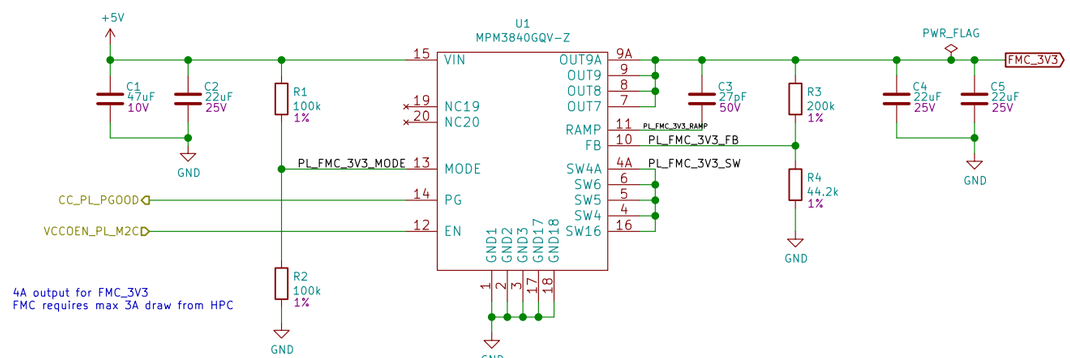
Decoupling Caps FMC



FMC_12V



FMC_3V3



Author: Chance Reimer
SCH: APT-KRIA-FMC
ApotheoTech LLC

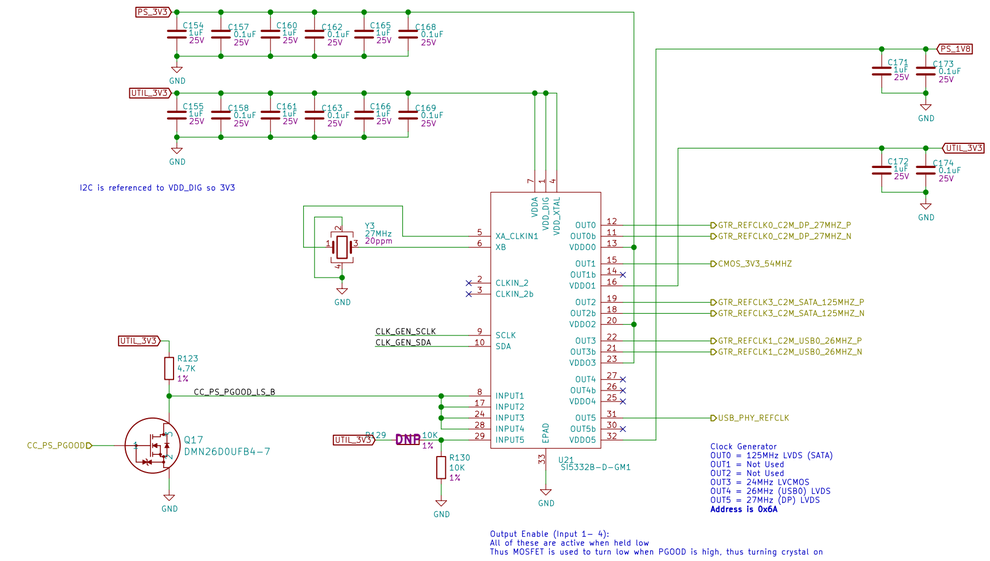
Sheet: /FMC_PWR/
File: FMC_PWR.sch

Title: FMC Power (VADJ, 3.3V, and 12V filt)

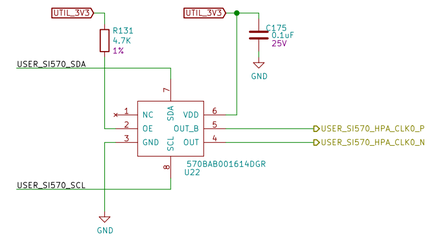
Size: A3	Date: 2022-01-04	**Rev: 1.00**
KiCad E.D.A. kicad (5.1.10)-1		Id: 17/20

Clocking for Kria/Camera MCLK/SYSCLK

Clock Generator



User Clk for Kria 200MHz for MIPI DPHY

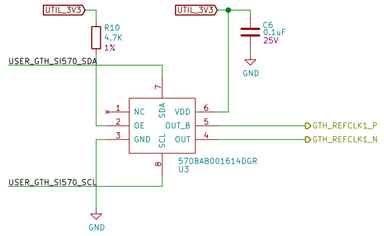


New Note: Looks like on Kria board they put 1.8V LVDS signal to the input pins of FPGA HPC side even if it isn't right standard. Use the programmable for HPC where 1.8V will support LVDS 1.8V, and we'll just use the 200MHz for HPB, which will be at 1.2V

The Note is we can't use LVDS in I/O VCCO bank 2A. bank 0 for HPC. VCCO must be 1.2V. Use CMOS/LVCMOS15 or above only!

Programming Connector For Clock Generators

I2C Mux for Kria Clock Gens



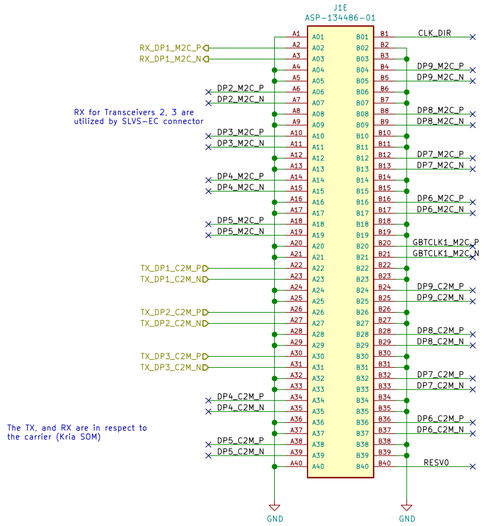
Author: Chance Reimer
SCH: APT-KRIA-FMC
ApotheoTech LLC
Sheet: /Clocks_All/
File: PS_Clocks.sch

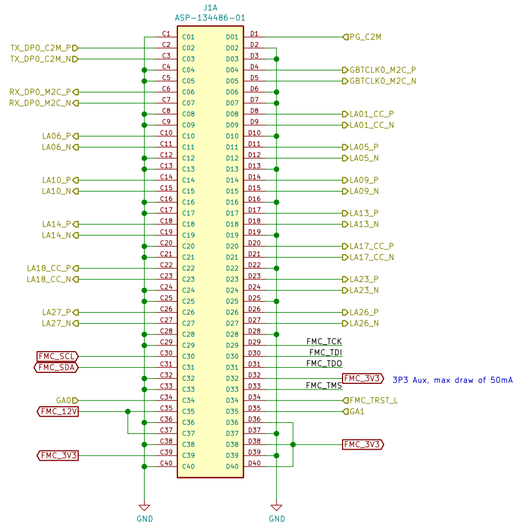
Title: Clocking PS and GTH

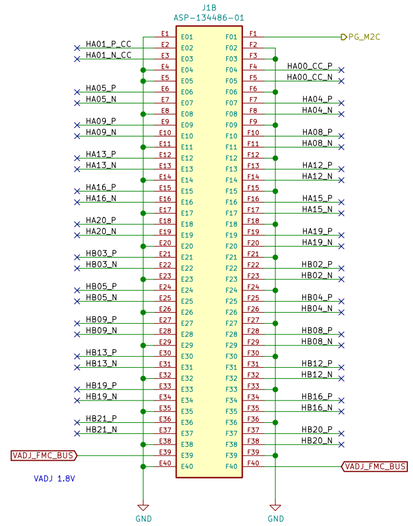
Size: A2	Date: 2022-01-04	**Rev: 1.00**
KiCad E.D.A. kicad (5.1.10)-1		Id: 18/20

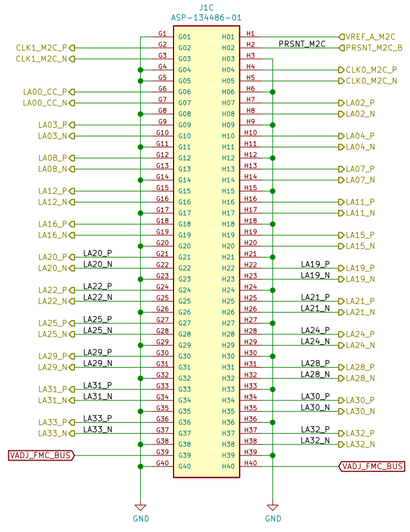
FMC Connector

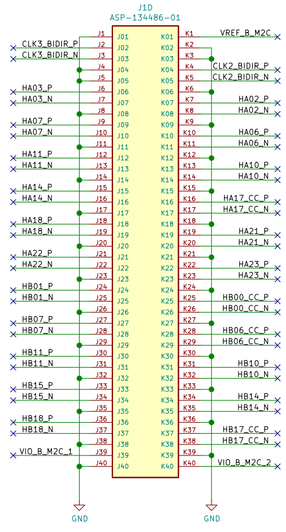
Modified HPC connection



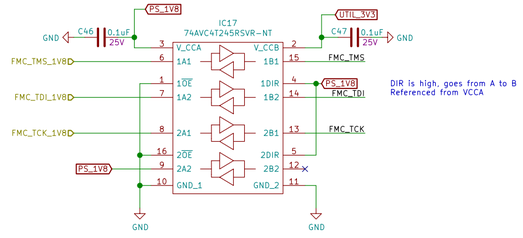


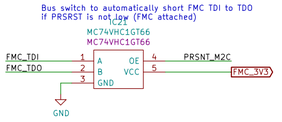


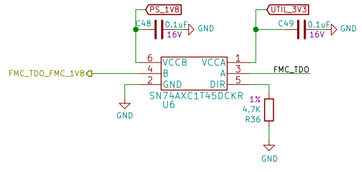




JTAG Voltage Level Shifter (1.8V to 3.3V)







Author: Chance Reimer
SCH: APT-KRIA-FMC
ApotheoTech LLC

Sheet: /FMC_Carrier_Conn/
File: FMC_Carrier_Conn.sch

Title: FMC Connection

Size: A2	Date: 2022-01-04	**Rev: 1.00**
KiCad E.D.A. kicad (5.1.10)-1		Id: 19/20

Kria SOM240-2 GTH, HPIO Banks 65, 64, and HDIO Bank 43, 44

Remember Chance, We are the Carrier on this design

C2M -> RX for Kria module

M2C -> TX for Kria module

Author: Chance Reimer
SCH: APT-KRIA-FMC
ApotheoTech LLC

Sheet: /SOM240_2/
File: SOM240_2.sch

Title: SOM240_2 Kria Connector (GTH and Banks 65, 64, and 43)

Size: A3	Date: 2022-01-04	**Rev: 1.00**
KiCad E.D.A. kicad (5.1.10)-1		Id: 20/20