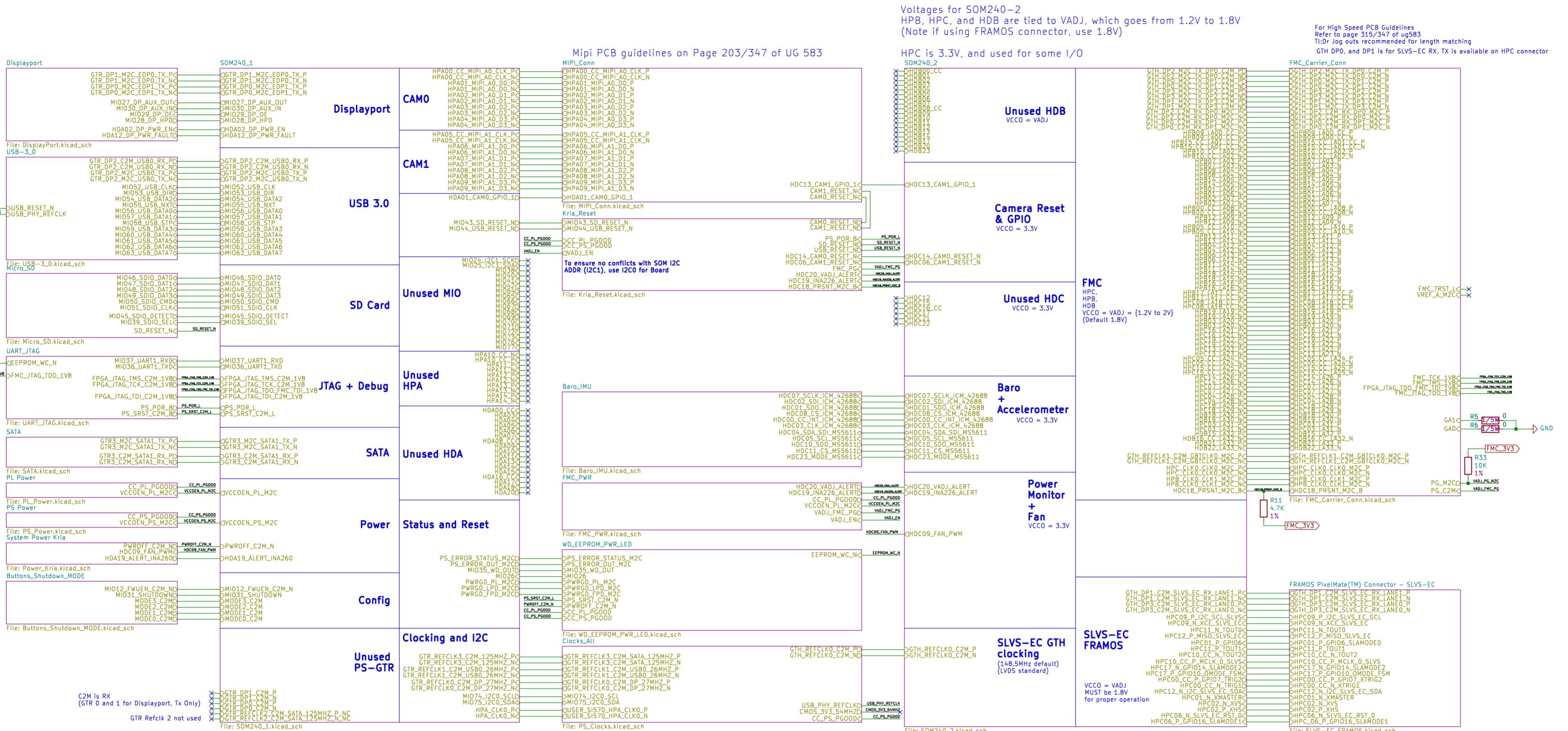
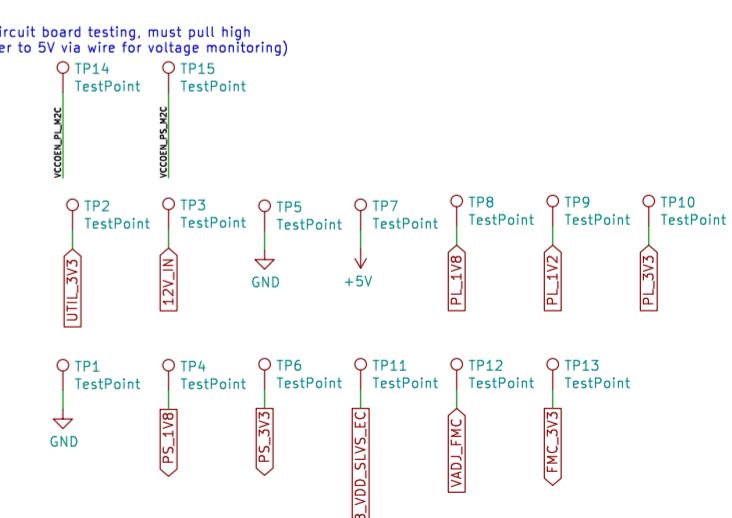


TOP SHEET

Revision 1



Test Points



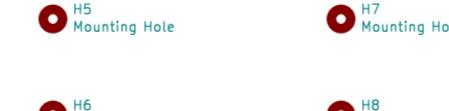
FMC Mounting Holes



FSM/FSA Mounting Holes



Mounting Holes



Kria JSOM mounting Hole

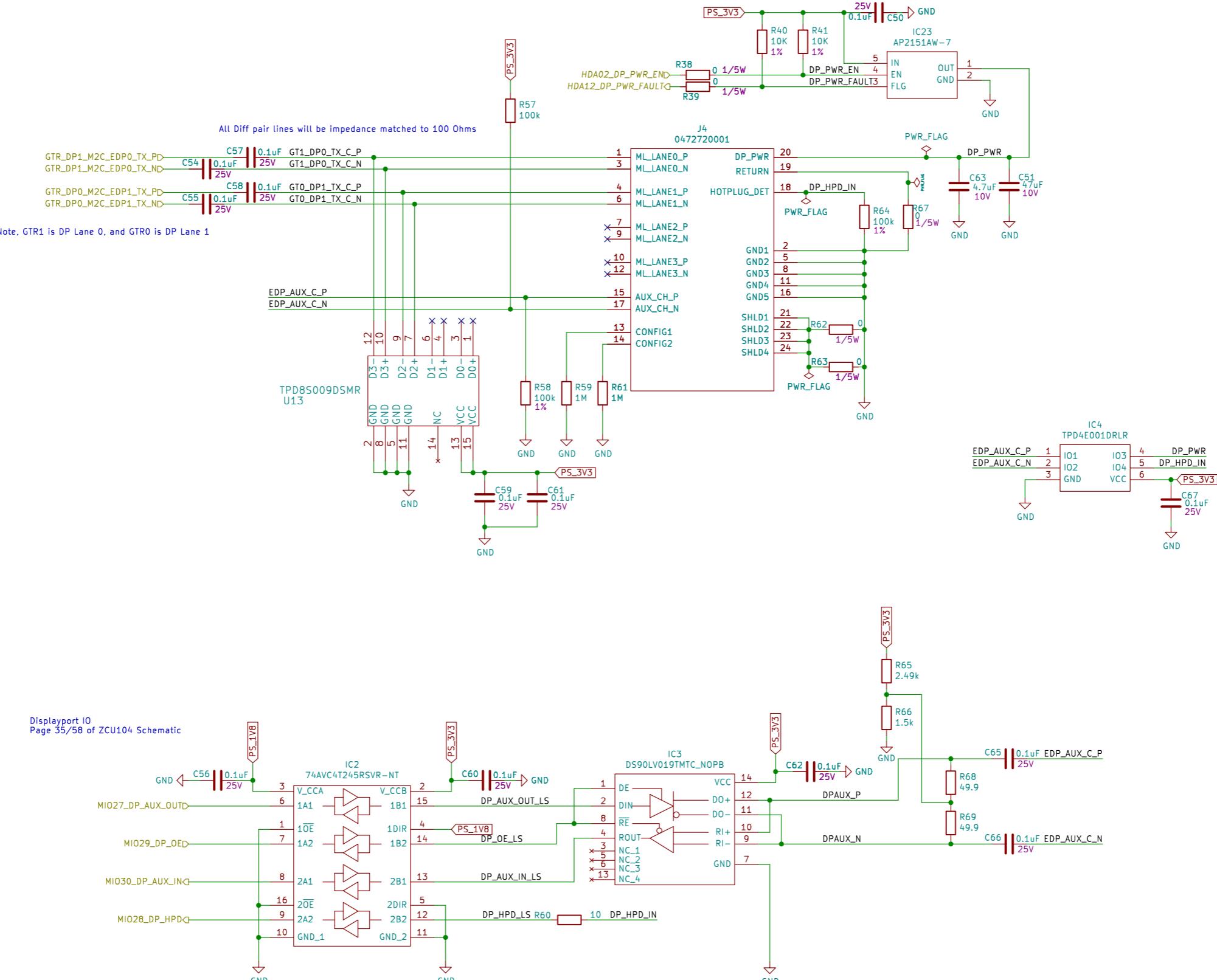


Author: Chance Reimer
SCH: APT-KRIA-FMC
ApotheoTech LLC
Sheet 4

_sch



DisplayPort GTR



Displayport IO
Page 35/58 of ZCU104 Schematic

Author: Chance Reimer

SCH: APT-KRIA-FMC

ApotheoTech LLC

Sheet: /DisplayPort/
File: DisplayPort.kicad_sch

Title: Mini DisplayPort

Size: A3 Date: 2022-01-04

KiCad E.D.A. kicad (7.0.0)

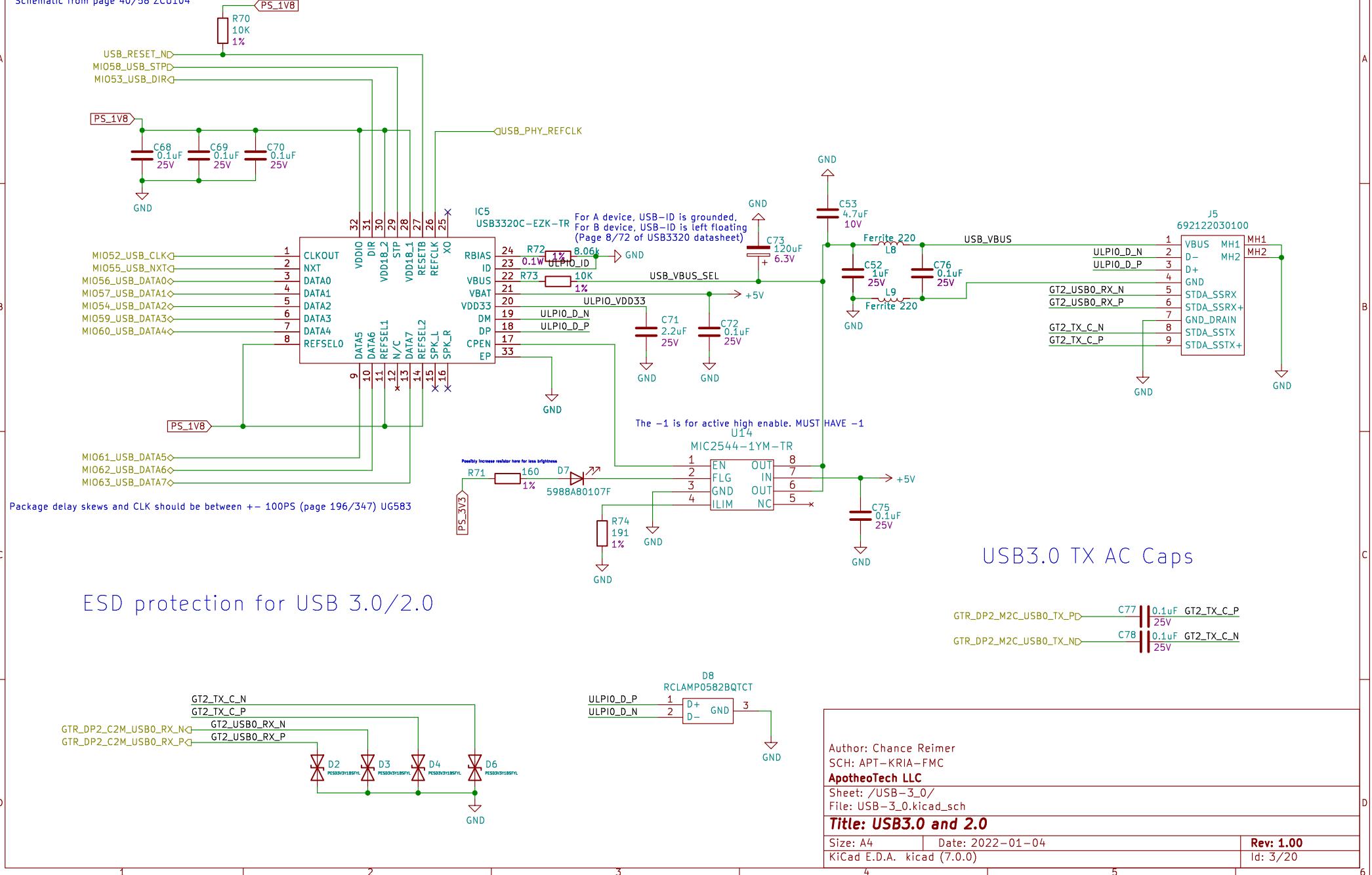
7

Id: 2/20

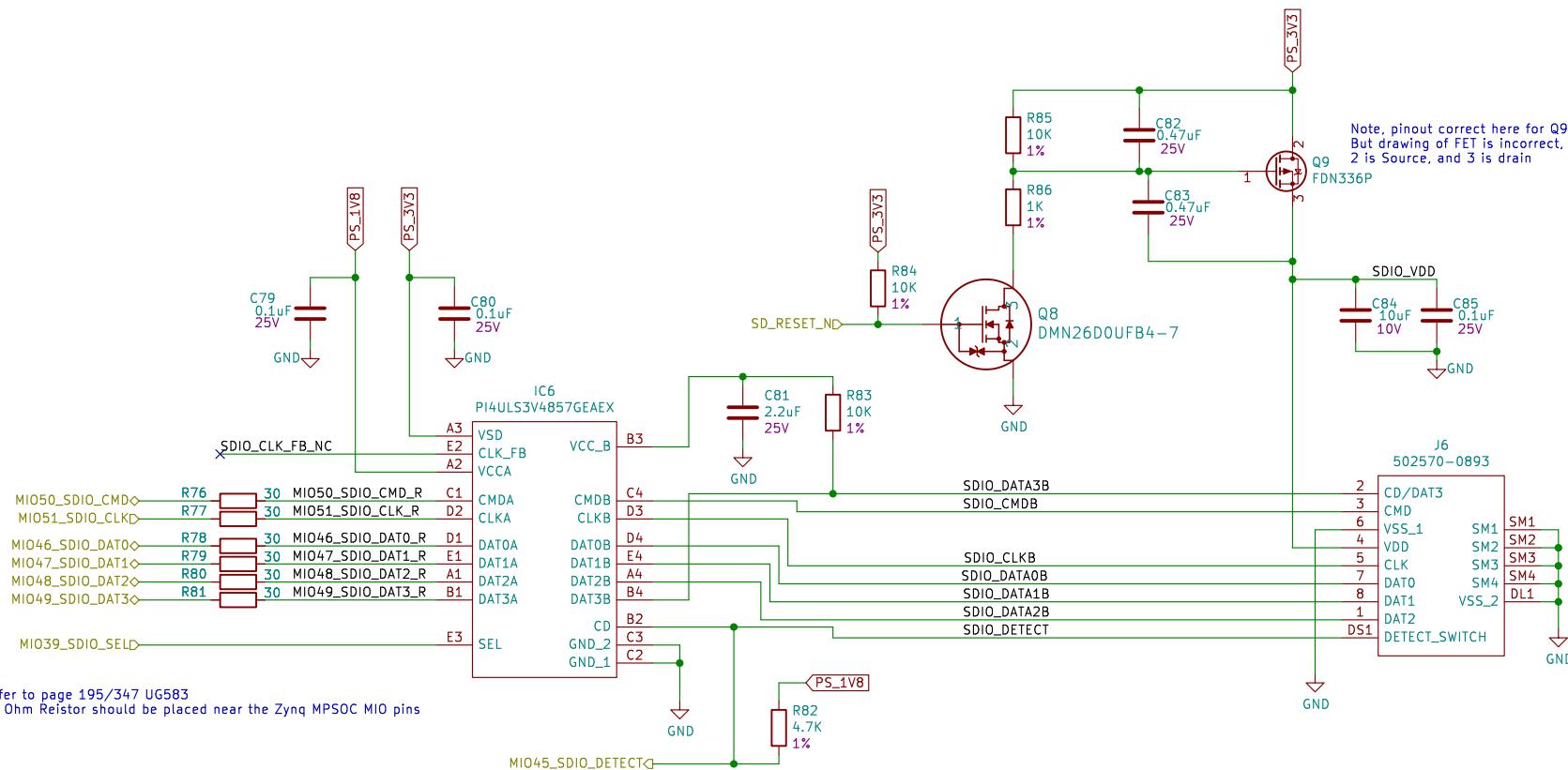
8

USB 3.0 and USB 2.0 (HOST)

Schematic from page 40/58 ZCU104



SD 3.0



Refer to page 195/347 UG583
30 Ohm Resistor should be placed near the Zynq MPSOC MIO pins

Author: Chance Reimer

SCH: APT-KRIA-FMC

ApotheoTech LLC

Sheet: /Micro_SD/
File: Micro_SD.kicad_sch

Title: SD 3.0 Card

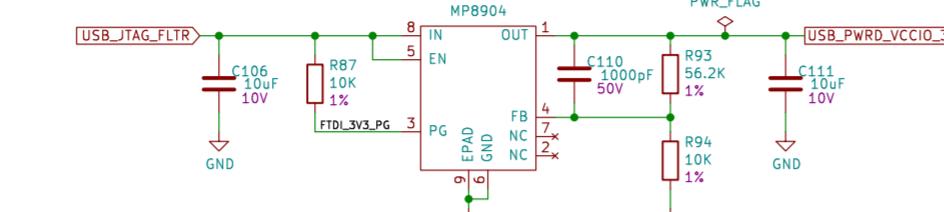
Size: A4 Date: 2023-01-01

KiCad EDA kicad (7.0)

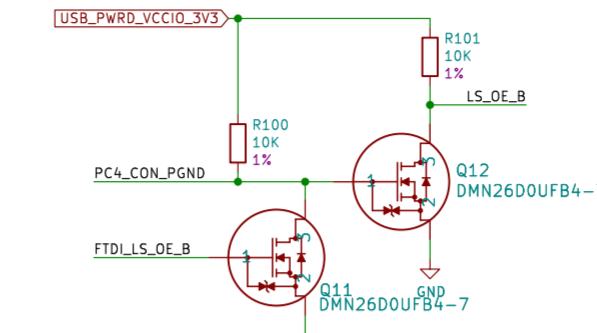
Rev. 1.00

Rev: 1.00
Id: 4/20

JTAG, USB DBG



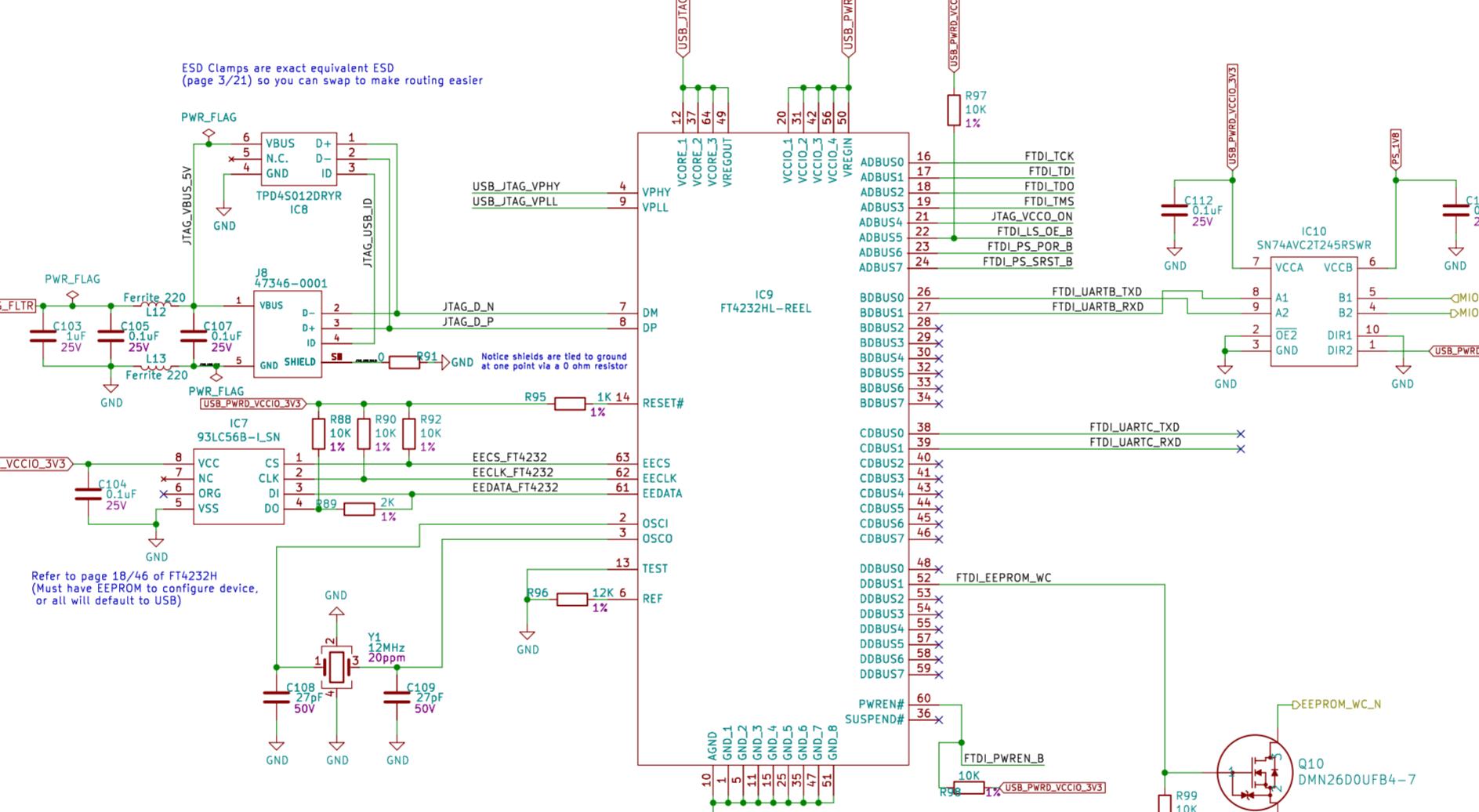
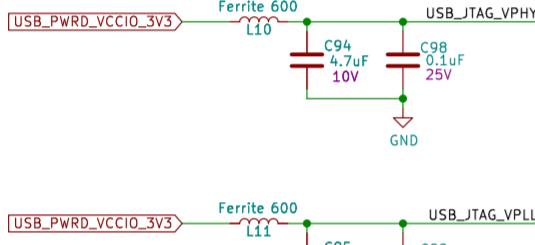
Reset Sequence for JTAG



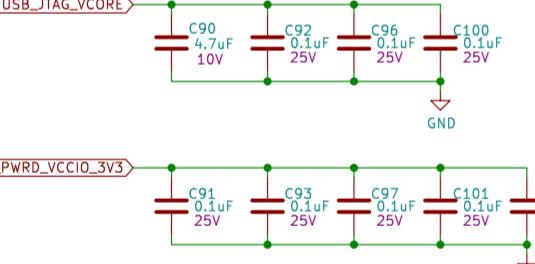
FT4232HL PLL and PHY filtering

FT4232, refer to page 9 of Kria Carrier Board

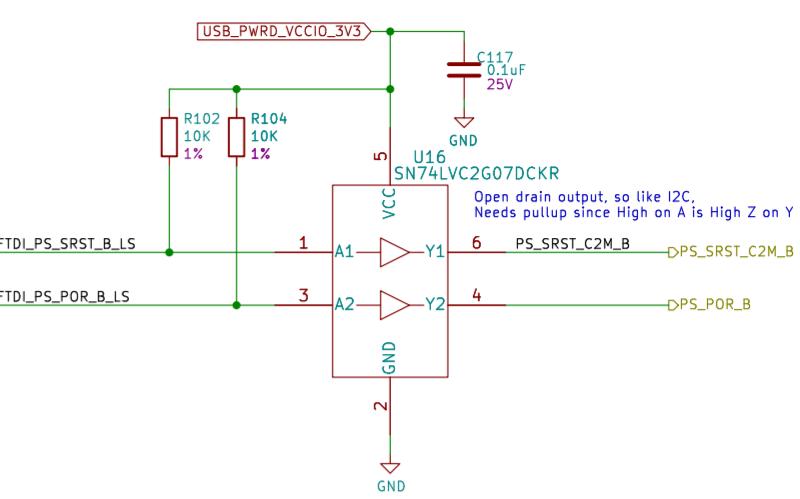
Must copy Kria EEPROM for FTDI USB to JTAG



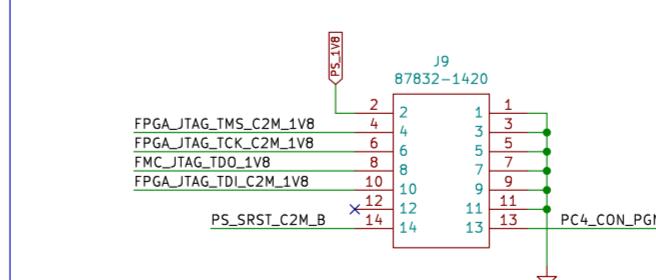
FT4232HL Decoupling Caps



Voltage level converters for JTAG and Status



Kria JTAG Connector



Note DS593 page 17. Note 5
Pin 13 is grounded on legacy Xilinx USB cables.
they need to be detached from 2mm connector
if FT4232H wants to communicate via JTAG.

Author: Chance Reimer

Author: Chance Rehner
SCH: APT-KRIA-FMC
ApotheoTech LLC
Sheet: /UART JTAG/

File: UART_JTAG.kicad_sch

Size: A2 Date: 2022-01-04 Rev: 1.00
KiCad E.D.A. kicad (7.0.0) Id: 5/20

10 11

SATA

A

A

B

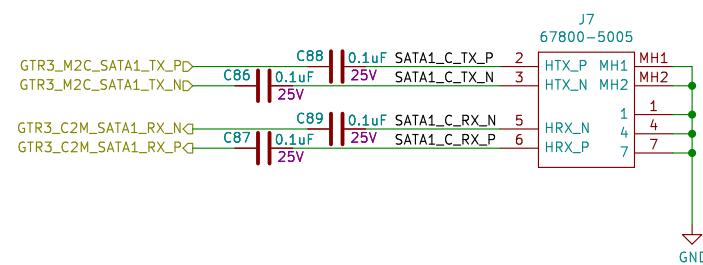
B

C

C

D

D



Author: Chance Reimer

SCH: APT-KRIA-FMC

ApotheoTech LLC

Sheet: /SATA/

File: SATA.kicad_sch

Title: SATA 1 lane

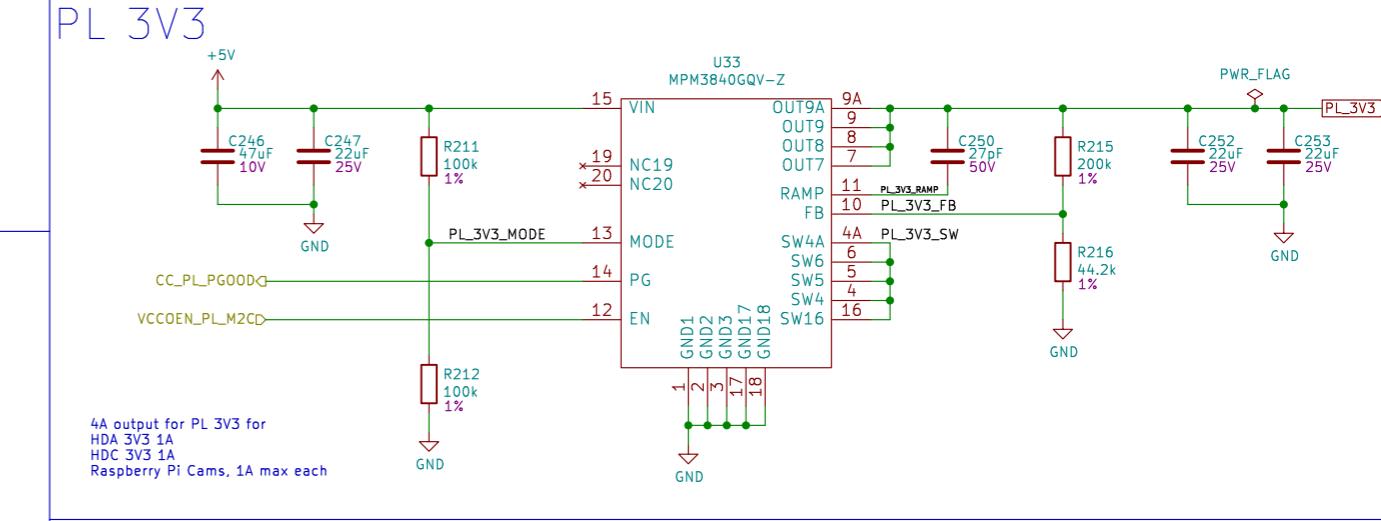
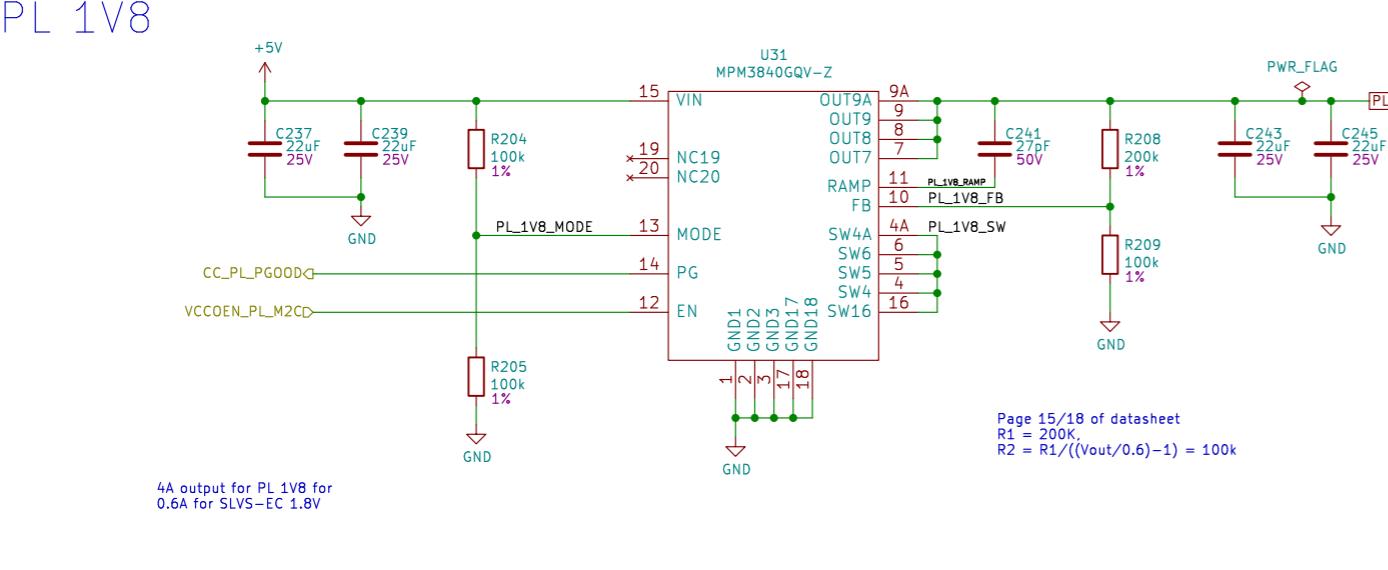
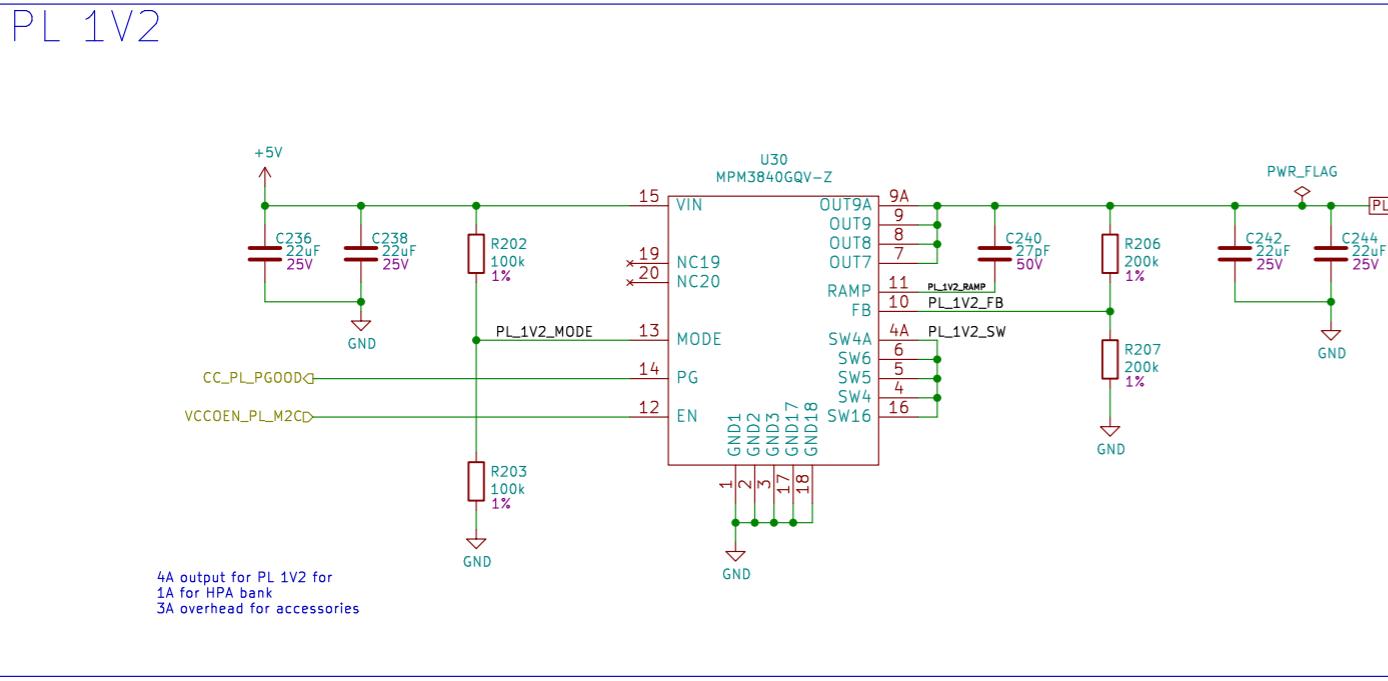
Size: A4 Date: 2022-01-04

KiCad E.D.A. kicad (7.0.0)

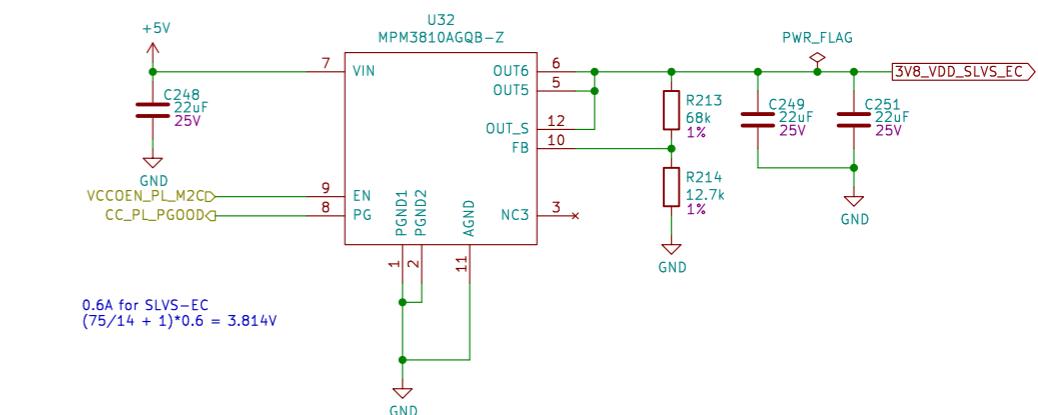
Rev: 1.00

Id: 6/20

Kria PL Power



SLVS-EC 3V8 for FRAMOS



Pull Up Resistor for CC_PL_PGO

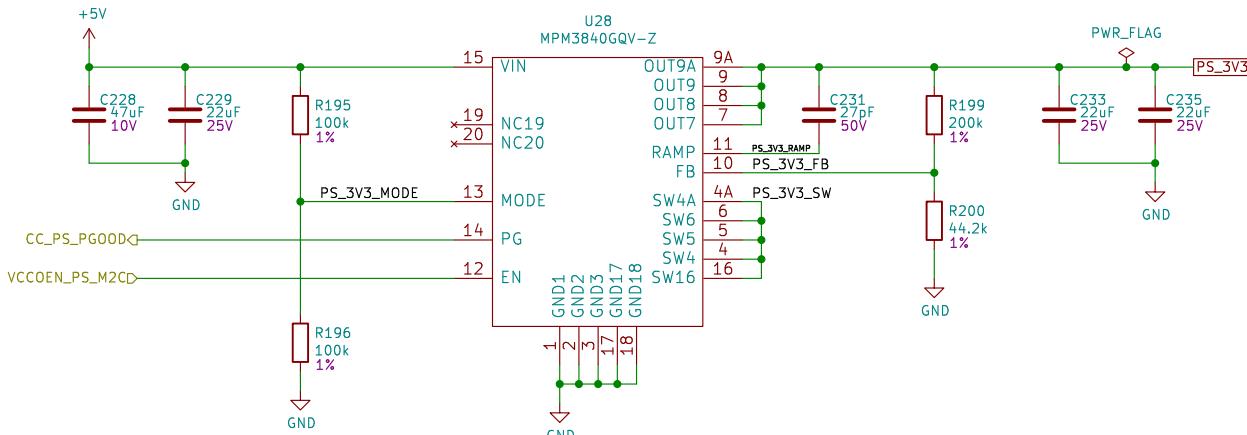


Author: Chance Reimer
SCH: APT-KRIA-FMC
AntheoTech LLC

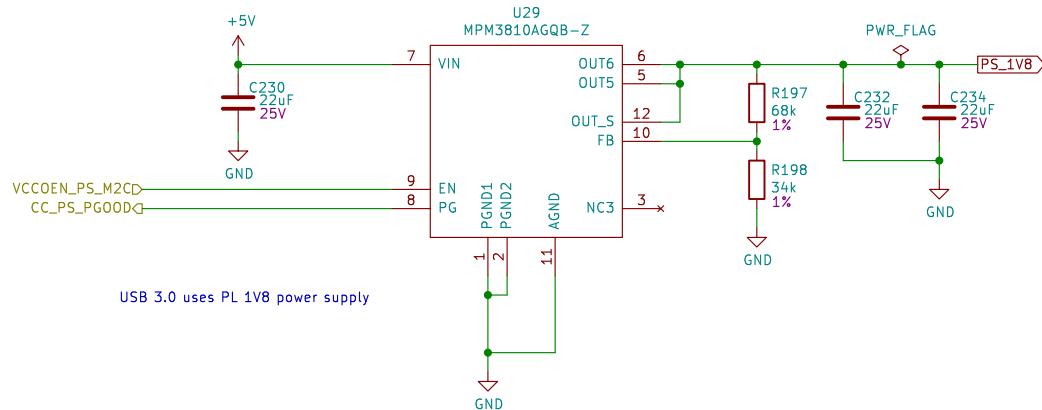
ApotheoTECH LLC
Sheet: /PL Power/
File: PL_Power.kicad_sch
Title: PL Power K

Kria PS Power

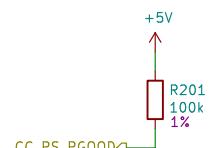
PS 3V3



PS 1V8



Pull Up Resistor for CC_PS_PGOOD



Author: Chance Reimer

SCH: APT-KRIA-FMC

ApotheoTech LLC

Sheet: /PS Power/

File: PS_Power.kicad_sch

Title: PS Power for Kria SOM

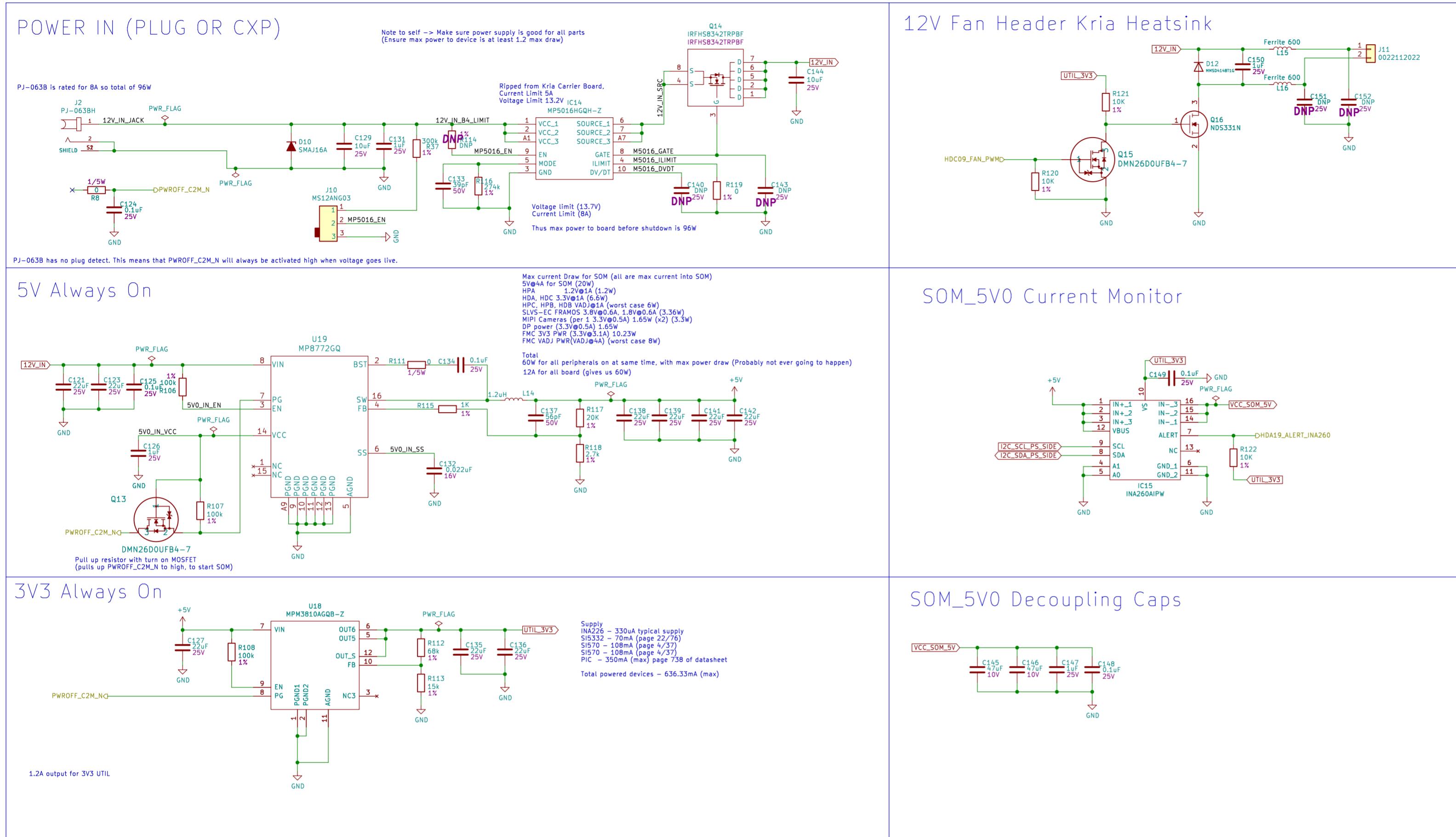
Size: A4 Date: 2022-01-04

KiCad E.D.A. kicad (7.0.0)

Rev: 1.00

Id: 8/20

Kria System Power



Author: Chance Reimer
SCH: APT-KRIA-FMC
ApotheoTech LLC
Sheet: /System Power Kria/
File: Power_Kria.kicad_sch

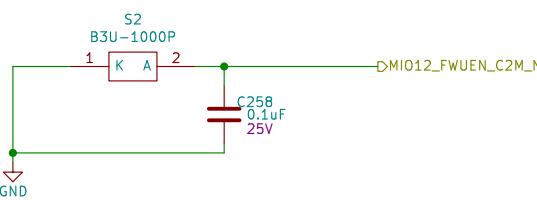
Title: System Power for Kria SOM

Size: A2 Date: 2022-01-0
KiCad E.D.A. kicad (7.0.0)

10

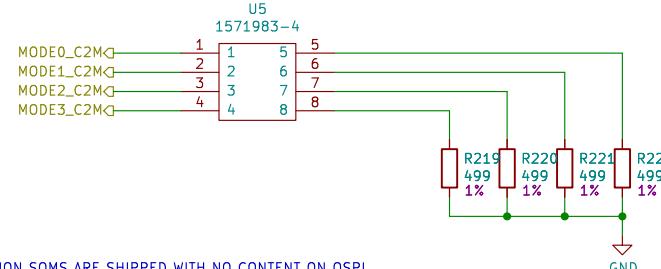
Buttons, Shutdown, and Mode switch

FWUEN BUTTON



MODE SWITCH

Read Page 30 UG1091, MODE pins are tied to 1.8V on SOM.
Switches will leave the pins floating, and ground them when turned "on"



SHUTDOWN



NOTE: PRODUCTION SOMS ARE SHIPPED WITH NO CONTENT ON QSPI
THUS BSP MUST BE USED WITH A SINGLE BOOT DEVICE!
(Source: <https://xilinx-wiki.atlassian.net/wiki/spaces/A/pages/1641152513/Kria+K26+SOM#SD-Card-Images>)
Go to Petalinux board support Packages Table

Note Boot Mode in UG1091 references UG1283, and UG1283 describes how to create boot image for EITHER QSPI or SD CARD.
Must use Mode pins to select which device to boot from

Note Boot Mode from Mode Pins

We are Interested in
boot_mode <= 4'b0_ (JTAG)
boot_mode <= 4'b0010 (QSPI 32bit)
boot_mode <= 4'b0101(MIO[51:43])

Author: Chance Reimer

SCH: APT-KRIA-FMC

ApotheoTech LLC

Sheet: /Buttons_Shutdown_MODE/

File: Buttons_Shutdown_MODE.kicad_sch

Title: Buttons, Mode pins, Shutdown

Size: A4 Date: 2022-01-04

KiCad E.D.A. kicad (7.0.0)

Rev: 1.00

Id: 10/20

Kria SOM240-1 GTR, HPIO Banks 66, MIO banks, HDIO bank 45

Remember Chance, We are the Carrier on this design

C2M → RX for Kria module
M2C → TX for Kria module

Note, to support MIPI pin standard,
VCC0 must be 1.2V
(Page 143, UG571)



SOM 5VO Decoupling

Author: Chance Reimer

SCH: APT-KRIA-FMC

ArotheoTech LLC

Sheet: /SOM240_1/

File: SOM240_1.kicad_sch

Title: SOM240-1

Size: A3 Date: 2022-01-0

KiCad E.D.A. kicad (7.0.0)

Digitized by srujanika@gmail.com

Rev: 1.00

Id: 11/20

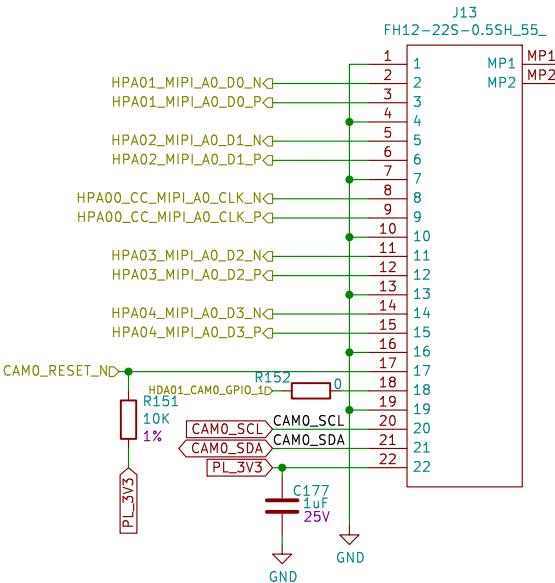
3

10 of 10

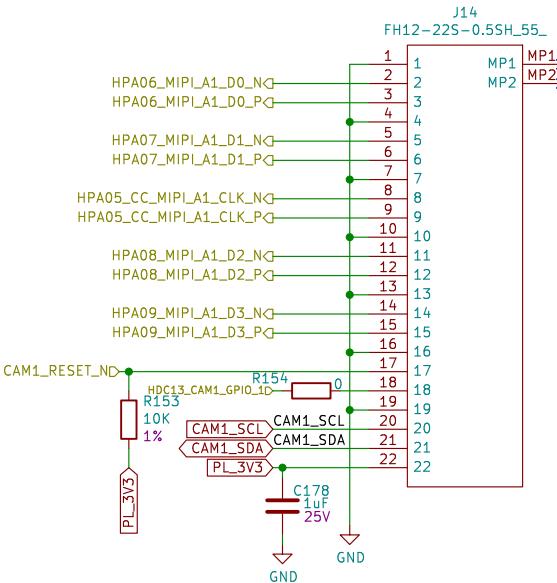
ALL MIPI CONNECTORS

Referenced from <https://www.arducam.com/raspberry-pi-camera-pinout/>
And from CM4IOV5 schematic for MIPI connectors

MIPI CSI-2 Connectors



Mipi PCB guidelines on Page 203/347 of UG 583



Author: Chance Reimer

SCH: APT-KRIA-FMC

ApotheoTech LLC

Sheet: /MIPI_Conn/

File: MIPI_Conn.kicad_sch

Title: MIPI DSI and CSI-2 Connectors

Size: A4 Date: 2022-01-04

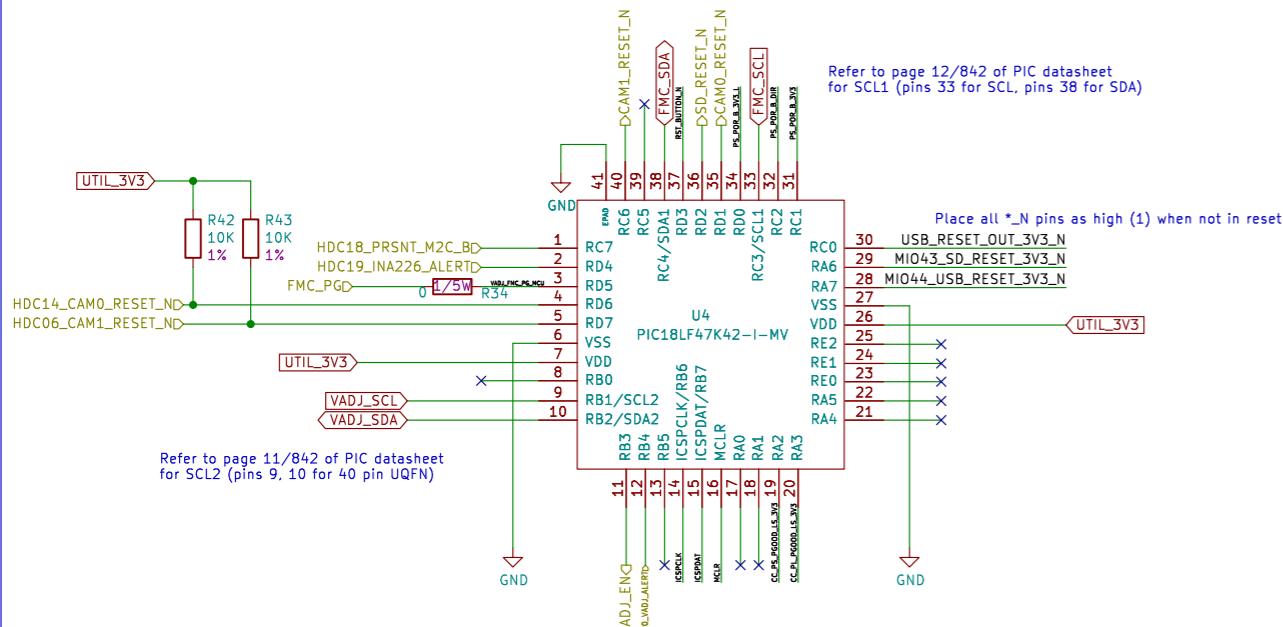
KiCad E.D.A. kicad (7.0.0)

Rev: 1.00

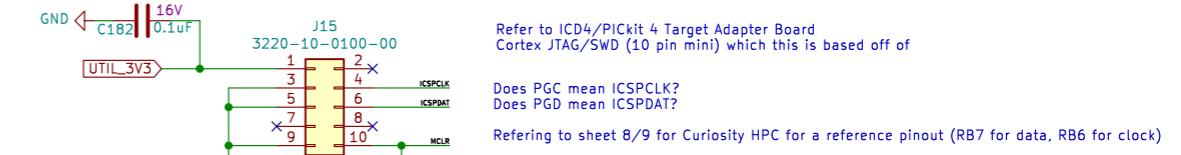
Id: 12/20

PIC18LF47K42-I/MV Reset for Kria Carrier

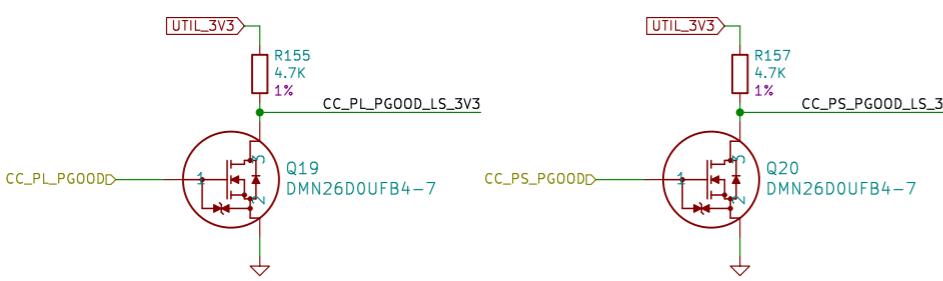
PIC18LF47K42-I/MV Reset Pinout



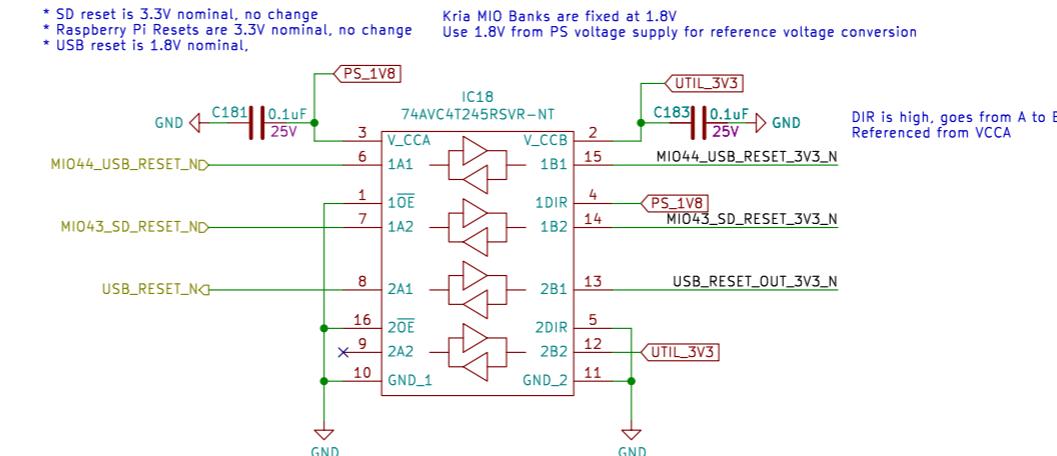
CORTEX JTAG/SWD (10 pin mini)



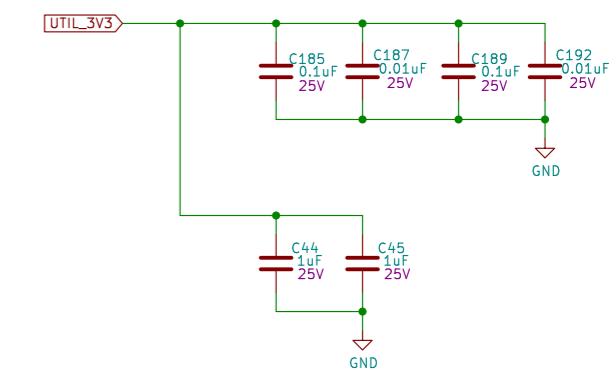
CC_PL Voltage Changes



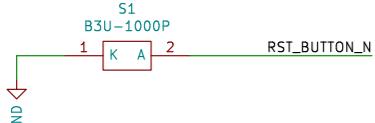
Voltage Level Conversion



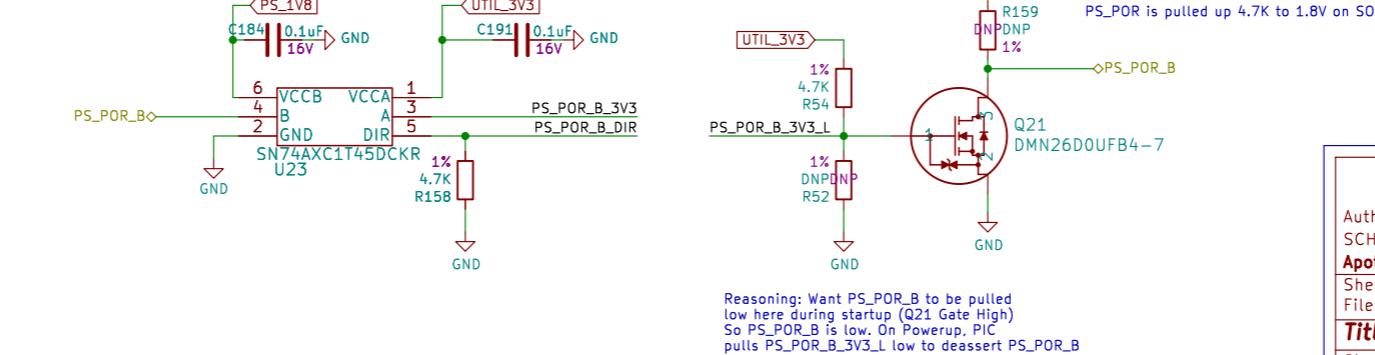
Decoupling Caps



Reset Button

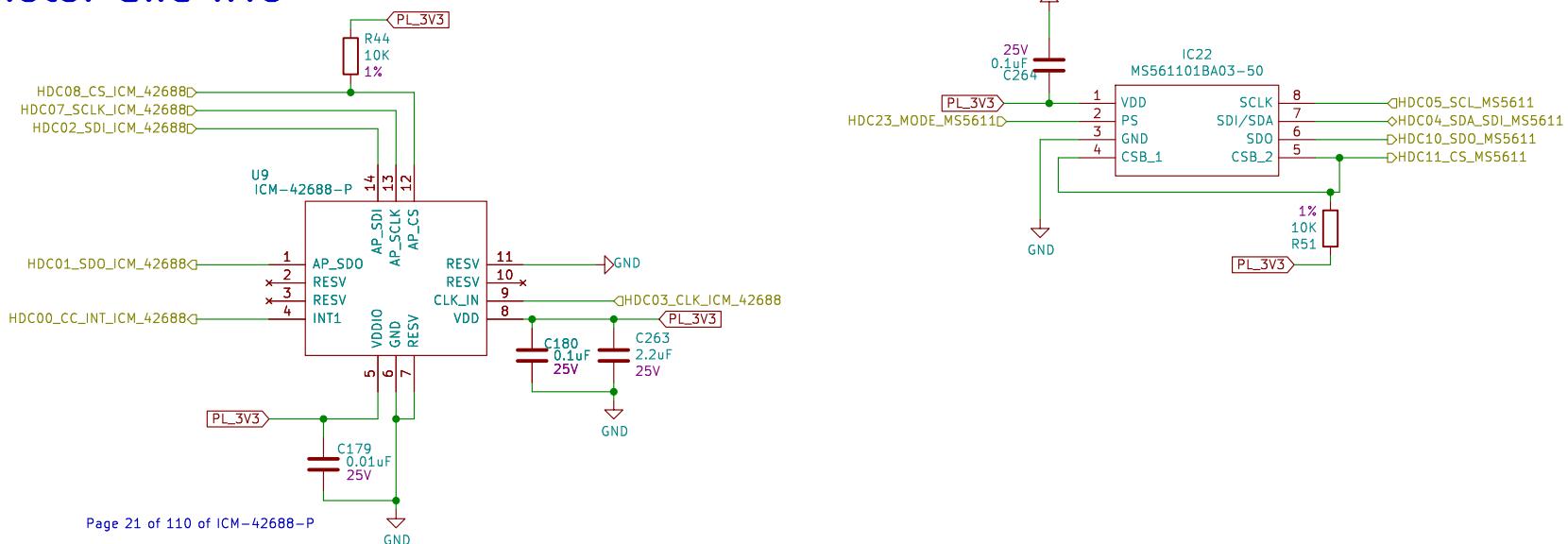


PS_POR_B



Author: Chance Reimer
 SCH: APT-KRIA-FMC
 ApotheoTech LLC
 Sheet: /Kria_Reset/
 File: Kria_Reset.kicad_sch
Title: IGLOO nano Reset for Kria Carrier
 Size: A3 | Date: 2022-01-04
 KiCad E.D.A. kicad (7.0.0) | Rev: 1.00
 Id: 13/20

Barometer and IMU



Author: Chance Reimer

SCH: APT-KRIA-FMC

ApotheoTech LLC

Sheet: /Baro_IMU/

File: Baro_IMU.kicad_sch

Title:

Size: A4 | Date: 2022-01-04

KiCad E.D.A. kicad (7.0.0)

Rev: 1.00

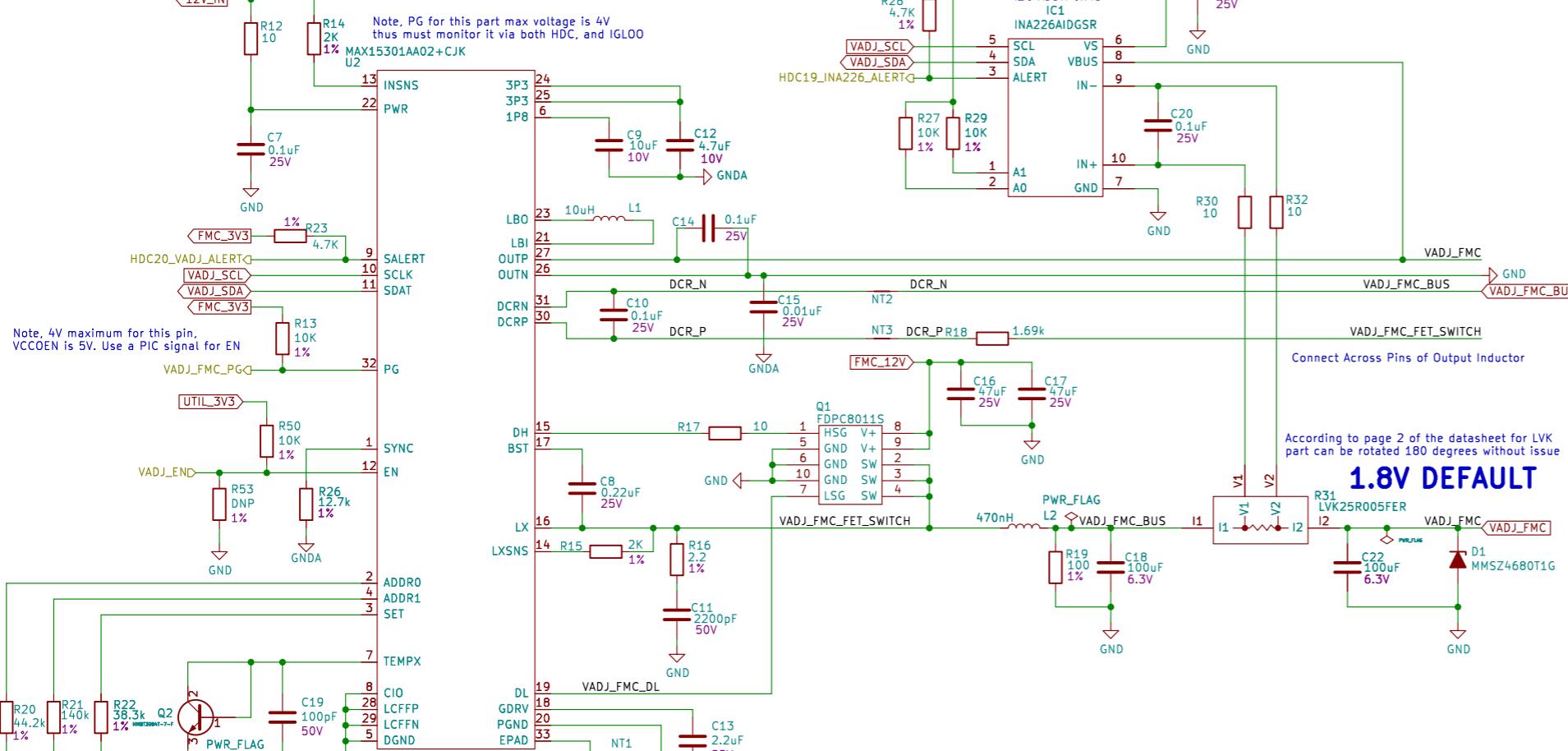
Id: 14/20

FMC POWER

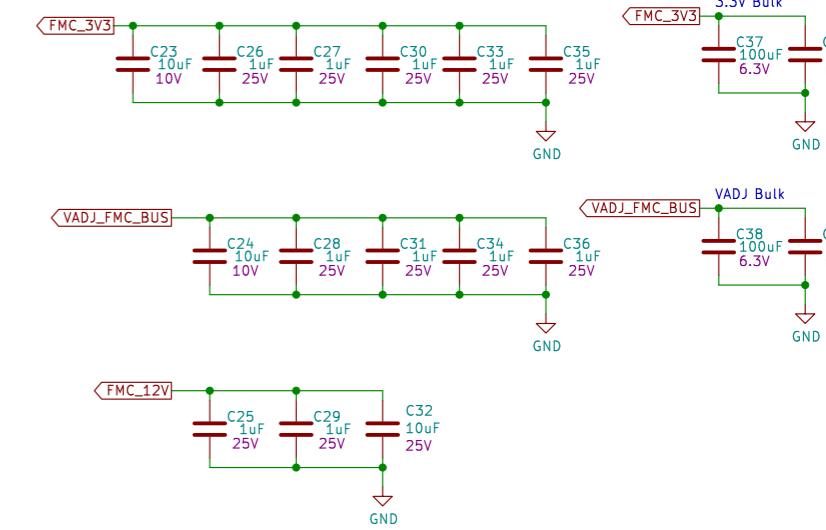
(VADJ, 3.3V, and 12V lines from Kria SOM)

FMC VADJ (1.2, 1.5, 1.8V)

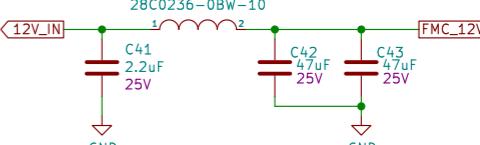
Page 73/95 ZCU106 Schematic for Reference



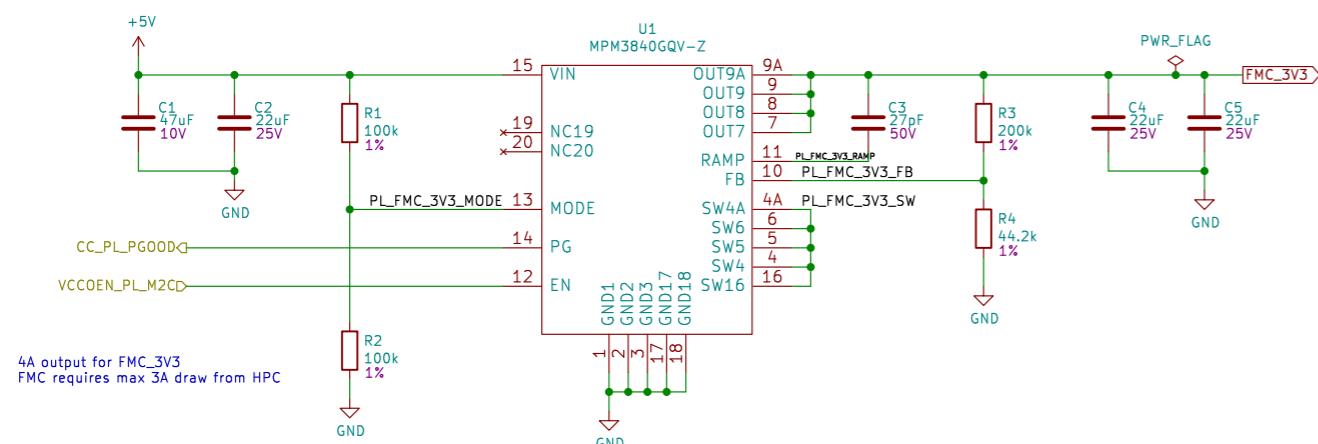
Decoupling Caps FMC



FMC_12V



FMC_3V3



Author: Chance Reimer

SCH: APT-KRIA-FMC

ApotheoTech LLC

Sheet: /FMC_PWR/

File: FMC_PWR.kicad_sch

Title: FMC Power (VADJ, 3.3V, and 12V filt)

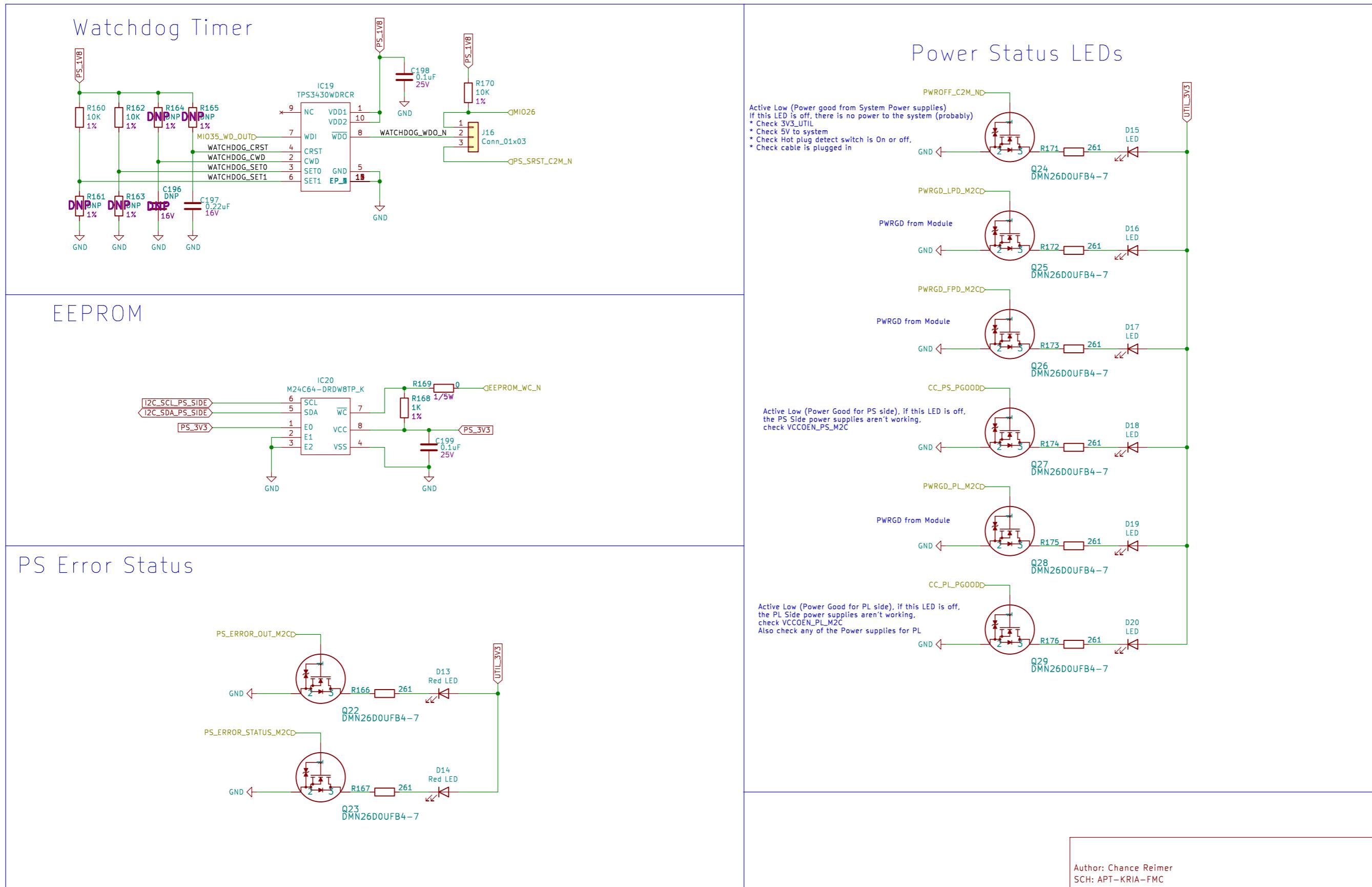
Size: A3 | Date: 2022-01-04

KiCad E.D.A. kicad (7.0.0)

Rev: 1.00

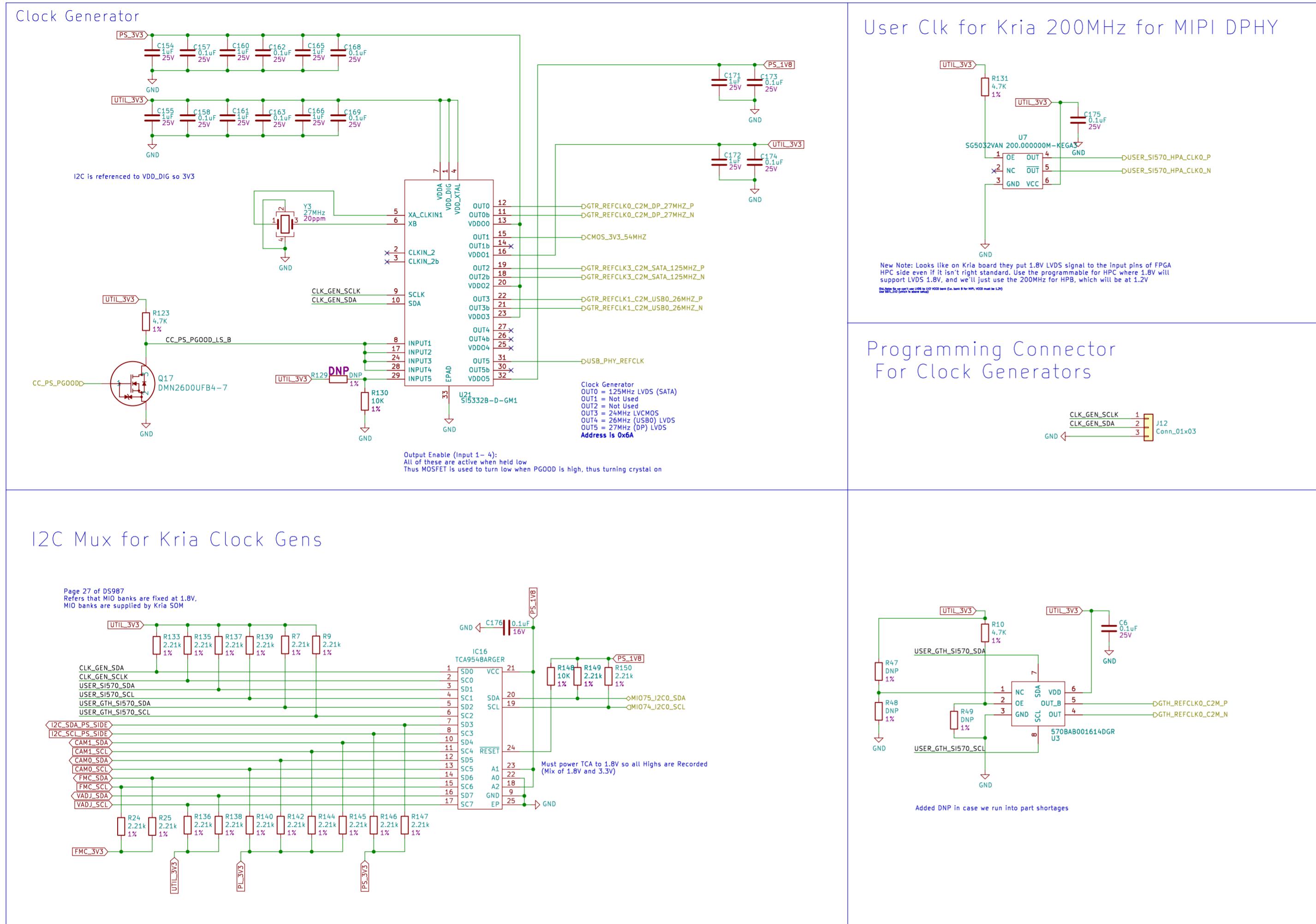
Id: 15/20

WatchDog Timer, EEPROM, and Power LED Signals



Author: Chance Reimer
 SCH: APT-KRIA-FMC
ApotheoTech LLC
 Sheet: /WD_EEPROM_PWR_LED/
 File: WD_EEPROM_PWR_LED.kicad_sch
Title: WatchDog, EEPROM, Power LED
 Size: A3 | Date: 2022-01-04
 KiCad E.D.A. kicad (7.0.0) | Rev: 1.00
 Id: 16/20

Clocking for Kria/Camera MCLK/SYSCLK



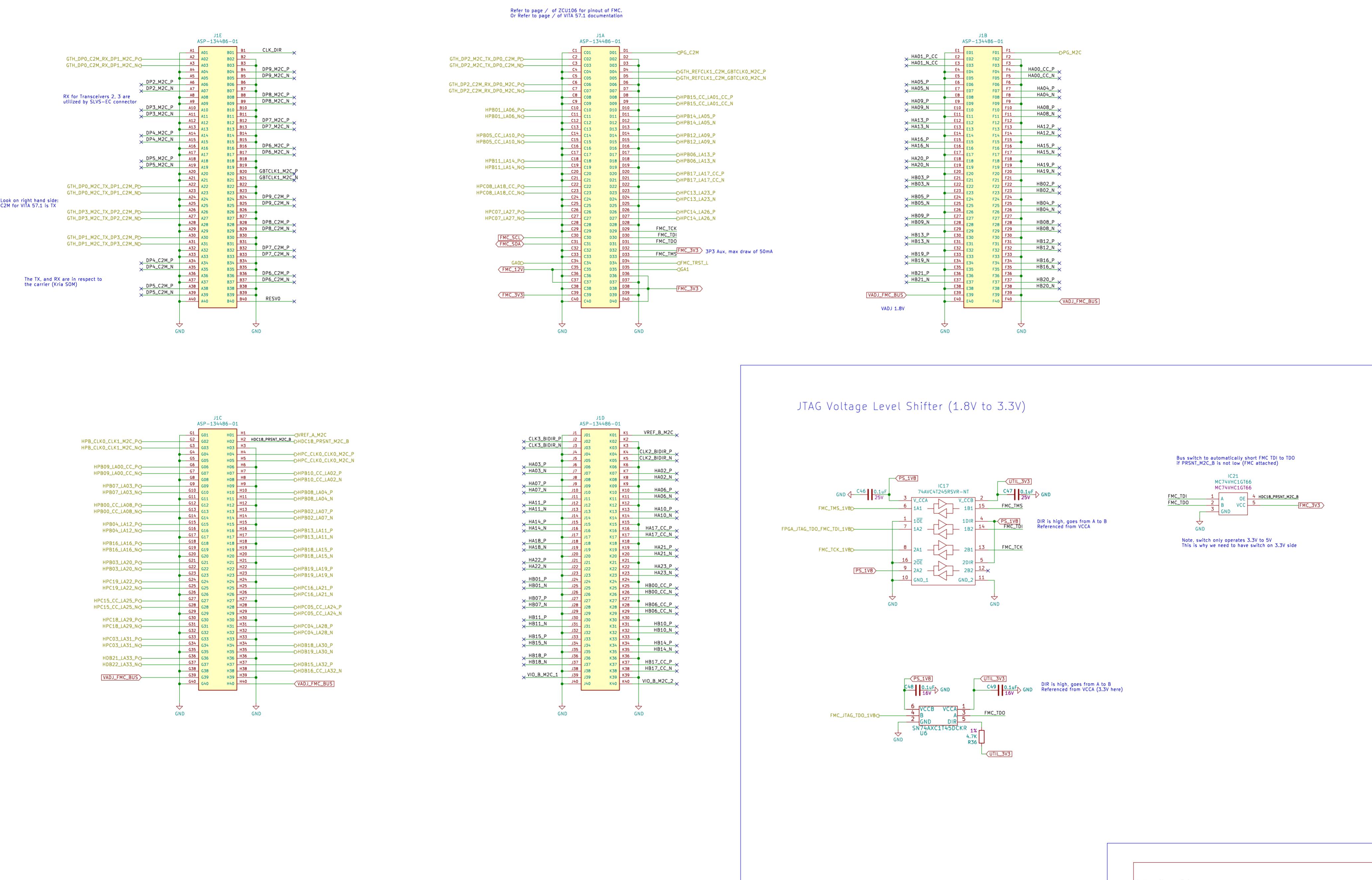
Author: Chance Reimer
SCH: APT-KRIA-FMC
ApotheoTech LLC
Sheet: /Clocks_All/
File: PS_Clocks.kicad_sch
Title: Clocking PS and GTH

Size: A2 Date: 2022-01-04
KiCad E.D.A. kicad (7.0.0) Rev: 1.00

16: 17/20

FMC Connector

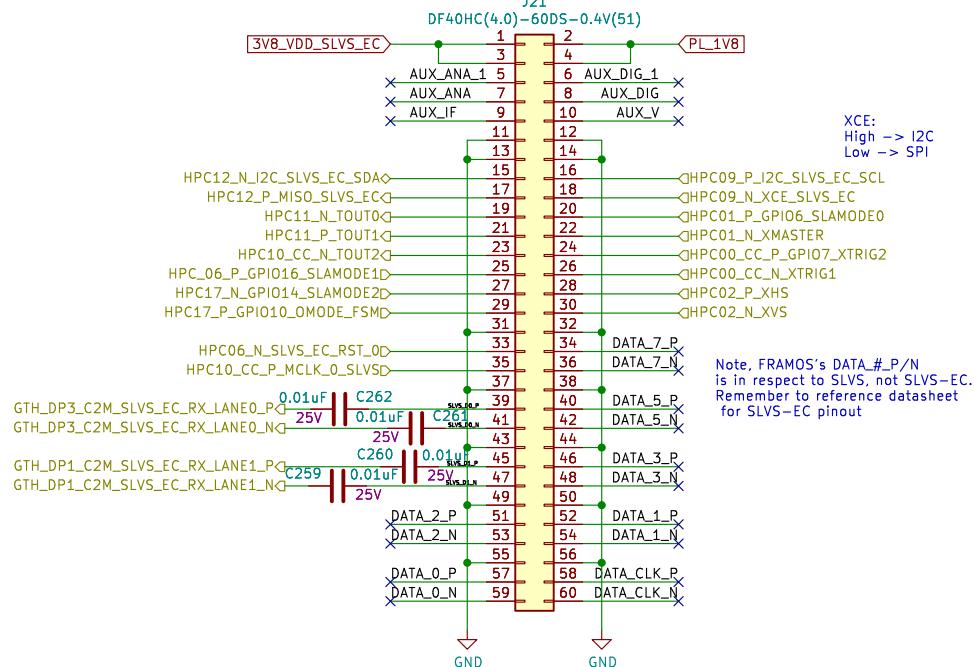
Modified HPC connection



FRAMOS PixelMate(TM) Connector – SLVS-EC

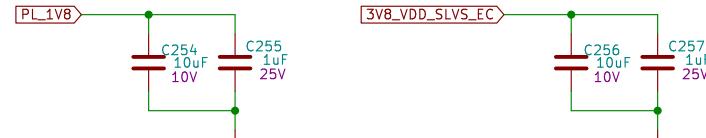
A

FRAMOS PixelMate(TM) Pinout SLVS-EC

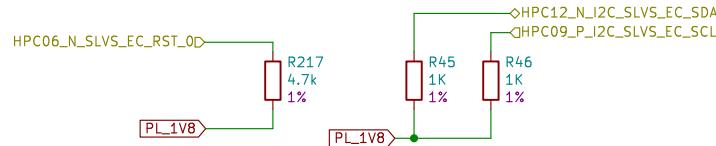


Info about FRAMOS nomenclature:
 FSM: Sensor Module
 FSA: Sensor Module Adapter (has voltage specific for sensor)
 FPA: Processing Board Adapter
 FSA for SLVS-EC is on page 30/62
 (Connector J1 to FPA, which is this board)
 Page 32 includes Amp draw
 3V8VDD has 0.3A draw per pin, max 0.6A
 1V8VDD has 0.3A draw per pin, max 0.6A
 ALL GPIO and connection pins are
 LVCMOS18 (1.8V)
 SLVS-EC has no clock line
 Stands for SLVS- Embedded Clock

Decoupling Caps



Pull up Resistors



Edit -> Have SCK and XCE and SDA pulled to PL 1V8 to allow for I2C or SPI communication
 Pull down MISO so it does not float

Author: Chance Reimer
 SCH: APT-KRIA-FMC
ApotheoTech LLC

Sheet: /FRAMOS PixelMate(TM) Connector – SLVS-EC/
 File: SLVS-EC_FRAMOS.kicad_sch

Title: FRAMOS PixelMate(TM) Connector – SLVS-EC

Size: A4 Date: 2022-01-04
 KiCad E.D.A. kicad (7.0.0)

Rev: 1.00
 Id: 20/20