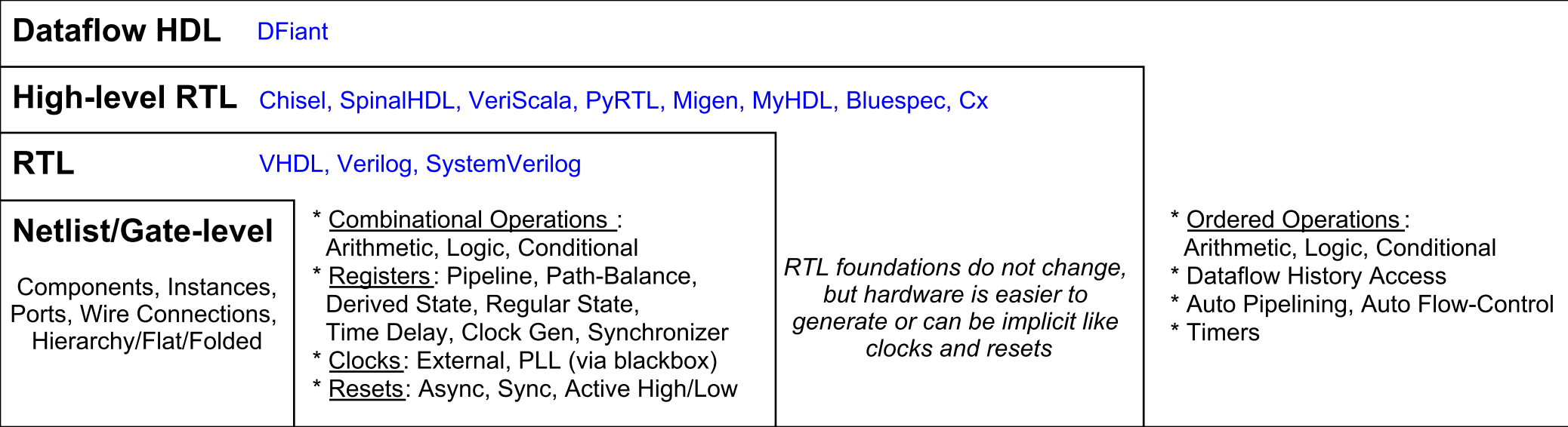
Dataflow HDL
DFiant
High-level RTL
Chisel, SpinalHDL, VeriScala, PyRTL, Migen, MyHDL, Bluespec, Cx
RTL
VHDL, Verilog, SystemVerilog
Netlist/Gate-level
Components, Instances, Ports, Wire Connections, Hierarchy/Flat/Folded
* Combinational Operations : Arithmetic, Logic, Conditional
* Registers: Pipeline, Path-Balance, Derived State, Regular State, Time Delay, Clock Gen, Synchronizer
* Clocks: External, PLL (via blackbox)
* Resets: Async, Sync, Active High/Low
RTL foundations do not change, but hardware is easier to generate or can be implicit like clocks and resets
* Ordered Operations: Arithmetic, Logic, Conditional
* Dataflow History Access
* Auto Pipelining, Auto Flow-Control
* Timers