✘ Bad
✓- Nice
✓ Good
+✓ Very Good

Property Group	Properties	HLS	DF-HDL	HL-RTL	RTL	Comments
		Tools & Languages:	VivadoHLS, LegUp, Catapult, Intel OpenCL, MaxJ,	DFiant	Chisel, SpinalHDL, PyRTL, Migen, MyHDL, Bluespec, Cx	VHDL, Verilog, SystemVerilog
Hardware Design Fundementals	Concurrent Semantics	✓-	✓	✓	✓	
	Bit Accurate Type Safety	✓-	✓+	✓	✓	
	Clear Synthesizability	✘	✓	✓	✘	Legal language syntax, but illegal for synthesis purposes
	IO Ports & Connectivity	✓-	✓+	✓+	✓	
	Hierarchies & Compositions	✓-	✓+	✓+	✓	
	RTL/Netlist Blackbox Interface	✓-	✓	✓	✓	
	Clock and Reset Management	✓-	✓-	✓	✓	
	General Purpose Top-Level Design	✘	✓	✓	✓	
Design Abstraction & Automation	State Abstraction	✓	✓	✘	✘	
	Time Abstraction	✘	✓-	✘	✘	
	Auto-Balanced Manual Pipelining	✓-	✓	✘	✘	
	Automatic Pipelining	✓+	✓	✘	✘	
	Automatic Flow-Control	✓+	✓	✓-	✘	
	Control Loop Pipelining	✓+	✘	✘	✘	
Meta-Programming	Conditional & Looped Generation	✓	✓	✓	✓	
	Recursive Construction	✓-	✓	✓	✘	
	Inheritance/Typeclasses	✘	✓	✓	✘	
	Polymorphic Interfaces	✓-	✓	✓	✓-	
Post-Design Capabilities	Legible RTL Output		✓		✓	
	Simulation	✓	✓-			
	Verification	✓				
	Debugging		✓			
Other Properties	Open Source	✘	✓	✓	✓	
	Maturity	✓	✘	✓-	✓	
	Documentation	✓	✘	✓-	✓	
	Familiar Semantics	✓-	✘	✓-	✓	