Use Case	Design Source	Pipeline Latency [Cyc]	Max Freq. [MHz]	LUTs [#]	FFs [#]	LoC [#]	LoC Reduction [%]	DFiant Pipelining Method	Hardware Proven	Comment
AES Cypher	**DFiant**	38	442	3782	11437	334	64	**Automatic**	**Yes**	Three key widths supported. Compared at 128-bit.
	Hsing Core	21	454	11103	5386	922				
FP Multiplier	**DFiant**	23	354	3733	2246	180	47	**Automatic**	**Yes**	
	Lundgren Core	24	322	3744	1633	340				
Two-Stage RISC-V	**DFiant**	2	117	1345	1025	557	-79	**Manual**	**Yes**	The RTL code registers are inferred differently and are mapped to LUTRAM.
	Samsoniuk Core	2	103	1163	161	311				
CRC	**DFiant**	NA	217	23	17	41	60	**Not Applicable**	**No**	Compared with the parallel CRC module at 16-bit polynomial and 16-bit data input.
	Drange Core	NA	217	23	17	103				
Fibonacci Gen	**DFiant**	NA	339	32	30	8	74	**Not Applicable**	**No**	
	ExampleProblems	NA	339	32	30	31				
Sequence Detector	**DFiant**	NA	567	5	3	32	56	**Not Applicable**	**No**	Change is due different FSM state encoding inference (one-hot or not)
	FPGA4Student	NA	577	6	6	73				
Moving Average 4x4	**DFiant**	2	226	217	299	19	74	**Manual**	**No**	
	Our RTL	2	226	217	299	72				
Bitonic Sort Network	**DFiant**	0	33	3424	0	36	60	**None**	**No**	
	VLSICoding	0	33	3424	0	90				
Priority Encoder	**DFiant**	0	178	154	0	10	52	**None**	**No**	Compared at 128-bit input
	Kaufmann Core	0	178	154	0	21				