Latency Analysis: The no of time gap between the initiation of a pipeline in b/w a particular stage

Forbidden latency: latency which causes collision.
Permissible latency: latency that will not cause collision
Minimal Avg. latency (MAL) : max. diff. w.r.t. pipeline w/o collision.

Collision Vector: combined set of permissable & forbidden latencies.

$C = (C_m, C_{m-1} \ldots C_2 C_1)$

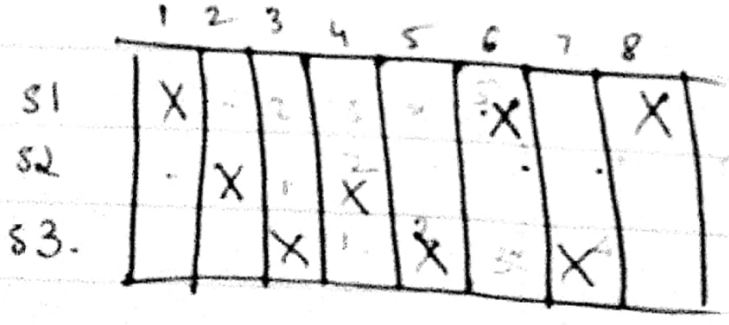
where C_m must always be 1.

M: maximum forbidden latency.

$C_i : 0 \rightarrow$ permissible.

$C_i : 1 \rightarrow$ forbidden.

Find out the permissible & forbidden latency of the reservation table for function x, also design the collision vector and state transition diagram for the collision vector.



2017 MAY

Week 21
145-220
Thursday 25

F.Lx = 5, 7, 2, 4 * (diff. from 1st x to the next in each row)

(Forbidden Latency in terms of x)

PLx = 1, 3, 6, 8

Cx = 1011010 * [Start 4m max. forbidden (7)]

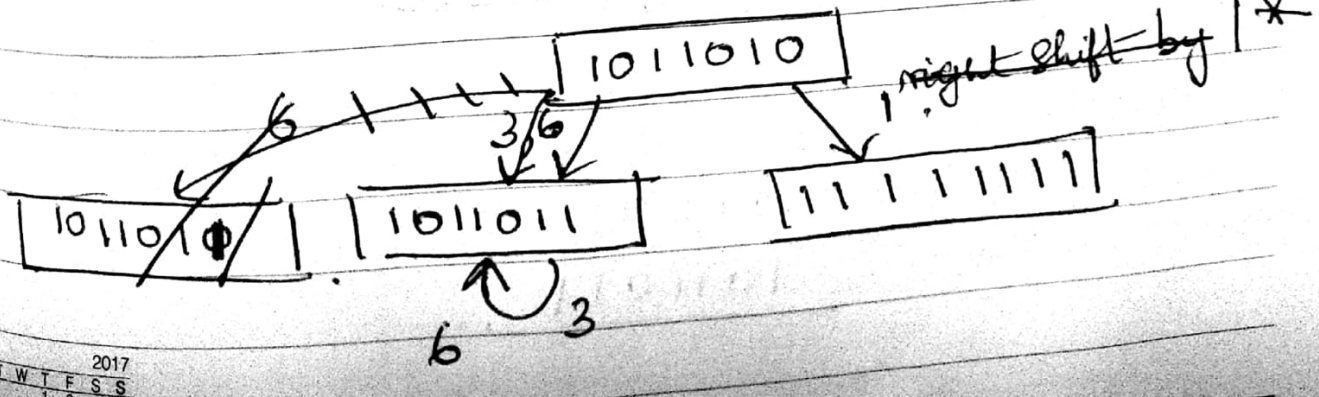
Collision Vector = 6 3 1 → 1011010

* identify positions of 0 and right shift the collision vector acc. to the pos. & preform the OR operation w/ the org. value.

Right shift by 1 : 0101101
(adding 1 zero to left & discarding last one)

OR with

```
  1011010
  0101101
---------
  1111111
```



RS : 00010110
by 3

OR : 1011010
0001011

1011011

RS by 6 : 000000

OR : 1011010
000000
1011011

Now consider (3) — 6 3 1 [1011011]

~~RS by~~

RS by 3 : 0001011
1011011

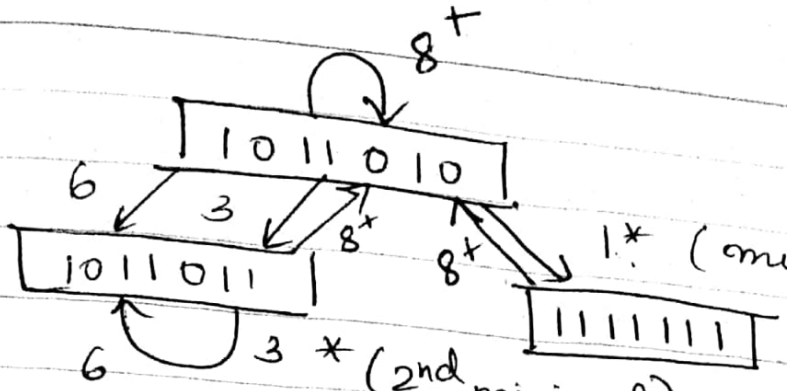
OR : 1011011

RS by 6 : 0000001
1011011

OR 1011011

2017 MAY

Week 21
147-218
Saturday 27



~~① Identify max.~~

② Identify max. forbidden latency, increment by 1 which leads to the same result of collision vector and indicate the digit by the symbol +:

Point towards the org. collision vector with M+1. [7+1 = 8]

no. of digits

Week 21
148-217
Sunday 28

Identify the ~~Symbol~~ simple cycle and greedy cycle.

ones with repitation.

→ Simple Cycle = 3, 6, 8, (1,8) (comb. w/ reverse & forward arrow)
(3,8), (6,8)

~~Greedy Cycle =~~

~~MAL =~~

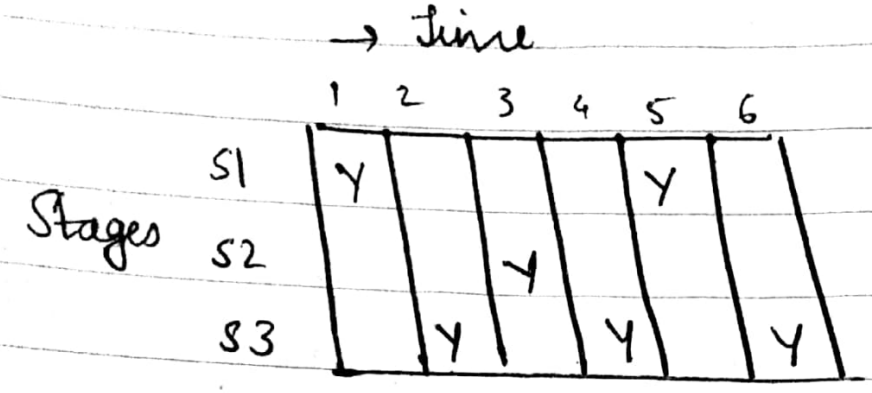
identify minimal latency & groups

→ Greedy Cycle = 3, (1,8)

MAL = 3 // [3 < $\frac{8+1}{2}$]

~~Repositories~~

Identify the collision vector, the state transition diagram & also find out simple cycle, greedy cycle and MAL.



F.L xy = 4, 2

F.L y = 1, 3, 5, 6.

C_y = 1010

4	3	2	1
1	0	1	0

RS by 1 : 0 1 0 1

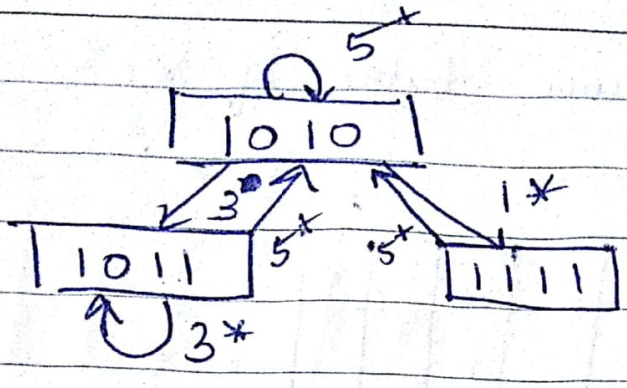
OR : 1 0 1 0

1 1 1 1

RS by 3 : 0 0 0 1

OR : 1 0 1 0

1 0 1 1



3 2 1
1011

RS by 3: 0001
OR: 1010
1011

Max. forbidden latency, M = 4.

M+1 = 5 → leads to the same latency.

Simple cycle = 3, 5 (loops), (1,5), (3,5) (flw & reverse arrows)

↓min ↓min

Greedy cycle = 3, (1,5)

MAL = 3.

Plot the reservation table of X:

	1	2	3	4	5	6	7	8
S1	X					X		X
S2		X		X				
S3			X		X		X	

Consider the functions X, derive the reservation table for latency 2 and latency 5. Identify the stages that are forbidden. Assume that the clock cycle ranges from 1 to 10.

Latency 2 →

	1	2	3	4	5	6	7	8	9	10	11
S1	X_1		X_2		X_3	X_1	X_4	X_1	X_5	X_3	..
S2		X_1		X_1		X_2		X_2		X_4	..
S3		.	X_1	X_2	X_1	X_3	X_2	X_3	X_2	X_5	..
					X_2		X_1	X_4	X_3		..
							X_3	.	X_4		

Latency 5 →

	1	2	3	4	5	6	7	8	9	10	11
S1	X_1					X_2 X_1	.	X_1	.		..
S2		X_1		X_1			X_2	.	X_2		
S3			X_1		X_1	.	X_1	X_2	.	X_2	

2017 JUNE

Week 22
152-213
Thursday

Forbidden latencies :-

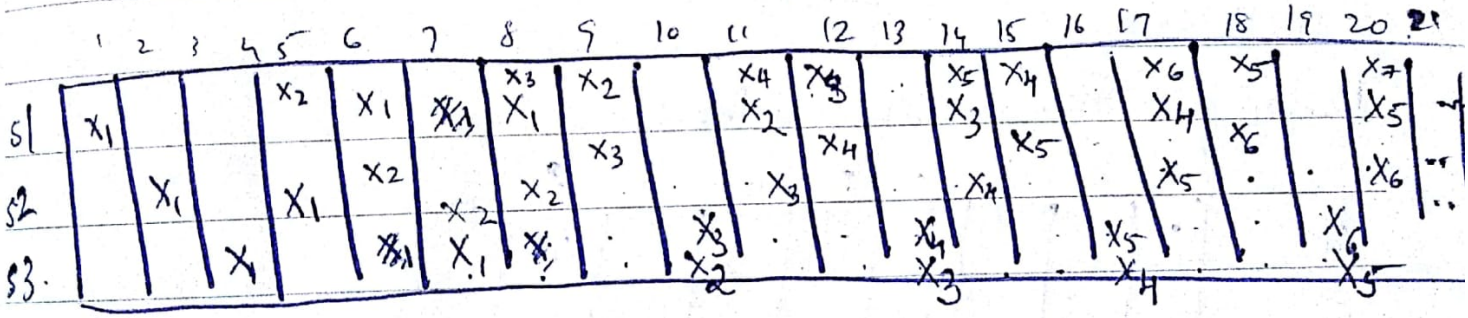
Latency 2 :- X_1 & X_2 will collide for clock cycle 8 at stage 1.

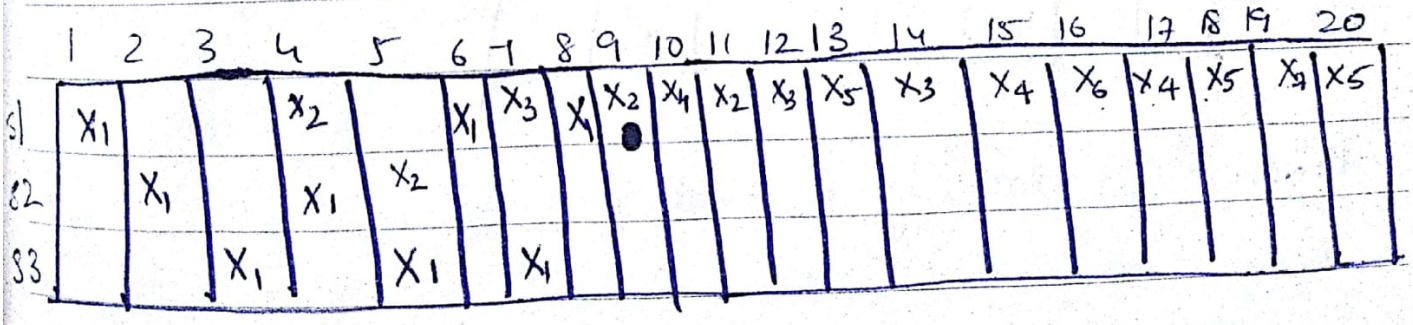
X_2, X_3 and X_4 for clock cycle 9 at stage 3.

Latency 5 :-

Forbidden latency - X_1 and X_2 will collide ~~at~~ at ~~for~~ clock cycle 6 ~~in at~~ stage 1.

Identify the efficiency for the reservation table X mentioned above w.r.t. latency 3, clock cycle 1 to 20., and continues from 21.





JUNE

only 8 are busy out of 9.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
X_1			X_2		X_1	X_3	X_1	X_2	X_4	X_2	X_3	X_5	X_3	X_4	X_6	X_7
	X_1		X_1	X_2		X_2	X_3		X_3	X_4		X_4	X_5		X_5	X_6
		X_1		X_1	X_2	X_1	X_2	X_3	X_2	X_3	X_4	X_3	X_4	X_5	X_4	X_5

Thus a match b/w (7,8,9) | (10,11,12)

$$\text{Efficiency} = \frac{\text{Busy Stage}}{\text{Total Stage}} \times 100.$$

$$\eta = \frac{8}{9} \times 100$$

$$= 88.88.1$$

Deriving Reservation Table:

	1	2	3	4	5	6	7	8
S1	X					X		X
S2		X		X				
S3			X		X		X	

Receive w/ latency 2 and 5.