USN | | | | | | | | | | |

NMAM INSTITUTE OF TECHNOLOGY, NITTE

(An Autonomous Institution affiliated to VTU, Belgaum)

VII Sem B.E. (CSE) Mid Semester Examinations – II October 2012

CS702 – ADVANCED COMPUTER ARCHITECTURE

Duration: 1 Hour | Max. Marks: 20

*Note: Answer any **One** full question from **each Unit.***

Unit – I

1. a) Draw a 3-D hypercube interconnection network and show the static routing based on dimension order. 4

   b) Show the following loop unrolled on a dual issue (1 FP instruction and 1 anything else) superscalar processor, so that there are five copies of the loop body. Also calculate the number of clock cycles required per iteration of the unrolled loop. Assume that the number of loop iterations is a multiple of 5.

```
Loop:   L.D   F0,0(R1)
        ADD.D  F4,F0,F2
        S.D   F4,0(R1)
        SUBI   R1,R1,#8
        BNEZ R1, Loop
```

Consider the following intervening latencies between two dependent instructions:

Instruction producing result	Instruction using result	Latency
FP ALU	FP ALU	3
FP ALU	SD	2
LD	FP ALU	1
LD	SD	0
Int ALU	Branch	1
Int ALU	Int ALU	0

6

2. a) Draw the block diagram of a (2, 2) correlating predictor. 4

   b) In a processor having Tomasulo-based dynamic scheduling and speculation (using ROB) capacity, determine the sequence of clock cycles in which the write-back and commit operations are performed for the following instruction sequence.

	Instruction	Operands
1	DIV	R2, R3, R4
2	MUL	R1, R5, R6
3	ADD	R3, R7, R8
4	MUL	R1, R1, R3
5	SUB	R4, R1, R5
6	ADD	R1, R4, R2

The latencies for the functional units are as follows:

Functional units	Latencies
add	2
multiply	10
divide	40
load	2

The number of load buffers is 2, number of FP add reservation stations is 3, and number of FP multiply reservation stations is 2. 6

P.T.O.

Unit – II

3. a) Briefly explain characteristics of interconnection networks. Distinguish between static and dynamic interconnection networks. 4

   b) If the instructions in the following example code are scheduled dynamically using Tomasulo's algorithm, what are the contents of reservation stations and register tags when all the instruction are issued.

```
L.D  F6, 32(R2)
L.D  F2, 44(R3)
MUL.D F0, F2, F4
SUB.D F8, F2, F6
DIV.D F10, F0, F6
ADD.D F6, F8, F2
```

   The latencies for the functional units and the number of various reservation stations are same as that of question 2(b) 6

4. a) Explain how write-invalidate snoopy protocol achieves data consistency among write-through caches. 5

   b) Giving the structure of Branch Target Buffer compare its operation to that of a branch predictor. 5

****

USN | | | | | | | | | | |

NMAM INSTITUTE OF TECHNOLOGY, NITTE

(An Autonomous Institution affiliated to VTU, Belgaum)

VII Sem B.E. (CSE) Mid Semester Examinations – II, October 2013

CS702 – ADVANCED COMPUTER ARCHITECTURE

ıration: 1 Hour Max. Marks: 20

*Note: Answer any **One** full question from **each Unit.***

Unit – I

a) Give the structure of a floating point processor unit based on extended Tomasulo's algorithm to handle speculation. Briefly explain the four steps involved in the execution of any instruction in this processor. 6

b) Show the following loop unrolled on a dual issue (1 FP instruction and 1 anything else) superscalar processor, so that there are five copies of the loop body. Also calculate the number of clock cycles required per iteration of the unrolled loop. Assume that the number of loop iterations is a multiple of 5.

```
Loop:   L.D   F0,0(R1)
        ADD.D F4,F0,F2
        S.D   F4,0(R1)
        SUBI  R1,R1,#8
        BNEZ R1, Loop
```

Consider the following intervening latencies between two dependent instructions:

Instruction producing result	Instruction using result	Latency
FP ALU	FP ALU	3
FP ALU	SD	2
LD	FP ALU	1
LD	SD	0
Int ALU	Branch	1
Int ALU	Int ALU	0

4

a) With state transition diagram explain the functioning of 2 bit dynamic branch predictor for the inner loop in the following code:

```
for ( i=0;  i<100;  i++ )
  for ( j=0;  j<3;  j++ )
   // whatever code
```

5

b) What is cache coherence problem? What are the causes of cache inconsistency? Explain how cache inconsistency occurs during data sharing. 5

Unit – II

a) Show the contents of reservation stations and register tags for the first 4 clock cycles when the instructions in the following example code are scheduled dynamically using basic Tomasulo's algorithm (without speculation).

```
SUB.D  F8, F2, F6
ADD.D  F6, F8, F2
DIV.D  F10, F0, F6
```

The latencies for the functional units are as follows:

Functional units	Latencies
Add/Sub	2
Multiply	10
Divide	40

The number of FP add reservation stations is 2, and number of FP multiply reservation stations is 1. 5

P.T.O.

b) With block diagram explain the operation of Branch Target Buffer. 5

a) With state transition diagram explain how write-invalidate snoopy protocol achieves data consistency among write-back caches. 6

b) Assuming 8K bits in the branch history table (BHT), calculate the number of entries in the BHT for the following (m,n) predictors:

i) (0,2)
ii) (1,2)
iii) (3,2)
iv) (10,2)

(note : 1K=1024) 4

****

USN | | | | | | | | | | |

NMAM INSTITUTE OF TECHNOLOGY, NITTE

(An Autonomous Institution affiliated to VTU, Belgaum)

VII Sem B.E. (CSE) Mid Semester Examination – II, October 2014

CS702 – ADVANCED COMPUTER ARCHITECTURE

ion: 1 Hour

Max. Marks: 20

*Note: Answer any **One** full question from **each Unit.***

Unit – I

a) Consider the following pipeline reservation table.

	1	2	3	4	5	6	7	8
S1	X					X		X
S2		X		X				
S3			X		X		X	

(a) What are the forbidden latencies?
(b) Draw the state transition diagram.
(c) List all the simple cycles and greedy cycles.
(d) Determine the optimal constant latency cycle and the minimal average latency.
(e) Let the pipeline clock period be τ = 20 ns. Determine the throughput of the pipeline. 10

Describe dynamic scheduling using Tomasulo's approach. 10

Unit – II

What is cache coherence problem? Explain the cache coherence through bus snooping. 10

Describe the three types of cache directory protocols. 10

****

USN

NMAM INSTITUTE OF TECHNOLOGY, NITTE

(An Autonomous Institution affiliated to VTU, Belagavi)

VII Sem B.E. (CSE) Mid Semester Examinations - II, October 2015

12CS702 – ADVANCED COMPUTER ARCHITECTURE

Duration: 1 Hour

Max. Marks: 20

*Note: Answer any **One** full question from **each Unit.***

Unit – I

			Marks	BT*
1.	a)	Unroll the following loop such a way that there are two copies of the loop body. Assume that the number of loop iterations in the given loop is multiple of 2.		

```
Loop:  L.D   F0,0(R1)
       ADD.D F4,F0,F2
       S.D   F4,0(R1)
       SUBI  R1,R1,#8
       BNEZ R1, Loop
```

Given- The intervening latencies between two dependent instructions is as follows:

Instruction producing result	Instruction using result	Latency		
FP ALU op	FP ALU op	3		
FP ALU op	SD	2		
LD	FP ALU op	1		
LD	SD	0		
Int ALU op	Branch	1		
Int ALU op	Int ALU op	0	05	L5

b) Considering the branch of the inner loop in the following code, discuss the working of 2-bit dynamic branch predictor with a state diagram.

```
for ( i=0;  i<100;  i++ )
  for ( j=0;  j<3;  j++ )
      // whatever code
```

05 L4

2. a) Assume that the following instructions are executed on a processor having Tomasulo-based dynamic scheduling and speculation (using ROB) capacity. Determine the sequence of clock cycles in which the write-back and commit operations are performed for the following instruction sequence.

```
ADD.D  F8, F2, F6
MULT.D F10, F0, F6
SUB.D  F6, F8, F2
MULT.D F6, F10, F6
```

Given-: latencies of the functional units are as follows:

Functional units	Latencies
Add/Sub	2
Multiply	10
Divide	40

The number of FP add reservation stations is 2, and number of FP multiply reservation stations is 2. Assume that there are enough entries in ROB. 06 L5

P.T.O.

b) Assuming 8K bits in the branch history table (BHT), calculate the number of entries in the BHT for the following (m,n) predictors
For the following (m,n) predictors, how many entries will be in the branch history table (BHT) of 8K bits:
i) (0,2)
ii) (12,1) 04 L5

Unit – II

3. a) With the block diagram of Tomasulo based Floating point unit, explain the steps of instruction execution. 06 L2

b) Explain how Branch Target Buffer increases the instruction fetch bandwidth. 04 L2

4. a) Show the following loop unrolled on a **dual issue** (1 FP instruction and 1 anything else) superscalar processor, so that there are five copies of the loop body. Also calculate the number of clock cycles required per iteration of the unrolled loop. Assume that the number of loop iterations is a multiple of 5.

```
Loop:  L.D   F0,0(R1)
       ADD.D  F4,F0,F2
       S.D   F4,0(R1)
       SUBI   R1,R1,#8
       BNEZ R1, Loop
```

The intervening latencies between two dependent instructions are same as that of question 1 (a). 6 L5

b) What do you mean by a hazard? Explain the three types of data hazards. 4 L1

BT* Bloom's Taxonomy, L* Level

****

USN | | | | | | | | | | |

NMAM INSTITUTE OF TECHNOLOGY, NITTE

(An Autonomous Institution affiliated to VTU, Belagavi)

VII Sem B.E. (CSE) Mid Semester Examinations - II, October, 2017

14CS702 – ADVANCED COMPUTER ARCHITECTURE

uration: 1 Hour

Max. Marks: 20

*Note: Answer any **One** full question from **each Unit.***

			Marks	BT*
		Unit – I		
1.	a)	Explain the basic structure of MIPS floating point using Tomasulos Algorithm.	06	L*2
	b)	What is branch target buffer? Design and explain the steps involved in handling an instruction with branch target buffer.	04	L6
2.	a)	Define ILP. Explain control Dependences with examples.	04	L1
	b)	For the following instructions, using Dynamic Scheduling determine the status of R.O.B , Reservation station when only MUL.D is ready to go to commit. Two Load instructions are already committed. Assume latencies load 1 clock, add is 2 clock cycles, multiply is 6 clock cycles, and divide is 12 clock cycles. L.D F6,32(R2) L.D F2,44(R3) MUL.D F0,F2,F4 SUB.D F8,F6,F2 DIV.D F10,F0,F6 ADD.D F6,F8,F2 Number of FP add reservation stations is 2 and number of FP multiply reservation stations is 2.	06	L5
		Unit – II		
3.	a)	What is cache coherence? Explain various cache coherence problem types and solution in detail with examples.	06	L4
	b)	Compare static and dynamic data flow.	04	L2
4.	a)	Identify the various static connection networks and construct their topologies in terms of network parameters. (Explain any Six).	06	L3
	b)	Describe the ETL EM- 4 dataflow architecture with neat diagram.	04	L6

T* Bloom's Taxonomy, L* Level

****

USN | | | | | | | | | | |

NMAM INSTITUTE OF TECHNOLOGY, NITTE

(An Autonomous Institution affiliated to VTU, Belagavi)

VII Sem B.E. (CSE) Mid Semester Examinations - II, October 2016

13CS702 – ADVANCED COMPUTER ARCHITECTURE

ation: 1 Hour

Max. Marks: 20

*Note: Answer any **One** full question from **each Unit.***

Unit – I

		Marks	BT*
a)	Explain how Instruction Level Parallelism (ILP) is exploited through Dynamic Scheduling of Instructions in case of Tomasulo's Algorithm with a neat block diagram?	06	L*5
b)	Comment on the problem of Branch Prediction encountered during instruction execution through pipelining? How the problem is resolved through the use of Brach-Target Buffer?	04	L4
2. a)	With a neat diagram explain how Instruction Level Parallelism (ILP) is exploited through Dynamic Scheduling of Instructions by using the ReOrder Buffer (ROB)?	06	L5
b)	Explain the concept of Loop Unrolling with an example?	04	L4

UNIT- II

3. a)	Define Cache Coherence Problem? Explain the different ways (scenarios) in which the cache data becomes inconsistent?	06	L3
b)	Write a note on perfect shuffle and exchange and hyper cube routing function.	04	L2
4. a)	What is the motive behind Snoopy Bus Protocols? Explain Write-Through Cache and Write-Back Cache Protocols with transition diagrams?	06	L3
b)	Explain any two dynamic connection networks.	04	L1

BT* Bloom's Taxonomy, L* Level

****