USN | | | | | | | | | | |

NMAM INSTITUTE OF TECHNOLOGY, NITTE

(An Autonomous Institution affiliated to VTU, Belgaum)

VII Sem B.E. (CSE) Mid Semester Examinations – I September 2012

CS702 – ADVANCED COMPUTER ARCHITECTURE

Duration: 1 Hour | Max. Marks: 20

*Note: Answer any **One** full question from **each Unit.***

Unit – I

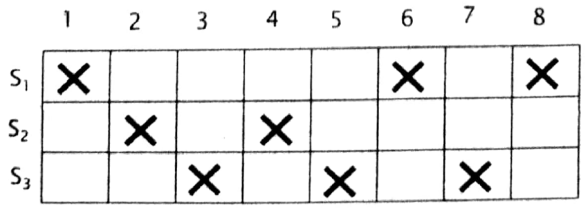
1. a) Explain briefly the SPEC benchmarks. Explain how SPEC ratio is calculated? 5
   b) State and explain Amdhal's law. Derive an expression for overall speedup of a computer? 5

2. a) Explain with diagram how parallel architectures are classified according to Flynn's classification. Give examples for each type of architecture. 5
   b) In a graphics processor, suppose FP square root (FPSQR) is responsible for 20% of the execution time of a critical graphics benchmark. To achieve speedup, one proposal is to enhance the FPSQR hardware and speed up this operation by a factor of 10. The other alternative is just to try to make all FP instructions in the graphics processor run faster by a factor of 1.6; FP instructions are responsible for half of the execution time for the application. The design team believes that they can make all FP instructions run 1.6 times faster with the same effort as required for the fast square root. Compare these two design alternatives and state which one is better. 5

Unit – II

3. a) With block diagram explain the MIPS pipeline clearly specifying the operations performed on each stage of the pipeline. 6
   b) Suppose that data references constitute 40% of the mix, and that the ideal CPI of the pipelined processor, ignoring the structural hazard, is 1. Assume that the processor with the structural hazard has a clock rate that is 1.05 times higher than the clock rate of the processor without the hazard. Disregarding any other performance losses, is the pipeline with or without the structural hazard faster, and by how much? 4

4. a) What do you mean by pipeline Hazard? Explain data hazard and control hazards in a 5 stage pipeline? 5
   b) For the following reservation table of a nonlinear pipeline find the minimal average latency (MAL) for a collision free scheduling.



5

****

USN | | | | | | | | | | |

NMAM INSTITUTE OF TECHNOLOGY, NITTE

(An Autonomous Institution affiliated to VTU, Belgaum)

VII Sem B.E. (CSE) Mid Semester Examinations – I, September 2013

CS702 – ADVANCED COMPUTER ARCHITECTURE

uration: 1 Hour Max. Marks: 20

*Note: Answer any **One** full question from **each Unit.***

Unit – I

1. a) With block diagrams explain the shared memory multiprocessor architectures. 5
   b) What is the significance of benchmark programs? Explain briefly the SPEC benchmarks. Explain how SPEC ratio is calculated? 5

2. a) Based on Amdahl's law mention the factor that affects speedup of processor and derive an expression for overall speedup of a computer? 5
   b) Suppose we have made the following measurements on a processor:
   Frequency of FP operations =25%
   Average CPI of FP operations =4.0
   Average CPI of other instructions = 1.33
   Frequency of FPSQR operations=2%
   CPI of FPSQR operations =20
   There are two design alternatives to increase the performance. The first one is to decrease the CPI of FPSQR to 2. The other alternative is to decrease the average CPI of all FP operations to 2.5. Compare these two design alternatives using the processor performance equation. 5

Unit – II

3. a) Explain with block diagram how R,I,J type of instructions are executed on a MIPS pipeline. 6
   b) For the following reservation table of a nonlinear pipeline find the minimal average latency (MAL) for a collision free scheduling.

	1	2	3	4
S1	X			X
S2		X		
S3			X	

4

4. a) Explain data hazard with an example. Show how data forwarding can be used to overcome the data hazard. 5
   b) Suppose that data references constitute 40% of the mix, and that the ideal CPI of the pipelined processor, ignoring the structural hazard, is 1. Assume that the processor with the structural hazard has a clock rate that is 1.05 times higher than the clock rate of the processor without the hazard. Disregarding any other performance losses, is the pipeline with or without the structural hazard faster, and by how much? 5

****

USN | | | | | | | | | | |

NMAM INSTITUTE OF TECHNOLOGY, NITTE

(An Autonomous Institution affiliated to VTU, Belgaum)

VII Sem B.E. (CSE) Mid Semester Examinations – I, September 2014

CS702 – ADVANCED COMPUTER ARCHITECTURE

on: 1 Hour | Max. Marks: 20

*Note: Answer any **One** full question from **each Unit.***

Unit – I

a) Explain Amdahl's law 6

b) Consider a web servicing technique. The new processor is 10 times faster on computation in the web servicing application than the original processor. Assuming that the original processor is busy with computation 40 % of the time and is waiting for I/O 60% of the time. What is the overall speed up gained by incorporating the enhancement? 4

a) Explain process performance equation 4

b) Shared memory multiprocessor uses various models.Explain 6

Unit – II

Draw and explain the five stages of pipeline using pipeline registers 10

a) How to minimize data hazards 6

b) How an instruction flows through the data path for unpipeline MIPS 4

****

(An Autonomous Institution affiliated to VTU, Belagavi)

VII Sem B.E. (CSE) Mid Semester Examinations - I, September 2015

12CS702 – ADVANCED COMPUTER ARCHITECTURE

Duration: 1 Hour

Max. Marks: 20

*Note: Answer any **One** full question from **each Unit.***

Unit – I

			Marks	BT*
1.	a)	Define and explain Amdahl's law	06	L*2
	b)	Suppose we have made the following measurements: *Frequency of Floating point(FP) operations = 25%* *Average CPI of FP operations = 4.0* *Average CPI of other instructions = 1.33* *Frequency of Floating Point Square Root(FPSQR) = 2%* *CPI of FPSQR = 20* The two design alternatives are to decrease the CPI of FPSQR to 2 or decrease the average CPI of all FP operations to 2.5. Compare FP and FPSQR design alternatives using processor performance equation	04	L4
2.	a)	Explain various shared memory multi processor models with neat diagram	06	L2
	b)	Suppose you are on the design team for a new processor. The clock runs at 200 Mhz. we assume that the processor only executes one instruction at a time. The following table gives instruction frequencies for SPEC Benchmark S_B.		

Instruction Type	Frequency	Cycles
Load and Store	30%	6 Cycles
Arithmetic instructions	50%	4 Cycles
All others	20%	3 Cycles

(i) Calculate average clock cycles per instruction.
(ii) Determine the native MIPS processor speed for the benchmark in millions of instructions per second? 04 L5

Unit – II

3.	a)	Define Pipelining. Explain the simple implementation of MIPS data path.	06	L2
	b)	Analyze the following instructions and justify whether data hazard can be overcome using forwarding technique. **LD** R1, 0(R2) **DSUB** R4, R1, R5 **AND** R6, R1, R7 **OR** R8, R1, R9	04	L4

P.T.O.

4. Consider the following pipeline reservation table.

	1	2	3	4	5	6	7	8
S1	X					X		X
S2		X		X				
S3			X		X		X	

(a) What are the forbidden latencies?
(b) Draw the state transition diagram.
(c) List all the simple cycles and greedy cycles.
(d) Determine the optimal constant latency cycle and the minimal average latency.
(e) Let the pipeline clock period be τ = 20 ns. Determine the throughput of the pipeline.

10

BT* Bloom's Taxonomy, L* Level

****

USN | | | | | | | | | | |

NMAM INSTITUTE OF TECHNOLOGY, NITTE

(An Autonomous Institution affiliated to VTU, Belagavi)

VII Sem B.E. (CSE) Mid Semester Examinations - I, September 2017

14CS702 – ADVANCED COMPUTER ARCHITECTURE

Duration: 1 Hour | Max. Marks: 20

Note: Answer any One full question from each Unit.

			Marks	BT*
		Unit – I		
1.	a)	State Amdahl's law. Explain the CPU Performance Equation.	6	L*2
	b)	Differentiate between concurrent and parallel execution.	4	L5
2.	a)	Explain shared memory multiprocessors.	6	L4
	b)	Define benchmarks Identify its types and give examples.	4	L1
		Unit – II		
3.	a)	Consider the three-stage pipelined processor specified by the following reservation table.		

	1	2	3	4	5	6	7	8
S_1	X					X		X
S_2		X		X				
S_3			X		X		X	

1. List all the set of forbidden latencies and collision vector.
2. Design a state transition diagram.
3. List all the simple cycles and greedy cycles
4. What is the minimum average latency (MAL) of this pipeline?

	b)	What are Hazards? List its types.	2	L1
4.	a)	Explain Classic Five stages pipeline for MIPS with neat diagram.	7	L4
	b)	Compare Linear and non linear pipeline processors.	3	L3

BT* Bloom's Taxonomy, L* Level

****

USN | | | | | | | | | | |

NMAM INSTITUTE OF TECHNOLOGY, NITTE

(An Autonomous Institution affiliated to VTU, Belagavi)

VII Sem B.E. (CSE) Mid Semester Examinations - I, September 2016

13CS702 – ADVANCED COMPUTER ARCHITECTURE

Duration: 1 Hour | Max. Marks: 20

*Note: Answer any **One** full question from **each Unit.***

			Marks	BT*
		Unit – I		
1.	a)	State Amdahl`s law and derive expression for the speedup.	05	L*5
	b)	Following measurements are made : Frequency of Floating point(FP) operations = 25% Average CPI of FP operations = 4.0 Average CPI of other instructions = 1.33 Frequency of Floating Point Square Root(FPSQR) = 2% CPI of FPSQR = 20 Assume that the two design alternatives are to decrease the CPI of FPSQR to 2 or decrease the average CPI of all FP operations to 2.5. Compare FP and FPSQR design alternatives using processor performance equation.	05	L5
2.	a)	Briefly explain the concept of concurrent and parallel execution.	02	L2
	b)	Discuss various shared memory multiprocessor system models and distributed memory multicomputers with neat diagram.	08	L6
		UNIT- II		
3.	a)	With the neat diagram analyze the execution of an instruction on MIPS data path.	05	L2
	b)	An unpipelined processor takes 6 ns to work on one instruction. The pipelined version of the processor has 6 stages with the following lengths: 1.0ns; 0.8ns; 0.4ns; 1.2ns; 1.3ns; 1.3ns. It then takes 0.3 ns to latch its results into latches. Answer the following, assuming that there are no stalls in the pipeline. 1. What are the cycle times in both processors? 2. How long does it take (in nano-seconds) to finish one instruction in both processors? (Note : Ignore the initial fill time in the pipelined processor) 3. What is the speedup achieved by the 6 stage pipeline with respect to unpipelined processor? 4) How long does it take (in nano-seconds) to finish 1000 instructions in both processors? (Note : Do not ignore the initial fill time in the pipelined processor)	05	L3

4 a) Consider the following pipeline reservation table.

S1	X					X		
S2		X		X				X
S3			X		X		X	

(a) What are the forbidden latencies?
(b) Draw the state transition diagram.
(c) List all the simple cycles and greedy cycles.
(d) Determine the minimal average latency.
(e) Find the efficiency of the pipeline

6 L3

b) What do you mean by a control hazard? How we can overcome from control hazards by filling the delay slot? 4 L1

3T* Bloom's Taxonomy, L* Level

****