

# CARTE DE PUISSANCE EUROBOT 2017

Date et signature de l'étudiant :		

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13018	9 mai 2016	2016/2017	1/2

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## INTRODUCTION

Dans le cadre du projet Eurobot, une nouvelle carte de puissance a été élaborée afin de fournir les différents consommateurs électriques. Ce document reprend l'analyse des besoins en tension et courant, le choix et la justification des différentes topologies ainsi que le détail des différents calculs. Enfin nous aborderons la mise en œuvre du PCB en lui-même.

Le développement et la fabrication de cette carte devra prendre en compte, la simplicité d'implémentation, une certaine modularité, une taille réduite et surtout un faible prix.

Ce document devra être lu en parallèle avec les datasheet des différents modules car le but n'est bien sur pas de les recopier mais de les clarifier et les appliquer à nos besoins. Une fois que les concepts de base sont compris, ces datasheet peuvent vraiment être utilisées comme des recettes de cuisine.

## ETUDE DES BESOINS

Le robot est uniquement alimenté par une batterie au Lithium de 19,8V capable de fournir plusieurs Ampères. Les différents modules électroniques sur le robot sont de multiple Arduino, une Raspberry-Pi, une DE0-nano, tous nécessitant de 5V et des capteurs demandant du 3.3V. Soit les deux tensions logiques de base. Une Raspberry-Pi pouvant nécessiter jusqu'à 2 Ampères. Les autres consommateurs sont généralement peu gourmand, mais leur nombre sur le bus peut très vite monter.

Ensuite il faut pouvoir alimenter deux moteurs en 24V pouvant tirer jusque 1A chacun.

Certains groupes doivent pouvoir alimenter deux moteurs 12V de 2A chacun.

Enfin, les Dynamixel qui peuvent vite être multipliés sur un robot peuvent tirer jusqu'à 1A chacun et demande une tension de 9,5V.

Dès le début, il a été décidé de placer deux modules de 5v sur la carte où l'un sera muni de deux connecteurs USB type A.

## CHOIX DES TOPOLOGIES

En raison d'une certaine expérience avec les régulateurs de chez Texas Instrument, les différents modules de la carte seront basés sur de IC de la famille TPS. Cela relève totalement d'un choix personnel, d'autres fabricants existent sur le marché. Bien que TI soit de bonne réputation et je trouve, fournit des datasheet très complètes.

Le lien suivant est un moteur de recherche permettant de choisir le régulateur le mieux adapté selon vos critères.

<http://www.ti.com/lscds/ti/power-management/non-isolated-dc-dc-switching-regulator-overview.page>

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Un luxe aurait été d'avoir une fonction d'indication « power good » mais cela renvoyait directement vers des régulateurs plus complexes. Tous les régulateurs sont par ailleurs munis d'un enable.

Le dernier critère essentiel était évidemment la disponibilité sur Farrell.

Pour le 12v et le 9.5v on se situe dans la même catégorie de consommateurs, plutôt costauds donc on part plus sur une gamme de 5A. La recherche renvoi vers le TPS54531 dont la datasheet se trouve en annexe 1. Celui-ci est doté du slow-start (ss) requis, d'une fonction UVLO (under voltage lock out), une fréquence de découpage fixe de 570 kHz et surtout un réseau de compensation externe. Ce dernier ajoutant à la complexité d'implémentation.

En soit ce même composant aurait très bien pu servir pour les bus 5v et 3.3v. Cependant, ne nécessitant pas les mêmes puissances et ce dernier étant assez complexe à implémenter, J'ai préférer partir sur le TPS54339. Pouvant monter jusque 3A, celui-ci est moins cher et moins complexe car ne demande de réseau de compensation externe pour sa boucle de régulation. N'oublions pas aussi que plus le rating en courant d'une inductance est grand plus sa taille (à une fréquence fixe) et son prix augmentent. Le TPS54339 possède une fonction de slow start et une fréquence de découpage fixe de 600kHz.

Nous en arrivons enfin aux 24v. Ici nous partons évidemment sur un boost. La recherche sur le lien ci-dessus nous renvoi vers un TSP55340 capable de monter jusque 5A, mais nous dimensionnerons le notre pour 3A. Ce composant nécessite un réseau de compensation externe et une résistance pour fixer sa fréquence de découpage.

Il est bon de noter qu'aucun des modules ne devra être muni d'un fusible car tous ces régulateurs sont dotés de protections en surcharge et en sur-température où ils coupent leurs sorties jusqu'à ce que la situation soit rétablie. En cas de sur-température, la sortie aura tendance à osciller. En effet, si la température est trop importante, la sortie sera désactivée, la température va chuter, réactivant la sortie au passage donc le composant resurchauffera et ainsi de suite.

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## IMPLÉMENTATIONS

Nous allons voir à présent dans le détail comment dimensionner les différents composants nécessaires au bon fonctionnement de chaque module. C'est ici que de bonnes datasheet sont importantes. Texas Instrument donne la marche à suivre pour dimensionner convenablement chaque circuit tout en donnant des exemples. De plus TI fournit des outils (spreadsheet Excel) pour faciliter les calculs. Ceci sera très utile pour le dimensionnement du compensateur du boost.

### TPS54339

Commençons par le plus facile des trois afin d'établir les concepts de base. Le schéma ci-dessous reprend la configuration de base pour faire fonctionner le régulateur. En plus d'être simple, TI fournit dans la datasheet un tableau donnant les valeurs des composants à utiliser en fonction de la tension de sortie désirée. Ceci diminuant la charge en calculs.

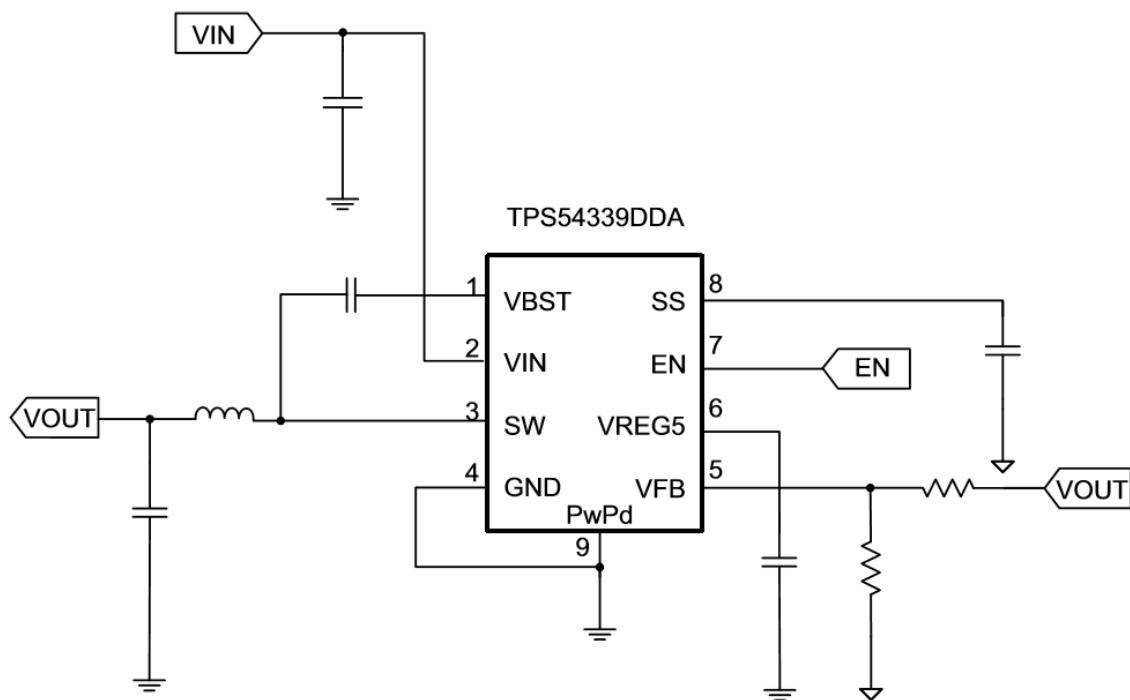


Figure 1 : schéma de base pour le TPS54339

### FEEDBACK

Pour maintenir la tension de sortie stable, le régulateur doit en permanence la comparer à sa tension de référence de 0.765V. La première chose à faire est donc de dimensionner le diviseur de tension entre Vout et VFB.

$$V_{out} = 0,765 \left(1 + \frac{R_{top}}{R_{bottom}}\right)$$

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On choisira des résistances de la série E96. Comme seul le rapport entre Rtop et Rbottom importe dans l'équation, on choisira pour obtenir 3.3v :

Rtop = 73.2K et Rbottom = 22.1K

Pour Vout = 5v on choisi

Rtop = 124K et Rbottom = 22.1K

Ce choix permet d'économiser une commande Farnell car les deux modules utilisent une même valeur de résistance.

## FILTRE LC

Il faut ensuite dimensionner le filtre LC qui redresse la tension. Une fois de plus la datasheet est gentille et nous donne des valeurs adaptées en fonction de la tension de sortie afin d'avoir une bande passante et une stabilité idéales.

Pour Vout = 3,3V on choisira donc d'après le tableau une inductance de 3.3 $\mu$ H et 2 fois 22 $\mu$ F comme capacité de sortie. Il nous reste à déterminer lesquelles.

Commençons par les condensateurs. L'idéale est d'avoir le moins de résistances équivalente possible. Les électrolytiques sont donc à bannir ! Et à relativement faible cout donc les tantalés aussi. On choisira donc des céramiques multicouches en 16V. Par soucis de prix on choisira des Multicomp.

Pour l'inductance il faut déterminer le courant de crête pour la saturation magnétique ainsi que le courant RMS pour l'échauffement. Les équations sont données dans la datasheet. Mais comprenons-les un peu.

On sait que  $U = L \frac{di}{dt}$  Or le courant dans la self est triangulaire, donc la variation de I (di) sur un temps de charge (dt) nous donne le courant crête à crête. dt vaut donc le rapport cyclique  $\alpha$  fois la période.  $dt = \frac{\alpha}{F_{sw}}$  on remetant ça dans la première équation et en sachant que  $\alpha = \frac{V_{out}}{V_{in}}$  et que  $Ul = V_{in} - V_{out}$  lors de sa charge, on obtient :  $I_{pp} = \frac{V_{out}}{V_{in}} \cdot \frac{V_{in} - V_{out}}{L \cdot F_{sw}} = 1.4A$

Le courant de crête vaut donc le courant moyen (3A) plus la moitié de l'amplitude de l'oscillation du courant soit 3,7A.

Pour le courant RMS max il faut faire un peu de géométrie pour déterminer l'aire sous la courbe qui est triangulaire et dont la fréquence est fixe. Le rapport cyclique n'intervient pas vu que l'aire d'un triangle vaut la moitié de la base fois la hauteur.  $I_{rms} = \sqrt{I^2 + \frac{1}{12} I_{pp}^2} = 3,03A$

Une recherche Farnell nous pointe vers une self de chez TDK ref : CLF7045NIT-3R3N-D.

Pour la version 5V on applique le raisonnement. On choisira donc 2 fois 22 $\mu$ F en 16V céramique multicouche pour les condensateurs. Pour la self on calcul 3,53A en courant de crête et 3,02A RMS, on choisira donc une TDK ref CLF7045NIT-4R7N-D. Cette dernière a le même footprint que la précédente ce qui permet de dessiner qu'un seul module, le copier et il suffit de changer les valeurs de composants en fonction de la tension souhaitée.

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N.B. On utilisera toujours pour ce circuit des condensateurs céramiques multicouches. En mettre plusieurs en parallèle plutôt qu'une seule plus grosse à pour avantage de couter moins chère et surtout, l'ESR est divisée par le nombre de capas en parallèle. Le seul inconvénient est l'encombrement.

## CONDENSATEUR ENTRÉE

Idéalement chaque module devrait se sentir seul sur le bus principal de la batterie. Ceci veut dire que pour un module, les transitoires des voisins ne devraient pas perturber sa tension en entrée. Mais aussi que chaque module devrait avoir une émission la plus faible possible pour venir polluer le moins possible le bus avec leur crasse à 600kHz. Pour cela, il faudrait un filtre LC amorti en entrée, ce qui demande beaucoup de calculs et plus de composants. On se contentera de mettre 2 fois 10µF 35V (attention la tension est plus élevée vu qu'on est sur le bus 19,8v) et une capa de 100nF 35v de découplage. Celle-ci devra donc être placée le plus proche possible du régulateur !!! On peut déjà dire que tous les modules auront les mêmes valeurs capa d'entrée et de découplage.

## SLOW START

Nous parlions plus haut du "slow start", il est indispensable que la tension en sortie du régulateur soit levée progressivement au démarrage. Avec un peu de notion d'automatique, on comprend bien que si on impose une consigne avec un échelon, on risque de partir en oscillation.

Ce démarrage lent est contrôlé par un condensateur externe chargé avec une source de courant pour faire monter la tension de référence. On veut que tous les modules démarrent en 10ms. La datasheet donne un courant de charge de 6µA.  $I.t = u.C$  donc  $C = I.t / Vref = 78nF$  on choisira 82nF.

## DIVERS

Il faut encore une capa pour le bootstrap (dont le fonctionnement est supposé compris par le lecteur). 100nF est une valeur adaptée et à pour bonus d'être identique aux capas de découplage.

La datasheet demande également de placer une capa de 470µF pour la tension interne de 5V. Ce qu'on fera, mais cela veut dire qu'on a accès à cette tension interne de régulation. On peut peut-être s'en servir pour donner une information de "power-good". Juste pour essayer j'ai décidé d'ajouter une LED tout en évitant de pomper trop de courant. Un transistor bipolaire à grand gain est donc utilisé, le BC846-7-F ( $hFE = 330$ ).

L'enable sera abordé plus tard dans ce document.

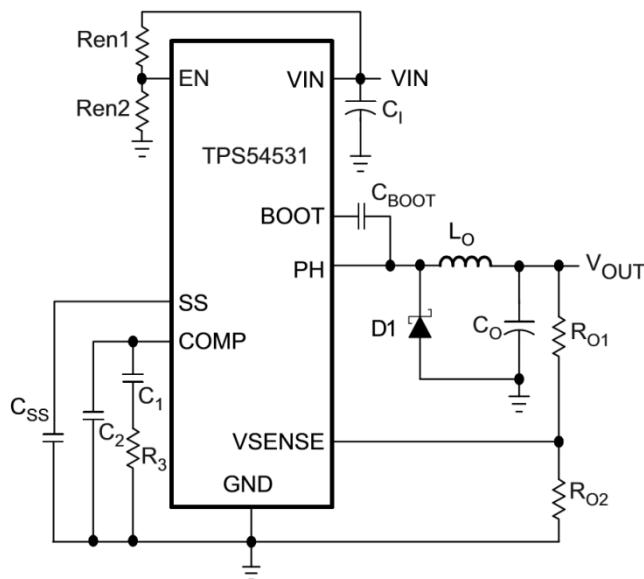
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## TPS54531

Maintenant qu'on à vu les bases du dimensionnement d'un tel circuit, on peut attaquer un plus gros morceau. Le TPS54531 sera utilisé pour réguler le 9,5V ainsi que le 12V et peut monter jusqu'à 5A. On peut déjà dire un mot la dessus, cela représente 60 watts de charge maximale. La datasheet donne un rendement autour des 90%. Ce qui paraît génial ! Mais si on fait vite un calcul sans rentrer dans les détails cela représente environ 6W dissipés par le régulateur dans un boîtier SOIC-8 !

Ci dessous on retrouve le schéma de base qu'il faut pour faire fonctionner le régulateur.



## BASES

On reconnaît déjà certaines choses. Comme La capa d'entrée, on l'a dit dans le chapitre précédent on choisi 2 fois 10µF et 100nF de découplage. On choisi également 100nF pour le bootstrap.

La capa de slow start est chargé avec 2µA jusque 0.8V donc on prendra 22nF.

Pour le pont diviseur, la datasheet propose de mettre 10K pour Rtop pour des raisons de gain du régulateur. Ce qui fait comme valeur pour Rbottom sachant que Vref = 0.8V :

Version 12V → 714,3 ohm

Version 9,5V → 919,6 ohm

## LC DE SORTIE

Pas de tableau prémâché cette fois. Il faut calculer la valeur minimale de la self de manière à éviter de tomber en régime lacunaire. L'équation donnée dans la datasheet est aussi basée sur

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$U = L \frac{di}{dt}$  comme pour le calcul de courant crête à crête sauf que cette fois l'inconnue est  $L$ . comme  $i$  est pas connu, TI défini un indice de ripple (Kind) entre le courant de sortie et la valeur crête à crête. Typiquement Kind est pris à 0,3.

Une fois qu'on a obtenu une valeur d'inductance, on peut calculer les vrais courants de crête et RMS avec les mêmes équations qu'au chapitre précédent. A la seule différence qu'ici, TI prend en compte un facteur de rendement un peu "worst case" pour avoir une marge de sécurité.

On calcule donc pour la version 12V, 5,6 $\mu$ H avec 5,03A RMS et 5,94A en crête. Ce qui nous dirige vers une Bourns ref : SRP6540 5R6M. La même convient pour la version 9,5V.

Il faut également calculer la valeur de la capa de sortie. On ne s'attardera pas là-dessus car les équations sont dans la datasheet, mais il faut savoir qu'il y a deux critères de sélection et il faut choisir le plus contraignant. Le premier est sur les transitoires de courant. Plus le transitoire est important, plus la capacité doit être grande pour garantir une chute de tension la plus faible possible. Le deuxième est sur l'oscillation résiduelle de la tension de sortie. Si la capa est trop faible, la tension de sortie ne pourra pas être suffisamment bien lissée. Attention que mettre une grosse capa signifie aussi souvent une ESR plus grande qui contribue à cette oscillation. On est parti sur le critère des transitoires vu que ces modules alimenteront principalement des moteurs. 2 fois 22 $\mu$ F 16V fonctionne bien dans notre cas et ajoute encore un peu à la standardisation des composants.

## DIODE DE ROUE LIBRE

Contrairement au module précédent, le régulateur ici n'est pas constitué d'un bras de hacheur complet (dont le fonctionnement est supposé compris par le lecteur). Il faut donc ajouter une diode de roue libre externe. Celle-ci doit avoir la chute de tension la plus faible possible pour dissiper le moins possible. Il faut donc une Schottky de puissance, on choisit un SS54 capable de monter à 5A et peut tenir 40V en inverse. C'est un peu limite niveau courant mais il est difficile d'avoir mieux sans sortir le portefeuille.

## UVLO

Le TPS54531 est muni d'une fonction d'UVLO ou "under-voltage lockout" qui désactive le régulateur dès que la tension d'entrée est en dessous d'un certain seuil. Ce dernier n'est activé que si la tension est supérieure à un deuxième seuil plus élevé. Il est bon pour ce genre de feature d'avoir de l'hystérèse, soit un écart suffisant entre les deux seuils pour éviter que le régulateur ne s'allume et s'éteigne sans cesse. La datasheet fournit les équations pour dimensionner les résistances. On choisit  $V_{start} = 17V$  et  $V_{stop} = 16V$  qui est la limite en dessous de laquelle la batterie au lithium doit être rechargée. C'est la raison pour laquelle il aurait été bien d'avoir un UVLO sur les autres régulateurs pour éviter de détruire la batterie en faisant trop chuter sa tension. Mais nous avons gardé le circuit d'alarme externe pour éviter ce problème.

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## COMPENSATION

Nous voici à présent entré dans la partie trouble de l'électronique de puissance et de la régulation, un aspect qui en a fait fuir plus d'un, la compensation de la boucle de régulation. Le circuit doit en effet réguler pour maintenir la tension adéquate en sortie malgré la charge et les transitoires. On a bien vu en automatique qu'un régulateur doit avoir une bande passante, une marge de phase et une marge de gain. Et bien pour ce régulateur, il faut définir ces aspects à travers le réseau RC du compensateur. Le fine tuning de la compensation ne se fait pas vraiment en deux coups de cuillère à pot et nécessite un analyseur de réseau (40 000 EUR). En revanche les équations dans la datasheet fonctionnent bien et peuvent être suivies aveuglement. Bien qu'un emplacement soit prévu sur le PCB, on ne placera pas dans notre cas de capa pour obtenir un phase boost. En effet celui-ci est souvent nécessaire lorsque l'ESR des capas de sortie est trop grande. En plus cela à tendance à apporter une part supplémentaire de mystère.

Si le lecteur est intéressé par cet aspect de la régulation, Texas instrument a rédigé une note assez bien expliquée sur le sujet qui s'intitule : « Demystifying Type II and Type III Compensators Using OpAmp and OTA for DC/DC Converters » disponible sur le net. Dans notre cas la partie sur les OTA nous intéresse plus.

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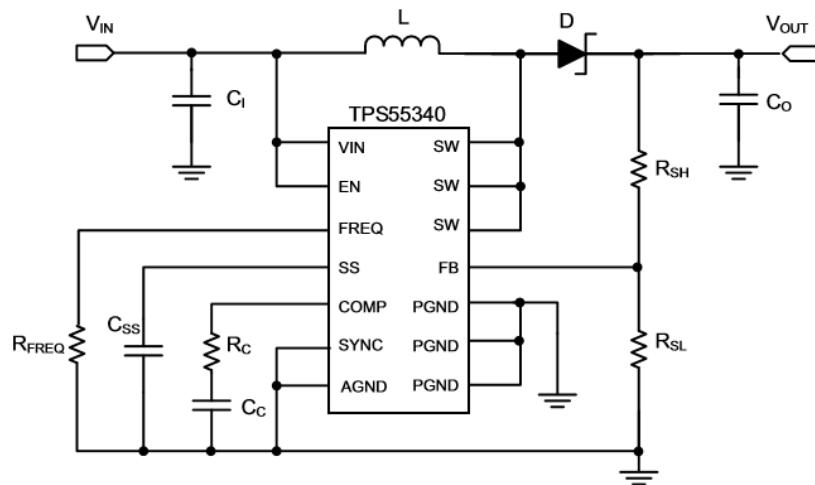
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## TPS55340

Chouette, vous êtes encore là ! On peut attaquer le plus gros morceau, le convertisseur boost pour fournir le 24V. Le régulateur choisi est le TPS55340. Avant de commencer, il faut déterminer les conditions d'utilisations.

- $V_{out} = 24V$
- $I_{out} (\text{max}) = 3A$  (bien que le régulateur puisse monter à 5A on s'impose cette limite)
- $V_{in}$  17v à 20v
- $F_{sw} = 600\text{kHz}$  Ici la fréquence peut être choisie, on verra comment. Comme les autres tournent à 600 et 570kHz on choisit 600kHz.

Le dimensionnement ressemble fort aux précédents mais est (pardonnez moi) plus chiant. Car comme le régulateur est plus complexe, la datasheet l'est aussi. Comme pour les autres, nous allons voir la marche à suivre. Voici déjà le schéma de base pour ce régulateur en mode boost.



A part que la topologie est différente des modules précédents, on reconnaît tous, sauf pour Rfreq. C'est donc par là que nous allons commencer.

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## FRÉQUENCE DE DÉCOUPAGE

Il est connu que la fréquence de découpage a un impact direct sur la taille des composants, notamment les inductances. On peut donc penser que monter à onze la fréquence de découpage n'est que bénéfique. Mais un problème parmi d'autres sont les pertes par commutations. Le choix de cette fréquence doit donc être un équilibre entre une multitude de paramètres. Pour notre application, on va juste dire qu'on choisit 600kHz car c'est la même fréquence que pour les 54531 et aussi parce que c'est l'exemple dans la datasheet donc on est sur que ça marche. Si on veut vraiment faire du rendement, c'est sur que c'est un paramètre très important.

Pour choisir la fréquence il faut dimensionner la résistance  $R_{freq}$  en appliquant une simple formule qui sort de quelque part dont personne en dehors de TI ne sait.  $R_{freq} = 57500 \cdot F_{sw}^{-1,03}$  pour une fréquence de 600kHz, la valeur la plus proche est 78,7KΩ. Même si la série E96 est déjà bien fournie, on verra plus tard comment obtenir une valeur très proche de celle voulue par les calculs.

Il est TRES IMPORTANT de placer cette résistance le plus proche possible du régulateur.

## CHOIX DE L'INDUCTANCE

C'est ici que les romains s'empoignèrent. Beaucoup de paramètres entrent en jeu et il faut parfois faire un travail itératif. Ne maîtrisant pas vraiment le boost (c'est la première fois que j'en implémente un) je creuse encore à ce jour cette partie. Les résultats obtenus fonctionnent bien cependant.

La première chose est de déterminer les deux rapports cycliques extrêmes pour  $V_{in}$  (min) = 17V et  $V_{in}$  (max)=20V. on obtient respectivement 30.6% et 18.4%.

Le choix de l'inductance ce fait en fonction du courant DC d'entrée maximal vu qu'elle est en ligne directe avec l'entrée. Le courant d'entrée est max lorsque le courant de sortie est max ET la tension d'entrée est minimale. On obtient donc 4.4A max en entrée du boost.

n.b. Contrairement au buck, dans le boost, il ne faut pas oublier que le courant d'entrée est supérieur au courant de sortie pour des raisons évidentes de conservation de l'énergie. D'où le choix de brider le boost à 3A max.

Comme pour les autres circuits on peut à présent déterminer la valeur minimale d'inductance avec  $U = L \cdot di/dt$  et une estimation de l'ondulation de courant ( $K_{ind}$ ). Ce calcul nous donne une valeur minimale de 9.8µH. Nous choisirons donc 10µH.

Une fois l'inductance choisie, nous pouvons déterminer les vrais courants de crête et efficaces. Les équations sont toujours les mêmes, juste mises dans un sens ou dans l'autre.

On obtient un courant de crête de 4.83A et un courant efficace de 4.42A ce qui nous dirige vers une Würth 74437368100.

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## CONDENSATEUR DE SORTIE

Une fois de plus, le choix du condensateur de sortie se fait soit en fonction des transitoires soit en fonction de l'ondulation admissible. Comme nous allons alimenter des moteurs, les transitoires sont évidemment le critère important. On s'autorise franchement 1V de chute de tension lors d'un transitoire de 0.8A (un peu tirer à la louche en fonction des moteurs du robot...). On choisira  $2 \times 10\mu F$  en 35V.

## DIODE

Le convertisseur boost a besoin d'une diode dans son bras. On choisira la même que pour les buck 5A pour standardiser les composants. Ses caractéristiques en courant et tension étant adaptées à cette utilisation.

## COMPENSATEUR

Plus que jamais, la stabilité de la boucle de régulation fut un véritable casse tête. La datasheet fournit des équations mais il est assez difficile de les comprendre et les appliquer bêtement n'a pas donné de bons résultats. Par chance TI fourni sur son site une document Excel qui calcule pour nous le réseau RC de compensation en fonction des paramètres de notre régulateur.

<http://www.ti.com/lit/zip/slvc430>

## CIRCUITS ANNEXES

Le circuit annexe important est une commande "enable" générale pour tous les modules. Les 54531 sont dotés d'un UVLO, mais il est important de pouvoir éteindre et allumer les modules sans devoir débrancher la batterie. Un N-MOS est donc mis entre chaque pin "EN" et la masse. Pour les modules sans UVLO, une pull-up est ajoutée entre "EN" et le bus principal. Attention ici tous les enable pouvaient monter au niveau du bus d'alimentation, mais ce n'est peut-être pas toujours le cas. Les grilles des N-MOS sont ensuite toutes mises en commun. Un jumper permet ensuite de mettre les grilles à la masse, dans quel cas les transistors sont bloqués et les modules allumés. Ou alors les grilles sont mises à la moitié de la tension du bus principal (Vg max étant de 10V pour le modèle choisi) à travers un diviseur de tension dans quel cas les N-MOS tirent les "EN" à la masse. Une troisième résistance a été ajoutée par la suite entre les grilles et Vcc/2 pour qu'en cas où le jumper n'est dans aucune position, les grilles ne sont pas flottantes et les modules sont éteints. Attention que pour le boost, la sortie est en ligne directe avec l'entrée. Donc même si celui-ci est désactivé, Vout sera toujours égal à Vin.

L'idéal aurait été d'ajouter l'alarme de sous tension de batterie sur le PCB. Pour la rev2 sûrement.

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## ROUTAGE DU PCB

Dans cette dernière partie nous allons aborder certains aspects de routage de PCB et surtout pour un PCB comme celui-ci qui peut être « modulable » et servir de testbench pour tester de nouvelles choses. Pour un tel PCB avec pas mal de superflu une taille autour des 10 x 16 est largement faisable et peut facilement être montée sur le robot.

### MODULARITÉ

La première chose à prendre en compte lors de la création d'un tel circuit est la modularité et la standardisation. Quand on regarde le PCB, beaucoup de choses sont identiques. Et pour cause, j'ai carrément fait un copier/coller dans Altium. Cela va sans dire, mais il doit y avoir une cohérence dans le placement des composants. Quand on voit le PCB, on voit tout de suite les 6 régulateurs avec tous leurs composants annexes très proches.

Il est bon aussi d'avoir une standardisation des composants. Cela revient à moins cher, on fait moins d'erreurs surtout si on les place à la main. Mais surtout on revient à la modularité. Par exemple pour les régulateurs 12V et 9,5V les inductances sont de la même famille avec le même footprint. Donc si quelqu'un préfère avoir 2 fois 12V ou deux fois 9,5V il peut le faire sans problème. Pareil pour les régulateurs 3,3V et 5V.

Enfin quand la datasheet vous propose des composants en option comme pour la compensation ou autre, même si vous ne comptez pas les utiliser, s'il vous plaît, placez-les quand-même sur le PCB...

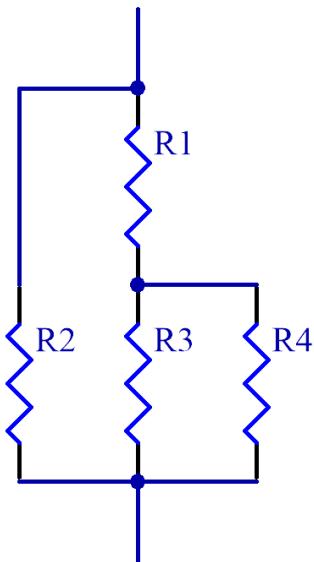
### RESISTANCES DE PRÉCISION

Lorsqu'on dessine un PCB surtout un peu style prototype modulable, on ne sait pas toujours la valeur des résistances et ce qu'il nous faut pour avoir une valeur précise. Un truc bien sympa pour les choses critiques est de placer le footprint pour 4 résistances dans la configuration ci-dessous. Avec ça on peut agencer des résistances comme on veut et obtenir quasi n'importe quoi comme valeur. Cette astuce m'a déjà bien aidé lors de débogging auparavant. C'est la raison pour laquelle tant de composants semblent absent sur le circuit.

Une fois qu'on est satisfait des perfos, si on veut réduire la taille du PCB, c'est un bon point de départ car ça prend pas mal de place mais ça en vaut parfois la peine.

Matricule ECAM	Date	Année académique	Exemplaire
13018	30 avril 2017	2017/2018	1

# CARTE DE PUISSANCE EUROBOT 2017



## CONNECTIQUE

Utiliser le même connecteur pour l'entrée batterie et la sortie 24V était clairement une mauvaise idée, l'erreur est trop vite commise. Même si je ne suis pas sûr que ça fasse beaucoup de dégâts voir même pas du tout avec la diode, on ne sait jamais... A changer plus tard.

## PROXIMITÉ DES COMPOSANTS ET CEM

On ne répète jamais assez de placer les composants proches les uns des autres pour avoir les plus petites pistes possibles. C'est surtout vrai pour les circuits de puissance. Il faut toujours penser, par où passe le courant Y compris le courant de retour trop souvent oublié dans le plan de masse. TI donne parfois des exemples de routage pour leurs régulateurs. Il faut vraiment que la boucle de puissance soit la plus refermée possible et la plus courte pour limiter les perturbations et placer les composants annexes (comme le diviseur de tension pour le feedback en dehors dans une zone « non polluée »).

Le bus principal est placé au centre du PCB et les différents taps montent verticalement vers les différents modules, sans faire de détours inutiles. Le courant de retour passe juste en dessous dans le plan de masse sur la couche inférieure.

C'est un bon endroit pour rappeler l'importance de la proximité de la capa de découplage du régulateur. Et proximité ne veut pas dire la mettre juste à côté puis faire une piste qui fait tout le tour du PCB... Il m'est déjà arrivé d'avoir des soucis parce que ma capa était même pas à 1cm de mon régulateur.

Matricule ECAM	Date	Année académique	Exemplaire
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## CARTE DE PUISSANCE EUROBOT 2017

Revenons au plan de masse. Il a plusieurs utilités très importantes. Ce n'est pas parce qu'il y en a un qu'on peut faire n'importe quoi. Ne jamais perdre de vue par où passe le courant de retour. Il choisira toujours le chemin de plus basse IMPEDANCE. À ces fréquences, il passera juste en dessous du courant allez. D'où l'importance de laisser le plan de masse bien dégager et ne rien router sur la couche inférieur. Sauf si c'est vraiment nécessaire mais tout en restant attentif à ne pas traverser le chemin de la puissance. Bon j'ai délimité les plans de masse de chaque module mais ce n'était pas forcément nécessaire.

Par contre ce qui est nécessaire, c'est de découper le plan de masse en dessous des inductances ! Ça évitera beaucoup de pollution dans la masse.

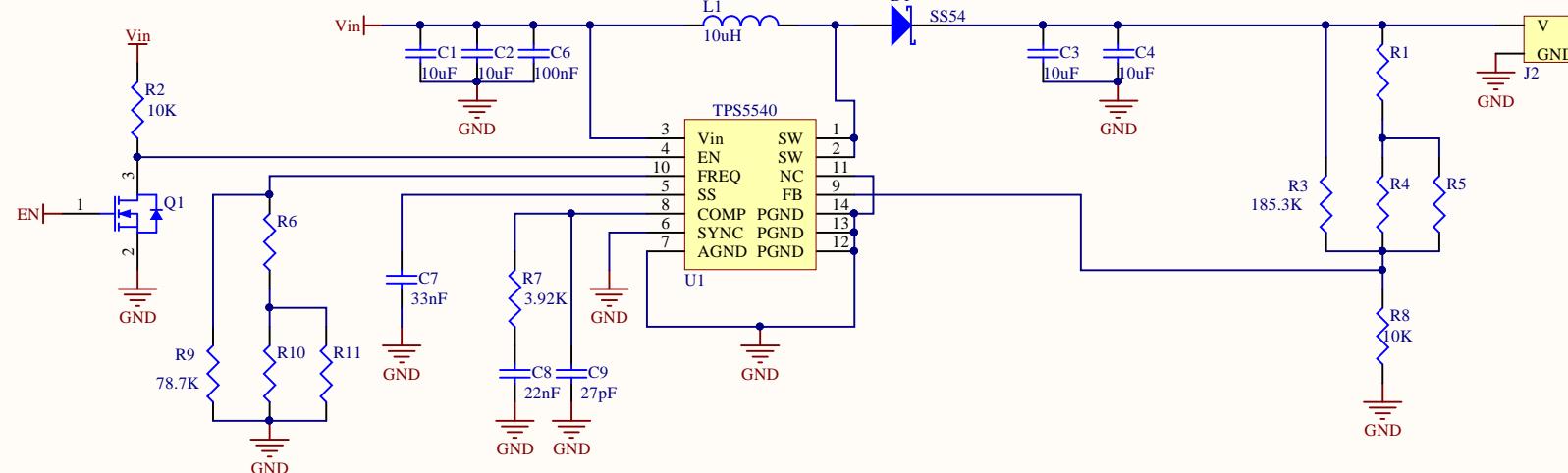
### ASPECTS THERMIQUE

Même si on fait du découpage en étant supposés avoir de bon rendements (supérieurs à 90%) on a vu qu'on dissipait vite 6W de chaleur dans un boîtier SOIC-8. Il faut donc dissiper cette chaleur pour éviter un thermal lockout. C'est la deuxième utilité du plan de masse, il fait office de dissipateur. Les régulateurs sont munis d'une plaque métallique en dessous pour avoir la plus petite résistance thermique. Il faut absolument augmenter au maximum la masse thermique sur le PCB en ajoutant un plan de masse sur la face du dessus là où c'est possible ainsi que mettre une flopée de vias pour transférer la chaleur vers le plan de masse principale.

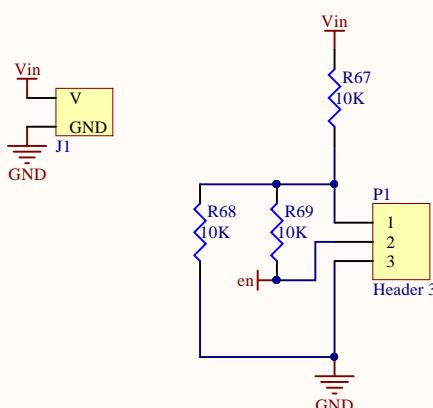
C'est à ce niveau-là qu'il y a eu une erreur de conception de ma part pour les régulateur 9.5V et 12V. En effet le plan de masse supérieur qui ne conduit pas de courant est sectionné pour laisser passer la commande de bootstrap. Ce qui a pour effet de donner une plus petite surface pour dissiper la chaleur. Mais le bootstrap ne peut pas passer autre part... j'ai augmenté l'épaisseur de cuivre lors de la fabrication, ainsi que le nombre de vias et mis de la pâte thermique entre le régulateur et le plan de masse. Ça a amélioré la situation, mais il a toujours du mal à 5A. A creuser pour plus tard.

Matricule ECAM	Date	Année académique	Exemplaire
13018	30 avril 2017	2017/2018	1

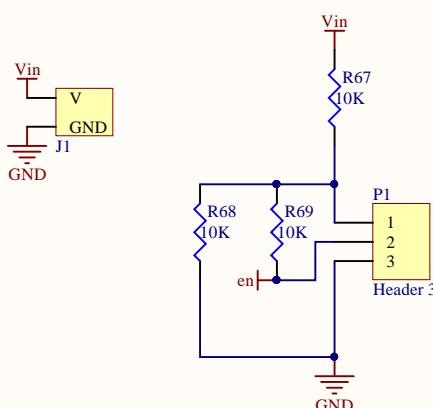
A



B



C



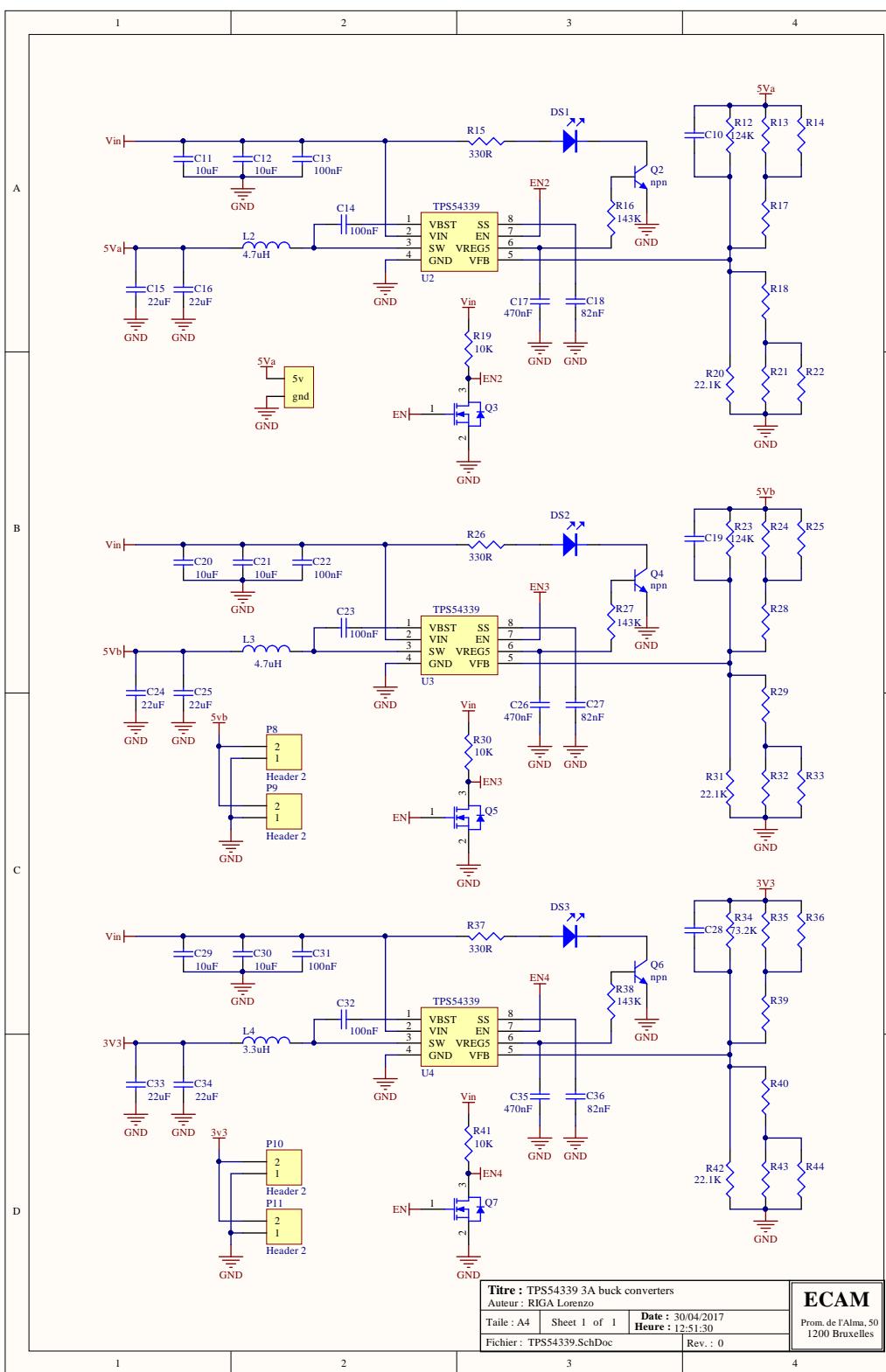
D

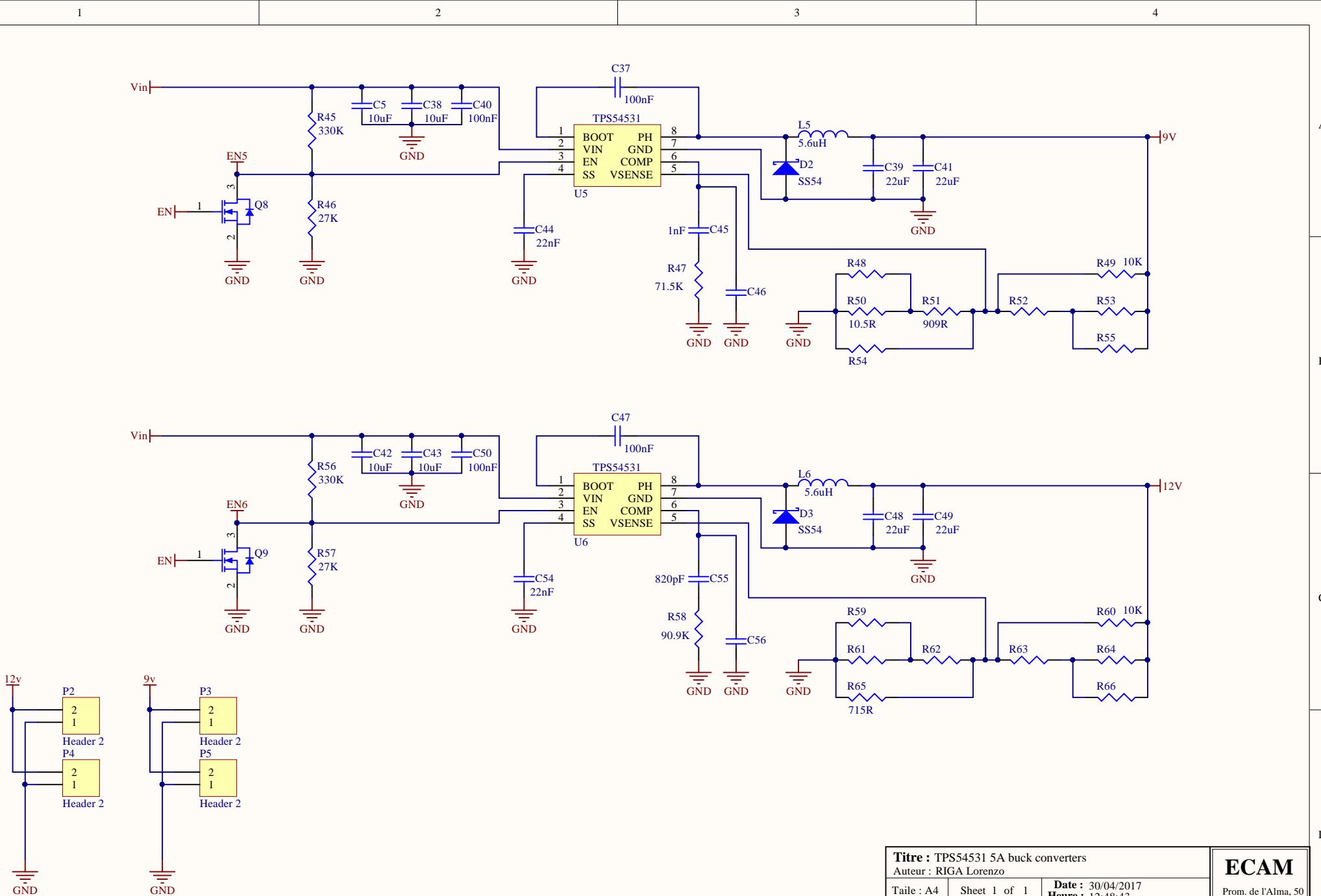
**Titre :** TPS55340 boost converter  
**Auteur :** RIGA Lorenzo

Taille : A4	Sheet 1 of 1	Date : 30/04/2017
		Heure : 12:49:02
Fichier : boost_schem.SchDoc		Rev. : 0

**ECAM**

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1200 Bruxelles





Titre : TPS54531 5A buck converters  
Auteur : RIGA Lorenzo

Taille : A4 Sheet 1 of 1 Date : 30/04/2017  
Heure : 12:48:43  
Fichier : tps54531.SchDoc Rev. : 0

**ECAM**  
Prom. de l'Alma, 50  
1200 Bruxelles

## 4.5 V to 23 V Input, 3-A Synchronous Step-Down SWIFT™ Converter

Check for Samples: [TPS54339](#)

### FEATURES

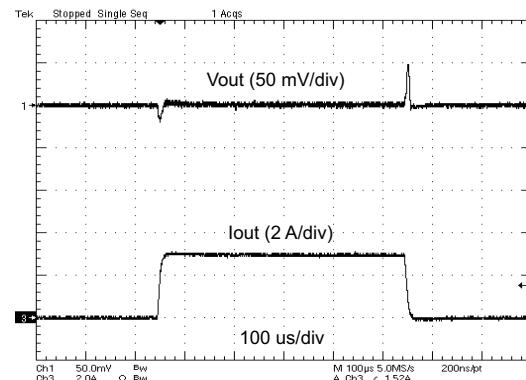
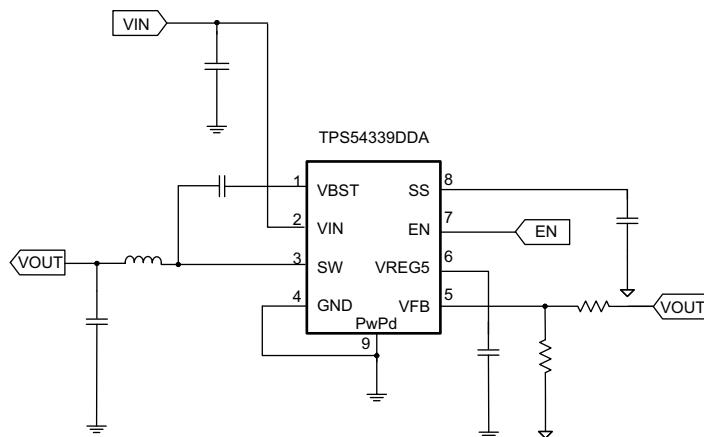
- D-CAP2™ Mode Enables Fast Transient Response
- Low Output Ripple and Allows Ceramic Output Capacitor
- Wide  $V_{IN}$  Input Voltage Range: 4.5 V to 23 V
- Output Voltage Range: 0.76 V to 7 V
- Highly Efficient Integrated FETs Optimized for Lower Duty Cycle Applications
  - 140 mΩ (High Side) and 70 mΩ (Low Side)
- High Efficiency, less than 10 µA at shutdown
- High Initial Bandgap Reference Accuracy
- Adjustable Soft Start
- Pre-Biased Soft Start
- 600-kHz Switching Frequency ( $f_{sw}$ )
- Cycle By Cycle Over Current Limit

### DESCRIPTION

The TPS54339 is an adaptive on-time D-CAP2™ mode synchronous buck converter. The TPS54339 enables system designers to complete the suite of various end-equipment power bus regulators with a cost effective, low component count, low standby current solution. The main control loop for the TPS54339 uses the D-CAP2™ mode control that provides a fast transient response with no external compensation components. The TPS54339 also has a proprietary circuit that enables the device to adapt to both low equivalent series resistance (ESR) output capacitors, such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors. The device operates from 4.5-V to 23-V  $V_{IN}$  input. The output voltage can be programmed between 0.76 V and 7 V. The device also features an adjustable soft start time. The TPS54339 is available in the 8-pin DDA package, and designed to operate from -40°C to 85°C.

### APPLICATIONS

- Wide Range of Applications for Low Voltage System
  - Digital TV Power Supply
  - High Definition Blu-ray Disc™ Players
  - Networking Home Terminal
  - Digital Set Top Box (STB)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

D-CAP2 is a trademark of Texas Instruments.

Blu-ray Disc is a trademark of Blu-ray Disc Association.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### ORDERING INFORMATION<sup>(1)</sup>

T <sub>A</sub>	PACKAGE <sup>(2) (3)</sup>	ORDERABLE PART NUMBER	PIN	TRANSPORT MEDIA
–40°C to 85°C	DDA	TPS54339DDA	8	Tube
		TPS54339DDAR		Tape and Reel

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).
- (2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).
- (3) All package options have Cu NIPDAU lead/ball finish.

### ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		VALUE		UNIT
		MIN	MAX	
Input voltage range	VIN, EN	–0.3	25	V
	VBST	–0.3	31	
	VBST (10 ns transient)	–0.3	33	
	VBST (vs SW)	–0.3	6.5	
	VFB, SS	–0.3	6.5	
	SW	–2	25	
Output voltage range	SW (10 ns transient)	–3	27	V
	VREG5	–0.3	6.5	
Electrostatic discharge	GND	–0.3	0.3	V
	Human Body Model (HBM)		2	
Operating junction temperature, T <sub>J</sub>	Charged Device Model (CDM)		500	°C
		–40	150	
Storage temperature, T <sub>stg</sub>		–55	150	

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### THERMAL INFORMATION

	THERMAL METRIC <sup>(1)</sup>	TPS54339	UNITS
		DDA (8 PINS)	
θ <sub>JA</sub>	Junction-to-ambient thermal resistance	46.2	°C/W
θ <sub>JCTop</sub>	Junction-to-case (top) thermal resistance	53.9	
θ <sub>JB</sub>	Junction-to-board thermal resistance	29.7	
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	10.0	
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	29.6	
θ <sub>JCbot</sub>	Junction-to-case (bottom) thermal resistance	6.6	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range, (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>IN</sub>	Supply input voltage range		4.5	23	V
V <sub>I</sub>	Input voltage range	VBST	-0.1	29	V
		VBST (10 ns transient)	-0.1	32	
		VBST(vs SW)	-0.1	5.7	
		SS	-0.1	5.7	
		EN	-0.1	23	
		VFB	-0.1	5.5	
		SW	-1.8	23	
		SW (10 ns transient)	-3	26	
		GND	-0.1	0.1	
V <sub>O</sub>	Output voltage range	VREG5	-0.1	5.7	V
I <sub>O</sub>	Output Current range	I <sub>VREG5</sub>	0	10	mA
T <sub>A</sub>	Operating free-air temperature		-40	85	°C
T <sub>J</sub>	Operating junction temperature		-40	150	°C

## ELECTRICAL CHARACTERISTICS

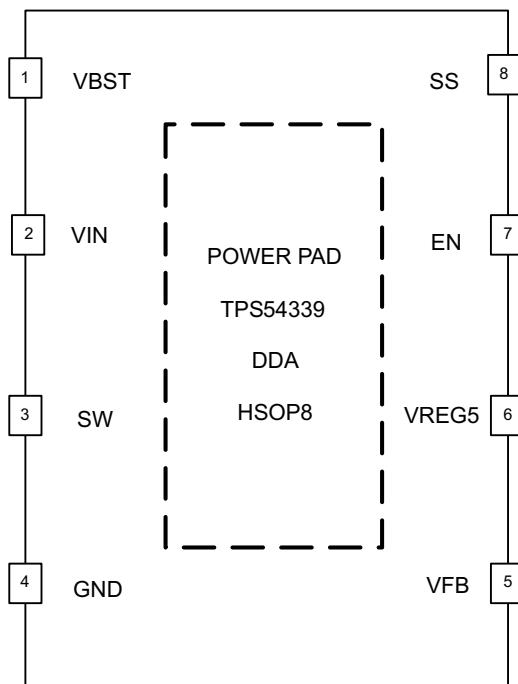
over operating free-air temperature range, V<sub>IN</sub> = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY CURRENT</b>						
I <sub>VIN</sub>	Operating - non-switching supply current	V <sub>IN</sub> current, T <sub>A</sub> = 25°C, EN = 5V, V <sub>FB</sub> = 0.8V	850	1200	1200	µA
I <sub>VINSDN</sub>	Shutdown supply current	V <sub>IN</sub> current, T <sub>A</sub> = 25°C, EN = 0 V	3.0	10	10	µA
<b>LOGIC THRESHOLD</b>						
V <sub>ENH</sub>	EN high-level input voltage	EN	1.6			V
V <sub>ENL</sub>	EN low-level input voltage	EN		0.6		V
R <sub>EN</sub>	EN pin resistance to GND	V <sub>EN</sub> = 12 V	200	400	800	kΩ
<b>V<sub>FB</sub> VOLTAGE AND DISCHARGE RESISTANCE</b>						
V <sub>FBTH</sub>	V <sub>FB</sub> threshold voltage	T <sub>A</sub> = 25°C, V <sub>O</sub> = 1.05 V, continuous mode operation	749	765	781	mV
I <sub>VFB</sub>	V <sub>FB</sub> input current	V <sub>FB</sub> = 0.8 V, T <sub>A</sub> = 25°C	0	±0.1	±0.1	µA
<b>V<sub>REG5</sub> OUTPUT</b>						
V <sub>VREG5</sub>	V <sub>REG5</sub> output voltage	T <sub>A</sub> = 25°C, 6.0 V < V <sub>IN</sub> < 23 V, 0 < I <sub>VREG5</sub> < 5 mA	5.2	5.5	5.7	V
I <sub>VREG5</sub>	Output current	V <sub>IN</sub> = 6 V, V <sub>REG5</sub> = 4.0 V, T <sub>A</sub> = 25°C	20			mA
<b>MOSFET</b>						
R <sub>DS(on)h</sub>	High side switch resistance	25°C, V <sub>BST</sub> - SW = 5.5 V <sup>(1)</sup>	140			mΩ
R <sub>DS(on)l</sub>	Low side switch resistance	25°C <sup>(1)</sup>	70			mΩ
<b>CURRENT LIMIT</b>						
I <sub>ocl</sub>	Current limit	L out = 2.2 µH <sup>(1)</sup>	3.5	4.1	5.7	A
<b>THERMAL SHUTDOWN</b>						
T <sub>SDN</sub>	Thermal shutdown threshold	Shutdown temperature <sup>(1)</sup>	165			°C
		Hysteresis <sup>(1)</sup>	40			
<b>ON-TIME TIMER CONTROL</b>						
t <sub>ON</sub>	On time	V <sub>IN</sub> = 12 V, V <sub>O</sub> = 1.05 V	160			ns
t <sub>OFF(MIN)</sub>	Minimum off time	T <sub>A</sub> = 25°C, V <sub>FB</sub> = 0.7 V <sup>(1)</sup>	260	310	310	ns

(1) Not production tested.

**ELECTRICAL CHARACTERISTICS (continued)**over operating free-air temperature range,  $V_{IN} = 12\text{ V}$  (unless otherwise noted)

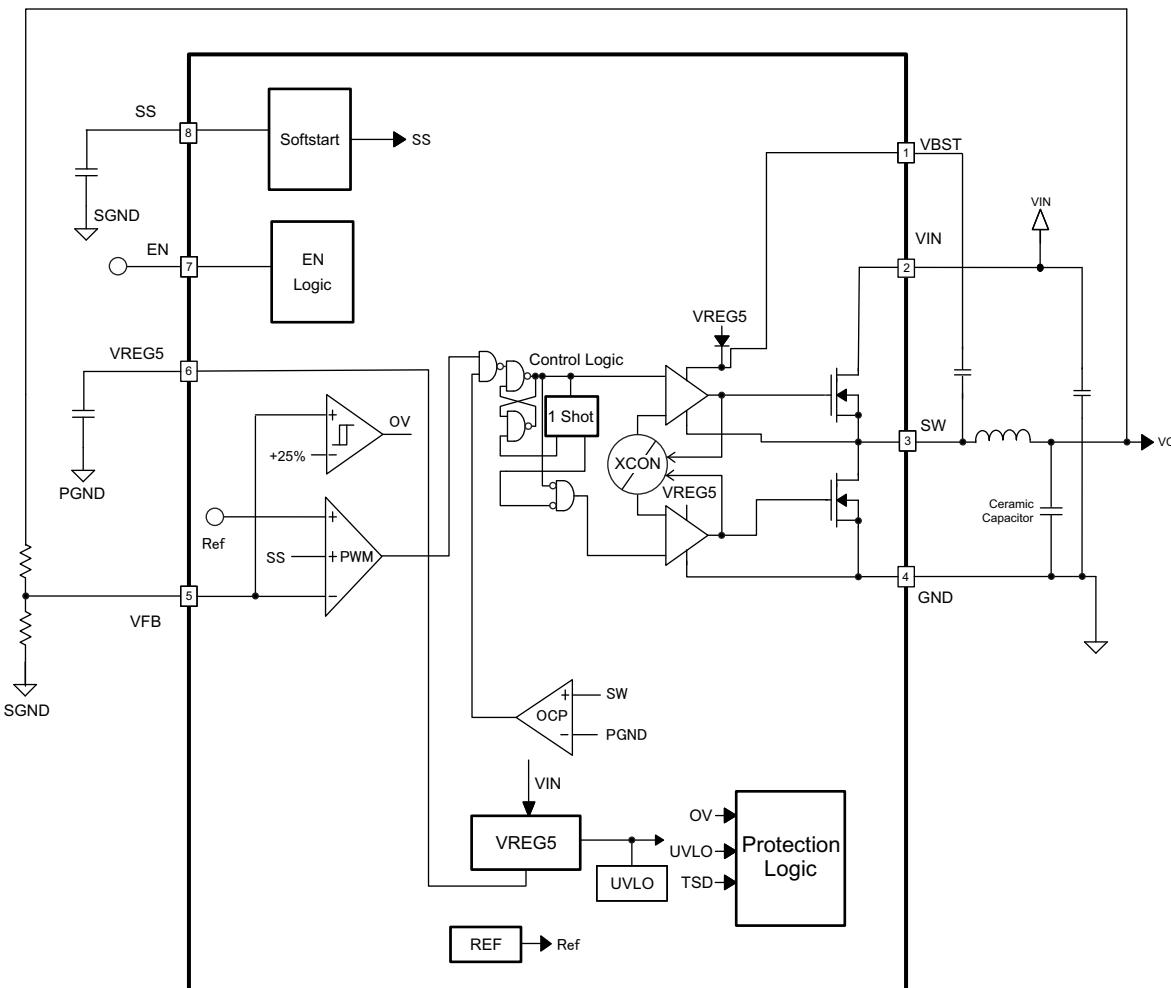
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SOFT START</b>						
I <sub>SSC</sub>	SS charge current	V <sub>SS</sub> = 1.0 V	4.2	6.0	7.8	μA
I <sub>SSD</sub>	SS discharge current	V <sub>SS</sub> = 0.5 V	0.8	1.5		mA
<b>HICCUP AND OVERVOLTAGE PROTECTION</b>						
V <sub>OVP</sub>	Output OVP threshold	OVP Detect (L>H)	125%			
V <sub>UV</sub> P	Output Hiccup threshold	Hiccup detect (H>L)	65%			
T <sub>UVPDEL</sub>	Output Hiccup delay	to Hiccup state	6			μs
T <sub>UVPEN</sub>	Output Hiccup Enable delay	Relative to soft-start time	x1.7			
<b>UVLO</b>						
UVLO	UVLO threshold	Wake up V <sub>REG5</sub> voltage	3.45	3.75	4.05	V
		Hysteresis V <sub>REG5</sub> voltage	0.17	0.33	0.47	

**DEVICE INFORMATION**DDA PACKAGE  
(TOP VIEW)**PIN FUNCTIONS**

PIN		DESCRIPTION
NAME	NO.	
VBST	1	Supply input for the high-side FET gate drive circuit. Connect 0.1μF capacitor between VBST and SW pins. An internal diode is connected between VREG5 and VBST.
VIN	2	Input voltage supply pin.
SW	3	Switch node connection between high-side NFET and low-side NFET.
GND	4	Ground pin. Power ground return for switching circuit. Connect sensitive SS and VFB returns to GND at a single point.
VFB	5	Converter feedback input. Connect to output voltage with feedback resistor divider.

**PIN FUNCTIONS (continued)**

<b>PIN</b>		<b>DESCRIPTION</b>
<b>NAME</b>	<b>NO.</b>	
VREG5	6	5.5 V power supply output. A capacitor (typical 0.47 $\mu$ F) should be connected to GND. VREG5 is not active when EN is low.
EN	7	Enable input control. EN is active high and must be pulled up to enable the device.
SS	8	Soft-start control. An external capacitor should be connected to GND.
Exposed Thermal Pad	Back side	Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Must be connected to GND.

**FUNCTIONAL BLOCK DIAGRAM**


## OVERVIEW

The TPS54339 is a 3-A synchronous step-down (buck) converter with two integrated N-channel MOSFETs. It operates using D-CAP2™ mode control. The fast transient response of D-CAP2™ control reduces the output capacitance required to meet a specific level of performance. Proprietary internal circuitry allows the use of low ESR output capacitors including ceramic and special polymer types.

## DETAILED DESCRIPTION

### PWM Operation

The main control loop of the TPS54339 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ mode control. D-CAP2™ mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot is set by the converter input voltage, VIN, and the output voltage, VO, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.

### PWM Frequency and Adaptive On-Time Control

TPS54339 uses an adaptive on-time control scheme and does not have a dedicated on board oscillator. The TPS54339 runs with a pseudo-constant frequency of 600 kHz by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage; therefore, when the duty ratio is VOUT/VIN, the frequency is constant.

### Soft Start and Pre-Biased Soft Start

The soft start function is adjustable. When the EN pin becomes high, 6  $\mu$ A current begins charging the capacitor which is connected from the SS pin to GND. Smooth control of the output voltage is maintained during start up. The equation for the slow start time is shown in [Equation 1](#). VFB voltage is 0.765 V and SS pin source current is 6  $\mu$ A.

$$t_{SS}^{(ms)} = \frac{C_{SS}^{(nF)} \times V_{REF} \times 1.1}{I_{SS}^{(\mu A)}} = \frac{C_{SS}^{(nF)} \times 0.765 \times 1.1}{6} \quad (1)$$

The TPS54339 contains a unique circuit to prevent current from being pulled from the output during startup if the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft start becomes greater than feedback voltage  $V_{FB}$ ), the controller slowly activates synchronous rectification by starting the first low side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-bias output, and ensure that the out voltage ( $V_O$ ) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased start-up to normal mode operation.

### Current Protection

The output overcurrent protection (OCP) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored by measuring the low-side FET switch voltage between the SW pin and GND. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by  $V_{IN}$ ,  $V_{OUT}$ , the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current  $I_{out}$ . The TPS54339 constantly monitors the low-side FET switch voltage, which is proportional to the switch current, during the low-side on-time. If the measured voltage is above the voltage proportional to the current limit, an internal counter is incremented per each SW cycle and the converter maintains the low-side switch on until the measured voltage is below the voltage corresponding to the current limit at which time the switching cycle is terminated and a new switching

cycle begins. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner. If the over current condition exists for 7 consecutive switching cycles, the internal OCL threshold is set to a lower level, reducing the available output current. When a switching cycle occurs where the switch current is not above the lower OCL threshold, the counter is reset and the OCL limit is returned to the higher value.

There are some important considerations for this type of over-current protection. The load current one half of the peak-to-peak inductor current higher than the over-current threshold. Also when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output voltage to fall. When the VFB voltage becomes lower than 65% of the target voltage, the UVP comparator detects it. After 6μs detecting the UVP voltage, device will shut down and restart after 7 times SS period for Hiccup.

When the over current condition is removed, the output voltage returns to the regulated value. This protection is non-latching.

### Over Voltage Protection

TPS54339 detects over voltage conditions by monitoring the feedback voltage (VFB). This function is enabled after approximately 1.7 x times the soft start time.

When the feedback voltage becomes higher than 125% of the target voltage, the OVP comparator output goes high and both the high-side MOSFET driver and the low-side MOSFET driver turn off. This function is non-latch operation.

### UVLO Protection

Undervoltage lock out protection (UVLO) monitors the voltage of the V<sub>REG5</sub> pin. When the V<sub>REG5</sub> voltage is lower than UVLO threshold voltage, the TPS54339 is shut off. This protection is non-latching.

### Thermal Shutdown

TPS54339 monitors the temperature of itself. If the temperature exceeds the threshold value (typically 165°C), the device is shut off. This is non-latch protection.

## TYPICAL CHARACTERISTICS

$V_{IN} = 12\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted).

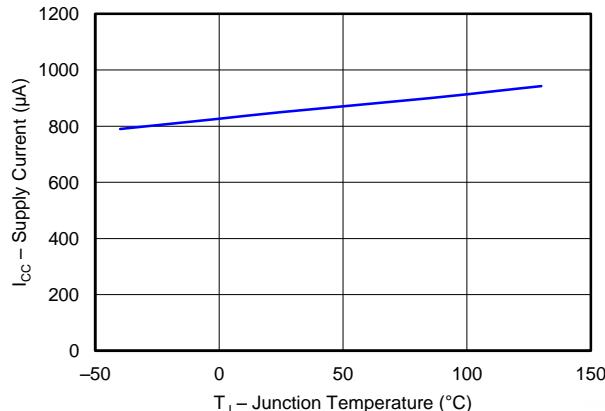


Figure 1. **VIN CURRENT vs JUNCTION TEMPERATURE**

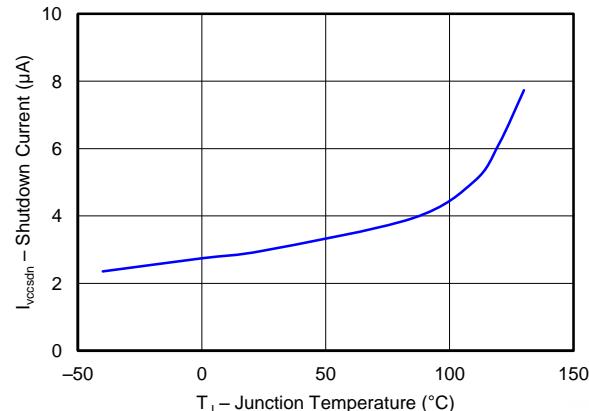


Figure 2. **VIN SHUTDOWN CURRENT vs JUNCTION TEMPERATURE**

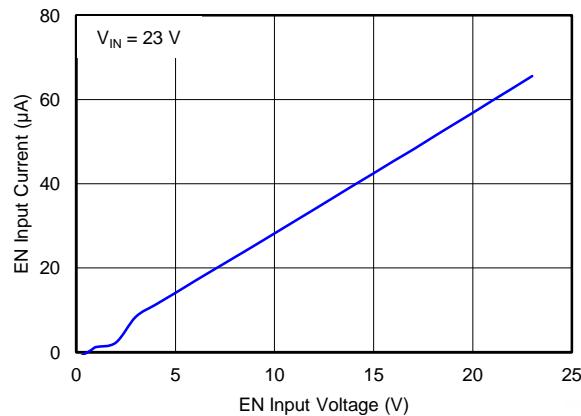


Figure 3. **EN CURRENT vs EN VOLTAGE**

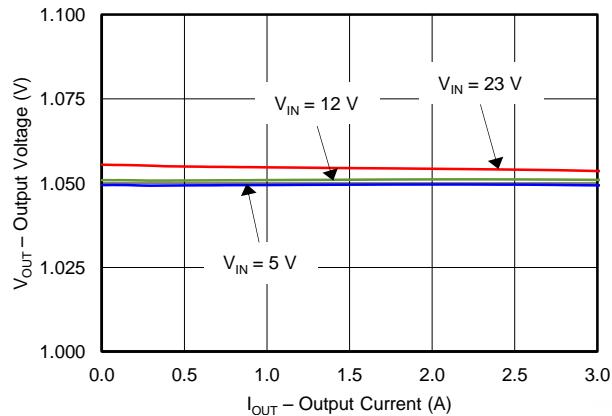


Figure 4. **1.05-V OUTPUT VOLTAGE vs OUTPUT CURRENT**

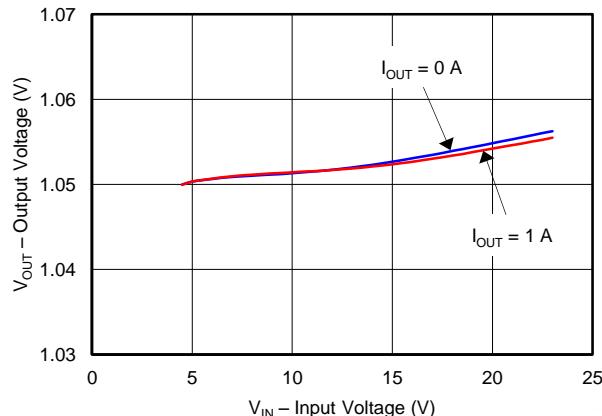


Figure 5. **1.05-V OUTPUT VOLTAGE vs INPUT VOLTAGE**

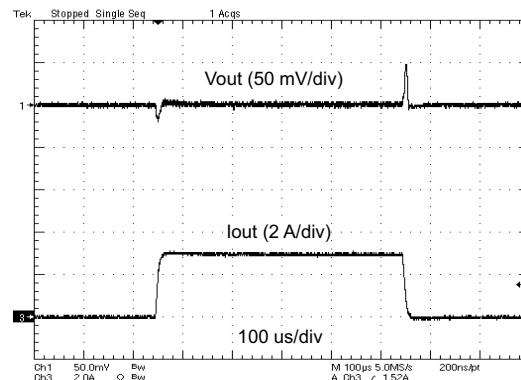
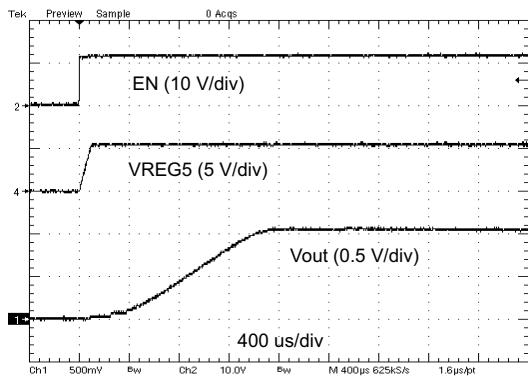


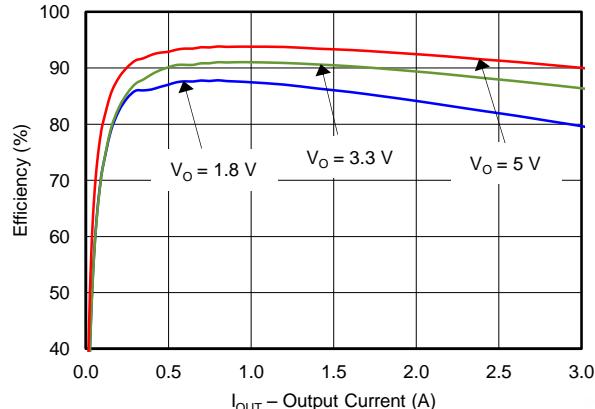
Figure 6. **1.05-V, LOAD TRANSIENT RESPONSE**

## TYPICAL CHARACTERISTICS

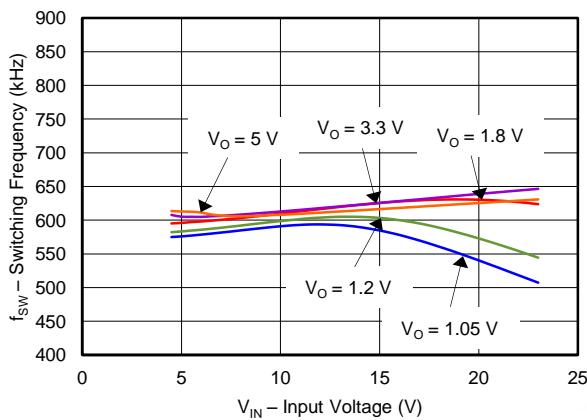
V<sub>IN</sub> = 12 V, T<sub>A</sub> = 25°C (unless otherwise noted).



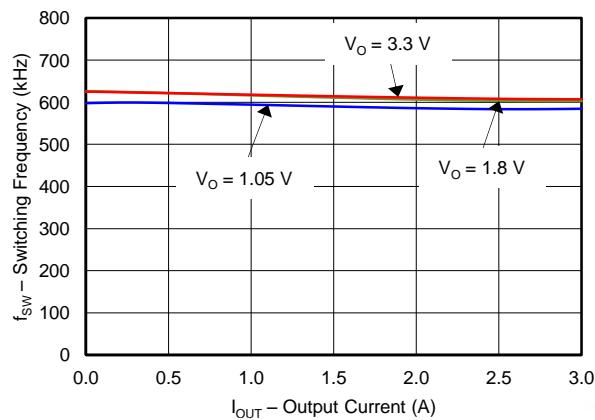
**Figure 7. START-UP WAVE FORM**



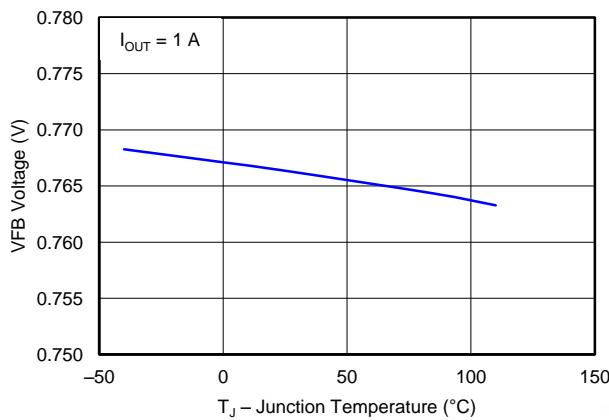
**Figure 8. EFFICIENCY vs OUTPUT CURRENT**



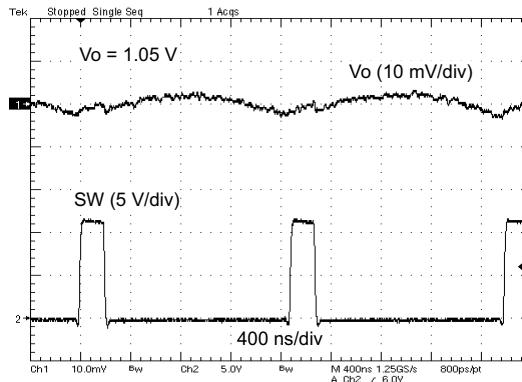
**Figure 9. SWITCHING FREQUENCY vs INPUT VOLTAGE (I<sub>O</sub> = 1 A)**



**Figure 10. SWITCHING FREQUENCY vs OUTPUT CURRENT**



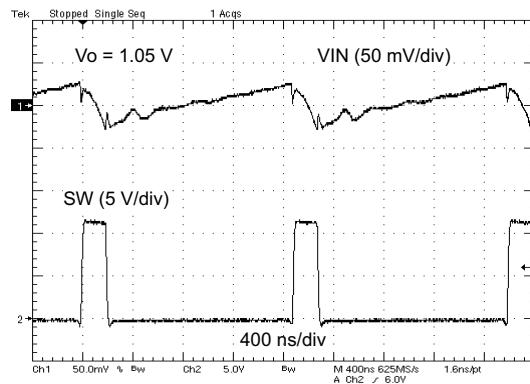
**Figure 11. VFB VOLTAGE vs JUNCTION TEMPERATURE (I<sub>O</sub> = 1 A)**



**Figure 12. VOLTAGE RIPPLE AT OUTPUT (I<sub>O</sub> = 3A)**

**TYPICAL CHARACTERISTICS (continued)**

VIN = 12 V, TA = 25°C (unless otherwise noted).

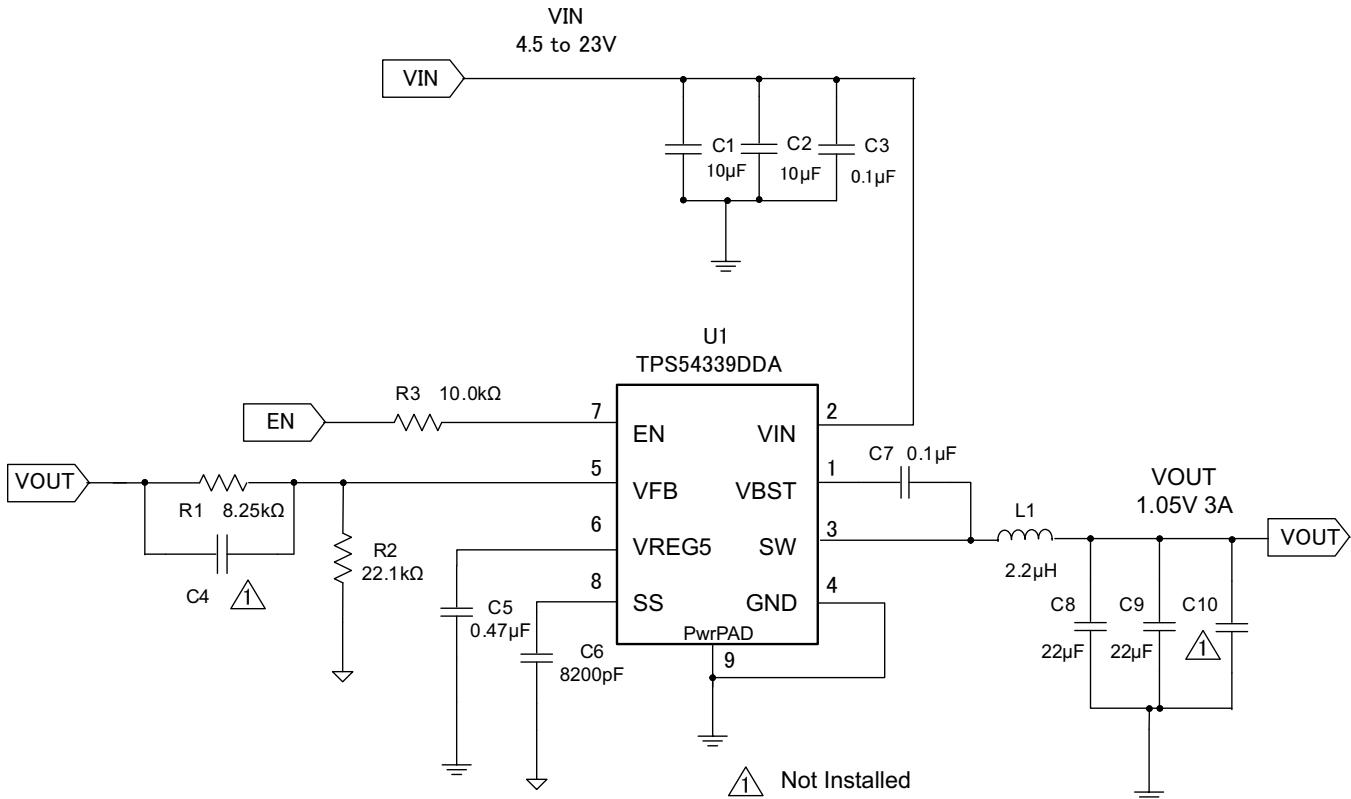
**Figure 13. VOLTAGE RIPPLE AT INPUT (I<sub>O</sub> = 3 A)**

## DESIGN GUIDE

### Step-By-Step Design Procedure

To begin the design process, the user must know a few application parameters:

- Input voltage range
- Output voltage
- Output current
- Output voltage ripple
- Input voltage ripple



**Figure 14.** Shows the schematic diagram for this design example.

### Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. It is recommended to use 1% tolerance or better divider resistors. Start by using [Equation 2](#) to calculate  $V_{OUT}$ .

To improve efficiency at light loads consider using larger value resistors, high resistance is more susceptible to noise, and the voltage errors from the VFB input current are more noticeable.

$$V_{OUT} = 0.765 \times \left(1 + \frac{R_1}{R_2}\right) \quad (2)$$

### Output Filter Selection

The output filter used with the TPS54339 is an LC circuit. This LC filter has double pole at:

$$f_p = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \quad (3)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS54339. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a -40 dB per decade rate and the phase drops rapidly. D-CAP2™ introduces a high frequency zero that reduces the gain roll off to -20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor selected for the output filter must be selected so that the double pole of [Equation 3](#) is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in [Table 1](#)

**Table 1. Recommended Component Values**

Output Voltage (V)	R1 (kΩ)	R2 (kΩ)	C4 (pF) <sup>(1)</sup>			L1 (μH)			C8 + C9 + C10 (μF)	
			Min	Typ	Max	Min	Typ	Max	Min	Max
1	6.81	22.1	5	150	220	1.5	2.2	4.7	22	68
1.05	8.25	22.1	5	150	220	1.5	2.2	4.7	22	68
1.2	12.7	22.1	5		100	1.5	2.2	4.7	22	68
1.5	21.5	22.1	5		68	1.5	2.2	4.7	22	68
1.8	30.1	22.1	5		22	2.2	3.3	4.7	22	68
2.5	49.9	22.1	5		22	2.2	3.3	4.7	22	68
3.3	73.2	22.1	5		22	2.2	3.3	4.7	22	68
5	124	22.1	5		22	3.3		4.7	22	68
6.5	165	22.1	5		22	3.3		4.7	22	68

(1) Optional

Since the DC gain is dependent on the output voltage, the required inductor value increases as the output voltage increases. Additional phase boost can be achieved by adding a feed forward capacitor (C4) in parallel with R1. The amount of available phase boost is dependent on the output voltage. Higher output voltages will allow greater phase boost.

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using [Equation 4](#), [Equation 5](#) and [Equation 6](#). The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current. Use 600 kHz for  $f_{SW}$ .

Use 600 kHz for  $f_{SW}$ . Make sure the chosen inductor is rated for the peak current of [Equation 5](#) and the RMS current of [Equation 6](#).

$$I_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \quad (4)$$

$$I_{PEAK} = I_O + \frac{I_{P-P}}{2} \quad (5)$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} I_{P-P}^2} \quad (6)$$

For this design example, the calculated peak current is 3.38 A and the calculated RMS current is 3.01 A. The inductor used is a TDK CLF7045T-2R2N with a peak current rating of 5.5 A and an RMS current rating of 4.3 A. For high current designs, TDK SPM6530T-4R7M 4.7μH is also recommended. The SPM6530 series has a higher current rating than the CLF7045 series.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS54339 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 22μF to 68μF. Use [Equation 7](#) to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \quad (7)$$

For this design two TDK C3216X5R0J226M 22μF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.22 A and each output capacitor is rated for 4A.

### Input Capacitor Selection

The TPS54339 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10  $\mu\text{F}$  is recommended for the decoupling capacitor. An additional 0.1  $\mu\text{F}$  capacitor from pin 2 to ground is optional to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

### Bootstrap Capacitor Selection

A 0.1  $\mu\text{F}$ . ceramic capacitor must be connected between the VBST to SW pin for proper operation. It is recommended to use a ceramic capacitor.

### VREG5 Capacitor Selection

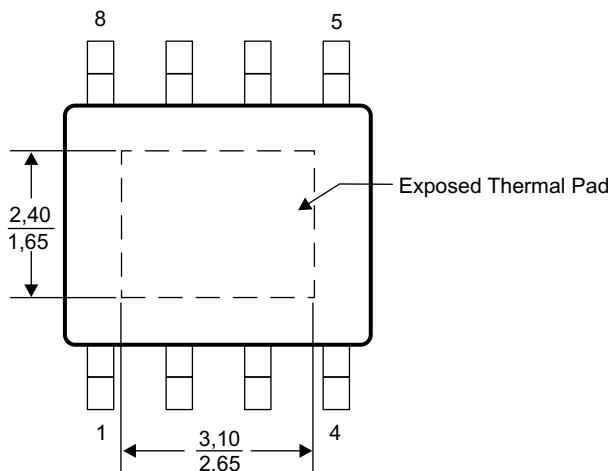
A 0.47  $\mu\text{F}$ . ceramic capacitor must be connected between the VREG5 to GND pin for proper operation. It is recommended to use a ceramic capacitor.

## THERMAL INFORMATION

This 8-pin DDA package incorporates an exposed thermal pad that is designed to be directly to an external heartsick. The thermal pad must be soldered directly to the printed board (PCB). After soldering, the PCB can be used as a heartsick. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heartsick structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the exposed thermal pad and how to use the advantage of its heat dissipating abilities, see the Technical Brief, PowerPAD™ Thermally Enhanced Package, Texas Instruments Literature No. [SLMA002](#) and Application Brief, PowerPAD™ Made Easy, Texas Instruments Literature No. [SLMA004](#).

The exposed thermal pad dimensions for this package are shown in the following illustration.



**Figure 15. Thermal Pad Dimensions**

## LAYOUT CONSIDERATIONS

1. Keep the input switching current loop as small as possible.
2. Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections should be brought from the output to the feedback pin of the device.
3. Keep analog and non-switching components away from switching components.
4. Make a single point connection from the analog ground to power ground.
5. Do not allow switching current to flow under the device.
6. Keep the pattern lines for VIN and PGND broad.
7. Exposed pad of device must be connected to PGND with solder.
8. VREG5 capacitor should be placed near the device, and connected to PGND.
9. Output capacitor should be connected to a broad pattern of the PGND.
10. Voltage feedback loop should be as short as possible, and preferably with ground shield.
11. Lower resistor of the voltage divider which is connected to the VFB pin should be tied to analog ground trace.
12. Providing sufficient via is preferable for VIN, SW and PGND connection.
13. VIN input bypass capacitor and VIN high frequency bypass capacitor must be placed as near as possible to the device.
14. Performance based on four layer printed circuit board.

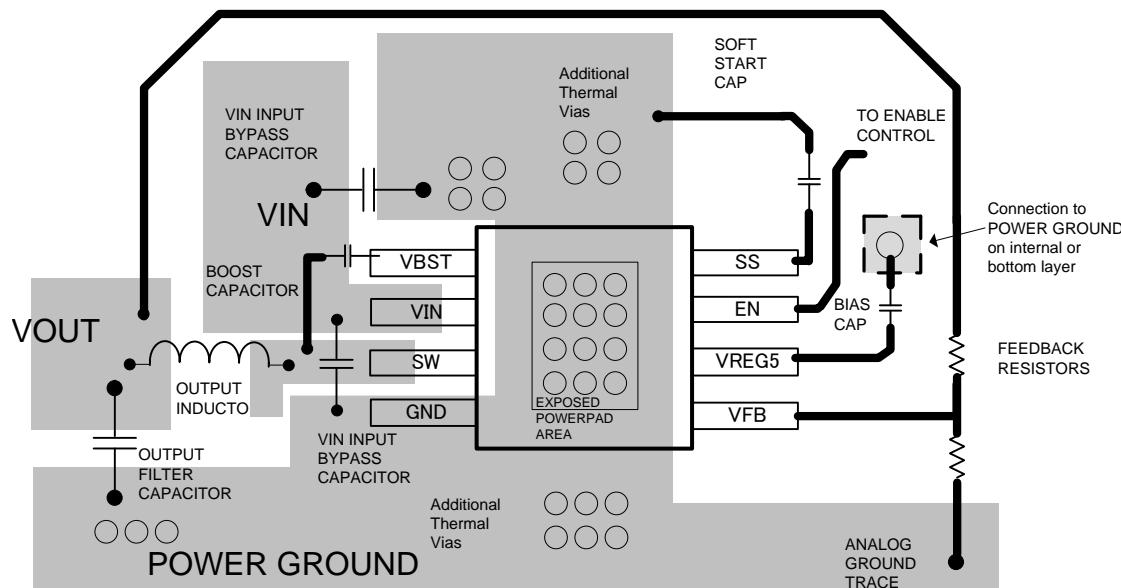


Figure 16. PCB Layout

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54339DDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	54339	<b>Samples</b>
TPS54339DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	54339	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## PACKAGE OPTION ADDENDUM

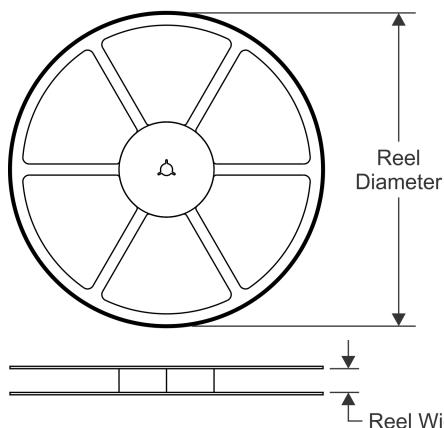
2-May-2015

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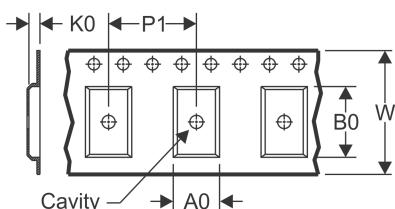
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## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

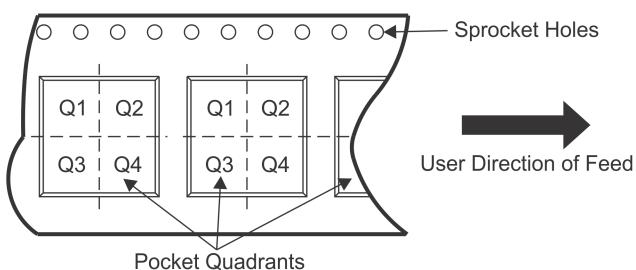


### TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

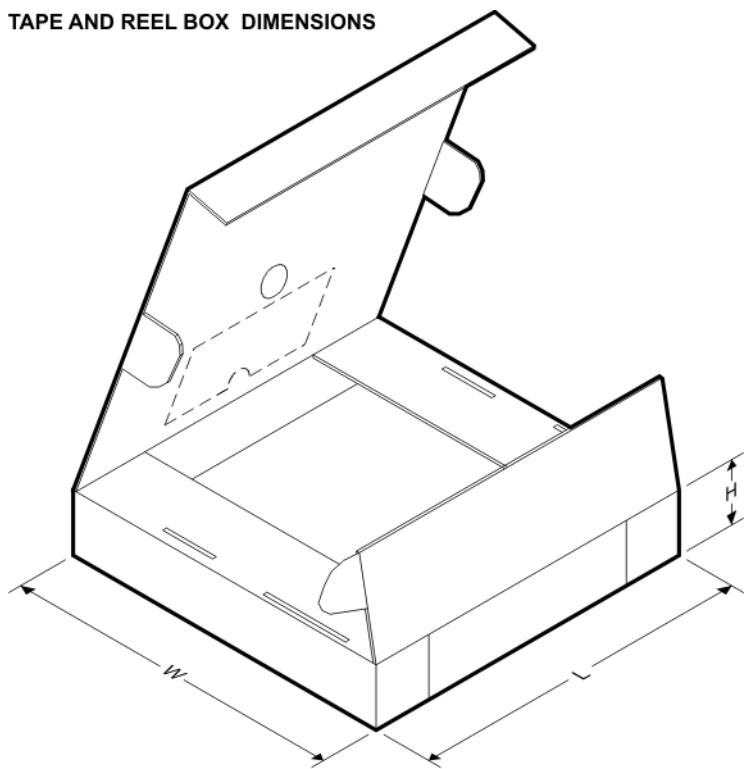
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54339DDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



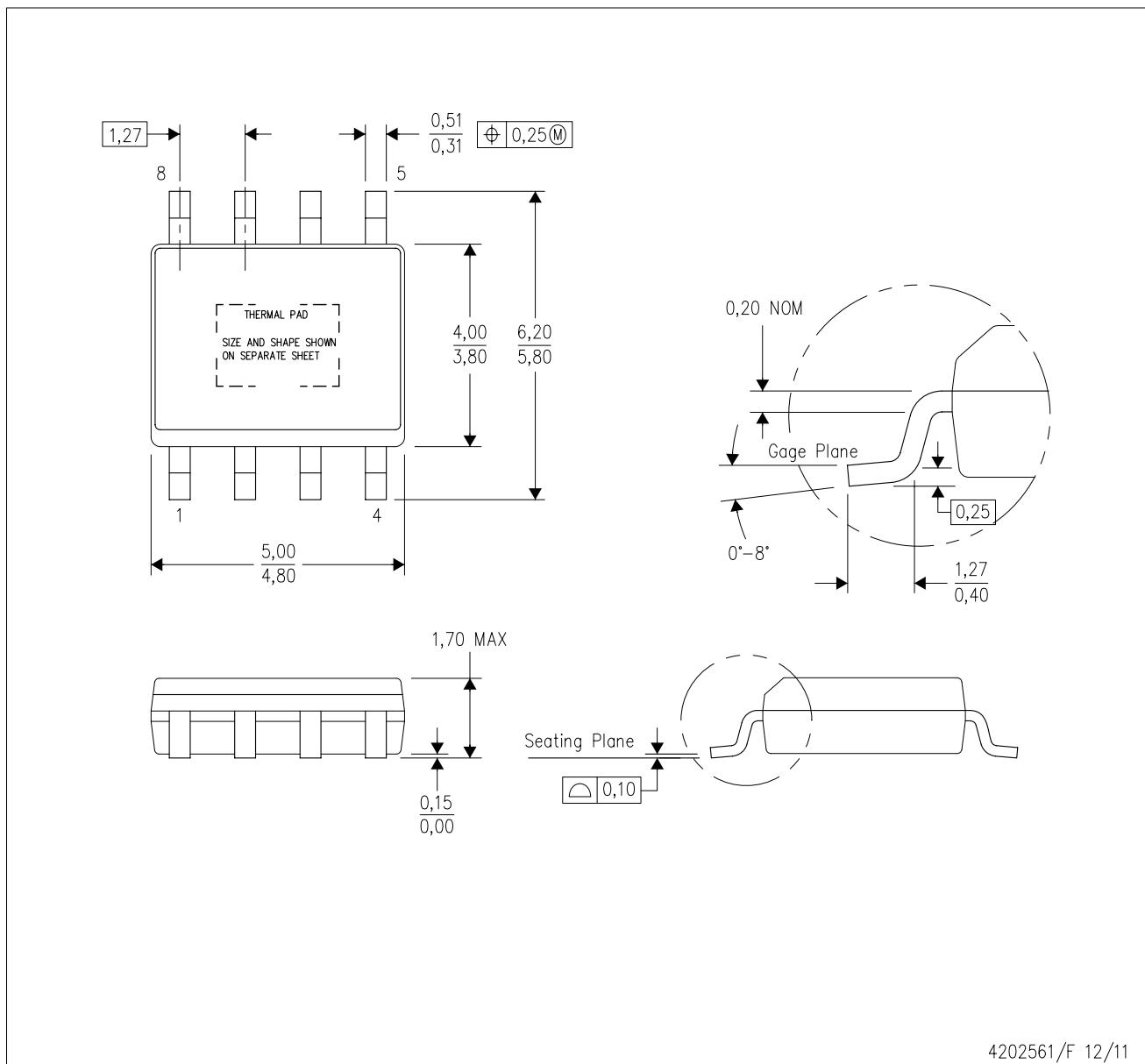
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54339DDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0

## MECHANICAL DATA

DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL-OUTLINE



4202561/F 12/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. This package complies to JEDEC MS-012 variation BA

PowerPAD is a trademark of Texas Instruments.

# THERMAL PAD MECHANICAL DATA

DDA (R-PDSO-G8)

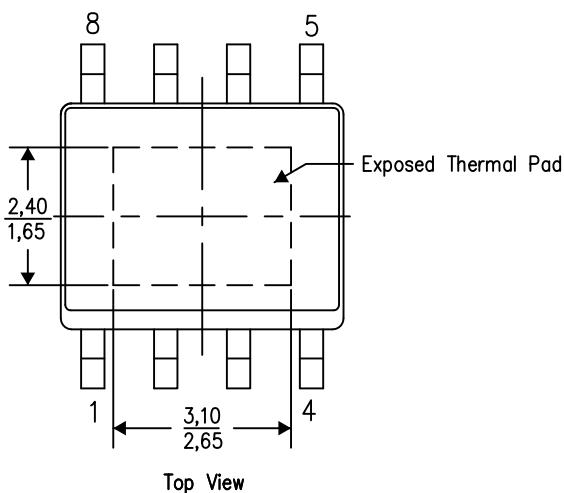
PowerPAD™ PLASTIC SMALL OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206322-6/L 05/12

NOTE: A. All linear dimensions are in millimeters

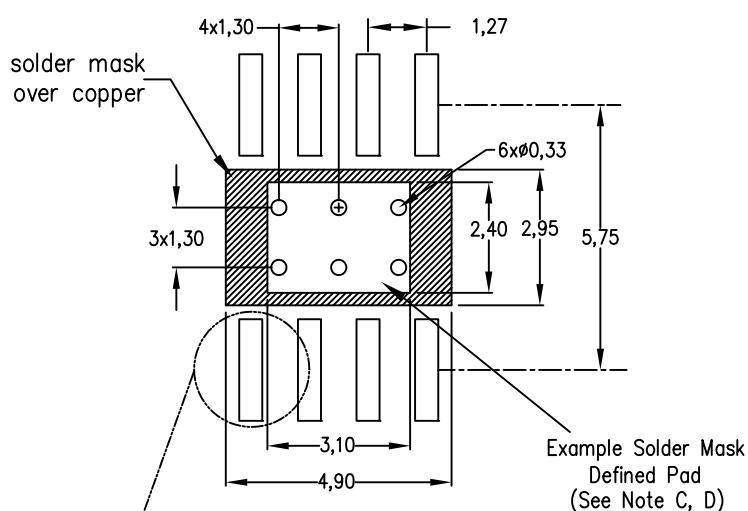
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# LAND PATTERN DATA

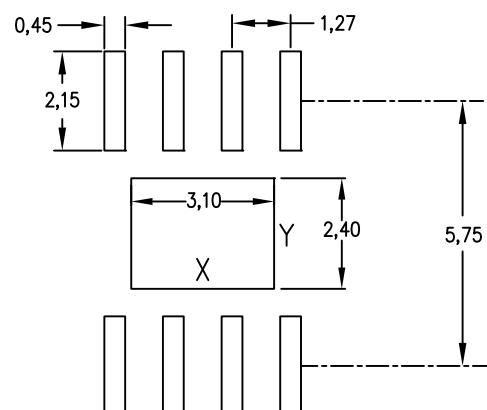
DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE

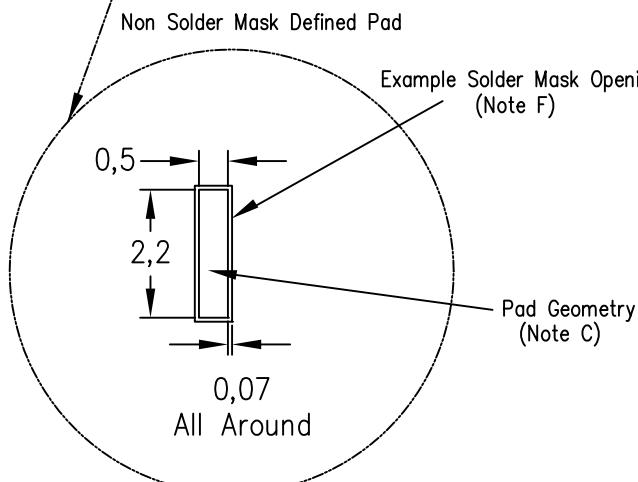
Example Board Layout  
Via pattern and copper pad size  
may vary depending on layout constraints



0,127mm Thick Stencil Design Example  
Reference table below for other  
solder stencil thicknesses  
(Note E)



Example Solder Mask  
Defined Pad  
(See Note C, D)



Example Solder Mask Opening  
(Note F)

Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

4208951-6/D 04/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>	Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>	Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>	Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>	<b>TI E2E Community</b>	
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>	<a href="http://e2e.ti.com">e2e.ti.com</a>	
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>		

## **TPS54531 5-A, 28-V Input, Step-Down SWIFT™ DC-DC Converter With Eco-mode™**

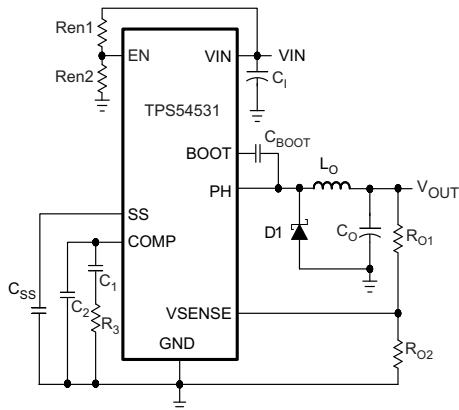
### **1 Features**

- 3.5 to 28-V Input Voltage Range
- Adjustable Output Voltage Down to 0.8 V
- Integrated 80-mΩ High-Side MOSFET Supports up to 5-A Continuous Output Current
- High Efficiency at Light Loads with a Pulse Skipping Eco-mode™
- Fixed 570kHz Switching Frequency
- Typical 1µA Shutdown Quiescent Current
- Adjustable Slow Start Limits Inrush Currents
- Programmable UVLO Threshold
- Overvoltage Transient Protection
- Cycle-by-Cycle Current-Limit, Frequency Fold Back, and Thermal Shutdown Protection
- Available in Easy-to-Use Thermally Enhanced 8-Pin SO PowerPAD™ Package

### **2 Applications**

- Consumer Applications such as Set-Top Boxes, CPE Equipment, LCD Displays, Peripherals, and Battery Chargers
- Industrial and Car Audio Power Supplies
- 5-V, 12-V and 24-V Distributed Power Systems

### **4 Simplified Schematic**



### **3 Description**

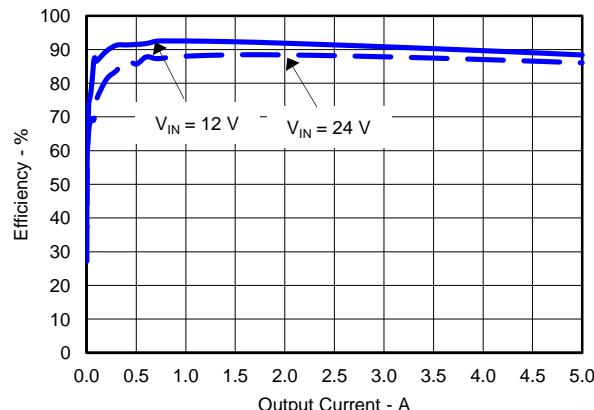
The TPS54531 device is a 28-V, 5-A non-synchronous buck converter that integrates a low  $R_{DS(on)}$  high-side MOSFET. To increase efficiency at light loads, a pulse skipping Eco-mode feature is automatically activated. Furthermore, the 1- $\mu$ A shutdown supply current allows the device to be used in battery powered applications. Current mode control with internal slope compensation simplifies the external compensation calculations and reduces component count while allowing the use of ceramic output capacitors. A resistor divider programs the hysteresis of the input under-voltage lockout. An overvoltage transient protection circuit limits voltage overshoots during startup and transient conditions. A cycle-by-cycle current-limit scheme, frequency fold back, and thermal shutdown protect the device and the load in the event of an overload condition. The TPS54531 device is available in 8-pin SO PowerPAD™ package that has been internally optimized to improve thermal performance.

#### **Device Information<sup>(1)</sup>**

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS54531	SO PowerPAD (8)	4.90 mm × 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

#### **TPS54531 Efficiency**



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

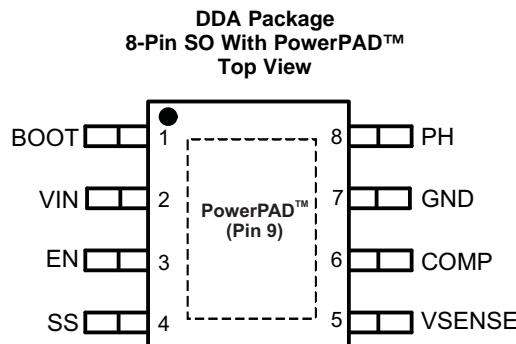
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## 5 Revision History

Changes from Original (May 2013) to Revision A	Page
• Added the <i>Handling Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> section, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	1
• Added equation for $I_{\text{ripple}}$ in the <i>Inductor Selection</i> section .....	15

## 6 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	BOOT	O	A 0.1- $\mu$ F bootstrap capacitor is required between the BOOT and PH pins. If the voltage on this capacitor falls below the minimum requirement, the high-side MOSFET is forced to switch off until the capacitor is refreshed.
2	VIN	I	This pin is the 3.5- to 28-V input supply voltage.
3	EN	I	This pin is the enable pin. To disable, pull below 1.25 V. Float this pin to enable. Programming the input undervoltage lockout with two resistors is recommended.
4	SS	I	This pin is slow-start pin. An external capacitor connected to this pin sets the output rise time.
5	VSENSE	I	This pin is the inverting node of the transconductance (gm) error amplifier.
6	COMP	O	This pin is the error-amplifier output and the input to the PWM comparator. Connect frequency compensation components to this pin.
7	GND	—	Ground pin
8	PH	O	The PH pin is the source of the internal high-side power MOSFET.
9	PowerPAD™	—	For proper operation, the GND pin must be connected to the exposed pad.

## 7 Specifications

### 7.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input Voltage	VIN	-0.3	30	V
	EN	-0.3	6	
	BOOT		38	
	VSENSE	-0.3	3	
	COMP	-0.3	3	
	SS	-0.3	3	
Output Voltage	BOOT-PH		8	V
	PH	-0.6	30	
	PH (10 ns transient from ground to negative peak)		-5	
Source Current	EN		100	µA
	BOOT		100	mA
	VSENSE		10	µA
	PH		Current Limit	A
Sink Current	VIN		Current Limit	A
	COMP		100	µA
	SS		200	
Operating Junction Temperature		-40	150	°C

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 Handling Ratings

		MIN	MAX	UNIT
T <sub>stg</sub>	Storage temperature range	-65	150	°C
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	-2	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	-1	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Operating Input Voltage on the VIN pin	3.5	28	V
T <sub>J</sub> Operating junction temperature	-40	150	°C

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		DDA 8 PINS	UNIT
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	55	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	63.2	
R <sub>θJB</sub>	Junction-to-board thermal resistance	31.5	
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	14.9	
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	31.4	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	8.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

T<sub>J</sub> = –40°C to 150°C, VIN = 3.5V to 28V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY VOLTAGE (VIN PIN)</b>					
Internal undervoltage lockout threshold	Rising and falling		3.5		V
Shutdown supply current	EN = 0V, VIN = 12V, –40°C to 85°C	1	4		µA
Operating – non-switching supply current	VSENSE = 0.85 V	110	190		µA
<b>ENABLE AND UVLO (EN PIN)</b>					
Enable threshold	Rising and falling	1.25	1.35		V
Input current	Enable threshold – 50 mV	–1			µA
Input current	Enable threshold + 50 mV	–4			µA
<b>VOLTAGE REFERENCE</b>					
Voltage reference		0.772	0.8	0.828	V
<b>HIGH-SIDE MOSFET</b>					
On resistance	BOOT-PH = 3 V, VIN = 3.5 V	115	200		mΩ
	BOOT-PH = 6 V, VIN = 12 V	80	150		
<b>ERROR AMPLIFIER</b>					
Error amplifier transconductance (gm)	–2 µA < I <sub>(COMP)</sub> < 2 µA, V <sub>(COMP)</sub> = 1 V	92			µmhos
Error amplifier DC gain <sup>(1)</sup>	VSENSE = 0.8 V	800			V/V
Error amplifier unity gain bandwidth <sup>(1)</sup>	5 pF capacitance from COMP to GND pins	2.7			MHz
Error amplifier source/sink current	V <sub>(COMP)</sub> = 1 V, 100-mV overdrive	±7			µA
Switch current to COMP transconductance <sup>(1)</sup>	VIN = 12 V	20			A/V
<b>SWITCHING FREQUENCY</b>					
Switching Frequency	VIN = 12V, 25°C	456	570	684	kHz
Minimum controllable on time	VIN = 12V, 25°C		105	130	ns
Maximum controllable duty ratio <sup>(1)</sup>	BOOT-PH = 6 V	90%	93%		
<b>PULSE SKIPPING Eco-mode™</b>					
Pulse skipping Eco-mode switch current threshold		160			mA
<b>CURRENT LIMIT</b>					
Current-limit threshold	VIN = 12 V	6.3	10.5		A
<b>THERMAL SHUTDOWN</b>					
Thermal Shutdown		165			°C
<b>SLOW START (SS PIN)</b>					
Charge current	V <sub>(SS)</sub> = 0.4 V	2			µA

(1) Specified by design

## 7.6 Typical Characteristics

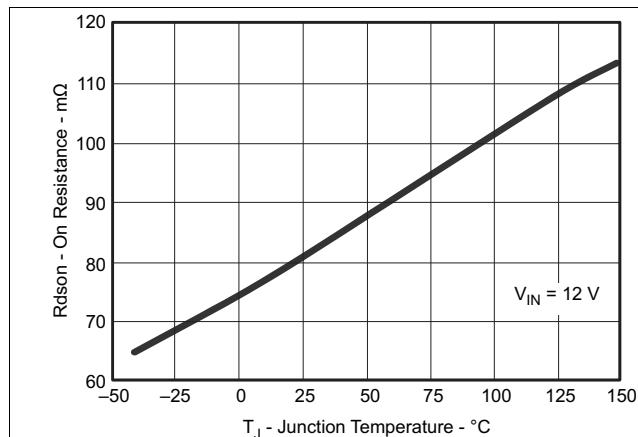


Figure 1. ON Resistance vs Junction Temperature

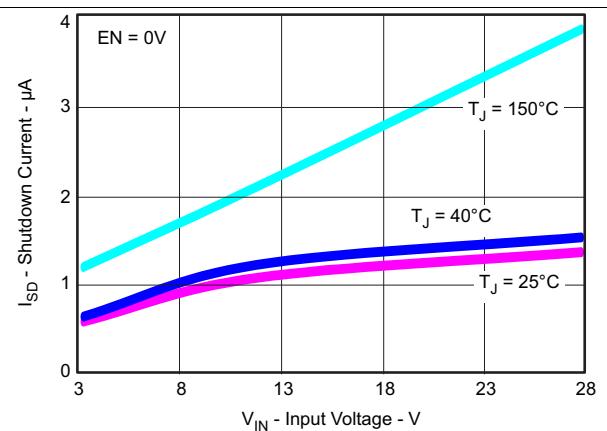


Figure 2. Shutdown Quiescent Current vs Input Voltage

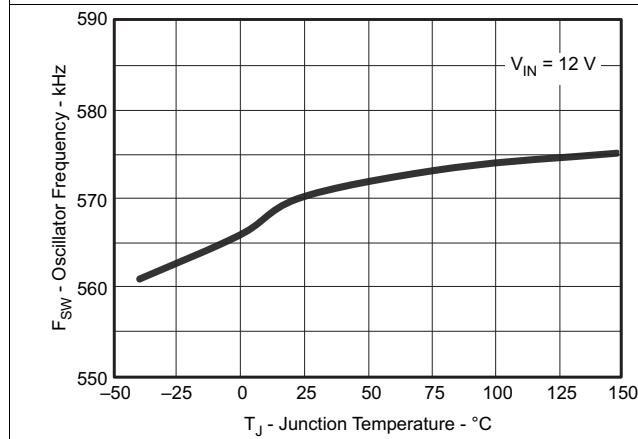


Figure 3. Switching Frequency vs Junction Temperature

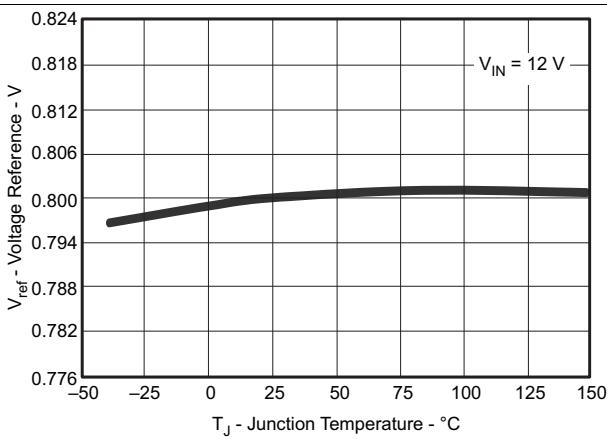


Figure 4. Voltage Reference vs Junction Temperature

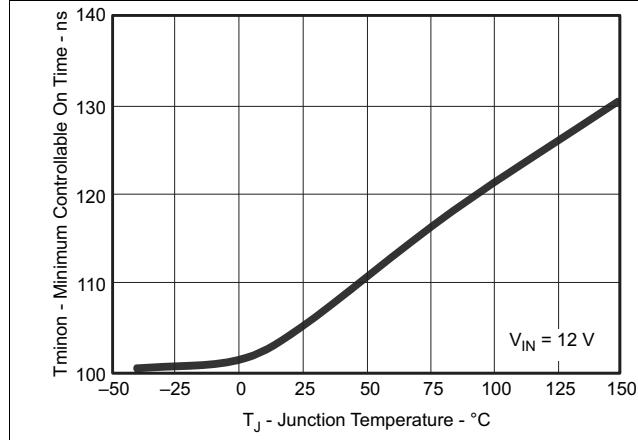


Figure 5. Minimum Controllable ON Time vs Junction Temperature

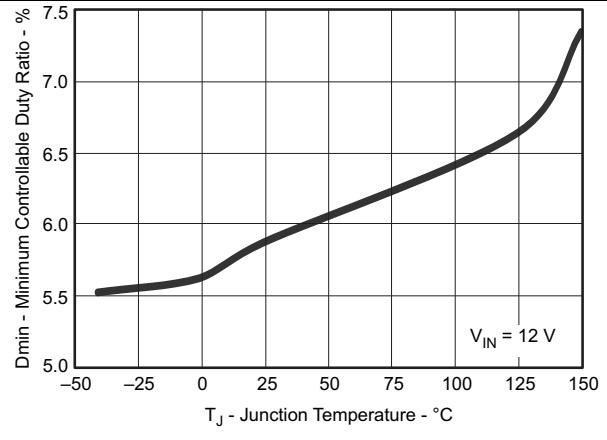
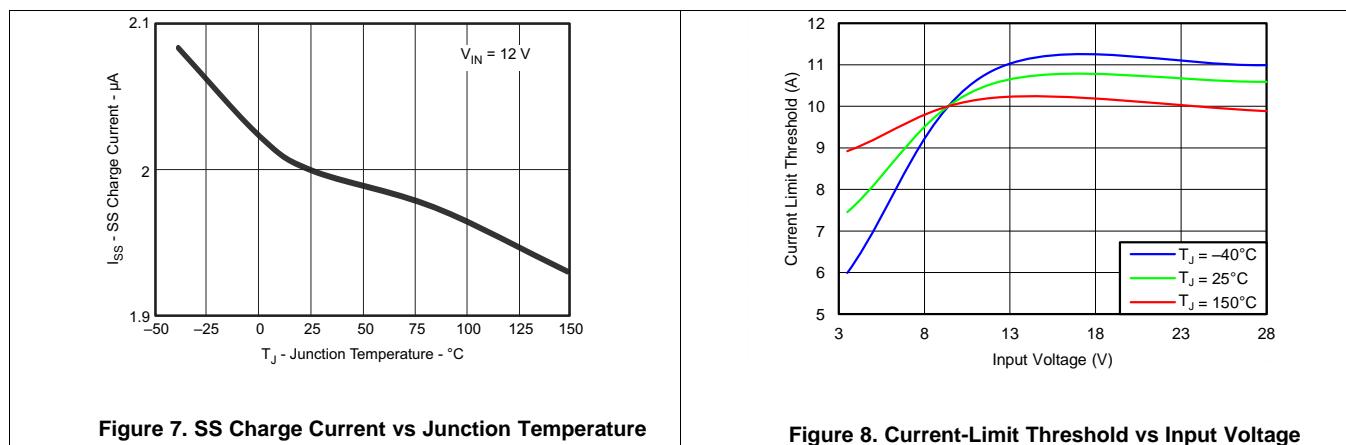


Figure 6. Minimum Controllable Duty Ratio vs Junction Temperature

## Typical Characteristics (continued)



## 8 Detailed Description

### 8.1 Overview

The TPS54531 device is a 28-V, 5-A, step-down (buck) converter with an integrated high-side n-channel MOSFET. To improve performance during line and load transients, the device implements a constant-frequency, current mode control which reduces output capacitance and simplifies external frequency compensation design. The TPS54531 device has a preset switching frequency of 570 kHz.

The TPS54531 device requires a minimum input voltage of 3.5 V for normal operation. The EN pin has an internal pullup current source that can be used to adjust the input-voltage undervoltage lockout (UVLO) with two external resistors. In addition, the pullup current provides a default condition when the EN pin is floating for the device to operate. The operating current is 110  $\mu$ A (typical) when not switching and under no load. When the device is disabled, the supply current is 1  $\mu$ A (typical).

The integrated 80-m $\Omega$  high-side MOSFET allows for high-efficiency power-supply designs with continuous output currents up to 5 A.

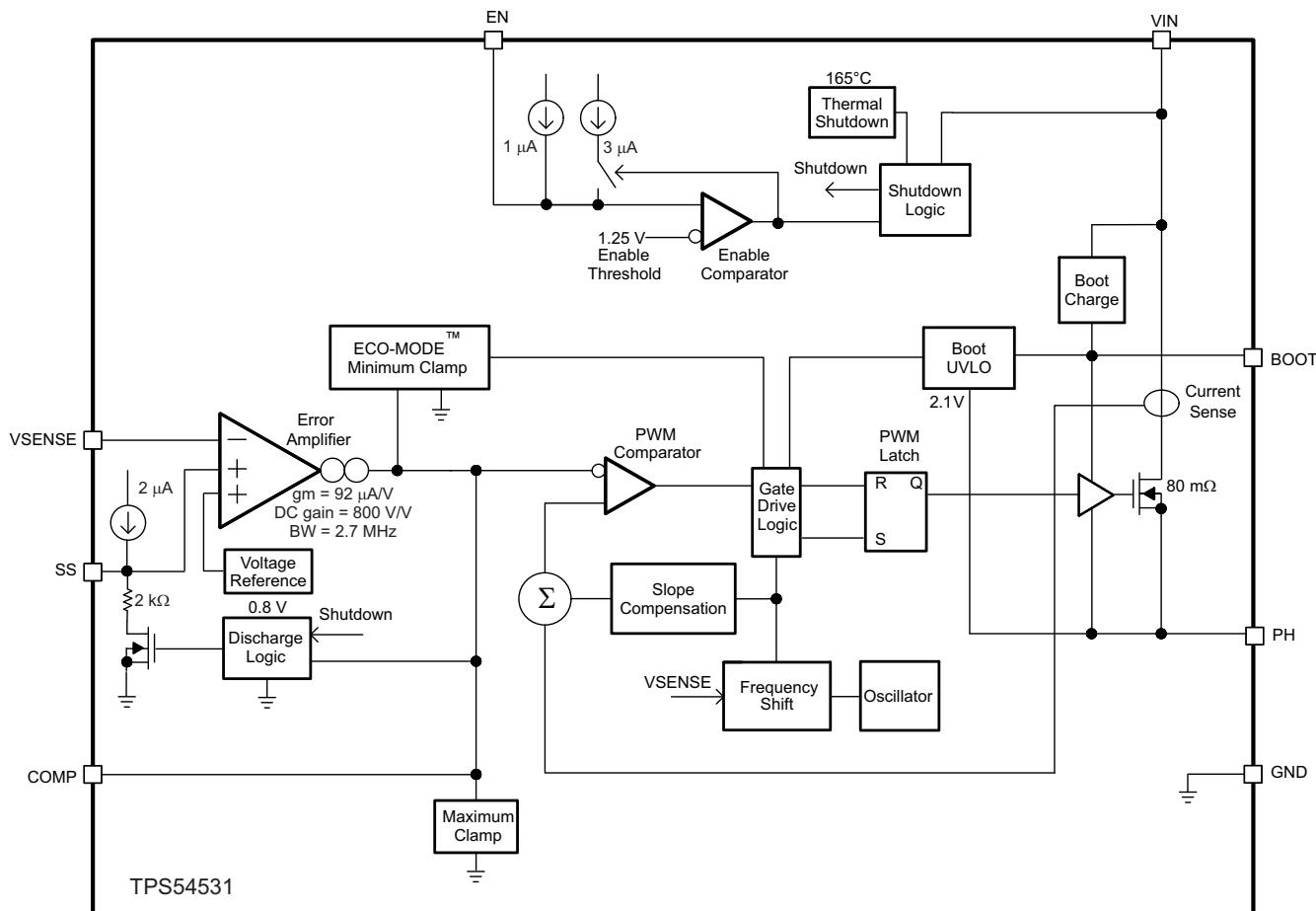
The TPS54531 device reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high-side MOSFET is supplied by an external capacitor on the BOOT to PH pin. The boot capacitor voltage is monitored by an UVLO circuit and turns the high-side MOSFET off when the voltage falls below a preset threshold of 2.1 V (typical). The output voltage can be stepped down to as low as the reference voltage.

By adding an external capacitor, the slow-start time of the TPS54531 device can be adjustable which enables flexible output filter selection.

To improve the efficiency at light load conditions, the TPS54531 device enters a special pulse skipping Eco-mode when the peak inductor current drops below 160 mA (typical).

The frequency foldback reduces the switching frequency during startup and overcurrent conditions to help control the inductor current. The thermal shut down provides the additional protection under fault conditions.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Fixed-Frequency PWM Control

The TPS54531 device uses a fixed-frequency, peak-current mode control. The internal switching frequency of the TPS54531 device is fixed at 570 kHz.

### 8.3.2 Voltage Reference ( $V_{ref}$ )

The voltage reference system produces a  $\pm 2\%$  initial accuracy voltage reference ( $\pm 3.5\%$  over temperature) by scaling the output of a temperature stable bandgap circuit. The typical voltage reference is designed at 0.8 V.

### 8.3.3 Bootstrap Voltage (BOOT)

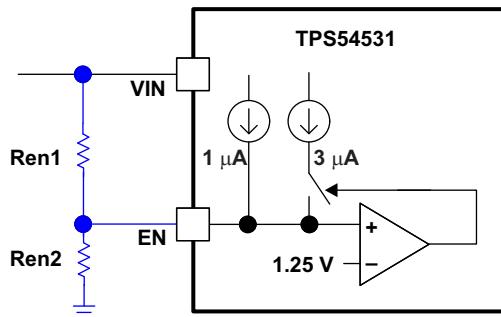
The TPS54531 device has an integrated boot regulator and requires a 0.1- $\mu$ F ceramic capacitor between the BOOT and PH pins to provide the gate-drive voltage for the high-side MOSFET. A ceramic capacitor with an X7R- or X5R-grade dielectric is recommended because of the stable characteristics over temperature and voltage. To improve drop out, the TPS54531 device is designed to operate at 100% duty cycle as long as the BOOT-to-PH pin voltage is greater than 2.1 V (typical).

### 8.3.4 Enable and Adjustable Input Undervoltage Lockout (VIN UVLO)

The EN pin has an internal pullup current-source that provides the default condition of the TPS54531 device while operating when the EN pin floats.

## Feature Description (continued)

The TPS54531 device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. Using an external VIN UVLO to add at least 500-mV hysteresis is recommended unless the VIN voltage is greater than ( $V_{OUT} + 2$  V). To adjust the VIN UVLO with hysteresis, use the external circuitry connected to the EN pin as shown in [Figure 9](#). When the EN pin voltage exceeds 1.25 V, an additional 3  $\mu$ A of hysteresis is added. Use [Equation 1](#) and [Equation 2](#) to calculate the resistor values required for the desired VIN UVLO threshold voltages. The  $V_{STOP}$  should always be greater than 3.5 V.



**Figure 9. Adjustable Input Undervoltage Lockout**

$$Ren1 = \frac{V_{START} - V_{STOP}}{3 \mu\text{A}}$$

where

- $V_{START}$  is the input start threshold voltage
  - $V_{STOP}$  is the input stop threshold voltage
- (1)

$$Ren2 = \frac{V_{EN}}{\frac{V_{START} - V_{EN}}{Ren1} + 1 \mu\text{A}}$$

where

- $V_{EN}$  is the enable threshold voltage of 1.25 V
- (2)

The external start and stop voltages are approximate. The actual start and stop voltages may vary.

### 8.3.5 Programmable Slow Start Using SS Pin

Programming the slow-start time externally is highly recommended because no slow-start time is implemented internally. The TPS54531 device effectively uses the lower voltage of the internal voltage reference or the SS pin voltage as the reference voltage of the power supply that is fed into the error amplifier and regulates the output accordingly. A capacitor ( $C_{SS}$ ) on the SS pin to ground implements a slow-start time. The TPS54531 device has an internal pullup current source of 2  $\mu$ A that charges the external slow-start capacitor. Use [Equation 3](#) to calculate the slow-start time (10% to 90%).

$$T_{SS} (\text{ms}) = \frac{C_{SS} (\text{nF}) \times V_{ref} (\text{V})}{I_{SS} (\mu\text{A})}$$

where

- $V_{ref} = 0.8$  V
  - $I_{SS} = 2 \mu\text{A}$
- (3)

The slow-start time should be set between 1 ms to 10 ms to ensure good startup behavior. The value slow-start capacitor should not exceed 27 nF.

During normal operation, the TPS54531 device stops switching if the input voltage drops below the VIN UVLO threshold, the EN pin is pulled below 1.25 V, or a thermal shutdown event occurs.

## Feature Description (continued)

### 8.3.6 Error Amplifier

The TPS54531 device has a transconductance amplifier for the error amplifier. The error amplifier compares the VSENSE voltage to the internal effective voltage reference presented at the input of the error amplifier. The transconductance of the error amplifier is 92  $\mu\text{A}/\text{V}$  during normal operation. Frequency compensation components are connected between the COMP pin and ground.

### 8.3.7 Slope Compensation

In order to prevent the sub-harmonic oscillations when operating the device at duty cycles greater than 50%, the TPS54531 device adds a built-in slope compensation which is a compensating ramp to the switch-current signal.

### 8.3.8 Current-Mode Compensation Design

The device is able to work with various types of output capacitors with appropriate compensation designs. For designs using ceramic output capacitors, proper derating of ceramic output capacitance is recommended when performing the stability analysis because the actual ceramic capacitance drops considerably from the nominal value when the applied voltage increases. For the detailed guidelines, see the *Detailed Design Procedure* section.

### 8.3.9 Overcurrent Protection and Frequency Shift

The TPS54531 device implements current mode control that uses the COMP pin voltage to turn off the high-side MOSFET on a cycle-by-cycle basis. During each cycle the switch current and the COMP pin voltage are compared. When the peak inductor current intersects the COMP pin voltage, the high-side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP pin high, causing the switch current to increase. The COMP pin has a maximum clamp internally, which limits the output current.

The TPS54531 device provides robust protection during short circuits. Overcurrent runaway is possible in the output inductor during a short circuit at the output. The TPS54531 device solves this issue by increasing the off time during short-circuit conditions by lowering the switching frequency. The switching frequency is divided by 1, 2, 4, and 8 as the voltage ramps from 0 V to 0.8 V on VSENSE pin. The relationship between the switching frequency and the VSENSE pin voltage is listed in [Table 1](#).

**Table 1. Switching Frequency Conditions**

SWITCHING FREQUENCY	VSENSE PIN VOLTAGE
570 kHz	$\text{VSENSE} \geq 0.6 \text{ V}$
570 kHz / 2	$0.6 \text{ V} > \text{VSENSE} \geq 0.4 \text{ V}$
570 kHz / 4	$0.4 \text{ V} > \text{VSENSE} \geq 0.2 \text{ V}$
570 kHz / 8	$0.2 \text{ V} > \text{VSENSE}$

### 8.3.10 Overvoltage Transient Protection

The TPS54531 device incorporates an overvoltage transient-protection (OVTP) circuit to minimize output voltage overshoot when recovering from output fault conditions or strong unload transients. The OVTP circuit includes an overvoltage comparator to compare the VSENSE pin voltage and internal thresholds. When the VSENSE pin voltage goes above  $109\% \times V_{\text{ref}}$ , the high-side MOSFET is forced off. When the VSENSE pin voltage falls below  $107\% \times V_{\text{ref}}$ , the high-side MOSFET is enabled again.

### 8.3.11 Thermal Shutdown

The device implements an internal thermal shutdown to protect the device if the junction temperature exceeds 165°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. When the die temperature decreases below 165°C, the device reinitiates the power-up sequence.

## 8.4 Device Functional Modes

### 8.4.1 Eco-mode™

The TPS54531 is designed to operate in pulse skipping Eco-mode at light load currents to boost light load efficiency. When the peak inductor current is lower than 160 mA (typical), the COMP pin voltage falls to 0.5 V (typical) and the device enters Eco-mode. When the device is in Eco-mode, the COMP pin voltage is clamped at 0.5-V internally which prevents the high-side integrated MOSFET from switching. The peak inductor current must rise above 160 mA for the COMP pin voltage to rise above 0.5 V and exit Eco-mode. Because the integrated current comparator catches the peak inductor current only, the average load current entering Eco-mode varies with the applications and external output filters.

### 8.4.2 Operation With $V_{IN} < 3.5$ V

The device is recommended to operate with input voltages above 3.5 V. The typical VIN UVLO threshold is not specified and the device can operate at input voltages down to the UVLO voltage. At input voltages below the actual UVLO voltage, the device does not switch. If the EN pin is externally pulled up or left floating, the device becomes active when the VIN pin passes the UVLO threshold. Switching begins when the slow-start sequence is initiated.

### 8.4.3 Operation With EN Control

The enable threshold voltage is 1.25 V (typical). With the EN pin held below that voltage the device is disabled and switching is inhibited even if the VIN pin is above the UVLO threshold. The IC quiescent current is reduced in this state. If the EN voltage increases above the threshold while the VIN pin is above the UVLO threshold, the device becomes active. Switching is enabled, and the slow-start sequence is initiated.

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

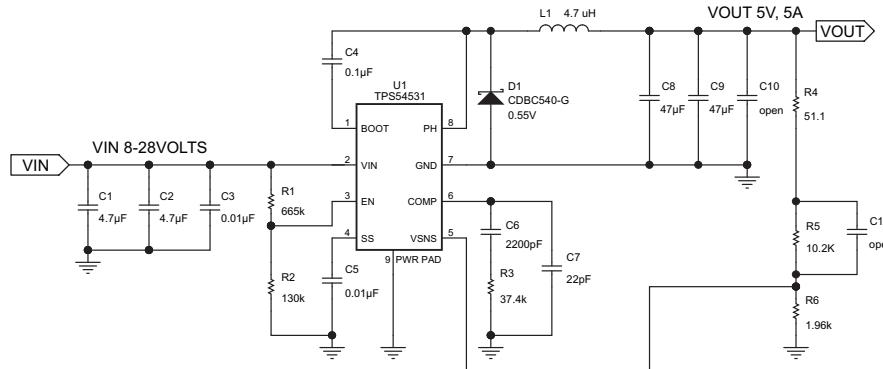
### 9.1 Application Information

The TPS54531 device is typically used as a step-down converter, which converts a voltage from 3.5 V to 28 V to a lower voltage. WEBENCH® software is available to aid in the design and analysis of circuits.

For additional design needs, see the following devices:

	<b>TPS54231</b>	<b>TPS54232</b>	<b>TPS54233</b>	<b>TPS54531</b>	<b>TPS54332</b>
I(max)	2 A	2 A	2 A	5 A	3.5 A
Input voltage range	3.5 to 28 V				
Switching frequency (typ)	570 kHz	1000 kHz	285 kHz	570 kHz	1000 kHz
Switch current limit (min)	2.3 A	2.3 A	2.3 A	5.5 A	4.2 A
Pin and package	8SOIC	8SOIC	8SOIC	8SO PowerPAD™	8SO PowerPAD™

### 9.2 Typical Application



**Figure 10. Typical Application Schematic**

#### 9.2.1 Design Requirements

For this design example, use the values listed in [Table 2](#) as the input parameters

**Table 2. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	8 to 28 V
Output voltage	5 V
Transient response, 2.5-A load step	$\Delta V_{OUT} = \pm 5\%$
Input ripple voltage	400 mV
Output ripple voltage	30 mV
Output current rating	5 A
Operating Frequency	570 kHz

## 9.2.2 Detailed Design Procedure

The following design procedure can be used to select component values for the TPS54531 device. Alternately, the WEBENCH software can be used to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

### 9.2.2.1 Switching Frequency

The switching frequency for the TPS54531 is fixed at 570 kHz.

### 9.2.2.2 Output Voltage Set Point

The output voltage of the TPS54531 device is externally adjustable using a resistor divider network. As shown in [Figure 10](#), this divider network is comprised of R5 and R6. The relationship of the output voltage to the resistor divider is given by [Equation 4](#) and [Equation 5](#):

$$R_6 = \frac{R_5 \times V_{ref}}{V_{OUT} - V_{ref}} \quad (4)$$

$$V_{OUT} = V_{ref} \times \left[ \frac{R_5}{R_6} + 1 \right] \quad (5)$$

Select a value of R5 to be approximately 10 kΩ. Slightly increasing or decreasing the value of R5 can result in closer output-voltage matching when using standard value resistors. In this design, R5 = 10.2 kΩ and R6 = 1.96 kΩ, resulting in a 4.96 V output voltage. The 51.1-Ω resistor, R4, is provided as a convenient location to break the control loop for stability testing.

### 9.2.2.3 Undervoltage Lockout Set Point

The undervoltage lockout (UVLO) can be adjusted using the external voltage divider network of R1 and R2. R1 is connected between the VIN and EN pins of the TPS54531 device and R2 is connected between the EN and GND pins. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. For the design example, the minimum input voltage is 8 V. Therefore the start voltage threshold is set to 7 V with 2-V hysteresis. Use [Equation 1](#) and [Equation 2](#) to calculate the values for the upper and lower resistor values of R1 and R2.

### 9.2.2.4 Input Capacitors

The TPS54531 device requires an input decoupling capacitor and, depending on the application, a bulk input capacitor. The typical recommended value for the decoupling capacitor is 10 µF. A high-quality ceramic type X5R or X7R is recommended. The voltage rating should be greater than the maximum input voltage. A smaller value can be used as long as all other requirements are met; however 10 µF has been shown to work well in a wide variety of circuits. Additionally, some bulk capacitance may be required, especially if the TPS54531 circuit is not located within about 2 inches from the input voltage source. The value for this capacitor is not critical but should be rated to handle the maximum input voltage including ripple voltage, and should filter the output so that input ripple voltage is acceptable. For this design two 4.7-µF capacitors are used for the input decoupling capacitor. The capacitors are X7R dielectric rated for 50 V. The equivalent series resistance (ESR) is approximately 2 mΩ and the current rating is 3 A. Additionally, a small 0.01 µF capacitor is included for high frequency filtering.

Use [Equation 6](#) to calculate the input ripple voltage.

$$\Delta V_{IN} = \frac{I_{O(MAX)} \times 0.25}{C_{BULK} \times f_{sw}} + (I_{O(MAX)} \times ESR_{MAX}) \quad (6)$$

where

- $I_{O(MAX)}$  is the maximum load current
- $C_{BULK}$  is the bulk capacitor value
- $f_{sw}$  is the switching frequency
- $ESR_{MAX}$  is the maximum series resistance of the bulk capacitor

The maximum RMS ripple current must also be checked. For worst case conditions, use [Equation 7](#) to calculate the maximum-RMS input ripple current,  $I_{CIN(RMS)}$ .

$$I_{CIN(RMS)} = \frac{I_{O(MAX)}}{2} \quad (7)$$

In this case, the input ripple voltage is 243 mV and the RMS ripple current is 2.5 A.

#### NOTE

The actual input voltage ripple is greatly affected by parasitics associated with the layout and the output impedance of the voltage source.

The actual input voltage ripple for this circuit is listed in [Table 2](#) and is larger than the calculated value. This measured value is still below the specified input limit of 300 mV. The maximum voltage across the input capacitors would be  $V_{IN(MAX)} + \Delta V_{IN} / 2$ . The selected bulk and bypass capacitors are each rated for 50 V and the ripple current capacity is greater than 3 A, both providing ample margin. The maximum ratings for voltage and current must not be exceeded under any circumstance.

### 9.2.2.5 Output Filter Components

Two components must be selected for the output filter,  $L_{OUT}$  and  $C_{OUT}$ . Because the TPS54531 is an externally compensated device, a wide range of filter component types and values can be supported.

#### 9.2.2.5.1 Inductor Selection

To calculate the minimum value of the output inductor, use [Equation 8](#)

$$L_{MIN} = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times K_{IND} \times I_{OUT} \times f_{SW}} \quad (8)$$

where

- $K_{IND}$  is a coefficient that represents the amount of inductor ripple current relative to the maximum output current

In general, this value is at the discretion of the designer; however, the following guidelines may be used. For designs using low-ESR output capacitors such as ceramics, a value as high as  $K_{IND} = 0.3$  may be used. When using higher ESR output capacitors,  $K_{IND} = 0.2$  yields better results.

For this design example, use  $K_{IND} = 0.3$  and the minimum inductor value is calculated as 4.8  $\mu$ H. For this design, a close, standard value was chosen: 4.7  $\mu$ H.

For the output filter inductor, do not exceed the RMS current and saturation current ratings. Use [Equation 9](#) to calculate the inductor ripple current ( $I_{ripple}$ ).

$$I_{ripple} = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times L_{OUT} \times f_{SW} \times 0.8} \quad (9)$$

Use [Equation 10](#) to calculate the RMS inductor current.

$$I_{L(RMS)} = \sqrt{I_{O(MAX)}^2 + \frac{1}{12} \times \left( \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times L_{OUT} \times f_{SW} \times 0.8} \right)^2} \quad (10)$$

Use [Equation 11](#) to calculate the peak inductor current.

$$I_{L(PK)} = I_{O(MAX)} + \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{1.6 \times V_{IN(MAX)} \times L_{OUT} \times f_{SW}} \quad (11)$$

For this design, the RMS inductor current is 5.03 A and the peak inductor current is 5.96 A. The selected inductor is a Wurth 4.7  $\mu$ H. This inductor has a saturation current rating of 19 A and an RMS current rating of 7 A, which meets these requirements. Smaller or larger inductor values can be used depending on the amount of ripple current the designer wants to allow, so long as the other design requirements are met. Larger value inductors have lower AC current and result in lower output voltage ripple, while smaller inductor values will increase AC current and output voltage ripple. In general, inductor values for use with the TPS54531 device are in the range of 1  $\mu$ H to 47  $\mu$ H.

#### 9.2.2.5.2 Capacitor Selection

Selecting the value of the output capacitor is based on three primary considerations. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance must be selected based on the more stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The output capacitor must supply the load with current when the regulator can not. This situation occurs if desired hold-up times occur for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily not able to supply sufficient output current if a large, fast increase occurs in the current needs of the load, such as a transition from no load to full load. The regulator usually requires two or more clock cycles for the control loop to respond to the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of drop in the output voltage. Use [Equation 12](#) to calculate minimum output capacitance ( $C_O$ ) required in this case.

$$C_O > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}}$$

where

- $\Delta I_{OUT}$  is the change in output current
  - $f_{SW}$  is the switching frequency of the regulator
  - $\Delta V_{OUT}$  is the allowable change in the output voltage
- (12)

For this example, the transient load response is specified as a 5% change in  $V_{OUT}$  for a load step of 2.5 A. For this example,  $\Delta I_{OUT} = 2.5$  A and  $\Delta V_{OUT} = 0.05 \times 5 = 0.25$  V. Using these values results in a minimum capacitance of 35  $\mu$ F. This value does not consider the ESR of the output capacitor in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

Use [Equation 13](#) to calculate the minimum output capacitance needed to meet the output voltage ripple specification. In this case, the maximum output voltage ripple is 30 mV. Under this requirement [Equation 13](#), yields 14  $\mu$ F.

$$C_O > \frac{1}{8 \times f_{SW}} \times \frac{1}{\frac{V_{OUTripple}}{I_{ripple}}}$$

where

- $f_{SW}$  is the switching frequency
  - $V_{OUTripple}$  is the maximum allowable output voltage ripple
  - $I_{ripple}$  is the inductor ripple current
- (13)

Use [Equation 14](#) to calculate the maximum ESR an output capacitor can have to meet the output-voltage ripple specification. [Equation 14](#) indicates the ESR should be less than 15.6 m $\Omega$ . In this case, the ESR of the ceramic capacitor is much smaller than 15.6 m $\Omega$ .

$$R_{ESR} < \frac{V_{OUTripple}}{I_{ripple}}$$
(14)

Additional capacitance deratings for aging, temperature, and DC bias should be considered which increases this minimum value. For this example, two 47- $\mu$ F 10-V X5R ceramic capacitors with 3 m $\Omega$  of ESR are used. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the RMS (root mean square) value of the maximum ripple current. Use [Equation 15](#) to calculate the RMS ripple current that the output capacitor must support. For this application, [Equation 15](#) yields 554 mA.

$$I_{COUT(RMS)} = \frac{1}{\sqrt{12}} \times \left( \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times L_{OUT} \times f_{SW} \times N_C} \right) \quad (15)$$

### 9.2.2.6 Compensation Components

Several possible methods exist to design closed loop compensation for DC-DC converters. For the ideal current mode control, the design equations can be easily simplified. The power stage gain is constant at low frequencies, and rolls off at –20 dB/decade above the modulator pole frequency. The power stage phase is 0 degrees at low frequencies and begins to fall one decade below the modulator pole frequency reaching a minimum of –90 degrees one decade above the modulator pole frequency. Use [Equation 16](#) to calculate the modulator pole frequency.

$$f_{p\_mod} = \frac{I_{O(MAX)}}{2\pi \times V_{OUT} \times C_{OUT}} \quad (16)$$

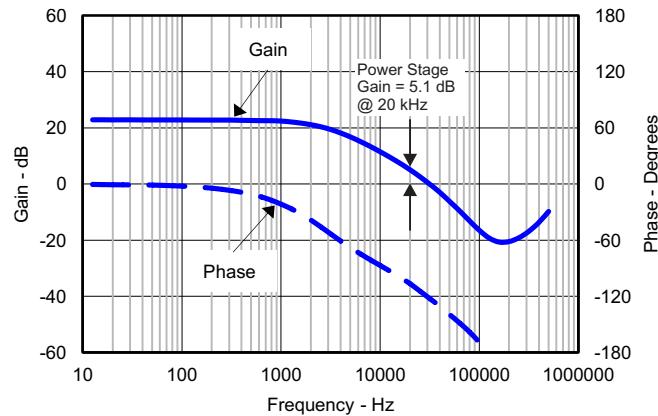
For the TPS54531 device, most circuits have relatively high amounts of slope compensation. As more slope compensation is applied, the power stage characteristics deviate from the ideal approximations. The phase loss of the power stage will now approach –180 degrees, making compensation more difficult. The power stage transfer function can be solved but it requires a tedious calculation. Use the PSpice model to accurately model the power-stage gain and phase so that a reliable compensation circuit can be designed. Alternately, a direct measurement of the power stage characteristics can be used. That is the technique used in this design procedure. For this design, the calculated values are as follows:

L1 = 4.7  $\mu$ H

C8 and C9 = 47  $\mu$ F (each)

ESR = 3 m $\Omega$

[Figure 11](#) shows the power stage characteristics.



**Figure 11. Power Stage Gain and Phase Characteristics**

For this design, the intended crossover frequency is 20 kHz. From the power stage gain and phase plots, the gain at 20 kHz is 5.1 dB and the phase is about –100 degrees. For 60 degrees of phase margin, additional phase boost from a feed-forward capacitor in parallel with the upper resistor of the voltage set point divider is not needed. R3 sets the gain of the compensated error amplifier to be equal and opposite the power stage gain at crossover. Use [Equation 17](#) to calculate the required value of R3.

$$R3 = \frac{10}{\frac{-G_{PWRSTG}}{gm_{ea}}} \times \frac{V_{OUT}}{V_{ref}} \quad (17)$$

To maximize phase gain, the compensator zero is placed one decade below the crossover frequency of 20 kHz. Use [Equation 18](#) to calculate the required value for C6.

$$C6 = \frac{1}{2 \cdot \pi \cdot R3 \cdot \frac{F_{CO}}{10}} \quad (18)$$

To maximize phase gain the high frequency pole is placed one decade above the crossover frequency of 20 kHz. The pole can also be useful to offset the ESR of aluminum electrolytic output capacitors. Use [Equation 19](#) to calculate the value for C7.

$$C7 = \frac{1}{2 \cdot \pi \cdot R3 \cdot 10 \cdot F_{CO}} \quad (19)$$

For this design, the calculated values are as follows:

$$R3 = 37.4 \text{ k}\Omega$$

$$C6 = 2200 \text{ pF}$$

$$C7 = 22 \text{ pF}$$

### 9.2.2.7 Bootstrap Capacitor

Every TPS54531 design requires a bootstrap capacitor, C4. The bootstrap capacitor value must be 0.1  $\mu\text{F}$ . The bootstrap capacitor is located between the PH and BOOT pins. The bootstrap capacitor should be a high-quality ceramic type with X7R or X5R grade dielectric for temperature stability.

### 9.2.2.8 Catch Diode

The TPS54531 device is designed to operate using an external catch diode between the PH and GND pins. The selected diode must meet the absolute maximum ratings for the application. The reverse voltage must be higher than the maximum voltage at the PH pin, which is  $V_{IN(MAX)} + 0.5 \text{ V}$ . Peak current must be greater than  $I_{O(MAX)}$  plus on half the peak-to-peak inductor current. The forward-voltage drop should be small for higher efficiencies. The catch diode conduction time is (typically) longer than the high-side FET on time, so attention paid to diode parameters can make a marked improvement in overall efficiency. Additionally, check that the selected device is capable of dissipating the power losses. For this design, a CDBC540-G was selected, with a reverse voltage of 40 V, forward current of 5 A, and a forward-voltage drop of 0.55 V.

### 9.2.2.9 Slow-Start Capacitor

The slow-start capacitor determines the minimum amount of time required for the output voltage to reach the nominal programmed value during power up which is useful if a load requires a controlled voltage slew rate. The slow-start capacitor is also used if the output capacitance is very large and requires large amounts of current to quickly charge the capacitor to the output voltage level. The large currents necessary to charge the capacitor may make the TPS54531 device reach the current limit. Excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output voltage slew rate solves both of these problems. Use [Equation 3](#) to calculate the value of the slow-start capacitor. For the example circuit, the slow-start time is not too critical because the output capacitor value is  $2 \times 47 \mu\text{F}$  which does not require much current to charge to 5 V. The example circuit has the slow-start time set to an arbitrary value of 4 ms which requires a 10-nF capacitor. For the TPS54531 device,  $I_{SS}$  is 2  $\mu\text{A}$  and  $V_{ref}$  is 0.8 V.

### 9.2.2.10 Output Voltage Limitations

Because of the internal design of the TPS54531 device, any given voltage has both upper and lower output voltage limits for any given input voltage. The upper limit of the output-voltage set point is constrained by the maximum duty cycle of 91% and is calculated with [Equation 20](#). The equation assumes the maximum ON resistance for the internal high-side FET.

$$V_{O(MAX)} = 0.91 \times ((V_{IN(MIN)} - I_{O(MAX)} \times R_{DS(on)max}) + V_D) - (I_{O(MAX)} \times R_L) - V_D$$

where

- $V_{IN(MIN)}$  = Minimum input voltage
  - $I_{O(MAX)}$  = Maximum load current
  - $V_D$  = Catch diode forward voltage
  - $R_L$  = Output inductor series resistance
- (20)

The lower limit is constrained by the minimum controllable on time which may be as high as 130 ns. The approximate minimum output voltage for a given input voltage and minimum load current is given by [Equation 21](#).

$$V_{O(MIN)} = 0.089 \times ((V_{IN(MAX)} - I_{O(MIN)} \times R_{DS(on)min}) + V_D) - (I_{O(MIN)} \times R_L) - V_D$$

where

- $V_{IN(MAX)}$  = Maximum input voltage
  - $I_{O(MIN)}$  = Minimum load current
  - $V_D$  = Catch diode forward voltage
  - $R_L$  = Output inductor series resistance
- (21)

This equation assumes nominal on-resistance for the high-side FET and accounts for worst case variation of operating frequency set point. Any design operating near the operational limits of the device should be carefully checked to ensure proper functionality.

### 9.2.2.11 Power Dissipation Estimate

The following formulas show how to estimate the device power dissipation under continuous-conduction mode (CCM) operations. These formulas should not be used if the device is working in the discontinuous-conduction mode (DCM) or pulse-skipping Eco-mode™.

The device power dissipation includes:

1. Conduction loss:

$$P_{con} = I_{OUT}^2 \times R_{DS(on)} \times V_{OUT} / V_{IN}$$

where

- $I_{OUT}$  is the output current (A)
- $R_{DS(on)}$  is the on-resistance of the high-side MOSFET ( $\Omega$ )
- $V_{OUT}$  is the output voltage (V)
- $V_{IN}$  is the input voltage (V)

2. Switching loss:

$$P_{sw} = 0.5 \times 10^{-9} \times V_{IN}^2 \times I_{OUT} \times f_{sw}$$

where

- $f_{sw}$  is the switching frequency (Hz)

3. Gate charge loss:

$$P_{gc} = 22.8 \times 10^{-9} \times f_{sw}$$

4. Quiescent current loss:

$$P_q = 0.11 \times 10^{-3} \times V_{IN}$$

Therefore:

$$P_{tot} = P_{con} + P_{sw} + P_{gc} + P_q$$

where

- $P_{tot}$  is the total device power dissipation (W)

For given  $T_A$ :

$$T_J = T_A + R_{th} \times P_{tot}$$

where

- $T_J$  is the junction temperature ( $^{\circ}\text{C}$ )
- $T_A$  is the ambient temperature ( $^{\circ}\text{C}$ )
- $R_{th}$  is the thermal resistance of the package ( $^{\circ}\text{C}/\text{W}$ )

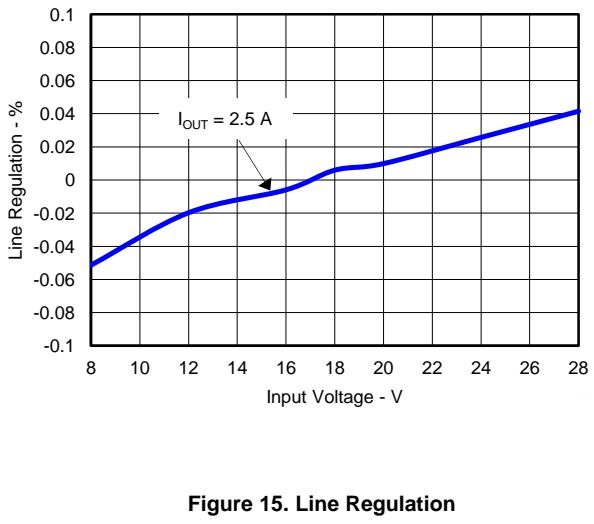
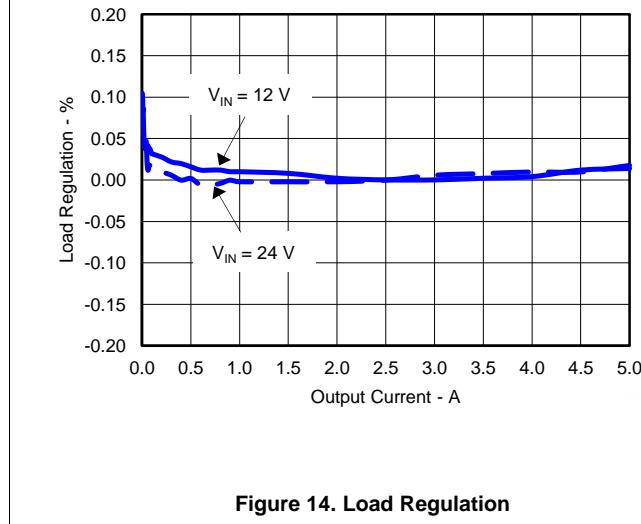
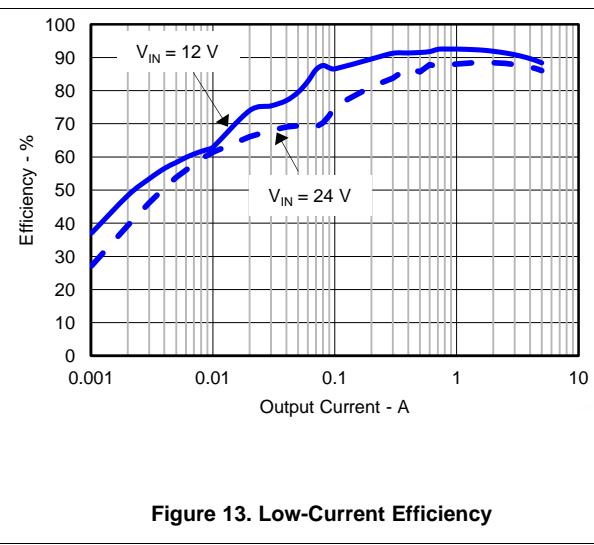
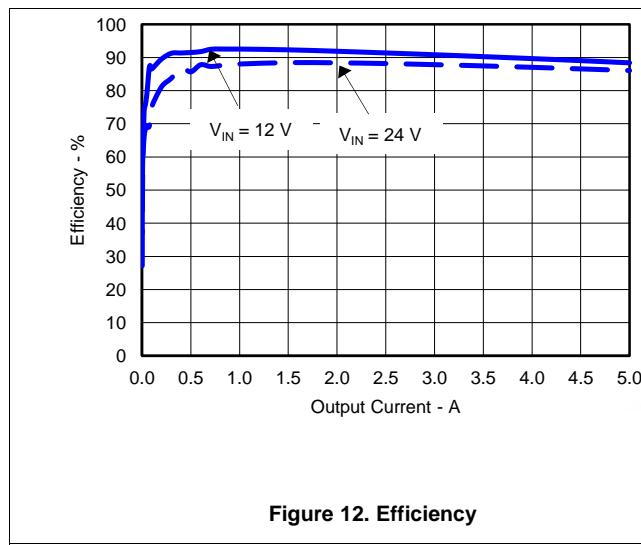
For given  $T_{JMAX} = 150^{\circ}\text{C}$ :

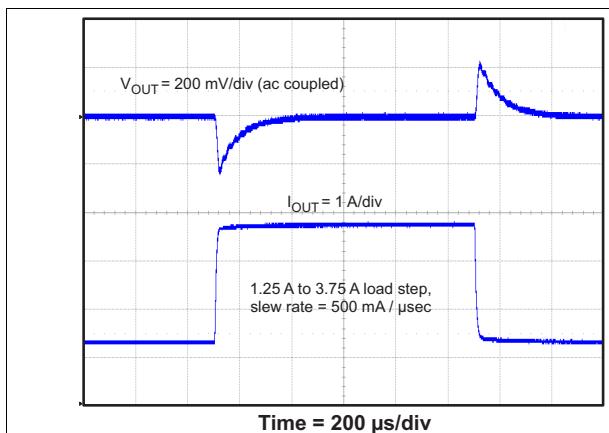
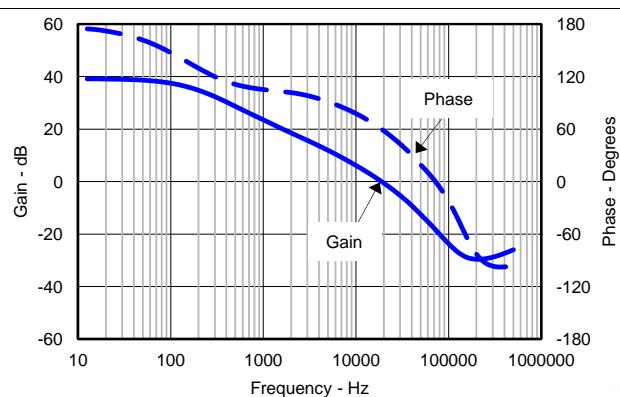
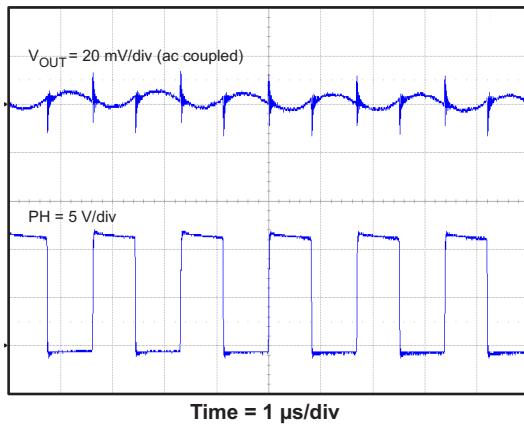
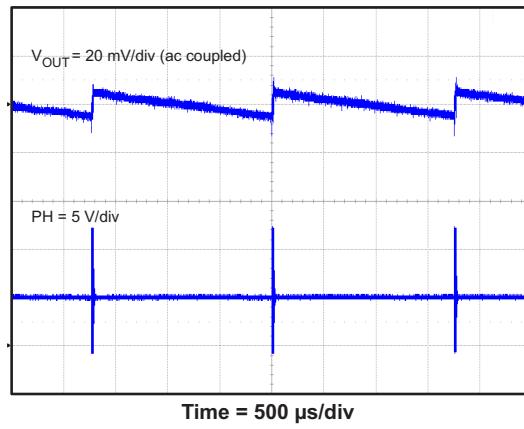
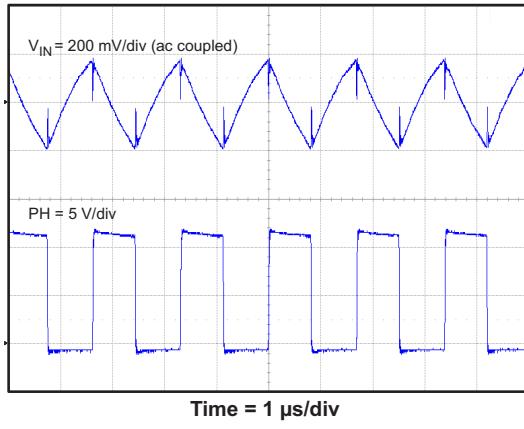
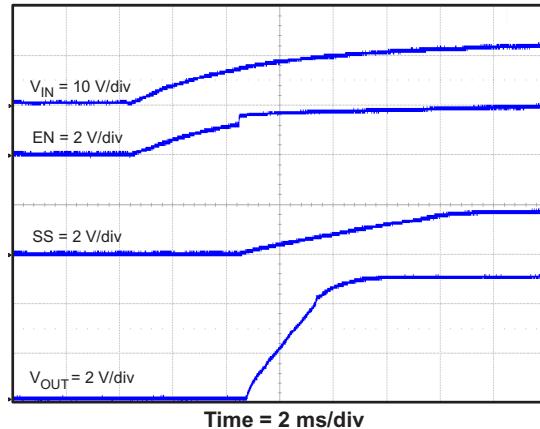
$$T_{AMAX} = T_{JMAX} - R_{th} \times P_{tot}$$

where

- $T_{JMAX}$  is maximum junction temperature ( $^{\circ}\text{C}$ )
- $T_{AMAX}$  is maximum ambient temperature ( $^{\circ}\text{C}$ )

### 9.2.3 Application Curves




**Figure 16. Transient Response**

**Figure 17. Loop Response**

**Figure 18. Full-Load Output Ripple**

**Figure 19. Eco-mode Output Ripple**

**Figure 20. Full-Load Input Ripple**

**Figure 21. Startup Relative to VIN**

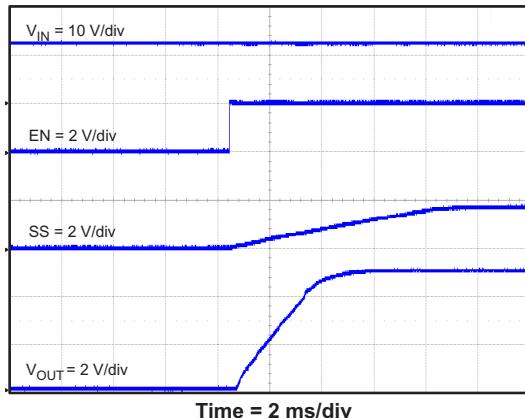


Figure 22. Startup Relative to Enable

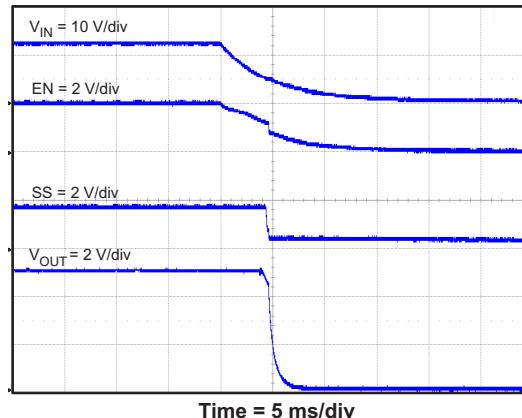


Figure 23. Shut Down Relative to VIN

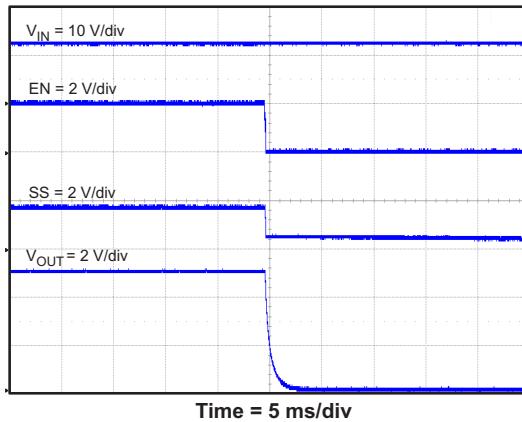


Figure 24. Shut Down Relative to EN

## 10 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range between 3.5 V and 28 V. This input supply should be well regulated. If the input supply is located more than a few inches from the converter additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 100  $\mu$ F is a typical choice.

## 11 Layout

### 11.1 Layout Guidelines

The VIN pin should be bypassed to ground with a low-ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the anode of the catch diode. The typical recommended bypass capacitance is 10- $\mu$ F ceramic with a X5R or X7R dielectric and the optimum placement is closest to the VIN pins and the source of the anode of the catch diode. Figure 25 shows a PCB layout example. The GND pin should be tied to the PCB ground plane at the pin of the device. The PH pin should be routed to the cathode of the catch diode and to the output inductor. Because the PH connection is the switching node, the catch diode and output inductor should be located very close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. For operation at full rated load, the exposed thermal pad should be soldered directly to the top-side ground area under the device. Use thermal vias

## Layout Guidelines (continued)

to connect the top-side ground area to an internal or bottom-layer ground plane. The total copper area must provide adequate heat dissipation. Additional vias adjacent to the device can be used to improve heat transfer to the internal or bottom-layer ground plane . The additional external components can be placed approximately as shown. Obtaining acceptable performance with alternate layout schemes may be possible, however this layout has been shown to produce good results and is intended as a guideline.

### 11.2 Layout Example

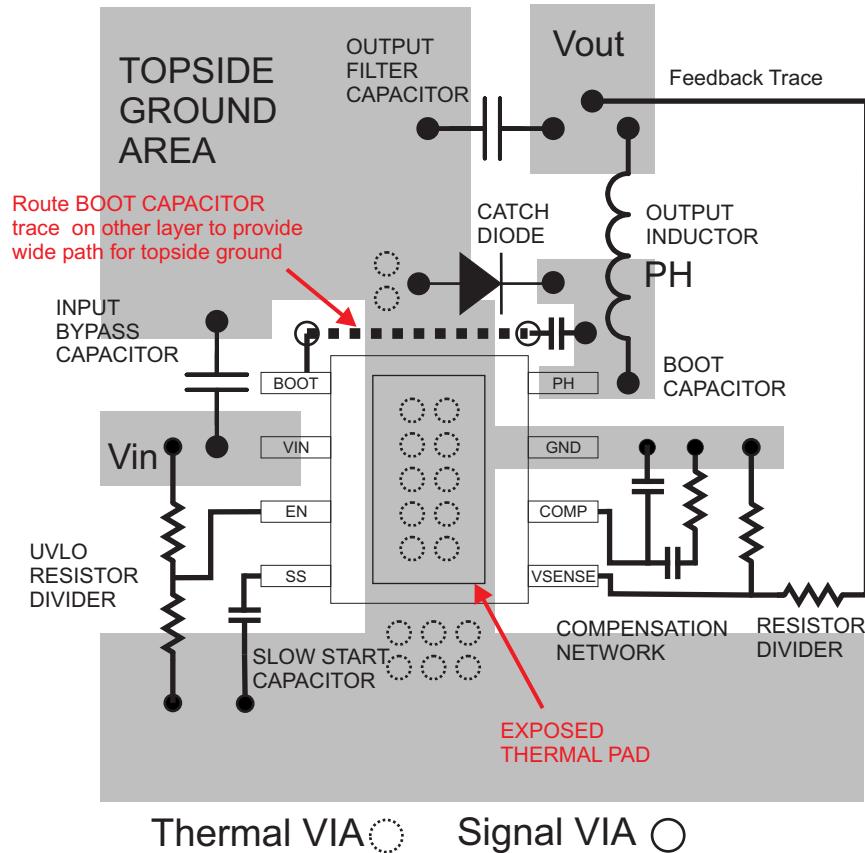


Figure 25. TPS54531DDA Board Layout

### 11.3 Electromagnetic Interference (EMI) Considerations

As EMI becomes a rising concern in more and more applications, the internal design of the TPS54531 device includes features to reduce the EMI. The high-side MOSFET gate drive is designed to reduce the PH pin voltage ringing. The internal IC rails are isolated to decrease the noise sensitivity. A package bond wire scheme is used to lower the parasitics effects.

To achieve the best EMI performance, external component selection and board layout are equally important. Follow the steps listed in the [Detailed Design Procedure](#) section to prevent potential EMI issues.

## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 Development Support

For the WEBENCH Software Tool, go to [www.TI.com/WEBENCH](http://www.TI.com/WEBENCH).

### 12.2 Trademarks

Eco-mode, PowerPAD are trademarks of Texas Instruments.

WEBENCH is a registered trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.4 Glossary

[SLYZ022 — TI Glossary](#).

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54531DDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	54531	<b>Samples</b>
TPS54531DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	54531	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## PACKAGE OPTION ADDENDUM

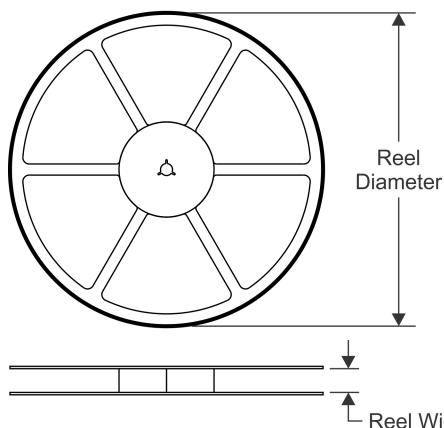
27-Oct-2014

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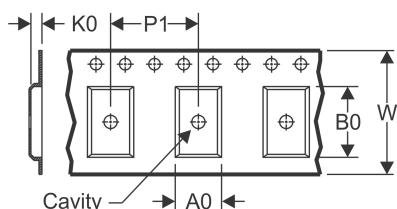
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

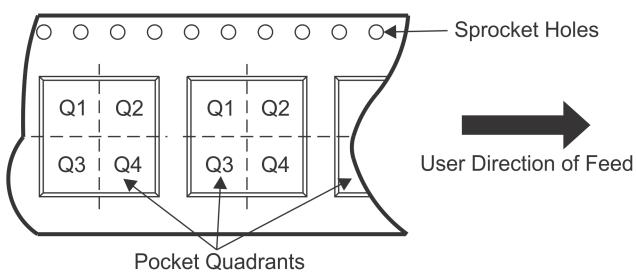


### TAPE DIMENSIONS



$A_0$	Dimension designed to accommodate the component width
$B_0$	Dimension designed to accommodate the component length
$K_0$	Dimension designed to accommodate the component thickness
$W$	Overall width of the carrier tape
$P_1$	Pitch between successive cavity centers

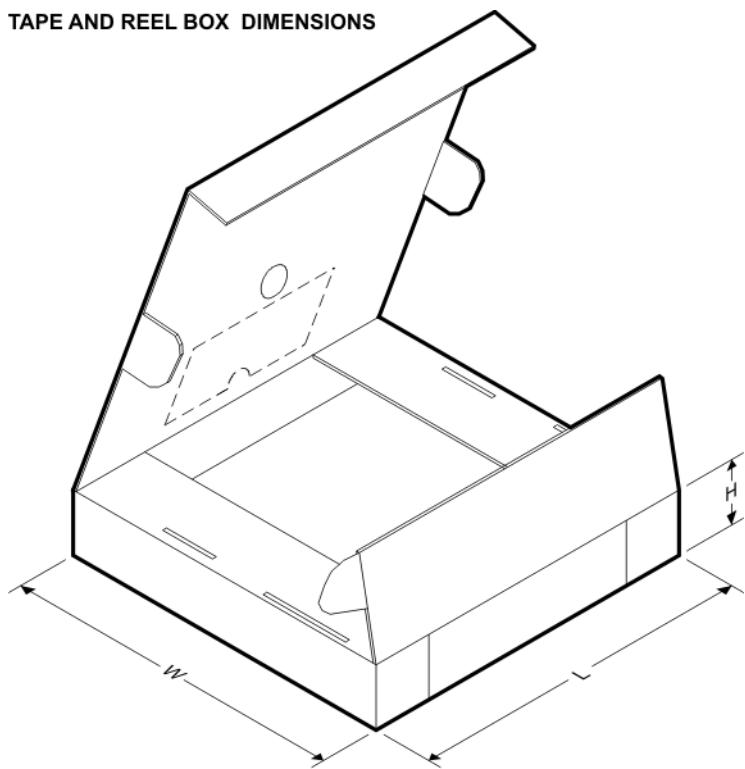
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	$A_0$ (mm)	$B_0$ (mm)	$K_0$ (mm)	$P_1$ (mm)	$W$ (mm)	Pin1 Quadrant
TPS54531DDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



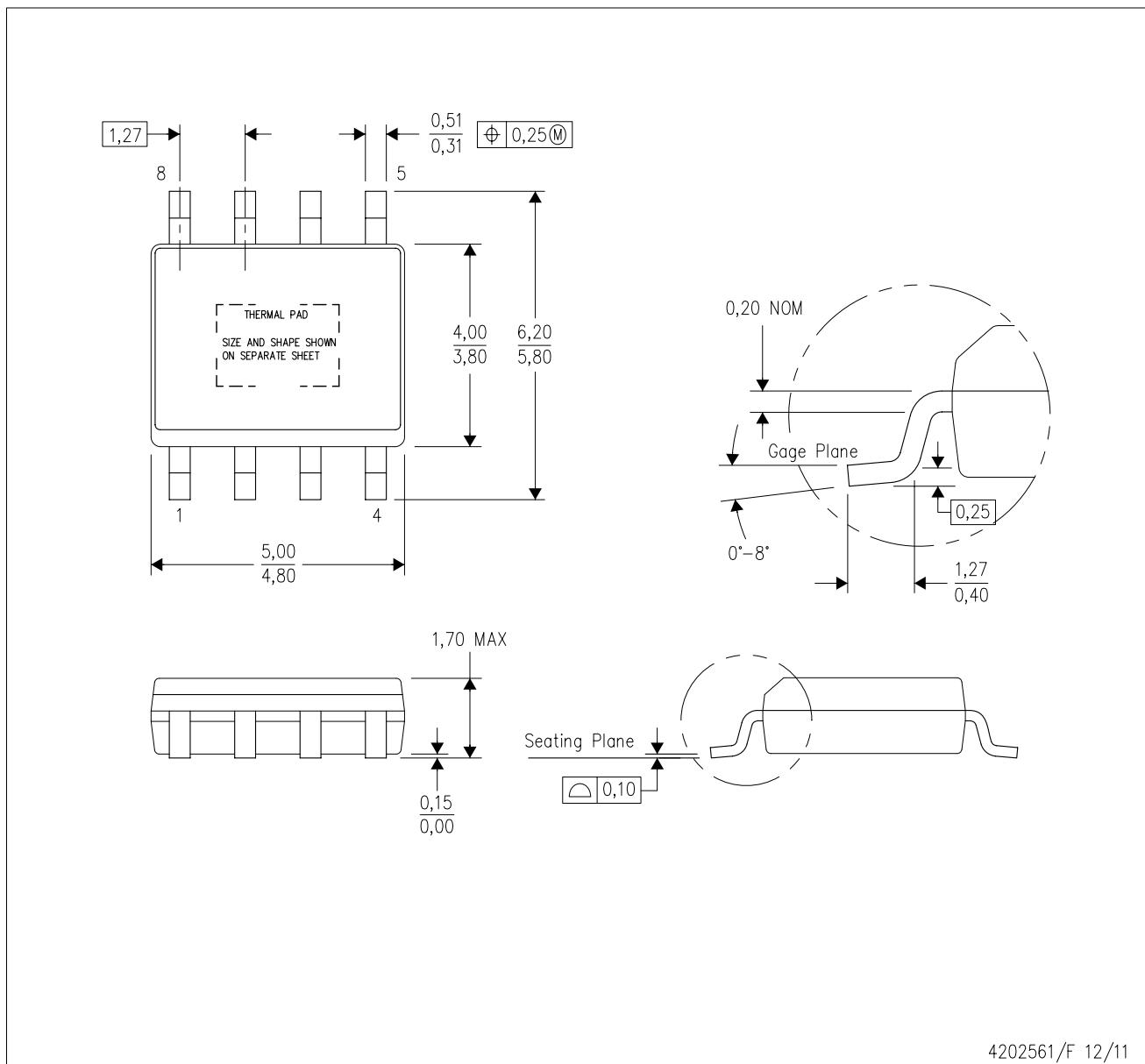
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54531DDAR	SO PowerPAD	DDA	8	2500	364.0	364.0	27.0

## MECHANICAL DATA

DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL-OUTLINE



4202561/F 12/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - This package complies to JEDEC MS-012 variation BA

PowerPAD is a trademark of Texas Instruments.

# THERMAL PAD MECHANICAL DATA

DDA (R-PDSO-G8)

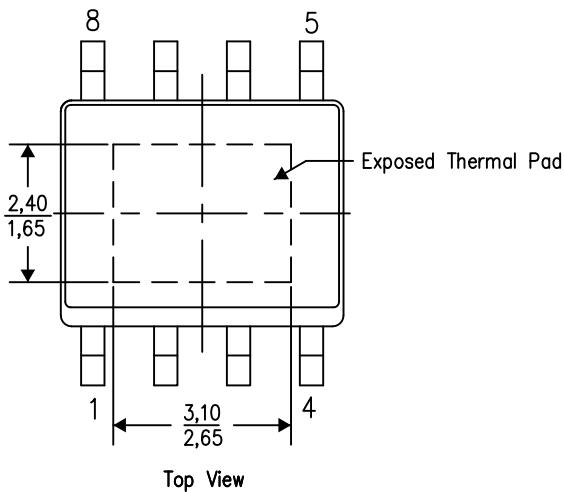
PowerPAD™ PLASTIC SMALL OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206322-6/L 05/12

NOTE: A. All linear dimensions are in millimeters

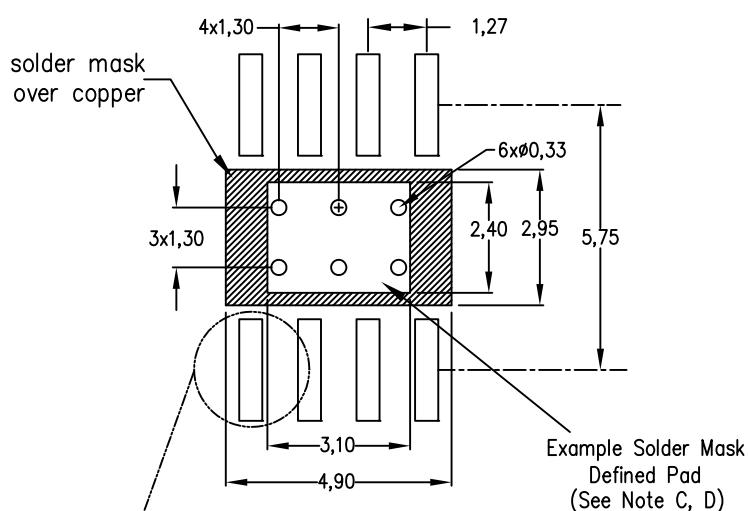
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# LAND PATTERN DATA

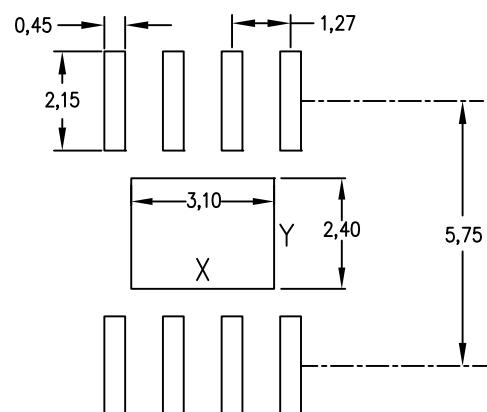
DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE

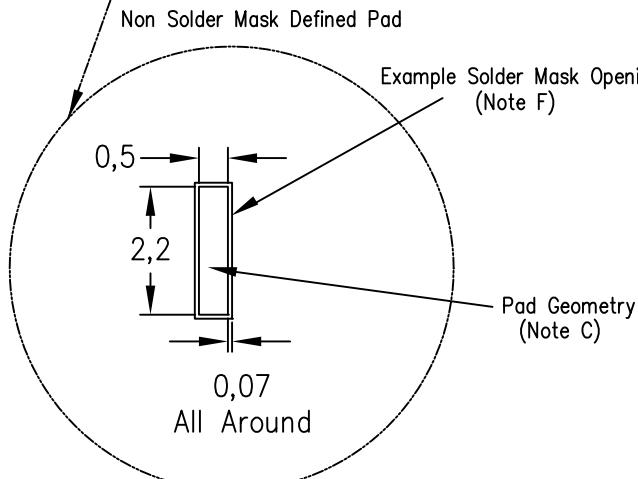
Example Board Layout  
Via pattern and copper pad size  
may vary depending on layout constraints



0,127mm Thick Stencil Design Example  
Reference table below for other  
solder stencil thicknesses  
(Note E)



Example Solder Mask  
Defined Pad  
(See Note C, D)



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

4208951-6/D 04/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

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Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
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Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
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RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>	<b>TI E2E Community</b>	
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>	<a href="http://e2e.ti.com">e2e.ti.com</a>	
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>		

## TPS55340 Integrated 5-A Wide Input Range Boost/SEPIC/Flyback DC-DC Regulator

### 1 Features

- Internal 5-A, 40-V Low-Side MOSFET Switch
- 2.9-V to 32-V Input Voltage Range
- $\pm 0.7\%$  Reference Voltage
- 0.5-mA Operating Quiescent Current
- 2.7- $\mu$ A Shutdown Supply Current
- Fixed Frequency Current Mode PWM Control
- Frequency Adjustable From 100 kHz to 1.2 MHz
- Synchronization Capability to External Clock
- Adjustable Soft-Start Time
- Pulse Skipping for Higher Efficiency at Light Loads
- Cycle-by-Cycle Current Limit, Thermal Shutdown, and UVLO Protection
- QFN-16 (3-mm x 3-mm) and HTSSOP-14 Packages With PowerPAD™
- Wide  $-40^\circ\text{C}$  to  $150^\circ\text{C}$  Operating  $T_J$  Range
- Create a Custom Design Using the TPS55340 with the [WEBENCH Power Designer](#)

### 2 Applications

- 3.3-V, 5-V, 12-V, 24-V Power Conversion
- Boost, SEPIC, and Flyback Topologies
- Thunderbolt Port, USB Type-C Power Delivery, Power Docking for Tablets and Portable PCs
- Industrial Power Systems
- ADSL Modems

### 3 Description

The TPS55340 is a monolithic, nonsynchronous switching regulator with integrated 5-A, 40-V power switch. The device can be configured in several standard switching-regulator topologies, including boost, SEPIC, and isolated flyback. The device has a wide input voltage range to support applications with input voltage from multicell batteries or regulated 3.3-V, 5-V, 12-V, and 24-V power rails.

The TPS55340 regulates the output voltage with current mode PWM (pulse width modulation) control, and has an internal oscillator. The switching frequency of PWM is set by either an external resistor or by synchronizing to an external clock signal. The user can program the switching frequency from 100 kHz to 1.2 MHz.

The device features a programmable soft-start function to limit inrush current during start-up and has other built-in protection features including cycle-by-cycle overcurrent limit and thermal shutdown.

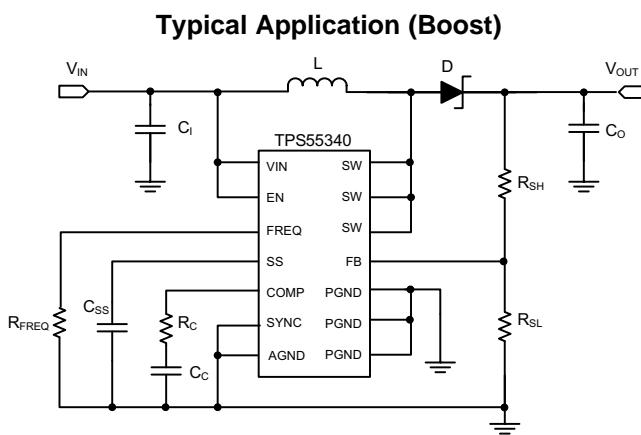
The TPS55340 is available in a small 3-mm x 3-mm 16-pin QFN as well as 14-pin HTSSOP packages with PowerPAD for enhanced thermal performance.

The 5-A, 40-V TPS55340 boost converter in the HTSSOP-14 package is pin-to-pin compatible with the 3-A, 40-V TPS61175 and it extends the maximum input voltage from 18 V to 32 V.

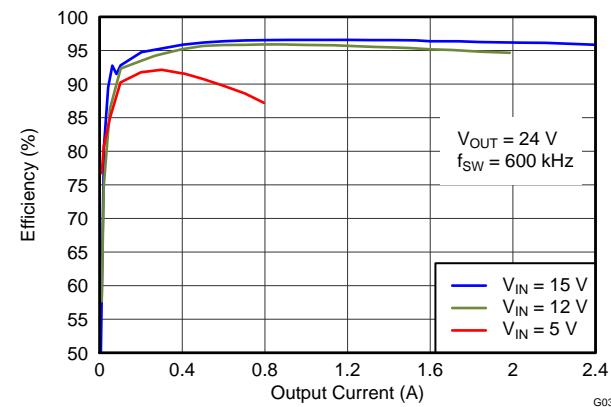
### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS55340	HTSSOP (14)	5.00 mm x 4.40 mm
	WQFN (16)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



### Efficiency vs Output Current



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

### Changes from Revision B (October 2012) to Revision C

	Page
• Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	1

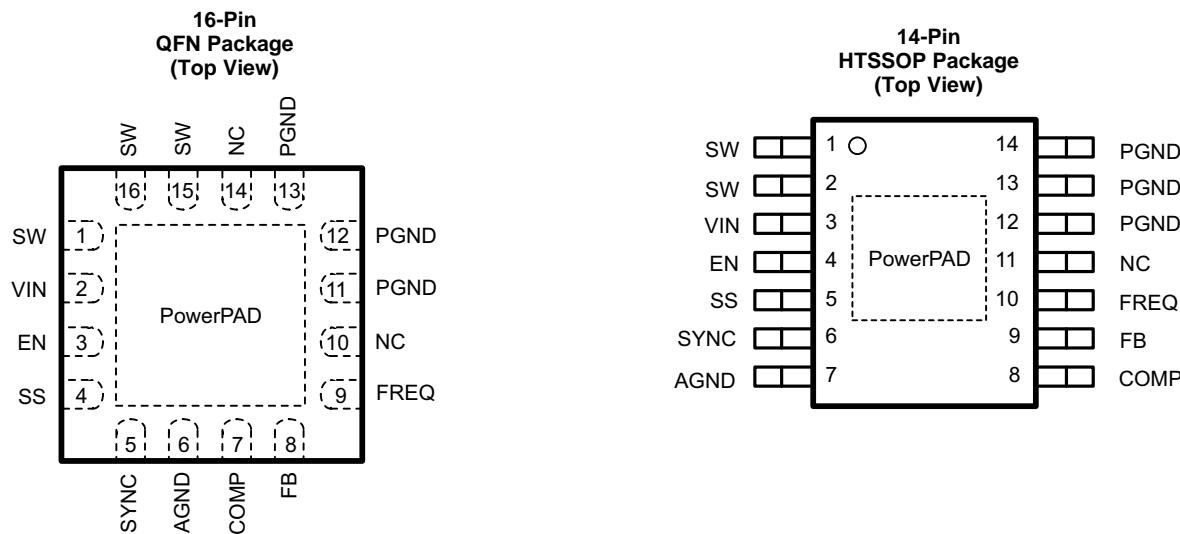
### Changes from Revision A (October 2012) to Revision B

	Page
• Corrected the pin numbers to the QFN-16 Package drawing .....	3

### Changes from Original (May 2012) to Revision A

	Page
• Added PWP package .....	1
• Added HTSSOP-14 package to FEATURES .....	1
• Added 14-pin HTSSOP package to DESCRIPTION .....	1
• Added paragraph to end of DESCRIPTION .....	1
• Added PWP package to PIN ASSIGNMENTS .....	3
• Added PWP package to PIN FUNCTIONS .....	3
• Added HTSSOP package to THERMAL INFORMATION .....	4

## 5 Pin Configuration and Functions



### Pin Functions

PIN			DESCRIPTION
NAME	QFN-16	HTSSOP-14	
AGND	6	7	Signal ground of the IC.
COMP	7	8	Output of the transconductance error amplifier. An external RC network connected to this pin compensates the regulator feedback loop.
EN	3	4	Enable pin. When the voltage of this pin falls below the enable threshold for more than 1 ms, the IC turns off.
FB	8	9	Error amplifier input and feedback pin for positive voltage regulation. Connect to the center tap of a resistor divider to program the output voltage.
FREQ	9	10	Switching frequency program pin. An external resistor connected between the FREQ pin and AGND sets the switching frequency.
NC	10, 14	11	Reserved pin that must be connected to ground.
PGND	11, 12, 13	12, 13, 14	Power ground of the IC. It is connected to the source of the internal power MOSFET switch.
PowerPAD	—	—	The PowerPAD should be soldered to the AGND. If possible, use thermal vias to connect to internal ground plane for improved power dissipation.
SS	4	5	Soft-start programming pin. A capacitor between the SS pin and AGND pin programs soft-start timing.
SW	1, 15, 16	1, 2	SW is the drain of the internal power MOSFET. Connect SW to the switched side of the boost or SEPIC inductor or the flyback transformer.
SYNC	5	6	Switching frequency synchronization pin. An external clock signal can be used to set the switching frequency between 200 kHz and 1.0 MHz. If not used, this pin should be tied to AGND.
VIN	2	3	The input supply pin to the IC. Connect VIN to a supply voltage between 2.9 V and 32 V. It is acceptable for the voltage on the pin to be different from the boost power stage input.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	MAX	UNIT
Supply voltages on pin VIN <sup>(2)</sup>	-0.3	34	V
Voltage on pin EN <sup>(2)</sup>	-0.3	34	V
Voltage on pins FB, FREQ, and COMP <sup>(2)</sup>	-0.3	3	V
Voltage on pin SS <sup>(2)</sup>	-0.3	5	V
Voltage on pin SYNC <sup>(2)</sup>	-0.3	7	V
Voltage on pin SW <sup>(2)</sup>	-0.3	40	V
Operating junction temperature	-40	150	°C
Storage temperature, T <sub>stg</sub>	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
V <sub>IN</sub>	Input voltage range	2.9	32	V
V <sub>OUT</sub>	Output voltage range	V <sub>IN</sub>	38	V
V <sub>EN</sub>	EN voltage range	0	32	V
V <sub>SYN</sub>	External switching frequency logic input range	0	5	V
T <sub>A</sub>	Operating free-air temperature	-40	125	°C
T <sub>J</sub>	Operating junction temperature	-40	150	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	TPS55340		UNIT
	QFN (16 PINS)	HTSSOP (14 PINS)	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	43.3	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	38.7	
R <sub>θJB</sub>	Junction-to-board thermal resistance	14.5	
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.4	
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	14.5	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	3.5	
		3.9	

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report ([SPRA953](#)).

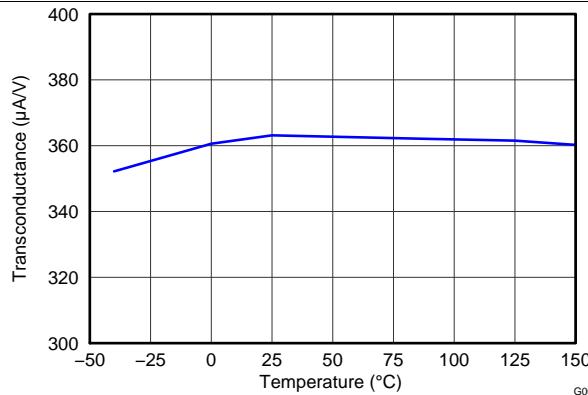
## 6.5 Electrical Characteristics

$V_{IN} = 5 \text{ V}$ ,  $T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$ , unless otherwise noted. Typical values are at  $T_A = 25^\circ\text{C}$ .

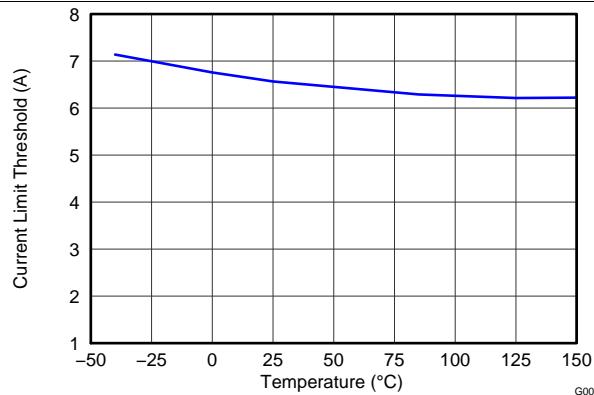
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>SUPPLY CURRENT</b>						
$V_{IN}$	Input voltage range	2.9	32		V	
$I_Q$	Operating quiescent current into $V_{IN}$	Device nonswitching, $V_{FB} = 2 \text{ V}$	0.5		mA	
$I_{SD}$	Shutdown current	EN = GND	2.7	10	$\mu\text{A}$	
$V_{UVLO}$	Undervoltage lockout threshold	$V_{IN}$ falling	2.5	2.7	V	
$V_{hys}$	Undervoltage lockout hysteresis		120	140	mV	
<b>ENABLE AND REFERENCE CONTROL</b>						
$V_{EN}$	EN threshold voltage	EN rising input	0.9	1.08	1.30	V
$V_{EN}$	EN threshold voltage	EN falling input	0.74	0.92	1.125	V
$V_{ENh}$	EN threshold hysteresis		0.16		V	
$R_{EN}$	EN pulldown resistor		400	950	1600	$\text{k}\Omega$
$T_{off}$	Shutdown delay, SS discharge	EN high to low		1.0		ms
$V_{SYNh}$	SYN logic high voltage		1.2		V	
$V_{SYNI}$	SYN logic low voltage			0.4	V	
<b>VOLTAGE AND CURRENT CONTROL</b>						
$V_{REF}$	Voltage feedback regulation voltage		1.204	1.229	1.254	V
		$T_A = 25^\circ\text{C}$	1.220	1.229	1.238	
$I_{FB}$	Voltage feedback input bias current	$T_A = 25^\circ\text{C}$		1.6	20	nA
$I_{sink}$	COMP pin sink current	$V_{FB} = V_{REF} + 200 \text{ mV}$ , $V_{COMP} = 1 \text{ V}$		42		$\mu\text{A}$
$I_{source}$	COMP pin source current	$V_{FB} = V_{REF} - 200 \text{ mV}$ , $V_{COMP} = 1 \text{ V}$		42		$\mu\text{A}$
$V_{CCLP}$	COMP pin clamp voltage	High Clamp, $V_{FB} = 1 \text{ V}$		3.1		V
		Low Clamp, $V_{FB} = 1.5 \text{ V}$		0.75		
$V_{CTH}$	COMP pin threshold	Duty cycle = 0%		1.04		V
$G_{ea}$	Error amplifier transconductance		240	360	440	$\mu\text{S}$
$R_{ea}$	Error amplifier output resistance			10		$\text{M}\Omega$
$f_{ea}$	Error amplifier crossover frequency			500		kHz
<b>FREQUENCY</b>						
$f_{SW}$	Frequency	$R_{FREQ} = 480 \text{ k}\Omega$	75	94	130	kHz
		$R_{FREQ} = 80 \text{ k}\Omega$	460	577	740	
		$R_{FREQ} = 40 \text{ k}\Omega$	920	1140	1480	
$D_{max}$	Maximum duty cycle	$V_{FB} = 1.0 \text{ V}$ , $R_{FREQ} = 80 \text{ k}\Omega$	89%	96%		
$V_{FREQ}$	FREQ pin voltage			1.25		V
$T_{min\_on}$	Minimum on pulse width	$R_{FREQ} = 80 \text{ k}\Omega$		77		ns
<b>POWER SWITCH</b>						
$R_{DS(ON)}$	N-channel MOSFET on-resistance	$V_{IN} = 5 \text{ V}$	60	110		$\text{m}\Omega$
		$V_{IN} = 3 \text{ V}$	70	120		
$I_{LN\_NFET}$	N-channel leakage current	$V_{DS} = 25 \text{ V}$ , $T_A = 25^\circ\text{C}$		2.1		$\mu\text{A}$
<b>OCP and SS</b>						
$I_{LIM}$	N-channel MOSFET current limit	$D = D_{max}$	5.25	6.6	7.75	A
$I_{SS}$	Soft-start bias current	$V_{SS} = 0 \text{ V}$		6		$\mu\text{A}$
<b>THERMAL SHUTDOWN</b>						
$T_{shutdown}$	Thermal shutdown threshold			165		$^\circ\text{C}$
$T_{hysteresis}$	Thermal shutdown threshold hysteresis			15		$^\circ\text{C}$

## 6.6 Typical Characteristics

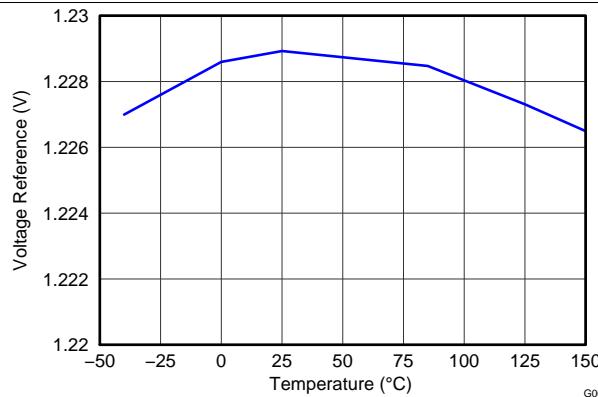
$V_{IN} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)



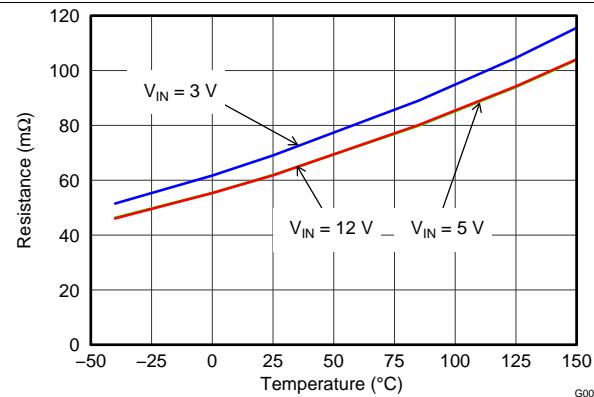
**Figure 1. Error Amplifier Transconductance vs Temperature**



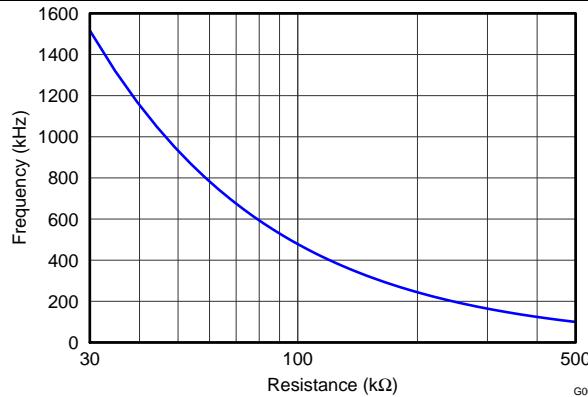
**Figure 2. Switch Current Limit vs Temperature**



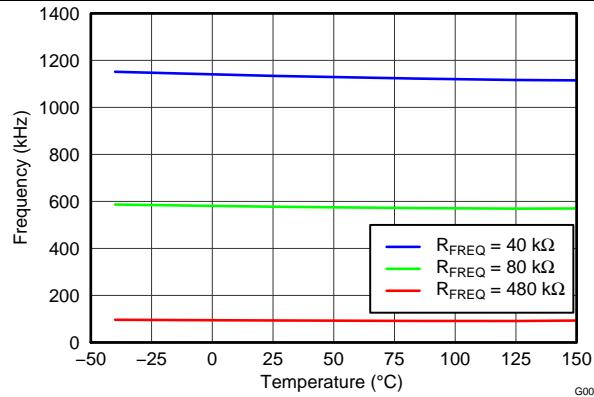
**Figure 3. Feedback Voltage Reference vs Temperature**



**Figure 4.  $R_{DS(ON)}$  vs Temperature**



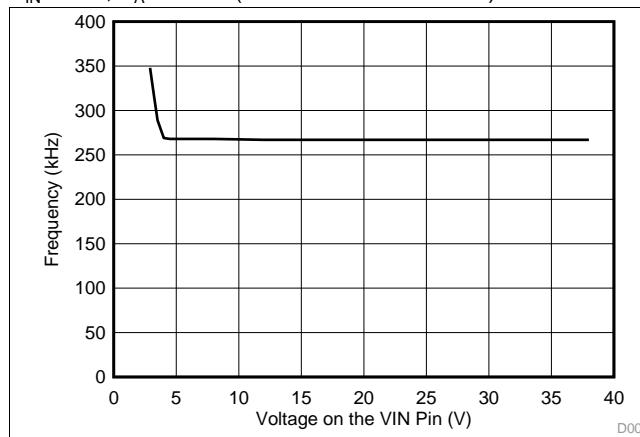
**Figure 5. Frequency vs FREQ Resistance**



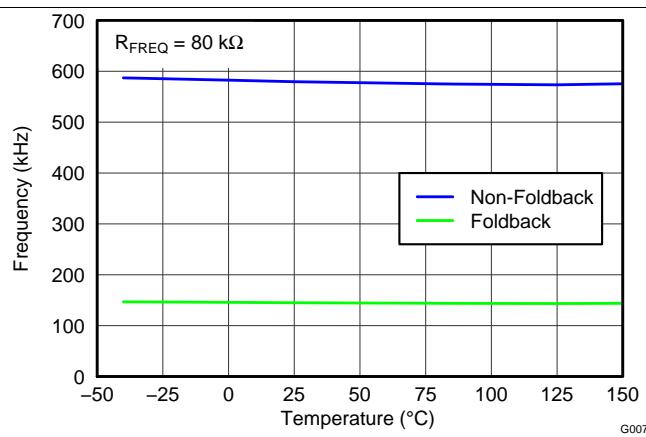
**Figure 6. Frequency vs Temperature**

## Typical Characteristics (continued)

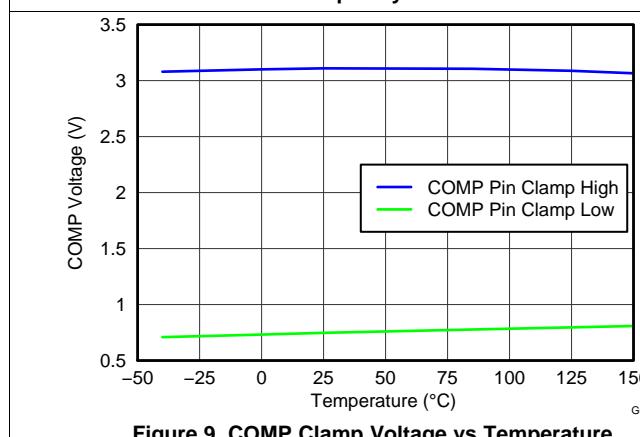
$V_{IN} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)



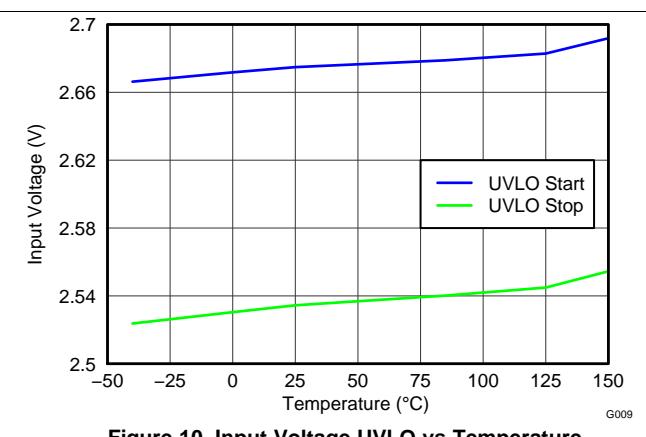
**Figure 7. Minimum Switching Frequency for Quick Recovery from Frequency Foldback**



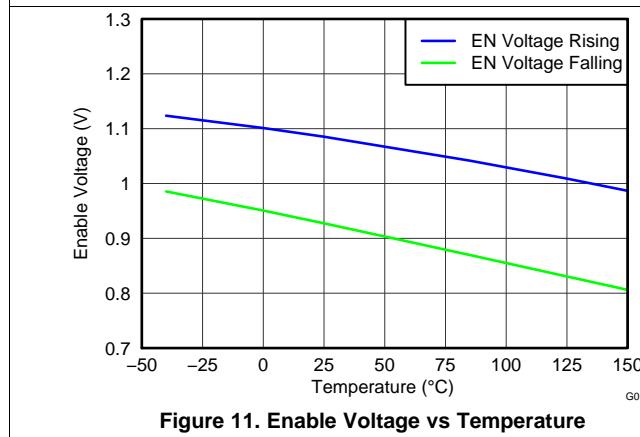
**Figure 8. Nonfoldback Frequency vs Foldback Frequency**



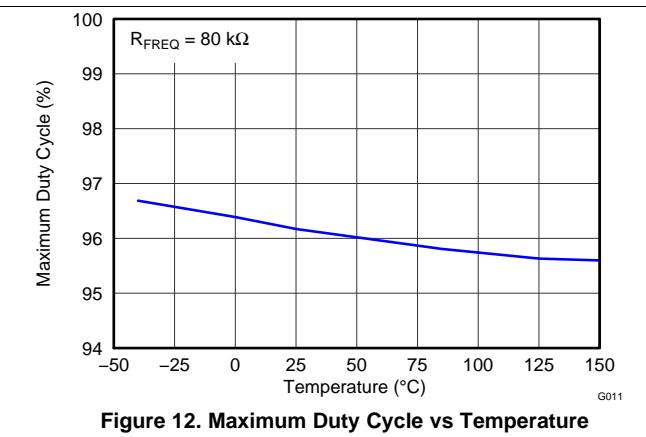
**Figure 9. COMP Clamp Voltage vs Temperature**



**Figure 10. Input Voltage UVLO vs Temperature**



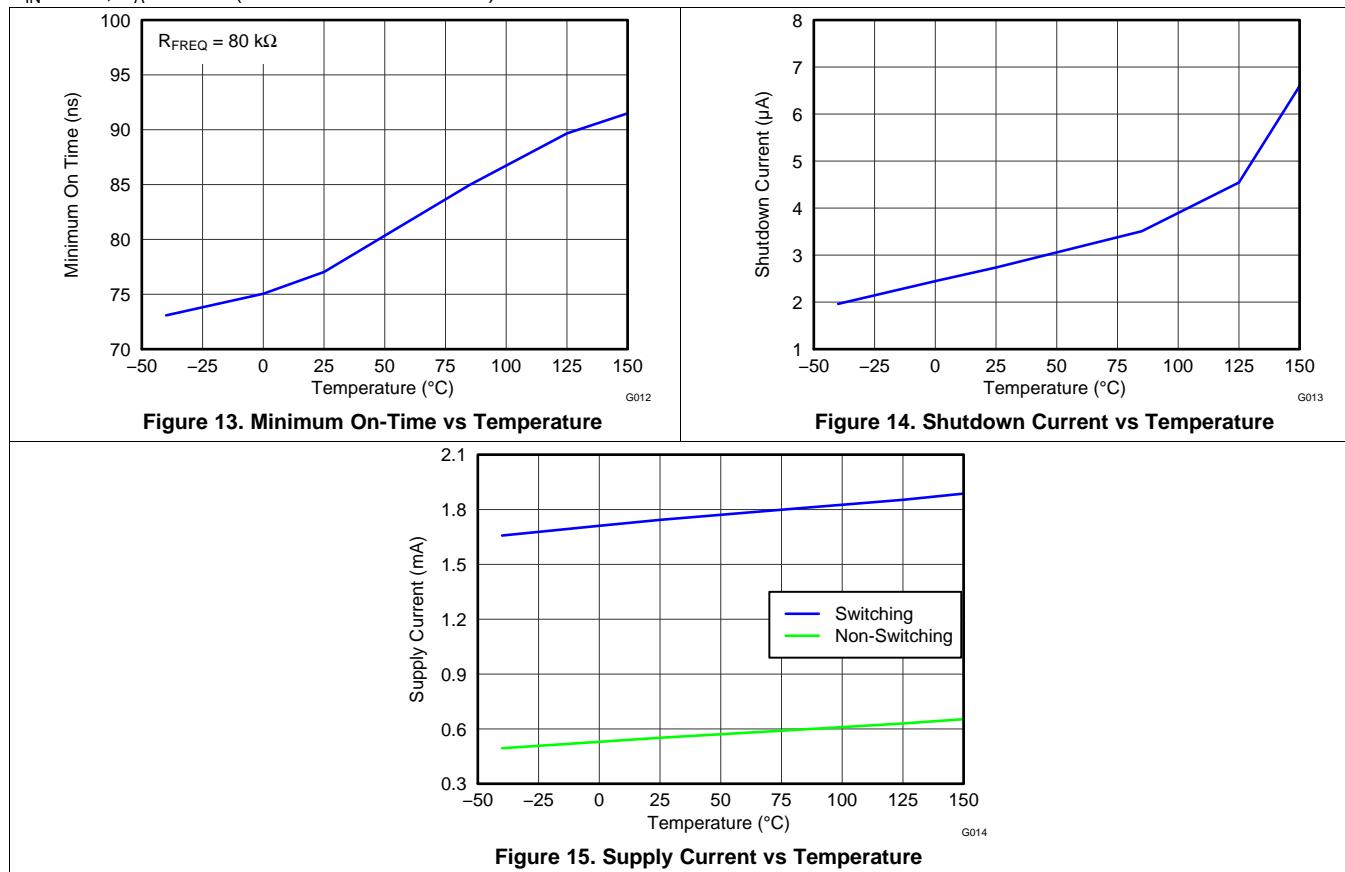
**Figure 11. Enable Voltage vs Temperature**



**Figure 12. Maximum Duty Cycle vs Temperature**

## Typical Characteristics (continued)

$V_{IN} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

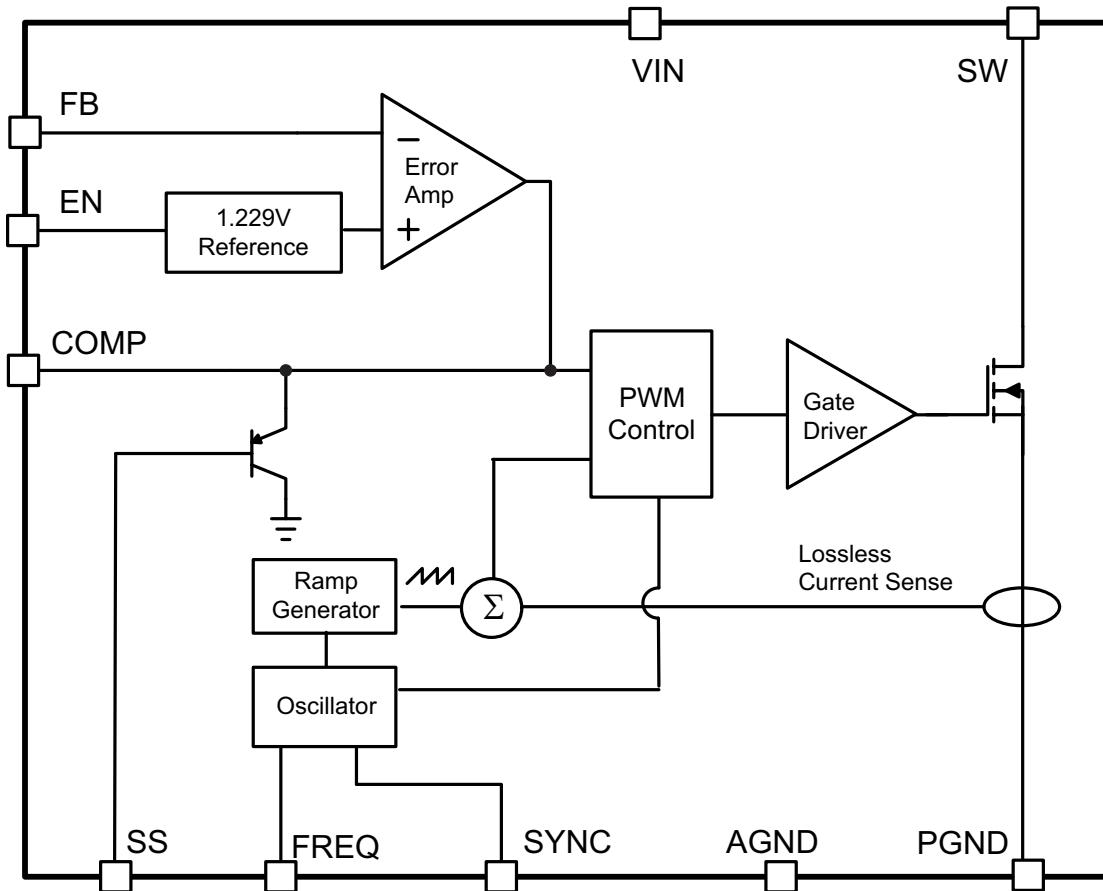


## 7 Detailed Description

### 7.1 Overview

The TPS55340 device is a monolithic, nonsynchronous, switching regulator with an integrated 5-A, 40-V power switch. The device can be configured in several standard switching-regulator topologies, including boost, SEPIC, and isolated flyback. The device has a wide input voltage range to support applications with input voltage from multicell batteries or regulated 3.3-V, 5-V, 12-V, and 24-V power rails.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Operation

If designed as a boost converter, the TPS55340 device regulates the output with current-mode, pulse-width-modulation (PWM) control. The PWM control circuitry turns on the switch at the beginning of each oscillator clock cycle. The input voltage is applied across the inductor and stores the energy as inductor current ramps up. During this portion of the switching cycle, the load current is provided by the output capacitor. When the inductor current reaches a threshold level set by the error amplifier output, the power switch turns off and the external Schottky diode is forward biased to allow the inductor current to flow to the output. The inductor transfers stored energy to replenish the output capacitor and supply the load current. This operation repeats every switching cycle. The duty cycle of the converter is determined by the PWM control comparator which compares the error amplifier output and the current signal. The oscillator frequency is programmed by the external resistor or synchronized to an external clock signal.

## Feature Description (continued)

A ramp signal from the oscillator is added to the inductor current ramp to provide slope compensation. Slope compensation is required to avoid subharmonic oscillation that is intrinsic to peak-current mode control at duty cycles higher than 50%. If the inductor value is too small, the internal slope compensation may not be adequate to maintain stability.

The PWM control feedback loop regulates the FB pin to a reference voltage through a transconductance error amplifier. The output of the error amplifier is connected to the COMP pin. An external RC compensation network connected to the COMP pin is chosen for feedback loop stability and optimum transient response.

### 7.3.2 Switching Frequency

The switching frequency is set by a resistor ( $R_{FREQ}$ ) connected to the FREQ pin of the TPS55340. The relationship between the timing resistance  $R_{FREQ}$  and frequency is shown in the [Figure 5](#). Do not leave this pin open. A resistor must always be connected from the FREQ pin to ground for proper operation. The resistor value required for a desired frequency can be calculated using [Equation 1](#).

$$R_{FREQ}(\text{k}\Omega) = 57500 \times f_{sw}(\text{kHz})^{-1.03} \quad (1)$$

For the given resistor value, the corresponding frequency can be calculated by [Equation 2](#).

$$f_{sw}(\text{kHz}) = 41600 \times R_{FREQ}(\text{k}\Omega)^{-0.97} \quad (2)$$

The TPS55340 switching frequency can be synchronized to an external clock signal that is applied to the SYNC pin. The required logic levels of the external clock are shown in [Recommended Operating Conditions](#). The recommended duty cycle of the clock is in the range of 10% to 90%. A resistor must be connected from the FREQ pin to ground when the converter is synchronized to the external clock and the external clock frequency must be within  $\pm 20\%$  of the corresponding frequency set by the resistor. For example, if the frequency programmed by the FREQ pin resistor is 600 kHz, the external clock signal should be in the range of 480 kHz to 720 kHz.

With a switching frequency below 280 kHz (typical) after the TPS55340 enters frequency foldback as described in [Overcurrent Protection and Frequency Foldback](#), if a load remains when the overcurrent condition is removed, then the output may not recover to the set value. For the output to return to the set value, the load must be removed completely or the TPS55340 power cycled with the EN pin or VIN pin. Select a nominal switching frequency of 350 kHz for quicker recovery from frequency foldback.

### 7.3.3 Overcurrent Protection and Frequency Foldback

The TPS55340 provides cycle-by-cycle overcurrent protection that turns off the power switch once the inductor current reaches the overcurrent limit threshold. The PWM circuitry resets itself at the beginning of the next switch cycle. During an overcurrent event, the output voltage begins to drop as a function of the load on the output. When the FB voltage through the feedback resistors drops lower than 0.9 V, the switching frequency is automatically reduced to 1/4 of the normal value. [Figure 8](#) shows the nonfoldback frequency with an 80-k $\Omega$  timing resistor and the corresponding foldback frequency. The switching frequency does not return to normal until the overcurrent condition is removed and the FB voltage increases above 0.9 V. The frequency foldback feature is disabled during soft-start.

#### 7.3.3.1 Minimum On-Time and Pulse Skipping

The TPS55340 PWM control system has a minimum PWM pulse width of 77 ns (typical). This minimum on-time determines the minimum duty cycle of the PWM for any set switching frequency. When the voltage regulation loop of the TPS55340 requires a minimum on-time pulse width less than 77 ns, the IC enters pulse skipping mode. In this mode, the device will hold the power switch off for several switching cycles to prevent the output voltage from rising above the desired regulated voltage. This operation typically occurs in light load conditions when the PWM operates in discontinuous conduction mode. Pulse skipping increases the output ripple as shown in [Figure 22](#).

### 7.3.4 Voltage Reference and Setting Output Voltage

An internal voltage reference provides a precise 1.229-V voltage reference at the error amplifier noninverting input. To set the output voltage, select the FB pin resistor  $R_{SH}$  and  $R_{SL}$  according to [Equation 3](#).

## Feature Description (continued)

$$V_{OUT} = 1.229 \text{ V} \times \left( \frac{R_{SH}}{R_{SL}} + 1 \right) \quad (3)$$

### 7.3.5 Soft-Start

The TPS55340 has a built-in soft-start circuit which significantly reduces the start-up current spike and output voltage overshoot. When the IC is enabled, an internal bias current source (6  $\mu\text{A}$ , typical) charges a capacitor ( $C_{SS}$ ) on the SS pin. The voltage at the capacitor clamps the output of the internal error amplifier that determines the peak current and duty cycle of PWM controller. Limiting the peak switch current during start-up with a slow ramp on the SS pin will reduce in-rush current and output voltage overshoot. Once the capacitor reaches 1.8 V, the soft-start cycle is completed and the soft-start voltage no longer clamps the error amplifier output. When the EN is pulled low for at least 1 ms, the IC enters the shutdown mode and the SS capacitor is discharged through a 5-k $\Omega$  resistor to prepare for the next soft-start sequence.

### 7.3.6 Slope Compensation

The TPS55340 has internal slope compensation to prevent subharmonic oscillations. The sensed current slope of boost converter can be expressed as [Equation 4](#):

$$S_n = \frac{V_{IN}}{L} \times R_{SENSE} \quad (4)$$

The slope compensation  $dv/dt$  can be calculated using [Equation 5](#).

$$S_e = \frac{0.32 \text{ V}/R_{FREQ}}{16 \times (1-D) \times 6 \text{ pF}} + \frac{0.5 \mu\text{A}}{6 \text{ pF}} \quad (5)$$

In a converter with current mode control, in addition to the output voltage feedback loop, the inner current loop including the inductor current sampling effect as well as the slope compensation on the small signal response should be taken into account, which can be modeled as seen in [Equation 6](#):

$$H_e(s) = \frac{1}{1 + \frac{s \times \left[ \left( 1 + \frac{S_e}{S_n} \right) \times (1-D) - 0.5 \right]}{f_{sw}} + \frac{s^2}{(\pi \times f_{sw})^2}}$$

where

- $R_{SENSE}$  (15 m $\Omega$ ) is the equivalent current sense resistor.
  - $R_{FREQ}$  is timing resistor used to set frequency.
  - D is the duty cycle.
- 

#### NOTE

If  $S_n \ll S_e$ , the converter operates in voltage mode control rather than current mode control, and [Equation 6](#) is no longer valid.

### 7.3.7 Enable and Thermal Shutdown

The TPS55340 enters shutdown when the EN voltage is less than 0.68 V (minimum) for more than 1 ms. In shutdown, the input supply current for the device is less than 10  $\mu\text{A}$  (maximum). The EN pin has an internal 950-k $\Omega$  pulldown resistor to disable the device if the pin is floating.

An internal thermal shutdown turns off the device when the junction temperature exceeds 165°C (typical). The device will restart when the junction temperature drops by 15°C.

## Feature Description (continued)

### 7.3.8 Undervoltage Lockout (UVLO)

An undervoltage lockout circuit prevents mis-operation of the device at input voltages below 2.5 V (typical). When the input voltage is below the UVLO threshold, the device remains off and the internal power MOSFET is turned off. The UVLO threshold is set below minimum operating voltage of 2.9 V to ensure that a transient  $V_{IN}$  dip will not cause the device to reset. For the input voltages between UVLO threshold and 2.9 V, the device tries to operate, but the electrical specifications are not assured.

## 7.4 Device Functional Modes

### 7.4.1 Operation With $V_{IN} < 2.9$ V (Minimum $V_{IN}$ )

The TPS55340 device operates with input voltages above 2.9 V. The typical UVLO voltage (turning off) is 2.5 V and the TPS55340 device remains off at input voltages lower than that point. For the input voltages between UVLO threshold and 2.9 V, the device tries to operate, but the electrical specifications are not ensured.

### 7.4.2 Operation With EN Control

The enable rising-edge threshold voltage is 1.08 V (typical) with 0.16 V hysteresis (typical). With the EN pin held below the turn-off voltage, the device is disabled and switching is inhibited. The IC quiescent current is reduced in this state. When the input voltage is above the UVLO threshold and the EN pin voltage increases above the rising edge threshold, the device becomes active. Switching enables and the soft-start sequence initiates. The TPS55340 device starts at the soft-start time determined by the external soft-start capacitor.

### 7.4.3 Operation at Light Loads

The device is designed to operate in high-efficiency, pulse-skipping mode under light load conditions. Discontinuous-conduction-mode (DCM) operation initiates when the switch current falls to 0 A. During DCM operation, the catch diode stops conducting when the switch current falls to 0 A. The switching node (the SW pin) waveform takes on the characteristics of DCM operation as shown in [Figure 21](#). As the load decreases further and when the voltage-regulation loop of TPS55340 device requires an on-time pulse width less than the minimum PWM pulse width of 77 ns (typical), the IC enters pulse-skipping mode. In this mode, the device holds the power switch off for several switching cycles to prevent the output voltage from rising too much above the desired regulated voltage.

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

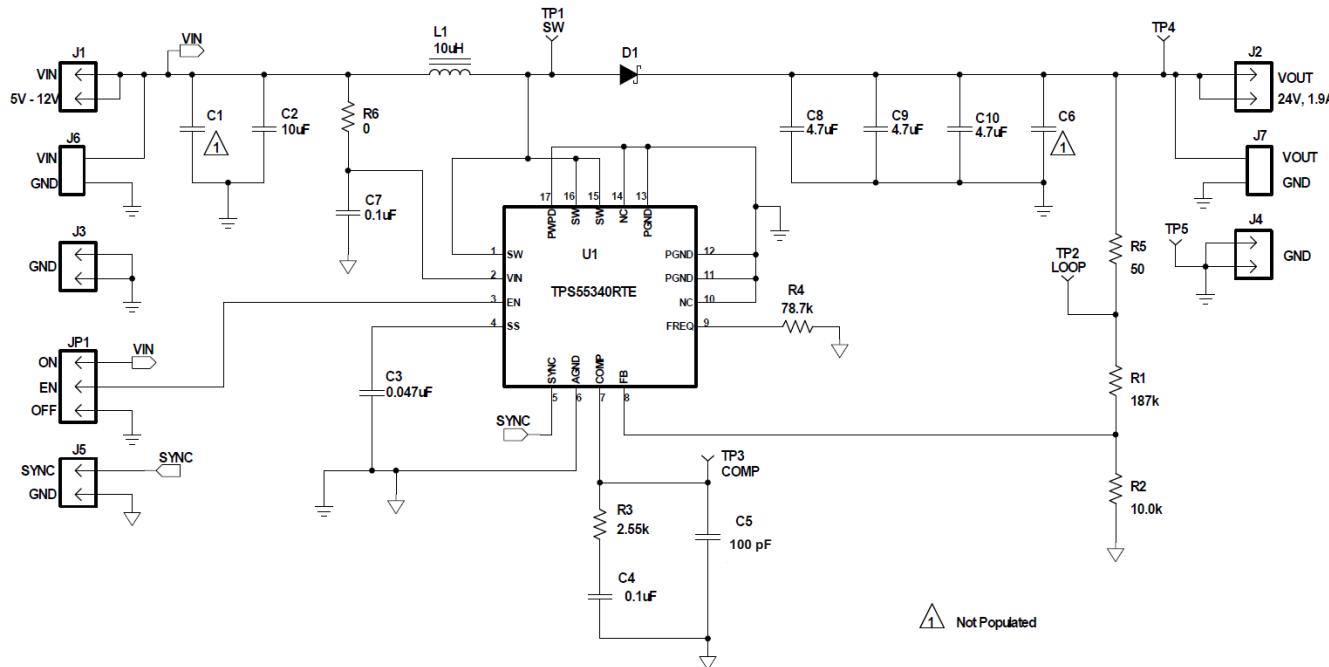
### 8.1 Application Information

The TPS55340 device can be configured in several standard switching-regulator topologies, including boost, SEPIC, and isolated flyback. For example, the device configured in boost topology is widely used to convert a lower dc voltage to a higher dc voltage with a maximum available switching current of 5.25 A. Use the following design procedure to select component values for a boost converter design or SEPIC design for the TPS55340 device. Alternately, use the WEBENCH® software to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

### 8.2 Typical Applications

The following section provides a step-by-step design approach for configuring the TPS55340 as a voltage regulating boost converter, as shown in [Figure 16](#). When configured as SEPIC or flyback converter, a different design approach is required. A design example of SEPIC converter is provided in the next section.

#### 8.2.1 Boost Converter



**Figure 16. Boost Converter Application Schematic**

#### 8.2.1.1 Design Requirements

For this design example, use the parameters listed in [Table 1](#). These parameters are typically determined at the system level.

**Table 1. Design Parameters**

PARAMETER	VALUE
Output voltage	24 V
Input voltage	5 V to 12 V
Maximum output current	800 mA
Transient response 50% load step ( $\Delta V_{OUT} = 3\%$ )	960 mV
Output voltage ripple (0.5% of $V_{OUT}$ )	120 mV

### 8.2.1.2 Detailed Design Procedure

#### 8.2.1.2.1 Custom Design with WEBENCH Tools

[Click here](#) to create a custom design using the TPS55340 device with the WEBENCH® Power Designer.

1. Start by entering your  $V_{IN}$ ,  $V_{OUT}$  and  $I_{OUT}$  requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
  - Run electrical simulations to see important waveforms and circuit performance,
  - Run thermal simulations to understand the thermal performance of your board,
  - Export your customized schematic and layout into popular CAD formats,
  - Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at [www.ti.com/webench](http://www.ti.com/webench).

#### 8.2.1.2.2 Selecting the Switching Frequency (R4)

The first step is to decide on a switching frequency for the regulator. There are tradeoffs to consider for a higher or lower switching frequency. A higher switching frequency allows for lower valued inductor and smaller output capacitors leading to the smallest solution size. A lower switching frequency will result in a larger solution size but better efficiency. The user will typically set the frequency for the minimum tolerable efficiency to avoid excessively large external components.

A switching frequency of 600 kHz is a good trade-off between efficiency and solution size. The appropriate resistor value is found from the resistance versus frequency graph of [Figure 5](#), or calculated using [Equation 1](#). R4 is calculated to be 78.4 kΩ and the nearest standard value resistor of 78.7 kΩ is selected. A resistor must be placed from the FREQ pin to ground, even if an external oscillation is applied for synchronization.

#### 8.2.1.2.3 Determining the Duty Cycle

The input-to-output voltage conversion ratio of the TPS55340 is limited by the worst case maximum duty cycle of 89% and the minimum duty cycle which is determined by the minimum on-time of 77 ns and the switching frequency. The minimum duty cycle can be estimated with [Equation 7](#). With a 600-kHz switching frequency the minimum duty cycle is 4%.

$$D_{PS} = T_{ON \ min} \times f_{sw} \quad (7)$$

The duty cycle at which the converter operates is dependent on the mode in which the converter is running. If the converter is running in DCM, where the inductor current ramps to zero at the end of each cycle, the duty cycle varies with changes of the load much more than it does when running in continuous conduction mode (CCM). In CCM, where the inductor maintains a minimum dc current, the duty cycle is related primarily to the input and output voltages as computed below. Assume a 0.5-V drop  $V_D$  across the Schottky rectifier. At the minimum input of 5 V, the duty cycle will be 80%. At the maximum input of 12 V, the duty cycle is 51%.

$$D = \frac{V_{OUT} + V_D - V_{IN}}{V_{OUT} + V_D} \quad (8)$$

At light loads the converter will operate in DCM. In this case the duty cycle is a function of the load, input and output voltages, inductance, and switching frequency as computed below. This can be calculated only after an inductance is chosen in the following section. While operating in DCM with very light load conditions, the duty cycle demand will force the TPS55340 to operate with the minimum on-time. The converter will then begin pulse skipping which can increase the output ripple.

$$D = \frac{\sqrt{2 \times (V_{OUT} + V_D - V_{IN}) \times L \times I_{OUT} \times f_{SW}}}{V_{IN}} \quad (9)$$

All converters using a diode as the freewheeling or catch component have a load current level at which they transit from DCM to CCM. At this point the inductor current just falls to zero during the off-time of the power switch. At higher load currents, the inductor current does not fall to zero and diode and switch current assume a trapezoidal wave shape as opposed to a triangular wave shape. The load current boundary between discontinuous conduction and continuous conduction can be found for a set of converter parameters as follows:

$$I_{OUT(crit)} = \frac{(V_{OUT} + V_D - V_{IN}) \times V_{IN}^2}{2 \times (V_{OUT} + V_D)^2 \times f_{SW} \times L} \quad (10)$$

For loads higher than the result of [Equation 10](#), the duty cycle is given by [Equation 8](#). For loads less than the results of [Equation 10](#), the duty cycle is given by [Equation 9](#). For [Equation 7](#) through [Equation 10](#), the variable definitions are as follows:

- $V_{OUT}$  is the output voltage of the converter in V.
- $V_D$  is the forward conduction voltage drop across the rectifier or catch diode in V.
- $V_{IN}$  is the input voltage to the converter in V.
- $I_{OUT}$  is the output current of the converter in A.
- $L$  is the inductor value in H.
- $f_{SW}$  is the switching frequency in Hz.

Unless otherwise stated, the design equations that follow assume that the converter is running in CCM which typically results in a higher efficiency for the power levels of this converter.

#### 8.2.1.2.4 Selecting the Inductor (L1)

The selection of the inductor affects steady-state operation as well as transient behavior and loop stability. These factors make it the most important component in power regulator design. There are three important inductor specifications: inductor value, dc resistance and saturation current. Considering inductor value alone is not enough. Inductor values can have  $\pm 20\%$  tolerance with no current bias. When the inductor current approaches saturation level, the effective inductance can fall to a fraction of the zero current value.

The minimum value of the inductor should be able to meet the inductor current ripple ( $\Delta I_L$ ) requirement at worst case. In a boost converter, maximum inductor current ripple occurs at 50% duty cycle. For the applications where duty cycle is always smaller or larger than 50%, [Equation 12](#) should be used with the duty cycle closest to 50% and corresponding input voltage to calculate the minimum inductance. For applications that must operate with 50% duty cycle when input voltage is somewhere between the minimum and the maximum input voltage, [Equation 13](#) should be used.  $K_{IND}$  is a coefficient that represents the amount of inductor ripple current relative to the maximum input current ( $I_{IN,DC} = I_{L,avg}$ ). The maximum input current can be estimated with [Equation 11](#), with an estimated efficiency based on similar applications ( $\eta_{EST}$ ). The inductor ripple current will be filtered by the output capacitor. Therefore, choosing high inductor ripple currents will impact the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value ( $K_{IND}$ ) is at the discretion of the designer. However, the following guidelines may be used.

For CCM operation, it is recommended to use  $K_{IND}$  values in the range of 0.2 to 0.4. Choosing  $K_{IND}$  closer to 0.2 results in a larger inductance value, maximizes the potential output current of the converter and minimizes EMI. Choosing  $K_{IND}$  closer to 0.4 results in a smaller inductance value, a physically smaller inductor, and improved transient response, but potentially worse EMI and lower efficiency. Using an inductor with a smaller inductance value may result in the converter operating in DCM. This reduces the maximum output current of the boost

converter, causes larger input voltage and output voltage ripple, and reduced efficiency. For this design, choose  $K_{IND} = 0.3$  and a conservative efficiency estimate of 85% with the minimum input voltage and maximum output current. [Equation 12](#) is used with the maximum input voltage because this corresponds to duty cycle closest to 50%. The maximum input current is estimated at 4.52 A and the minimum inductance is 7.53  $\mu$ H. A standard value of 10  $\mu$ H is chosen.

$$I_{IN DC} = \frac{V_{OUT} \times I_{OUT}}{\eta_{EST} \times V_{IN \min}} \quad (11)$$

$$L_O \min \geq \frac{V_{IN}}{I_{IN DC} \times K_{IND}} \times \frac{D}{f_{SW}} , D \neq 50\%, V_{IN} \text{ with } D \text{ closest to } 50\% \quad (12)$$

$$L_O \min \geq \frac{(V_{OUT} + V_D)}{I_{IN DC} \times K_{IND}} \times \frac{1}{4 \times f_{SW}} , D=50\% \quad (13)$$

After choosing the inductance, the required current ratings can be calculated. The inductor will be closest to its ratings with the minimum input voltage. The ripple with the chosen inductance is calculated with [Equation 14](#). The RMS and peak inductor current can be found with [Equation 15](#) and [Equation 16](#). For this design the current ripple is 663 mA, the RMS inductor current is 4.52 A, and the peak inductor current is 4.85 A. It is generally recommended for the peak inductor current rating of the selected inductor be 20% higher to account for transients during powerup, faults, or transient load conditions. The most conservative approach is to specify an inductor with a saturation current greater than the maximum peak current limit of the TPS55340. This helps to avoid saturation of the inductor. The chosen inductor is a Würth Elektronik 74437368100. It has a saturation current rating of 12.5 A, RMS current rating of 5.2 A, and typical DCR of 27.0 m $\Omega$ .

$$\Delta I_L = \frac{V_{IN \min}}{L_O} \times \frac{D_{max}}{f_{SW}} \quad (14)$$

$$I_{L \text{ rms}} = \sqrt{\left(I_{IN DC}\right)^2 + \left(\frac{\Delta I_L}{12}\right)^2} \quad (15)$$

$$I_{L \text{ peak}} = I_{IN DC} + \frac{\Delta I_L}{2} \quad (16)$$

The TPS55340 has built-in slope compensation to avoid subharmonic oscillation associated with current mode control. If the inductor value is too small, the slope compensation may not be adequate, and the loop can be unstable.

#### 8.2.1.2.5 Computing the Maximum Output Current

The overcurrent limit for the integrated power MOSFET limits the maximum input current and thus the maximum input power for a given input voltage. Maximum output power is less than maximum input power due to power conversion losses. Therefore, the current limit setting, input voltage, output voltage, and efficiency can all change maximum current output ( $I_{OUT \max}$ ). The current limit clamps the peak inductor current; therefore, the ripple has to be subtracted to derive maximum dc current. Decreasing the  $K_{IND}$  or designing for a higher efficiency will increase the maximum output current. This can be evaluated with the chosen inductance or the chosen  $K_{IND}$ . This should be evaluated with the minimum input voltage and minimum peak current limit ( $I_{LIM}$ ) of 5.25 A.

$$I_{OUT \max} = \frac{V_{IN \min} \times \left(I_{LIM} - \frac{\Delta I_L}{2}\right) \times \eta_{EST}}{V_{OUT}} = \frac{V_{IN \min} \times I_{LIM} \times \left(1 - \frac{K_{IND}}{2}\right) \times \eta_{EST}}{V_{OUT}} \quad (17)$$

In this design with a 5-V input boosted to a 24-V output and a 10- $\mu$ H inductor with an assumed Schottky forward voltage of 0.5 V and estimated efficiency of 85%, the maximum output current is 871 mA. With the 12-V input and increased estimated efficiency of 90%, the maximum output current increases to 2.13 A. This circuit was evaluated to its maximum output currents with both the minimum and maximum input voltage.

### 8.2.1.2.6 Selecting the Output Capacitors (C8, C9, C10)

At least 4.7  $\mu\text{F}$  of ceramic-type X5R or X7R capacitance is recommended at the output. The output capacitance is mainly selected to meet the requirements for the output ripple ( $V_{\text{RIPPLE}}$ ) and voltage change during a load transient. Then the loop is compensated for the output capacitor selected. The output capacitance should be chosen based on the most stringent of these criteria. The output ripple voltage is related to the capacitance and equivalent series resistance (ESR) of the output capacitor. Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by [Equation 18](#). If high ESR capacitors are used, it will contribute additional ripple. The maximum ESR for a specified ripple is calculated with [Equation 19](#). ESR ripple can be neglected for ceramic capacitors but must be considered if tantalum or electrolytic capacitors are used. The minimum ceramic output capacitance needed to meet a load transient requirement can be estimated by the [Equation 20](#). [Equation 21](#) can be used to calculate the RMS current that the output capacitor needs to support.

$$C_{\text{OUT}} \geq \frac{D_{\text{max}} \times I_{\text{OUT}}}{f_{\text{SW}} \times V_{\text{RIPPLE}}} \quad (18)$$

$$\text{ESR} \leq \frac{\left( V_{\text{RIPPLE}} - \frac{D_{\text{max}} \times I_{\text{OUT}}}{f_{\text{SW}} \times C_{\text{OUT}}} \right)}{\Delta I_L} \quad (19)$$

$$C_{\text{OUT}} \geq \frac{\Delta I_{\text{TRAN}}}{2 \times \pi \times f_{\text{BW}} \times \Delta V_{\text{TRAN}}} \quad (20)$$

$$I_{\text{COUT rms}} = I_{\text{OUT}} \sqrt{\frac{D_{\text{max}}}{(1-D_{\text{max}})}} \quad (21)$$

Using [Equation 18](#) for this design, the minimum output capacitance for the specified 120-mV output ripple is 8.8  $\mu\text{F}$ . For a maximum transient voltage change ( $\Delta V_{\text{TRAN}}$ ) of 960 mV with a 400-mA load transient ( $\Delta I_{\text{TRAN}}$ ) and a 6-kHz control loop bandwidth ( $f_{\text{BW}}$ ) with [Equation 20](#), the minimum output capacitance is 11.1  $\mu\text{F}$ . The most stringent criteria is the 11.1  $\mu\text{F}$  for the required load transient. [Equation 21](#) gives a 1.58-A RMS current in the output capacitor. The capacitor should also be properly rated for the desired output voltage.

Care must be taken when evaluating ceramic capacitors that derate under dc bias, aging, and ac signal conditions. For example, larger form factor capacitors (in 1206 size) have self-resonant frequencies in the range of converter switching frequency. Self-resonance causes the effective capacitance to be significantly lower. The dc bias can also significantly reduce capacitance. Ceramic capacitors can lose as much as 50% of the capacitance when operated at the rated voltage. Therefore, allow a margin in selected capacitor voltage rating to ensure adequate capacitance at the required output voltage. For this example, three 4.7- $\mu\text{F}$ , 50-V, 1210 X7R ceramic capacitors are used in parallel leading to a negligible ESR. Choosing 50-V capacitors instead of 35-V reduces the effects of dc bias and allows this example circuit to be rated for the maximum output voltage range of the TPS55340.

### 8.2.1.2.7 Selecting the Input Capacitors (C2, C7)

At least 4.7  $\mu\text{F}$  of ceramic input capacitance is recommended. Additional input capacitance may be required to meet ripple and/or transient requirements. High-quality ceramic, type X5R or X7R are recommended to minimize capacitance variations over temperature. The capacitor must also have an RMS current rating greater than the maximum RMS input current of the TPS55340 calculated with [Equation 22](#). The input capacitor must also be rated greater than the maximum input voltage. The input voltage ripple can be calculated with [Equation 23](#).

$$I_{\text{CIN rms}} = \frac{\Delta I_L}{\sqrt{12}} \quad (22)$$

$$V_{\text{ripple}} = \frac{\Delta I_L}{4 \times f_{\text{SW}} \times C_{\text{IN}}} + \Delta I_L \times R_{\text{CIN}} \quad (23)$$

In the design example, the input RMS current is calculated to be 191 mA. The chosen input capacitor is a 10- $\mu\text{F}$ , 35-V, 1210 X7R with 3-m $\Omega$  ESR. Although one with a lower voltage rating can be used, a 35-V rated capacitor was chosen to limit the affects of dc bias and to allow the circuit to be rated for the entire input range of the TPS55340. The input ripple is calculated to be 30 mV. An additional 0.1- $\mu\text{F}$ , 50-V, 0603 X5R is located close to the VIN and GND pins for extra decoupling.

### 8.2.1.2.8 Setting Output Voltage (R1, R2)

To set the output voltage in either DCM or CCM, select the values of R1 and R2 according to the following equations:

$$V_{\text{OUT}} = 1.229 \text{ V} \times \left( \frac{R_1}{R_2} + 1 \right) \quad (24)$$

$$R_1 = R_2 \times \left( \frac{V_{\text{OUT}}}{1.229 \text{ V}} - 1 \right) \quad (25)$$

Considering the leakage current through the resistor divider and noise decoupling into the FB pin, an optimum value for R2 is around 10 kΩ. The output voltage tolerance depends on the V<sub>FB</sub> accuracy and the tolerance of R1 and R2. In this example with a 24-V output using [Equation 25](#), R1 is calculated to 185.3 kΩ. The nearest standard value of 187 kΩ is used.

### 8.2.1.2.9 Setting the Soft-start Time (C7)

Choose the appropriate capacitor to set soft-start time and avoid overshoot. Increasing the soft-start time reduces the overshoot during startup. A 0.047-μF ceramic capacitor is used in this example.

### 8.2.1.2.10 Selecting the Schottky Diode (D1)

The high switching frequency of the TPS55340 demands high-speed rectification for optimum efficiency. Ensure that the average and peak current ratings of the diode exceed the average output current and peak inductor current. In addition, the reverse breakdown voltage of the diode must exceed the regulated output voltage. The diode must also be rated for the power dissipated which can be calculated with [Equation 26](#).

$$P_D = V_D \times I_{\text{OUT}} \quad (26)$$

In this conservative design example, the diode is chosen to be rated for the maximum output current of 2.13 A. During normal operation with 800-mA output current and assuming a Schottky diode drop of 0.5 V, the diode must be capable of dissipating 400 mW. The recommended minimum ratings for this design are a 40-V, 3-A diode. However, to improve the flexibility of this design, a Diodes Inc B540-13-F in an SMC package is used with voltage and current ratings of 40 V and 5 A.

### 8.2.1.2.11 Compensating the Control Loop (R3, C4, C5)

The TPS55340 requires external compensation which allows the loop response to be optimized for each application. The COMP pin is the output of the internal error amplifier. An external resistor R3 and ceramic capacitor C4 are connected to the COMP pin to provide a pole and a zero, shown in [Figure 16](#). This pole and zero, along with the inherent pole and zero of a boost converter, determine the closed-loop frequency response. This is important for converter stability and transient response. Loop compensation should be designed for the minimum operating voltage.

The following equations summarize the loop equations for the TPS55340 configured as a CCM boost converter. They include the power stage output pole ( $f_{\text{OUT}}$ ) and the right-half-plane zero ( $f_{\text{RHPZ}}$ ) of a boost converter calculated with [Equation 27](#) and [Equation 28](#), respectively. When calculating  $f_{\text{OUT}}$ , it is important to include the derating of ceramic output capacitors. In the example with an estimated 10.2-μF capacitance, these frequencies are calculated to be 980 kHz and 22.1 kHz, respectively. The dc gain (A) of the power stage is calculated with [Equation 27](#) and is 39.9 dB in this design. The compensation pole ( $f_p$ ) and zero ( $f_z$ ) generated by R3, C4, and internal transconductance amplifier are calculated with [Equation 30](#) and [Equation 31](#), respectively.

Most CCM boost converters will have a stable control loop if  $f_z$  is set slightly above  $f_p$  through proper sizing of R3 and C4. A good starting point is  $C_4 = 0.1 \mu\text{F}$  and  $R_3 = 2 \text{ k}\Omega$ . Increasing R3 or reducing C4 increases the closed-loop bandwidth, and therefore improves the transient response. Adjusting R3 and C4 in the opposite direction increases the phase and gain margin of the loop, which improves loop stability. It is generally recommended to limit the bandwidth of the loop to the lower of either 1/5 of the switching frequency  $f_{\text{SW}}$  or 1/3 the RHPZ frequency,  $f_{\text{RHPZ}}$  shown in [Equation 28](#). The spreadsheet tool located in the TPS55340 product folder at [www.ti.com](http://www.ti.com) can also be used to aid in compensation design.

$$f_{\text{OUT}} \approx \frac{2}{2\pi \times R_{\text{OUT}} \times C_{\text{OUT}}} \quad (27)$$

$$f_{RHPZ} \approx \frac{R_{OUT}}{2\pi \times L} \times \left( \frac{V_{IN}}{V_{OUT}} \right)^2 \quad (28)$$

$$A = \frac{1.229}{V_{OUT}} \times G_{ea} \times 10M\Omega \times \frac{V_{IN}}{V_{OUT} \times R_{SENSE}} \times R_{OUT} \times \frac{1}{2} \quad (29)$$

$$f_P = \frac{1}{2\pi \times 10M\Omega \times C4} \quad (30)$$

$$f_Z = \frac{1}{2\pi \times R3 \times C4} \quad (31)$$

$$f_{co1} = \frac{f_{SW}}{5} \quad (32)$$

$$f_{co2} = \frac{f_{RHPZ}}{3} \quad (33)$$

Where

- $C_{OUT}$  is the equivalent output capacitor ( $C_{OUT} = C_8 + C_9 + C_{10}$ )
- $R_{OUT}$  is the equivalent load resistance ( $V_{OUT}/I_{OUT}$ )
- $G_{ea}$  is the error amplifier transconductance located in [Electrical Characteristics](#)
- $R_{SENSE}$  (15 mΩ, typical) is the sense resistor in the current control loop
- $f_{co1}$  and  $f_{co2}$  are possible bandwidths.

An additional capacitor from the COMP pin to GND (C5) can be used to place a high-frequency pole in the control loop. This is not always necessary with ceramic output capacitors. If a nonceramic output capacitor is used, there is an additional zero ( $f_{ZESR}$ ) in the control loop which can be calculated with [Equation 35](#). The value of C5 and the pole created by C5 can be calculated with [Equation 36](#) and [Equation 34](#), respectively. Finally, if more phase margin is needed, an additional zero ( $f_{ZFF}$ ) can be added by placing a capacitor ( $C_{FF}$ ) in parallel with the top feedback resistor R1. It is recommended to place the zero at the target cross-over frequency or higher. The feed-forward capacitor also adds a pole at a higher frequency. The recommended value of  $C_{FF}$  can be calculated with [Equation 37](#).

$$f_{P2} = \frac{1}{2\pi \times R_3 \times C_5} \quad (34)$$

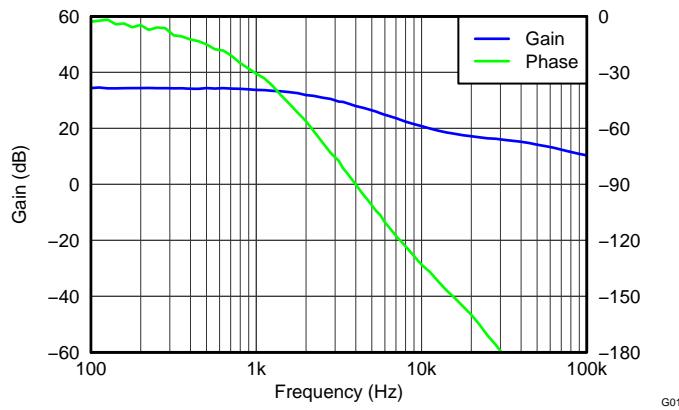
$$f_{ZESR} \approx \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \quad (35)$$

$$C_5 = \frac{R_{ESR} \times C_{OUT}}{R_3} \quad (36)$$

$$C_{FF} = \frac{1}{2\pi \times R_1 \times f_{ZFF} \times \sqrt{\frac{V_{REF}}{V_{OUT}}}} \quad (37)$$

where  $R_{ESR}$  is the ESR of the output capacitor.

If a network measurement tool is available, the most accurate compensation design can be achieved following this procedure. The power stage frequency response is first measured using a network analyzer at the minimum 5-V input and maximum 800-mA load. This measurement is shown in [Figure 17](#). In this design only one pole and one zero are used, so the maximum phase increase from the compensation will be 180 degrees. For a 60-degree phase margin, the power stage phase must be -120 degrees at its lowest point. Based on the target 6-kHz bandwidth, the measured power stage gain,  $K_{PS}(f_{BW})$ , is 24.84 dB and the phase is -110.3 degrees.



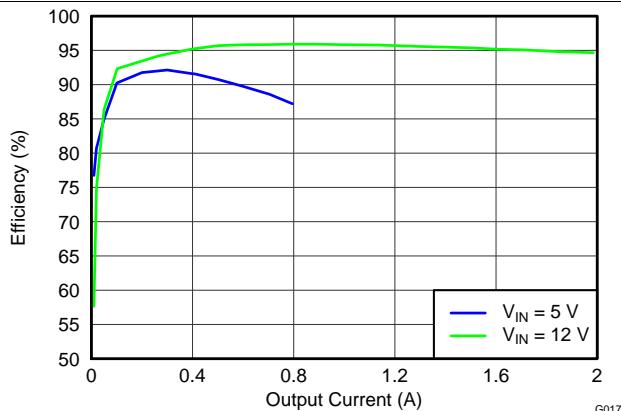
**Figure 17. Power Stage Gain and Phase of the Boost Converter**

R3 is then chosen to set the compensation gain to be the reciprocal of the power stage gain at the target bandwidth using [Equation 38](#). C4 is then chosen to place a zero at 1/10 the target bandwidth with [Equation 39](#). In this case, R3 is calculated to be 2.56 kΩ and the nearest standard value of 2.55 kΩ is used. C4 is calculated at 0.104 μF and the nearest standard value of 0.100 μF is used. Although not necessary because this design uses all ceramic capacitors, a 100-pF capacitor is selected for C5 to add a high-frequency pole at a frequency 100 times the target bandwidth.

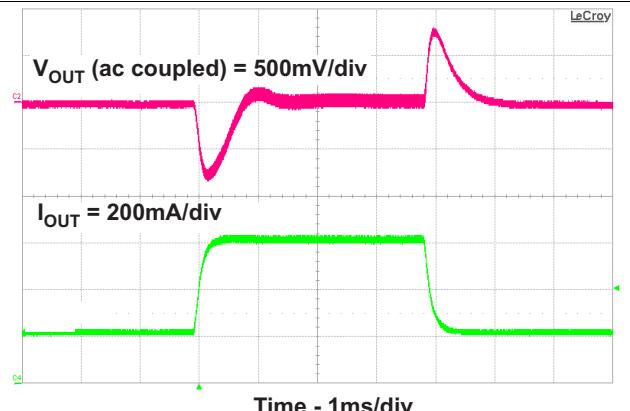
$$R3 = \frac{1}{G_{ea} \times \frac{R2}{(R1+R2)} \times 10^{\frac{K_{PS}(f_{BW})}{20}}} \quad (38)$$

$$C4 = \frac{1}{2\pi \times R3 \times \frac{f_{BW}}{10}} \quad (39)$$

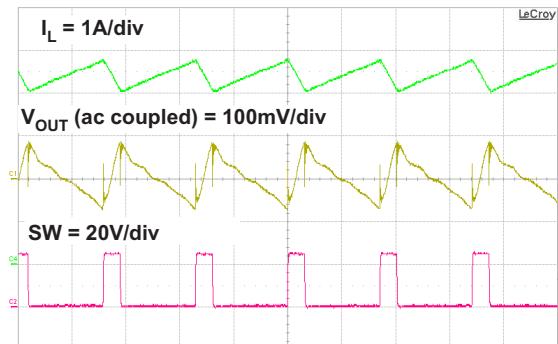
### 8.2.1.3 Application Curves



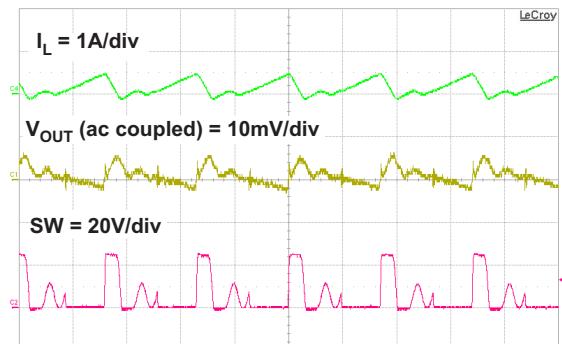
**Figure 18. Efficiency vs Output Current**



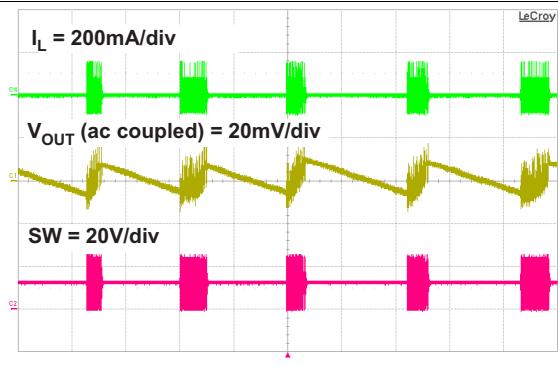
**Figure 19. Load Transient Response**



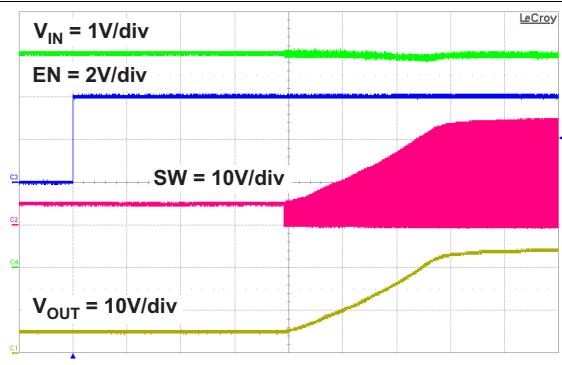
**Figure 20. CCM PWM Operation**



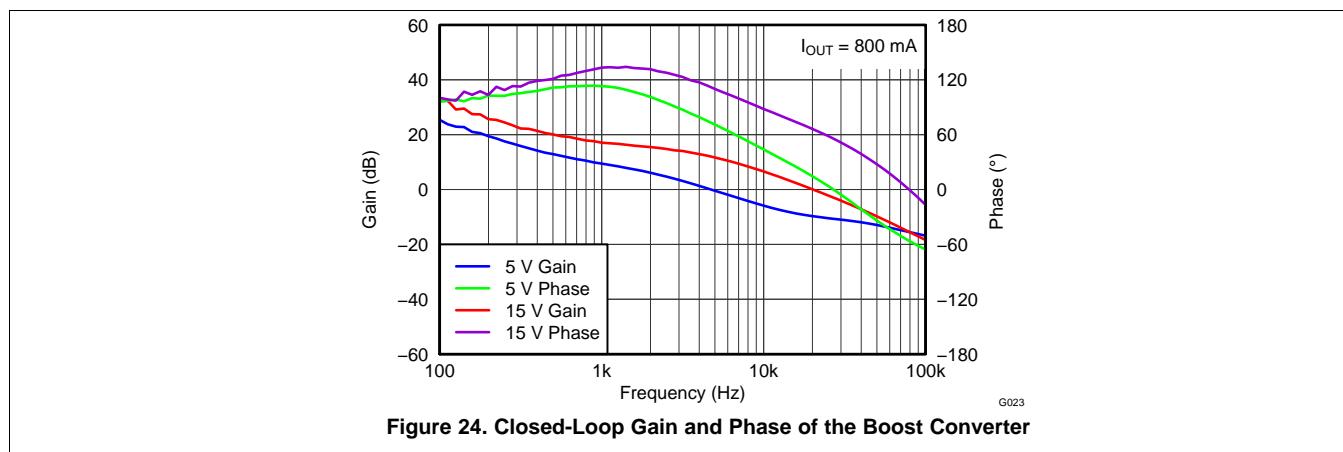
**Figure 21. DCM PWM Operation**



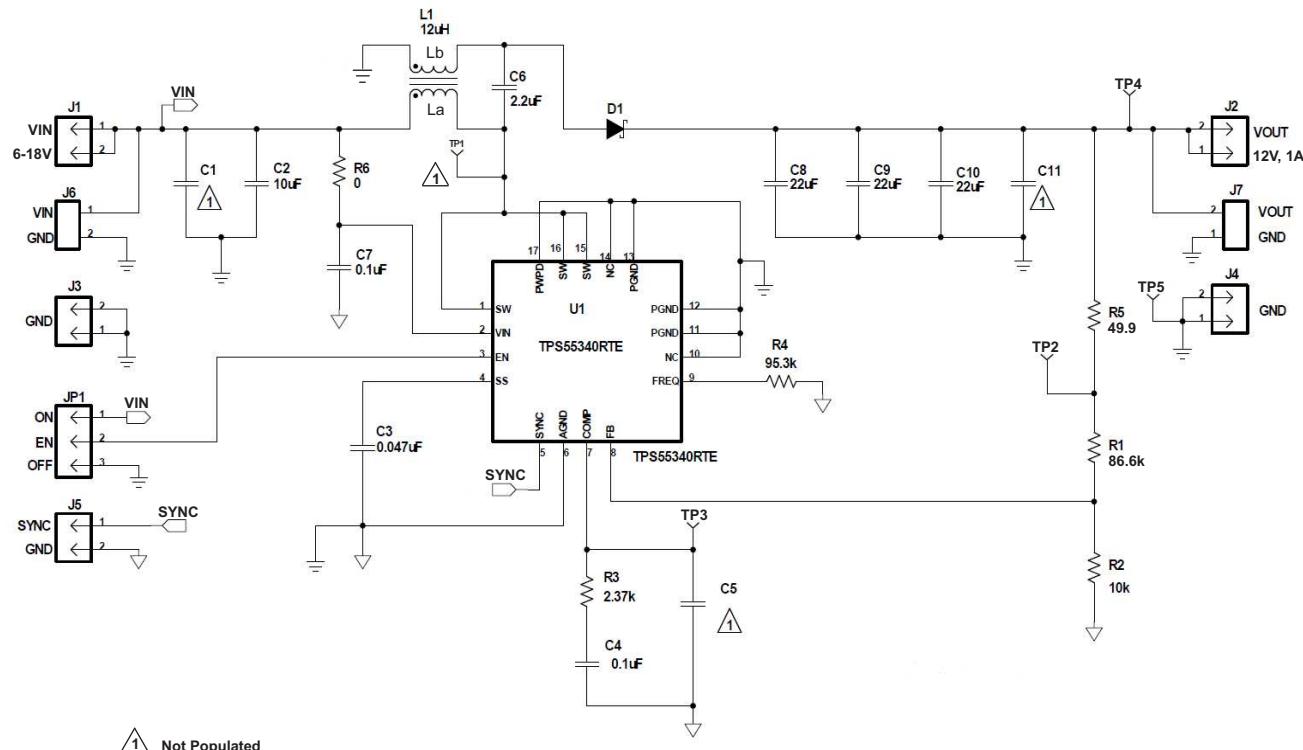
**Figure 22. Pulse Skipping**



**Figure 23. Start-Up**



### 8.2.2 SEPIC Converter



**Figure 25. SEPIC Converter Application Schematic**

#### 8.2.2.1 Design Requirements

The parameters listed in [Table 2](#) are used for a SEPIC converter design. These calculations are performed only for CCM operation. The use of a coupled inductor is assumed.

**Table 2. Design Parameters**

PARAMETER	VALUE
Output voltage	12 V
Input voltage	6 V to 18 V, 12 V nominal
Maximum output current	1 A
Transient response 50% load step ( $\Delta V_{OUT} = 4\%$ )	480 mV
Output voltage ripple (0.5% of $V_{OUT}$ )	60 mV

### 8.2.2.2 Detailed Design Procedure

#### 8.2.2.2.1 Selecting the Switching Frequency (R4)

A 500-kHz switching frequency ( $f_{SW}$ ) is selected for this design. Using [Equation 1](#), R4 is calculated and the nearest standard value of 95.3 k $\Omega$  is used.

#### 8.2.2.2.2 Duty Cycle

The duty cycle of a SEPIC converter is calculated with [Equation 40](#). With the 6-V minimum input voltage, the duty cycle is 68%; and with the 18-V maximum input voltage, the duty cycle is 41%.

$$D = \frac{V_{OUT} + V_D}{V_{OUT} + V_D + V_{IN}} \quad (40)$$

#### 8.2.2.2.3 Selecting the Inductor (L1)

With an estimated 85% efficiency, the input current is calculated with [Equation 9](#) to be 2.35 A. With  $K_{IND}$  of 0.3 and the maximum 18-V input voltage, the minimum inductance is calculated to be 10.5  $\mu$ H using [Equation 41](#). The nearest standard value of 12  $\mu$ H is used. As mentioned previously, this equation assumes a coupled inductor is used.

$$L \geq \frac{V_{IN} \max \times D_{min}}{2 \times f_{SW} \times I_{INDC} \times K_{IND}} \quad (41)$$

The inductor ripple current is recalculated to be 615 mA with [Equation 42](#). The peak current is calculated to be 3.69 A. The typical current limit is used as the saturation rating for the inductor used. The RMS current for La is approximately the average input current of 2.35 A. The RMS current for Lb is approximately the output current of 1 A. For this design, a CoilCraft MSD1260-123 is used with 6.86-A saturation, 74-m $\Omega$  DCR, and 3.12-A RMS current rating for one winding.

$$\Delta I_L = \frac{V_{IN} \max \times D_{min}}{2 \times f_{SW} \times L} \quad (42)$$

$$I_L \text{peak} = I_{La \text{peak}} + I_{Lb \text{peak}} = \left( I_{INDC} + \frac{\Delta I_L}{2} \right) + \left( I_{OUT} + \frac{\Delta I_L}{2} \right) \quad (43)$$

#### 8.2.2.2.4 Calculating the Maximum Output Current

The maximum output current with the minimum input voltage 6 V, chosen inductance 12  $\mu$ H, 5.25-A minimum current limit, and estimated 85% efficiency is calculated to be 1.47 A using [Equation 44](#).

$$I_{OUT \ max} = \frac{(I_{LIM} - \Delta I_L)}{\left( \frac{V_{OUT}}{V_{IN} \ min \times \eta_{EST}} + 1 \right)} = \frac{(I_{LIM} - I_{INDC} \times K_{IND})}{\left( \frac{V_{OUT}}{V_{IN} \ min \times \eta_{EST}} + 1 \right)} \quad (44)$$

#### 8.2.2.2.5 Selecting the Output Capacitors (C8, C9, C10)

To meet the 60-mV ripple specification, the minimum output capacitance is calculated to be 22.5  $\mu$ F with [Equation 45](#). This design uses ceramic output capacitors and the effects of ESR are ignored. To meet the transient response of 500 mA with less than 480-mV voltage change and a 7-kHz control loop bandwidth, the minimum output capacitance is calculated to be 23.7  $\mu$ F using [Equation 46](#). The RMS current is calculated with [Equation 22](#) to be 1.44 A. The output capacitors used in this design are 3  $\times$  22  $\mu$ F, 25 V, X7R 1210 ceramic capacitors. With voltage derating, the effective total output capacitance is estimated to be 30.4  $\mu$ F.

$$C_{OUT} \geq \frac{D_{max} \times I_{OUT}}{f_{SW} \times V_{RIPPLE}} \quad (45)$$

$$C_{OUT} \geq \frac{\Delta I_{TRAN}}{2\pi \times f_{BW} \times \Delta V_{TRAN}} \quad (46)$$

### 8.2.2.2.6 Selecting the Series Capacitor (C6)

The series capacitor is chosen to limit the ripple current to 5% of the maximum input voltage. Using [Equation 47](#) the minimum capacitance is 1.5  $\mu\text{F}$ . Using [Equation 48](#) the RMS current is calculated to be 1.63 A. A 2.2- $\mu\text{F}$  ceramic capacitor in a 1206 package is selected.

$$C_P \geq \frac{I_{\text{OUT}} \times D_{\text{max}}}{0.05 \times V_{\text{IN max}} \times f_{\text{SW}}} \quad (47)$$

$$I_{C_P\text{rms}} = I_{\text{INDC}} \times \sqrt{\frac{(1-D_{\text{max}})}{D_{\text{max}}}} \quad (48)$$

### 8.2.2.2.7 Selecting the Input Capacitor (C2, C7)

Based on the minimum 4.7- $\mu\text{F}$  ceramic recommended for the TPS55340, a 10- $\mu\text{F}$  X7R input capacitor is used with an additional 0.1  $\mu\text{F}$  placed close to the VIN and GND pins. With an estimated 6- $\mu\text{F}$  capacitance after voltage derating, the input ripple voltage is calculated to be 39.9 mV using [Equation 49](#). The RMS current of the input capacitance is calculated to be 0.177 A with [Equation 50](#).

$$V_{\text{ripple}} = \frac{\Delta I_L}{4 \times f_{\text{SW}} \times C_{\text{IN}}} \quad (49)$$

$$I_{C_I\text{rms}} = \frac{\Delta I_L}{\sqrt{12}} \quad (50)$$

### 8.2.2.2.8 Selecting the Schottky Diode (D1)

The selected diode must have a minimum breakdown voltage ( $V_{\text{BR}}$ ) calculated with [Equation 51](#) which is 30.5 V in this design. The average current rating is recommended to be greater than the maximum output current. With the maximum 18-V input, average current is calculated to be 2.6 A using [Equation 17](#). The package must also be capable of handling the power dissipation. With an estimated 0.5-V forward voltage, power dissipation is calculated with [Equation 26](#) to be 500 mW. Diodes Inc B340B is chosen with a 40-V, 3-A rating in an SMB package.

$$V_{\text{BR}} = V_O + V_{\text{IN max}} + V_F \quad (51)$$

### 8.2.2.2.9 Setting the Output Voltage (R1, R2)

With R2 fixed at 10 k $\Omega$  using [Equation 25](#) the nearest standard value of 86.6 k $\Omega$  is chosen for R1.

### 8.2.2.2.10 Setting the Soft-start Time (C3)

The recommended 0.047- $\mu\text{F}$  soft-start capacitor is used.

### 8.2.2.2.11 MOSFET Rating Considerations

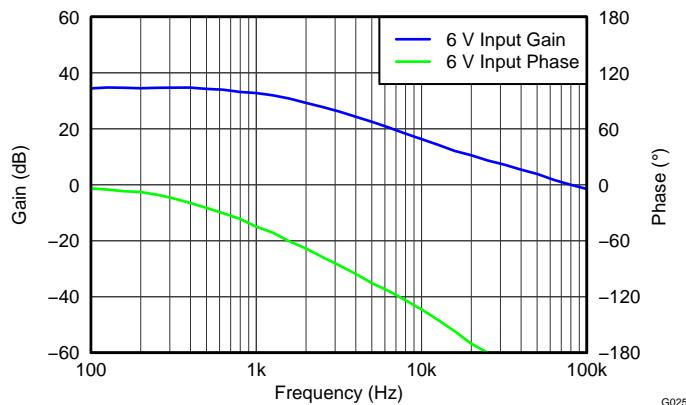
In a SEPIC converter the MOSFET must be rated to handle the sum of the input and output voltages. In this design with the maximum input voltage of 18 V and output voltage of 12 V, the FET will see approximately 30 V. A 10% tolerance is recommended to account for any ringing. The 40-V rating of the TPS55340 power MOSFET comfortably satisfies this requirement.

### 8.2.2.2.12 Compensating the Control Loop (R3, C4)

This design was compensated by measuring the frequency response of the power stage at the lowest input voltage of 6 V and choosing the components for the desired bandwidth. The lowest right half plane zero ( $f_{\text{RHPZ}}$ ) is calculated to be 36.7 kHz with [Equation 52](#). Using the recommendation to limit the bandwidth to 1/3 of  $f_{\text{RHPZ}}$ , the maximum recommended is 12.2 kHz.

$$f_{\text{RHPZ}} = \frac{\frac{V_{\text{OUT}}}{I_{\text{OUT}}}}{2 \times \pi \times L \times \left( \frac{D}{(1-D)} \right)^2} \quad (52)$$

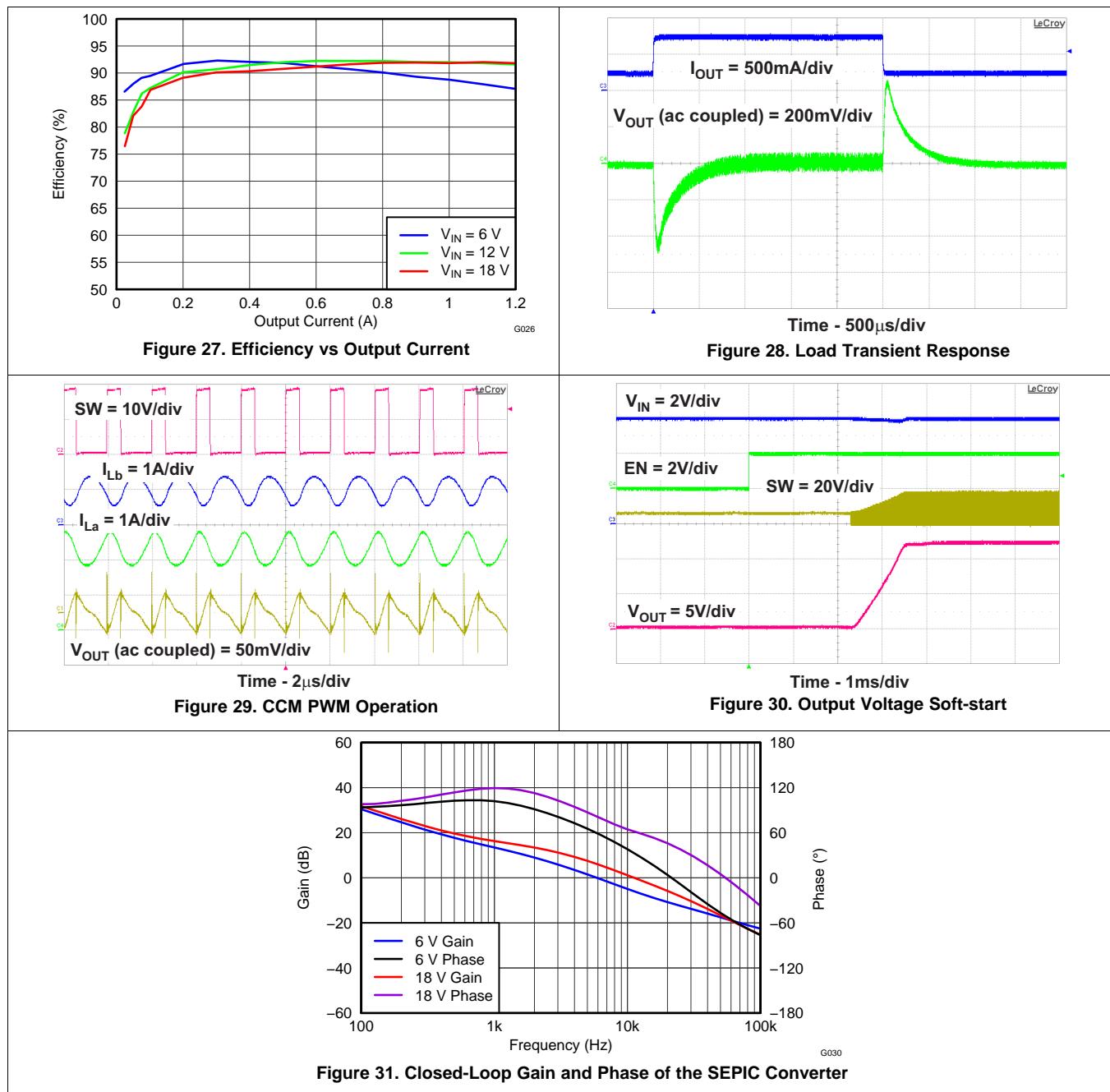
This design also uses only one pole and one zero. To achieve approximately 60 degrees of phase margin, the power stage phase must be no lower than approximately -120 degrees at the desired bandwidth. To ensure a stable design, R3 was initially set to 1 k $\Omega$  and C4 was 1  $\mu\text{F}$ . Figure 26 shows the measurement of the power stage. At 7 kHz the power stage has a gain of 19.52 dB and phase of -118.1 degrees.



**Figure 26. SEPIC Power Stage Gain and Phase**

As there are no changes in the transconductance amplifier, the equations used to calculate the external compensation components in a boost design can be used in the SEPIC design. Using the maximum  $G_{ea}$  from the electrical specification of 440  $\mu\text{mho}$ , Equation 38 calculates the nearest standard value of R3 to be 2.37 k $\Omega$ . Using Equation 39, C4 is calculated to the nearest standard value of 0.1  $\mu\text{F}$ .

### 8.2.2.3 Application Curves



## 9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.9 V and 32 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS55340 converter additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 100  $\mu$ F is a typical choice.

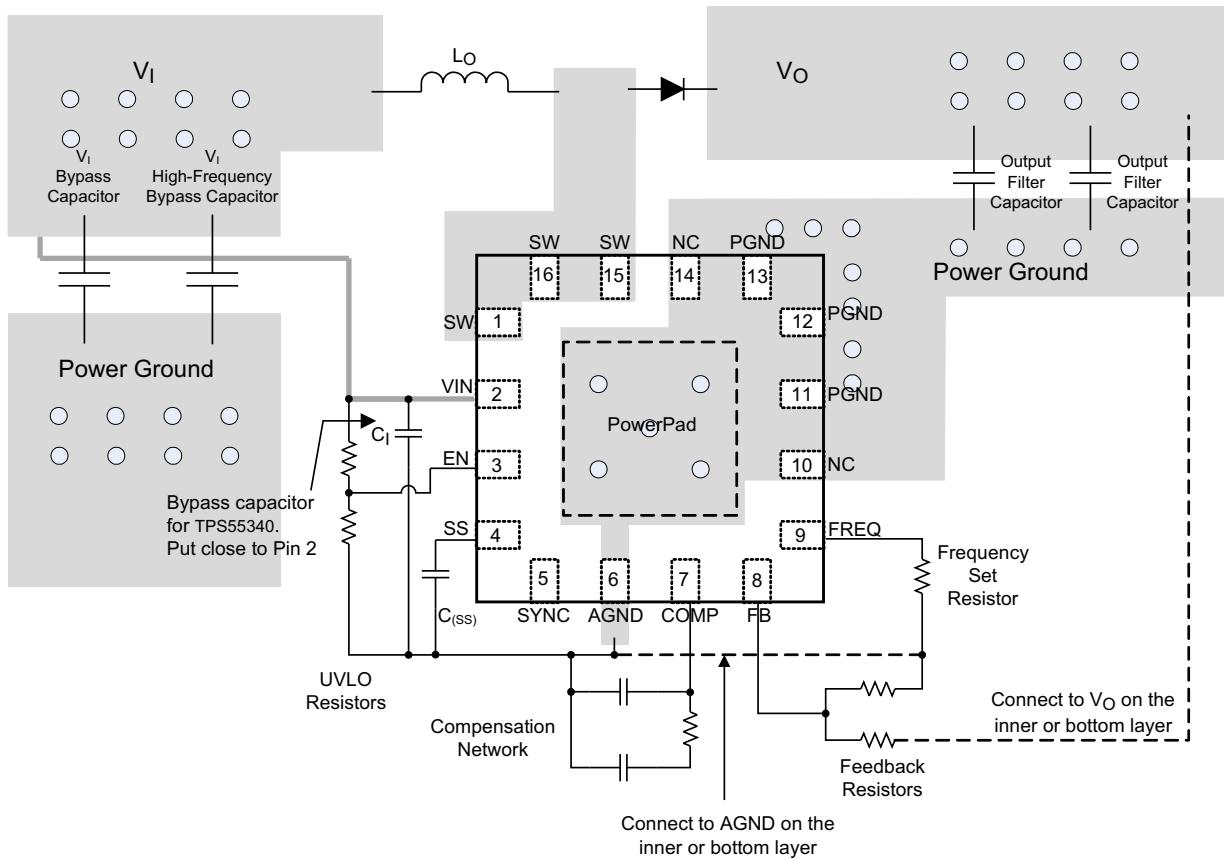
## 10 Layout

### 10.1 Layout Guidelines

As for all switching power supplies, especially those with high frequency and high switch current, printed-circuit board (PCB) layout is an important design step. If the layout is not carefully designed, the regulator can suffer from instability as well as noise problems. The following guidelines are recommended for good PCB layout.

- To prevent radiation of high-frequency resonance problems, use proper layout of the high-frequency switching path.
- Minimize the length and area of all traces connected to the SW pin and always use a ground plane under the switching regulator to minimize inter-plane coupling.
- The high current path, including the internal MOSFET switch, Schottky diode, and output capacitor, contains nanosecond rise times and fall times. Keep these rise times and fall times as short as possible.
- Place the VIN bypass capacitor as close to the VIN pin and the AGND pin as possible to reduce the IC supply ripple.
- Connect the AGND and PGND pins to thermal pad directly on the same layer.

### 10.2 Layout Example



**Figure 32. TPS55340 Layout Example**

## 10.3 Thermal Considerations

The maximum IC junction temperature should be restricted to 150°C under normal operating conditions. This restriction limits the power dissipation of the TPS55340. The TPS55340 features a thermally enhanced QFN package. This package includes a PowerPAD that improves the thermal capabilities of the package. The thermal resistance of the QFN package in any application greatly depends on the PCB layout and the PowerPAD connection. The PowerPAD must be soldered to the analog ground on the PCB. Use thermal vias underneath the PowerPAD to achieve good thermal performance.

## 11 Device and Documentation Support

### 11.1 Custom Design with WEBENCH Tools

[Click here](#) to create a custom design using the TPS55340 device with the WEBENCH® Power Designer.

1. Start by entering your  $V_{IN}$ ,  $V_{OUT}$  and  $I_{OUT}$  requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
  - Run electrical simulations to see important waveforms and circuit performance,
  - Run thermal simulations to understand the thermal performance of your board,
  - Export your customized schematic and layout into popular CAD formats,
  - Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at [www.ti.com/webench](http://www.ti.com/webench).

### 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.3 Trademarks

PowerPAD is a trademark of Texas Instruments.

WEBENCH is a registered trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.5 Glossary

[SLYZ022 — TI Glossary](#).

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS55340PWP	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	55340	Samples
TPS55340PWPR	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	55340	Samples
TPS55340RTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	55340	Samples
TPS55340RTET	ACTIVE	WQFN	RTE	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	55340	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



www.ti.com

## PACKAGE OPTION ADDENDUM

6-Oct-2014

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

### OTHER QUALIFIED VERSIONS OF TPS55340 :

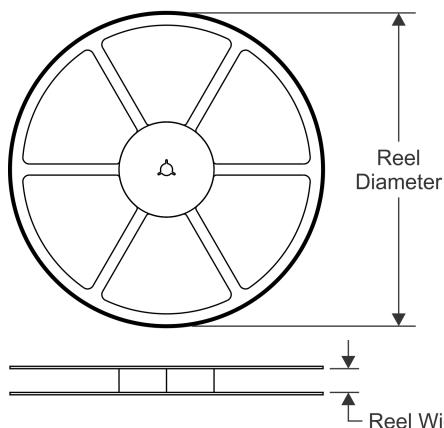
- Automotive: [TPS55340-Q1](#)
- Enhanced Product: [TPS55340-EP](#)

NOTE: Qualified Version Definitions:

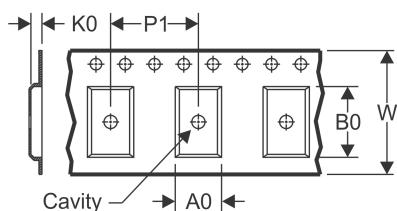
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

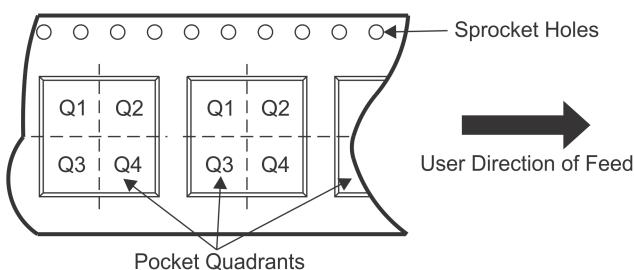


### TAPE DIMENSIONS



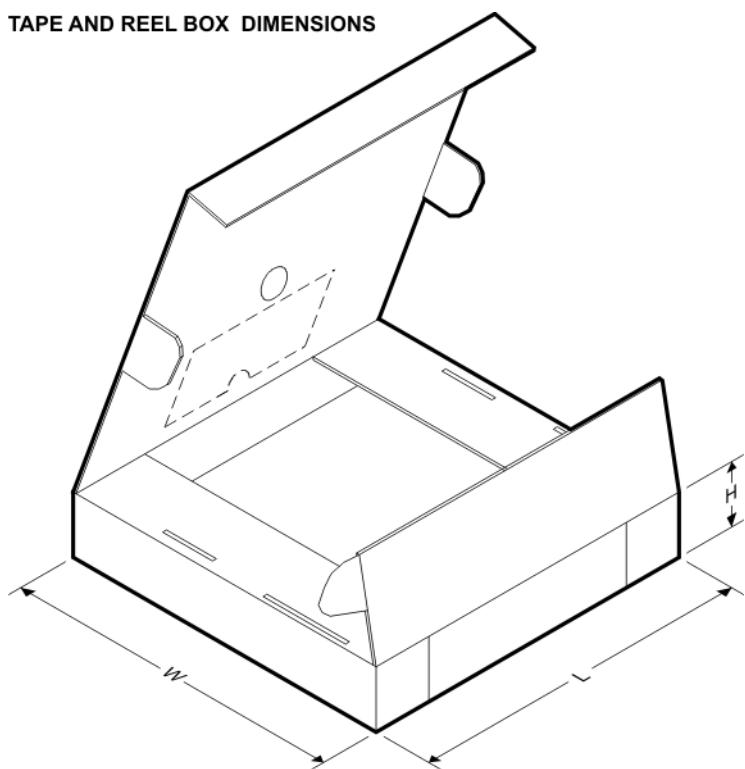
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS55340PWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS55340RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS55340RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


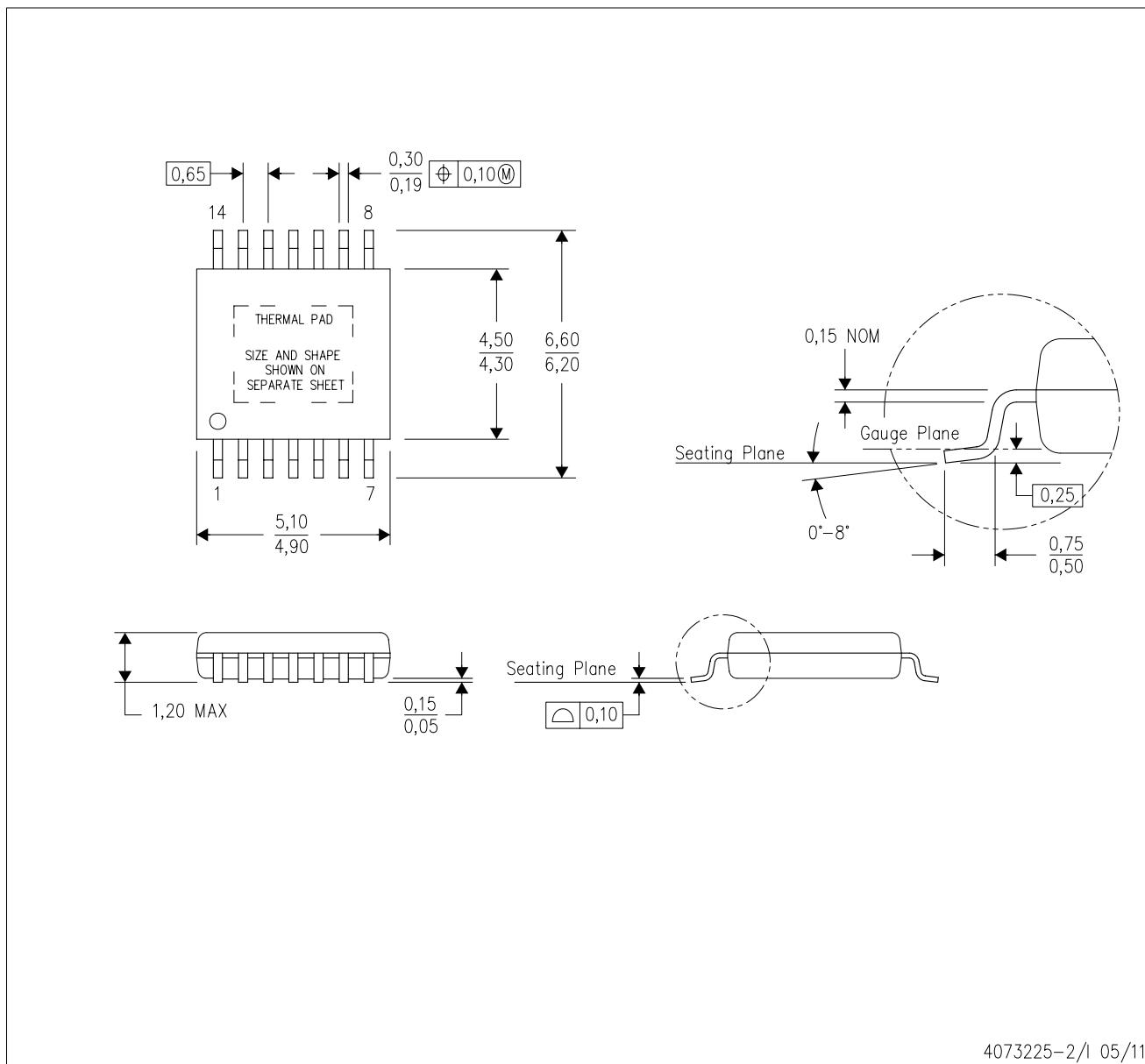
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS55340PWPR	HTSSOP	PWP	14	2000	367.0	367.0	38.0
TPS55340RTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS55340RTET	WQFN	RTE	16	250	210.0	185.0	35.0

## MECHANICAL DATA

PWP (R-PDSO-G14)

PowerPAD™ PLASTIC SMALL OUTLINE



4073225-2/1 05/11

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

# THERMAL PAD MECHANICAL DATA

PWP (R-PDSO-G14)

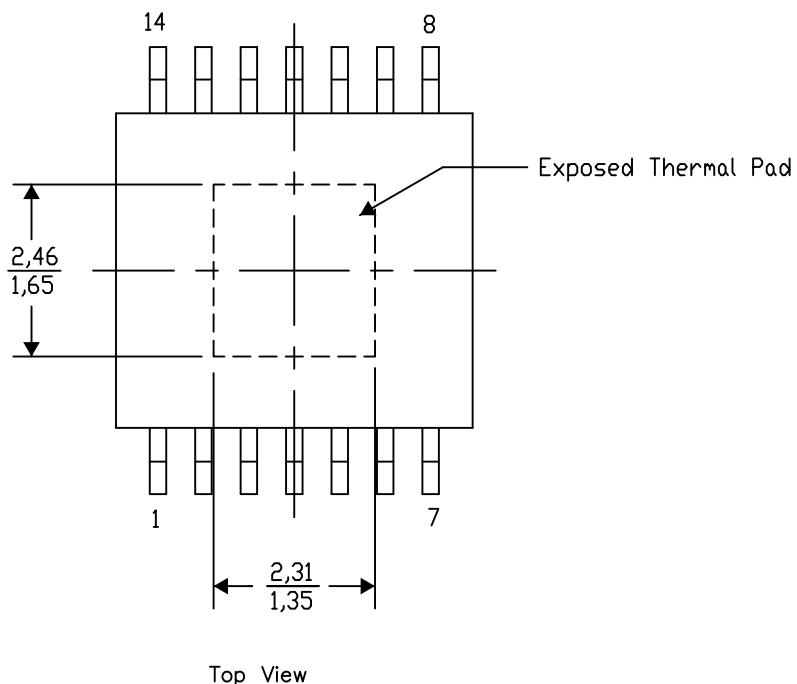
PowerPAD™ SMALL PLASTIC OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206332-2/AO 01/16

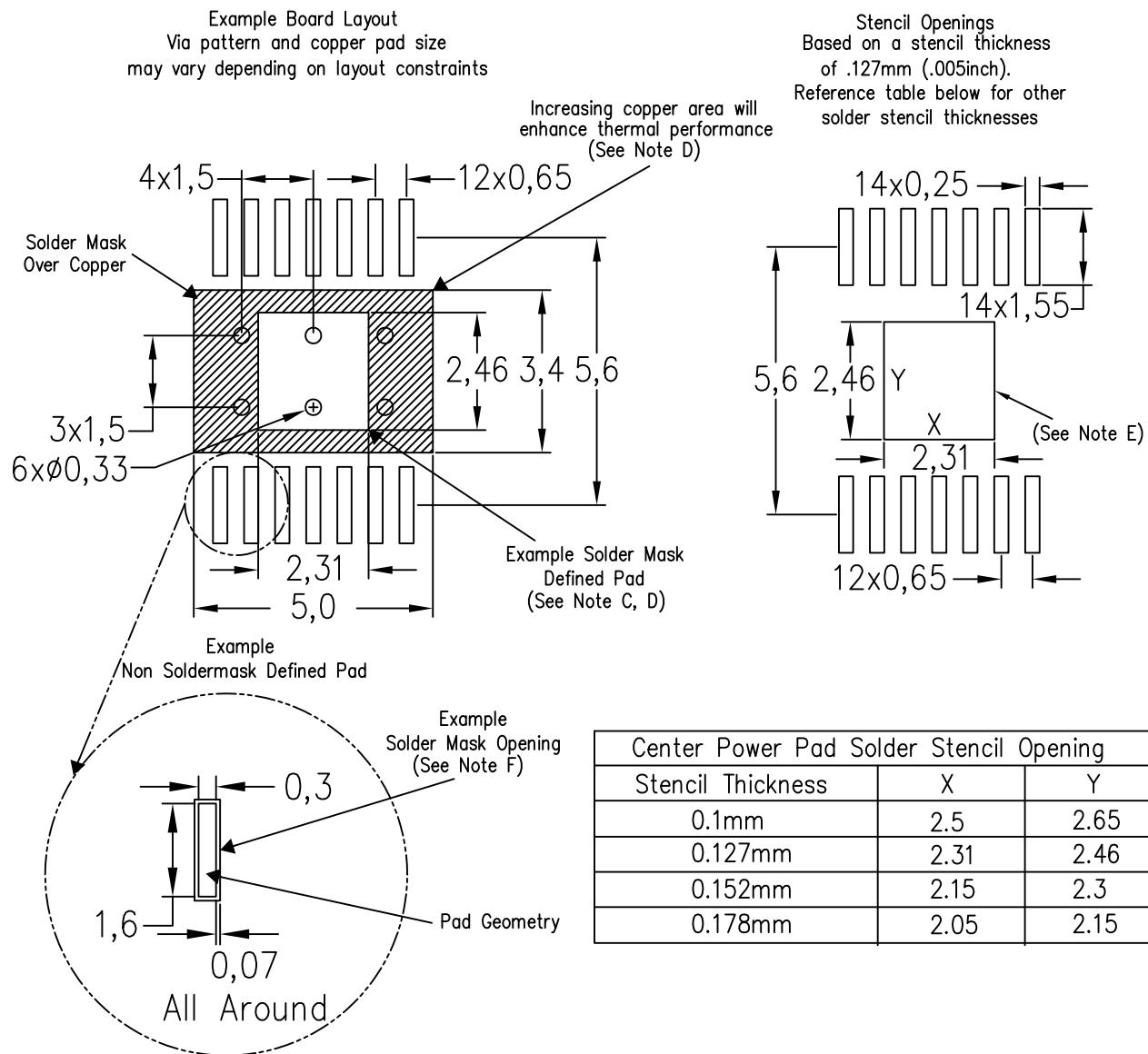
NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

# LAND PATTERN DATA

PWP (R-PDSO-G14)

PowerPAD™ PLASTIC SMALL OUTLINE



4207609-2/W 09/15

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# THERMAL PAD MECHANICAL DATA

PWP (R-PDSO-G14)

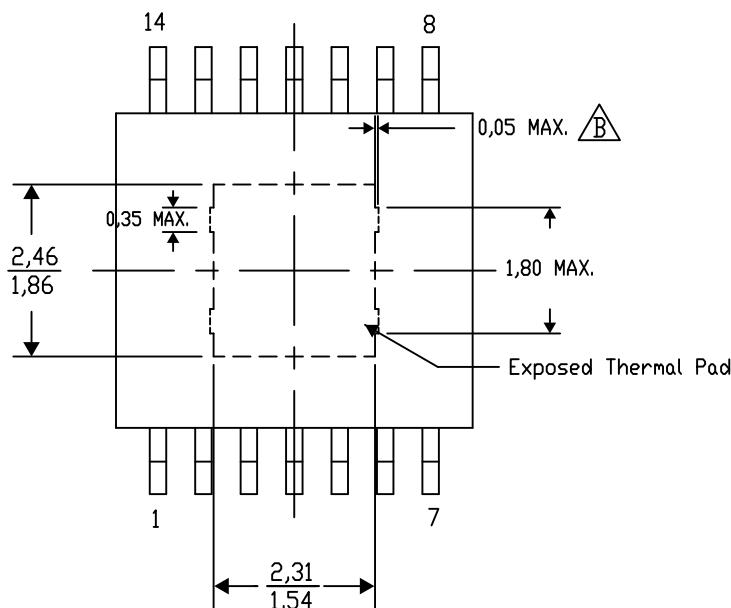
PowerPAD™ SMALL PLASTIC OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332-44/AO 01/16

NOTE: A. All linear dimensions are in millimeters

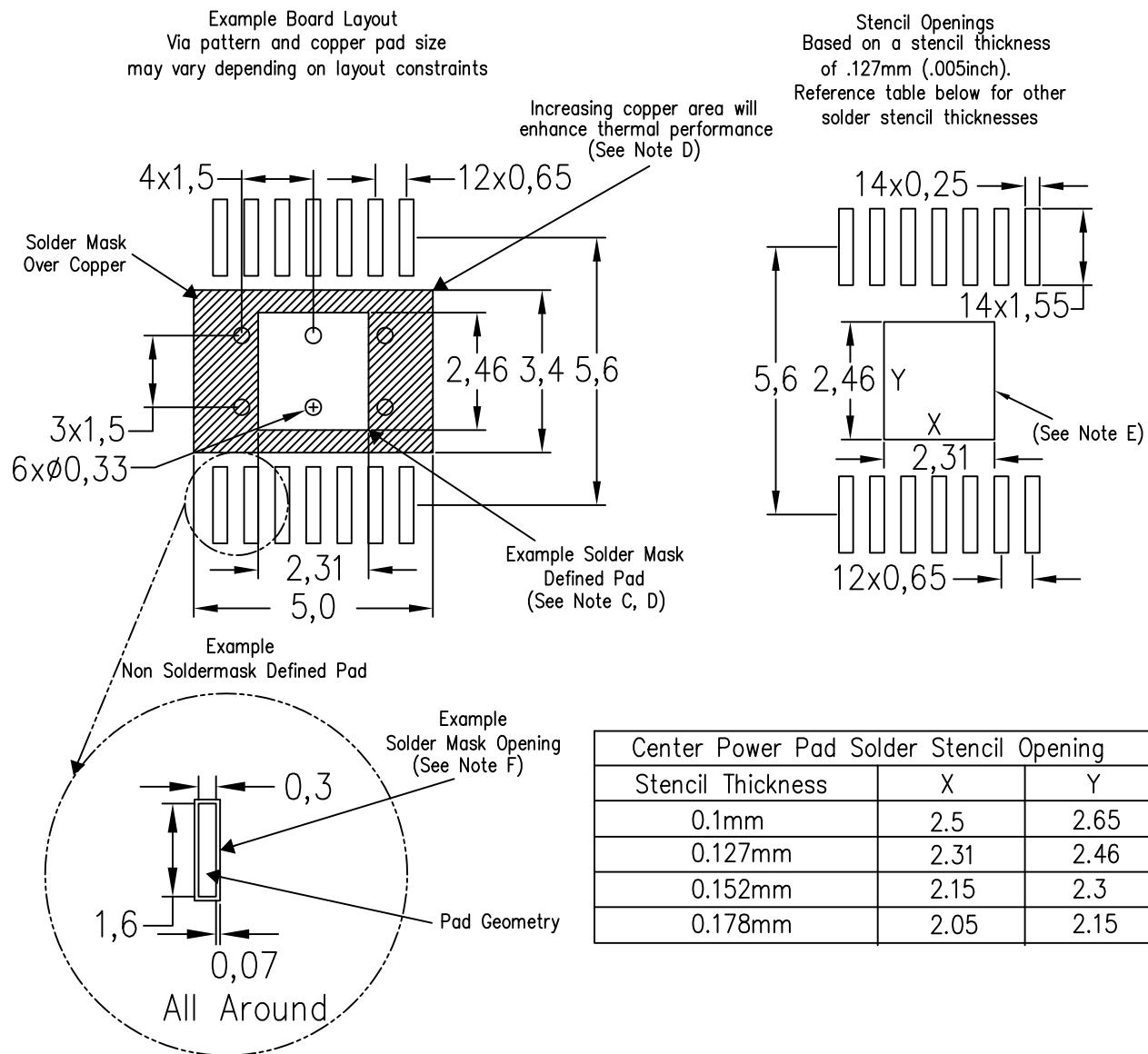
Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

# LAND PATTERN DATA

PWP (R-PDSO-G14)

PowerPAD™ PLASTIC SMALL OUTLINE



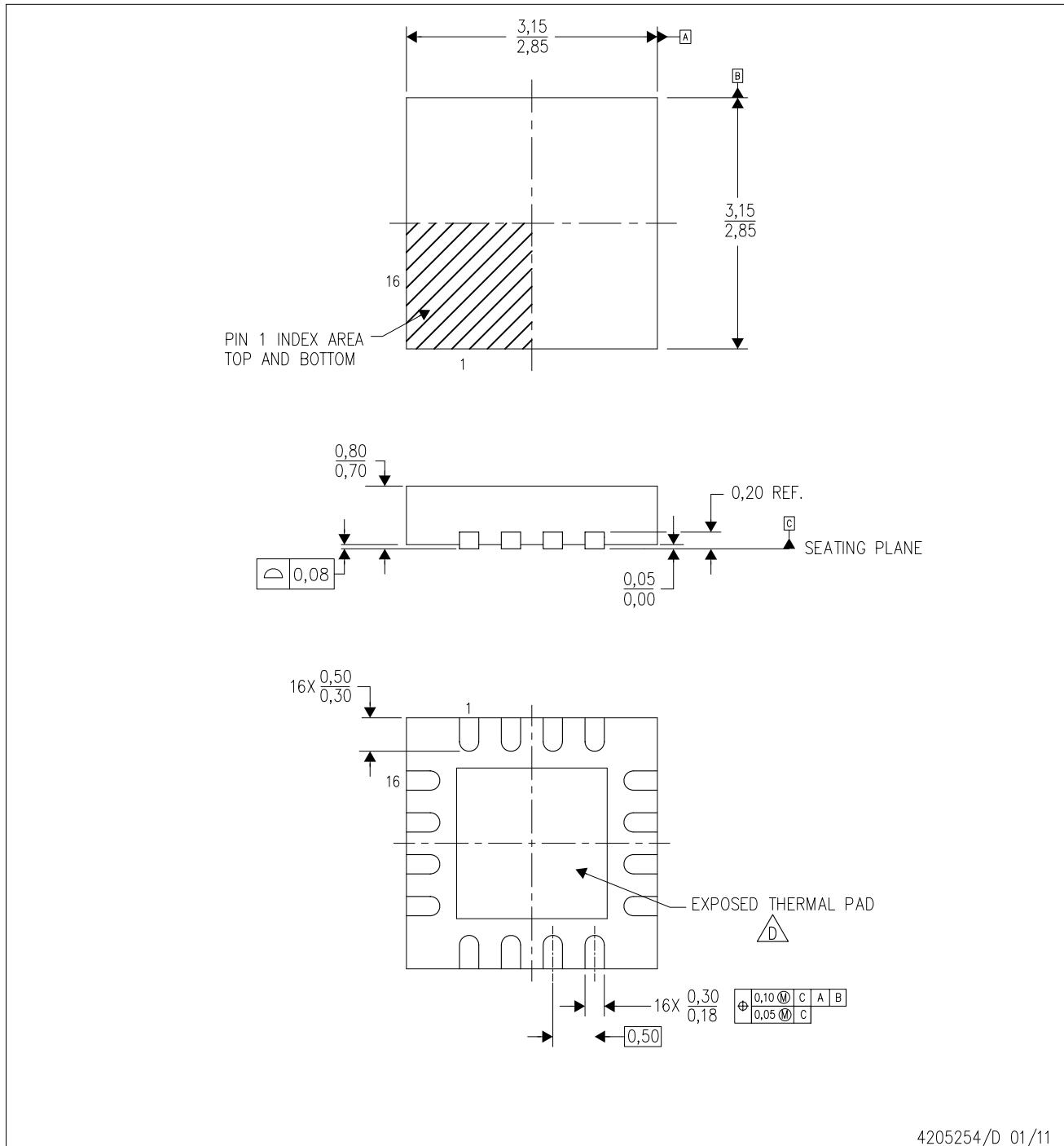
4207609-2/W 09/15

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

RTE (S-PWQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4205254/D 01/11

- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.  
B. This drawing is subject to change without notice.

C. Quad Flatpack, No-leads (QFN) package configuration.

**⚠** The package thermal pad must be soldered to the board for thermal and mechanical performance.  
See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

E. Falls within JEDEC MO-220.

## THERMAL PAD MECHANICAL DATA

RTE (S-PWQFN-N16)

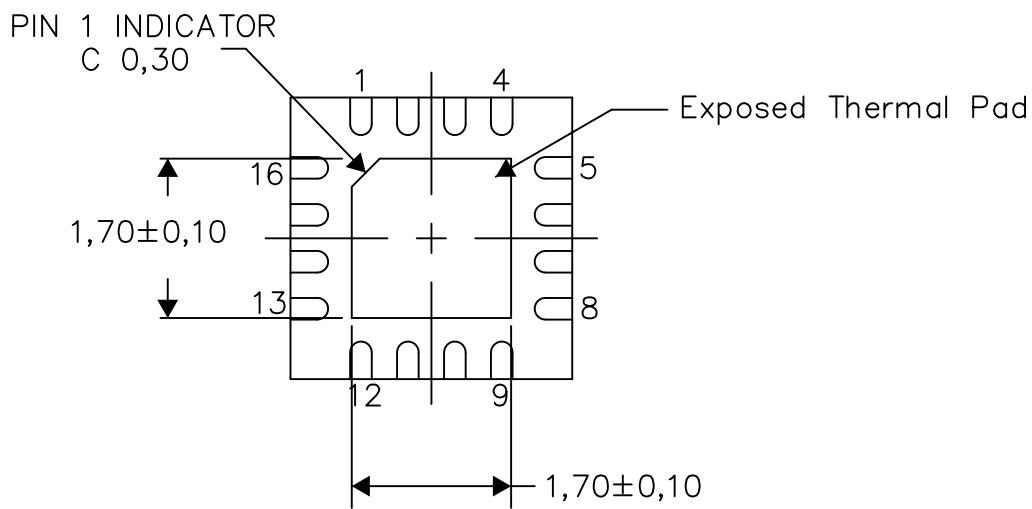
PLASTIC QUAD FLATPACK NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

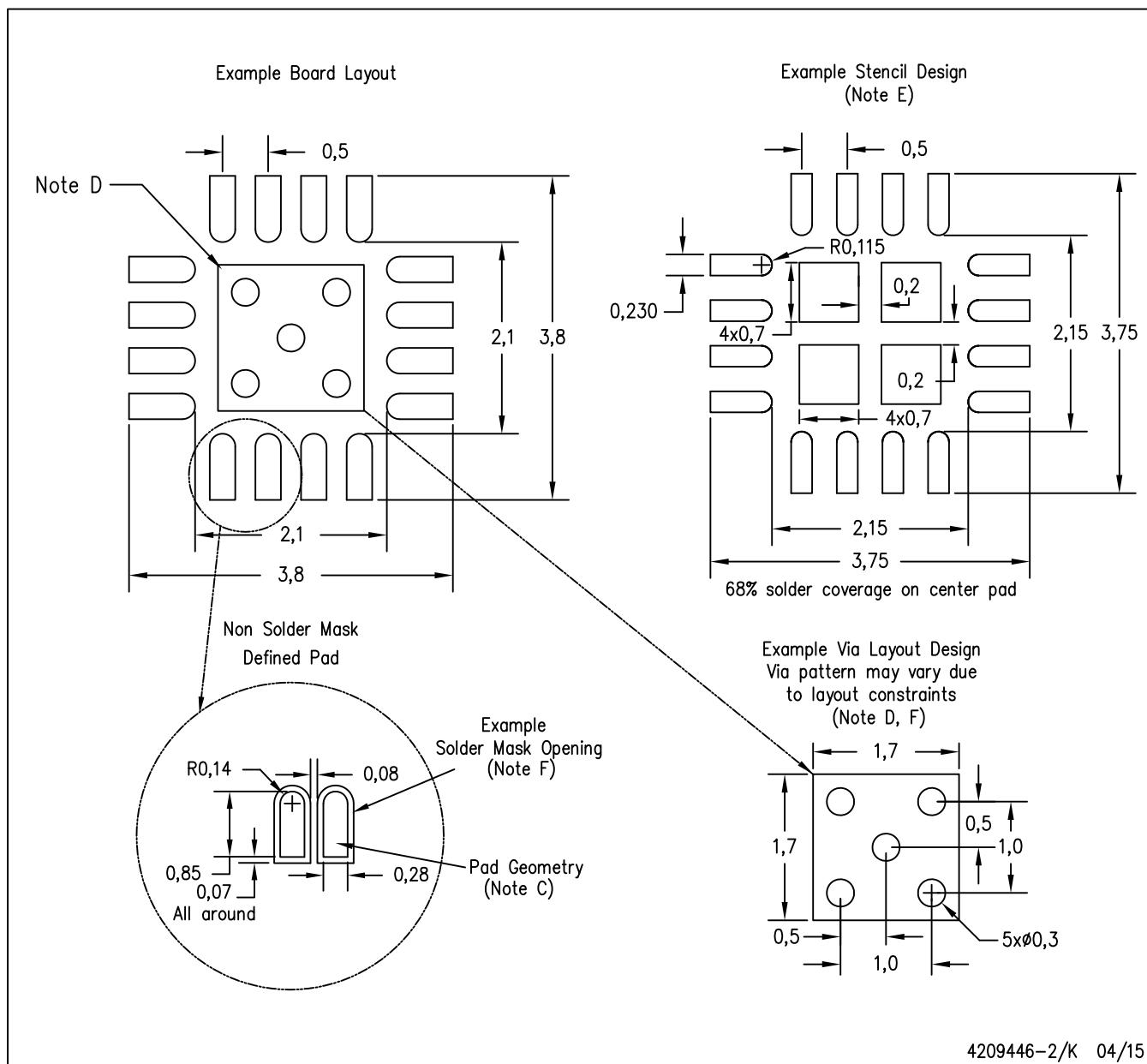
4206446-3/U 08/15

NOTE: A. All linear dimensions are in millimeters

## LAND PATTERN DATA

RTE (S-PWQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4209446-2/K 04/15

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

## THERMAL PAD MECHANICAL DATA

RTE (S-PWQFN-N16)

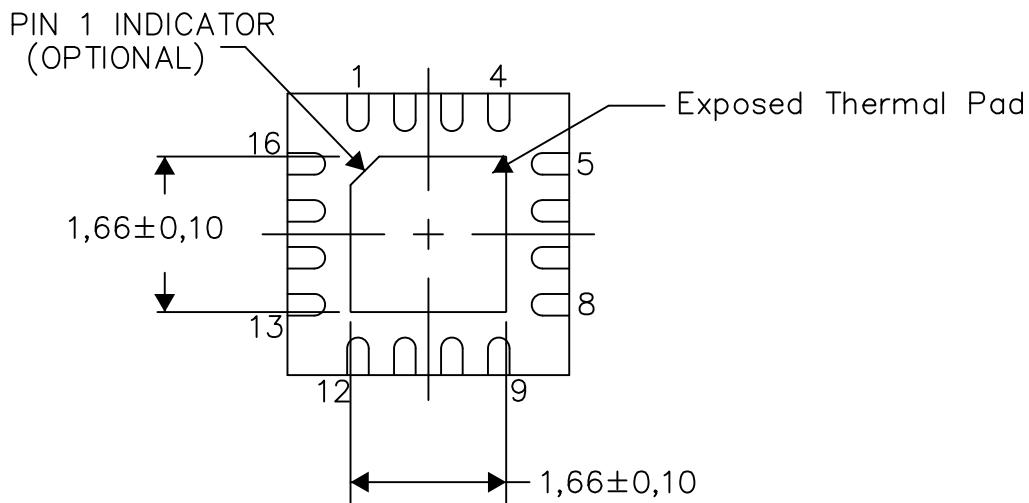
PLASTIC QUAD FLATPACK NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

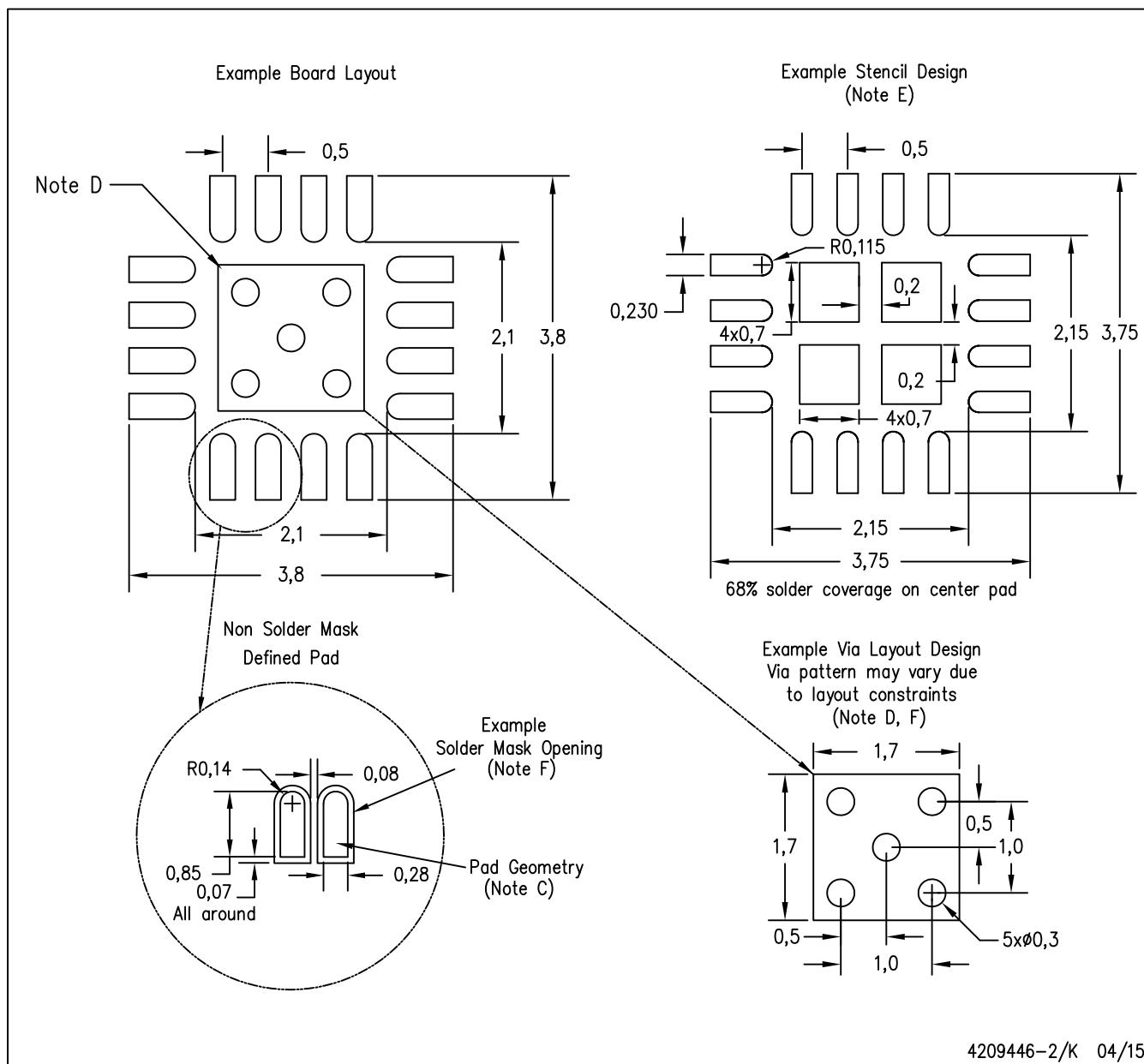
4206446-8/U 08/15

NOTE: A. All linear dimensions are in millimeters

# LAND PATTERN DATA

RTE (S-PWQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4209446-2/K 04/15

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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