NSPL 0.5㎛ Analog CMOS 2P3M 5V Design Rule

Version 1.0

National Semiconductor Public Laboratory (NSPL)

- Electronics and Telecommunications Research Institute (ETRI)
- Seoul National University (SNU)
- Daegu Gyeongbuk Institute of Science & Technology (DGIST)

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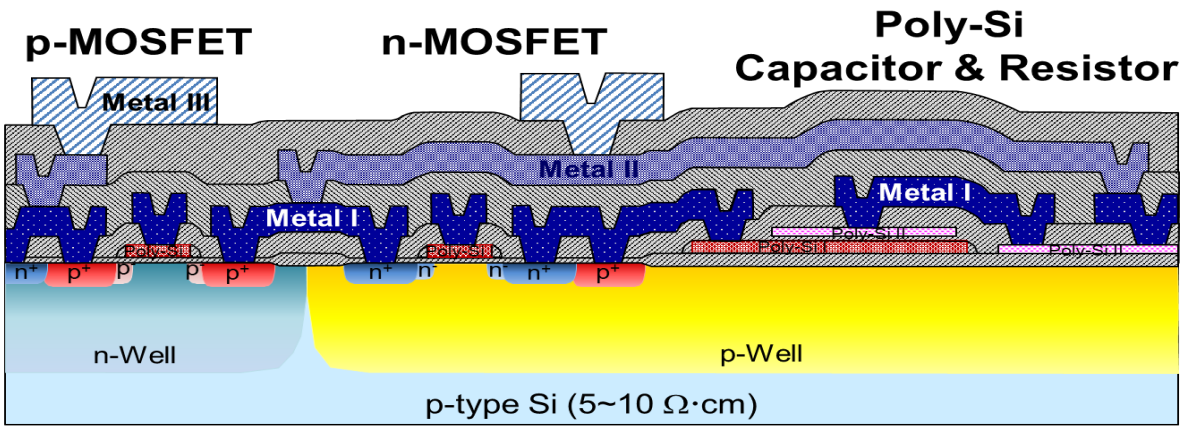
0. Revision History

Rev	Date	From	Description
1.00	2023.07.05	K.S. Park, J.I. Won, T.M. Roh	**Comes from "ETRI 0.5㎛ Analog CMOS 2P3M 5V Design Rule, Ver. 1.1" (T.M. Roh) and Modified/Added Below** **Modified Rules** 4.2 ACT Rules - 2.ACT.W1, 2.ACT.E3, 2.ACT.E5, 2.ACT.S 4.3 POLY1 Rules - 3.PL1.S2, 3.PL1.S3, 3.PL1.O 4.4 POLY2 Rules - 4.PL2.W 4.5 NSD Rules - 5.NSD.E 4.6 PSD Rules - 6.PSD.E 4.7 CONT Rules 4.9 VIA1 Rules - 9.VIA.S1, 9.VIA.E1, 9.VIA.E2, 9.VIA.E3, 9.VIA.E4, 9.VIA.S 4.11 VIA2 Rules - 11.VIA.S1, 11.VIA.E1, 11.VIA.E2, 11.VIA.E3, 11.VIA.E4, 11.VIA.S 4.14 Poly2 Resistor Rules - 14.PL2NR.E3, 14.PL2PR.E3 4.15 PIP Capacitor Rules - 15.CAP.S5 4.17 NPN BJT Rules - 17.PNP.E3 **Added Items** 1. Antenna rule - 3.PL1.ANT, 8.MET1.ANT, 10.MET2.ANT, 12.MET1.ANT
			Title **NSPL 0.5㎛ Analog CMOS 2P3M 5V Design Rule**
			Division **National Semiconductor Public Laboratory**

1. Technology Overview

1.1 Process Overview

- 0.5㎛ Analog CMOS (2-poly / 3-Metal)
- Single gate oxide 110Å for 5V CMOS
- Passive components: Poly-Si Resistor/Capacitor



1.2 Process Condition

- N-well lateral diffusion	: 1.40㎛ (70%)
- P-well lateral diffusion	: 1.40㎛ (70%)
- Field oxide encroachment	: 0.15㎛
- Spacer bias	: 0.18㎛
- N+ lateral diffusion	: 0.16㎛ (80%)
- P+ lateral diffusion	: 0.20㎛ (80%)

1.3 Align Tolerance

1) Direct alignment

- Critical layers	: ±0.15㎛
- Noncritical layers	: ±0.20㎛

2) Indirect alignment

: $[X12^2 + X23^2 + \cdots\cdots Xn(n+1)^2]^{0.5}$

Where Xim is the direct alignment tolerance between layer i and m.

2. Layer Information

2.1 Layers for Standard Process

Layer Name	Layer No.	Function	Digitized Area
KEY	1	Define Align key	C
NWELL	2	Define N-well for PMOS body	C
PWELL	3	Define P-well for NMOS body	C
ACT	11	Define Active area	D
POLY1	12	Define Poly-Si 1 for gate of transistor	D
POLY2	13	Define Poly-Si 2 for resistor and capacitor	D
NSD	14	Define N-type implant region for N-LDD and N+	C
PSD	15	Define N-type implant region for P-LDD and P+	C
ESDI	109	Define ESD implant	C
CONT	31	Define contact from MET1 to ACT, POLY1 and POLY2	C
MET1	32	Define Metal-1 for interconnection	D
VIA1	33	Define Via1 connecting MET1 and MET2	C
MET2	34	Define Metal-2 for interconnection	D
VIA2	35	Define Via2 connecting MET2 and MET3	C
MET3	36	Define Metal-3 for interconnection	D
PAD	37	Define open region of passivation for bonding pad	C

2.2 Layers for DRC, LVS and Text

Layer Name	Layer No.	Function	Digitized Area
POLY1TXT	41	Poly1 Text	
MET1TXT	42	MET1 Text	
MET2TXT	44	MET2 Text	
MET3TXT	46	MET3 Text	
PADTXT	47	PAD Text	
TEXT	48	Text	
RES	51	Poly-Si Resistor for DRC & LVS	
CAP	53	Poly-Si Capacitor for DRC & LVS	
HVMS	54	High Voltage MOSFET (Symmetric) for DRC & LVS	
HVMA	55	High Voltage MOSFET (Asymmetric) for DRC & LVS	
BJT	56	BJT for DRC & LVS	
DIODE	57	Diode for DRC & LVS	
NODRC	58	DRC check blocking layer	
ESDD	59	Define ESD device drain electrode	
LVSD	60	Extract Poly-Si Resistor/PIP CAP Area	
ESD	26	Define ESD device region for DRC	
DUMMY0	100		
DUMMY1	101		
DUMMY2	102		
DUMMY3	103		
DUMMY4	104		
DUMMY5	105		
DUMMY6	106		
DUMMY7	107		
DUMMY8	108		

2.3 Device layer table

- 0: Does not cover the structures
- 1: Covers or matches the structures

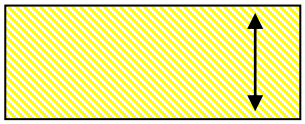
	Layer Name	NMOS	PMOS	N-Poly Res.	Poly Cap.	PNP-BJT*	P+/NW Diode	N+/PW Diode
Design Layers	NWELL	0	1	0	0	1	1	0
	PWELL	1	0	0	0	1	0	1
	ACT	1	1	0	0	1	1	1
	POLY1	1	1	0	1	0	0	0
	POLY2	0	0	1	1	0	0	0
	NSD	1	0	1	1	1	0	1
	PSD	0	1	0	0	1	1	0
	NHRI	0	0	0	0	0	0	0
	PHRI	0	0	0	0	0	0	0
Special Layers	RES	0	0	1	0	0	0	0
	LVSD	0	0	1	0	0	0	0
	CAP	0	0	0	1	0	0	0
	BJT	0	0	0	0	1	0	0
	DIODE	0	0	0	0	0	1	1

* PNP-BJT: Substrate PNP-BJT

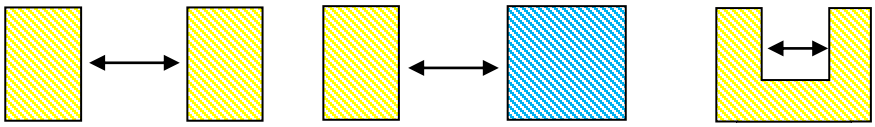
3. General Layout Information

3.1 Definition of Layout Layers

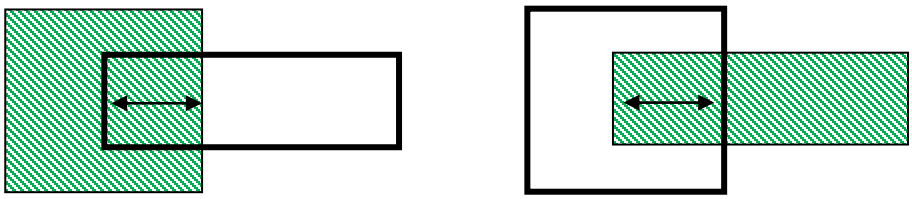
Width : Distance of interior-facing edge for a single layer (W)



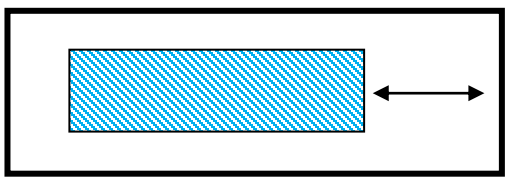
Space : Distance of exterior-facing edge for one or two layers (S)



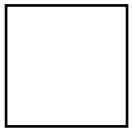
Overlap : Distance of interior-facing edge for two layers (O)

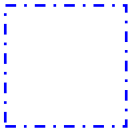


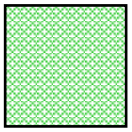
Extension : Distance of inside edge to outside edge (E)



3.2 Drawing Layer Symbols

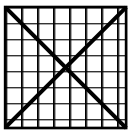

KEY


NSD

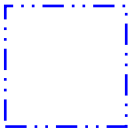

MET2

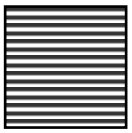

NWELL

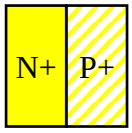

PSD


VIA2


PWELLL

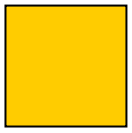

ESDI


MET3

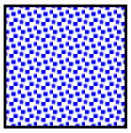


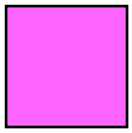
ACT

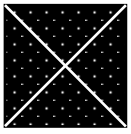

CONT


PAD


POLY1


MET1


POLY2


VIA1

3.3 General Information

- All rules are in microns (㎛)

- The design grid must be an integer multiple of 0.01 ㎛

- 0.01 ㎛ deviation is allowed for 45-degree polygon dimensions.

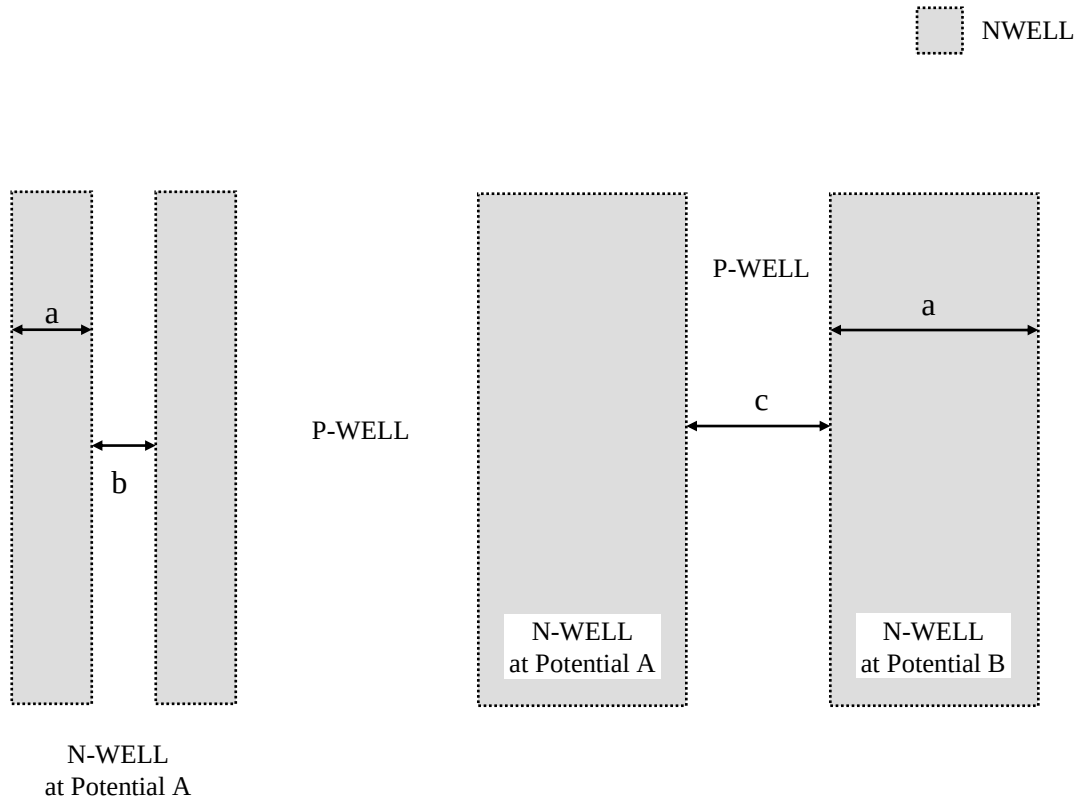
- Only shapes that are orthogonal or on a 45-degree angle are allowed.

4. Layout Rules and Guidelines

4.1 NWELL Rules

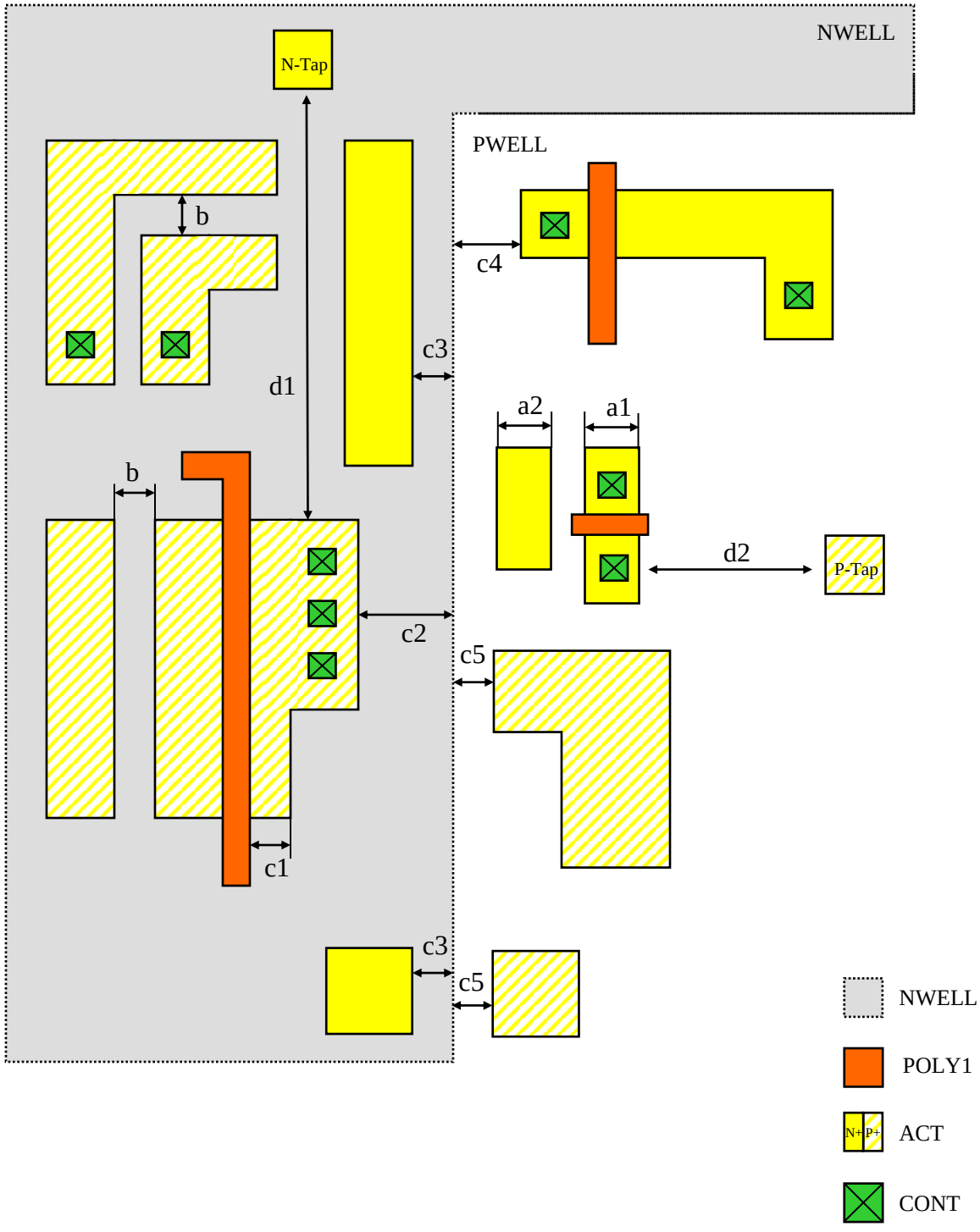
Rule No.	Description	Label		Value (㎛)
1.NWL.W	Width	a	≥	2.5
1.NWL.S.1	Space of two NWELL with same potential	b	≥	1.25
1.NWL.S.2	Space of two NWELL with different potential or resistor	c	≥	4.0
1.NWL.R	Resistor width		≥	5.0

*** PWELL is formed in reverse type of NWELL layer**



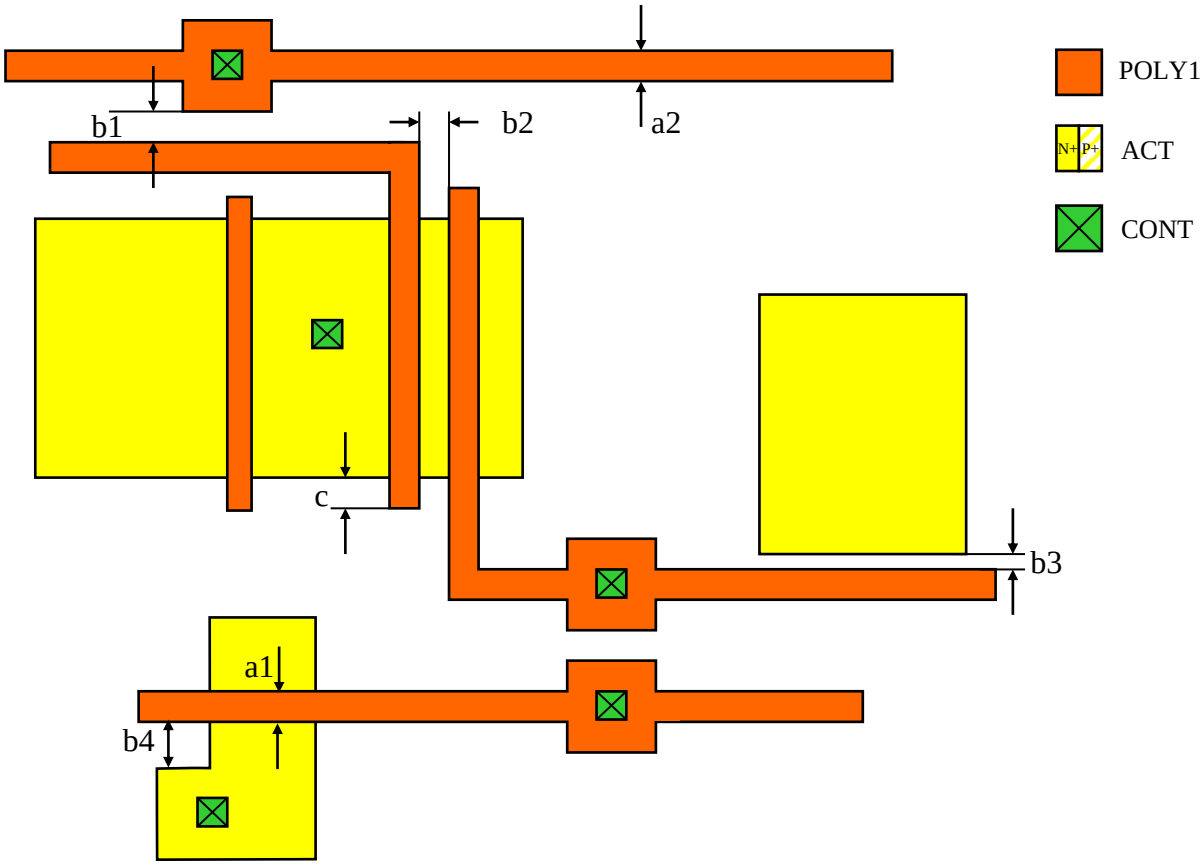
4.2 ACT Rules

Rule No.	Description	Label		Value (㎛)
2.ACT.W1	Minimum Transistor (N/PMOS) width	a1	≥	1.6
2.ACT.W2	Maximum Transistor (N/PMOS) width		≤	100
2.ACT.W3	Width of ACT region for interconnect	a2	≥	0.7
2.ACT.S	Space of two ACT	b	≥	1.0
2.ACT.E1	Extension of ACT beyond POLY1	c1	≥	0.85
2.ACT.E2	Extension of NWELL beyond ACT (P-type)	c2	≥	1.4
2.ACT.E3	Extension of NWELL beyond ACT (N-type)	c3	≥	0.5
2.ACT.E4	Extension of PWELL beyond ACT (N-type)	c4	≥	1.4
2.ACT.E5	Extension of PWELL beyond ACT (P-type)	c5	≥	0.5
2.ACT.T1	The maximum distance from any point in a N-tab to the nearest MOSFET in the same NWELL	d1	≤	60.0
2.ACT.T2	The maximum distance from any point in a P-tab to the nearest MOSFET in the same PWELL	d2	≤	60.0


NWELL
N-Tap
PWELL
b
c4
c3
d1
a2
a1
b
d2
P-Tap
c2
c5
c1
c3
c5
NWELL
POLY1
N+P+
ACT
CONT

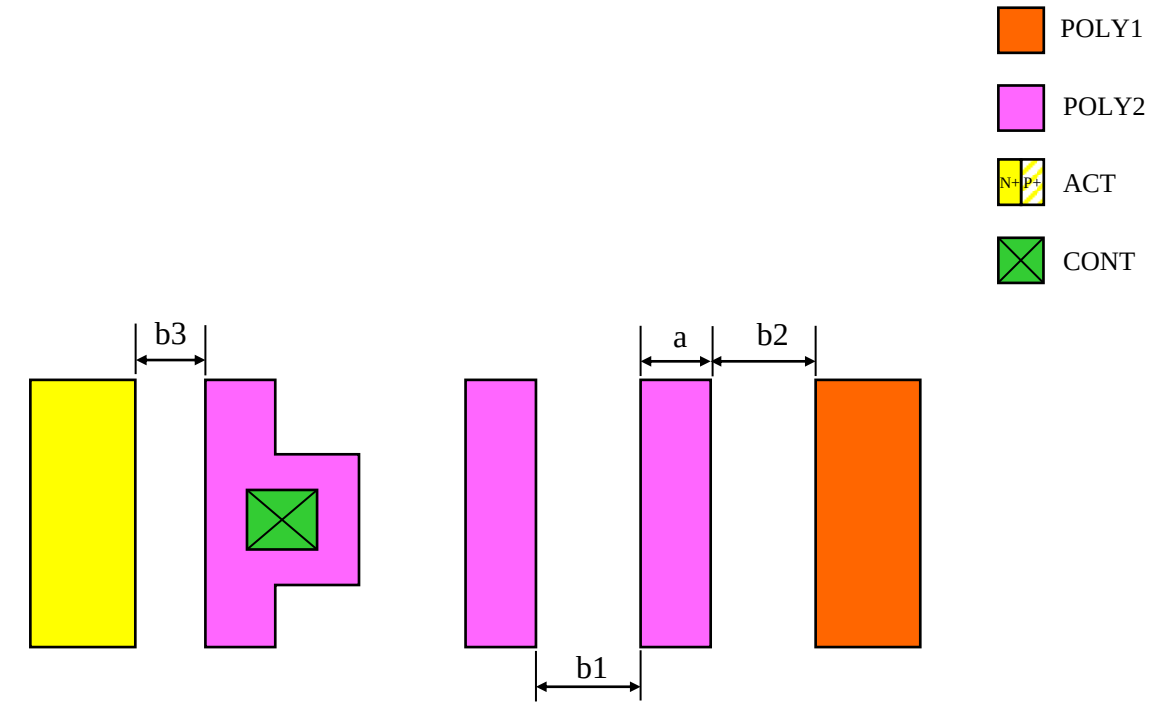
4.3 POLY1 Rules

Rule No.	Description	Label		Value (㎛)
3.PL1.W1	POLY1 width over ACT (NMOS or PMOS)	a1	≥	0.5
3.PL1.W2	Maximum POLY1 width (Transistor Channel Length)	a1	≤	100.0
3.PL1.W3	POLY1 width for interconnect	a2	≥	0.5
3.PL1.S1	POLY1 to POLY1 space in field	b1	≥	0.6
3.PL1.S2	POLY1 to POLY1 space on ACT	b2	≥	0.6
3.PL1.S3	Space from POLY1 in field to ACT	b3	≥	0.5
3.PL1.S4	ACT space to POLY1 in field	b4	≥	0.5
3.PL1.O	Overlap of POLY1 extended into field oxide	c	≥	0.5
3.PL1.ANT	Maximum ratio of field poly area to gate poly for a given transistor(antenna rule)		≤	200



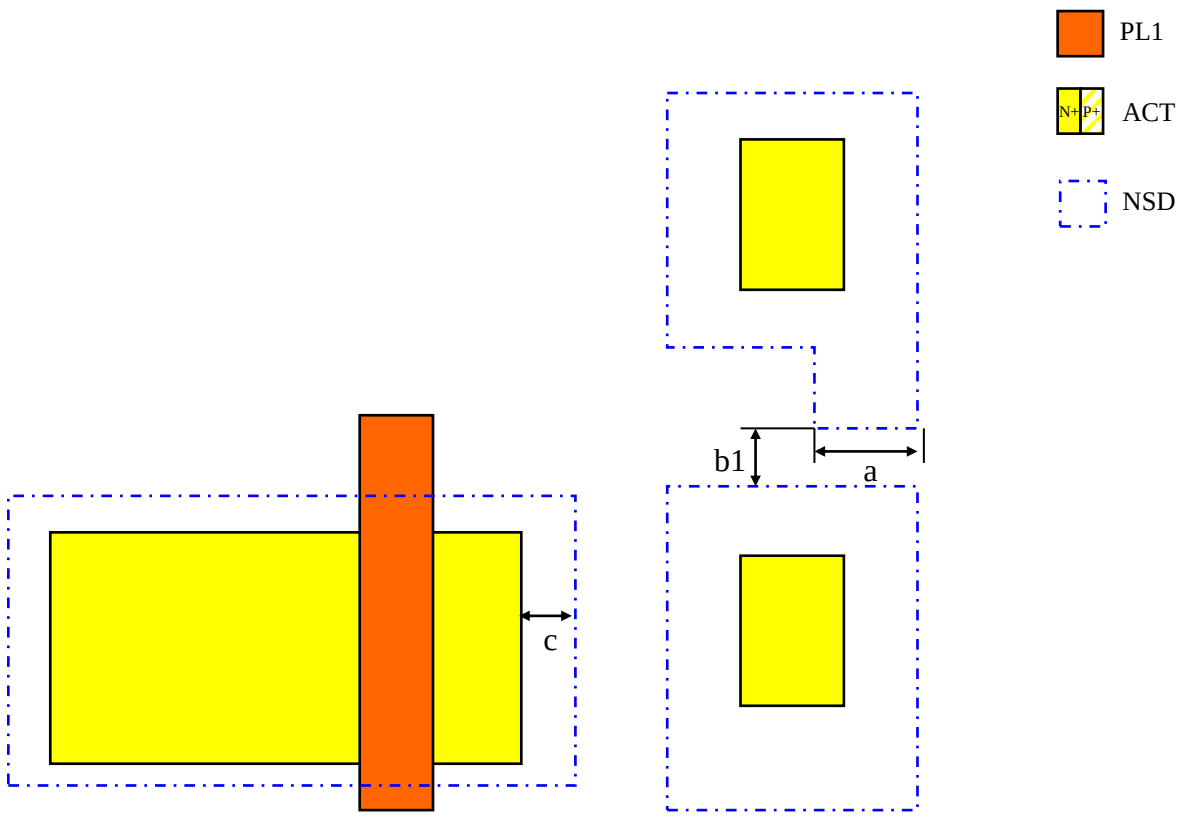
4.4 POLY2 Rules

Rule No.	Description	Label		Value (㎛)
4.PL2.W	POLY2 width	a	≥	0.6
4.PL2.S1	Space of two POLY2	b1	≥	0.75
4.PL2.S2	Space from POLY2 to POLY1	b2	≥	0.75
4.PL2.S3	Space from POLY2 to ACT	b3	≥	0.5



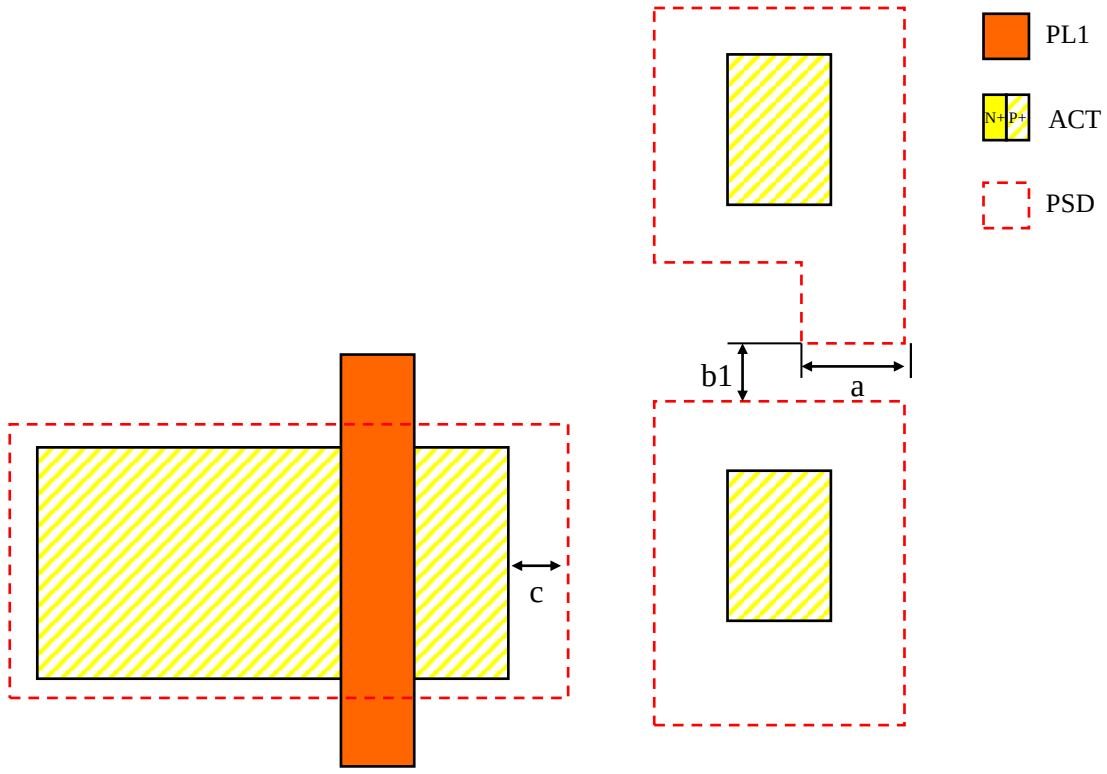
4.5 NSD Rules

Rule No.	Description	Label		Value (㎛)
5.NSD.W	Width	a	≥	0.75
5.NSD.S1	Space of two NSD Merge if the space is less than 0.75㎛	b	≥	0.75
5.NSD.E	Extension of ACT to NSD	c	≥	0.5
5.NSD.O	NSD overlapping with PSD is not allowed			



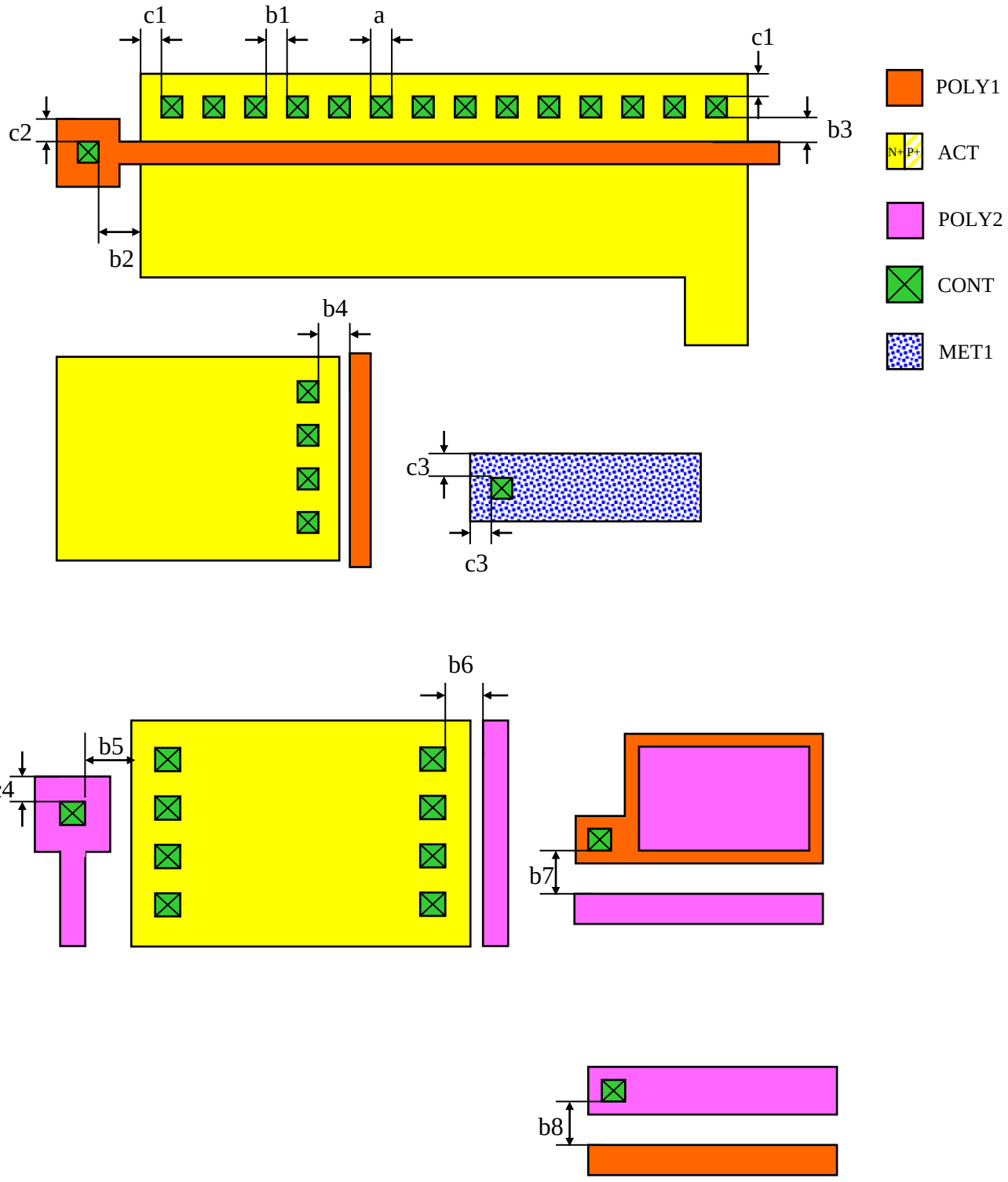
4.6 PSD Rules

Rule No.	Description	Label		Value (㎛)
6.PSD.W	Width	a	≥	0.75
6.PSD.S1	Space of two PSD Merge if the space is less than 0.75㎛	b	≥	0.75
6.PSD.E	Extension of ACT to PSD	c	≥	0.5
6.PSD.O	PSD overlapping with NSD is not allowed			



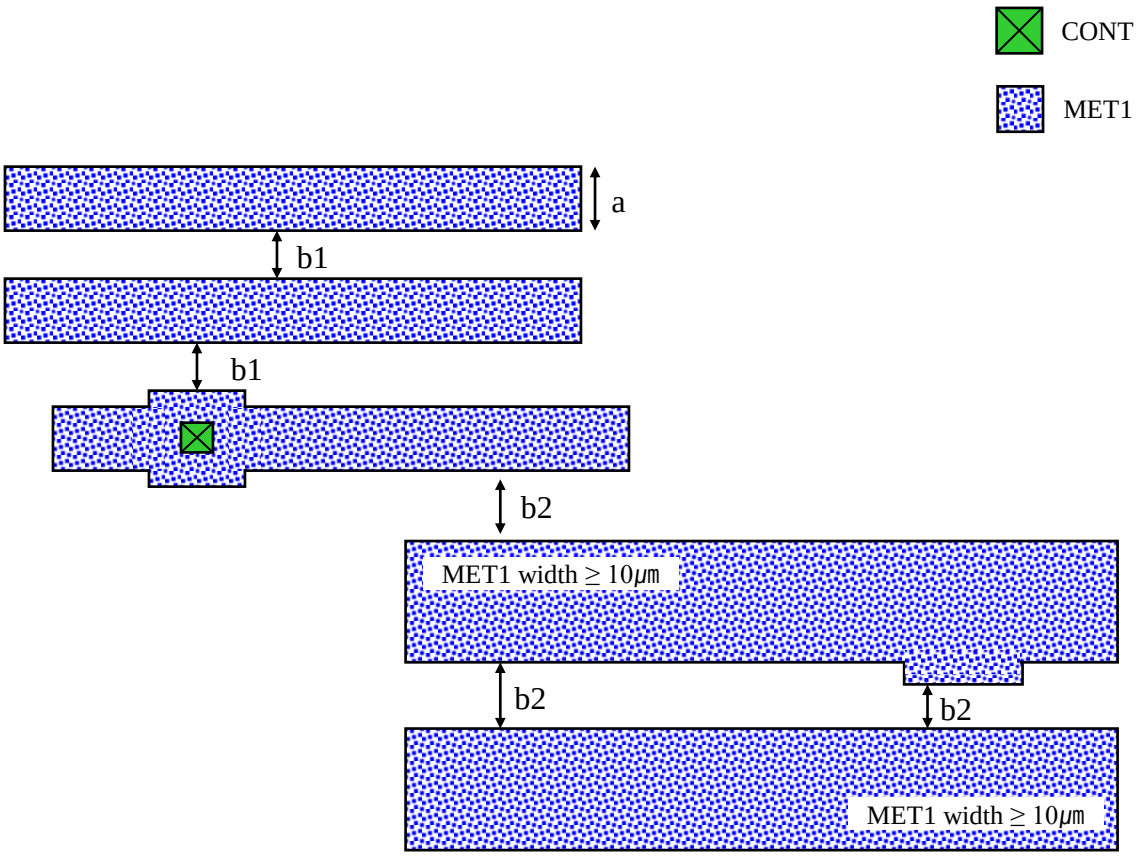
4.7 CONT Rules

Rule No.	Description	Label		Value (㎛)
7.CONT.W	Min/Max size	a		0.6 x 0.6 0.6 x 1.2
7.CONT.S1	Space of two CONT	b1	≥	0.6
7.CONT.S2	Space from CONT in POLY1 to ACT	b2	≥	1.0
7.CONT.S3	Space from CONT in ACT to POLY1 in ACT	b3	≥	0.75
7.CONT.S4	Space from CONT in ACT to POLY1 in field	b4	≥	0.75
7.CONT.S5	Space from CONT in POLY2 to ACT	b5	≥	1.0
7.CONT.S6	Space from CONT in ACT to POLY2	b6	≥	1.0
7.CONT.S7	Space form CONT in POLY1 to POLY2 for resistor	b7	≥	1.25
7.CONT.S8	Space form CONT in POLY2 to POLY1	b8	≥	1.25
7.CONT.E1	Extension of CONT to ACT	c1	≥	0.5
7.CONT.E2	Extension of CONT to POLY1	c2	≥	0.5
7.CONT.E3	Extension of CONT to MET1	c3	≥	0.6
7.CONT.E4	Extension of CONT to POLY2	c4	≥	0.5


c1
b1
a
c1
c2
b3
b2
b4
c3
c3
POLY1
N+
P+
ACT
POLY2
CONT
MET1
b6
b5
c4
b7
b8

4.8 MET1 Rules

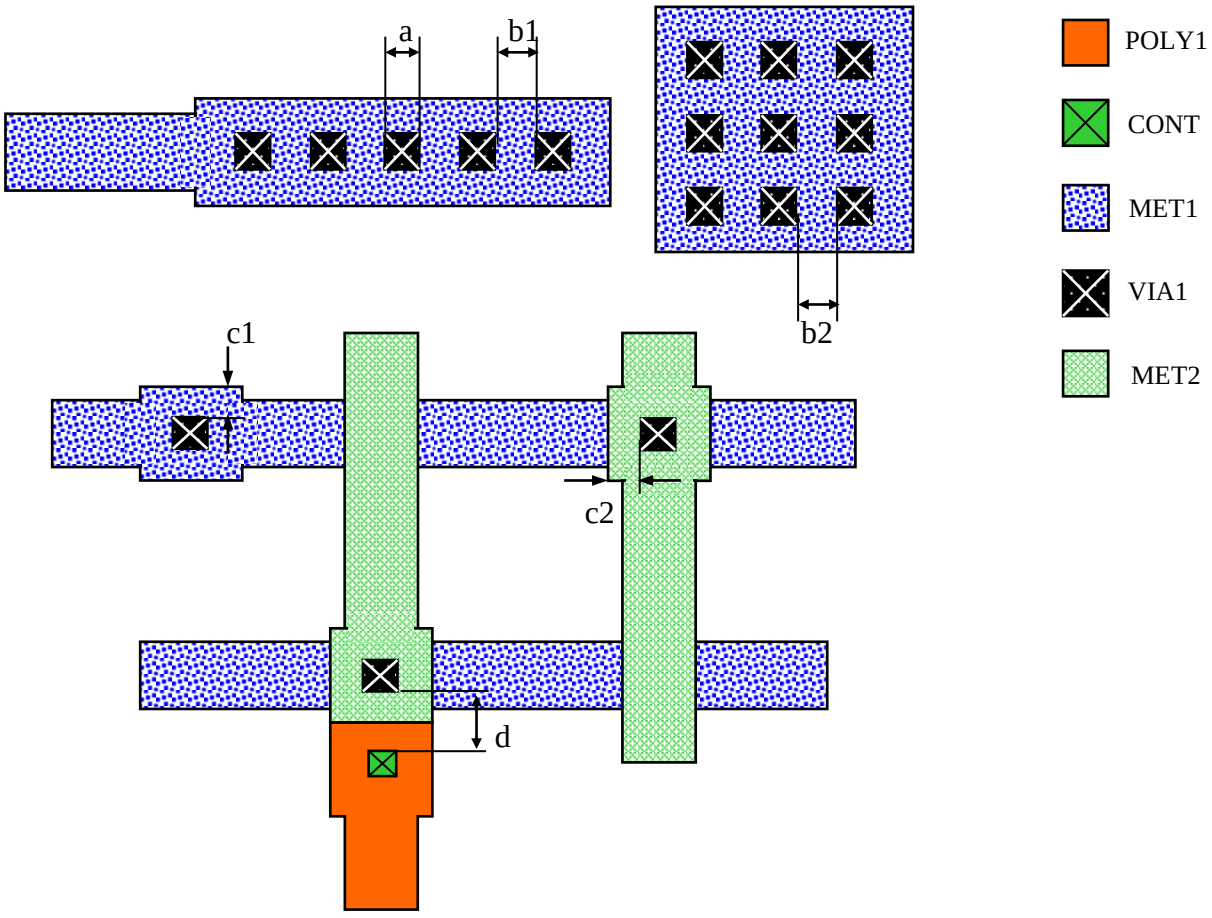
Rule No.	Description	Label		Value (μm)
8.MET1.W	Width	a	≥	0.8
8.MET1.S1	Space of MET1 (both MET1 width < 10μm)	b1	≥	0.8
8.MET1.S2	Space of wide MET1 (one or both MET1 width ≥ 10μm)	b2	≥	1.0
8.MET1.ANT	Maximum ratio of MET1 area to associated gate poly area for a given transistor(antenna rule)		≤	400



4.9 VIA1 Rules

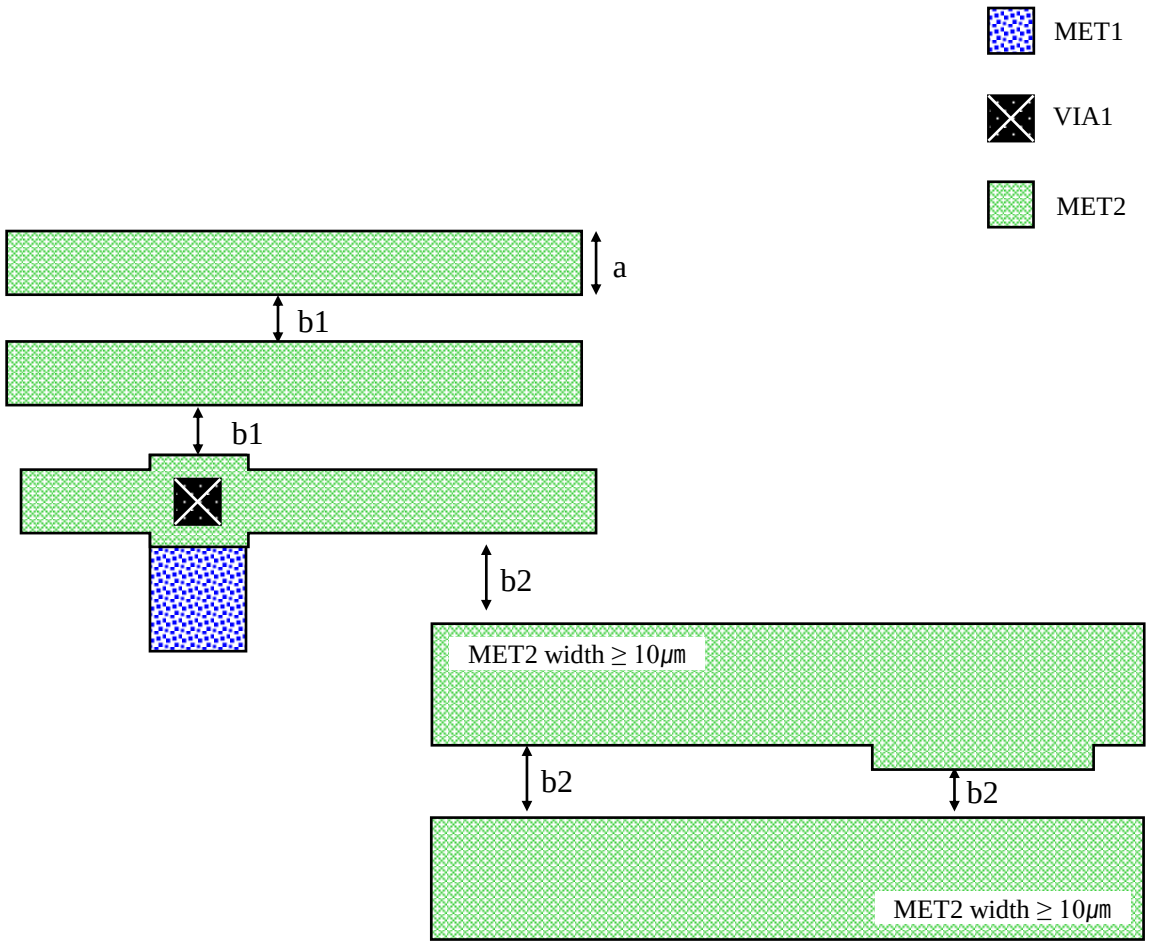
Rule No.	Description	Label		Value (μm)
9.VIA1.W	Min/Max size	a		0.8 x 0.8
9.VIA1.S1	Space of two VIA1	b1	≥	0.8
9.VIA1.S2	Space in VIA1 array [VIA1 number ≥ 3 x 3]	b2	≥	0.8
9.VIA1.E1	Extension of VIA1 to MET1 (Width < 10μm)	c1	≥	0.6
9.VIA1.E2	Extension of VIA1 to wide MET1 (width ≥ 10μm)		≥	0.6
9.VIA1.E3	Extension of VIA1 to MET2 (Width < 10μm)	c2	≥	0.6
9.VIA1.E4	Extension of VIA1 to wide MET2 (width ≥ 10μm)		≥	0.6
9.VIA1.S	Space from VIA1 to CONT * VIA1 can not be stacked on CONT	d	≥	0.6

*** Single VIA1 is not recommended**



4.10 MET2 Rules

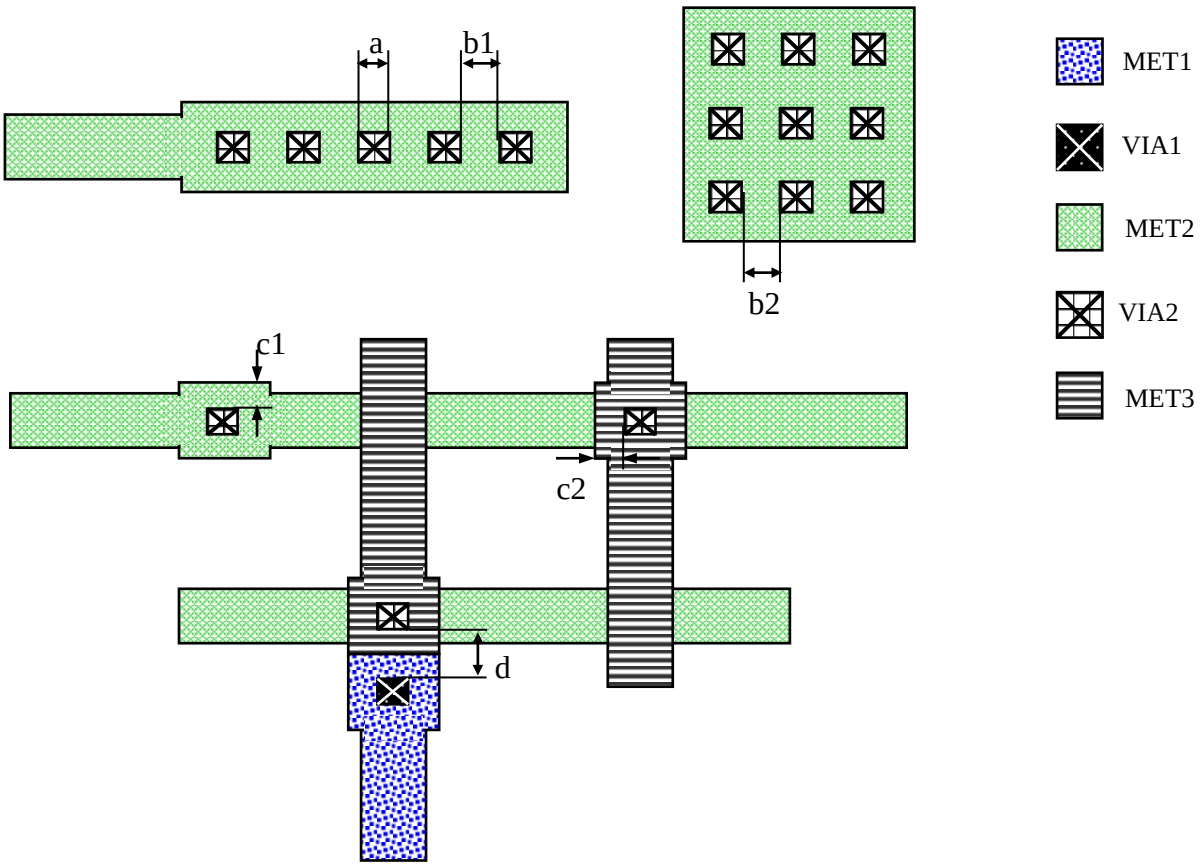
Rule No.	Description	Label		Value (μm)
10.MET2.W	Width	a	≥	1.0
10.MET2.S1	Space of MET2 (both MET2 width < 10μm)	b1	≥	1.0
10.MET2.S2	Space of wide MET2 (one or both MET2 width ≥ 10μm)	b2	≥	1.2
10.MET2.ANT	Maximum ratio of MET2 area to associated gate poly area for a given transistor(antenna rule)		≤	400



4.11 VIA2 Rules

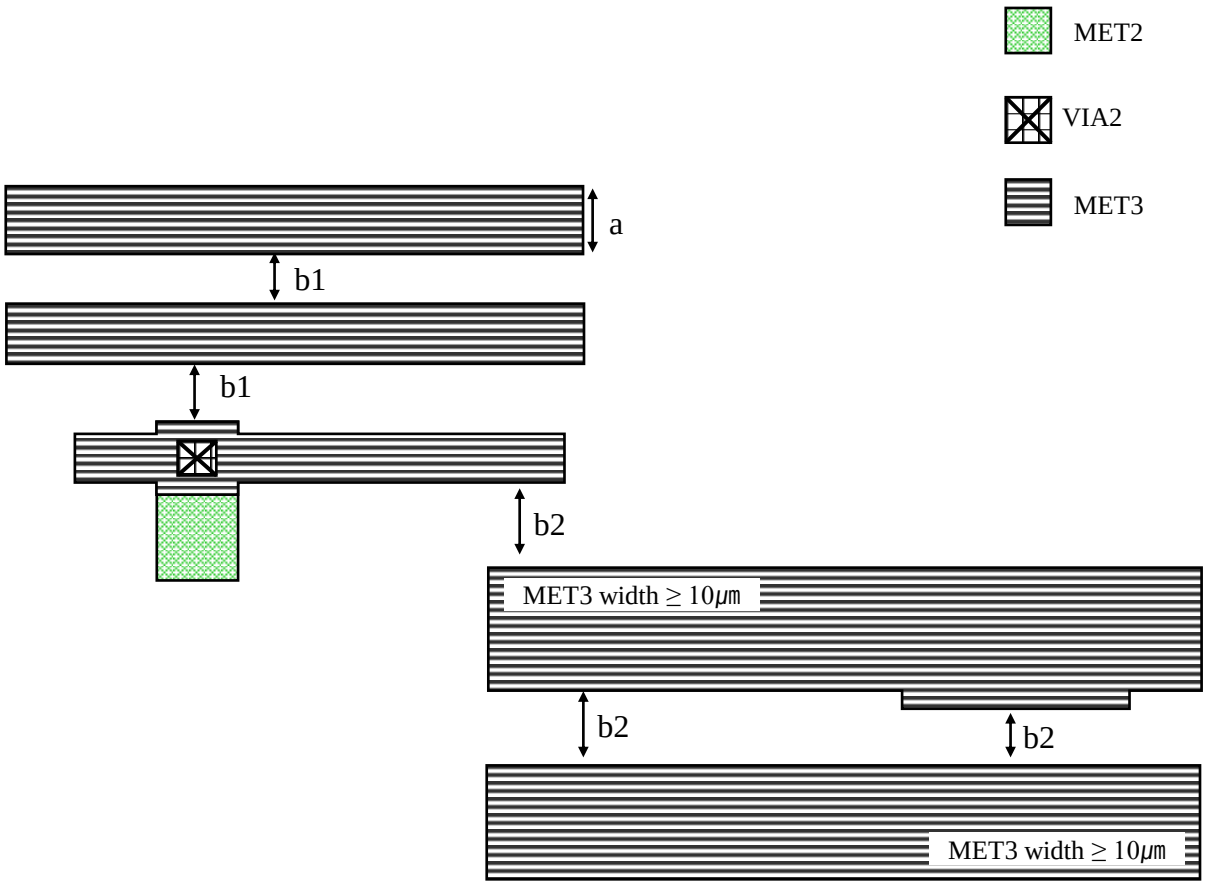
Rule No.	Description	Label		Value (μm)
11.VIA2.W	Min/Max size	a		0.8 x 0.8
11.VIA2.S1	Space of two VIA2	b1	≥	0.8
11.VIA2.S2	Space in VIA1 array [VIA1 number ≥ 3 x 3]	b2	≥	0.8
11.VIA2.E1	Extension of VIA2 to MET2 (Width < 10μm)	c1	≥	0.6
11.VIA2.E2	Extension of VIA2 to wide MET2 (width ≥ 10μm)		≥	0.6
11.VIA2.E3	Extension of VIA2 to MET3 (Width <10μm)	c2	≥	0.6
11.VIA2.E4	Extension of VIA2 to wide MET3 (width ≥ 10μm)		≥	0.6
11.VIA2.S	Space from VIA2 to VIA1 * VIA2 can not be stacked on VIA1	d	≥	0.6

*** Single VIA2 is not recommended**



4.12 MET3 Rules

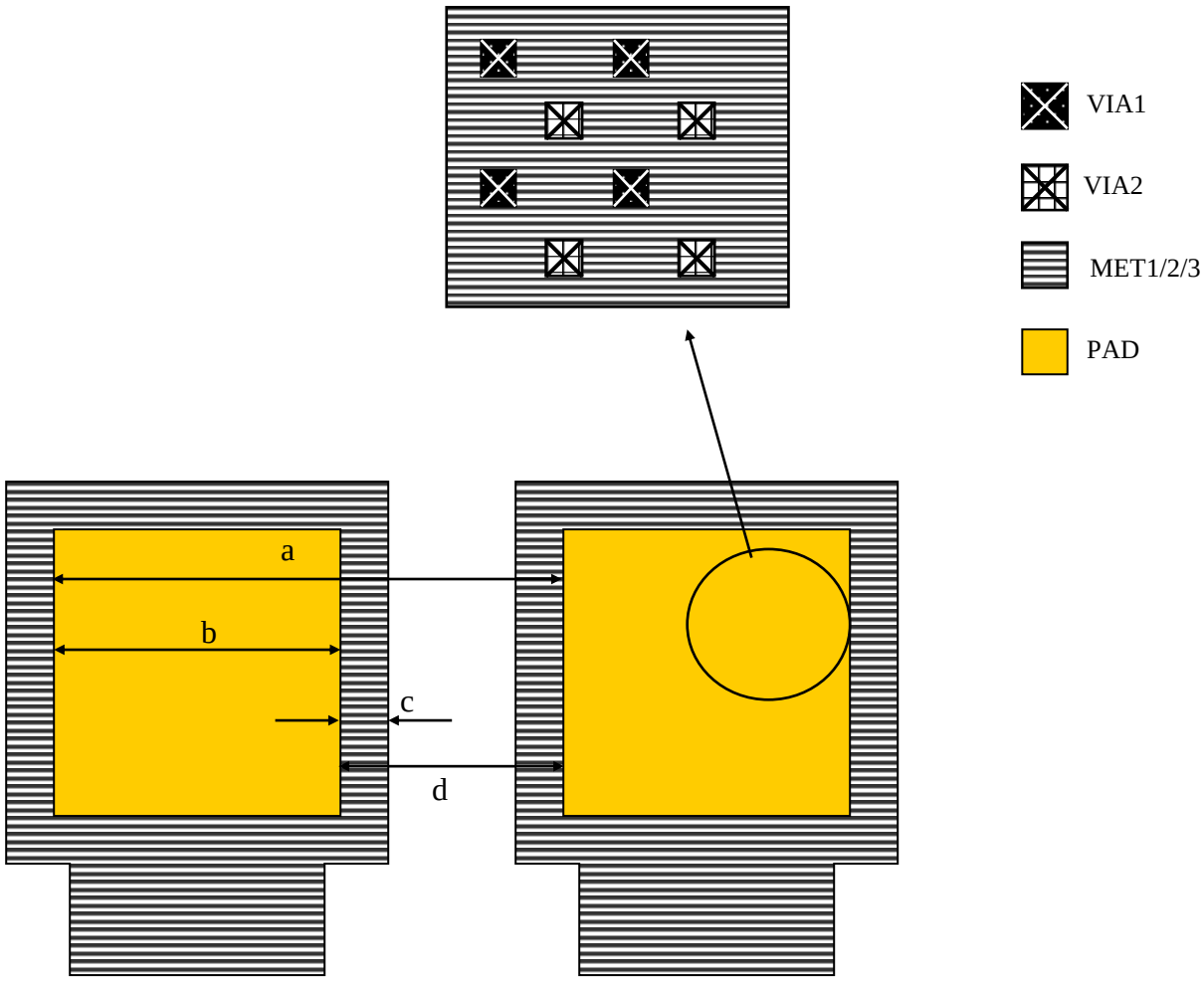
Rule No.	Description	Label		Value (μm)
12.MET3.W	Width	a	≥	1.2
12.MET3.S1	Space of MET3 (both MET3 width < 10μm)	b1	≥	1.0
12.MET3.S2	Space of wide MET3 (one or both MET3 width ≥ 10μm)	b2	≥	1.2
12.MET3.ANT	Maximum ratio of MET3 area to associated gate poly area for a given transistor(antenna rule)		≤	400



4.13 PAD Rules

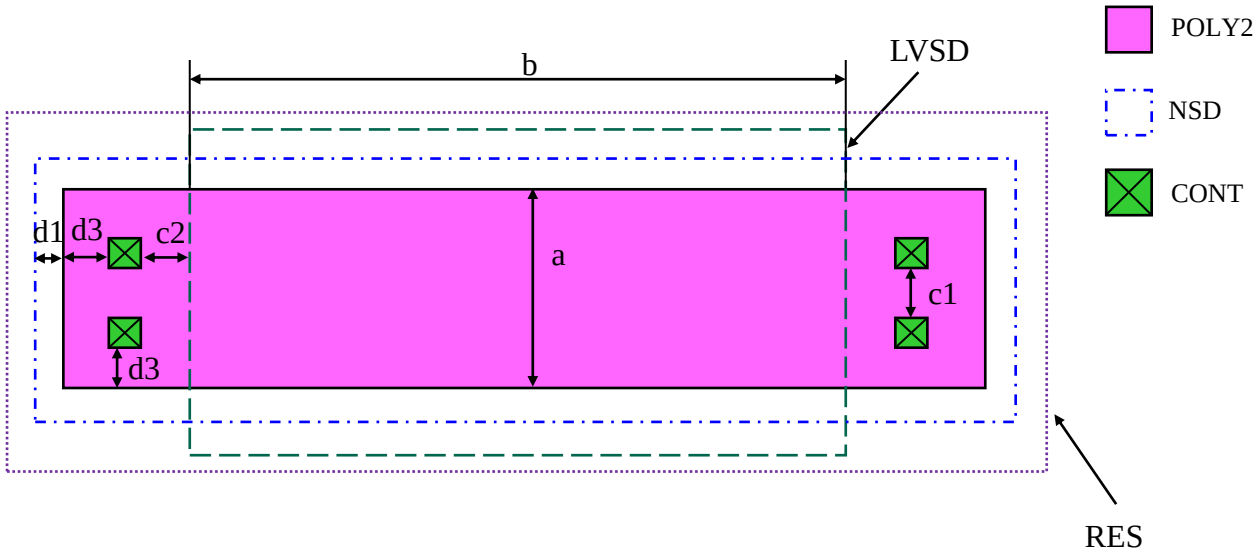
Rule No.	Description	Label		Value (㎛)
13.PAD.P	Pitch	a	≥	120
13.PAD.A	Size	b	≥	80 x 80
13.PAD.E	Extension of PAD to MET1/2/3	c	≥	2.5
13.PAD.S	Space	d	≥	40

*** The metals (MET1/2/3) under the PAD are connected via VIA1 and VIA2.**



4.14 Poly2 Resistor Rules (N-type)

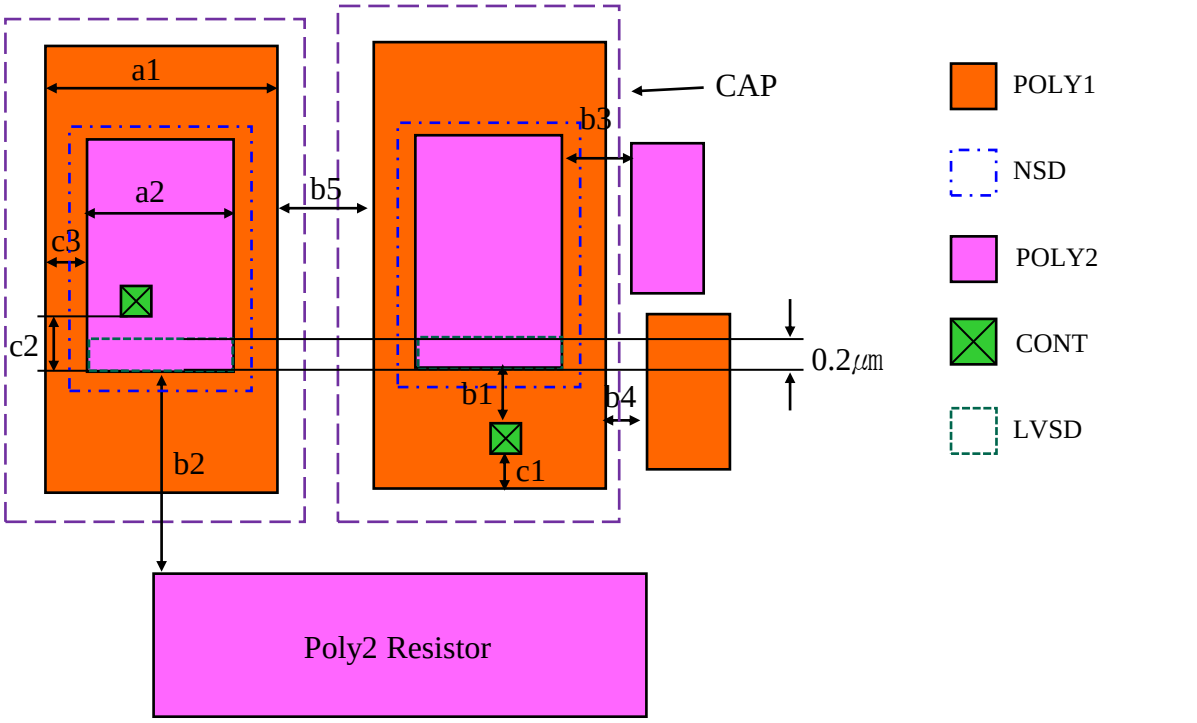
Rule No.	Description	Label		Value (㎛)
14.PL2NR.W	Width	a	≥	2.0
14.PL2NR.L	Length	b	≥	4.0
14.PL2NR.S1	Space of two CONT on PL2	c1	≥	0.6
14.PL2NR.S2	Space of CONT to LVSD	c2	≥	0.8
14.PL2NR.E1	Extension of PL2 to NSD	d1	≥	0.8
14.PL2NR.E2	Extension of PL2 to NHRI	d2	≥	0.8
14.PL2NR.E3	Extension of CONT to PL2	d3	≥	0.5



4.15 PIP Capacitor Rules

Rule No.	Description	Label		Value (㎛)
15.CAP.W1	POLY1 width	a1	≥	4.6
15.CAP.W2	POLY2 width	a2	≥	2.6
15.CAP.S1	Space from CONT in POLY1 to POLY2	b1	≥	1.0
15.CAP.S2	Space from POLY2 (CAP) to POLY2 (RES)	b2	≥	2.0
15.CAP.S3	Space from POLY2 (CAP) to POLY2 (Interconnect)	b3	≥	2.0
15.CAP.S4	Space from POLY1 (CAP) to POLY1 (Interconnect)	b4	≥	1.0
15.CAP.S5	Space from POLY1 (CAP) to POLY1 (CAP)	b5	≥	1.0
15.CAP.E1	Extension of CONT to POLY1	c1	≥	1.0
15.CAP.E2	Extension of CONT to POLY2	c2	≥	1.0
15.CAP.E3	Extension of POLY2 to POLY1	c3	≥	1.0

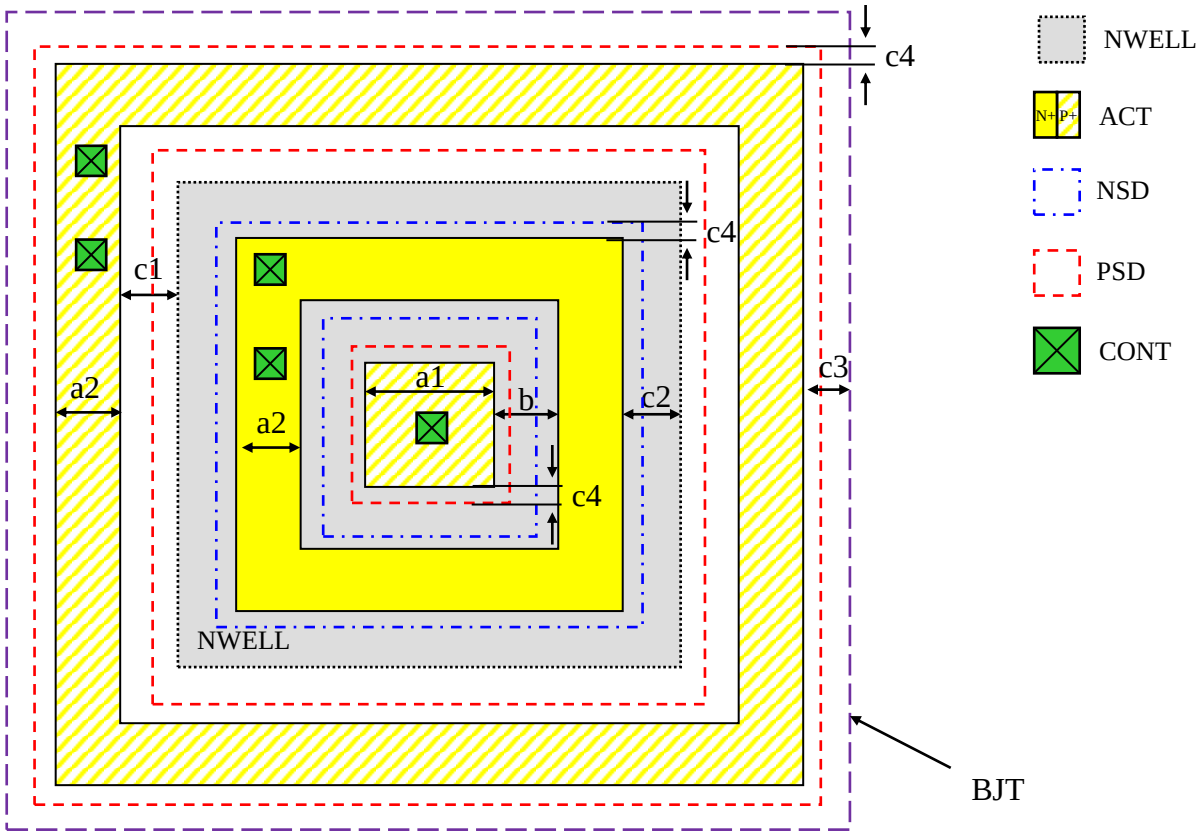
***Capacitor must be formed on field oxide**
****POLY2 must be inside POLY1**
***** LVSD length is must 0.2㎛ (for LVS check)**



4.16 PNP BJT Rules

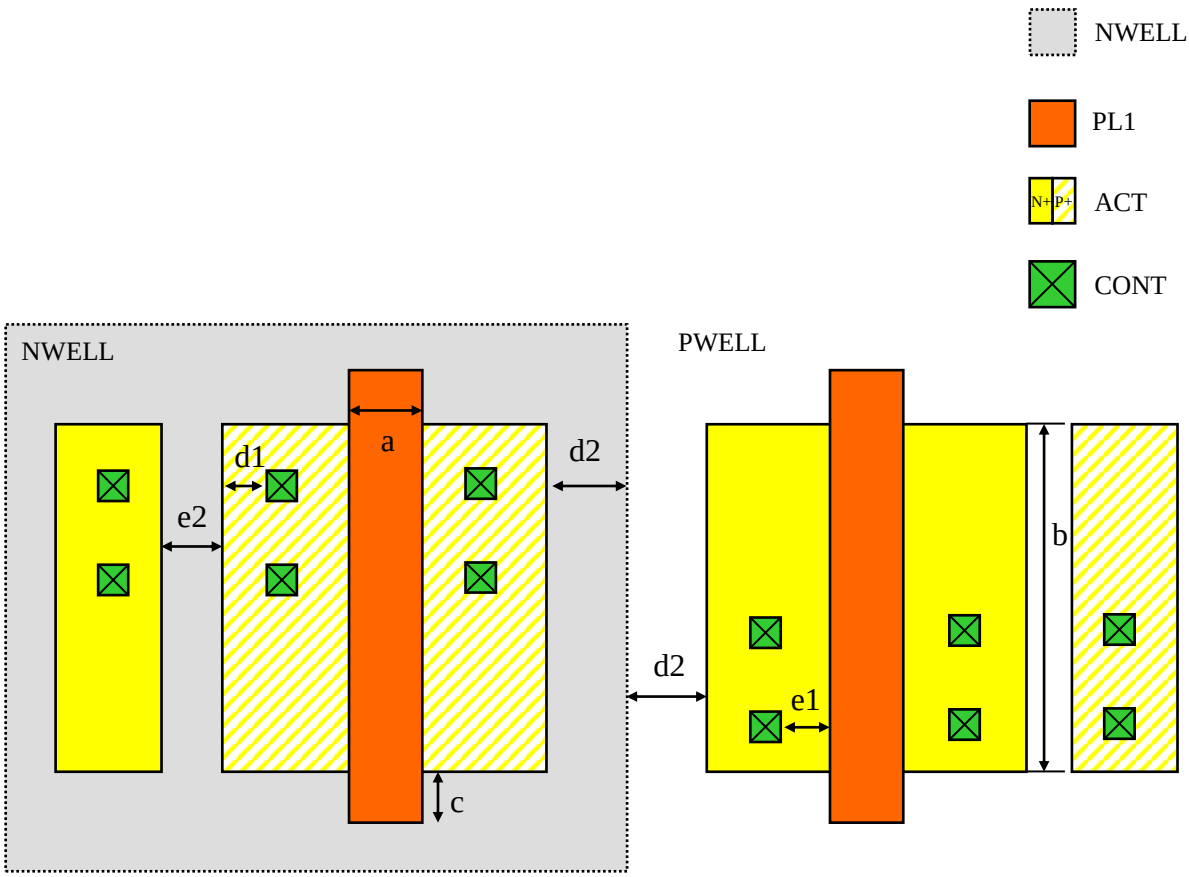
Rule No.	Description	Label		Value (㎛)
16.PNP.W1	Emitter width/length In case of Emitter size (W/L): 2/5/10	a1		2 x 2 5 x 5 10 x 10
16.PNP.W2	ACT (Collector, Base) width	a2	=	2.0
16.PNP.S	Space of two ACT (Base, Emitter)	b	=	4.5
16.PNP.E1	Extension of ACT (Collector) to PWELL	c1	=	4.5
16.PNP.E2	Extension of ACT (Base) to NWELL	c2	=	2.0
16.PNP.E3	Extension of ACT (Collector) to BJT	c3	≥	4.5
16.PNP.E4	Extension of ACT to NSD/PSD	c4	≥	1.0

Note)
1. PNP-BJT structure should be drawn symmetrically as donut



4.17 N/PMOS Guideline

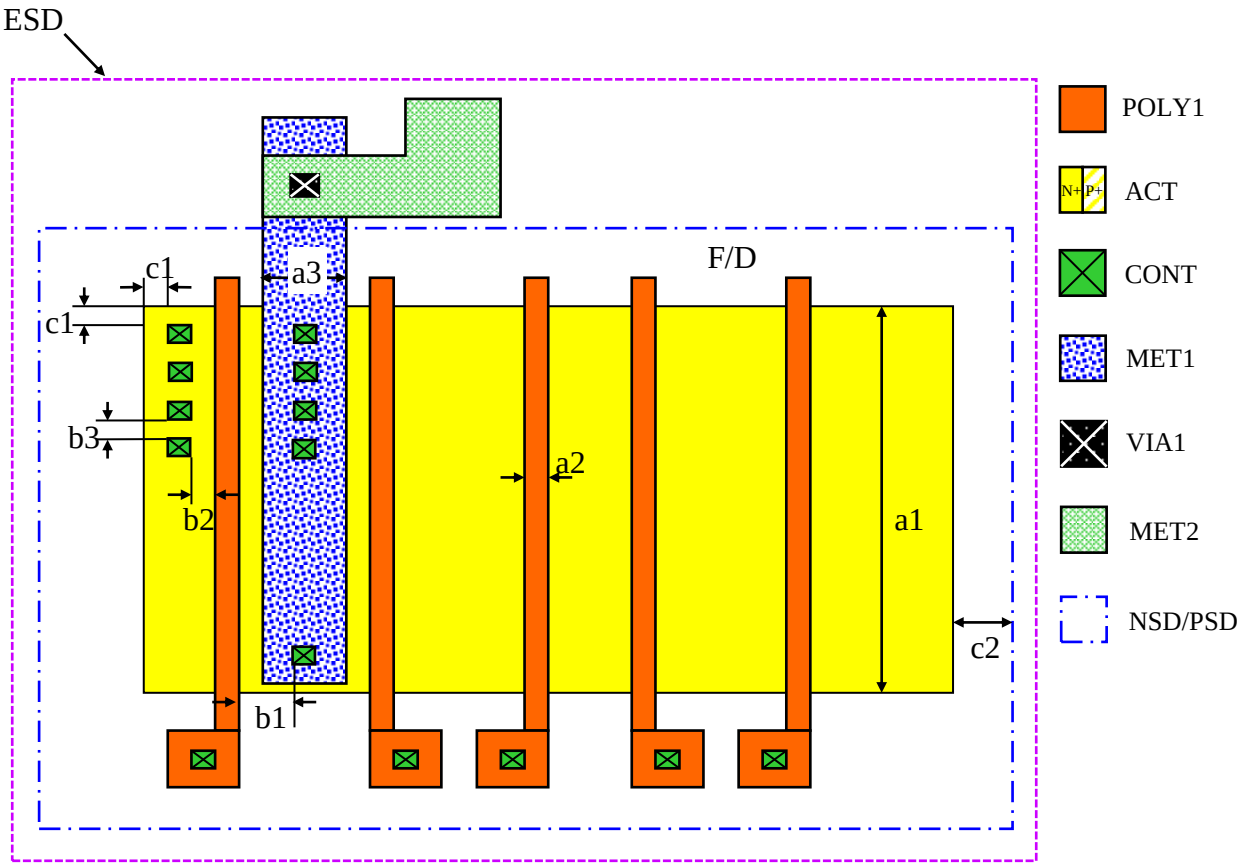
Rule No.	Description	Label		Value (㎛)
3.PL1.W1	PL1 width over ACT (Gate Length)	a	≥	0.5
2.ACT.W1	Transistor (N/PMOS) width	b	≥	1.6
3.PL1.O	Overlap of PL1 extended into field oxide	c	≥	0.5
7.CONT.E1	Extension of CONT to ACT	d1	≥	0.5
2.ACT.E2	Extension of NWL or PWL beyond ACT	d2	≥	1.4
7.CONT.S3	Space from CONT in ACT to PL1 in ACT	e1	≥	0.75
2.ACT.S	Space of two ACT	e2	≥	1.0



4.18 I/O ESD Protection Device Design Guideline

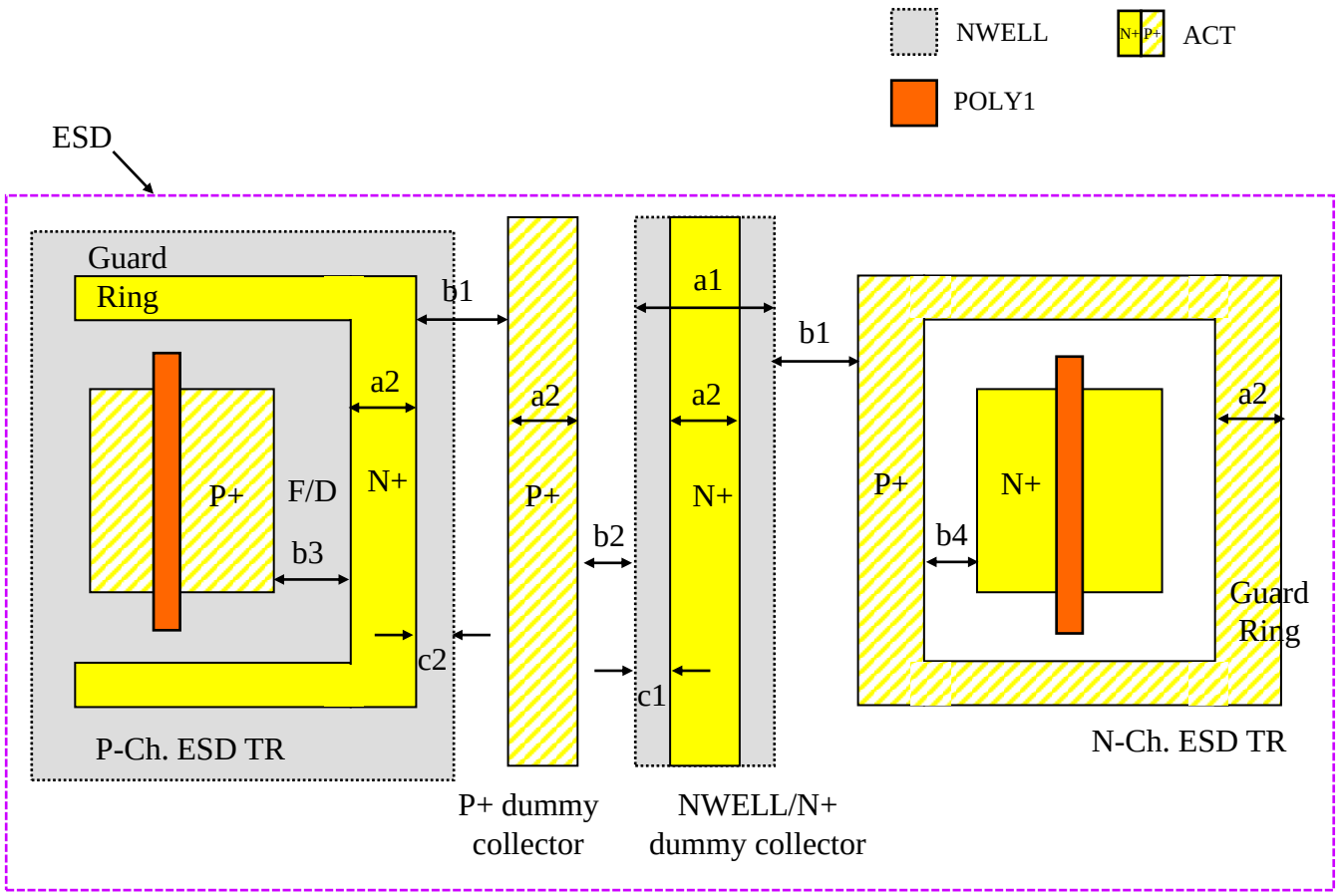
Rule No.	Description	Label		Value (㎛)
19.IO.F	ESD protection devices follow finger design with unique finger dimension and layout style.			
19.IO.W1	Total finger width for ESD protection		≥	720
19.IO.W2	Unit finger width	a1	≥	60
19.IO.W3	n/p-channel gate length	a2	≥	0.7
19.IO.W4	Metal width on drain side	a3	≥	6.0
19.IO.S1	DCGS (drain contact to gate space)	b1	≥	4.0
19.IO.S2	SCGS (source contact to gate space)	b2	≥	1.0
19.IO.S3	Space of two CONT	b3	≥	0.8
19.IO.E1	Extension of CONT to ACT for ESD protection	c1	≥	1.0
19.IO.E2	Extension of ACT to NSD/PSD	c2	≥	1.0

***The ESDD layer must be used over the drain region of ESD Transistor.**

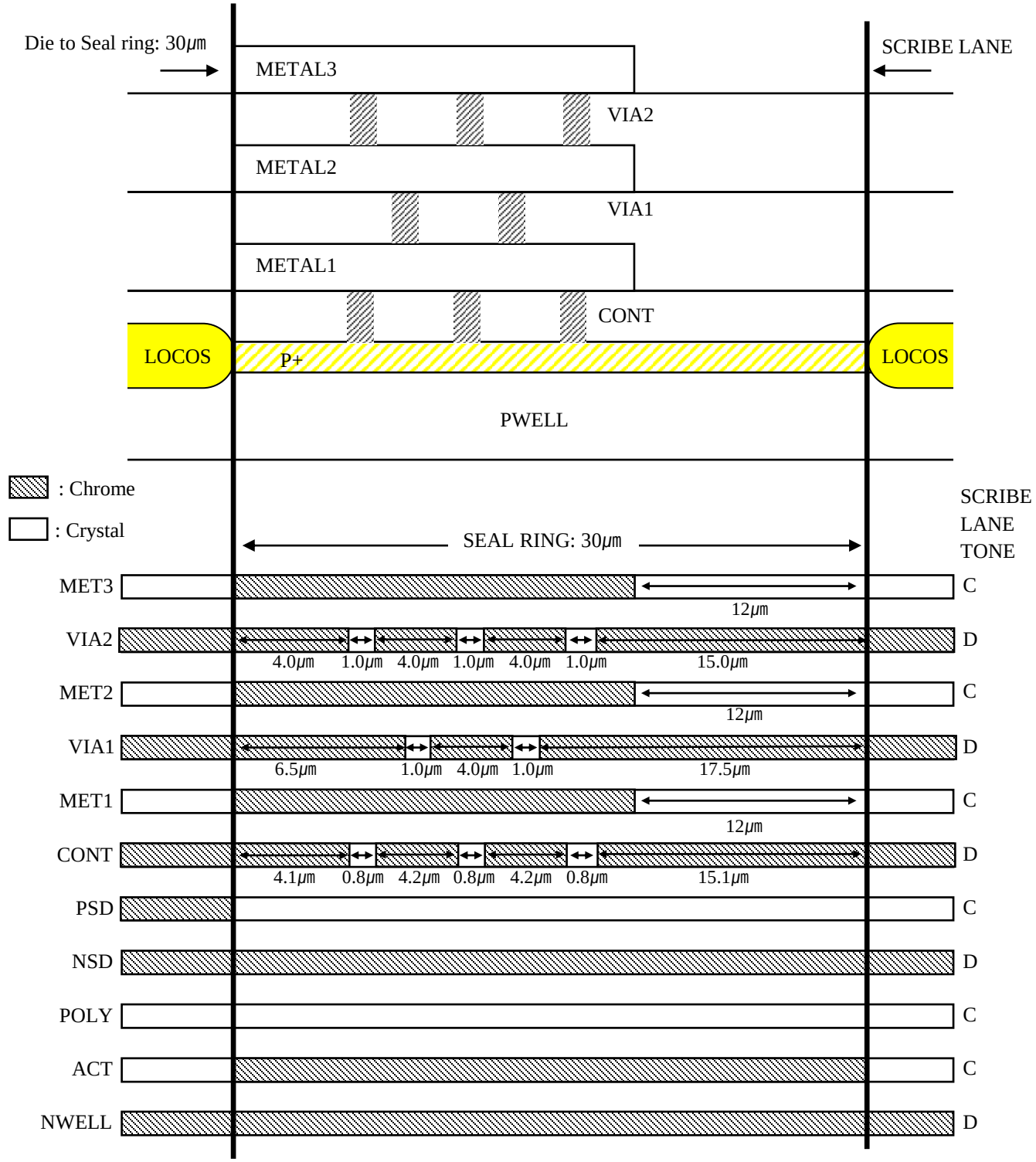


4.19 ESD Latch-up Design Guideline

Rule No.	Description	Label		Value (㎛)
20.LU.W1	Width of NWELL	a1	≥	12.0
20.LU.W2	Width of dummy collector (N/P-type)	a2	≥	10.0
20.LU.S1	Space of guard ring to dummy collector	b1	≥	5.0
20.LU.S2	Space of dummy collector to NWELL	b2	≥	5.0
20.LU.S3	Space of P+ to N+ guard ring	b3	≥	1.0
20.LU.S4	Space of N+ to P+ guard ring	b4	≥	1.0
20.LU.E1	Extension of dummy collector to NWELL	c1	≥	2.0
20.LU.E2	Extension of N+ guard ring to NWELL	c2	≥	2.0



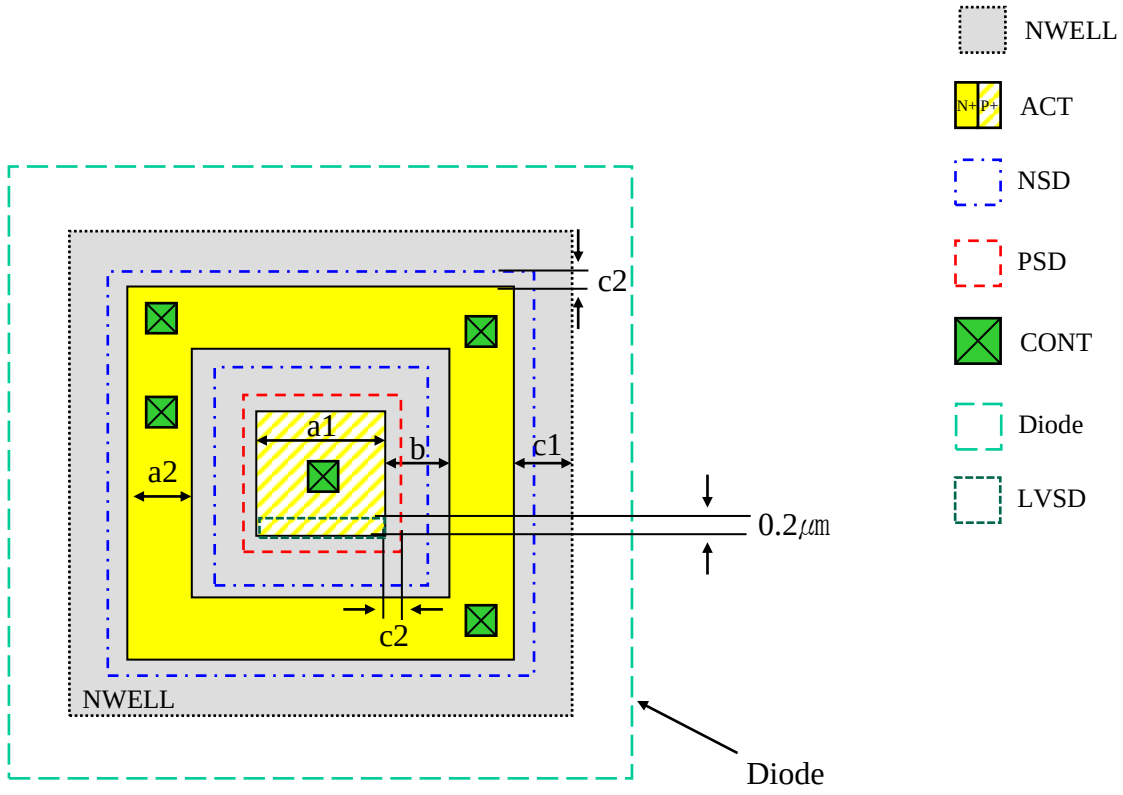
4.20 Seal-Ring Rules



4.21 P+/NW Diode Rules

Rule No.	Description	Label		Value (㎛)
22.PNW.W1	ACT (P-type) width/length In case of anode size (W/L): 2/5/10	a1		2 x 2 5 x 5 10 x 10 X x Y (X, Y ≤ 20)
22.PNW.W2	ACT (N-type) width	a2	=	2.0
22.PNW.S	Space of two ACT	b	=	4.5
22.PNW.E1	Extension of ACT (N-type) to NWELL	c1	=	2.0
22.PNW.E2	Extension of ACT to NSD/PSD	c2	=	1.0

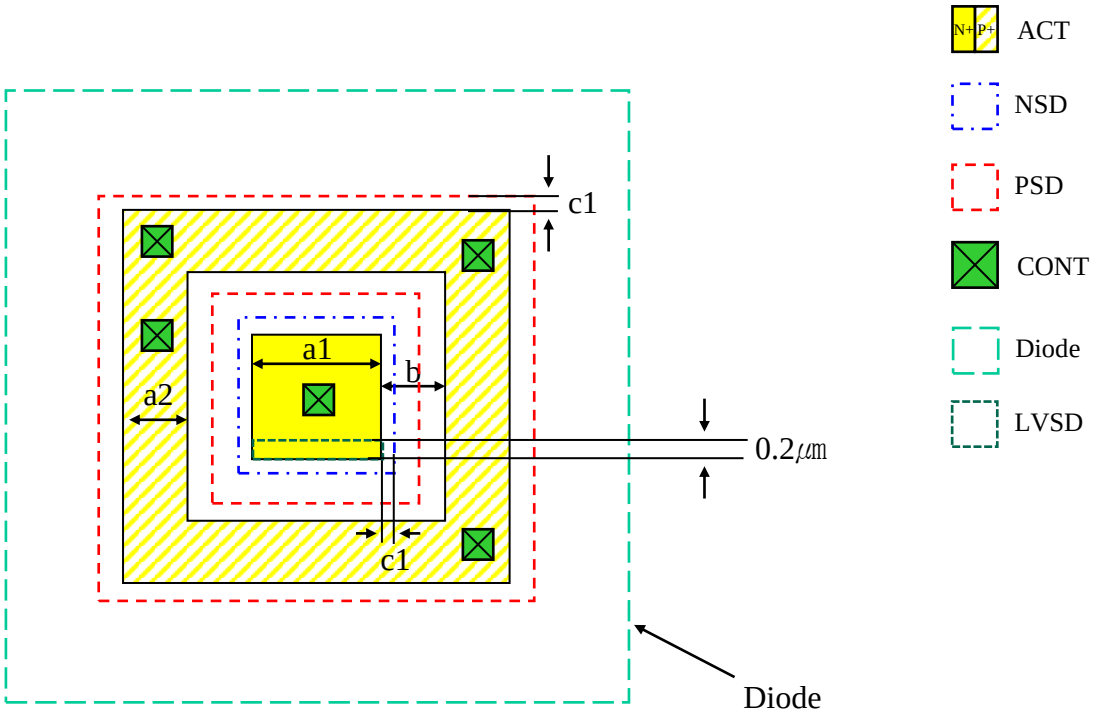
*** LVSD length is must 0.2㎛ (for LVS check)**



4.22 N+/PW Diode Rules

Rule No.	Description	Label		Value (㎛)
23.NPW.W1	ACT (N-type) width/length In case of cathode size (W/L): 2/5/10	a1		2 x 2 5 x 5 10 x 10 X x Y (X, Y ≤ 20)
23.NPW.W2	ACT (P-type) width	a2	=	2.0
23.NPW.S	Space of two ACT	b	=	4.5
23.NPW.E	Extension of ACT to NSD/PSD	c1	=	1.0

*** LVSD length is must 0.2㎛ (for LVS check)**



5. Electrical Targets

5.1 Transistor Key Parameter

Parameter		0.5㎛ Technology
NMOS	2ΔL [㎛]	0.10 ± 0.05
	2ΔW [㎛]	0.35 ± 0.10
	Vt [V]	0.75 ± 0.1 (@W/L=20/20㎛)
		0.75 ± 0.1 (@W/L= 20/0.5㎛)
	Idsat [㎂/㎛]	550 ± 50 (@W/L= 20/0.5㎛)
	BVDSS [V]	≥ 8
PMOS	2ΔL [㎛]	0.10 ± 0.05
	2ΔW [㎛]	0.40 ± 0.10
	Vt [V]	-0.85 ± 0.1 (@W/L=20/20㎛)
		-0.80 ± 0.1 (@W/L= 20/0.5㎛)
	Idsat [㎂/㎛]	-240 ± 30 (@W/L= 20/0.5㎛)
	BVDSS [V]	≤ -8
Field TR	Vtn [V]	≥ 10
	BVdss [V]	≥ 8
	Vtp [V]	≤ -10
	BVdss [V]	≤ -8

5.2 Sheet Resistance (Ω/sq.)

Parameter	Min.	Typ.	Max..
NWL	850	1000	1120
N+ S/D	50	65	80
P+ S/D	150	180	210
Poly	30	50	70
Poly 2 (npres)	110	125	140
Metal 1	0.06	0.08	0.10
Metal 2	0.06	0.08	0.10
Metal 3	0.03	0.05	0.06

5.3 Contact Resistance (Ω/ea.), Kelvin Pattern

Parameter	Min.	Typ.	Max..
N+ S/D Contact	20	30	50
P+ S/D Contact	70	90	110
POLY1 Contact	30	50	70
POLY2 Contact	60	130	200
VIA1	1.0	2.0	3.0
VIA2	0.5	1.5	2.5

5.4 Poly Capacitance (fF/μm^2) : pipcap

Parameter	Min.	Typ.	Max..
POLY 2 to POLY1	0.45	0.50	0.55

5.5 Parasitic Interconnect Capacitance (fF/μm^2)

Layer	Area Capacitance	Fringe Capacitance
N+ Diffusion to P-Well	0.6882	0.3212
P+ Diffusion to N-Well	0.7933	0.2277
Poly Gate (N-Channel)	2.9739	0.3134
Poly Gate (P-Channel)	2.9624	0.2138
Poly to Field	0.0902	0.0519
Metal 1 to Field	0.0435	0.0551
Metal 1 to Poly or Active	0.0703	0.0657
Metal 2 to Field	0.0241	0.0406
Metal 2 to Poly or Active	0.0299	0.0437
Metal 2 to Metal 1	0.0446	0.0487
Metal 3 to Field	0.0165	0.0332
Metal 3 to Poly or Active	0.0188	0.0353
Metal 3 to Metal 1	0.0222	0.0361
Metal 3 to Metal 2	0.0422	0.0479