ETRI 0.5㎛ Analog CMOS 2P3M 5V Design Guide Calibre

Version 1.0

National Semiconductor Public Laboratory (NSPL)

- Electronics and Telecommunications Research Institute (ETRI)
- Seoul National University (SNU)
- Daegu Gyeongbuk Institute of Science & Technology (DGIST)

Contents

Contents

1. Overview

1.1 Overview

The purpose of this guide is 0.5um Analog CMOS 2P3M 5V NSPL Design guide.

1.2 Software Version and Tools

- Virtuoso 6.1.8 version
- Calibre 2019.3_15.11

1.3 File Configuration

File : ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_V1.0.tar.gz

- ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL
  - ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL.tf : tech file
  - ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL.layermap : map file
  - display.drf : display file
  - ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_pcell : pcell library
  - ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_sch : sch library
  - ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_std_sch : sandard sch library
  - ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_std_lay : sandard lay library
  - Calibre/DRC
    - ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_DRC.cal : drc rule file
    - drc_header.cal : with header file
    - rundrc.com : run command
  - -Calibre/ LVS
    - ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_LVS.cal : lvs rule file
    - lvs_header.cal : with header file
    - runlvs.com : run command
  - Calibre/LVL
    - ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_LVL.cal : lvl rule file
    - lvl_header.cal : with header file
    - runlvl.com : run command
  - Calibre/PEX
    - ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_V1.0_PEX.cal : pex rule file
    - pex_header.cal : with header file

1.4 Documents

- ETRI 0.5um Analog CMOS 2P3M 5V Design Rule NSPL : Design rule
- ETRI 0.5um Analog CMOS 2P3M 5V Design Guide Calibre NSPL : Design Guide

1.5 Document history

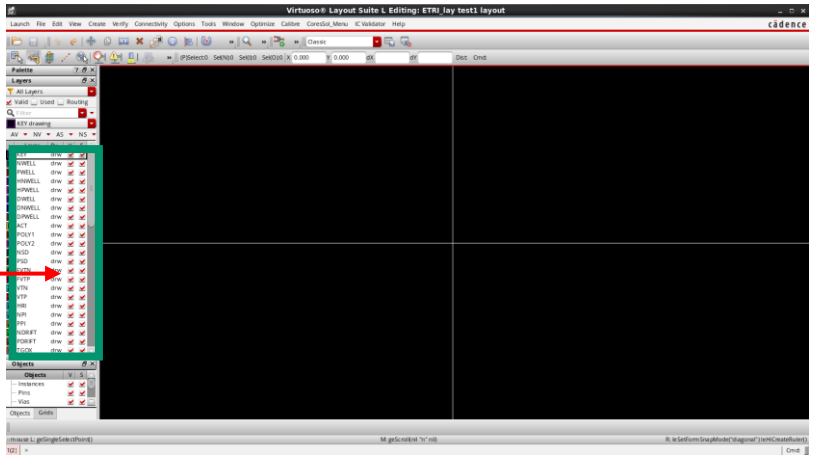
Rev	Date	From	Description
1.0	2023.08.21	Coressol	**Added Items** 1. Overview(version, file configuration, Documents) 2. Environment Files and About Use 3. Schematic Library 4. Parameter Cell Library 5. Standard Schematic Library 6. Standard Layout Library 7. Sealring 8. Calibre DRC 9. Calibre LVS 10. Calibre LVL
	2023.09.06	Coressol	**Added Items** 8. LVS Guide **Modify Items** 8.Calibre DRC → 9.Calibre DRC 9. Calibre LVS → 10.Calibre LVS 10. Calibre LVL → 11.Calibre LVL
			Title **ETRI 0.5㎛ Analog CMOS 2P3M 5V NSPL Design Guide**
			Division **Coressol**

2. Environment Files and About Use

2.1 Display.drf File

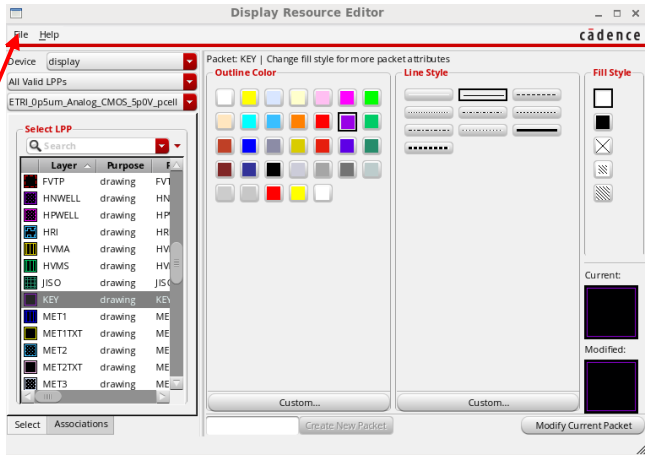
- This file should exist in the location where virtuoso is run.
- This file the color of the layer is specified.
- If you want to change the color, you can do so in the following ways

Shift +
left mouse
click.

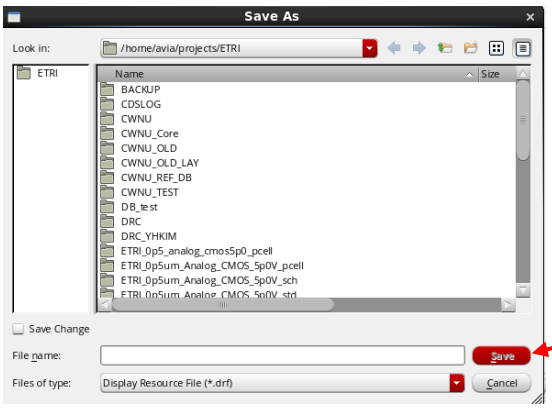


Layer Edit

Save at file



Select file or
New file name



Save

2.2 Technology File

Layer Name	Layer No.	Function	Digitized Area
KEY	1	Define Align key	C
NWELL	2	Define N-well for PMOS body	C
PWELL	3	Define P-well for NMOS body	C
ACT	11	Define Active area	D
POLY1	12	Define Poly-Si 1 for gate of transistor	D
POLY2	13	Define Poly-Si 2 for resistor and capacitor	D
NSD	14	Define N-type implant region for N-LDD and N+	C
PSD	15	Define N-type implant region for P-LDD and P+	C
NHRI	20	Define implant for N-type high resistance poly-Si resistor (poly)	C
PHRI	21	Define implant for P-type high resistance poly-Si resistor (poly)	C
ESD	26	Define ESD device region for DRC	
CONT	31	Define contact from MET1 to ACT, POLY1 and POLY2	C
MET1	32	Define Metal-1 for interconnection	D
VIA1	33	Define Via1 connecting MET1 and MET2	C
MET2	34	Define Metal-2 for interconnection	D
VIA2	35	Define Via2 connecting MET2 and MET3	C
MET3	36	Define Metal-3 for interconnection	D
PAD	37	Define open region of passivation for bonding pad	C
POLY1TXT	41	Poly1 Text	
MET1TXT	42	MET1 Text	
MET2TXT	44	MET2 Text	
MET3TXT	46	MET3 Text	
PADTXT	47	PAD Text	
TEXT	48	Text	
RES	51	Poly-Si Resistor for DRC & LVS	
CAP	53	Poly-Si Capacitor for DRC & LVS	
BJT	56	BJT for DRC & LVS	
DIODE	57	Diode for DRC & LVS	
NODRC	58	DRC check blocking layer	
ESDD	59	Define ESD device drain electrode	
LVSD	60	Extract Poly-Si Resistor/PIP CAP Area	
ESDI	109	Define ESD Implnat	C

2.3 Map File

Layer Name	Layer Purpose	Layer No.	Layer Data Type
KEY	drawing	1	0
NWELL	drawing	2	0
PWELL	drawing	3	0
ACT	drawing	11	0
POLY1	drawing	12	0
POLY2	drawing	13	0
NSD	drawing	14	0
PSD	drawing	15	0
NHRI	drawing	20	0
PHRI	drawing	21	0
ESD	drawing	26	0
CONT	drawing	31	0
MET1	drawing	32	0
VIA1	drawing	33	0
MET2	drawing	34	0
VIA2	drawing	35	0
MET3	drawing	36	0
PAD	drawing	37	0
POLY1TXT	drawing	41	0
MET1TXT	drawing	42	0
MET2TXT	drawing	44	0
MET3TXT	drawing	46	0
PADTXT	drawing	47	0
TEXT	drawing	48	0
RES	drawing	51	0
CAP	drawing	53	0
BJT	drawing	56	0
DIODE	drawing	57	0
NODRC	drawing	58	0
ESDD	drawing	59	0
LVSD	drawing	60	0
ESDI	drawing	109	0

2.4 How to Setup Library

- Bring the ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL.tar.gz file to the location where you want to run virtuoso and release the component with a command like the following:
  tar -zxvf ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL.tar.gz

```
30 09:44 Calibre/
30 09:44 ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL.layermap*
30 09:44 ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL.tf*
30 09:50 ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_pcell/
30 09:50 ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_sch/
30 09:50 ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_std_lay/
30 09:50 ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_std_sch/
30 09:44 display.drf*
```

- Define Library in cds.lib

ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_pcell
ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_sch
ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_std_lay
ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_std_sch

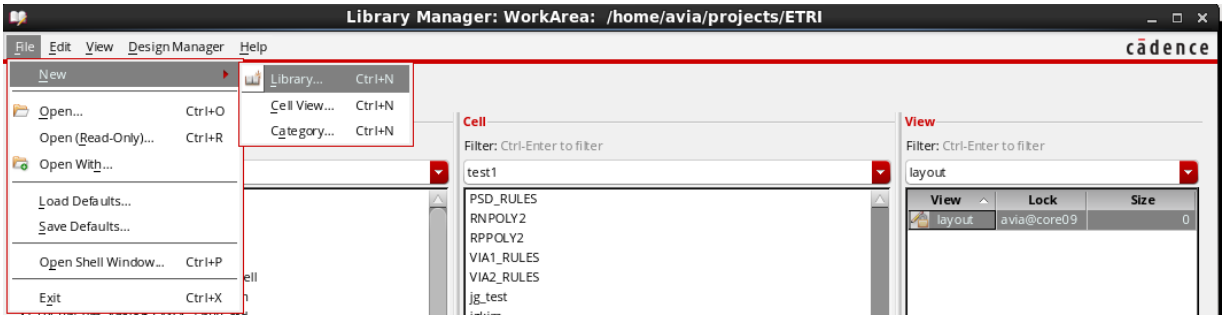
- DEFINE library_name library_path (following example – cds.lib)

```
DEFINE ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_pcell   /home/avia/projects/ETRI_0p5um/ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_pcell
DEFINE ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_sch     /home/avia/projects/ETRI_0p5um/ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_sch
DEFINE ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_std_lay /home/avia/projects/ETRI_0p5um/ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_std_lay
DEFINE ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_std_sch /home/avia/projects/ETRI_0p5um/ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_std_sch
```

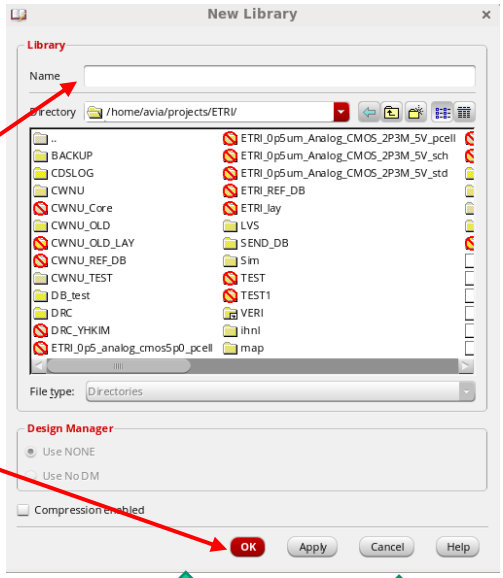
- Copy the files in the DRC Directory to the location where you want to run the DRC.
- Copy the files in the LVS Directory to the location where you want to run the LVS.
- Copy the files in the LVL Directory to the location where you want to run the LVL.

- display.drf file copy at virtuoso running.

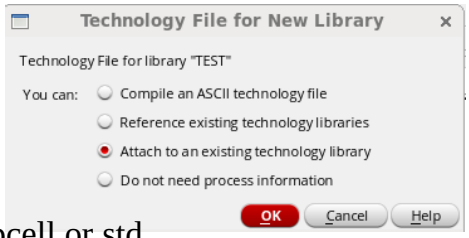
2.5 How to Create a Library



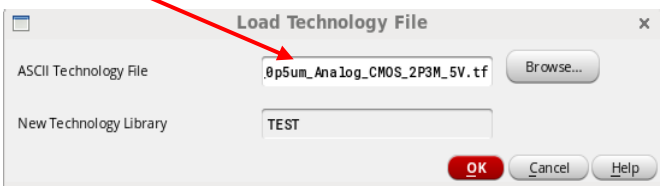
Library name



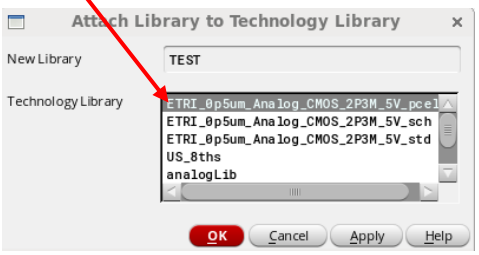
After write
Library name



Write Tech file with
location

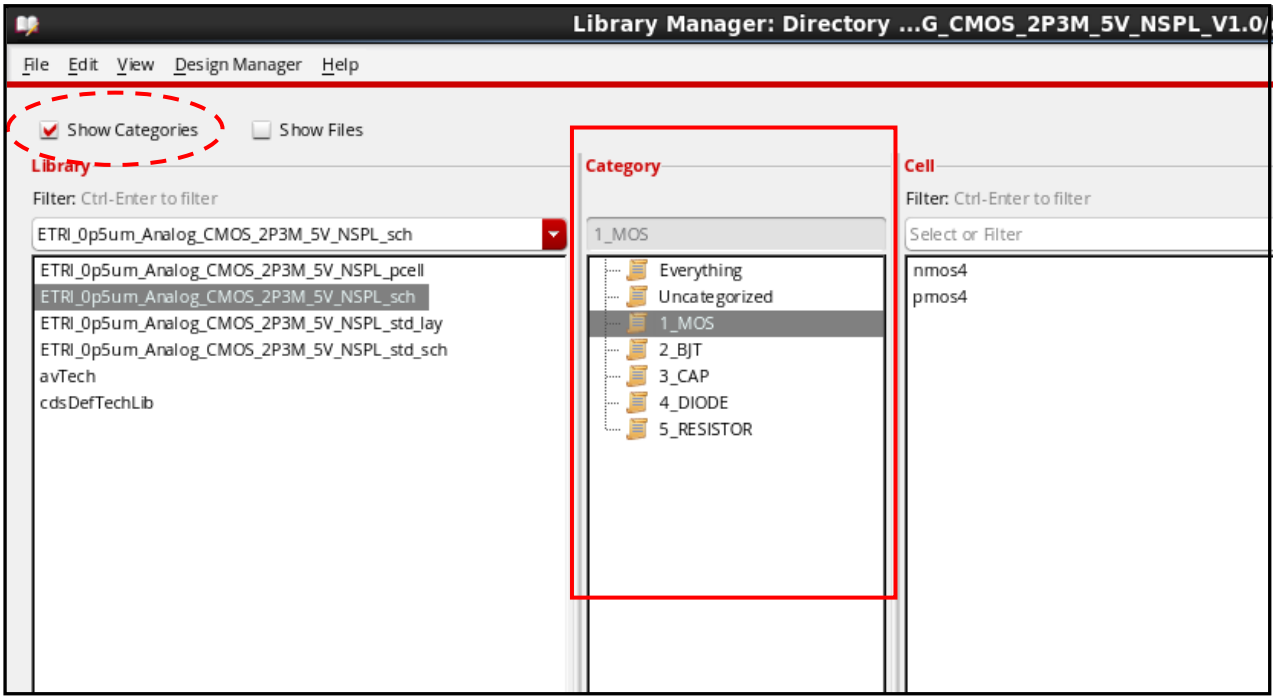


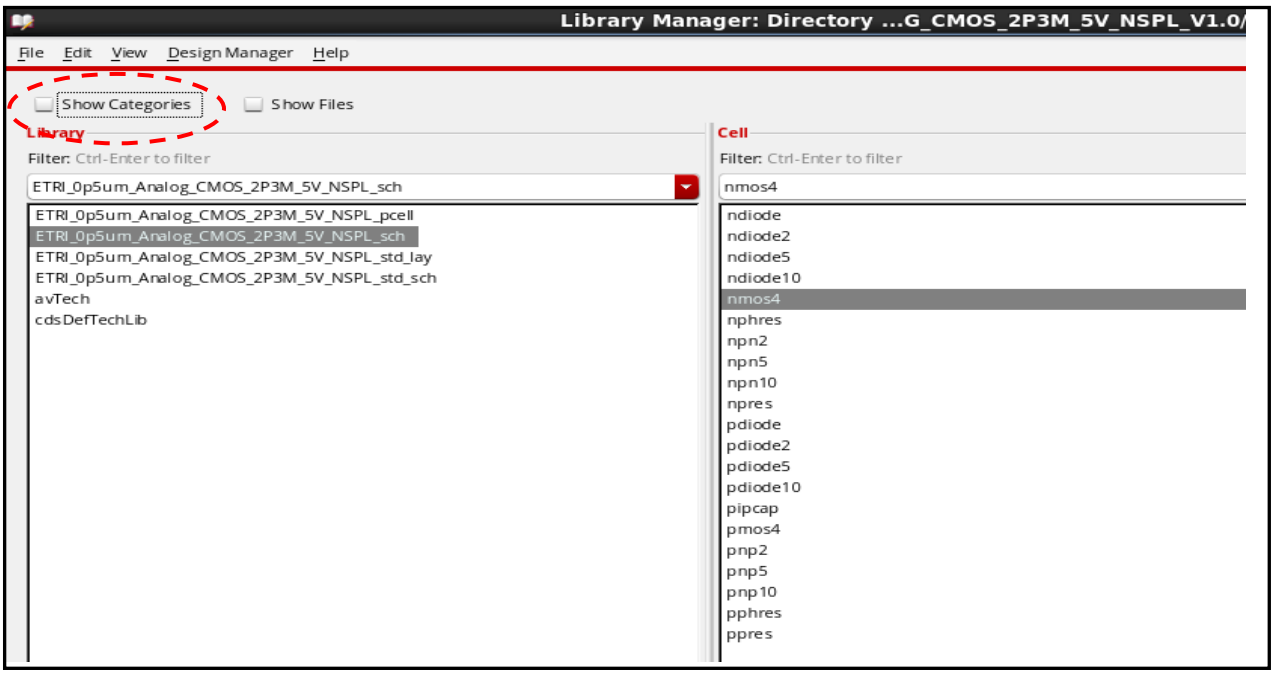
Select pcell or std
or sch library



3. Schematic Library

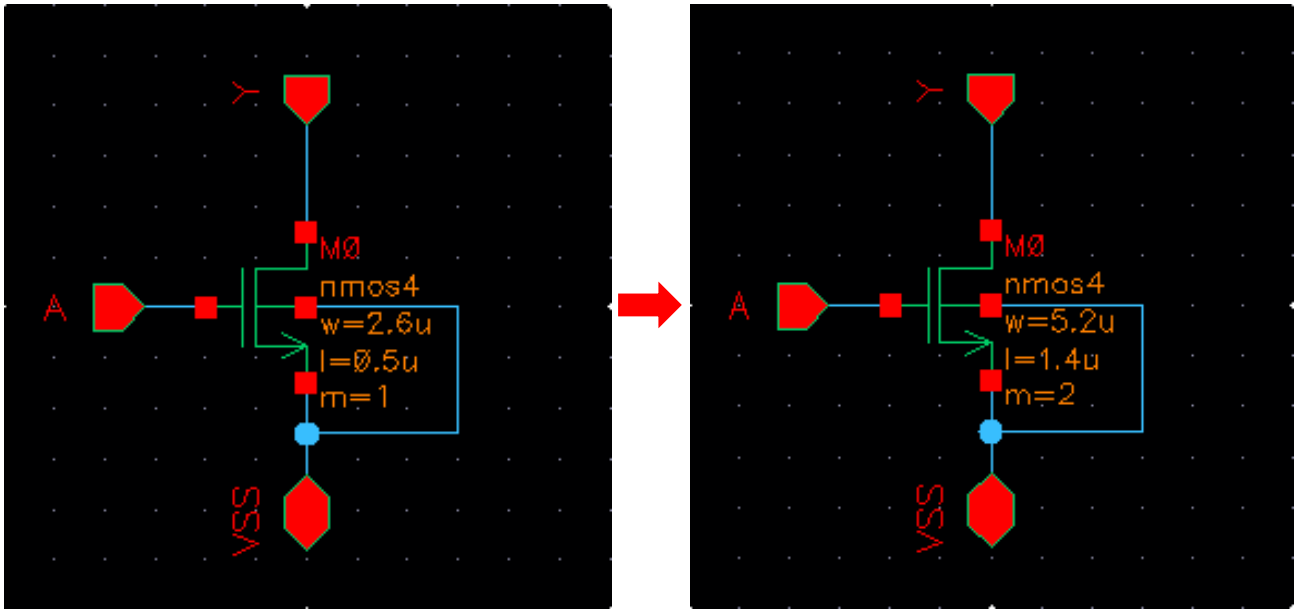
3.1 Library Category





3.2 nmos4

Parameter					
Width	2.6u → 5.2u	Length	0.5u → 1.4u	multiplier	1 → 2



<Schematic parameter>

```
********************************************
* Library Name: ETRI_lay
* Cell Name:    nmos4
* View Name:    schematic
********************************************

.SUBCKT nmos4 A VSS Y
*.PININFO A:I Y:O VSS:B
MM0 Y A VSS VSS nmos4 W=2.6u L=0.5u m=1
.ENDS
```

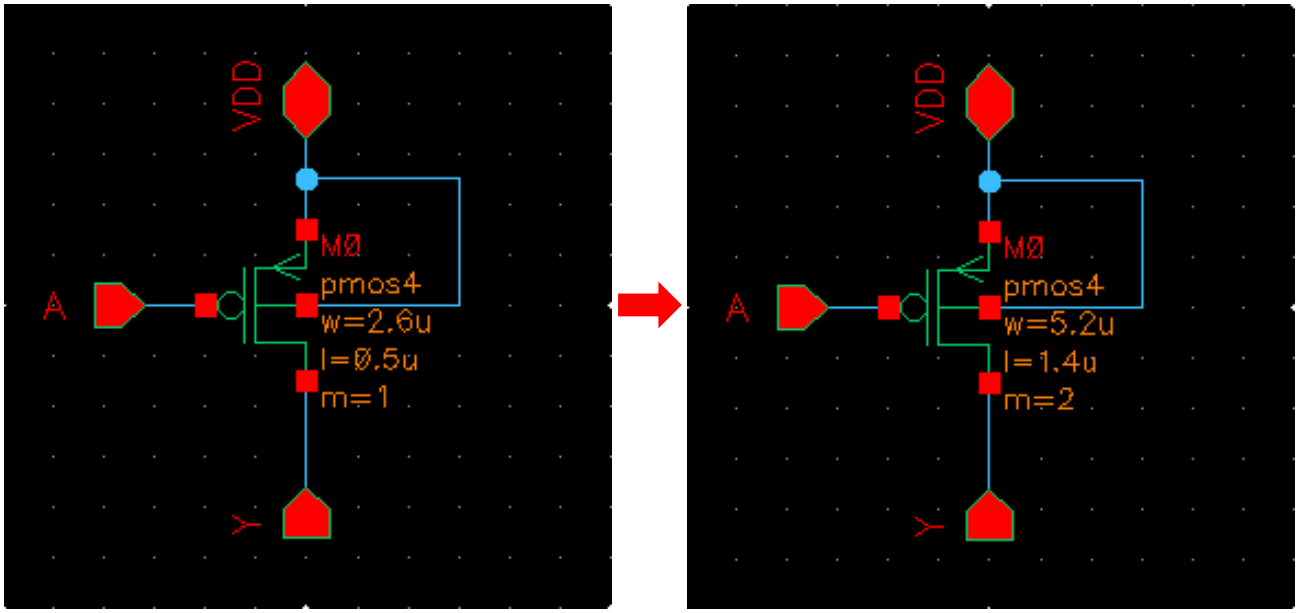
```
********************************************
* Library Name: ETRI_lay
* Cell Name:    nmos4
* View Name:    schematic
********************************************

.SUBCKT nmos4 A VSS Y
*.PININFO A:I Y:O VSS:B
MM0 Y A VSS VSS nmos4 W=5.2u L=1.4u m=2
.ENDS
```

<cdl output>

3.3 pmos4

Parameter					
Width	2.6u → 5.2u	Length	0.5u → 1.4u	multiplier	1 → 2



<Schematic parameter>

```
********************************************
* Library Name: ETRI_lay
* Cell Name:    pmos4
* View Name:    schematic
********************************************

.SUBCKT pmos4 A VDD Y
*.PININFO A:I Y:O VDD:B
MM0 Y A VDD VDD pmos4 W=2.6u L=0.5u m=1
.ENDS
```

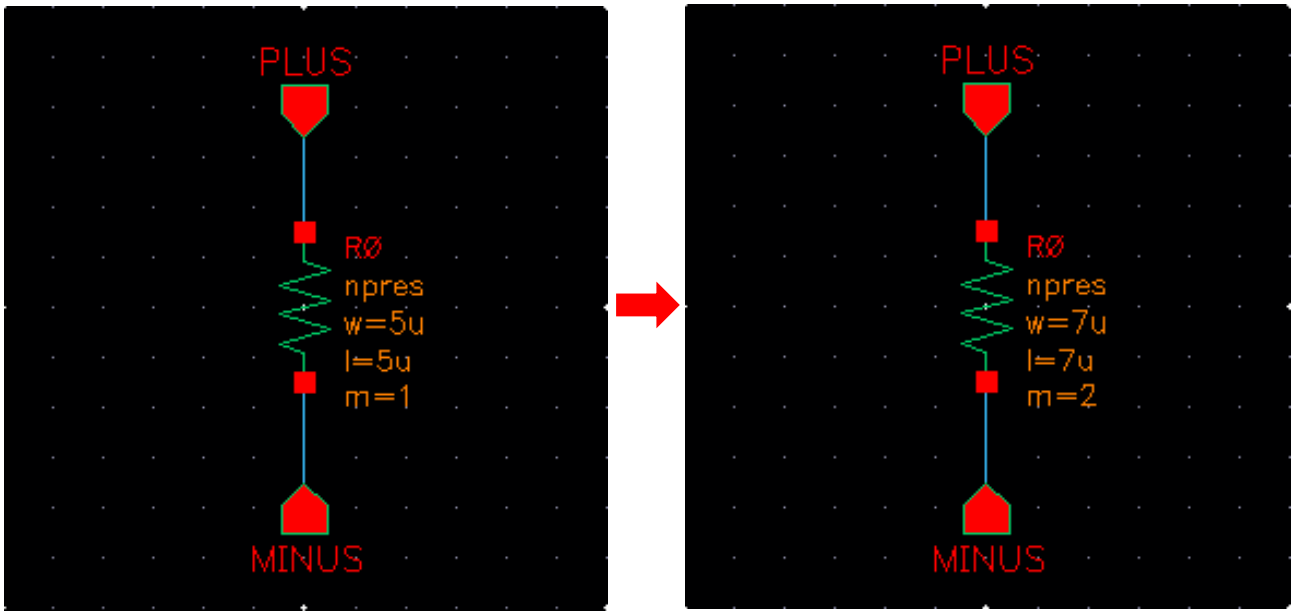
```
********************************************
* Library Name: ETRI_lay
* Cell Name:    pmos4
* View Name:    schematic
********************************************

.SUBCKT pmos4 A VDD Y
*.PININFO A:I Y:O VDD:B
MM0 Y A VDD VDD pmos4 W=5.2u L=1.4u m=2
.ENDS
```

<cdl output>

3.4 npres

Parameter					
Width	5u → 7u	Length	5u → 7u	multiplier	1 → 2



<Schematic parameter>

```
********************************************
* Library Name: ETRI_lay
* Cell Name:    npres
* View Name:    schematic
********************************************

.SUBCKT npres MINUS PLUS
*.PININFO PLUS:I MINUS:O
RR0 PLUS MINUS $[npres] m=1 w=5u l=5u
.ENDS
```

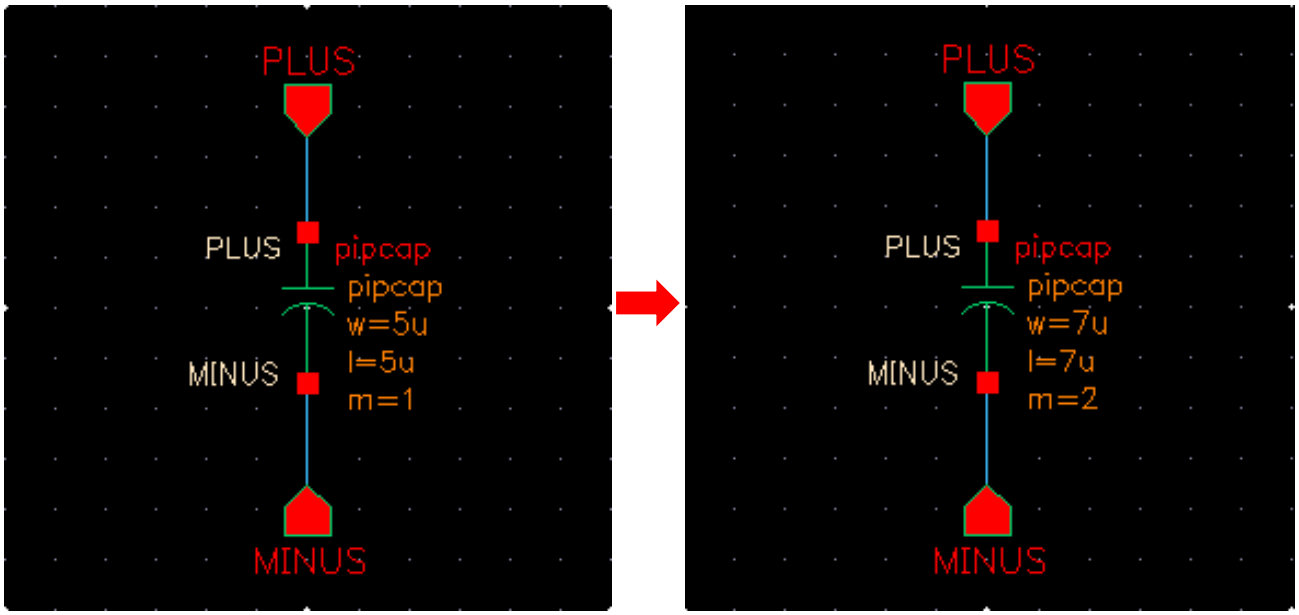
```
********************************************
* Library Name: ETRI_lay
* Cell Name:    npres
* View Name:    schematic
********************************************

.SUBCKT npres MINUS PLUS
*.PININFO PLUS:I MINUS:O
RR0 PLUS MINUS $[npres] m=2 w=7u l=7u
.ENDS
```

<cdl output>

3.5 pipcap

Parameter					
Width	5u → 7u	Length	5u → 7u	multiplier	1 → 2



<Schematic parameter>

```
********************************************
* Library Name: ETRI_lay
* Cell Name:    pipcap
* View Name:    schematic
********************************************

.SUBCKT pipcap MINUS PLUS
*.PININFO PLUS:I MINUS:O
CR0 PLUS MINUS $[pipcap] m=1 w=5u l=5u
.ENDS
```

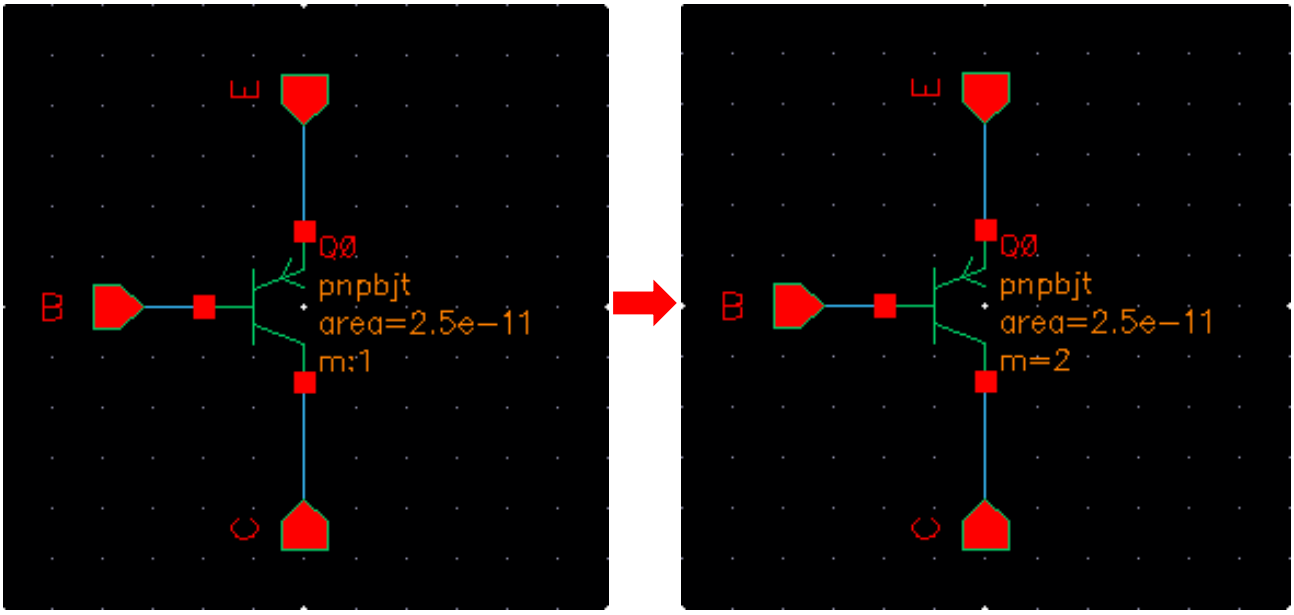
```
********************************************
* Library Name: ETRI_lay
* Cell Name:    pipcap
* View Name:    schematic
********************************************

.SUBCKT pipcap MINUS PLUS
*.PININFO PLUS:I MINUS:O
CR0 PLUS MINUS $[pipcap] m=2 w=7u l=7u
.ENDS
```

<cdl output>

3.6 pnp5

Parameter			
Area	2.5e-11	multiplier	1 → 2



<Schematic parameter>

```
*****************************************
* Library Name: ETRI_lay
* Cell Name:    pnp5
* View Name:    schematic
*****************************************

.SUBCKT pnp5 B C E
*.PININFO B:I C:I E:O
QQ0 C B E pnpbjt m=1 area=2.5e-11
.ENDS
```

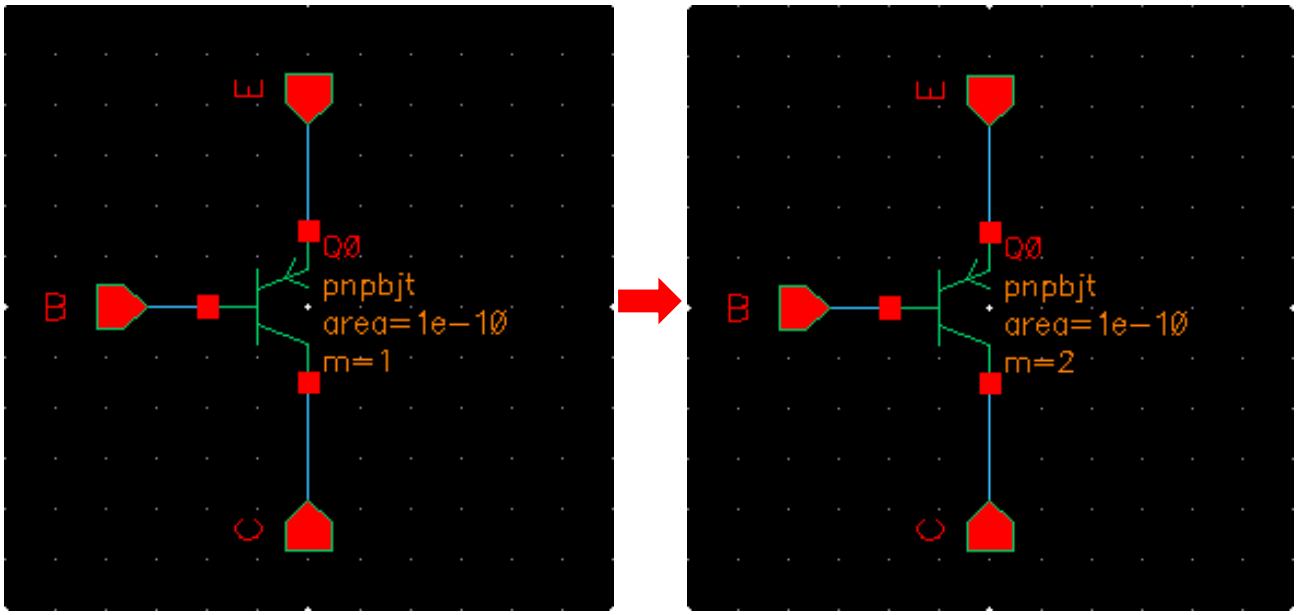
```
*****************************************
* Library Name: ETRI_lay
* Cell Name:    pnp5
* View Name:    schematic
*****************************************

.SUBCKT pnp5 B C E
*.PININFO B:I C:I E:O
QQ0 C B E pnpbjt m=2 area=2.5e-11
.ENDS
```

<cdl output>

3.7 pnp10

Parameter			
Area	1e-10	multiplier	1 → 2



<Schematic parameter>

```
********************************************
* Library Name: ETRI_lay
* Cell Name:    pnp10
* View Name:    schematic
********************************************

.SUBCKT pnp10 B C E
*.PININFO B:I C:I E:O
QQ0 C B E pnpbjt m=1 area=1e-10
.ENDS
```

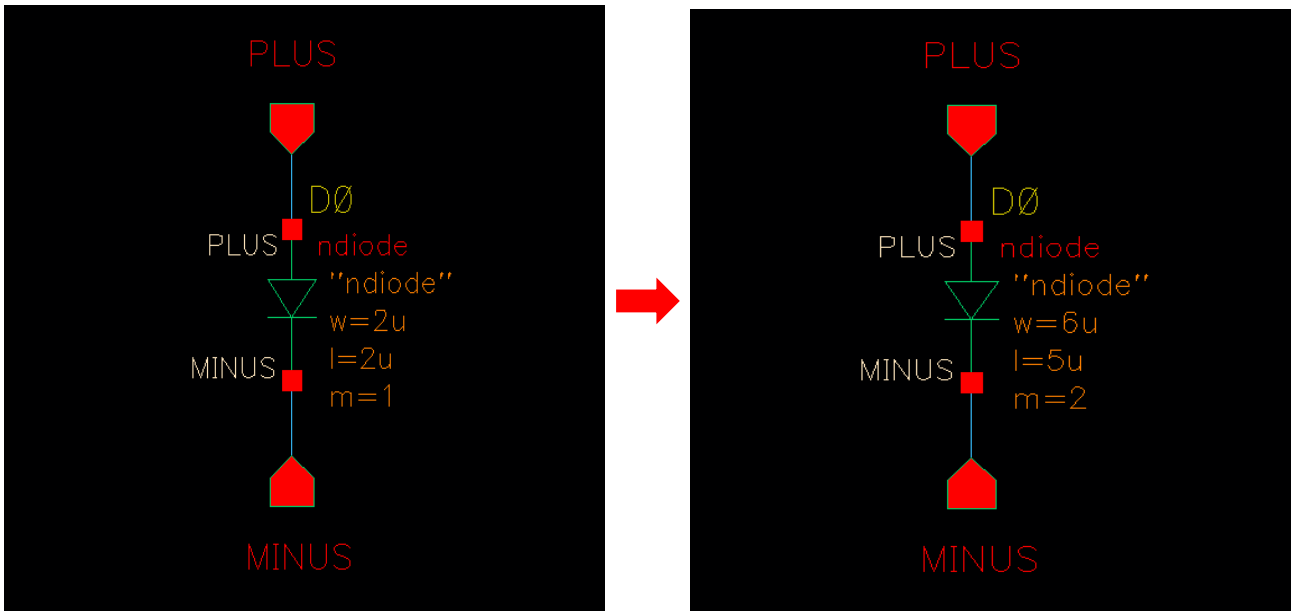
```
********************************************
* Library Name: ETRI_lay
* Cell Name:    pnp10
* View Name:    schematic
********************************************

.SUBCKT pnp10 B C E
*.PININFO B:I C:I E:O
QQ0 C B E pnpbjt m=2 area=1e-10
.ENDS
```

<cdl output>

3.8 ndiode

Parameter					
Width	2.0u → 6u	Length	2.0u → 5u	multiplier	1 → 2



<Schematic parameter>

```
**************************************************
* Library Name: ETRI_lay
* Cell Name:    ndiode
* View Name:    schematic
**************************************************

.SUBCKT ndiode MINUS PLUS
*.PININFO MINUS:I PLUS:I
DD0 PLUS MINUS ndiode m=1 w=2u l=2u
.ENDS
```

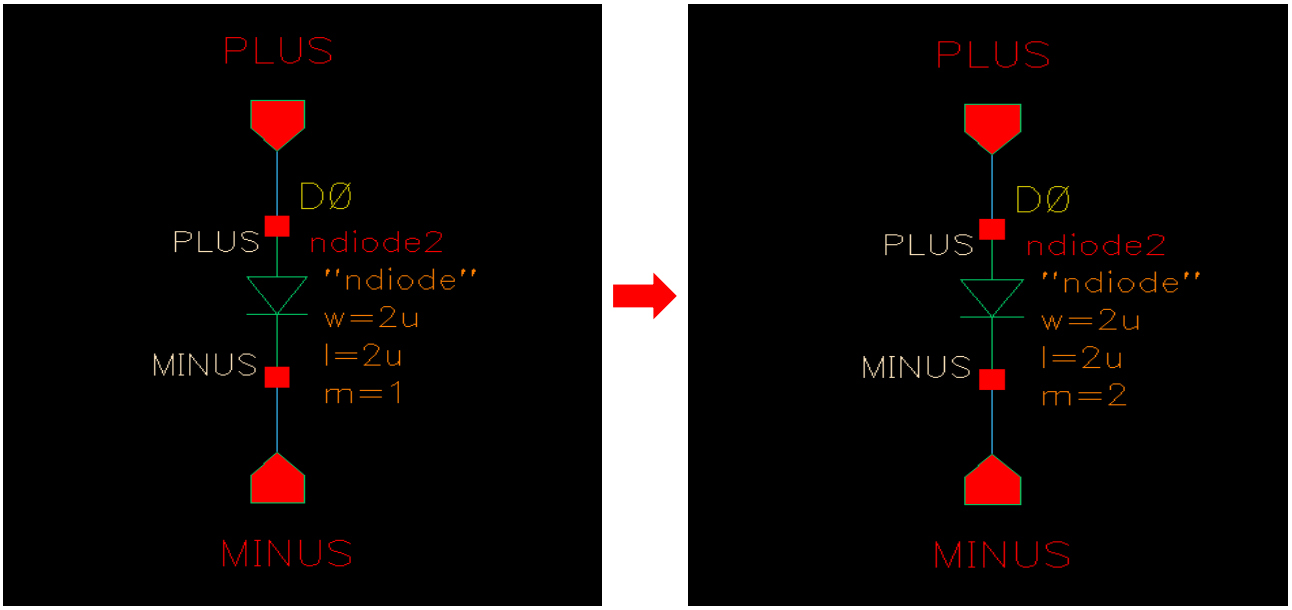
```
**************************************************
* Library Name: ETRI_lay
* Cell Name:    ndiode
* View Name:    schematic
**************************************************

.SUBCKT ndiode MINUS PLUS
*.PININFO MINUS:I PLUS:I
DD0 PLUS MINUS ndiode m=2 w=6u l=5u
.ENDS
```

<cdl output>

3.9 ndiode2

Parameter					
Width	2.0u	Length	2.0u	multiplier	1 → 2



<Schematic parameter>

```
**************************************************
* Library Name: ETRI_lay
* Cell Name:    ndiode2
* View Name:    schematic
**************************************************

.SUBCKT ndiode2 MINUS PLUS
*.PININFO MINUS:I PLUS:I
DD0 PLUS MINUS ndiode m=1 w=2u l=2u
.ENDS
```

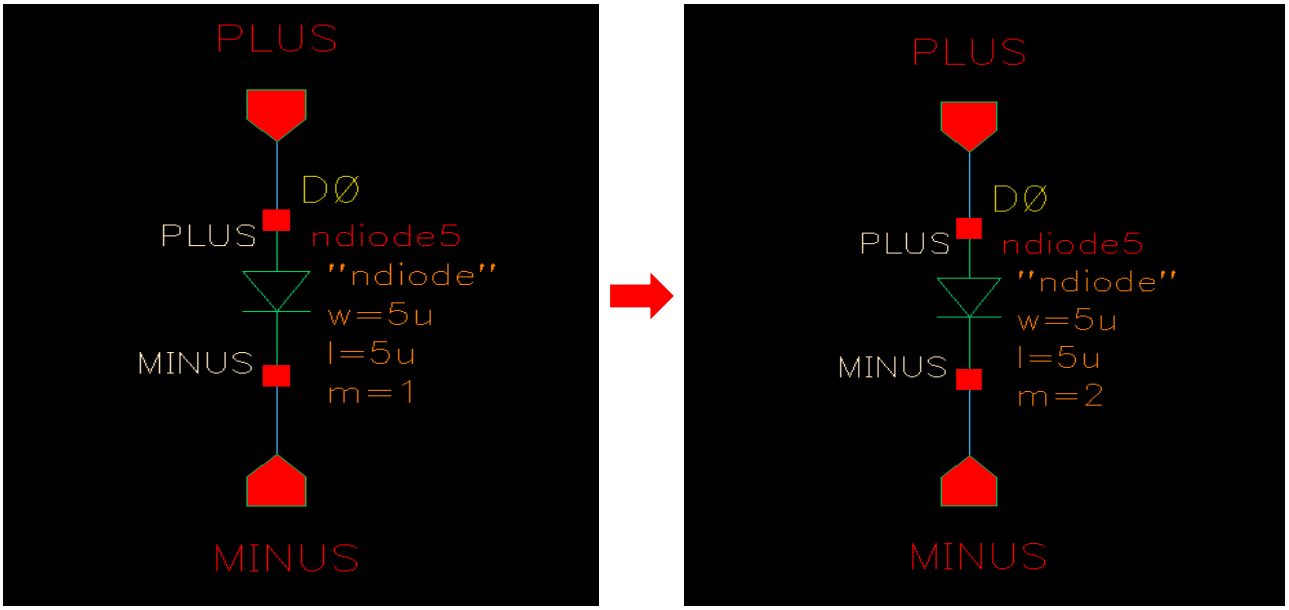
```
**************************************************
* Library Name: ETRI_lay
* Cell Name:    ndiode2
* View Name:    schematic
**************************************************

.SUBCKT ndiode2 MINUS PLUS
*.PININFO MINUS:I PLUS:I
DD0 PLUS MINUS ndiode m=2 w=2u l=2u
.ENDS
```

<cdl output>

3.10 ndiode5

Parameter					
Width	5.0u	Length	5.0u	multiplier	1 → 2



<Schematic parameter>

```
**********************************************
* Library Name: ETRI_lay
* Cell Name:    ndiode5
* View Name:    schematic
**********************************************

.SUBCKT ndiode5 MINUS PLUS
*.PININFO MINUS:I PLUS:I
DD0 PLUS MINUS ndiode m=1 w=5u l=5u
.ENDS
```

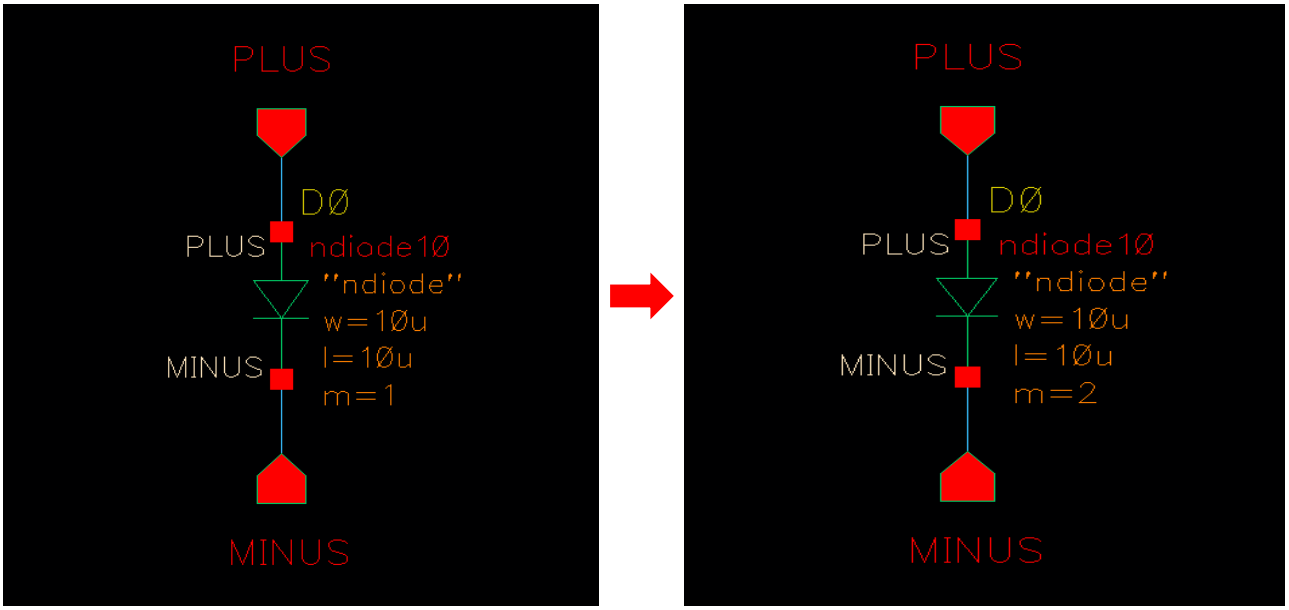
```
**********************************************
* Library Name: ETRI_lay
* Cell Name:    ndiode5
* View Name:    schematic
**********************************************

.SUBCKT ndiode5 MINUS PLUS
*.PININFO MINUS:I PLUS:I
DD0 PLUS MINUS ndiode m=2 w=5u l=5u
.ENDS
```

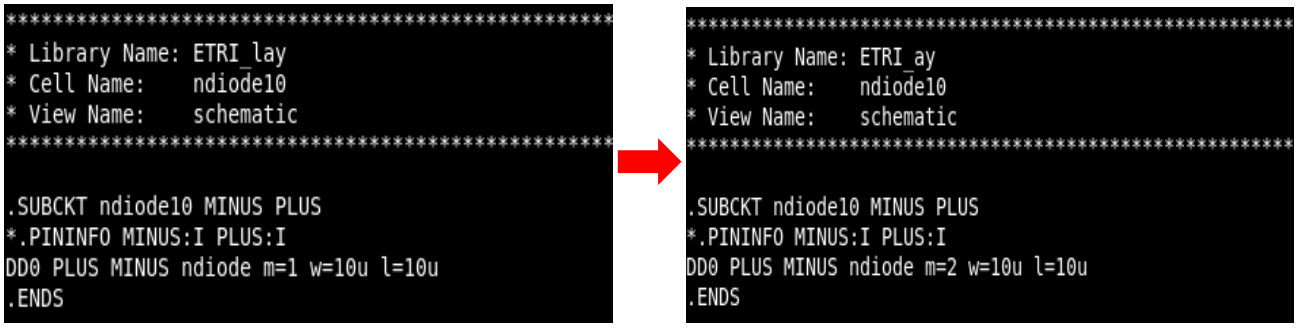
<cdl output>

3.11 ndiode10

Parameter					
Width	10.0u	Length	10.0u	multiplier	1 → 2



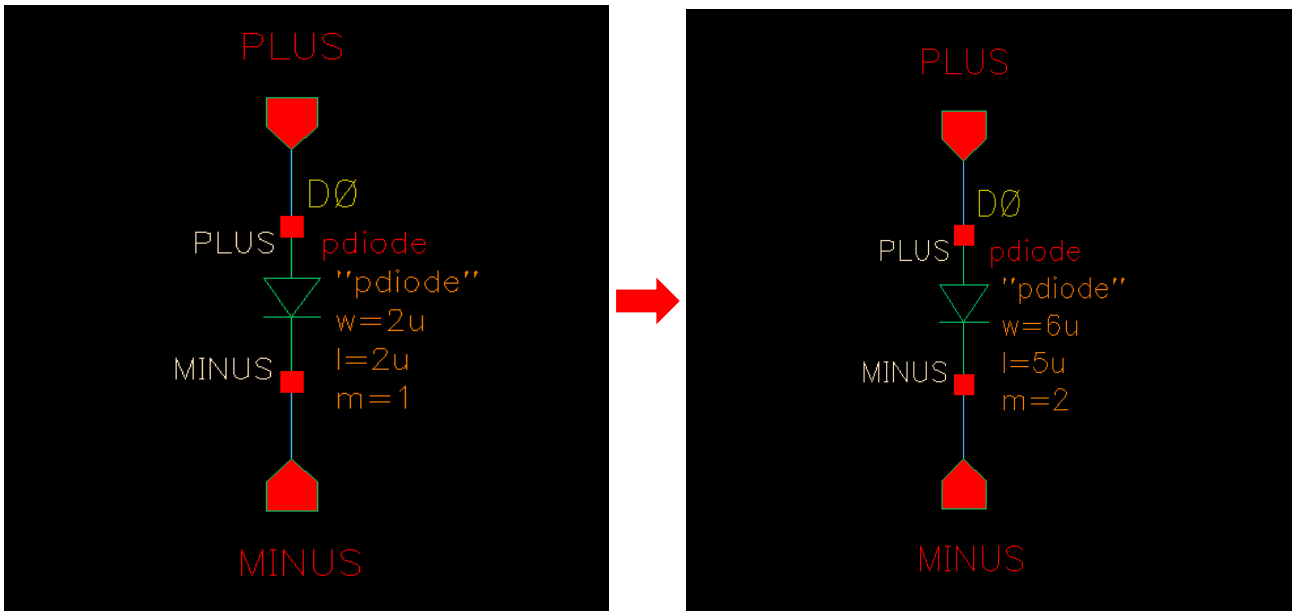
<Schematic parameter>



<cdl output>

3.12 pdiode

Parameter					
Width	2.0u → 6u	Length	2.0u → 5u	multiplier	1 → 2

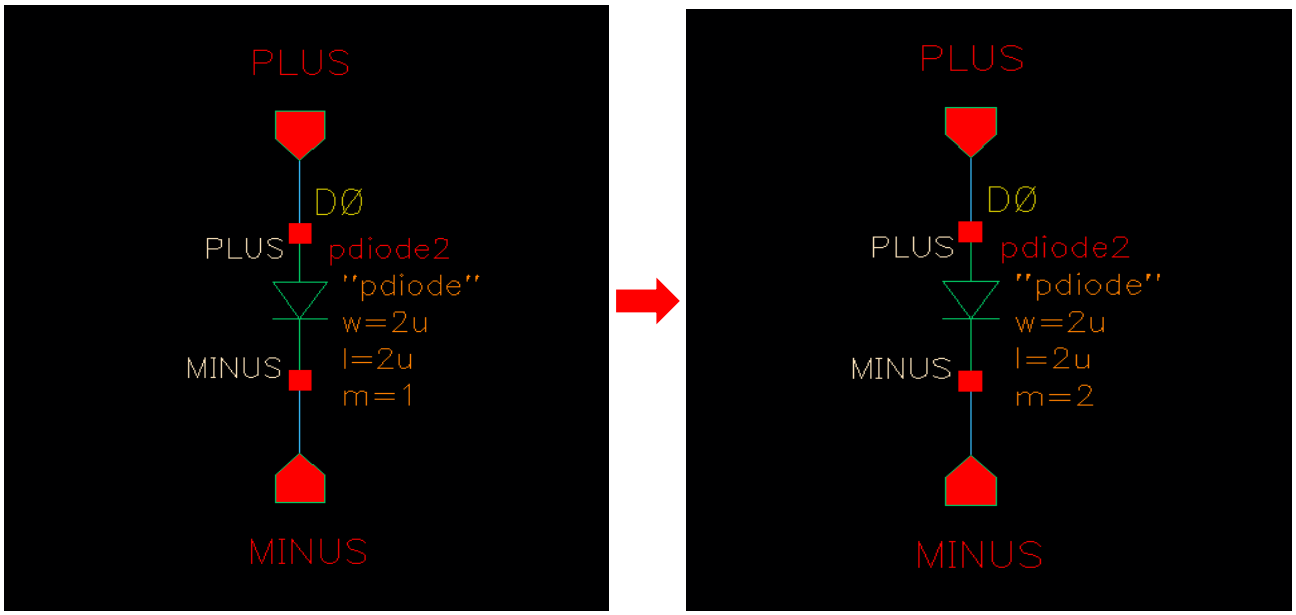


<Schematic parameter>

<cdl output>

3.13 pdiode2

Parameter					
Width	2.0u	Length	2.0u	multiplier	1 → 2

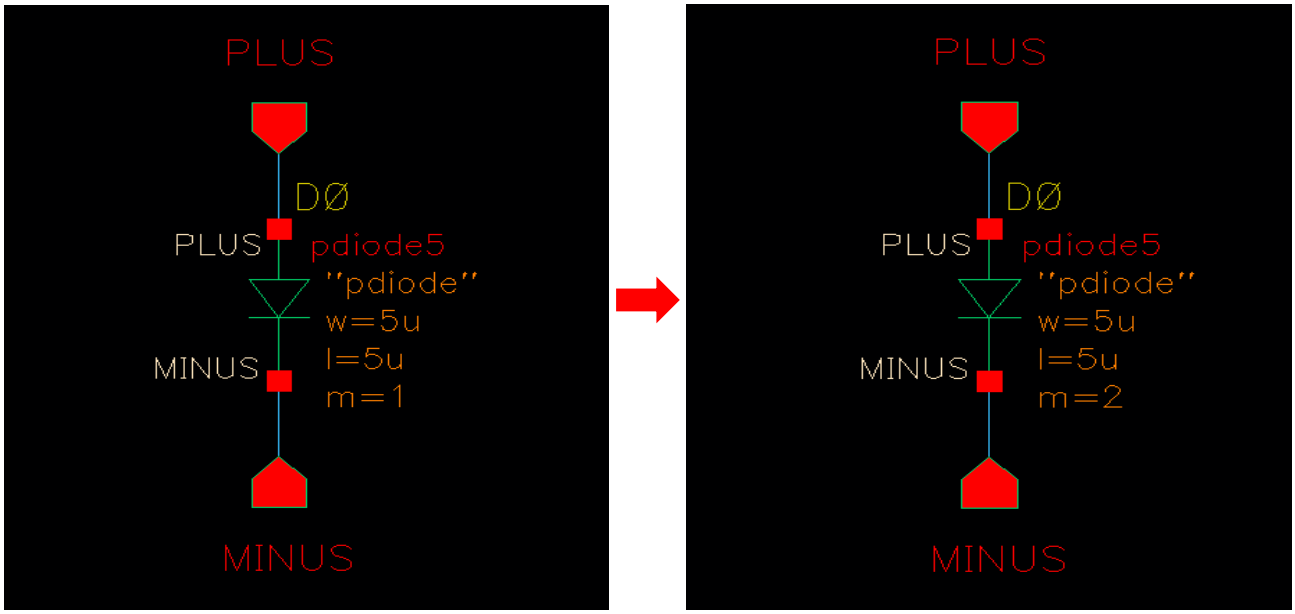


<Schematic parameter>

<cdl output>

3.14 pdiode5

Parameter					
Width	5.0u	Length	5.0u	multiplier	1 → 2



<Schematic parameter>

```
********************************************************
* Library Name: ETRI_lay
* Cell Name:    pdiode5
* View Name:    schematic
********************************************************

.SUBCKT pdiode5 MINUS PLUS
*.PININFO MINUS:I PLUS:I
DD0 PLUS MINUS pdiode m=1 w=5u l=5u
.ENDS
```

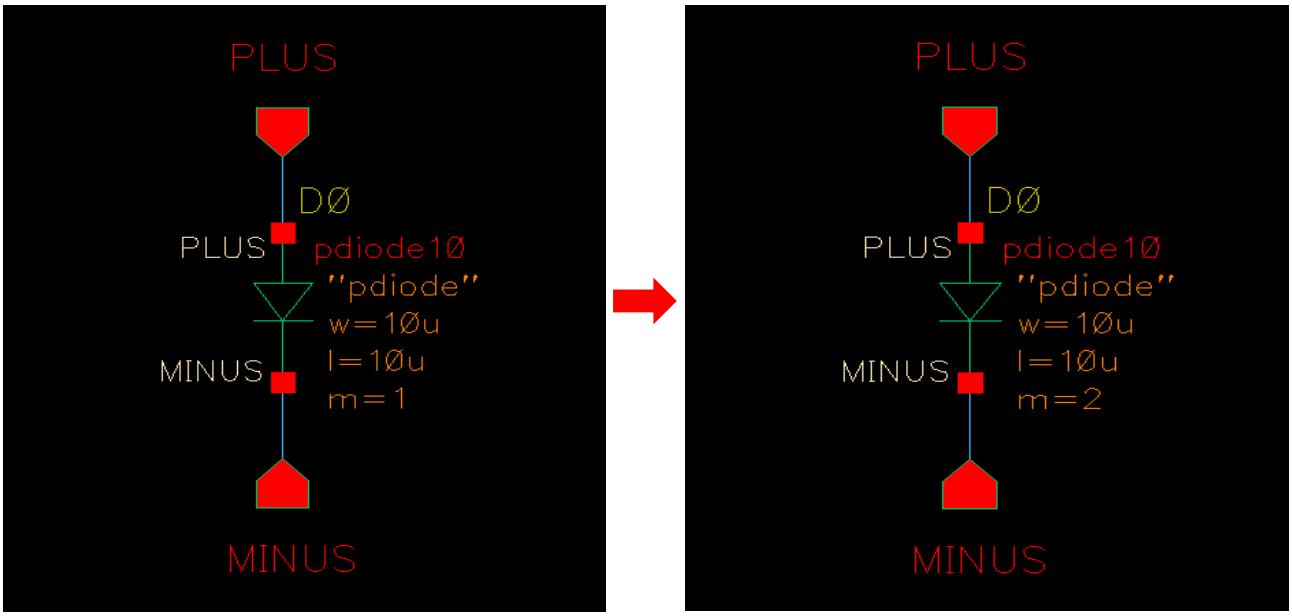
```
********************************************************
* Library Name: ETRI_lay
* Cell Name:    pdiode5
* View Name:    schematic
********************************************************

.SUBCKT pdiode5 MINUS PLUS
*.PININFO MINUS:I PLUS:I
DD0 PLUS MINUS pdiode m=2 w=5u l=5u
.ENDS
```

<cdl output>

3.15 pdiode10

Parameter					
Width	10.0u	Length	10.0u	multiplier	1 → 2



<Schematic parameter>

```
**************************************************
* Library Name: ETRI_lay
* Cell Name:    pdiode10
* View Name:    schematic
**************************************************

.SUBCKT pdiode10 MINUS PLUS
*.PININFO MINUS:I PLUS:I
DD0 PLUS MINUS pdiode m=1 w=10u l=10u
.ENDS
```

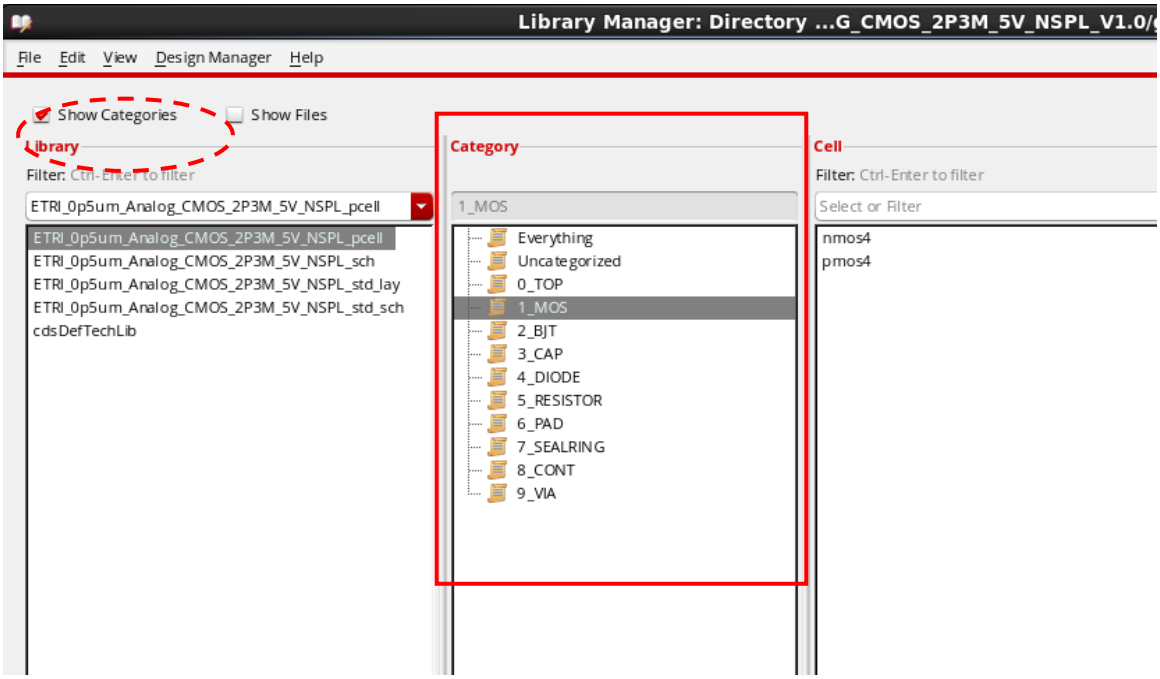
```
**************************************************
* Library Name: ETRI_lay
* Cell Name:    pdiode10
* View Name:    schematic
**************************************************

.SUBCKT pdiode10 MINUS PLUS
*.PININFO MINUS:I PLUS:I
DD0 PLUS MINUS pdiode m=2 w=10u l=10u
.ENDS
```

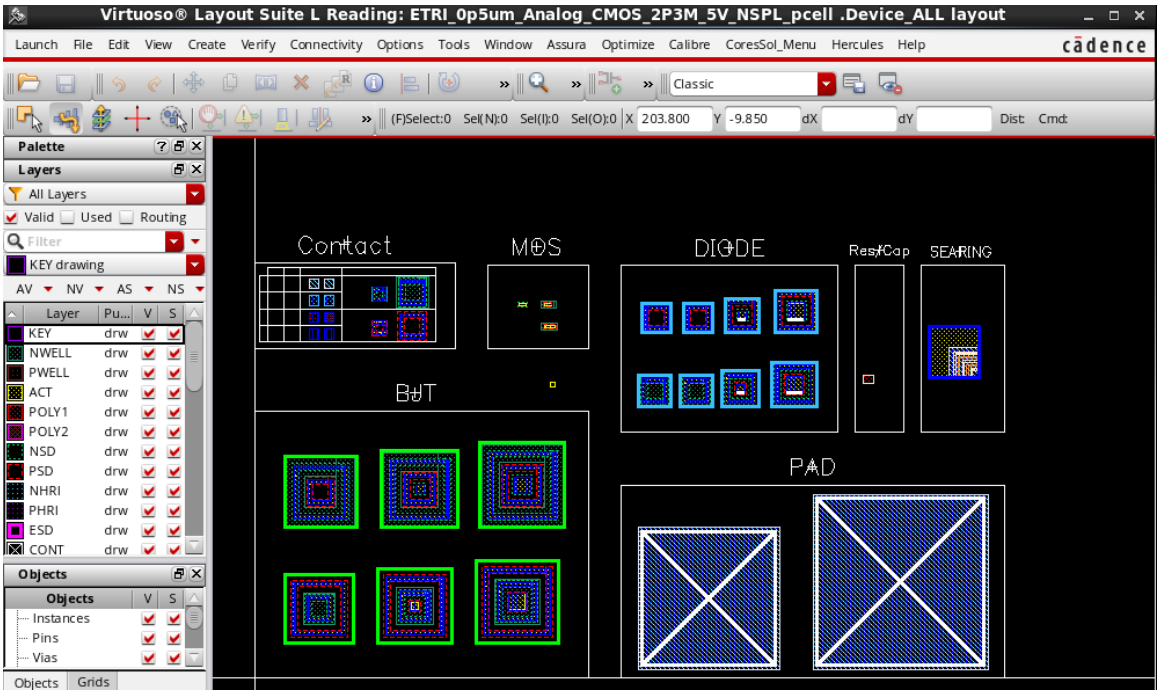
<cdl output>

4. PCELL Layout Library

4.1 Library Category

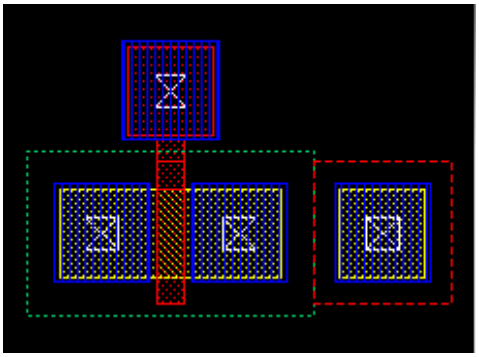


4.2 .Device_ALL

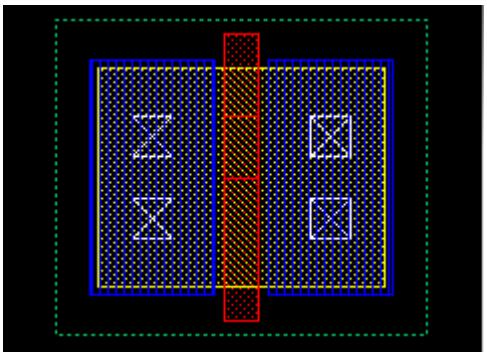


4.3 nmos4

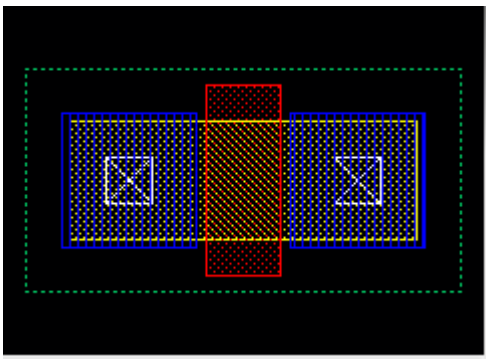
Parameter	Default	Change
width	1.6	*value*
length	0.5	*value*
multi	1	*value*
polyshift	0	*value*
polynumber	1	*value*
polycont	☑	☐
ptap	☑	☐



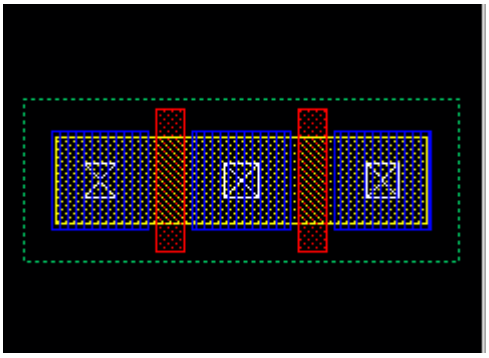
width	1.6	3.2



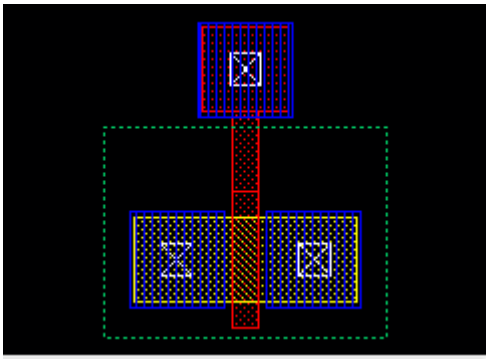
length	0.5	1.0



multi	1	2

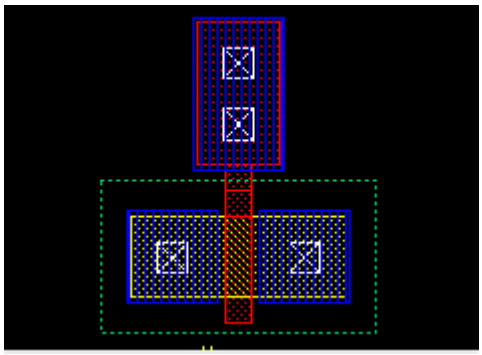


polyshift	0	1

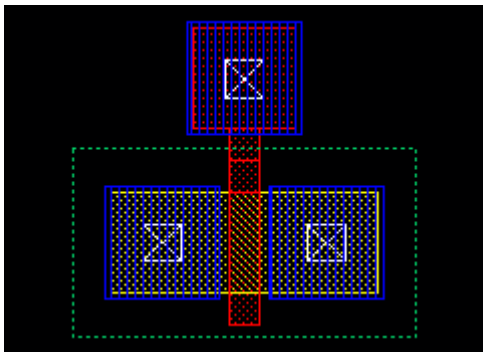


4.3 nmos4

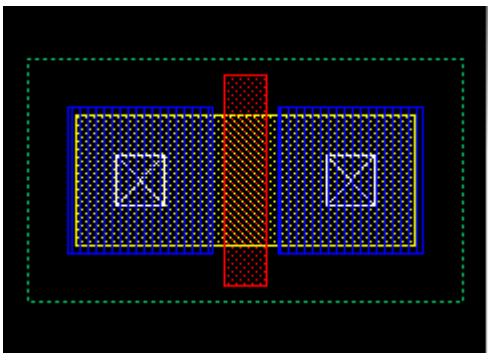
polynumber	1	*2*



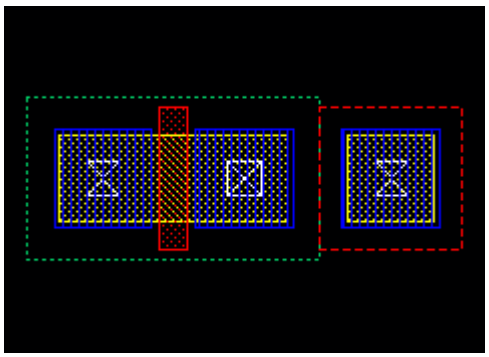
polycont	☑



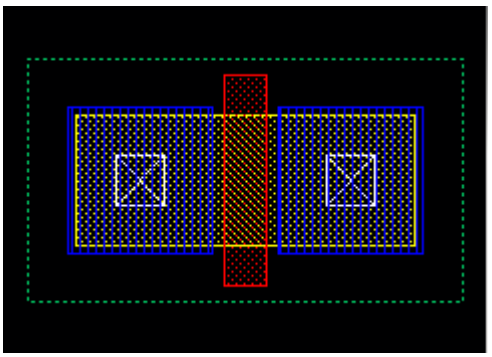
polycont	☐



ptap	☑

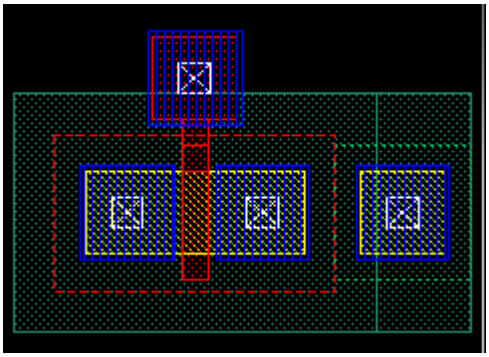


ptap	☐

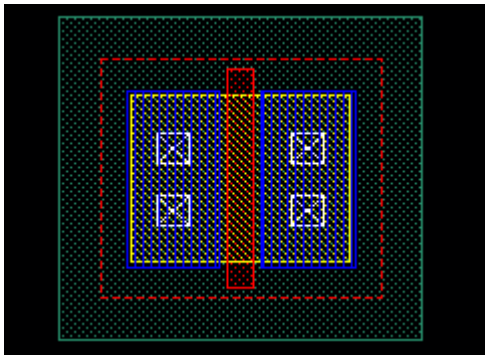


4.4 pmos4

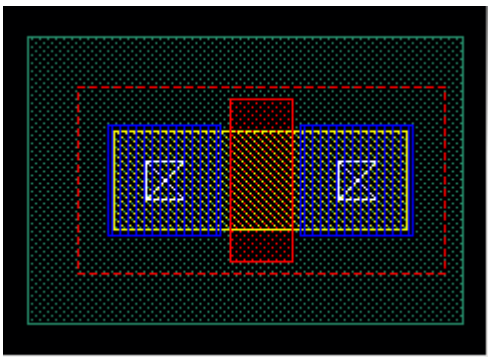
Parameter	Default	Change
width	1.6	*value*
length	0.5	*value*
multi	1	*value*
polyshift	0	*value*
polynumber	1	*value*
polycont	☑	☐
ntap	☑	☐



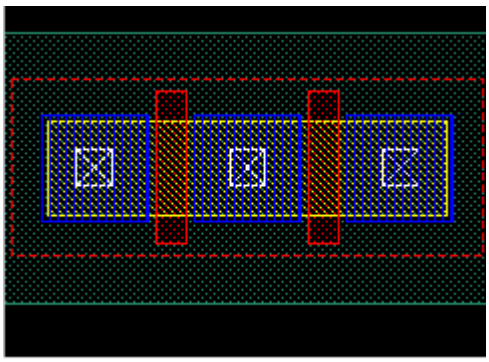
width	1.6	3.2



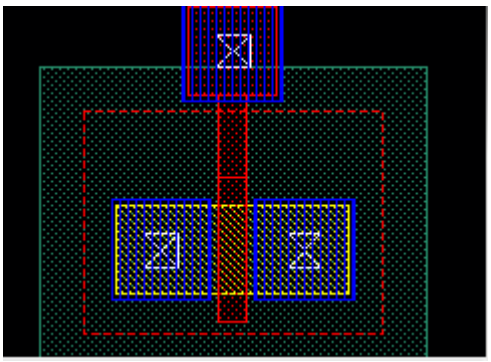
length	0.5	1.0



multi	1	2

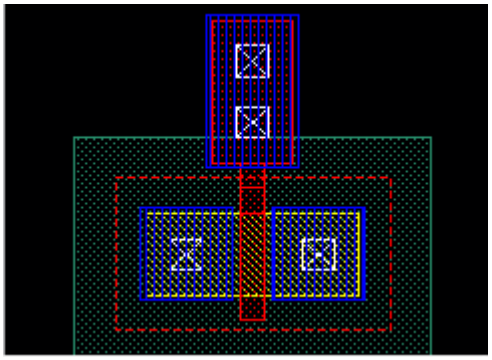


polyshift	0	1

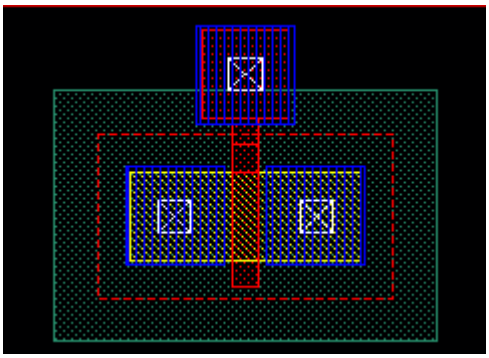


4.4 pmos4

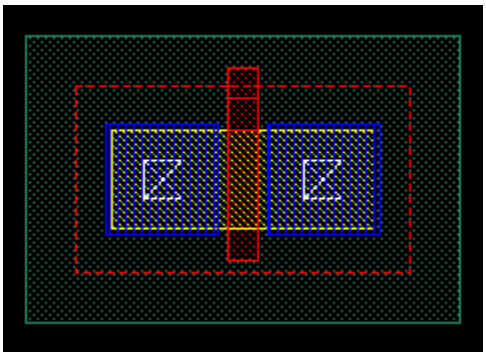
polynumber	1	*2*



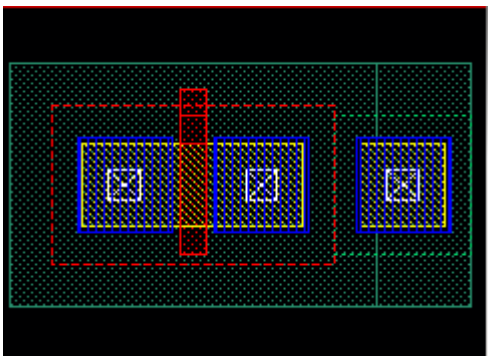
polycont	☑



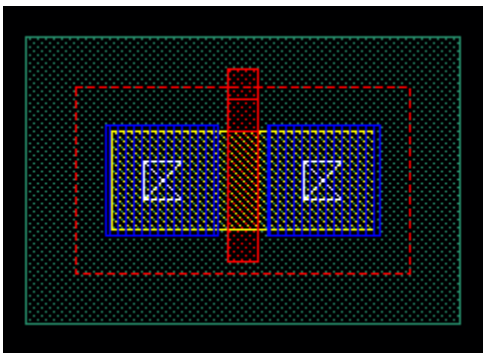
polycont	☐



ntap	☑

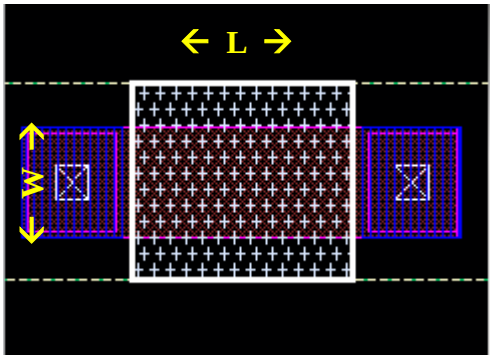


ntap	☐

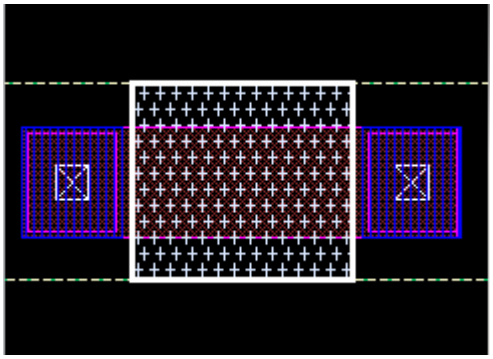


4.5 npres

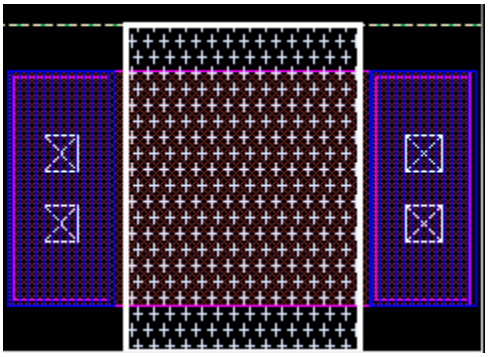
Parameter	Default	Change
W	2	*value*
L	4	*value*



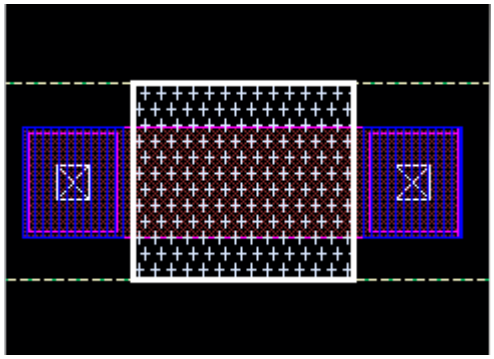
W	2



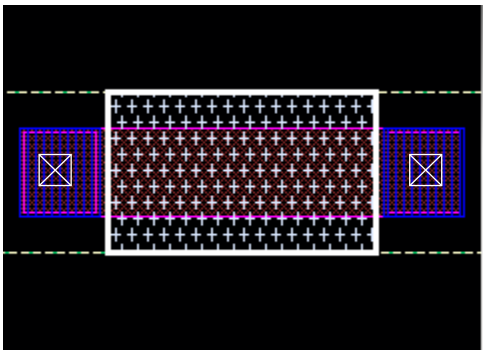
W	4



L	4

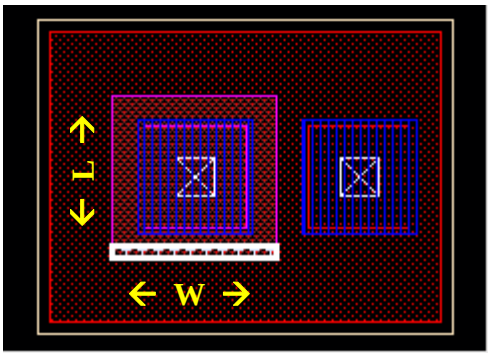


L	6



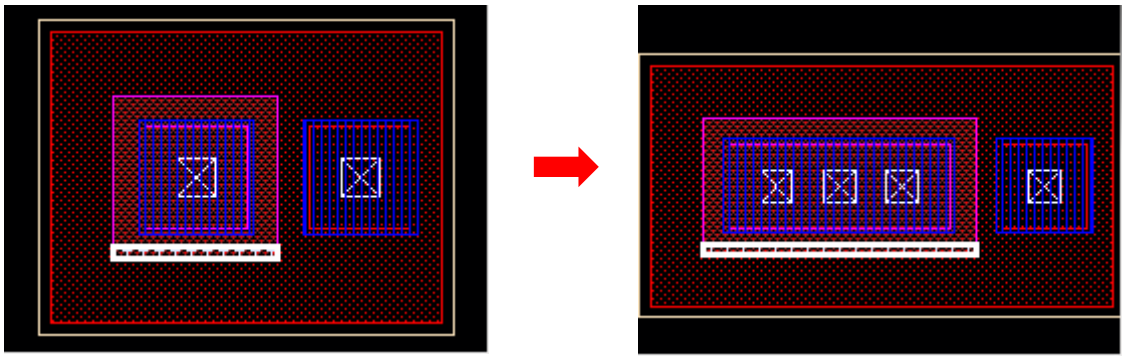
4.6 pipcap

Parameter	Default	Change
W	2.6	*value*
L	2.6	*value*



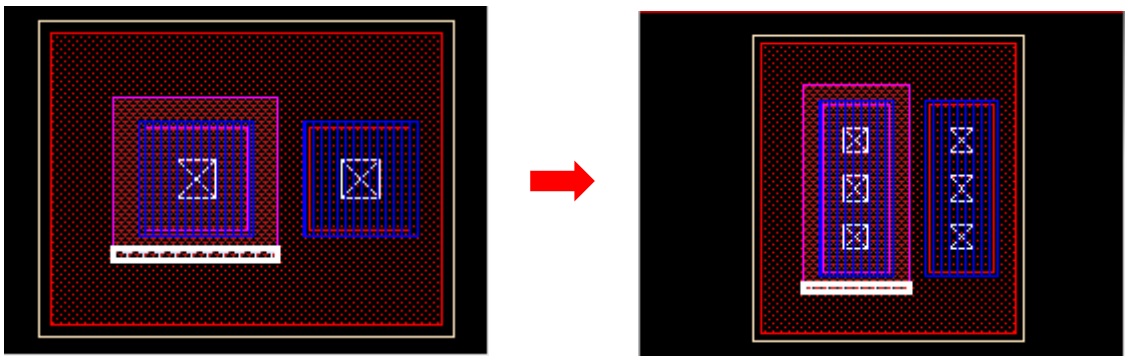
W	2.6

W	5.2



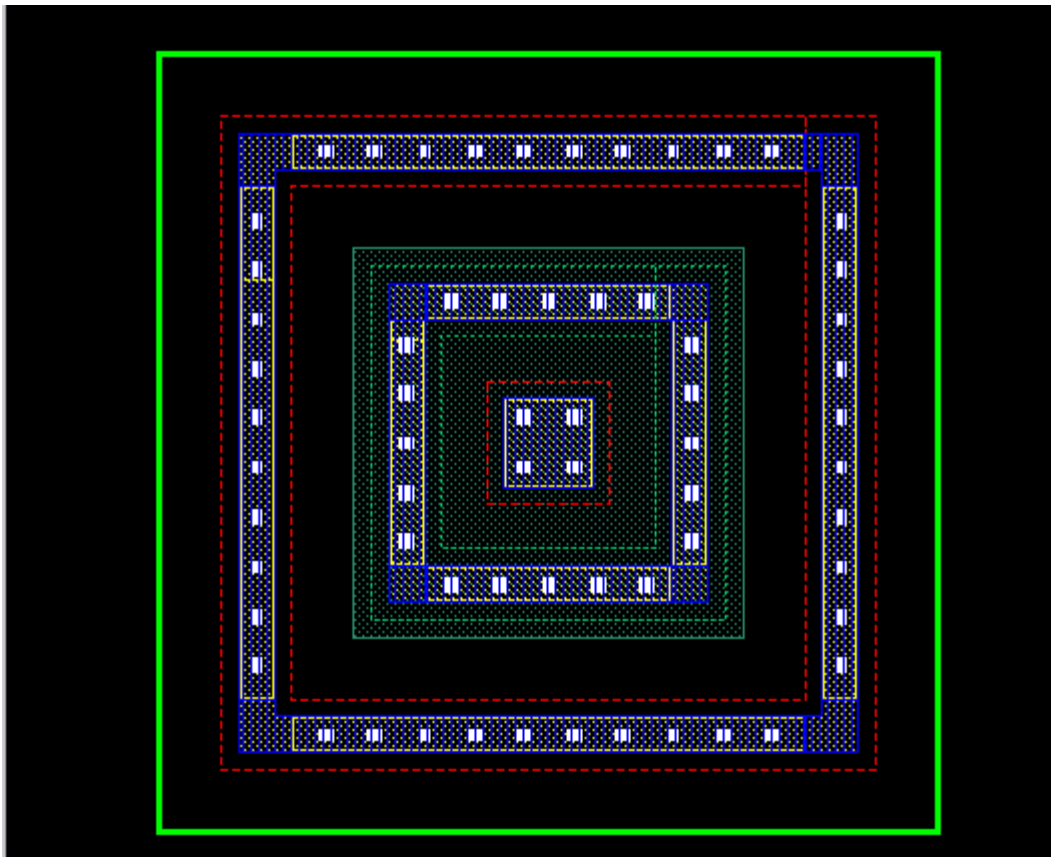
L	2.6

L	5.2



4.7 pnp5

Parameter	Default	Change
-	-	-

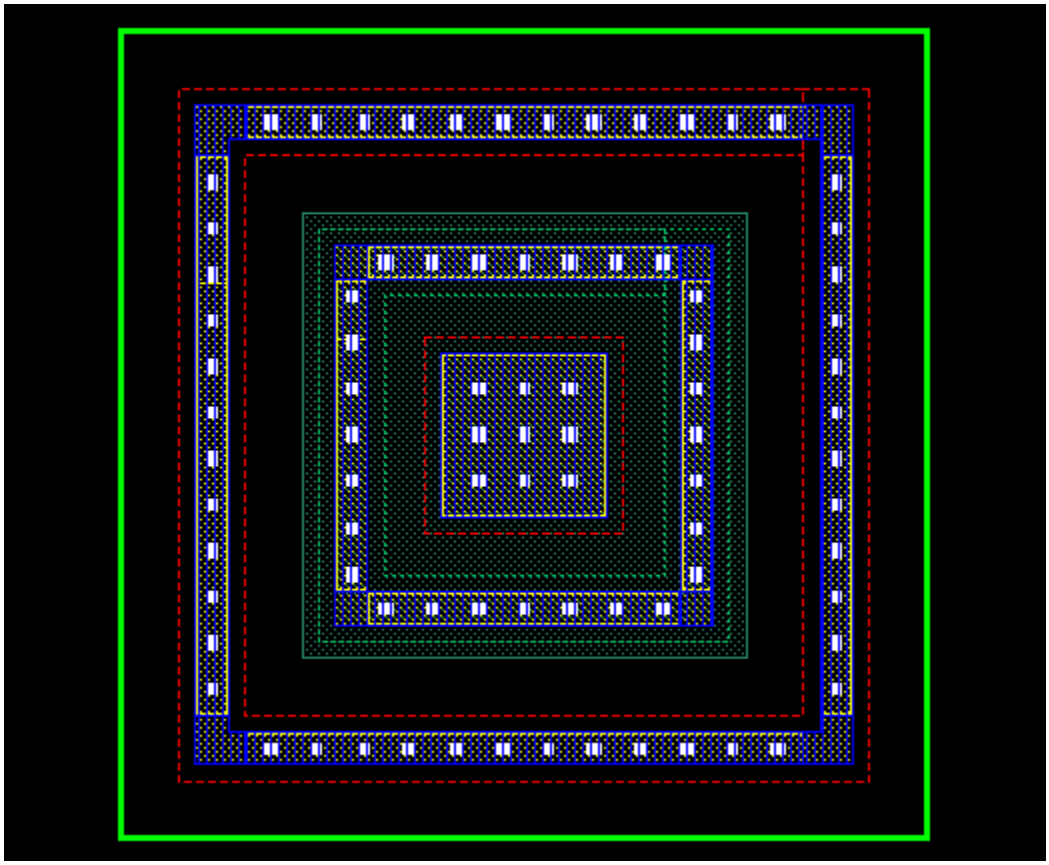


BJT doesn’t change PCELL
It must be used PCELL

BJT layer on BJT device
can’t be overlapped each other

4.8 pnp10

Parameter	Default	Change
-	-	-

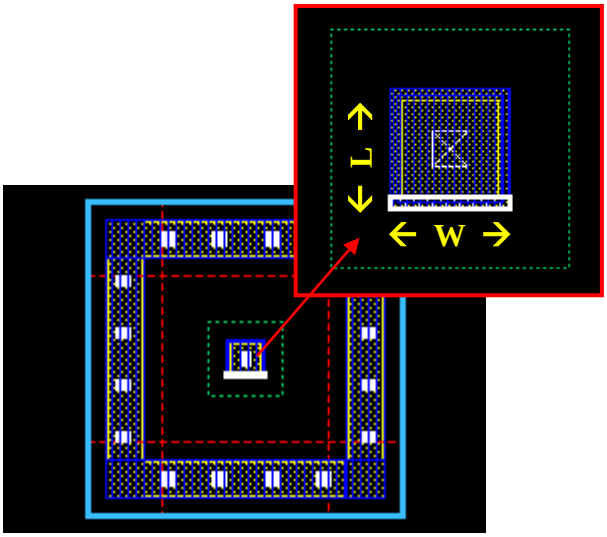


BJT doesn’t change PCELL
It must be used PCELL

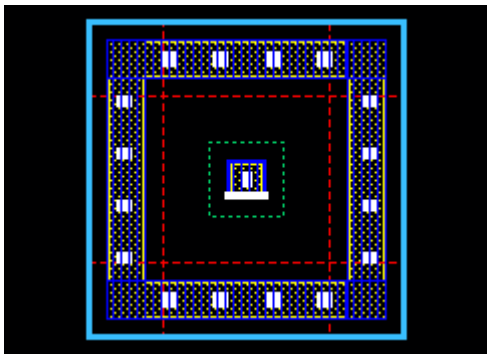
BJT layer on BJT device
can’t be overlapped each other

4.9 ndiode

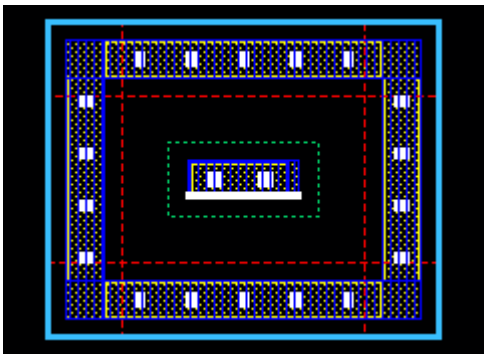
Parameter	Default	Change
W	2	*value*
L	2	*value*



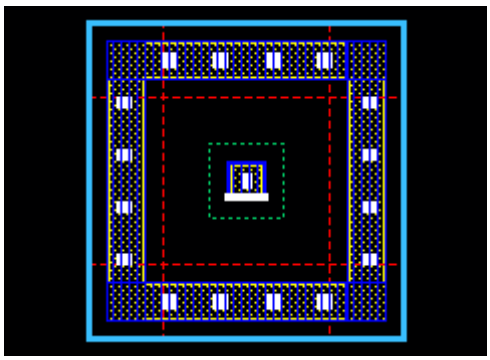
W	2



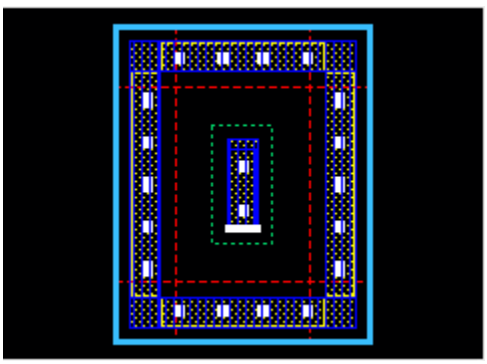
W	6



L	2

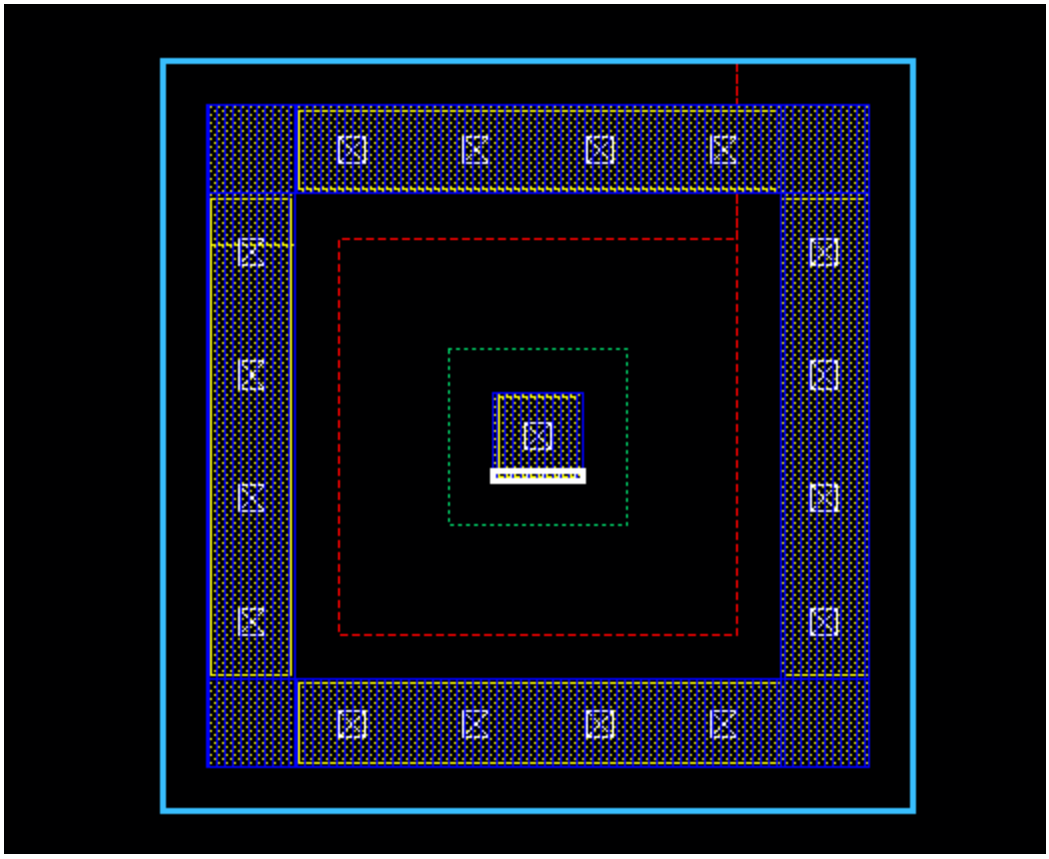


L	6



4.10 ndiode2

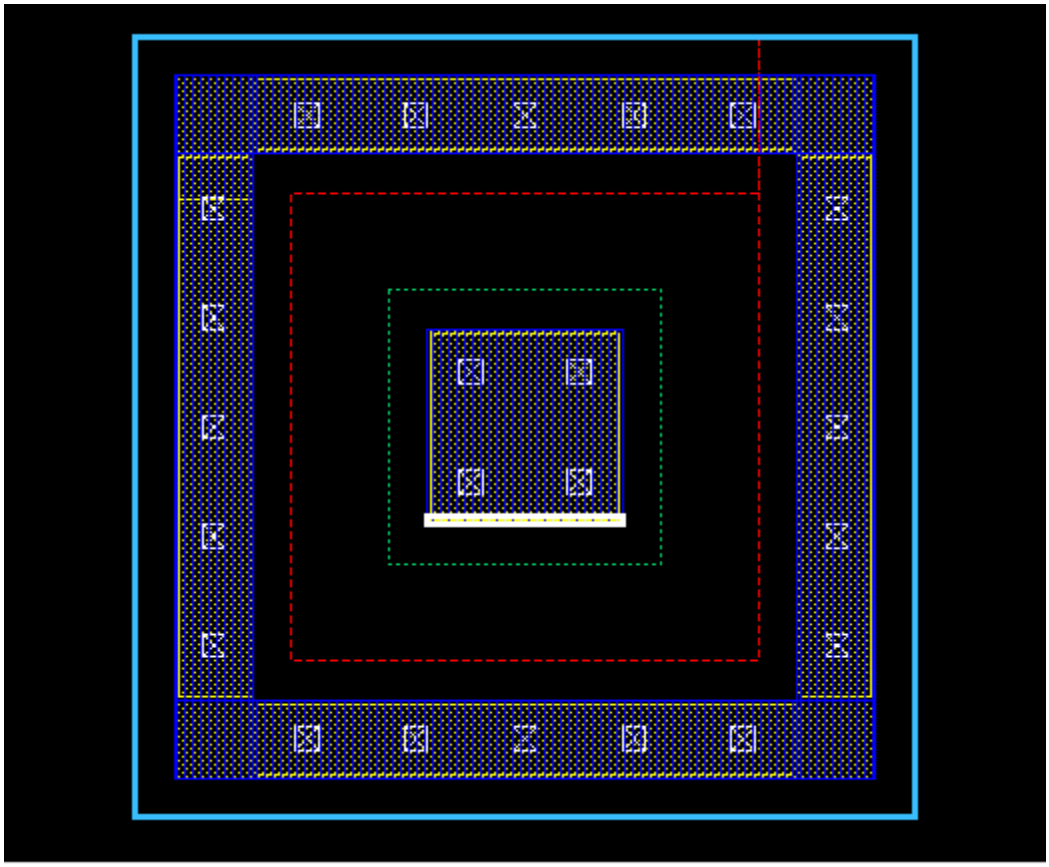
Parameter	Default	Change
-	-	-



NDIODE Fixed Size
→ doesn't provide parameter modification

4.11 ndiode5

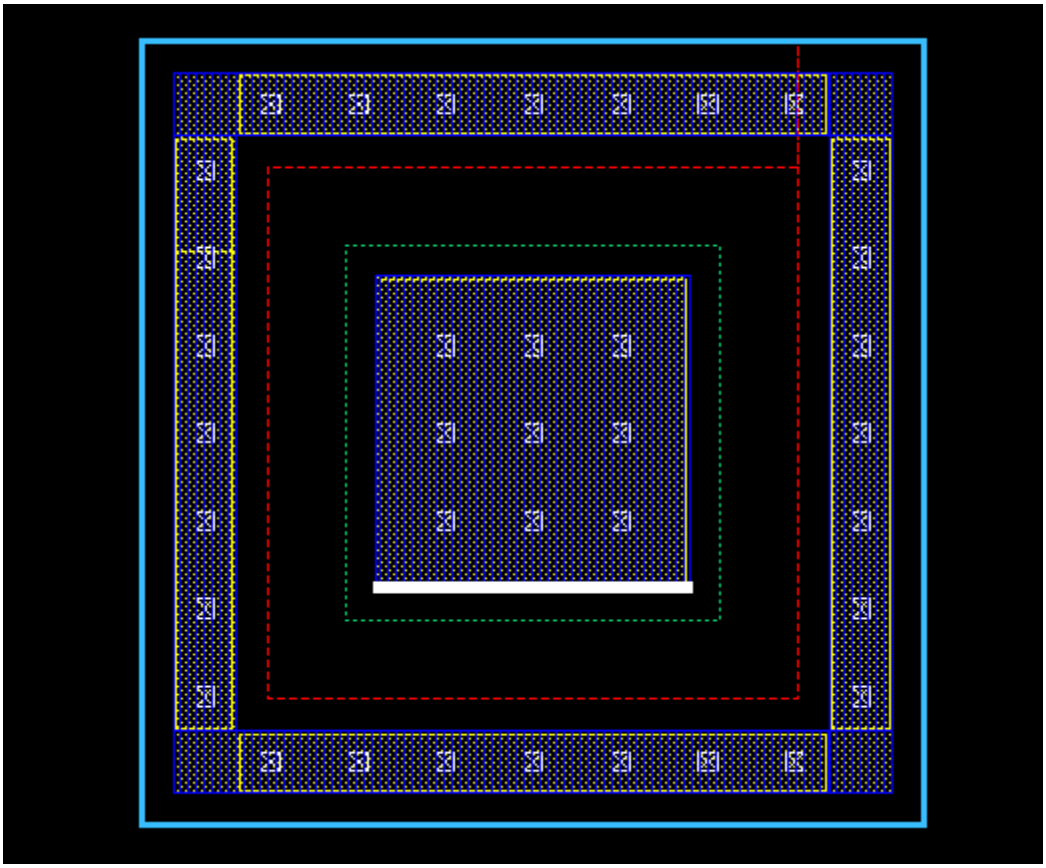
Parameter	Default	Change
-	-	-



NDIODE Fixed Size
→ doesn't provide parameter modification

4.12 ndiode10

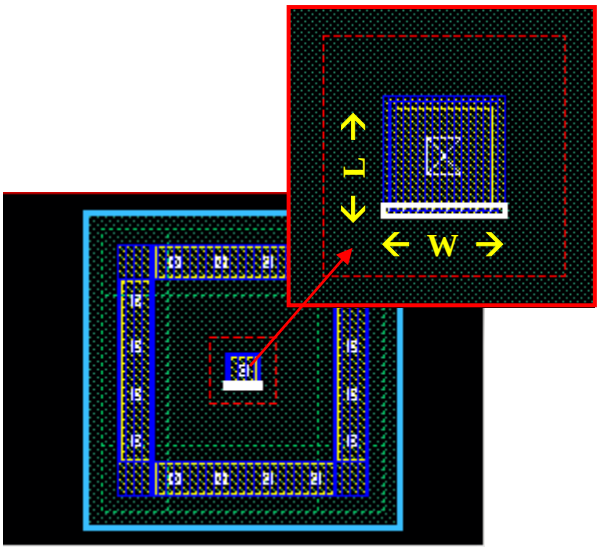
Parameter	Default	Change
-	-	-



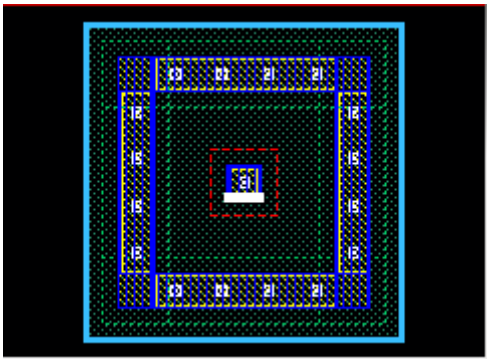
NDIODE Fixed Size
→ doesn't provide parameter modification

4.13 pdiode

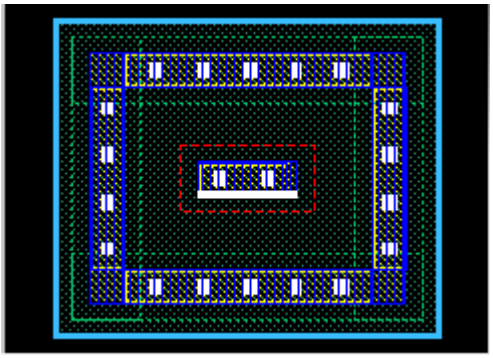
Parameter	Default	Change
W	2	*value*
L	2	*value*



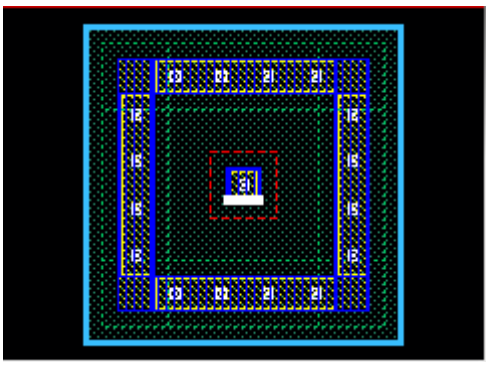
W	2



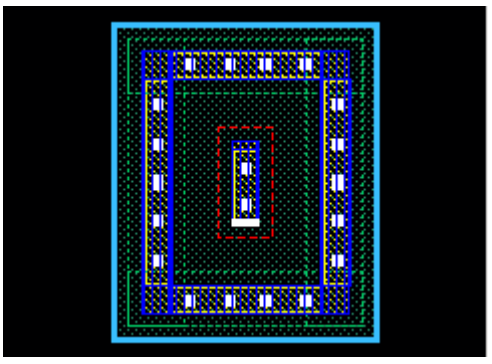
W	6



L	2

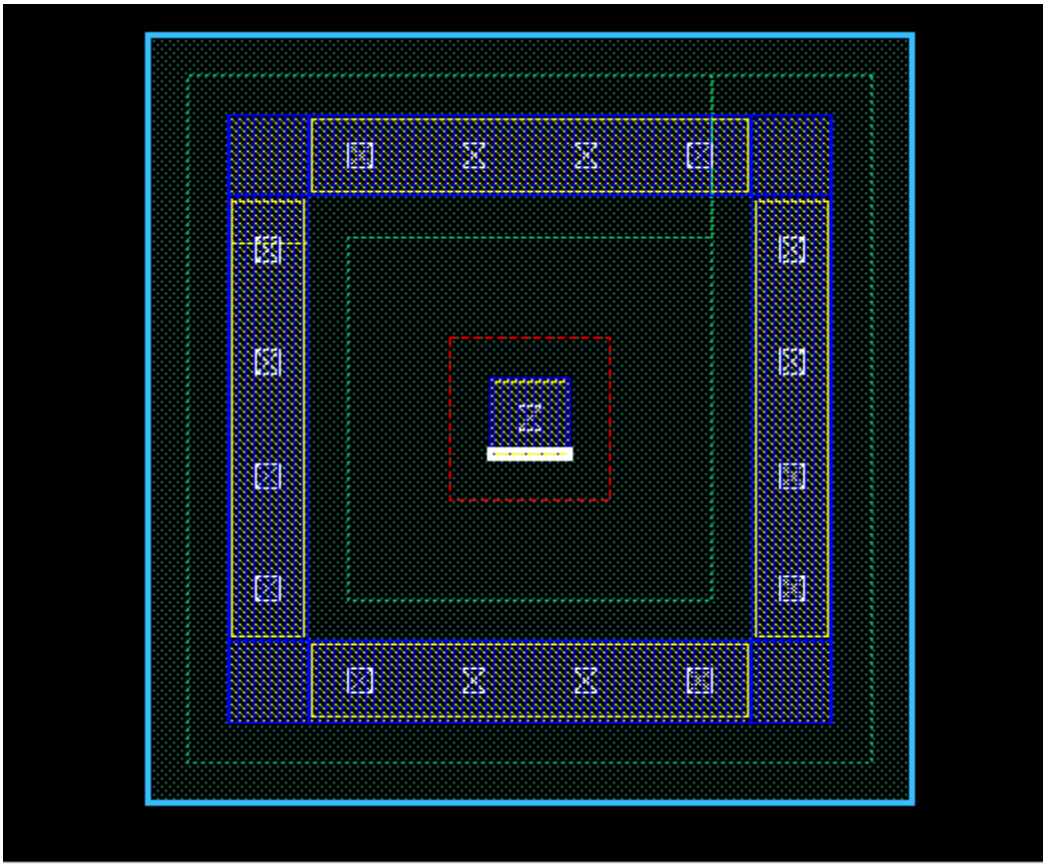


L	6



4.14 pdiode2

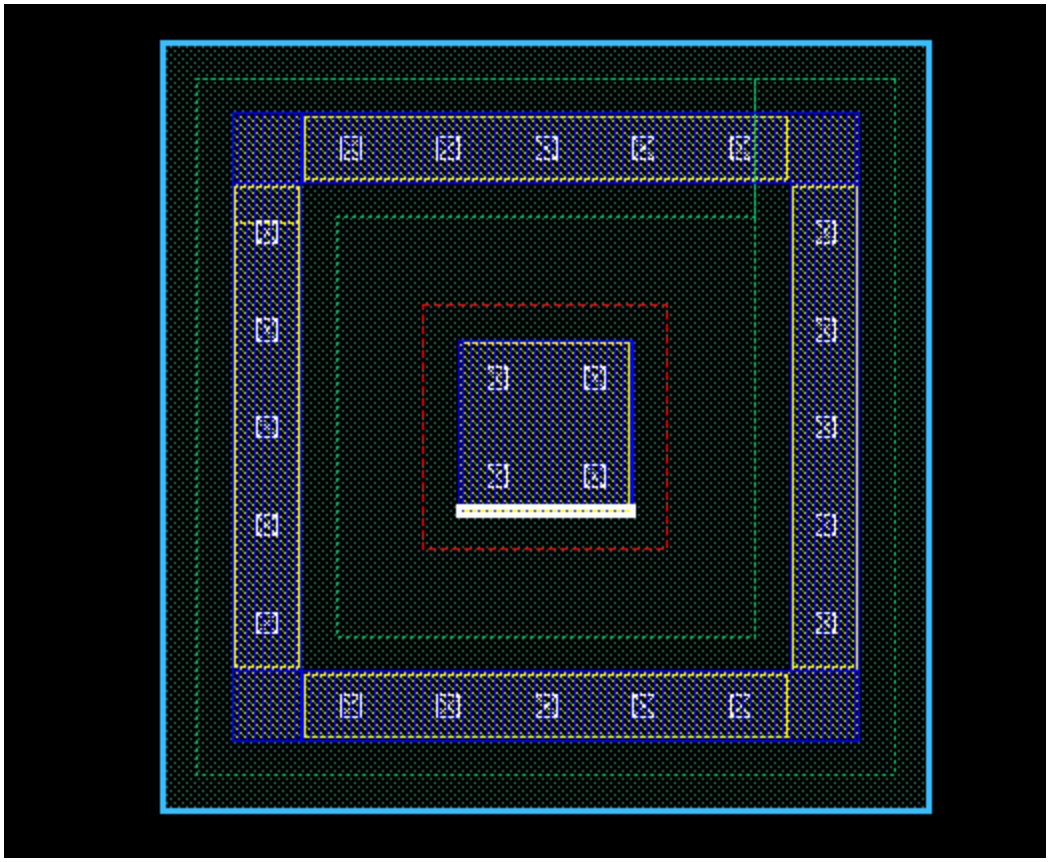
Parameter	Default	Change
-	-	-



PDIODE Fixed Size
→ doesn't provide parameter modification

4.15 pdiode5

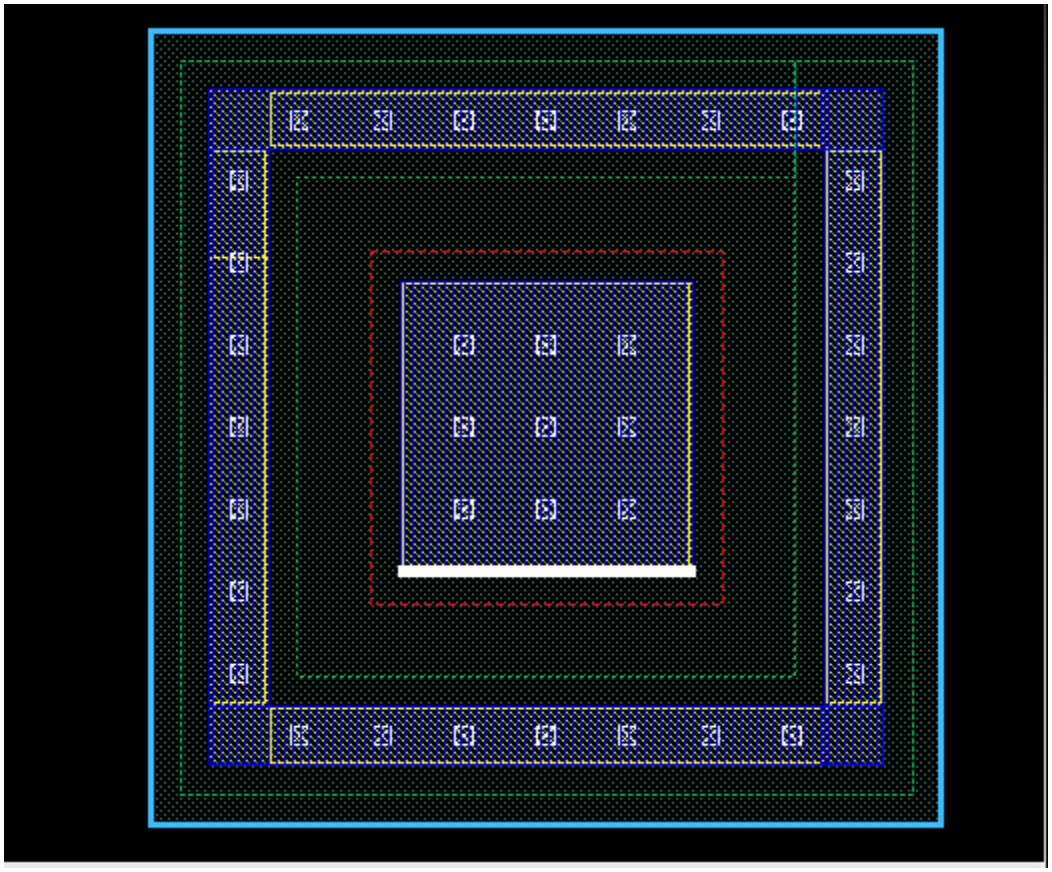
Parameter	Default	Change
-	-	-



PDIODE Fixed Size
→ doesn't provide parameter modification

4.16 pdiode10

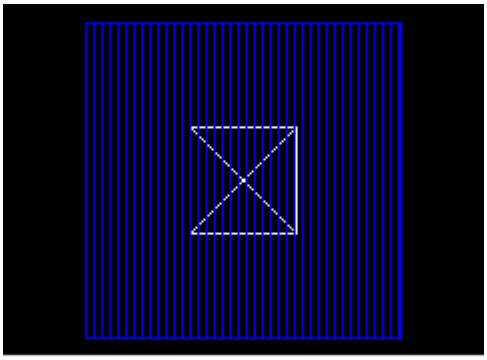
Parameter	Default	Change
-	-	-



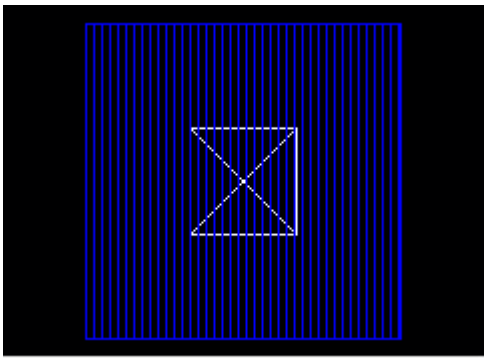
PDIODE Fixed Size
→ doesn't provide parameter modification

4.17 cont

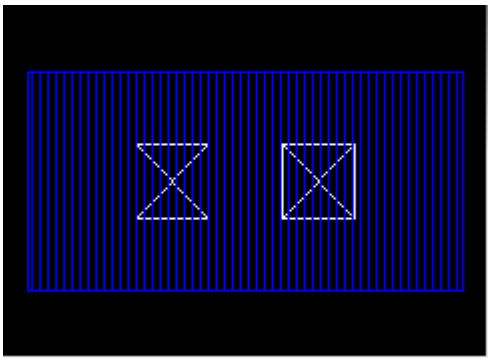
Parameter	Default	Change
x_size	1.8	*value*
y_size	1.8	*value*



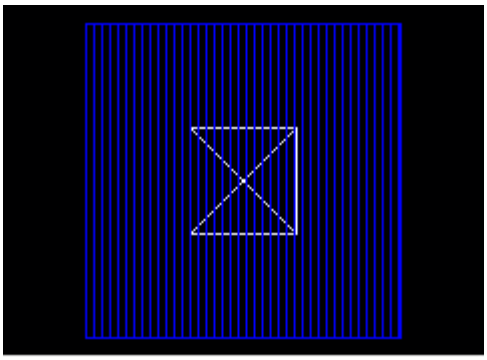
x_size	1.8



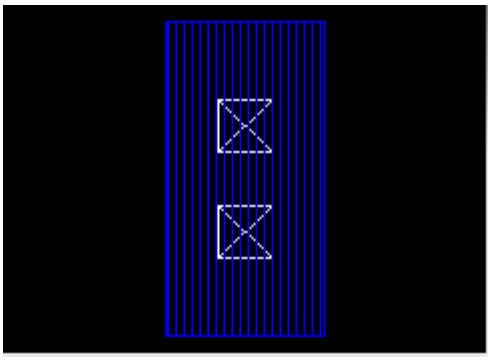
x_size	3.6



y_size	1.8

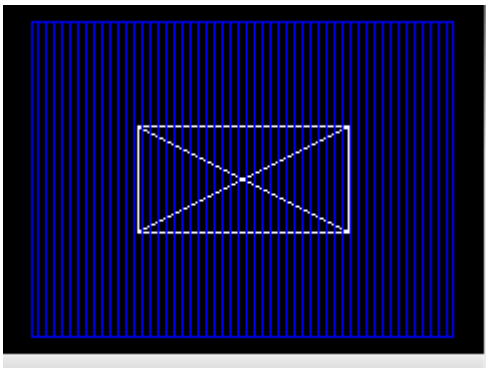


y_size	3.6

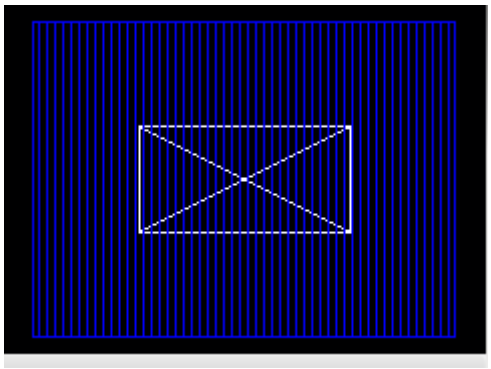


4.18 cont_bar

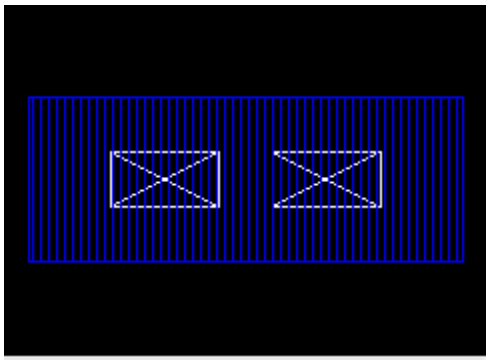
Parameter	Default	Change
x_size	2.4	*value*
y_size	1.8	*value*



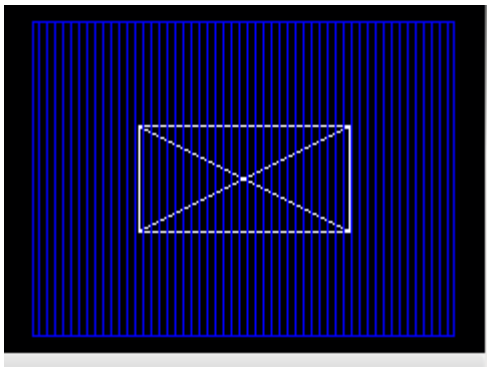
x_size	2.4



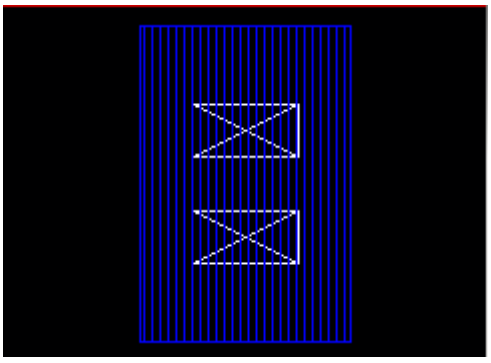
x_size	4.8



y_size	1.8

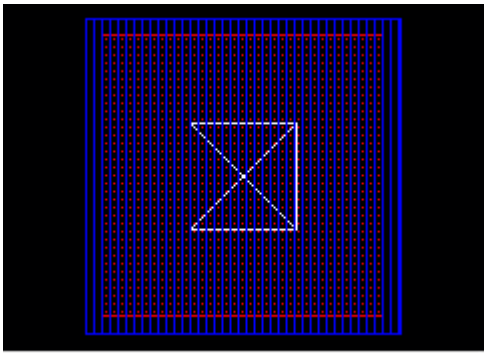


y_size	3.6

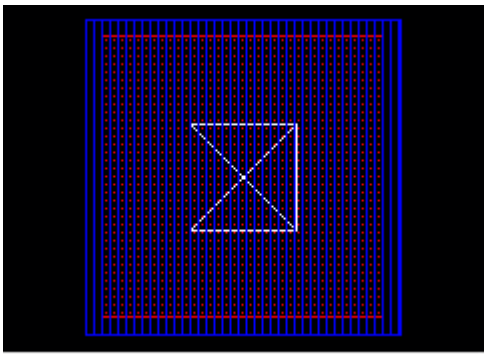


4.19 poly1cont

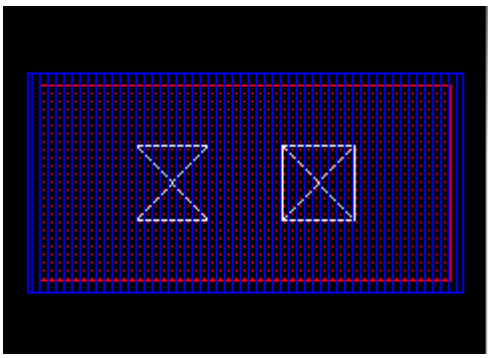
Parameter	Default	Change
x_size	1.8	*value*
y_size	1.8	*value*



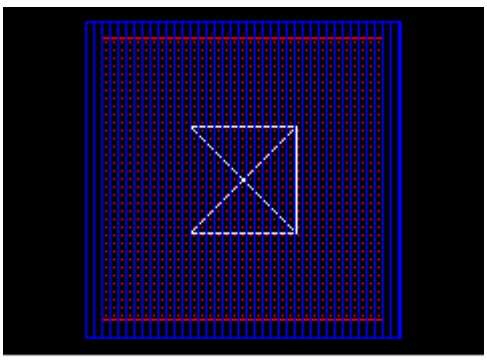
x_size	1.8



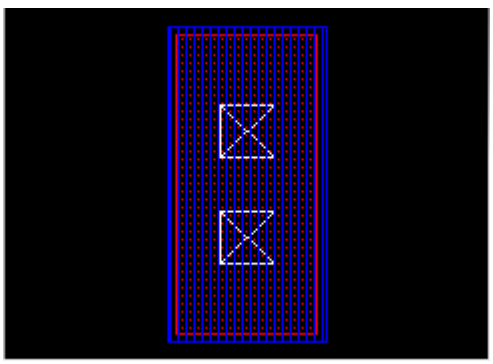
x_size	3.6



y_size	1.8

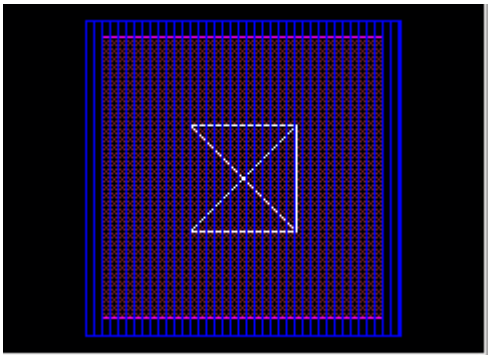


y_size	3.6

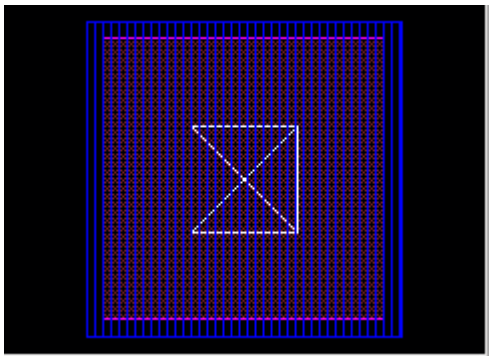


4.20 poly2cont

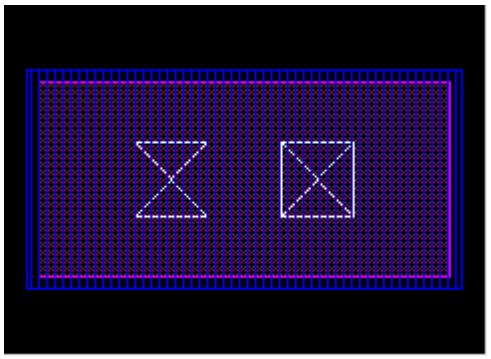
Parameter	Default	Change
x_size	1.8	*value*
y_size	1.8	*value*



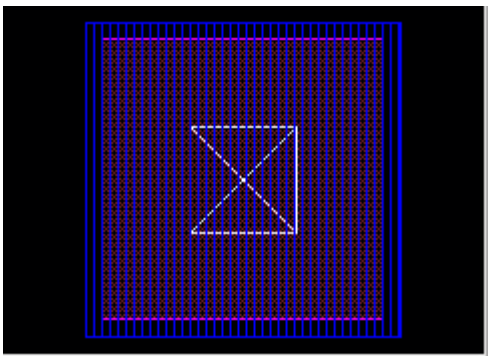
x_size	1.8



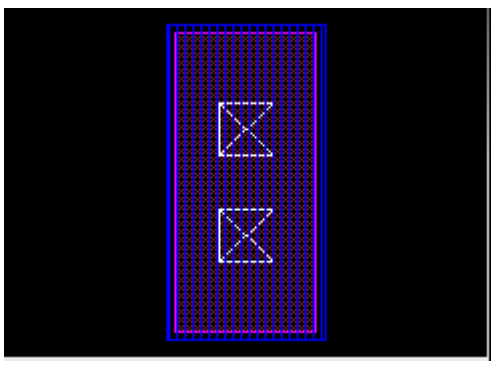
x_size	3.6



y_size	1.8

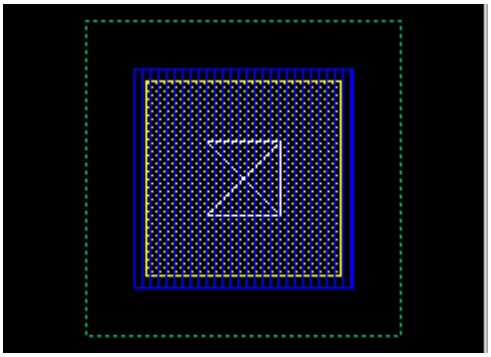


y_size	3.6

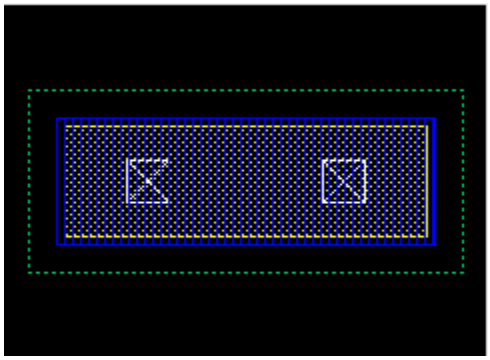


4.21 ntap

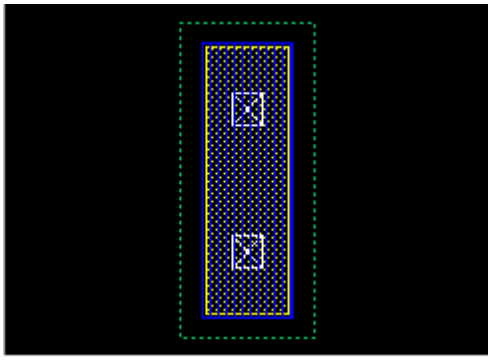
Parameter	Default	Change
x_size	1.8	*value*
y_size	1.8	*value*
NSD	☑	☐



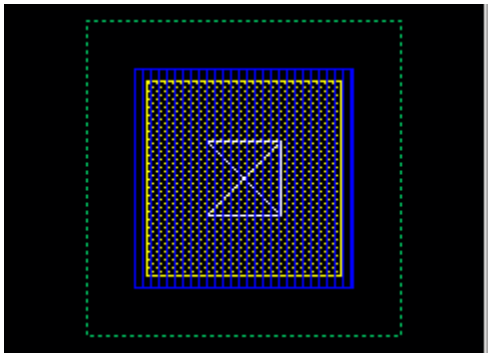
x_size	1.8	5.4



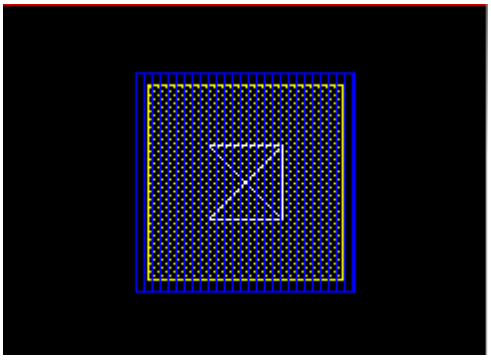
y_size	1.8	5.4



NSD	☑

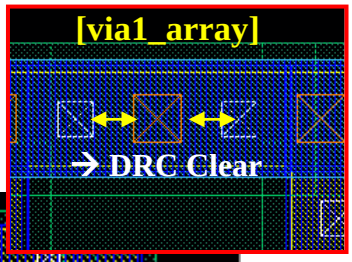


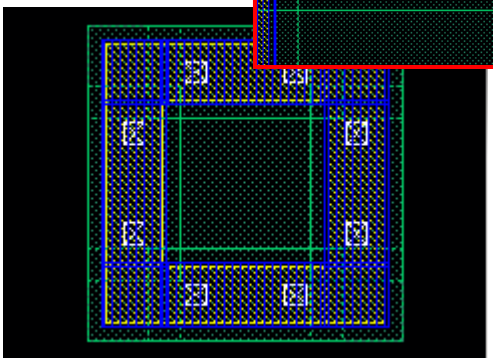
NSD	☐



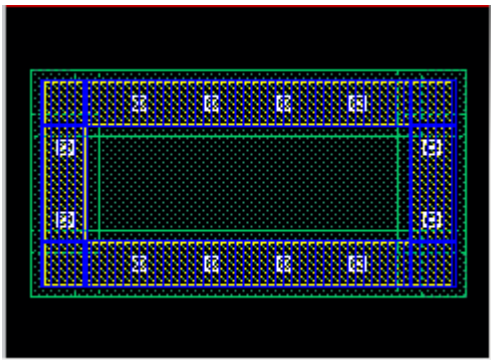
4.22 ntap_ring

Parameter	Default	Change
x_size	8	*value*
y_size	8	*value*
TOP	☑	☐
BOTTOM	☑	☐
LEFT	☑	☐
RIGHT	☑	☐

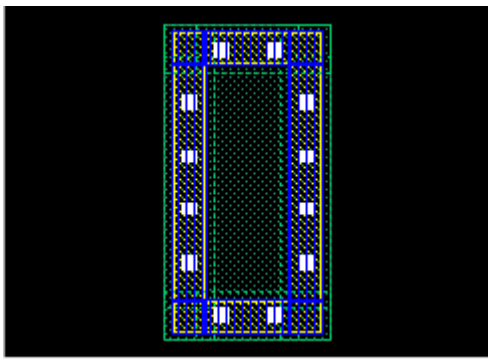




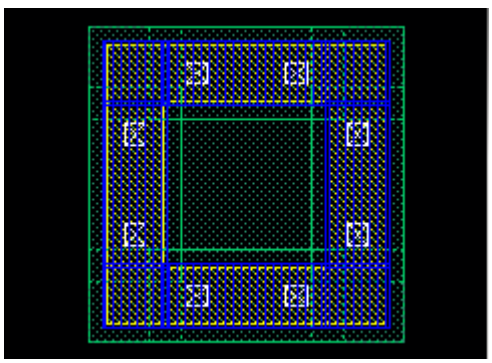
x_size	8	16



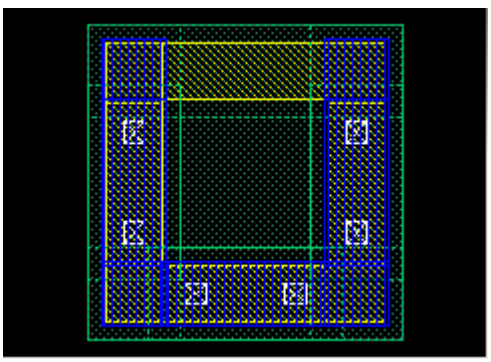
y_size	8	16



TOP	☑

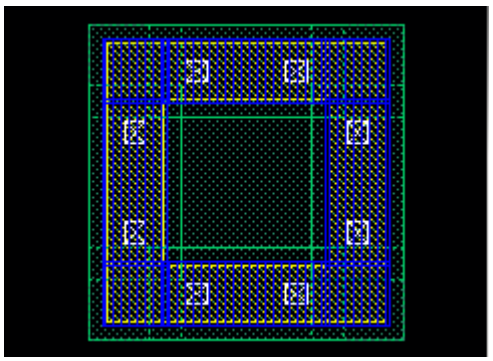


TOP	☐

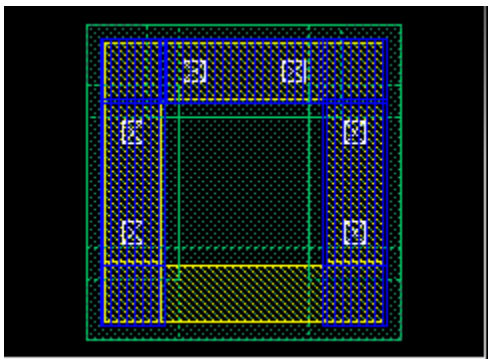


4.22 ntap_ring

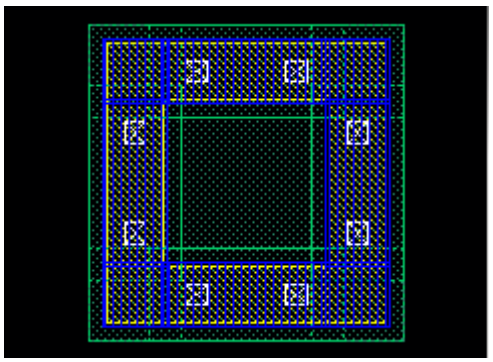
BOTTOM	☑



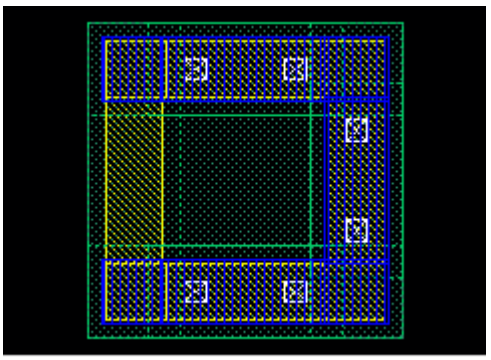
BOTTOM	☐



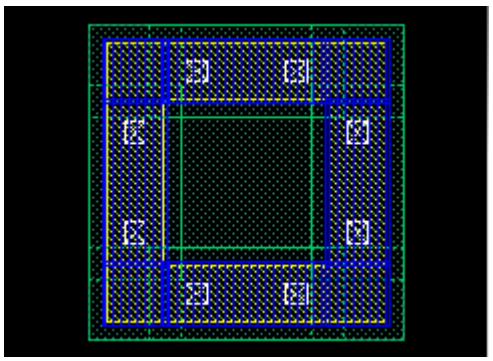
LEFT	☑



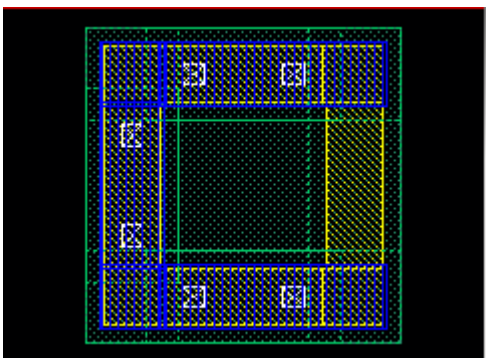
LEFT	☐



RIGHT	☑

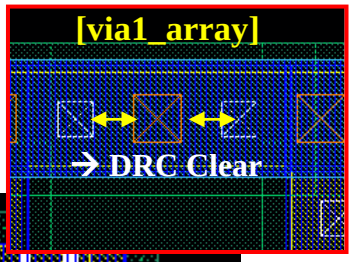


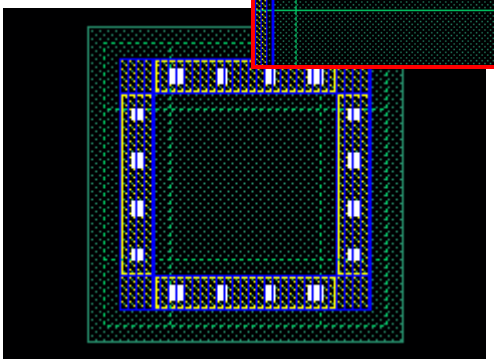
RIGHT	☐



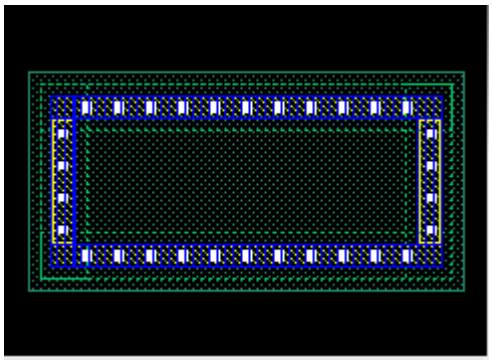
4.23 ntap_ring_pdiode

Parameter	Default	Change
x_size	19	*value*
y_size	19	*value*
TOP	☑	☐
BOTTOM	☑	☐
LEFT	☑	☐
RIGHT	☑	☐

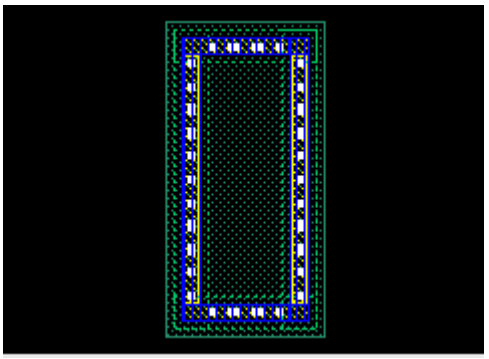




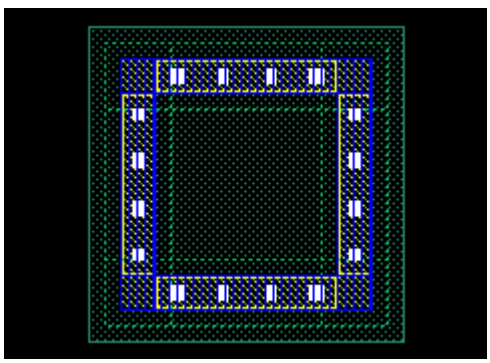
x_size	19	38



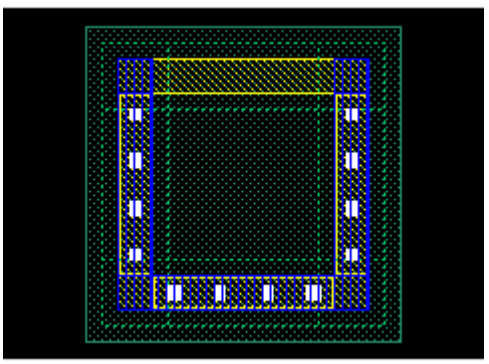
y_size	19	38



TOP	☑

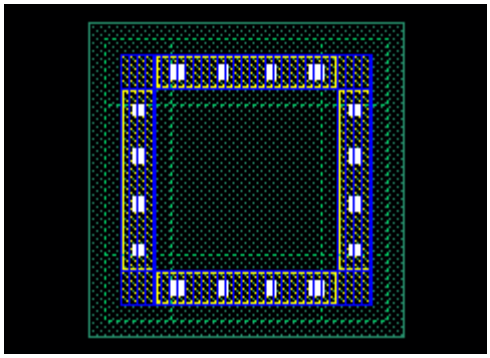


TOP	☐

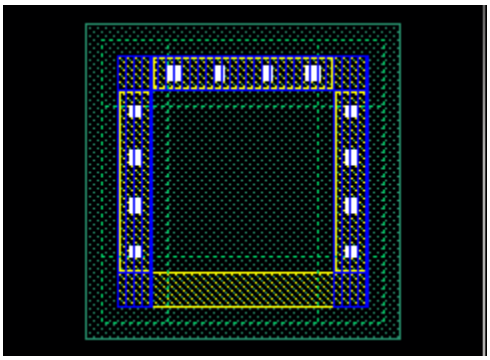


4.23 ntap_ring_pdiode

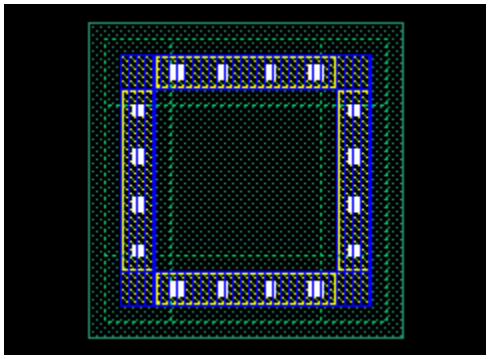
BOTTOM	☑



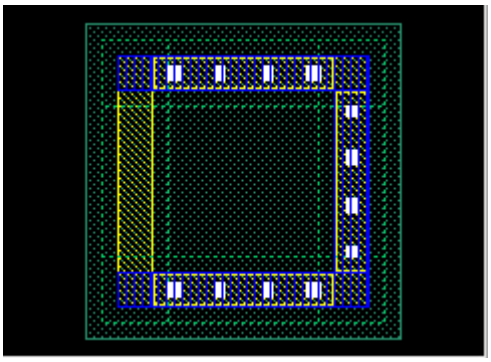
BOTTOM	☐



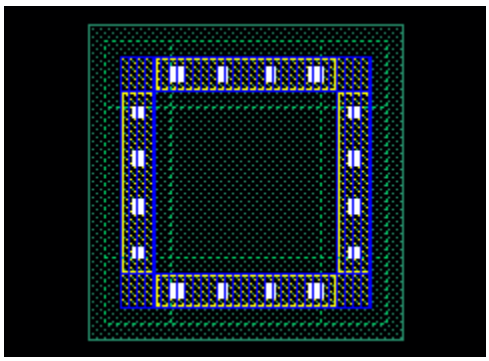
LEFT	☑



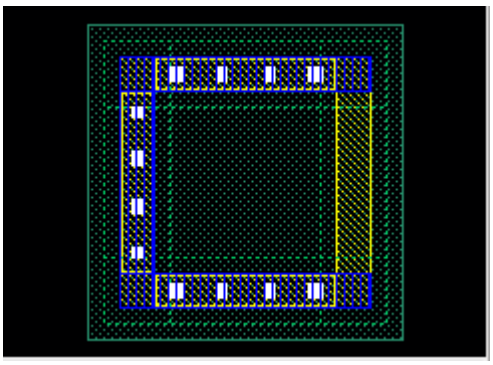
LEFT	☐



RIGHT	☑

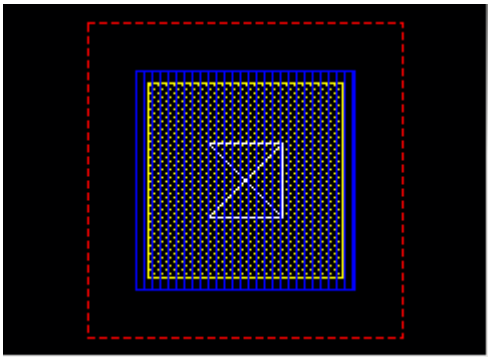


RIGHT	☐

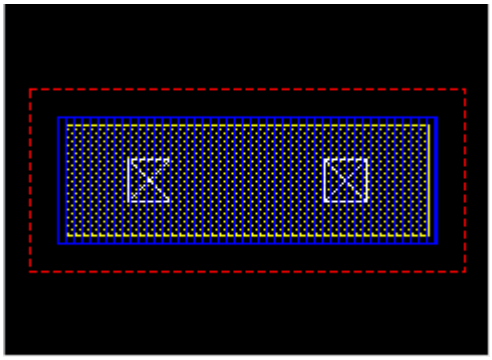


4.24 ptap

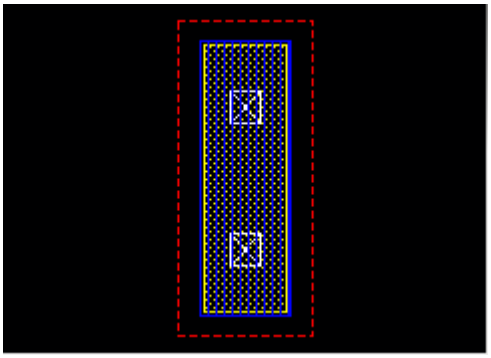
Parameter	Default	Change
x_size	1.8	*value*
y_size	1.8	*value*
PSD	☑	☐



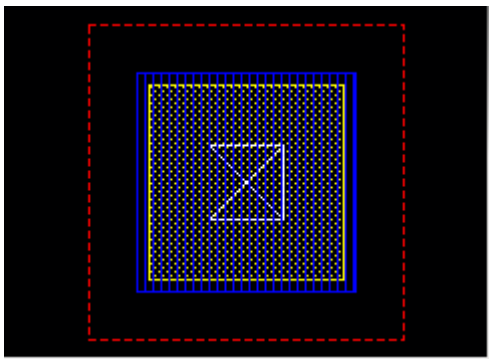
x_size	1.8	5.4



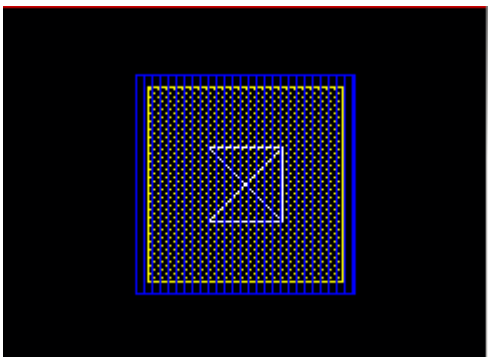
y_size	1.8	5.4



PSD	☑

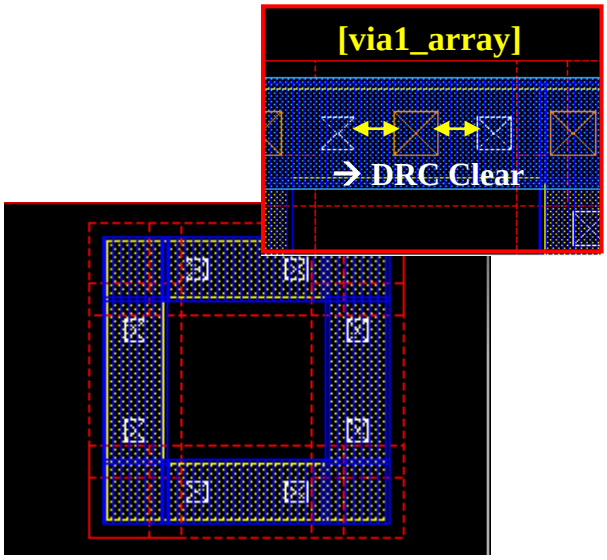


PSD	☐

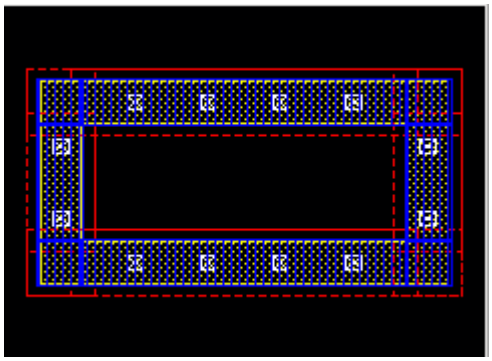


4.25 ptap_ring

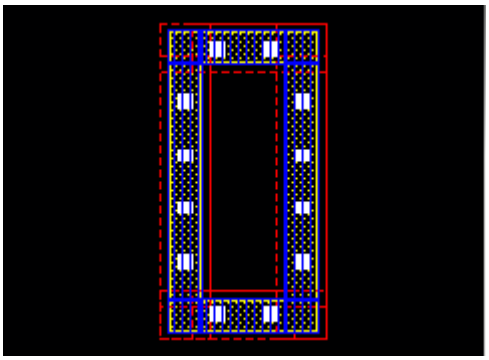
Parameter	Default	Change
x_size	8	*value*
y_size	8	*value*
TOP	☑	☐
BOTTOM	☑	☐
LEFT	☑	☐
RIGHT	☑	☐



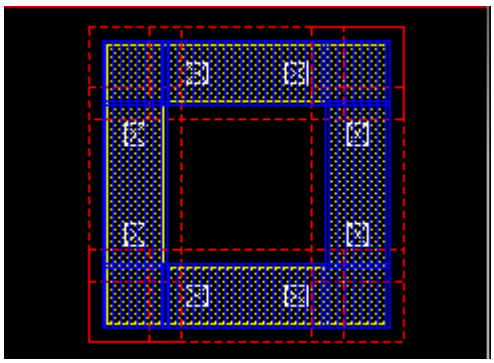
x_size	8	16



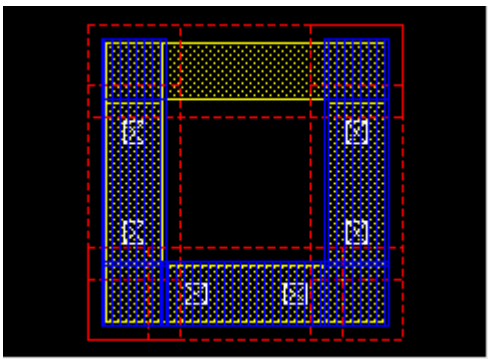
y_size	8	16



TOP	☑

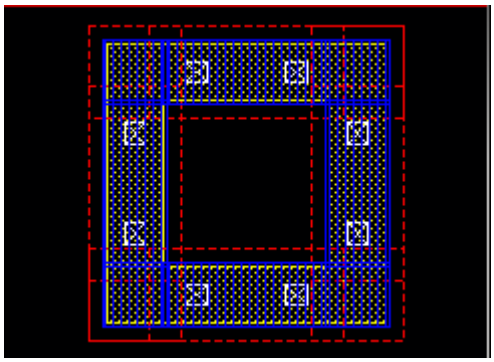


TOP	☐

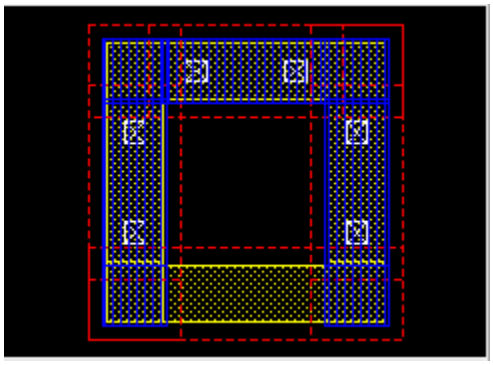


4.25 ptap_ring

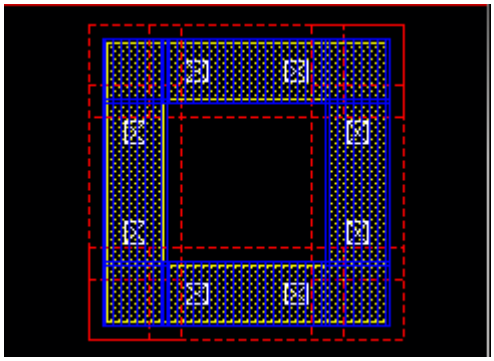
BOTTOM	☑



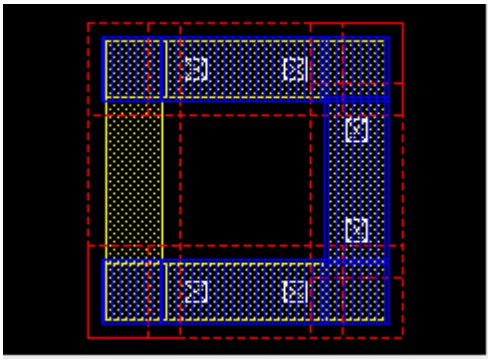
BOTTOM	☐



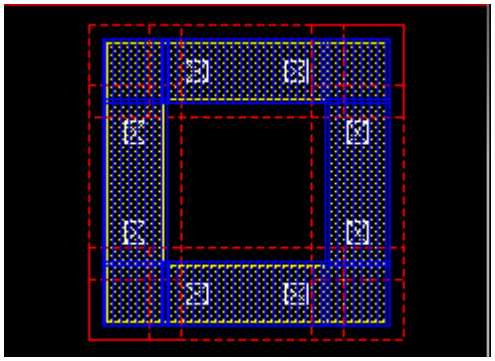
LEFT	☑



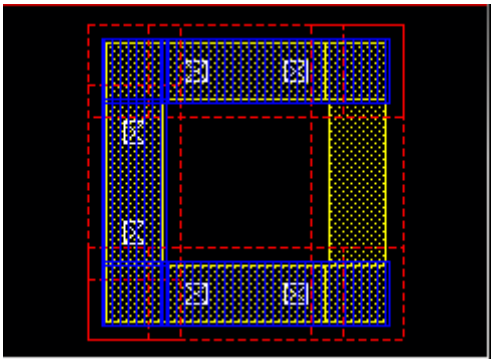
LEFT	☐



RIGHT	☑

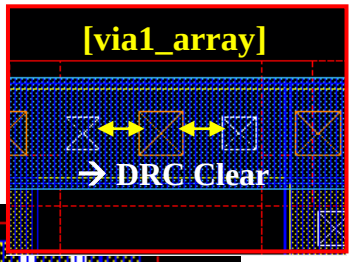


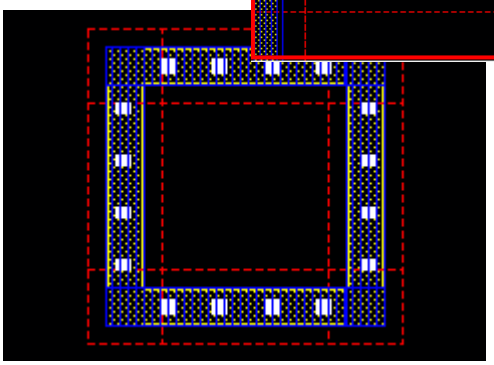
RIGHT	☐



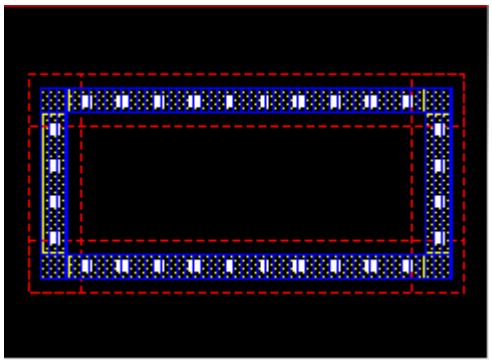
4.26 ptap_ring_ndiode

Parameter	Default	Change
x_size	17	*value*
y_size	17	*value*
TOP	☑	☐
BOTTOM	☑	☐
LEFT	☑	☐
RIGHT	☑	☐

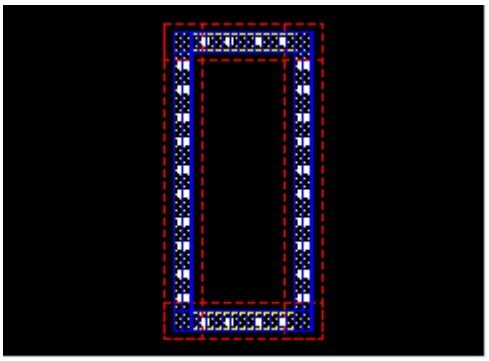




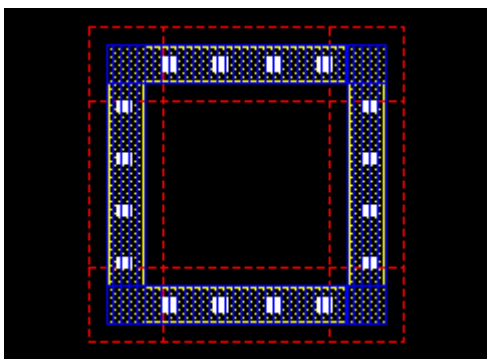
x_size	17	34



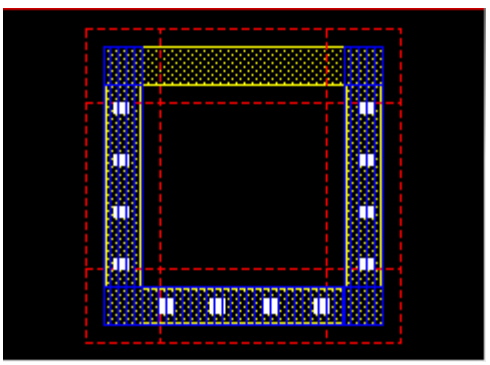
y_size	17	34



TOP	☑

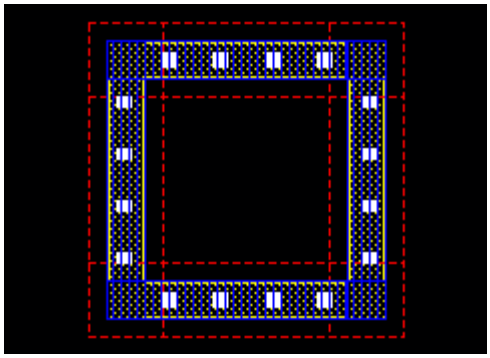


TOP	☐

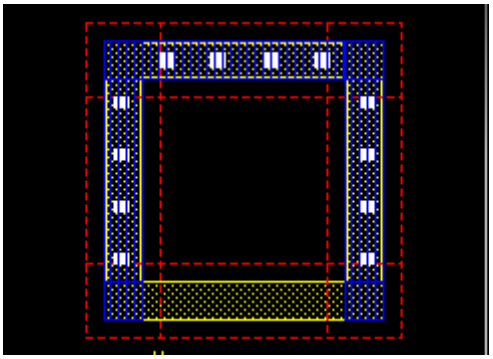


4.26 ptap_ring_ndiode

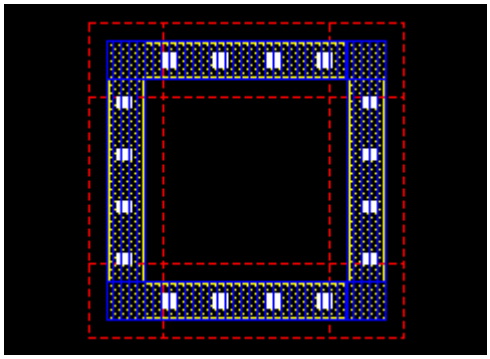
BOTTOM	☑



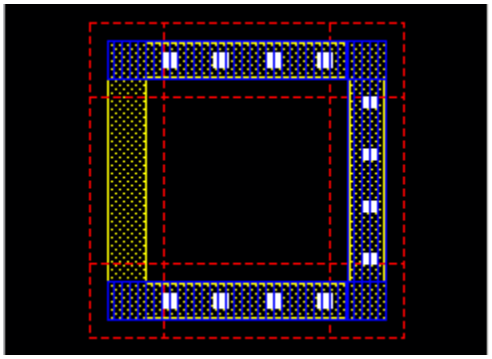
BOTTOM	☐



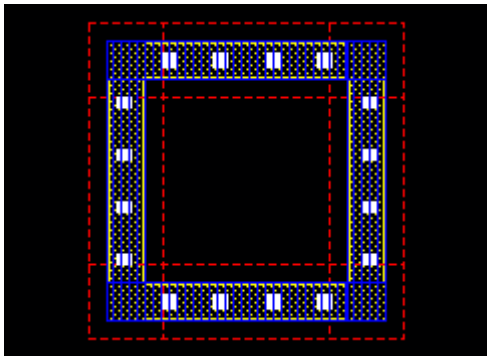
LEFT	☑



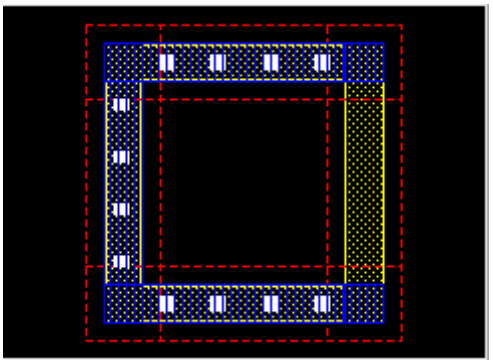
LEFT	☐



RIGHT	☑

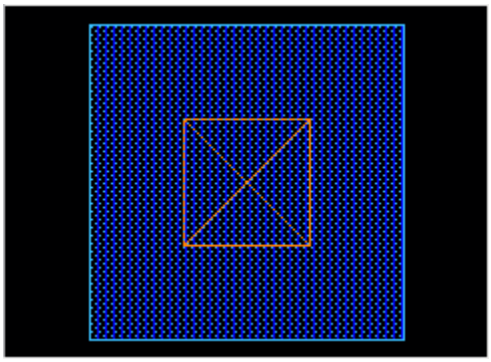


RIGHT	☐

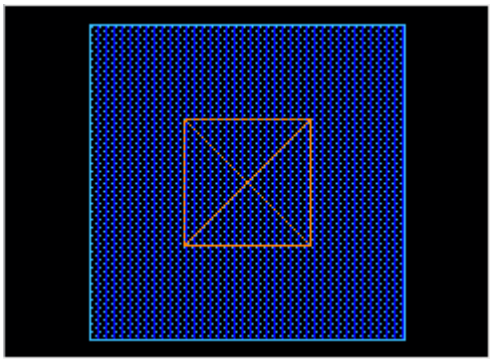


4.27 via1

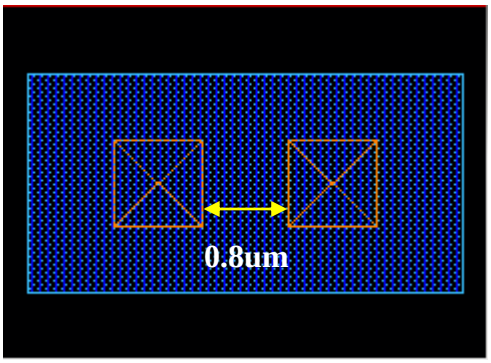
Parameter	Default	Change
x_size	2	*value*
y_size	2	*value*



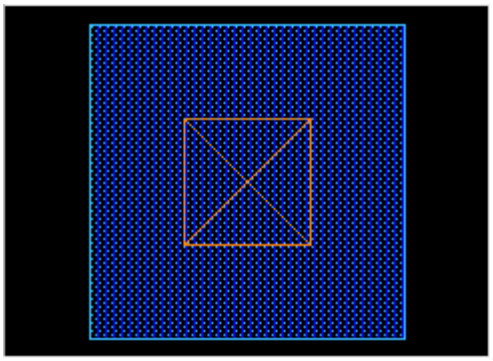
x_size	2



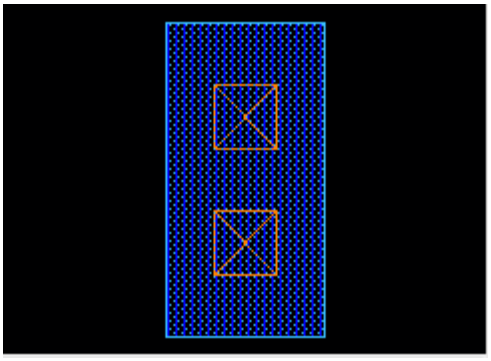
x_size	4



y_size	2

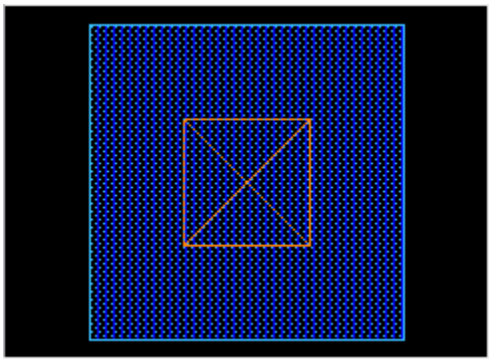


y_size	4

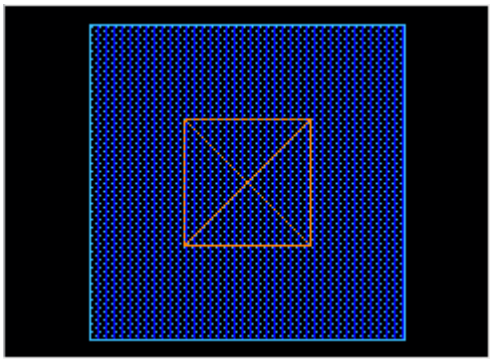


4.28 via1_array

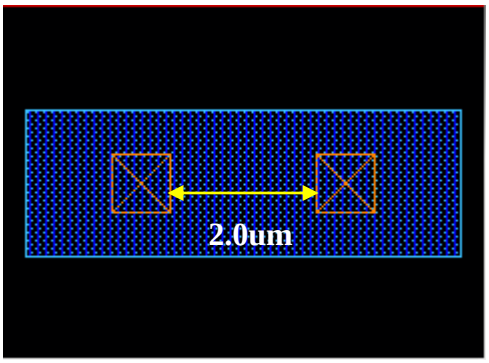
Parameter	Default	Change
x_size	2	*value*
y_size	2	*value*



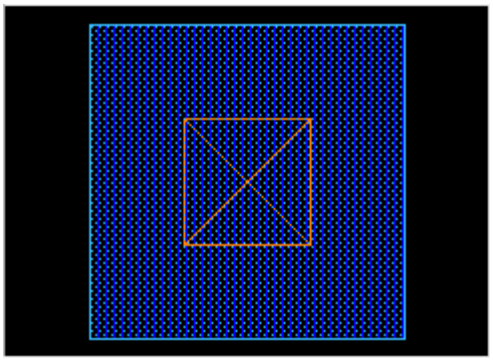
x_size	2



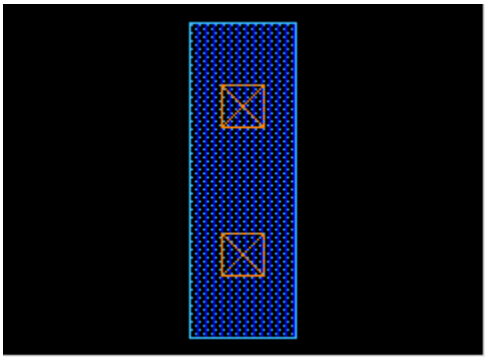
x_size	6



y_size	2

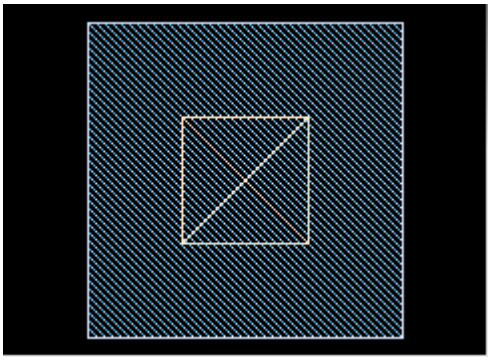


y_size	6

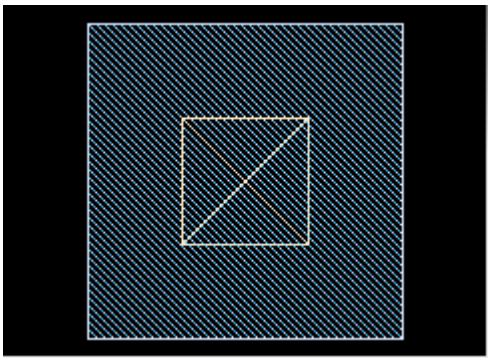


4.29 via2

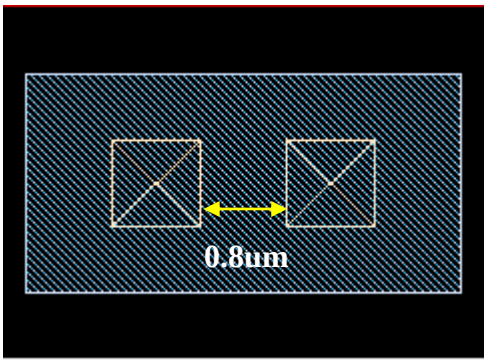
Parameter	Default	Change
x_size	2	*value*
y_size	2	*value*



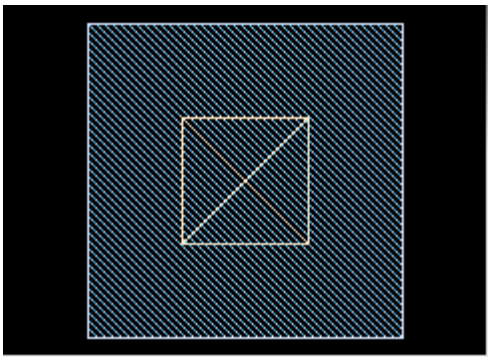
x_size	2



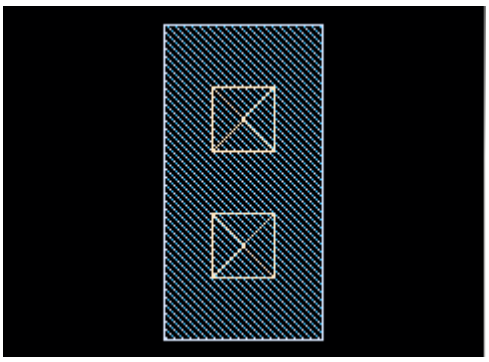
x_size	4



y_size	2

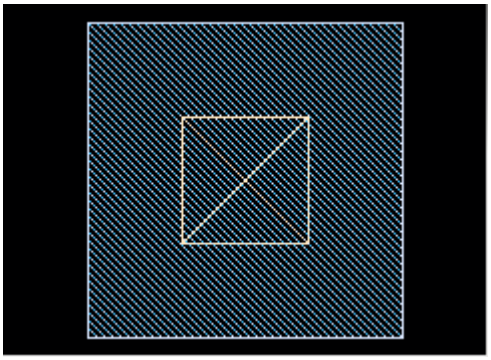


y_size	4

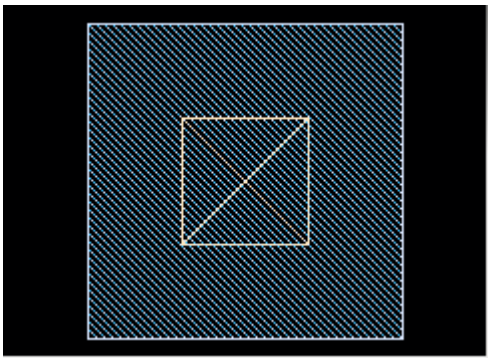


4.30 via2_array

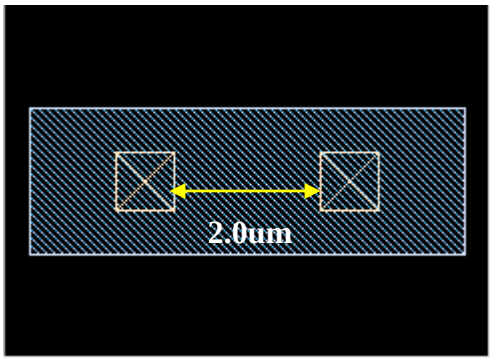
Parameter	Default	Change
x_size	2	*value*
y_size	2	*value*



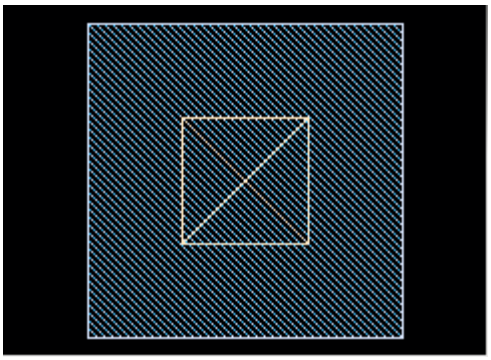
x_size	2



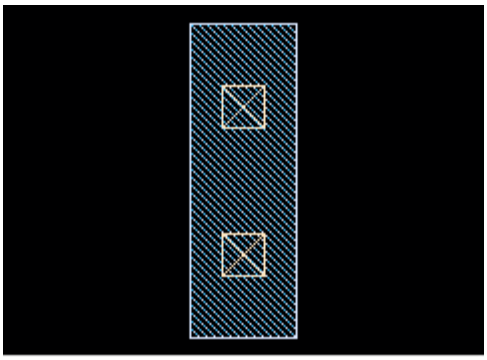
x_size	6



y_size	2



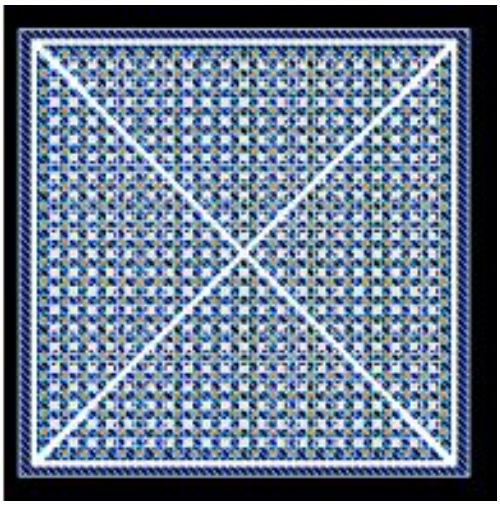
y_size	6



4.31 pad80 / pad100

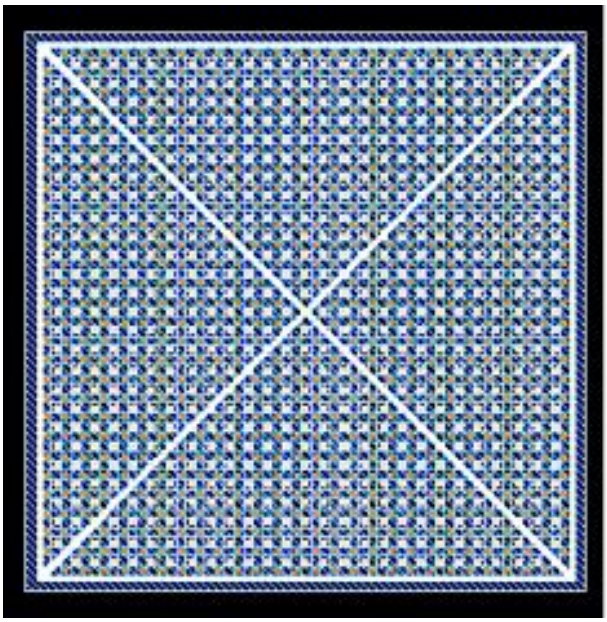
Parameter	Default	Change
-	-	-

pad80



PAD Fixed Size (80um * 80um)
→ doesn't provide parameter modification

pad100

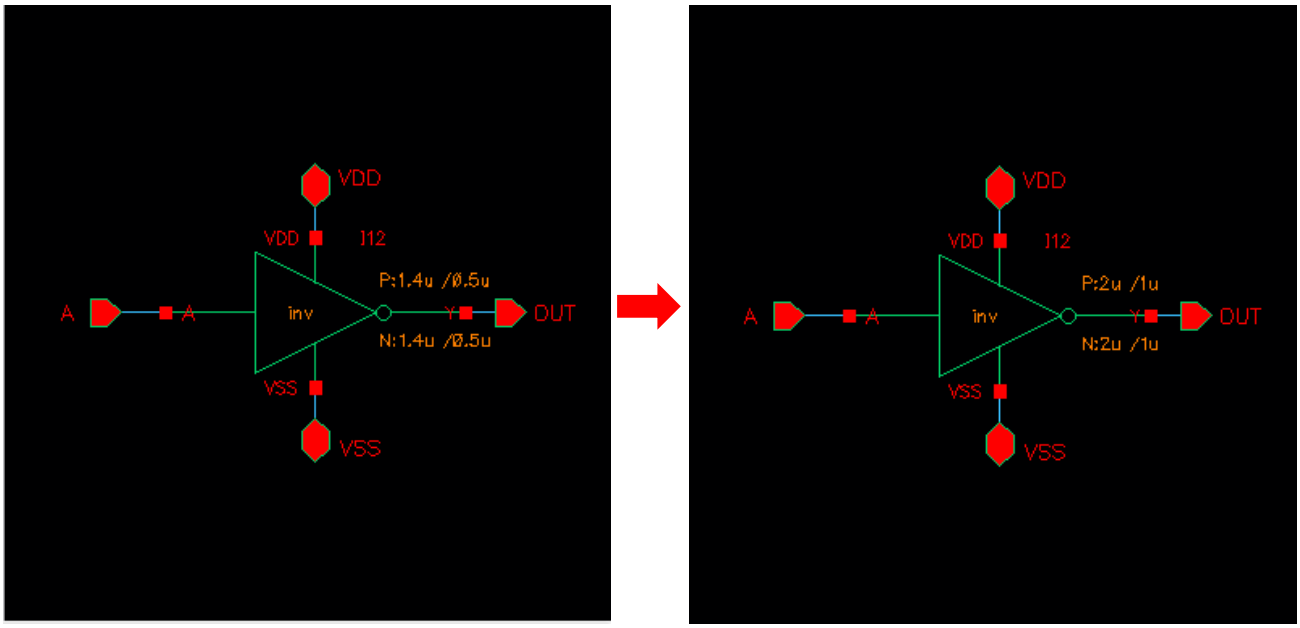


PAD Fixed Size (100um * 100um)
→ doesn't provide parameter modification

5. Standard Schematic Library

5.1 inv

Parameter							
pl		pw		nl		nw	
0.5u	1u	1.4u	2u	0.5u	1u	1.4u	2u



<Schematic parameter>

```
*********************************************************
* Library Name: ETRI_lay
* Cell Name:    inv_schematic
* View Name:    schematic
*********************************************************

.SUBCKT inv_schematic A OUT VDD VSS
*.PININFO A:I OUT:O VDD:B VSS:B
XI12 A VDD VSS OUT / inv pl=0.5u pw=1.4u nl=0.5u nw=1.4u
.ENDS
```

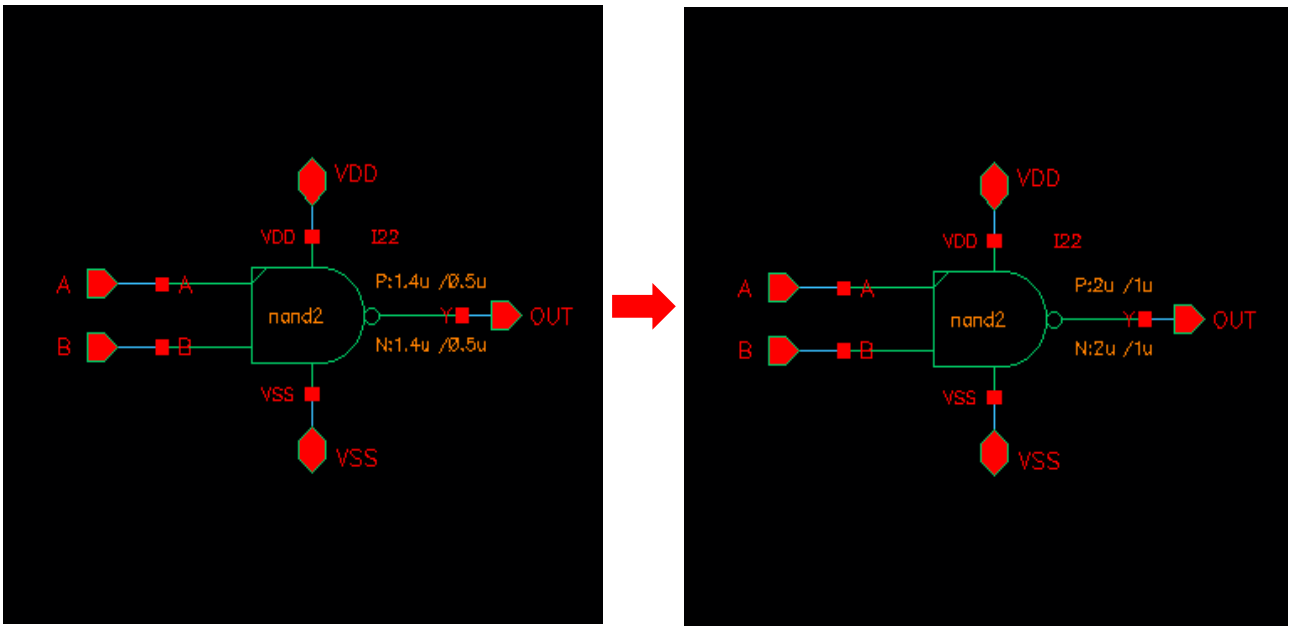
```
*********************************************************
* Library Name: ETRI_lay
* Cell Name:    inv_schematic
* View Name:    schematic
*********************************************************

.SUBCKT inv_schematic A OUT VDD VSS
*.PININFO A:I OUT:O VDD:B VSS:B
XI12 A VDD VSS OUT / inv pl=1u pw=2u nl=1u nw=2u
.ENDS
```

<cdl output>

5.2 nand2

Parameter							
pl		pw		nl		nw	
0.5u	1u	1.4u	2u	0.5u	1u	1.4u	2u



<Schematic parameter>

```
*********************************************************
* Library Name: ETRI_lay
* Cell Name:    nand2_schematic
* View Name:    schematic
*********************************************************

.SUBCKT nand2_schematic A B OUT VDD VSS
*.PININFO A:I B:I OUT:O VDD:B VSS:B
XI22 A B VDD VSS OUT / nand2 nl=0.5u nw=1.4u pl=0.5u pw=1.4u
.ENDS
```

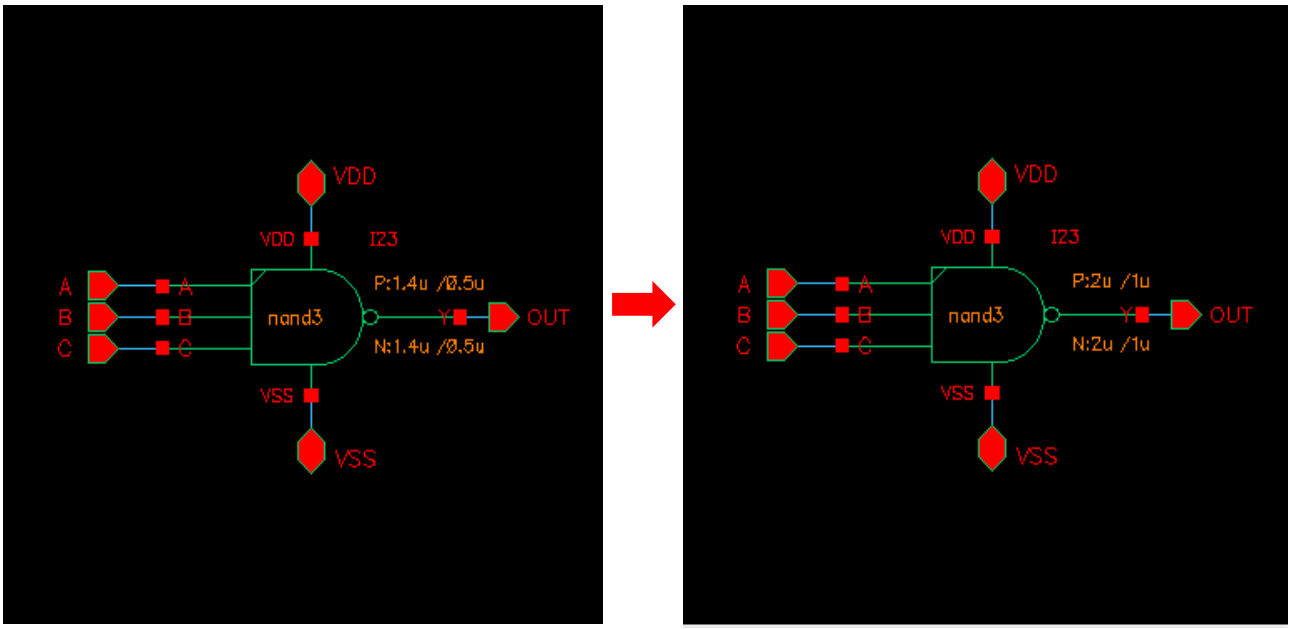
```
*********************************************************
* Library Name: ETRI_lay
* Cell Name:    nand2_schematic
* View Name:    schematic
*********************************************************

.SUBCKT nand2_schematic A B OUT VDD VSS
*.PININFO A:I B:I OUT:O VDD:B VSS:B
XI22 A B VDD VSS OUT / nand2 nl=1u nw=2u pl=1u pw=2u
.ENDS
```

<cdl output>

5.3 nand3

Parameter							
pl		pw		nl		nw	
0.5u	1u	1.4u	2u	0.5u	1u	1.4u	2u



<Schematic parameter>

```
*********************************************************
* Library Name: ETRI_lay
* Cell Name:    nand3_schematic
* View Name:    schematic
*********************************************************

.SUBCKT nand3_schematic A B C OUT VDD VSS
*.PININFO A:I B:I C:I OUT:O VDD:B VSS:B
XI23 A B C VDD VSS OUT / nand3 pl=0.5u pw=1.4u nl=0.5u nw=1.4u
.ENDS
```

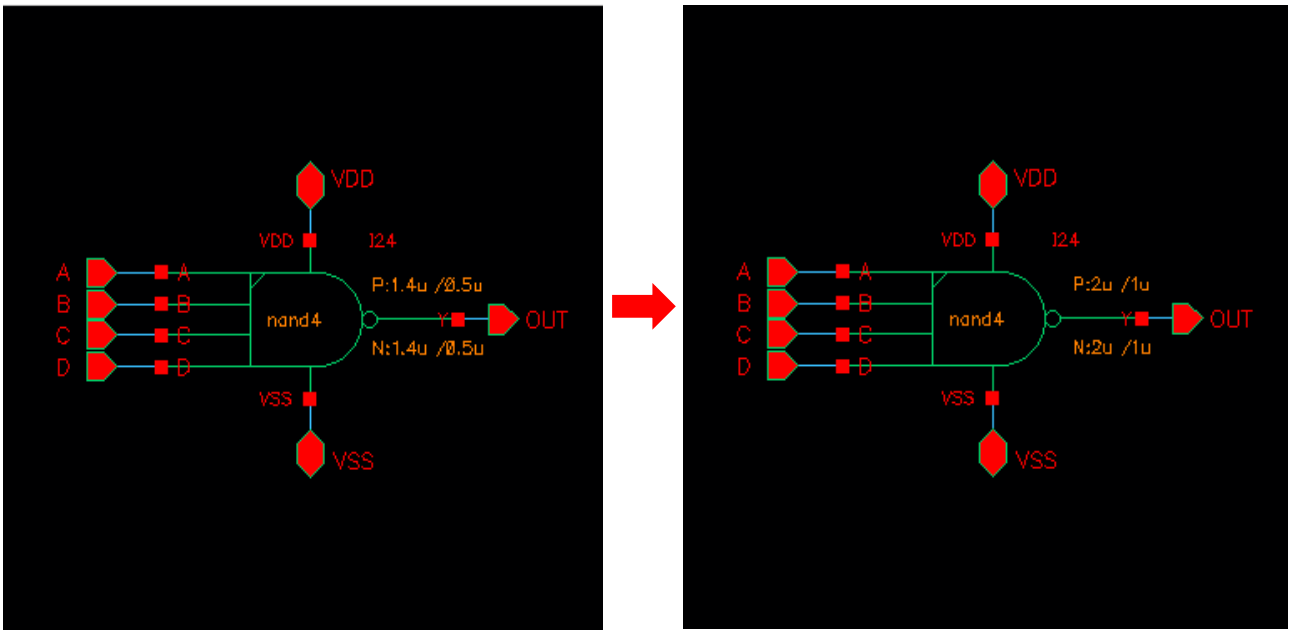
```
*********************************************************
* Library Name: ETRI_lay
* Cell Name:    nand3_schematic
* View Name:    schematic
*********************************************************

.SUBCKT nand3_schematic A B C OUT VDD VSS
*.PININFO A:I B:I C:I OUT:O VDD:B VSS:B
XI23 A B C VDD VSS OUT / nand3 pl=1u pw=2u nl=1u nw=2u
.ENDS
```

<cdl output>

5.4 nand4

Parameter							
pl		pw		nl		nw	
0.5u	1u	1.4u	2u	0.5u	1u	1.4u	2u



<Schematic parameter>

```
********************************************************************************
* Library Name: ETRI_lay
* Cell Name:    nand4_schematic
* View Name:    schematic
********************************************************************************

.SUBCKT nand4_schematic A B C D OUT VDD VSS
*.PININFO A:I B:I C:I D:I OUT:O VDD:B VSS:B
XI25 A B C D VDD VSS OUT / nand4 pl=0.5u pw=1.4u nl=0.5u nw=1.4u
.ENDS
```

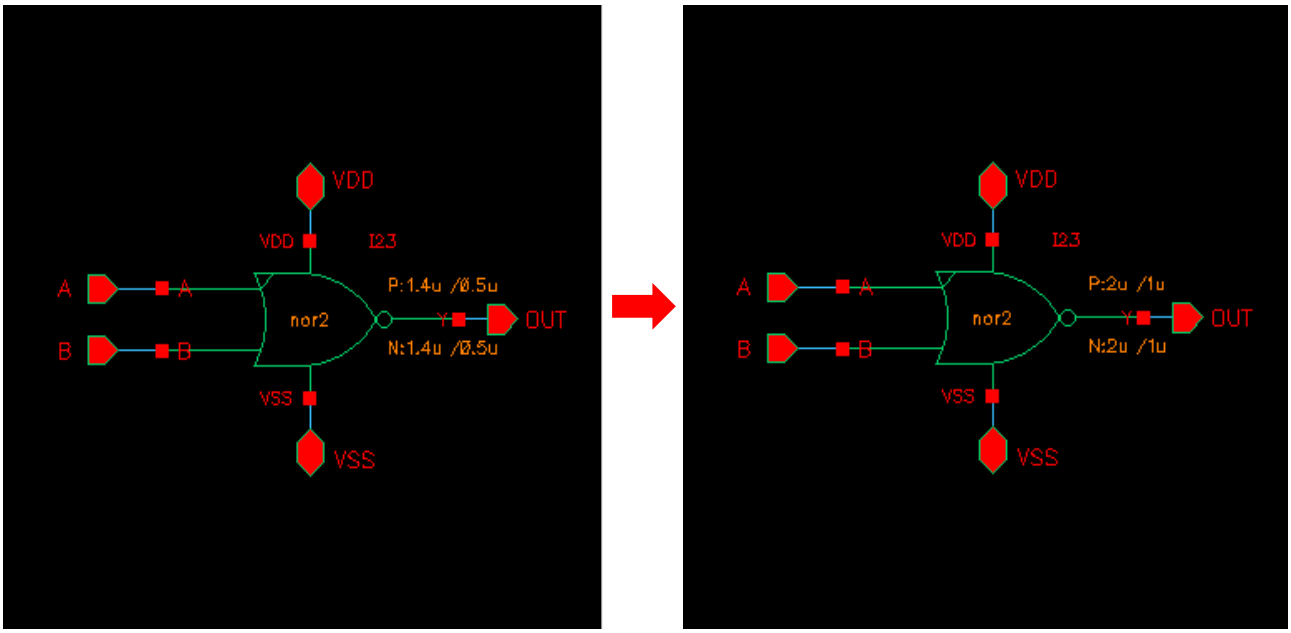
```
********************************************************************************
* Library Name: ETRI_lay
* Cell Name:    nand4_schematic
* View Name:    schematic
********************************************************************************

.SUBCKT nand4_schematic A B C D OUT VDD VSS
*.PININFO A:I B:I C:I D:I OUT:O VDD:B VSS:B
XI24 A B C D VDD VSS OUT / nand4 pl=1u pw=2u nl=1u nw=2u
.ENDS
```

<cdl output>

5.5 nor2

Parameter							
pl		pw		nl		nw	
0.5u	1u	1.4u	2u	0.5u	1u	1.4u	2u



<Schematic parameter>

```
********************************************************************************
* Library Name: ETRI_lay
* Cell Name:    nor2_schematic
* View Name:    schematic
********************************************************************************

.SUBCKT nor2_schematic A B OUT VDD VSS
*.PININFO A:I B:I OUT:O VDD:B VSS:B
XI23 A B VDD VSS OUT / nor2 pl=0.5u pw=1.4u nl=0.5u nw=1.4u
.ENDS
```

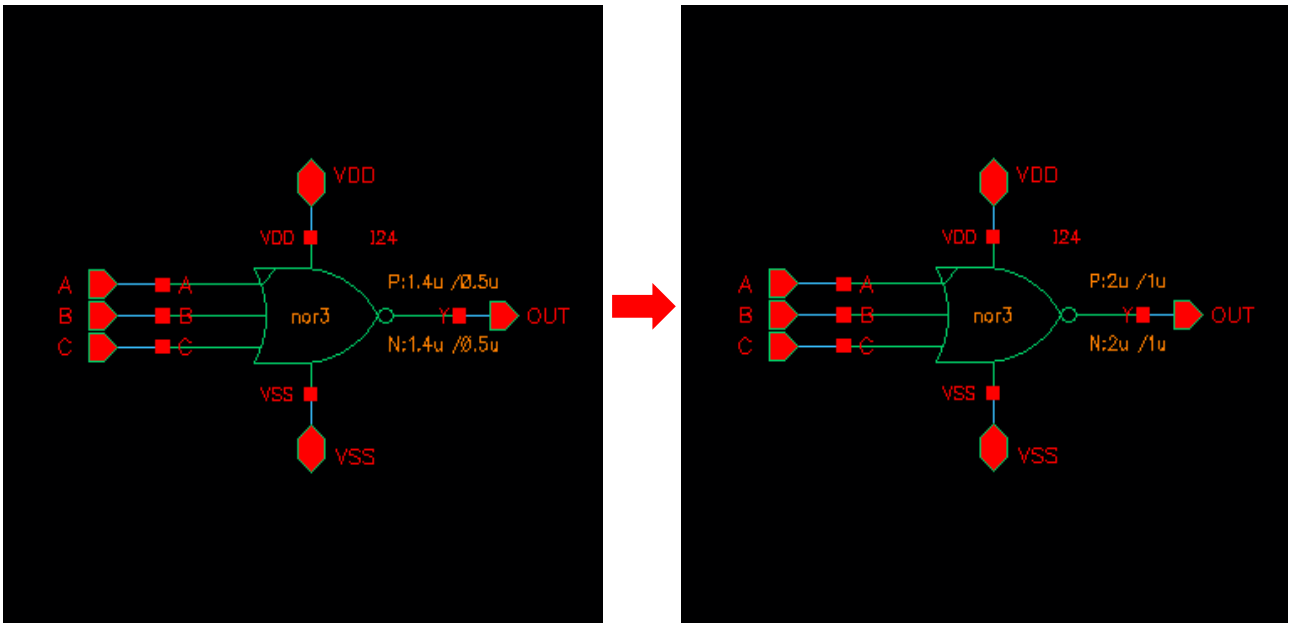
```
********************************************************************************
* Library Name: ETRI_lay
* Cell Name:    nor2_schematic
* View Name:    schematic
********************************************************************************

.SUBCKT nor2_schematic A B OUT VDD VSS
*.PININFO A:I B:I OUT:O VDD:B VSS:B
XI23 A B VDD VSS OUT / nor2 pl=1u pw=2u nl=1u nw=2u
.ENDS
```

<cdl output>

5.6 nor3

Parameter							
pl		pw		nl		nw	
0.5u	1u	1.4u	2u	0.5u	1u	1.4u	2u



<Schematic parameter>

```
*********************************************************
* Library Name: ETRI_lay
* Cell Name:    nor3_schematic
* View Name:    schematic
*********************************************************

.SUBCKT nor3_schematic A B C OUT VDD VSS
*.PININFO A:I B:I C:I OUT:O VDD:B VSS:B
XI24 A B C VDD VSS OUT / nor3 pl=0.5u pw=1.4u nl=0.5u nw=1.4u
.ENDS
```

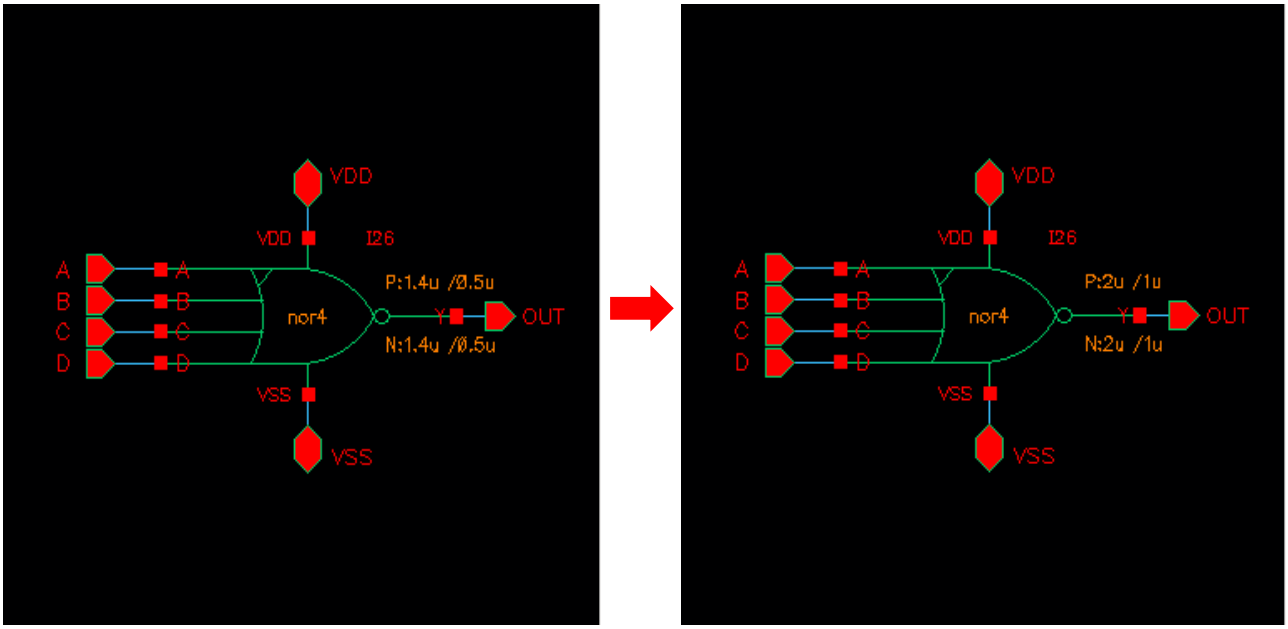
```
*********************************************************
* Library Name: ETRI_lay
* Cell Name:    nor3_schematic
* View Name:    schematic
*********************************************************

.SUBCKT nor3_schematic A B C OUT VDD VSS
*.PININFO A:I B:I C:I OUT:O VDD:B VSS:B
XI24 A B C VDD VSS OUT / nor3 pl=1u pw=2u nl=1u nw=2u
.ENDS
```

<cdl output>

5.7 nor4

Parameter							
pl		pw		nl		nw	
0.5u	1u	1.4u	2u	0.5u	1u	1.4u	2u



<Schematic parameter>

```
*********************************************************************
* Library Name: ETRI_lay
* Cell Name:    nor4_schematic
* View Name:    schematic
*********************************************************************

.SUBCKT nor4_schematic A B C D OUT VDD VSS
*.PININFO A:I B:I C:I D:I OUT:O VDD:B VSS:B
XI26 A B C D VDD VSS OUT / nor4 pl=0.5u pw=1.4u nl=0.5u nw=1.4u
.ENDS
```

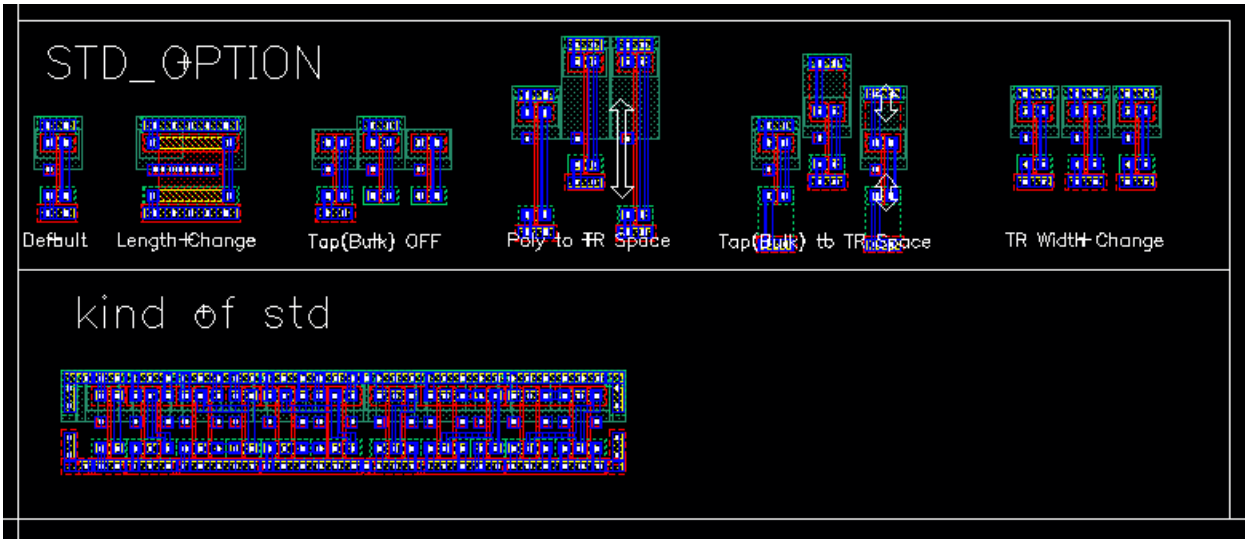
```
*********************************************************************
* Library Name: ETRI_lay
* Cell Name:    nor4_schematic
* View Name:    schematic
*********************************************************************

.SUBCKT nor4_schematic A B C D OUT VDD VSS
*.PININFO A:I B:I C:I D:I OUT:O VDD:B VSS:B
XI26 A B C D VDD VSS OUT / nor4 pl=1u pw=2u nl=1u nw=2u
.ENDS
```

<cdl output>

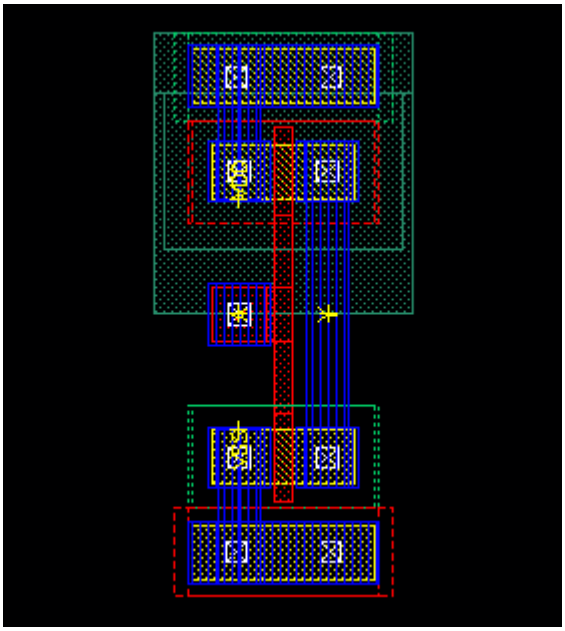
6. Standard Layout Library

6.1 .SAMPLE

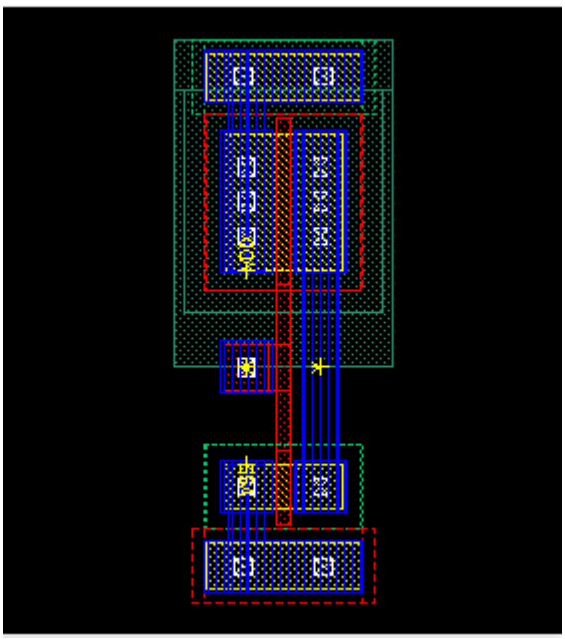


6.2 inv

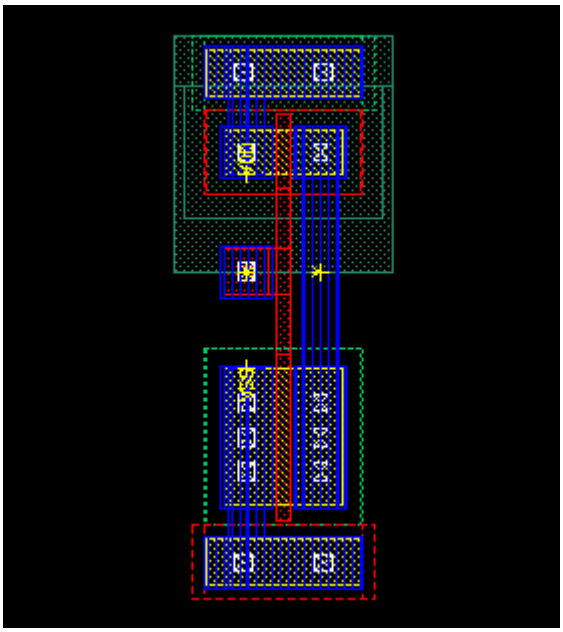
Parameter	Default	Change
P_WIDTH	1.6	*value*
N_WIDTH	1.6	*value*
LENGTH	0.5	*value*
POLY_TO_PTR_SPACE	2.6	*value*
POLY_TO_NTR_SPACE	2.6	*value*
PTAP_TO_TR_SPACE	0	*value*
NTAP_TO_TR_SPACE	0	*value*
PTAP	☑	☐
NTAP	☑	☐
POLY1CONT	☑	☐



P_WIDTH	1.6	4.8

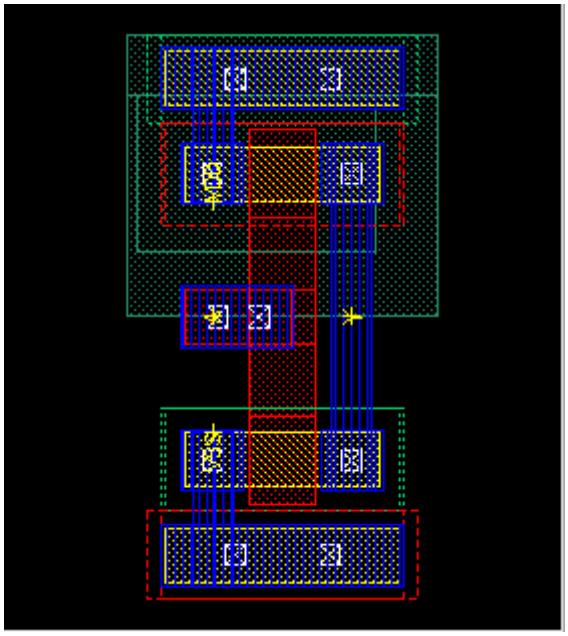


N_WIDTH	1.6	4.8

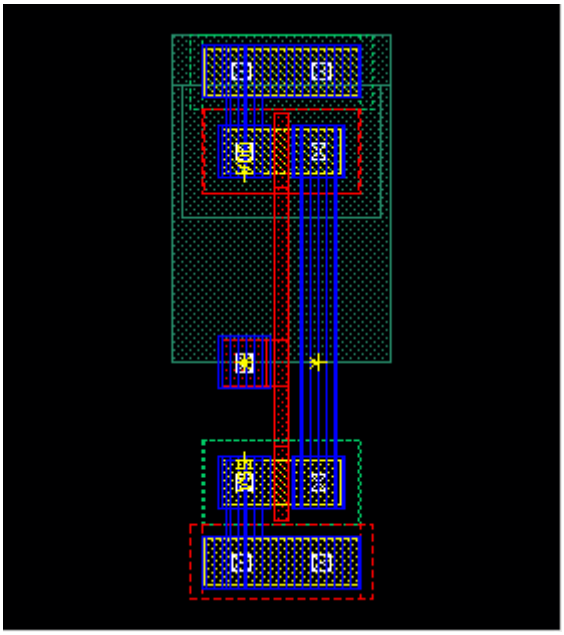


6.2 inv

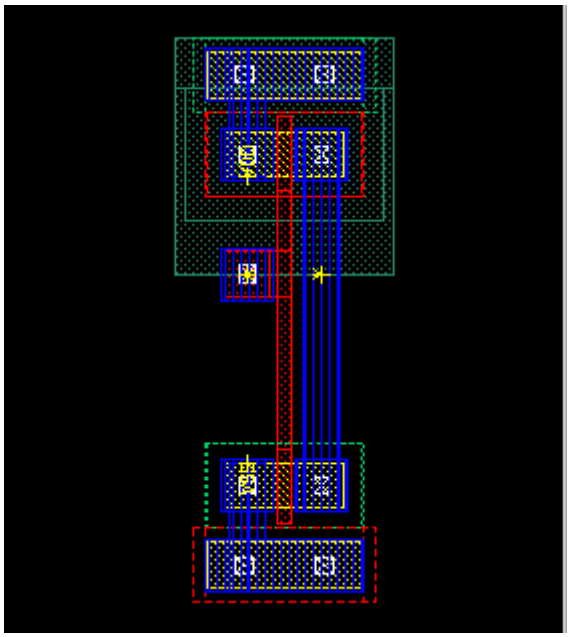
LENGTH	0.5	2



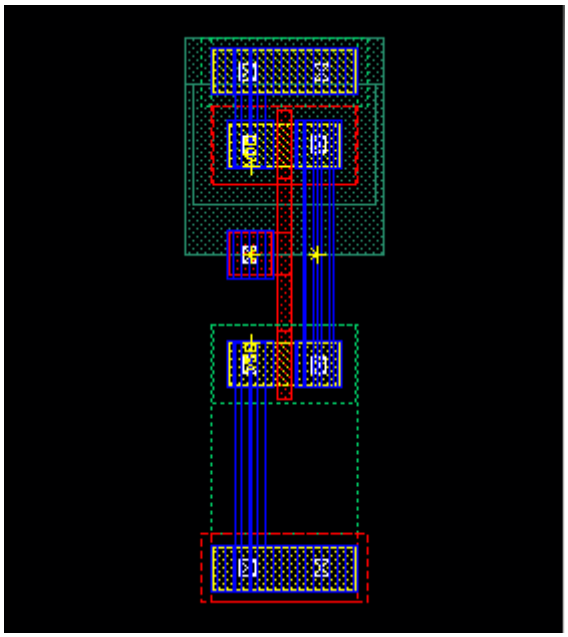
POLY_TO_PTR_SPACE	2.6	5.2



POLY_TO_NTR_SPACE	2.6	5.2

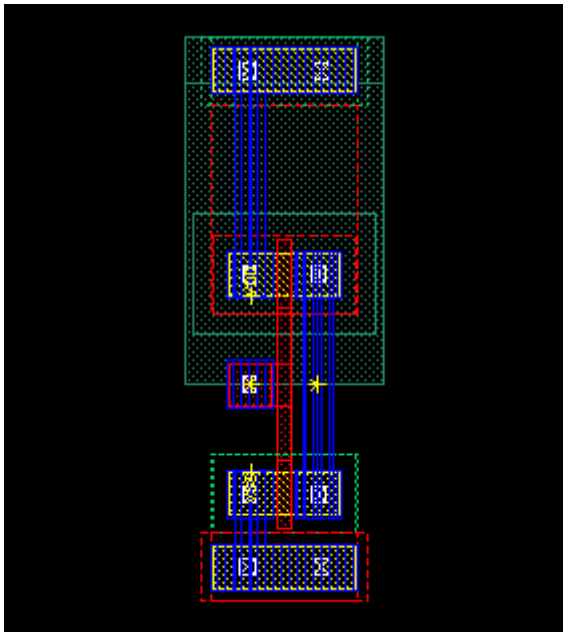


PTAP_TO_TR_SPACE	0	5.0

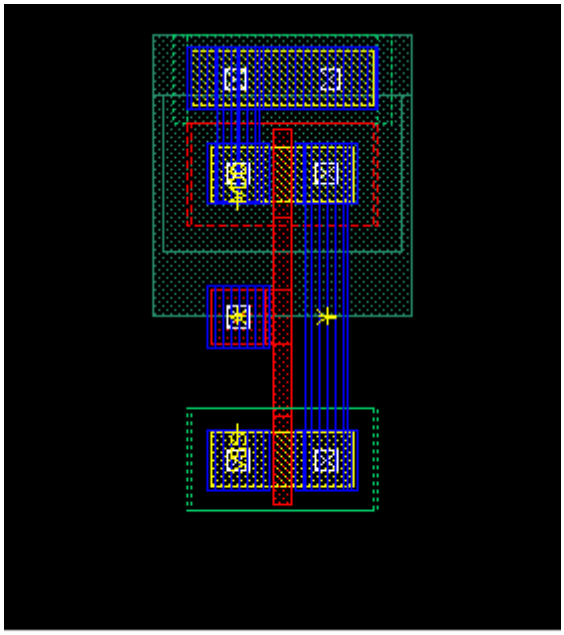


6.2 inv

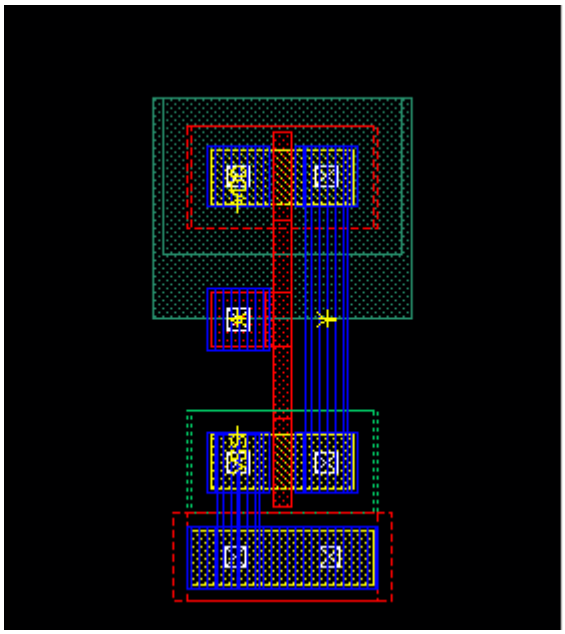
NTAP_TO_TR_SPACE	0	5



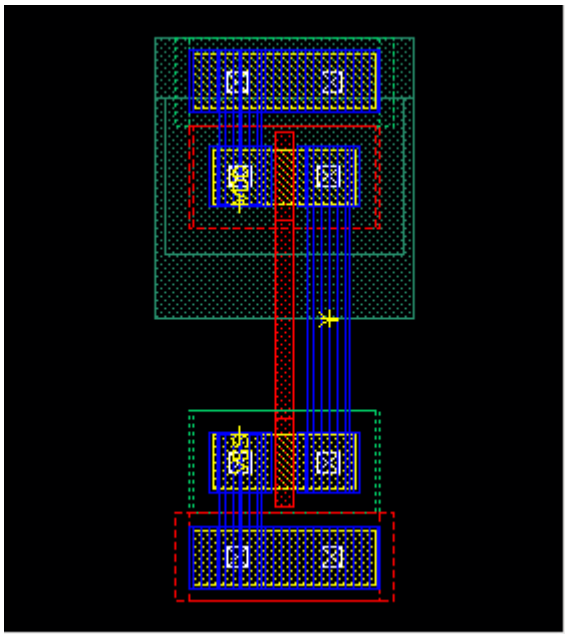
PTAP	☑ → ☐



NTAP	☑ → ☐

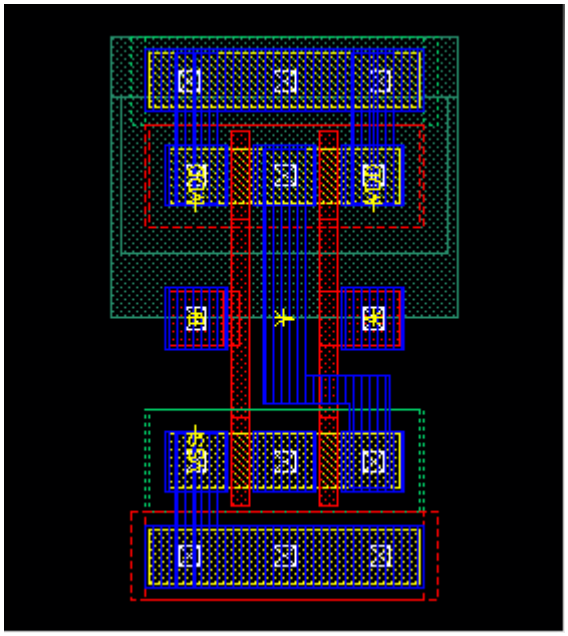


POLY1CONT	☑ → ☐

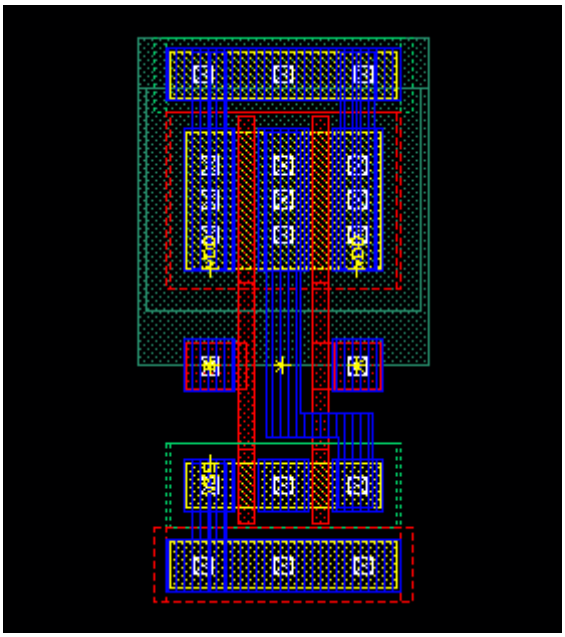


6.3 nand2

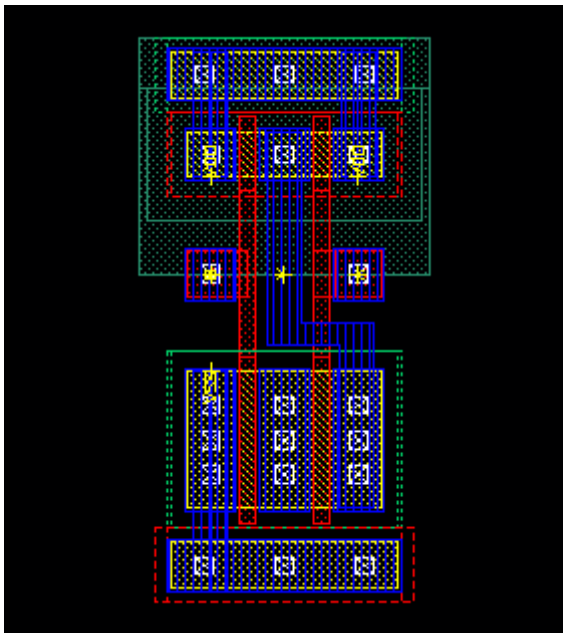
Parameter	Default	Change
P_WIDTH	1.6	*value*
N_WIDTH	1.6	*value*
LENGTH	0.5	*value*
POLY_TO_PTR_SPACE	2.6	*value*
POLY_TO_NTR_SPACE	2.6	*value*
PTAP_TO_TR_SPACE	0	*value*
NTAP_TO_TR_SPACE	0	*value*
PTAP	☑	☐
NTAP	☑	☐
POLY1CONTA	☑	☐
POLY1CONTB	☑	☐



P_WIDTH	1.6	4.8

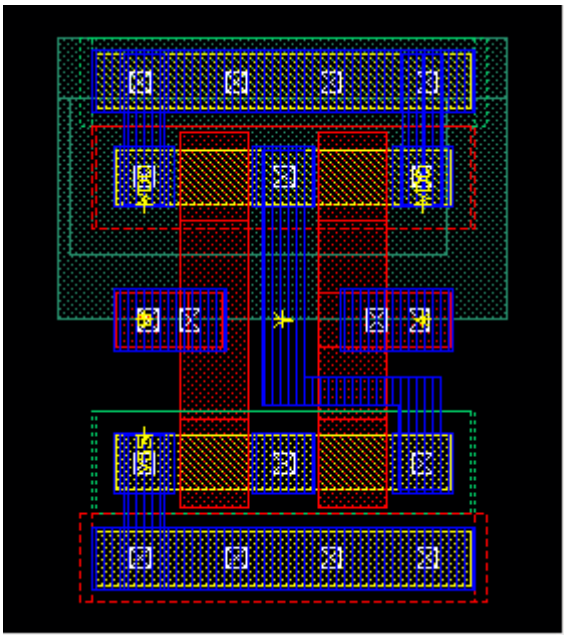


N_WIDTH	1.6	4.8

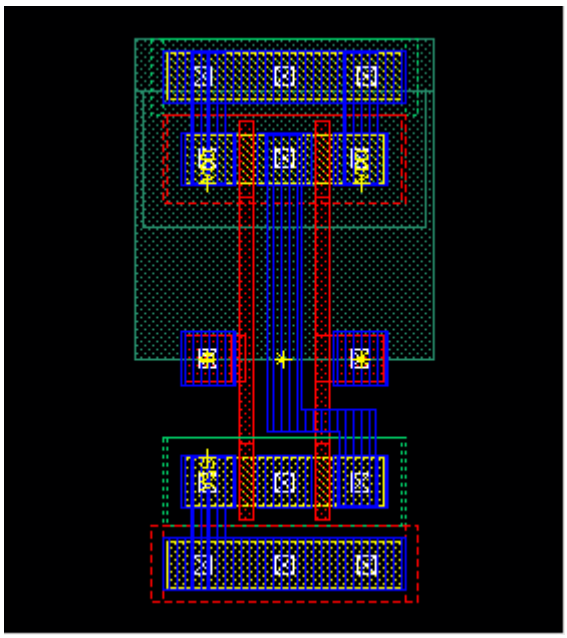


6.3 nand2

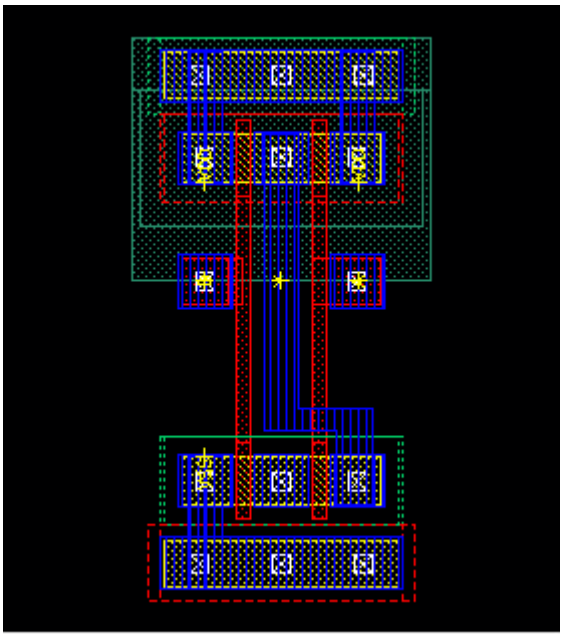
LENGTH	0.5	2



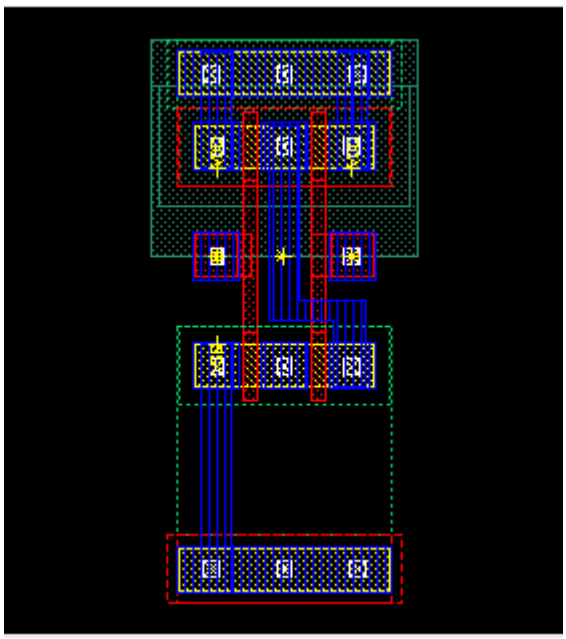
POLY_TO_PTR_SPACE	2.6	5.2



POLY_TO_NTR_SPACE	2.6	5.2

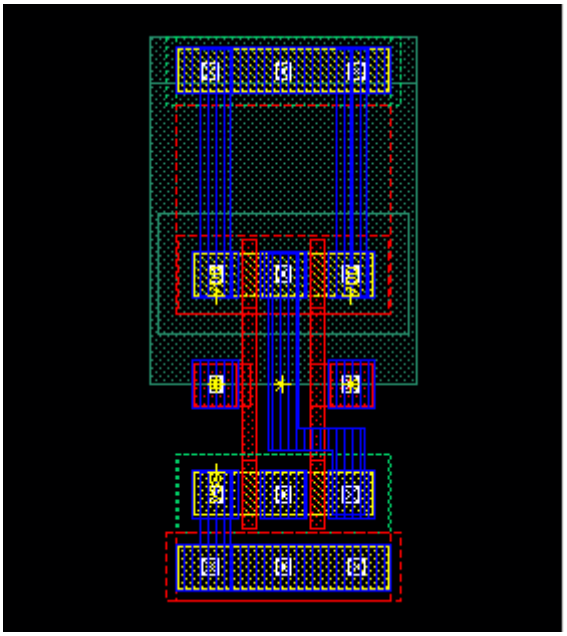


PTAP_TO_TR_SPACE	0	5.0

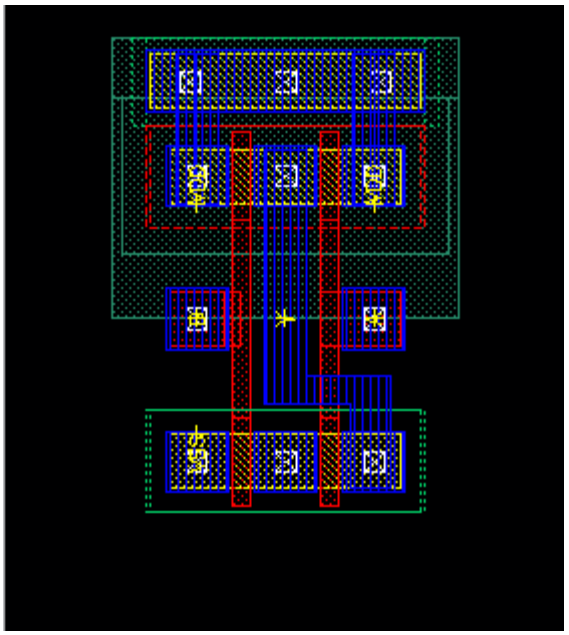


6.3 nand2

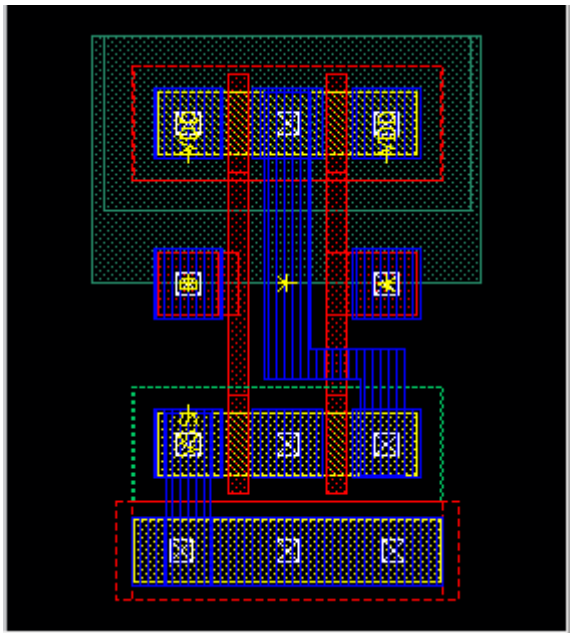
NTAP_TO_TR_SPACE	0	5



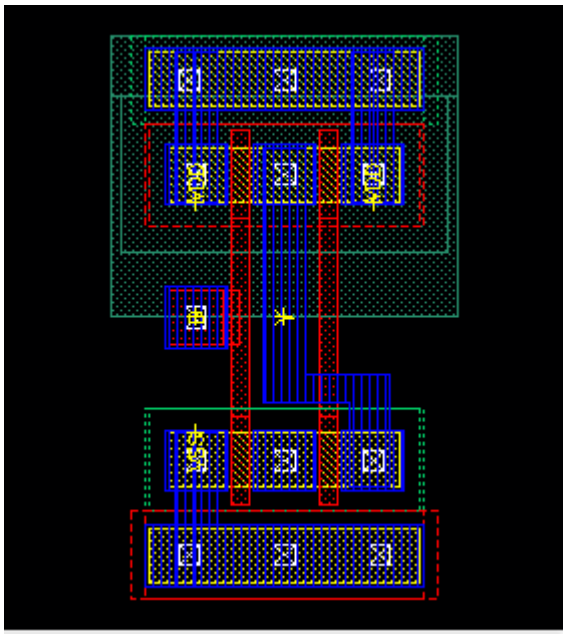
PTAP	☑ → ☐



NTAP	☑ → ☐

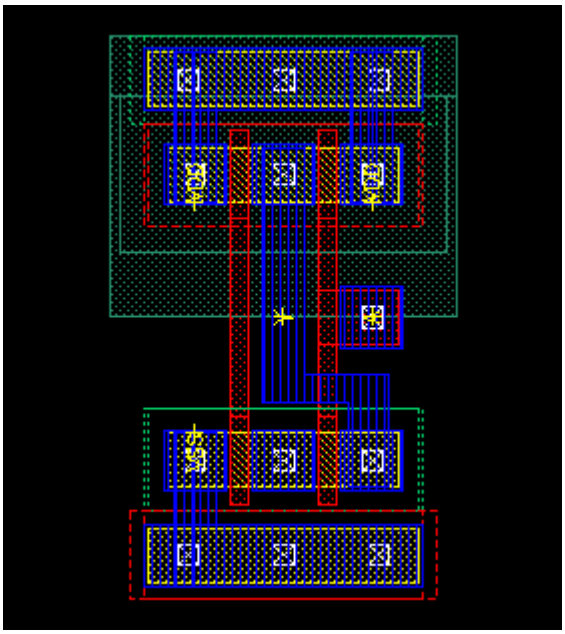


POLY1CONTA	☑ → ☐



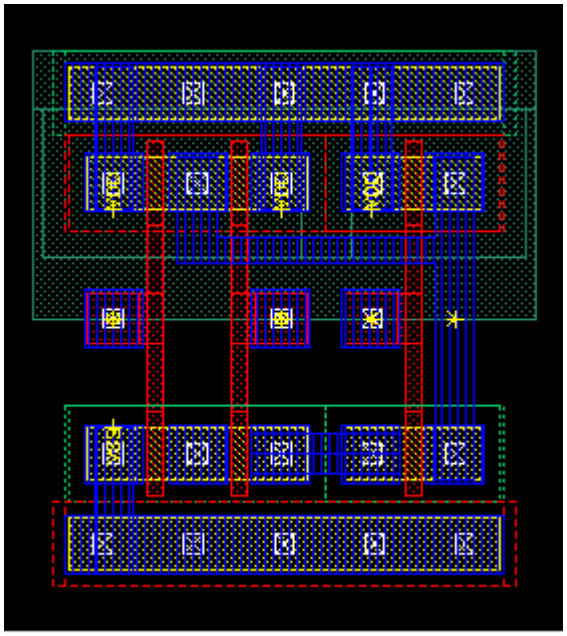
6.3 nand2

POLY1CONTB	☑ → ☐

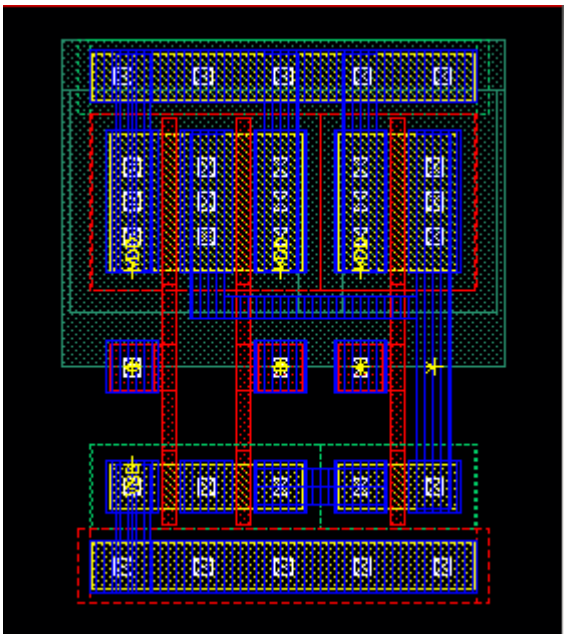


6.4 nand3

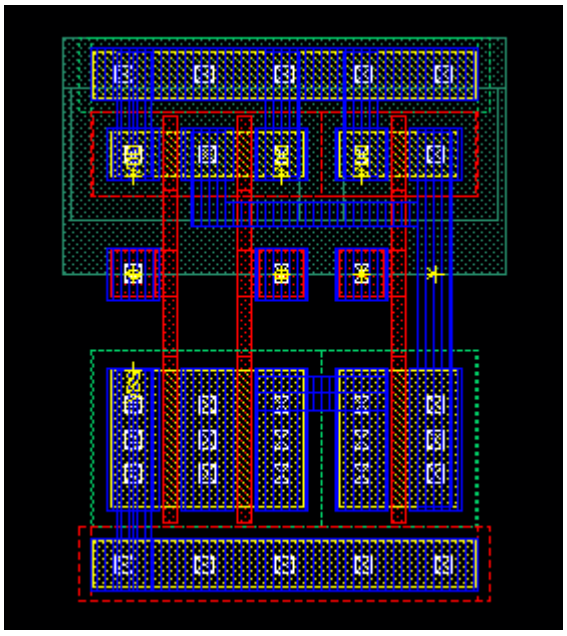
Parameter	Default	Change
P_WIDTH	1.6	*value*
N_WIDTH	1.6	*value*
LENGTH	0.5	*value*
POLY_TO_PTR_SPACE	2.6	*value*
POLY_TO_NTR_SPACE	2.6	*value*
PTAP_TO_TR_SPACE	0	*value*
NTAP_TO_TR_SPACE	0	*value*
PTAP	☑	☐
NTAP	☑	☐
POLY1CONTA	☑	☐
POLY1CONTB	☑	☐
POLY1CONTC	☑	☐



P_WIDTH	1.6	4.8

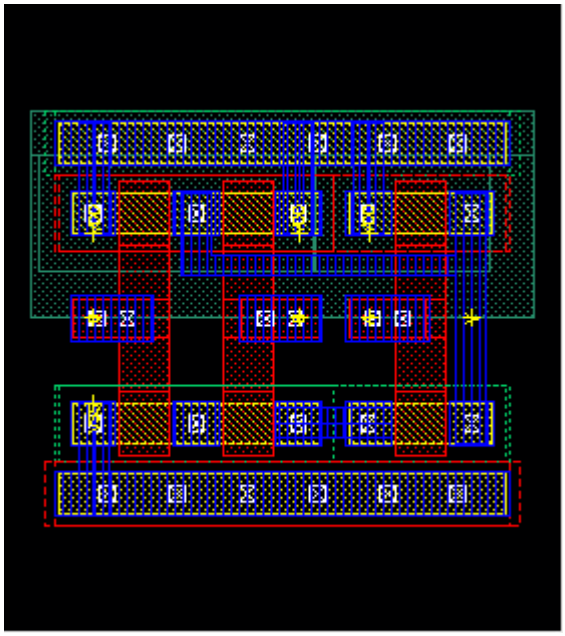


N_WIDTH	1.6	4.8

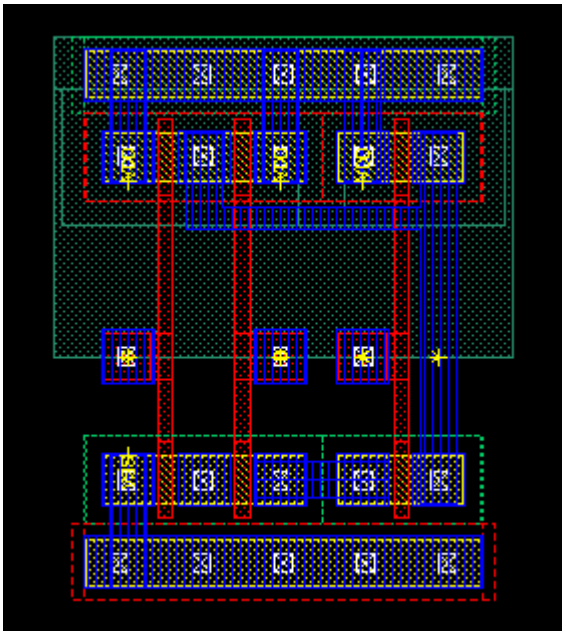


6.4 nand3

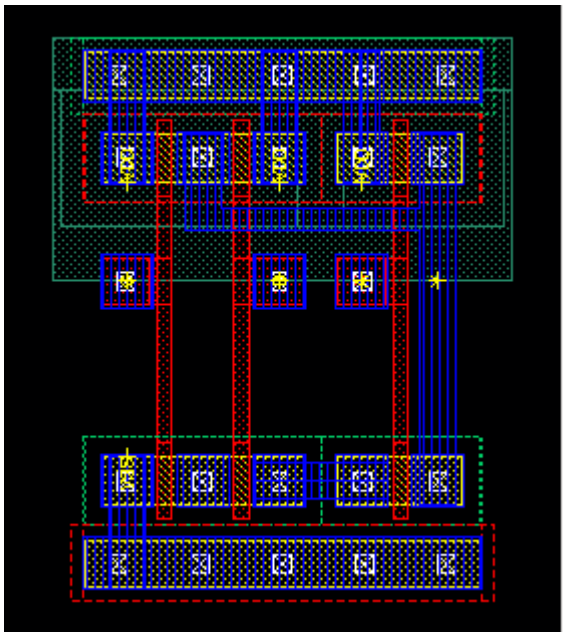
LENGTH	0.5	2



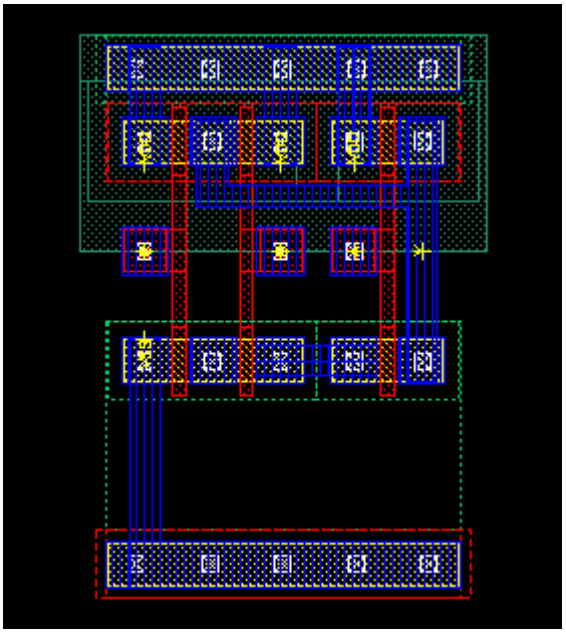
POLY_TO_PTR_SPACE	2.6	5.2



POLY_TO_NTR_SPACE	2.6	5.2

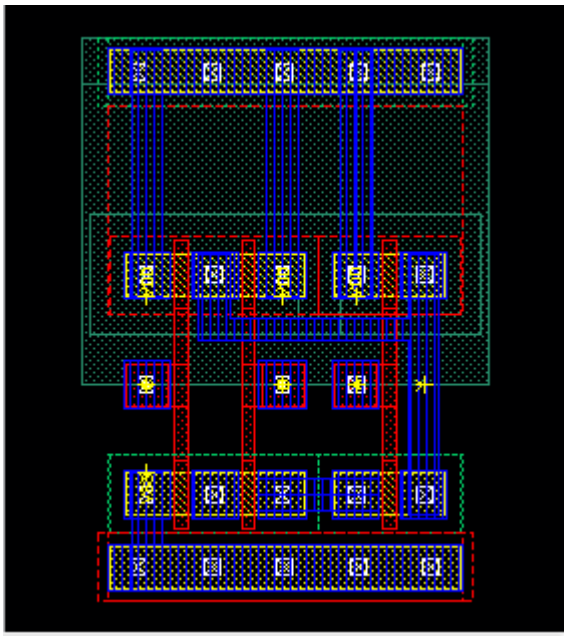


PTAP_TO_TR_SPACE	0	5.0

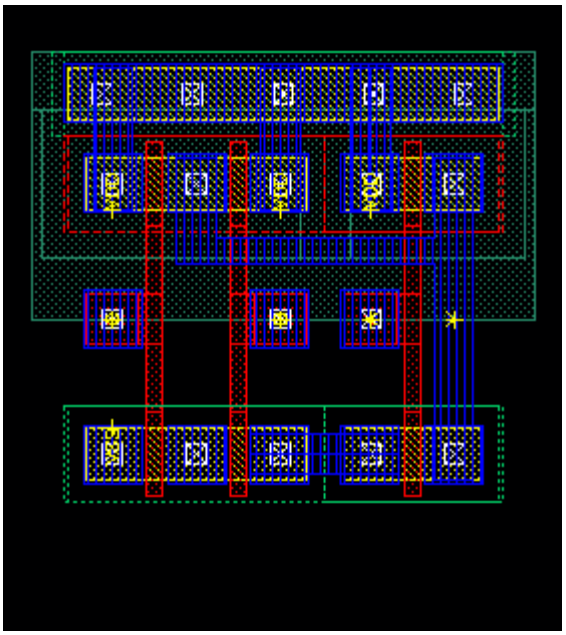


6.4 nand3

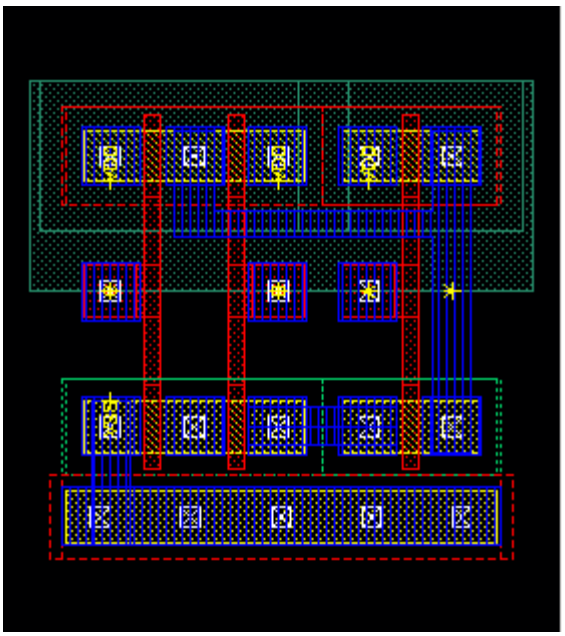
NTAP_TO_TR_SPACE	0	5



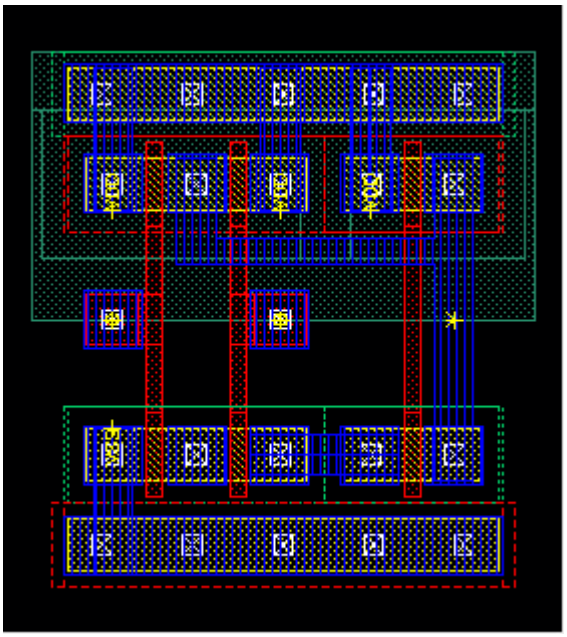
PTAP	☑ → ☐



NTAP	☑ → ☐

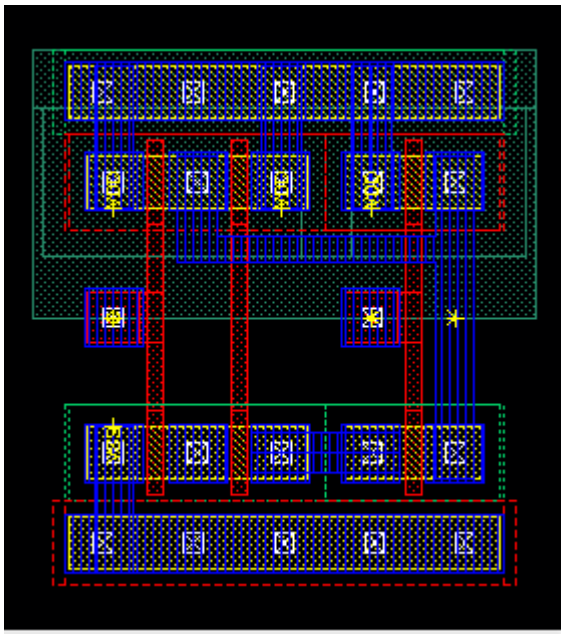


POLY1CONTA	☑ → ☐

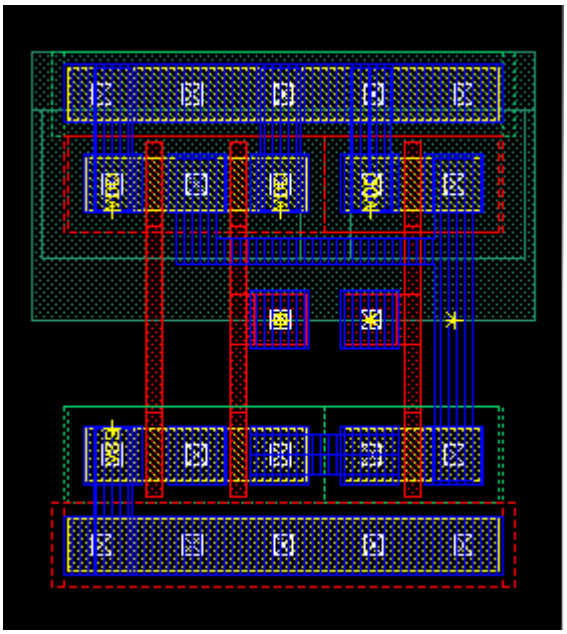


6.4 nand3

POLY1CONTB	☑ → ☐

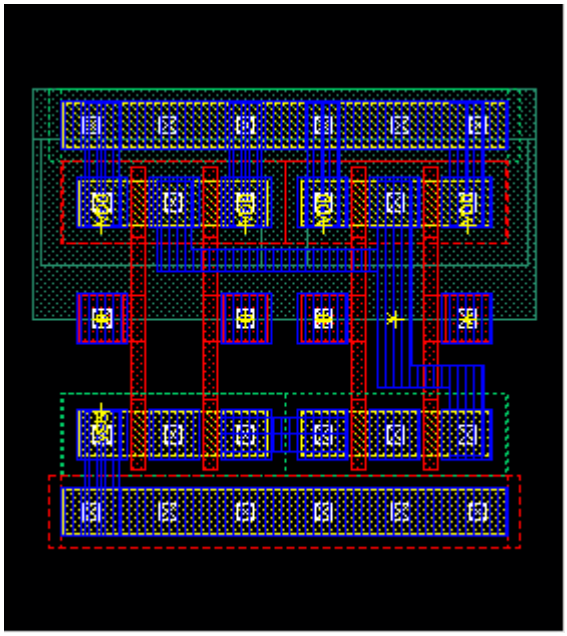


POLY1CONTC	☑ → ☐

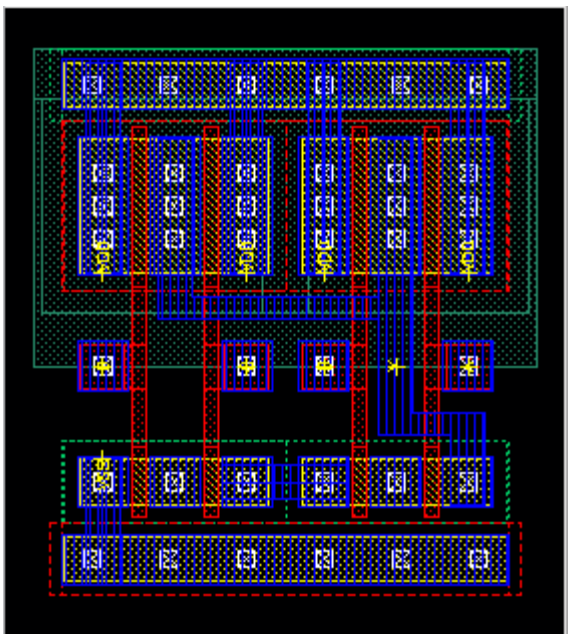


6.5 nand4

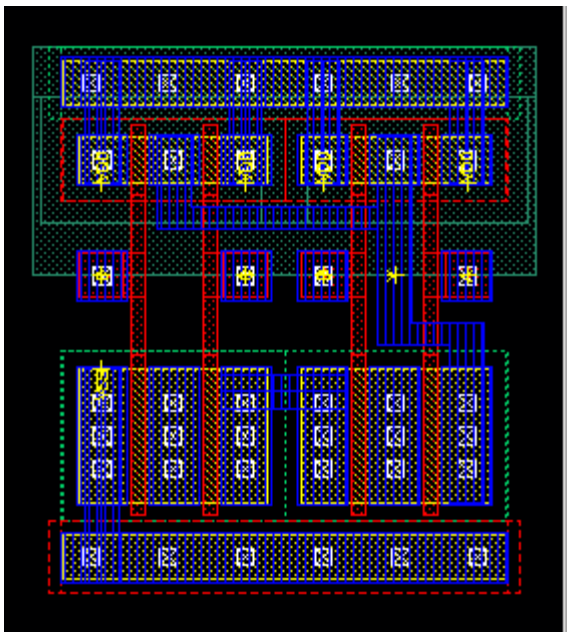
Parameter	Default	Change
P_WIDTH	1.6	*value*
N_WIDTH	1.6	*value*
LENGTH	0.5	*value*
POLY_TO_PTR_SPACE	2.6	*value*
POLY_TO_NTR_SPACE	2.6	*value*
PTAP_TO_TR_SPACE	0	*value*
NTAP_TO_TR_SPACE	0	*value*
PTAP	☑	☐
NTAP	☑	☐
POLY1CONTA	☑	☐
POLY1CONTB	☑	☐
POLY1CONTC	☑	☐
POLY1CONTD	☑	☐



P_WIDTH	1.6	4.8

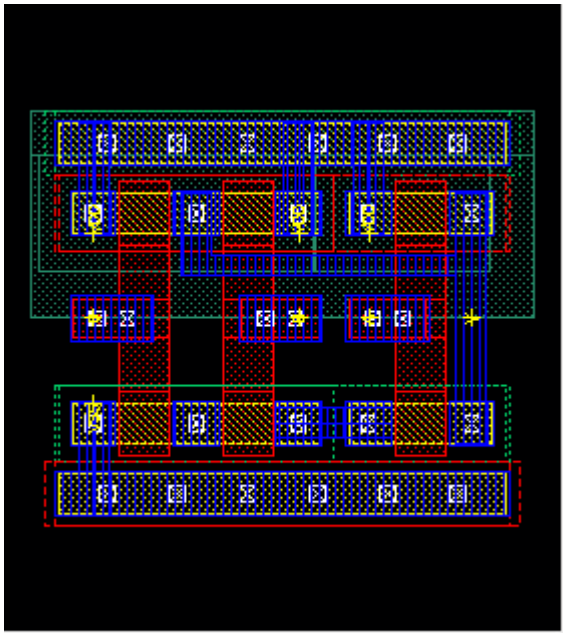


N_WIDTH	1.6	4.8

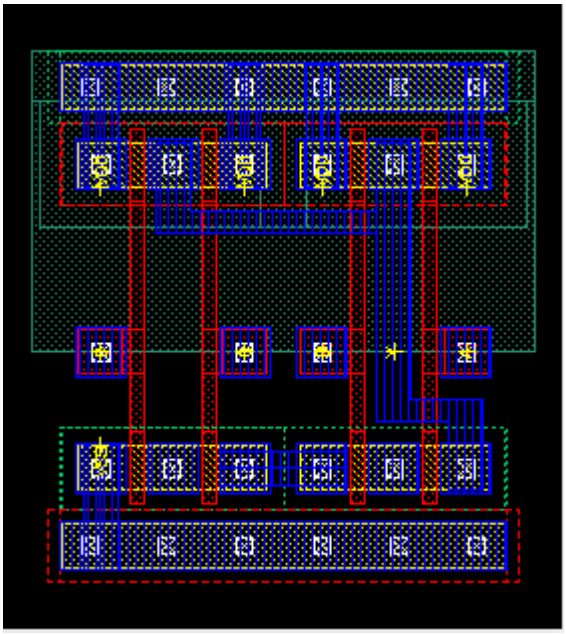


6.5 nand4

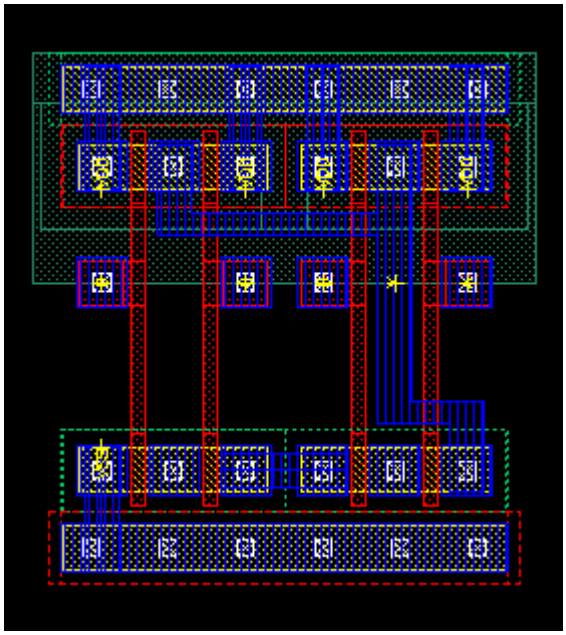
LENGTH	0.5	2



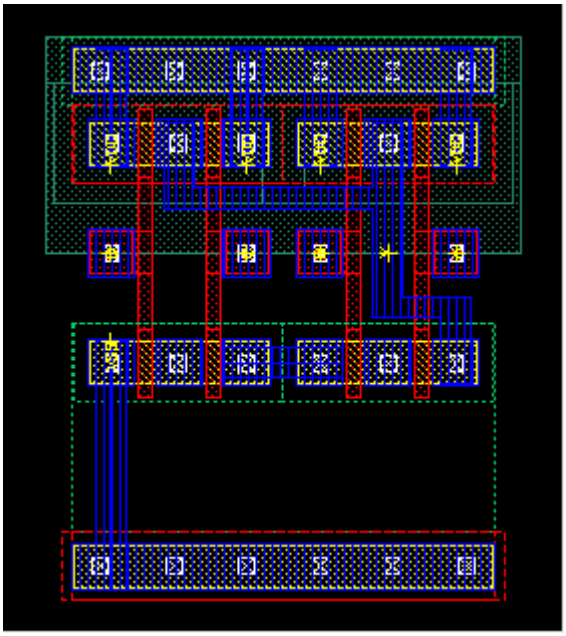
POLY_TO_PTR_SPACE	2.6	5.2



POLY_TO_NTR_SPACE	2.6	5.2

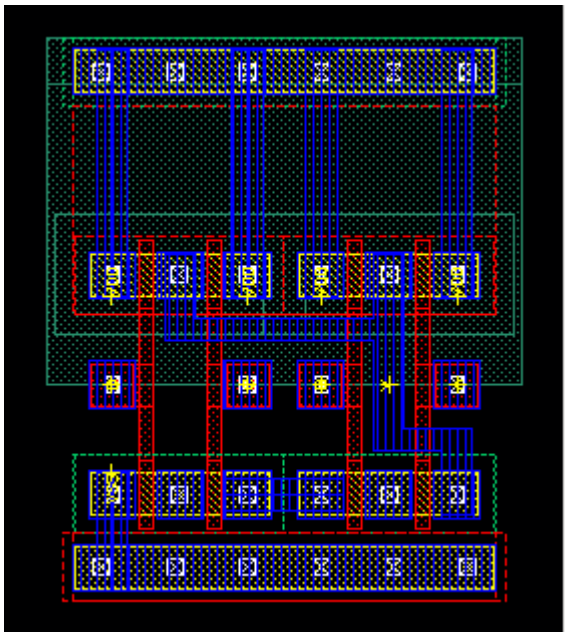


PTAP_TO_TR_SPACE	0	5.0

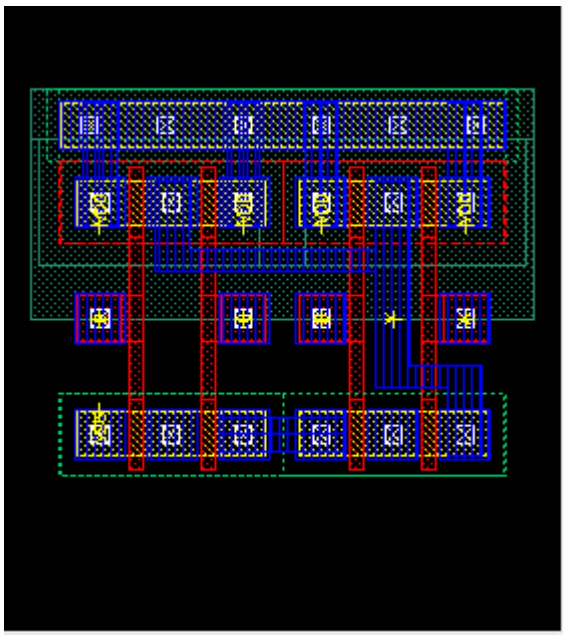


6.5 nand4

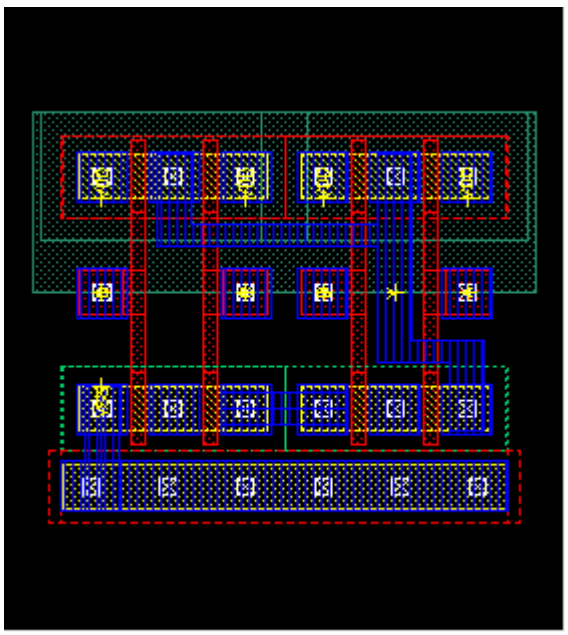
NTAP_TO_TR_SPACE	0	5



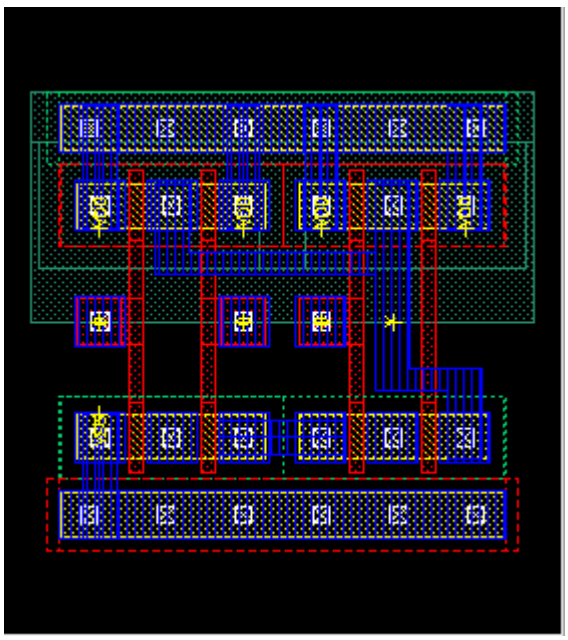
PTAP	☑ → ☐



NTAP	☑ → ☐

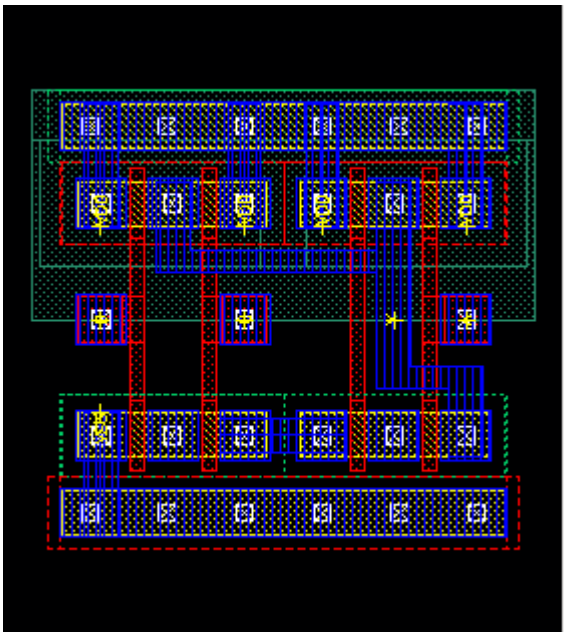


POLY1CONTA	☑ → ☐

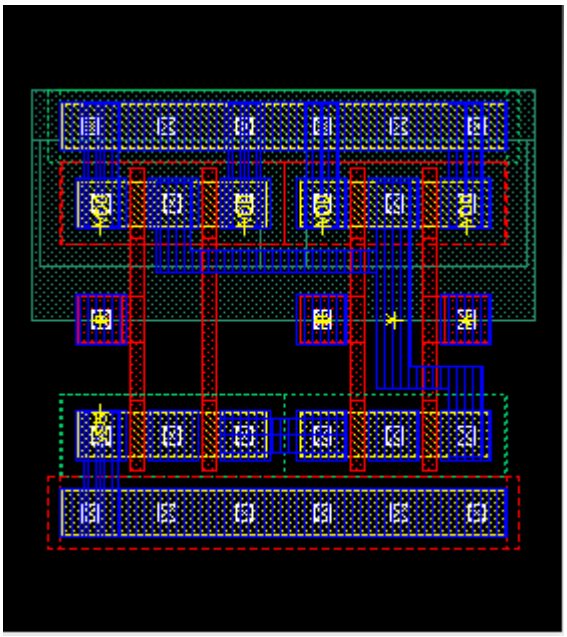


6.5 nand4

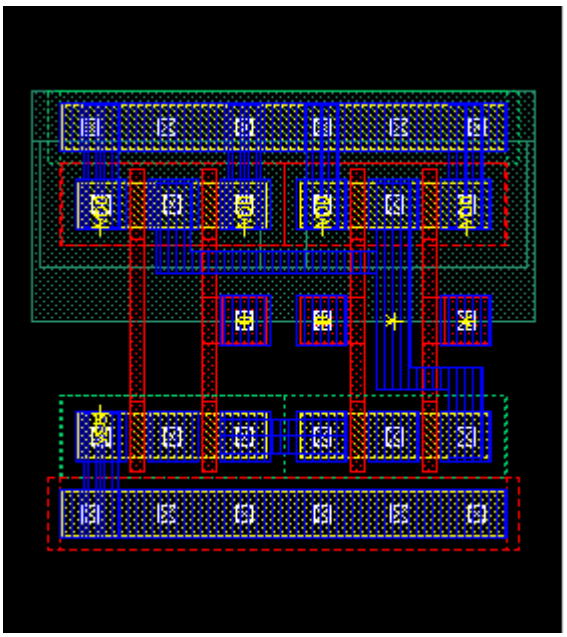
POLY1CONTB	☑ → ☐



POLY1CONTC	☑ → ☐

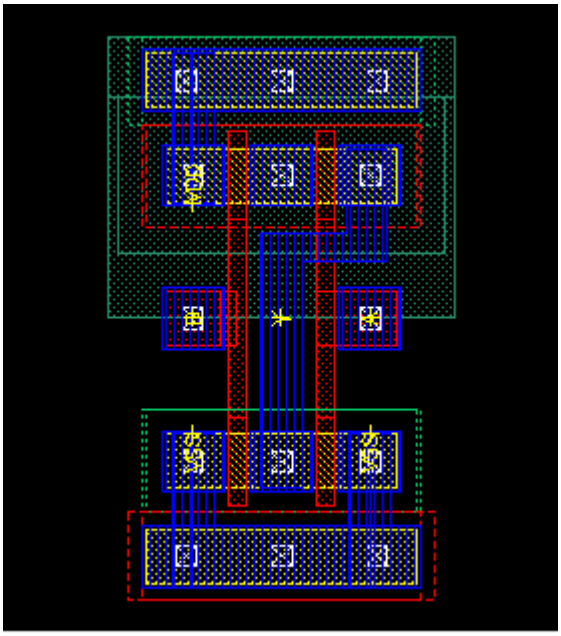


POLY1CONTD	☑ → ☐

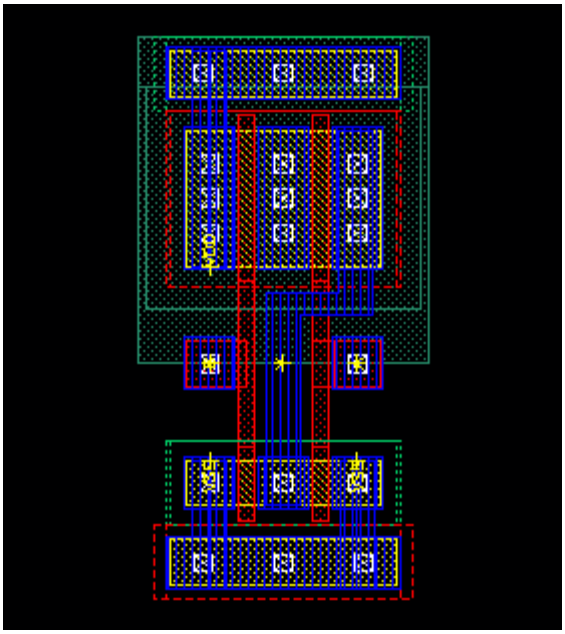


6.6 nor2

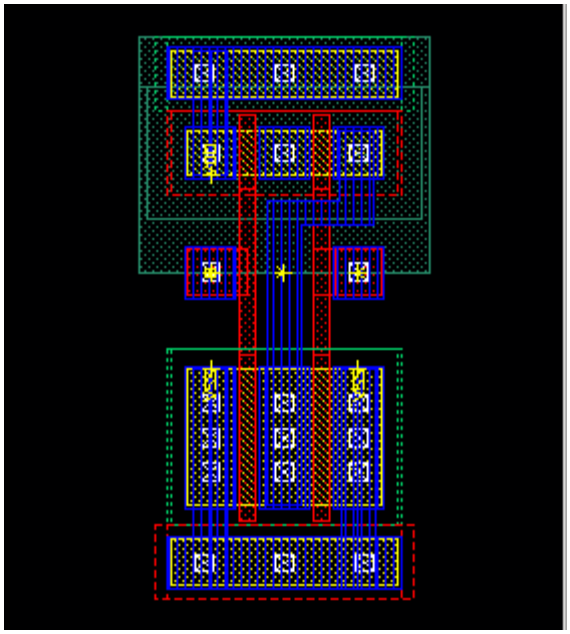
Parameter	Default	Change
P_WIDTH	1.6	*value*
N_WIDTH	1.6	*value*
LENGTH	0.5	*value*
POLY_TO_PTR_SPACE	2.6	*value*
POLY_TO_NTR_SPACE	2.6	*value*
PTAP_TO_TR_SPACE	0	*value*
NTAP_TO_TR_SPACE	0	*value*
PTAP	☑	☐
NTAP	☑	☐
POLY1CONTA	☑	☐
POLY1CONTB	☑	☐



P_WIDTH	1.6	4.8

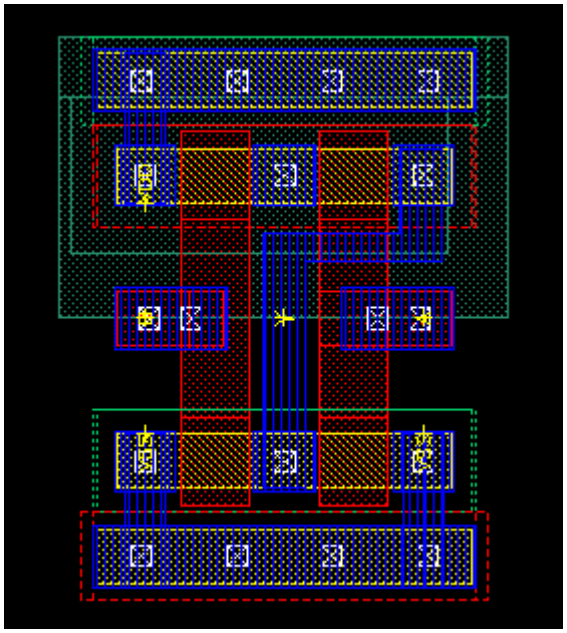


N_WIDTH	1.6	4.8

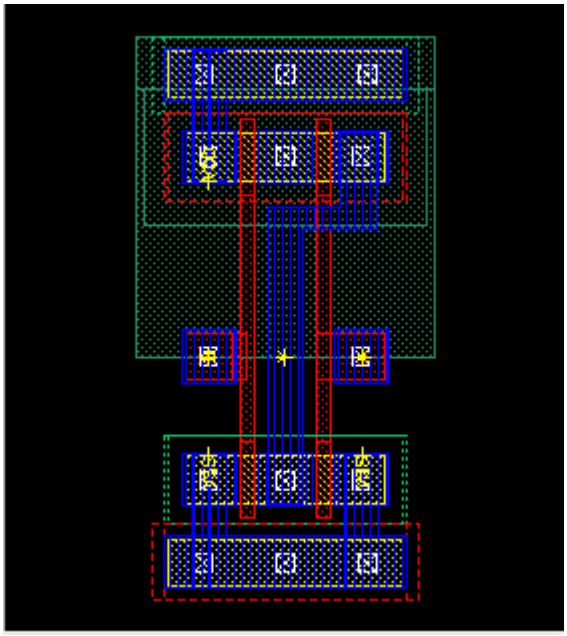


6.6 nor2

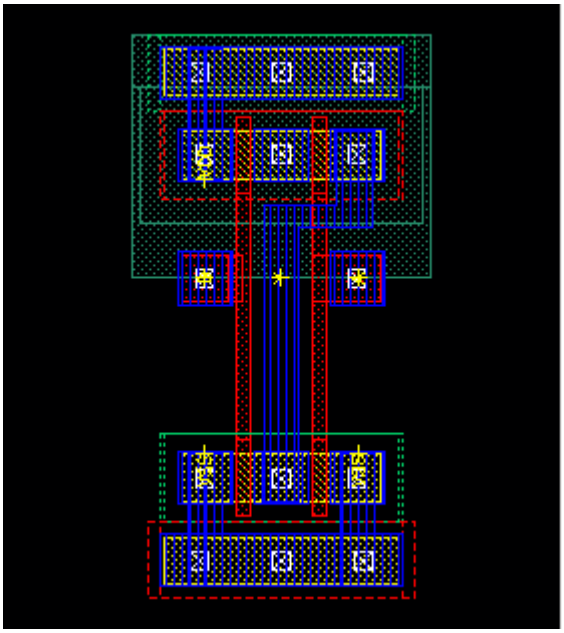
LENGTH	0.5	2



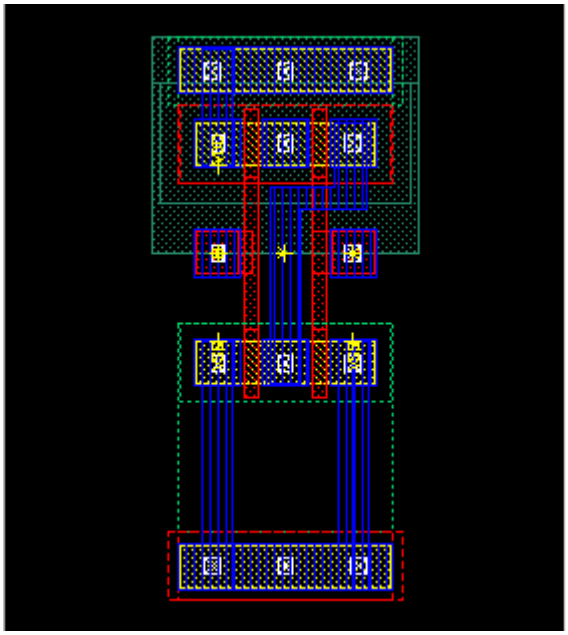
POLY_TO_PTR_SPACE	2.6	5.2



POLY_TO_NTR_SPACE	2.6	5.2

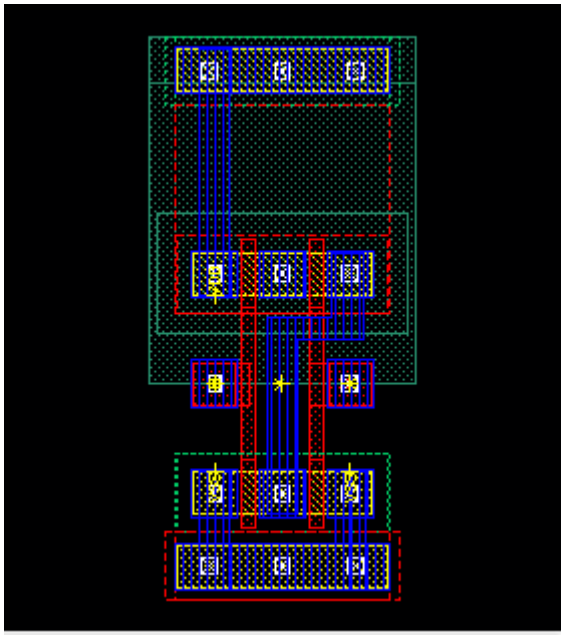


PTAP_TO_TR_SPACE	0	5.0

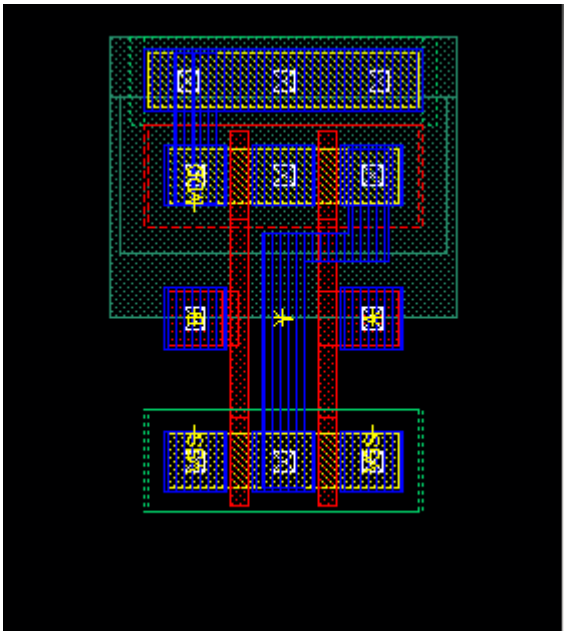


6.6 nor2

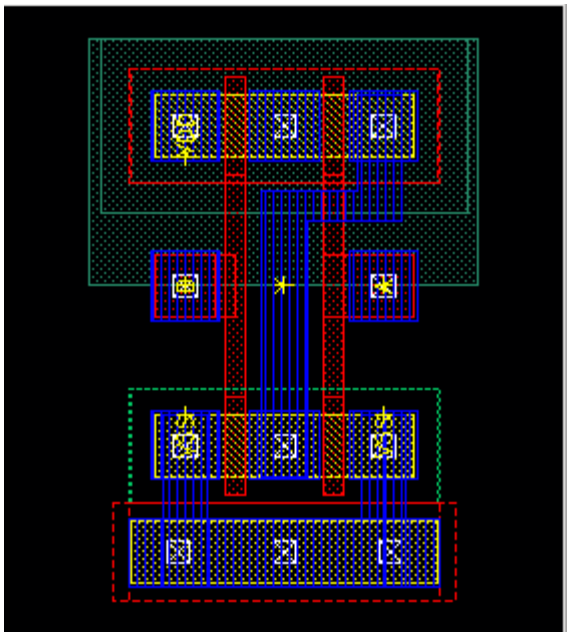
NTAP_TO_TR_SPACE	0	5



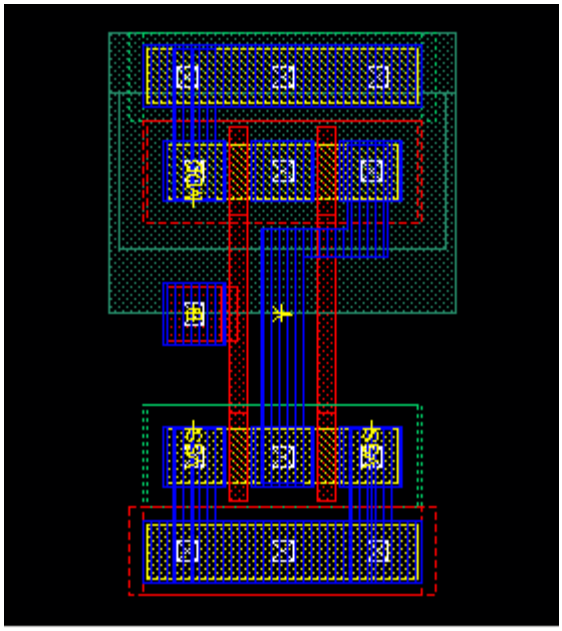
PTAP	☑ → ☐



NTAP	☑ → ☐

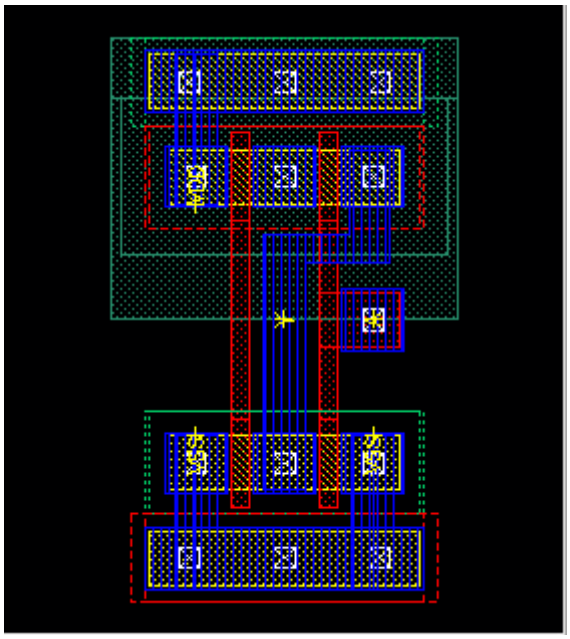


POLY1CONTA	☑ → ☐



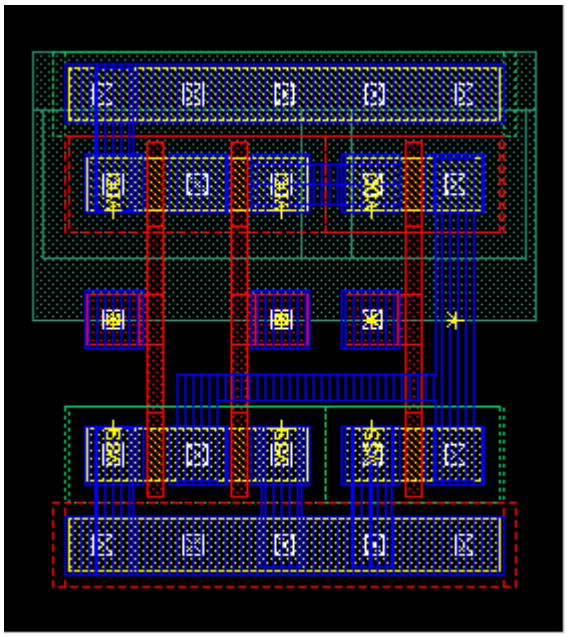
6.6 nor2

POLY1CONTB	☑ → ☐

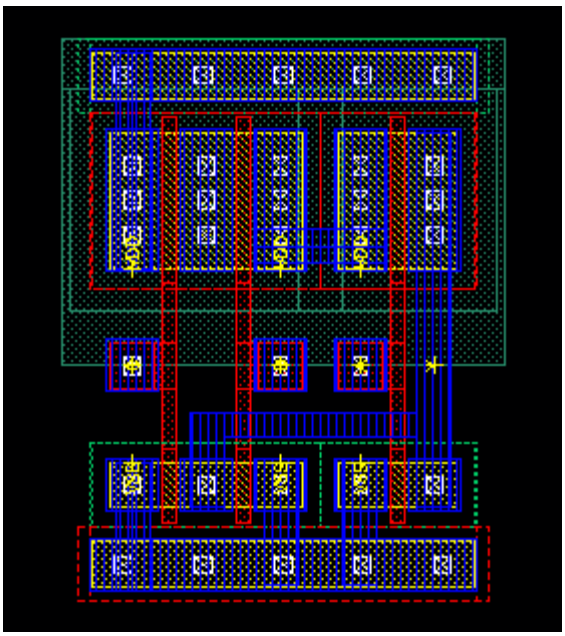


6.7 nor3

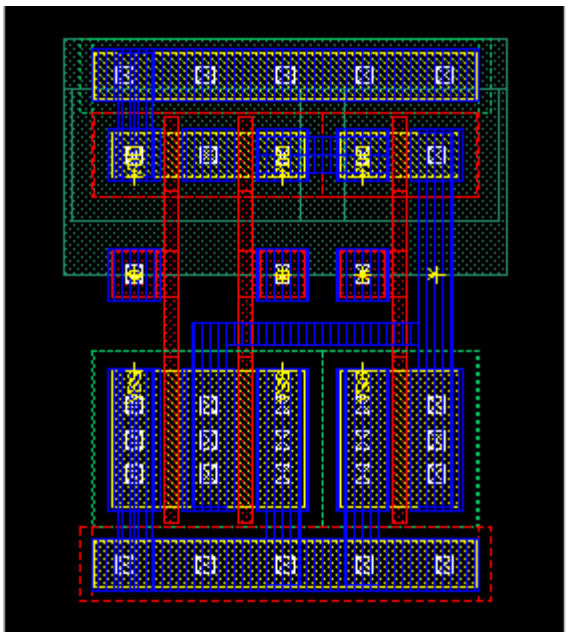
Parameter	Default	Change
P_WIDTH	1.6	*value*
N_WIDTH	1.6	*value*
LENGTH	0.5	*value*
POLY_TO_PTR_SPACE	2.6	*value*
POLY_TO_NTR_SPACE	2.6	*value*
PTAP_TO_TR_SPACE	0	*value*
NTAP_TO_TR_SPACE	0	*value*
PTAP	☑	☐
NTAP	☑	☐
POLY1CONTA	☑	☐
POLY1CONTB	☑	☐
POLY1CONTC	☑	☐



P_WIDTH	1.6	4.8

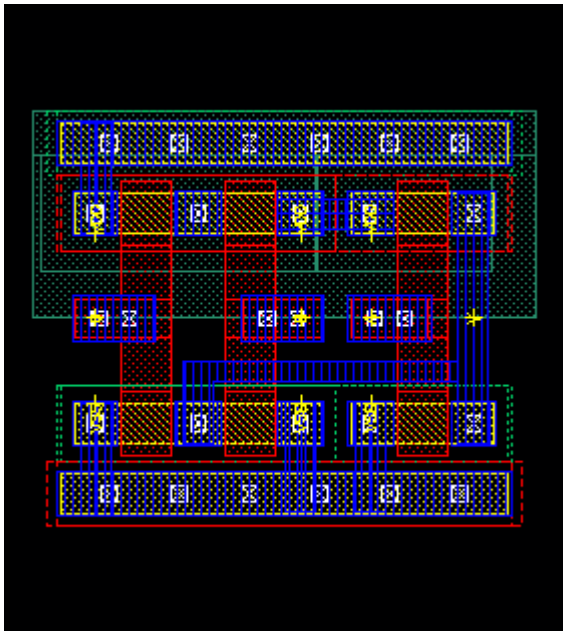


N_WIDTH	1.6	4.8

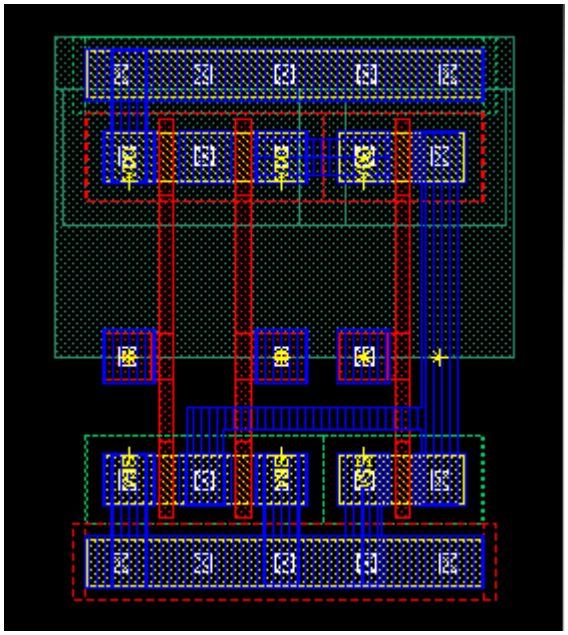


6.7 nor3

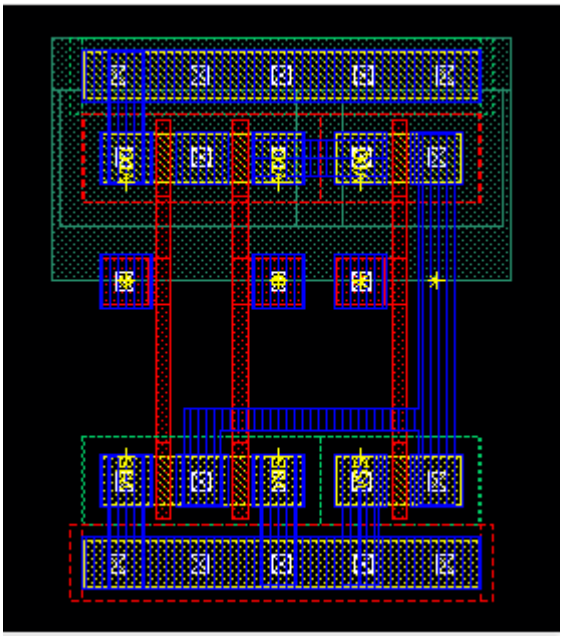
LENGTH	0.5	2



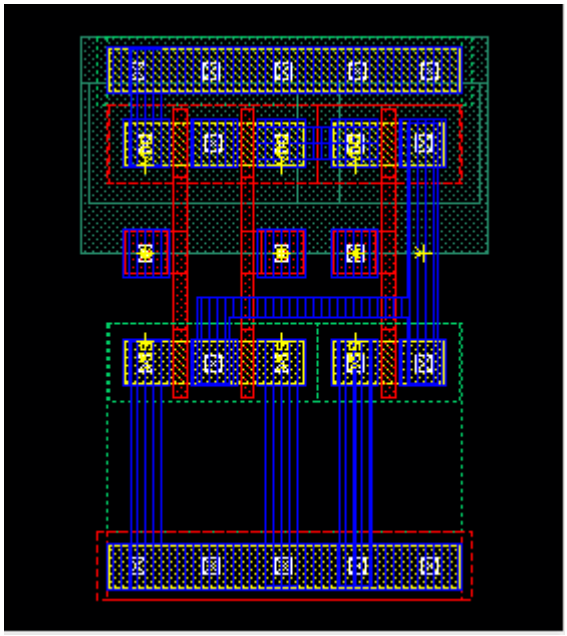
POLY_TO_PTR_SPACE	2.6	5.2



POLY_TO_NTR_SPACE	2.6	5.2

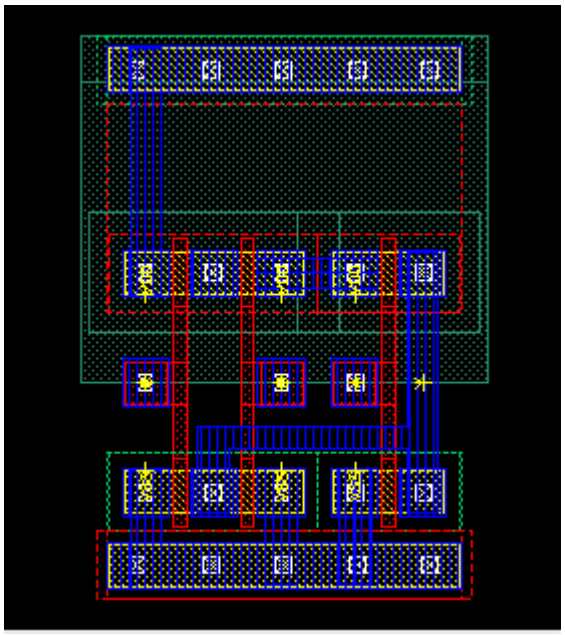


PTAP_TO_TR_SPACE	0	5.0

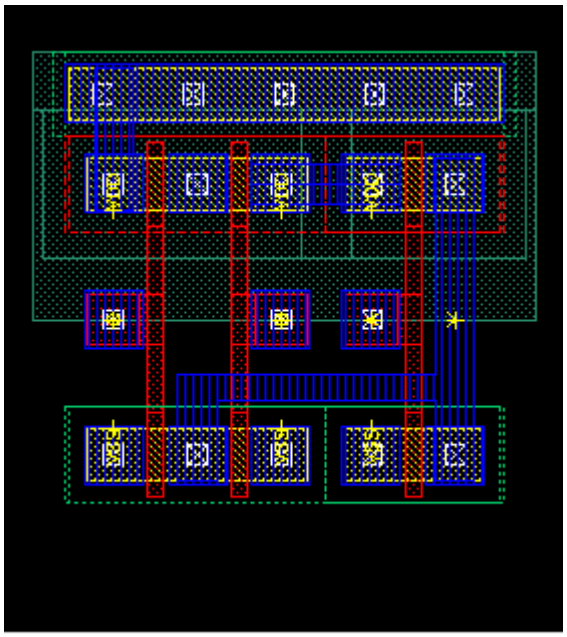


6.7 nor3

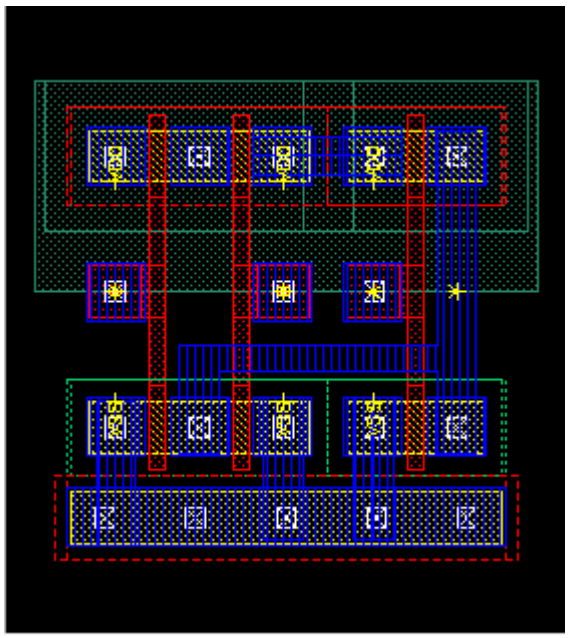
NTAP_TO_TR_SPACE	0	5



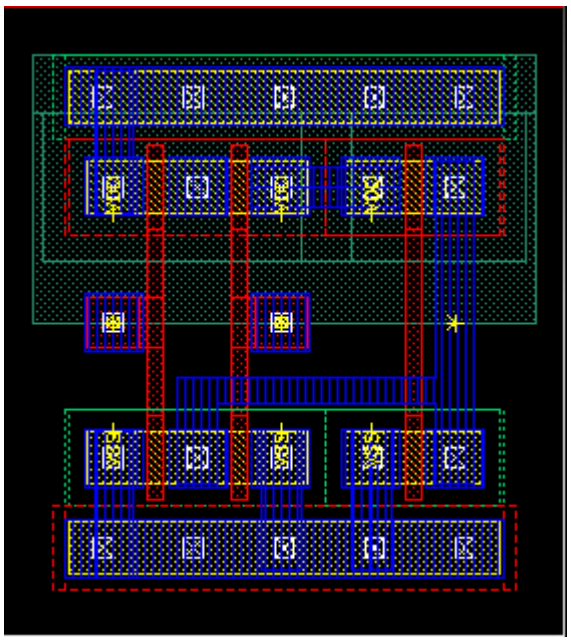
PTAP	☑ → ☐



NTAP	☑ → ☐

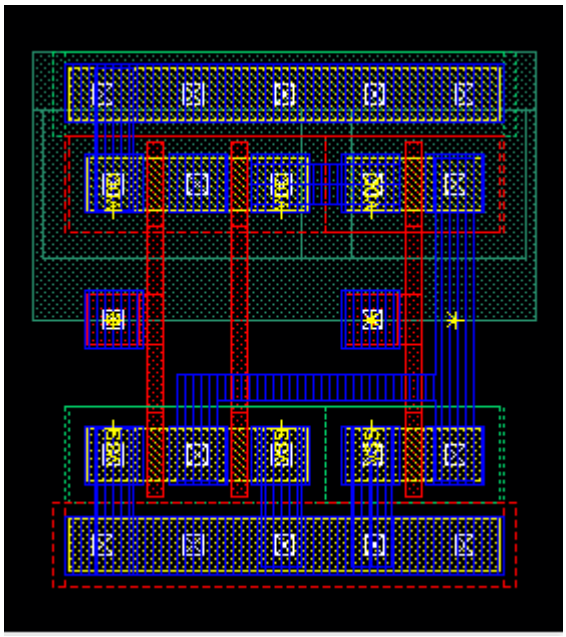


POLY1CONTA	☑ → ☐

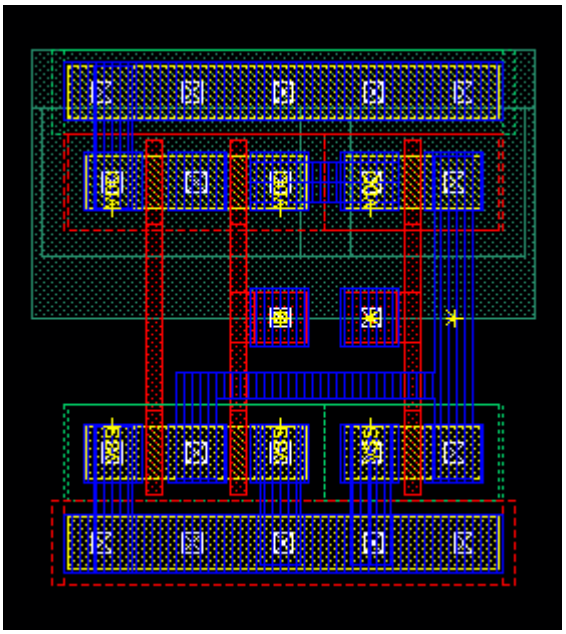


6.7 nor3

POLY1CONTB	☑ → ☐

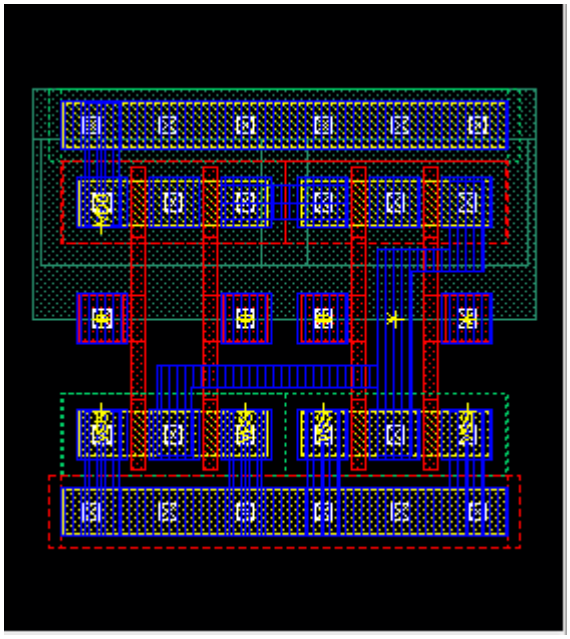


POLY1CONTC	☑ → ☐

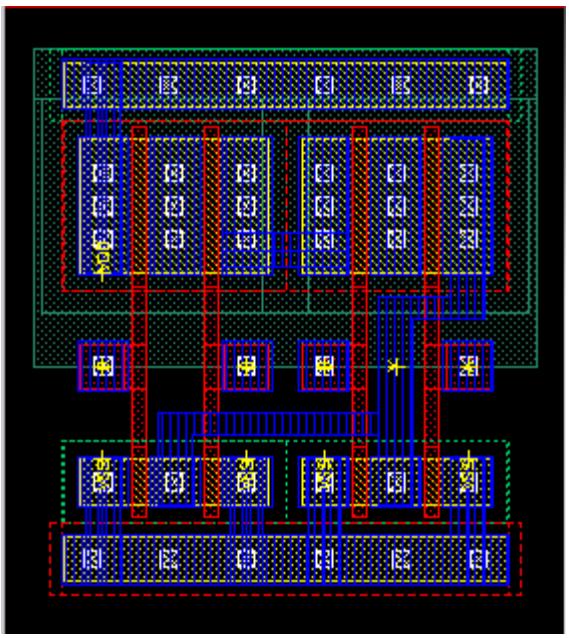


6.8 nor4

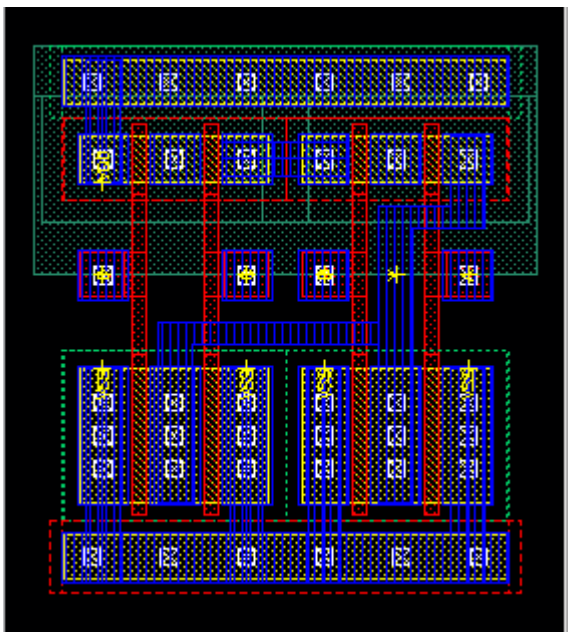
Parameter	Default	Change
P_WIDTH	1.6	*value*
N_WIDTH	1.6	*value*
LENGTH	0.5	*value*
POLY_TO_PTR_SPACE	2.6	*value*
POLY_TO_NTR_SPACE	2.6	*value*
PTAP_TO_TR_SPACE	0	*value*
NTAP_TO_TR_SPACE	0	*value*
PTAP	☑	☐
NTAP	☑	☐
POLY1CONTA	☑	☐
POLY1CONTB	☑	☐
POLY1CONTC	☑	☐
POLY1CONTD	☑	☐



P_WIDTH	1.6	4.8

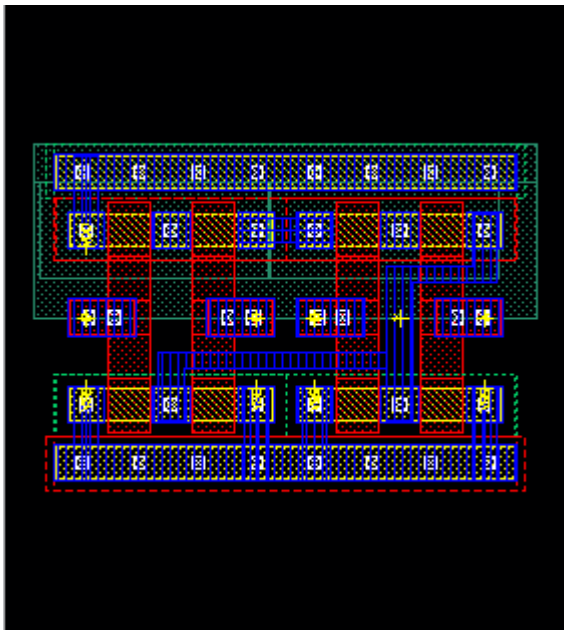


N_WIDTH	1.6	4.8

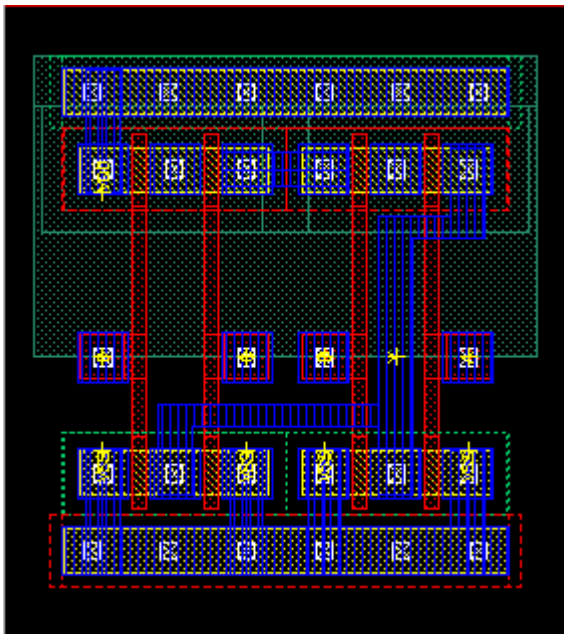


6.8 nor4

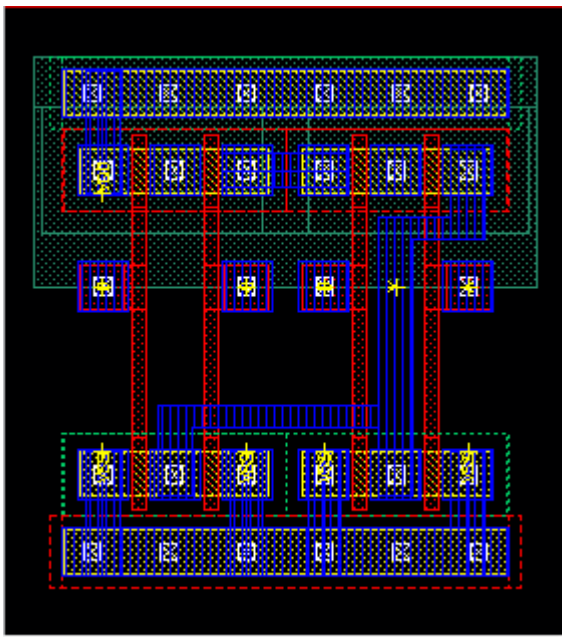
LENGTH	0.5	2



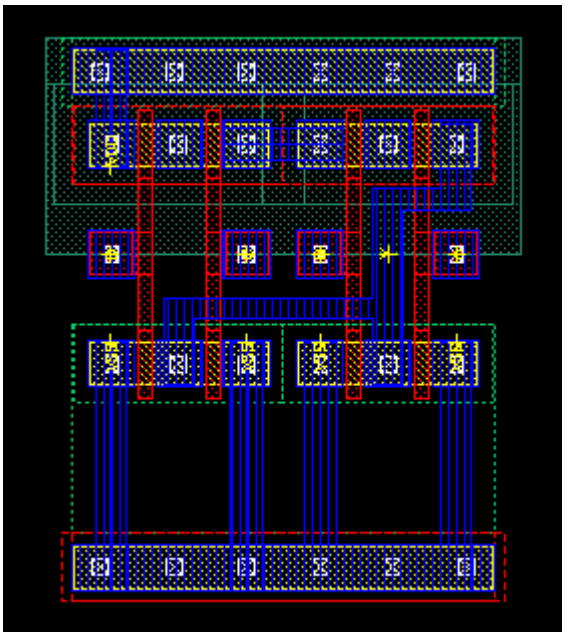
POLY_TO_PTR_SPACE	2.6	5.2



POLY_TO_NTR_SPACE	2.6	5.2

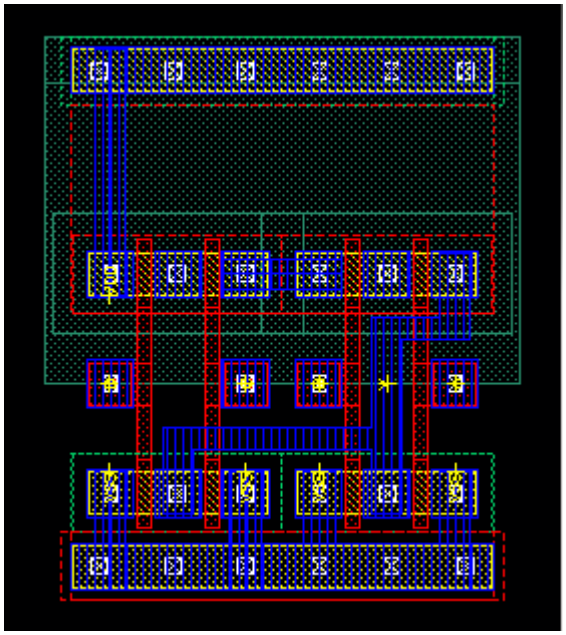


PTAP_TO_TR_SPACE	0	5.0

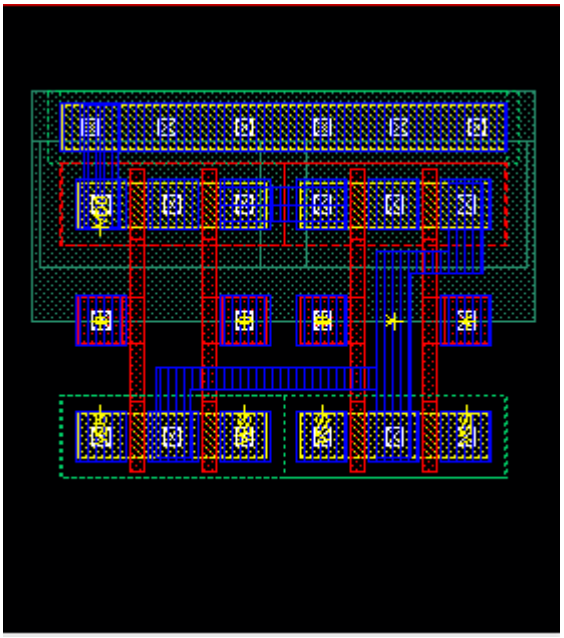


6.8 nor4

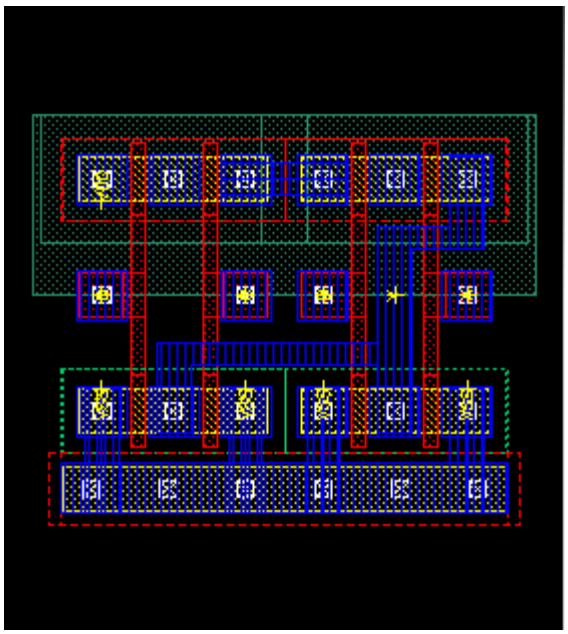
NTAP_TO_TR_SPACE	0	5



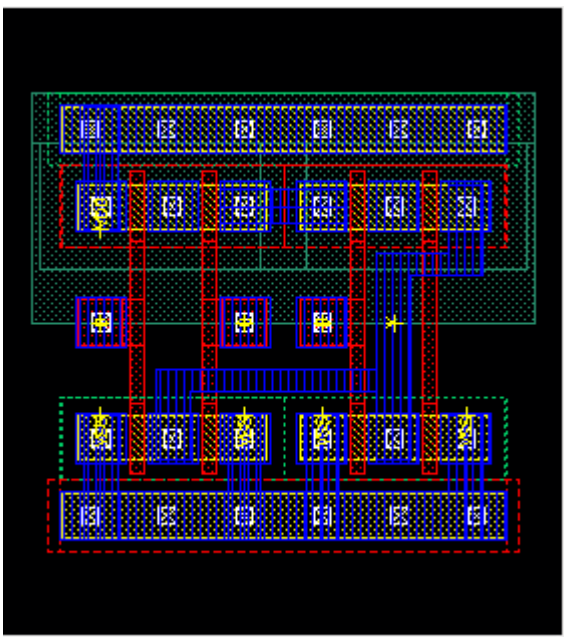
PTAP	☑ → ☐



NTAP	☑ → ☐

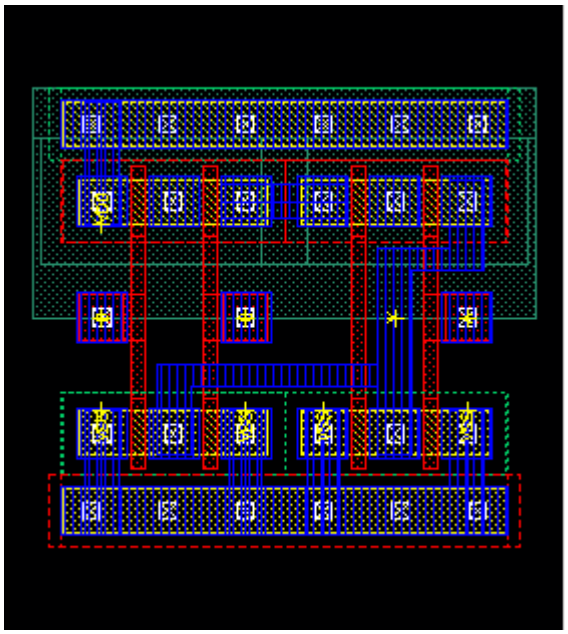


POLY1CONTA	☑ → ☐

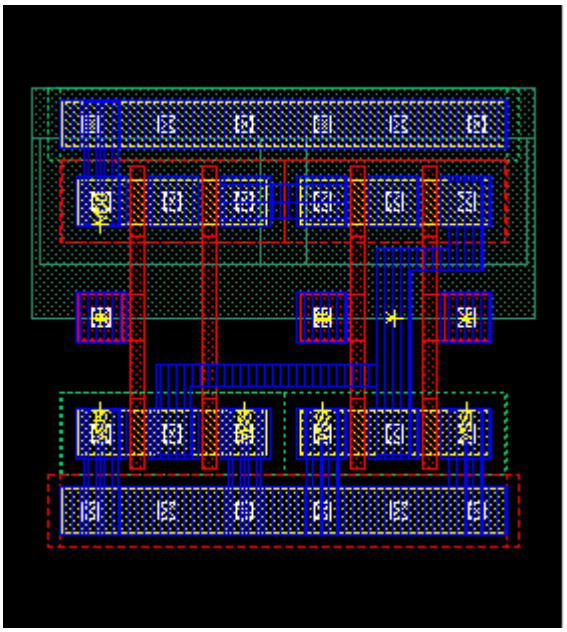


6.8 nor4

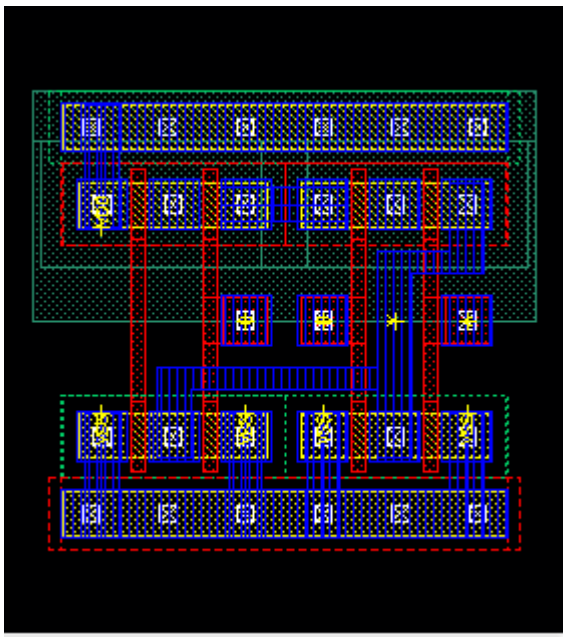
POLY1CONTB	☑ → ☐



POLY1CONTC	☑ → ☐

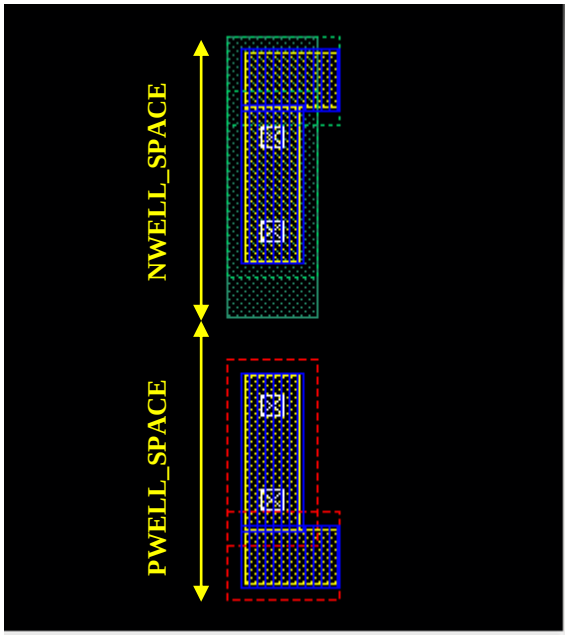


POLY1CONTD	☑ → ☐

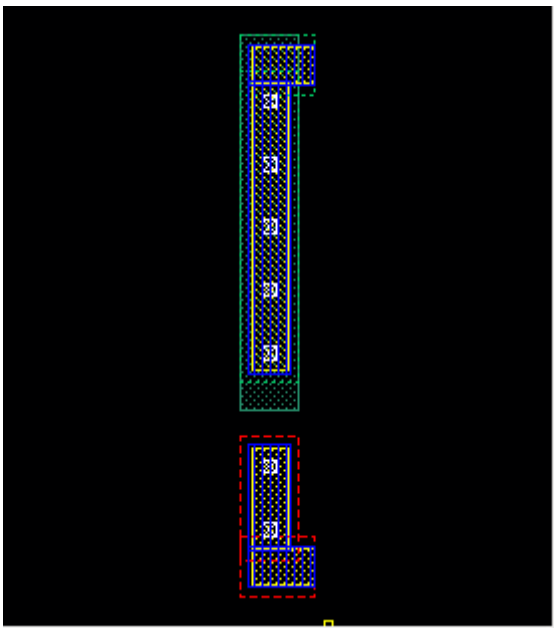


6.9 edge

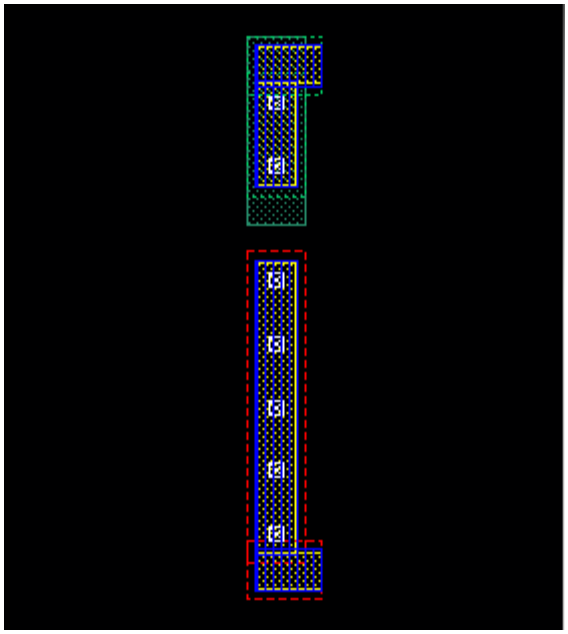
Parameter	Default	Change
NWELL_SPACE	8.3	*value*
PWELL_SPACE	8.3	*value*



NWELL_SPACE	8.3	16.6

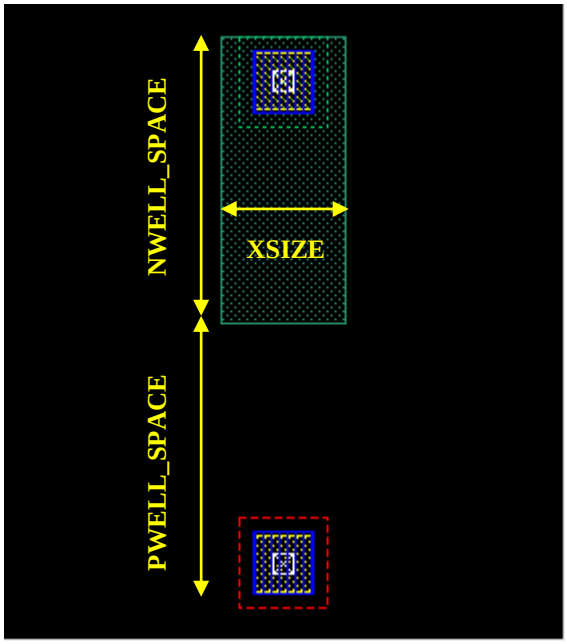


PWELL_SPACE	8.3	16.6

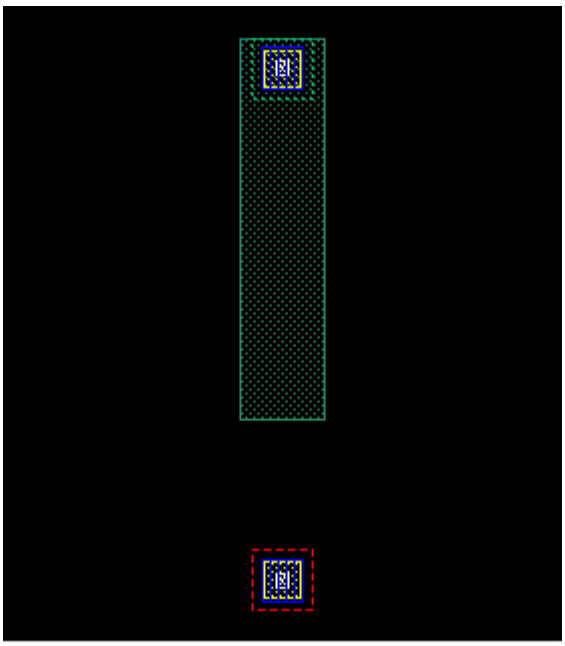


6.10 filler

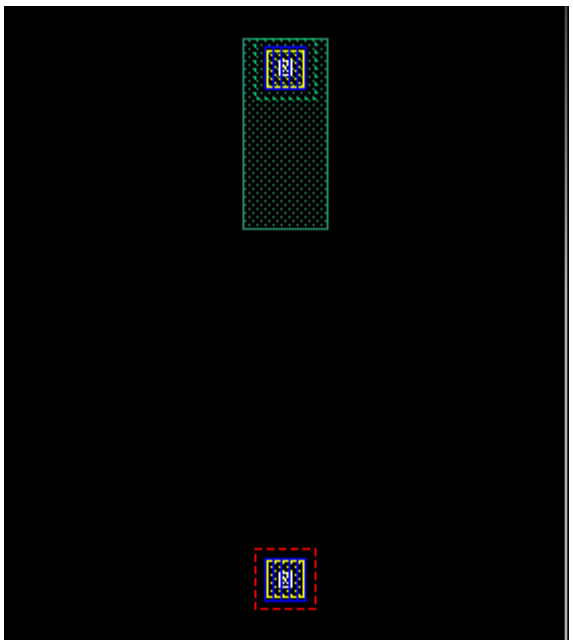
Parameter	Default	Change
NWELL_SPACE	8.3	*value*
PWELL_SPACE	8.3	*value*
XSIZE	1.8	*value*



NWELL_SPACE	8.3	16.6

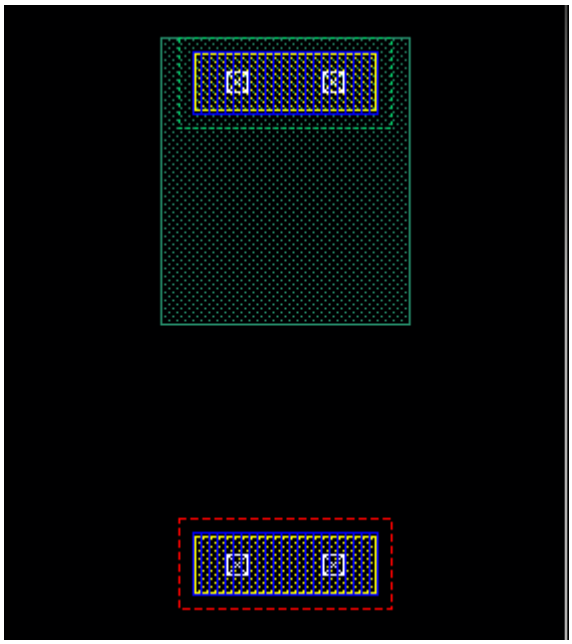


PWELL_SPACE	8.3	16.6

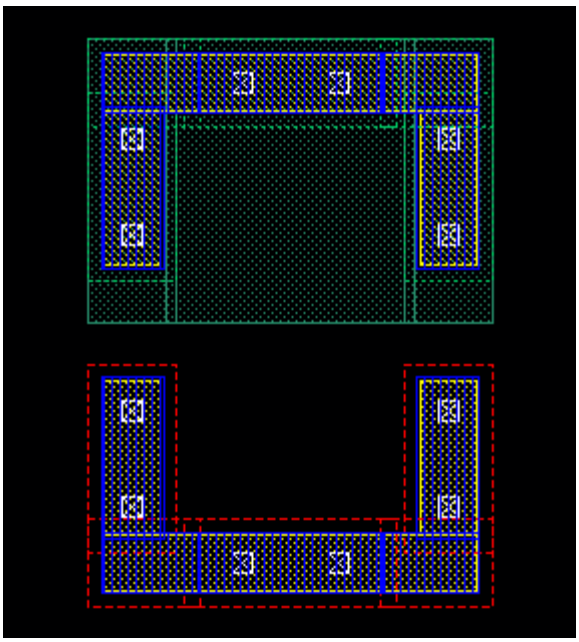


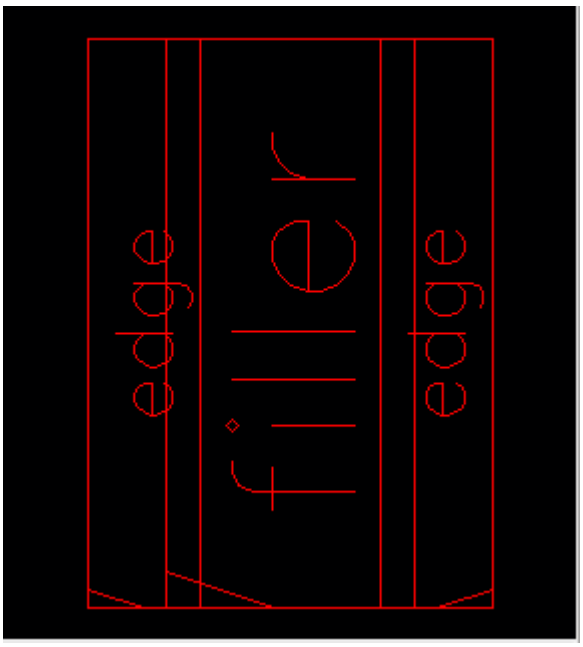
6.10 filler

XSIZE	1.8	5.4



6.11 edge_filler

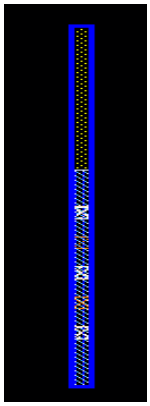


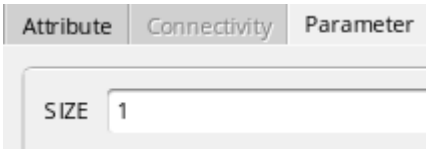


7. Sealring

7.1 Sealring information [ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_pcell]

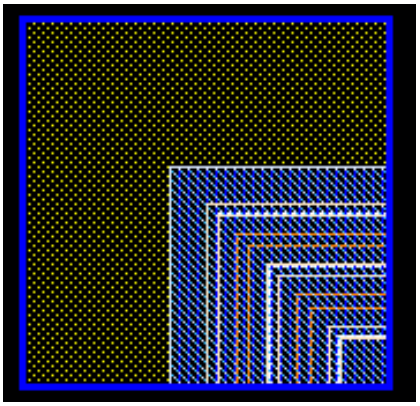
- For protect layout block from DIE cutting, you can use sealring cell in ETRI_0p5um_Analog_CMOS_5p0V_pcell library. (SEALRING_UNIT, SEALRING_CONER)





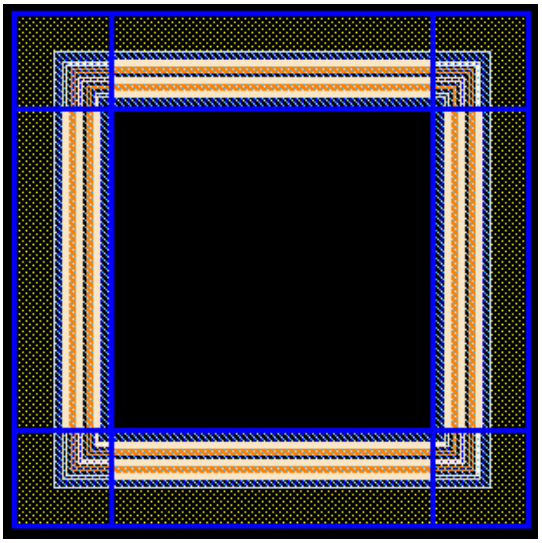
Can adjust size using SIZE parameter

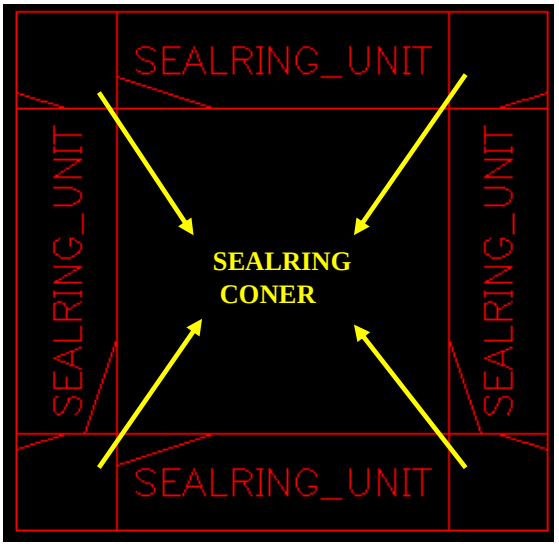
SIZE Minimum value is 1



-SEALRING_UNIT

-SEALRING_CONER



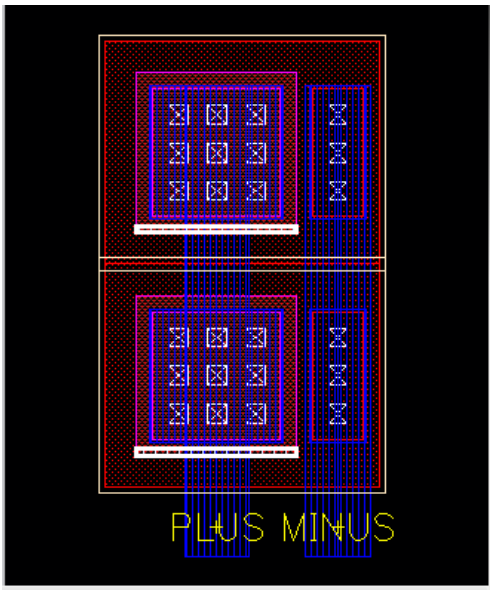


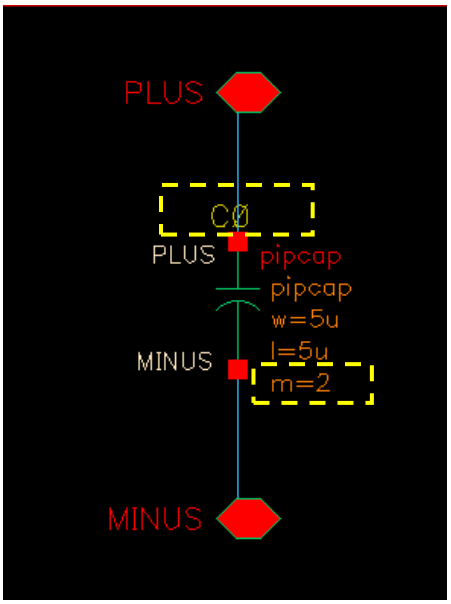
-Adjusted SEALRING_UNIT and SEALRING_CONER

8. LVS Guide

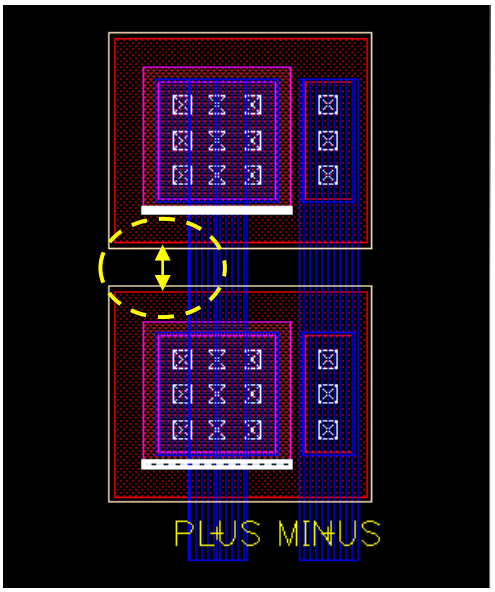
8.1 PIPCAP Layout/Circuit Structure

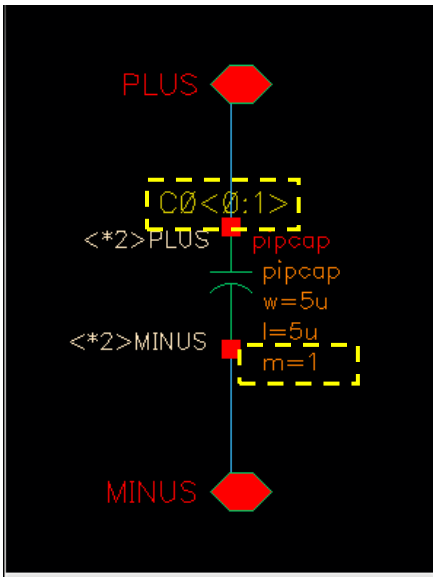
- **Case1 : Merged PIPCAP**





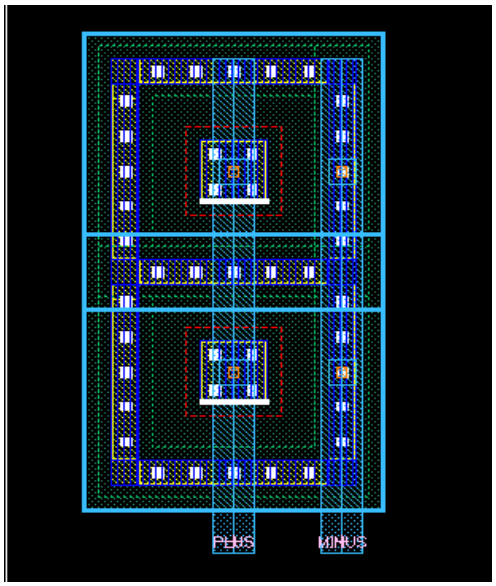
- **Case2 : Separated PIPCAP**

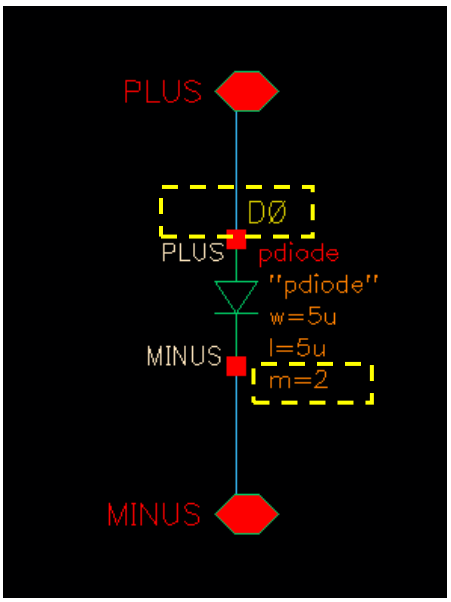




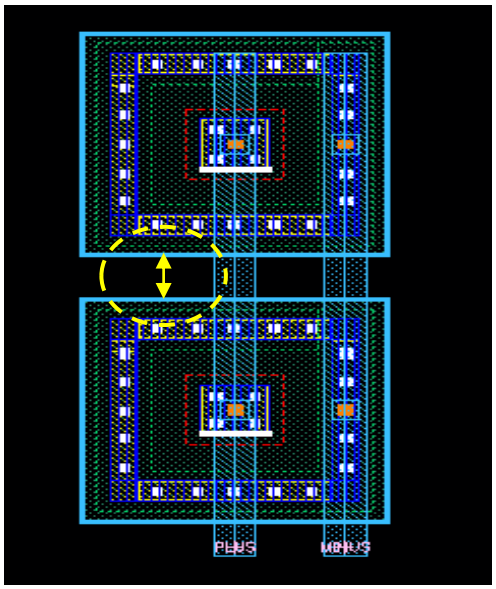
8.2 PDIODE Layout/Circuit Structure

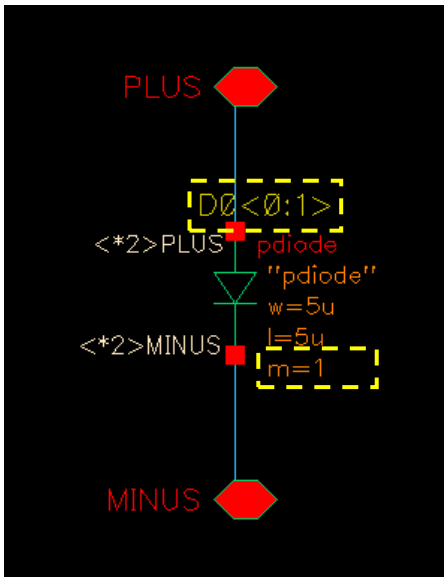
- **Case1 : Merged PDIODE**





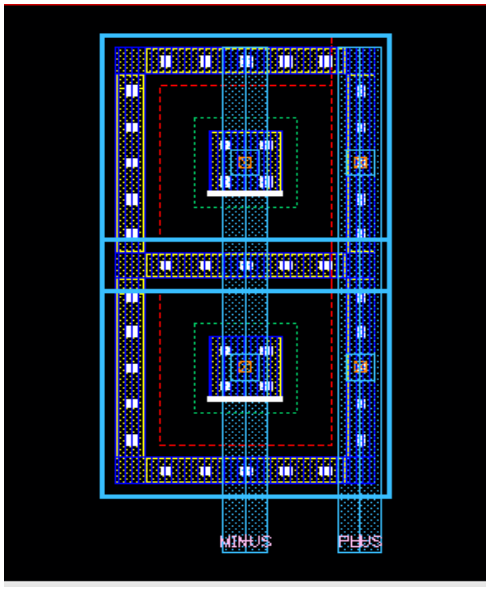
- **Case2 : Separated PDIODE**

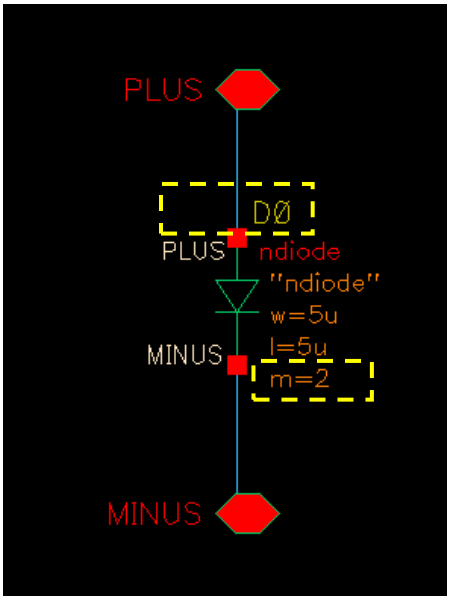




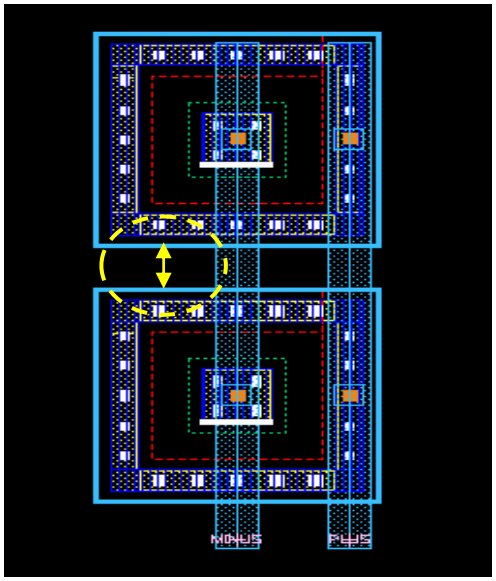
8.3 NDIODE Layout/Circuit Structure

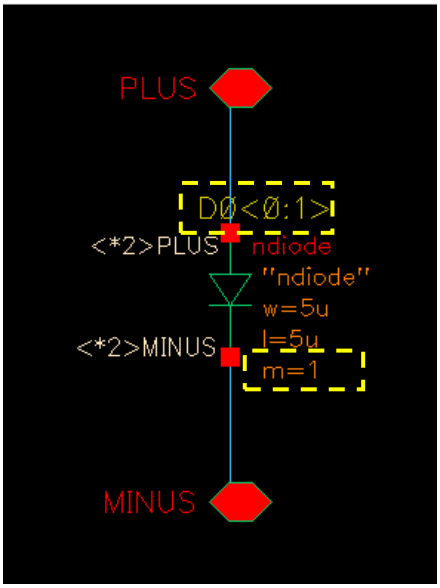
- **Case1 : Merged NDIODE**





- **Case2 : Separated NDIODE**



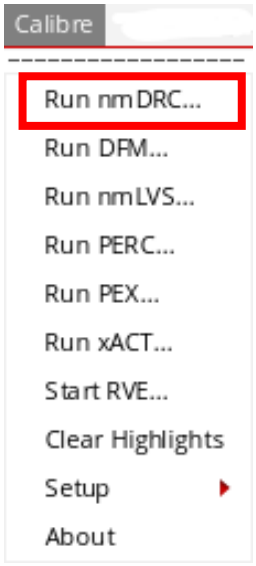


9. Calibre DRC

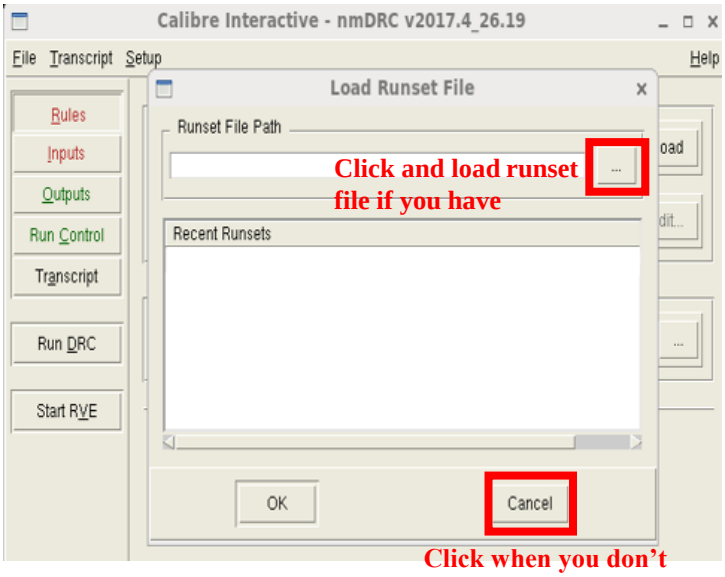
9.1 Run for DRC at GUI

- For running DRC(Design Rule Check) at GUI after layout, need to several steps like below pictures

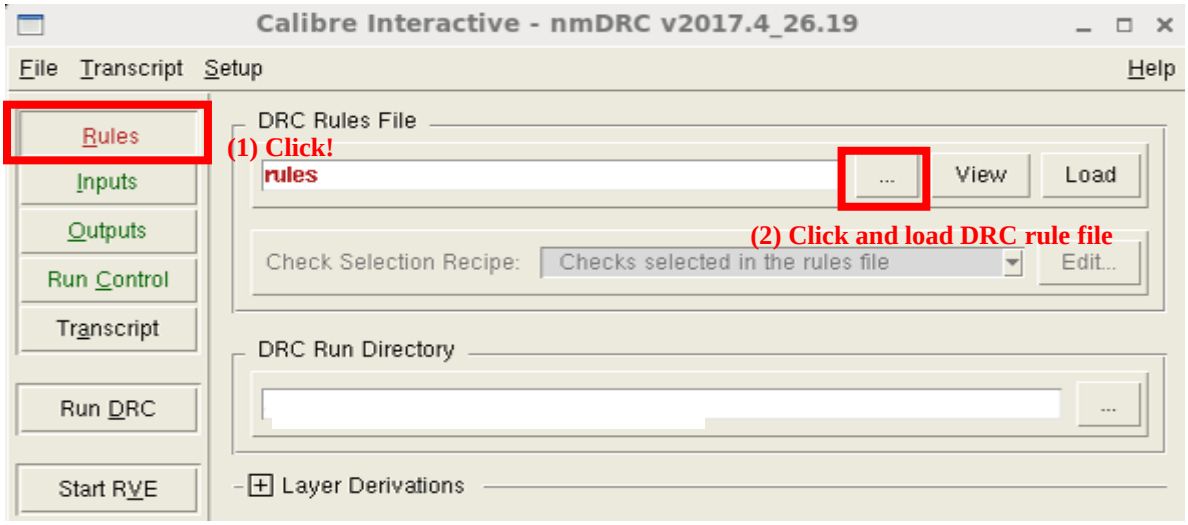
1 Click Run nmDRC in Calibre menu



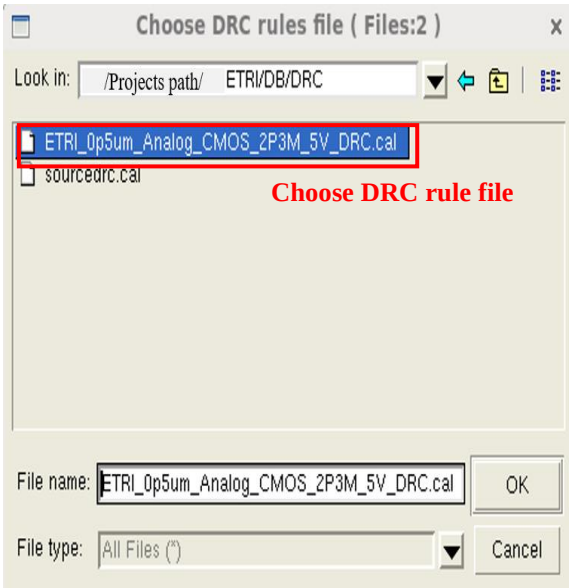
2 If runset file is exist, Load runset file. Runset file is not exist, click cancel



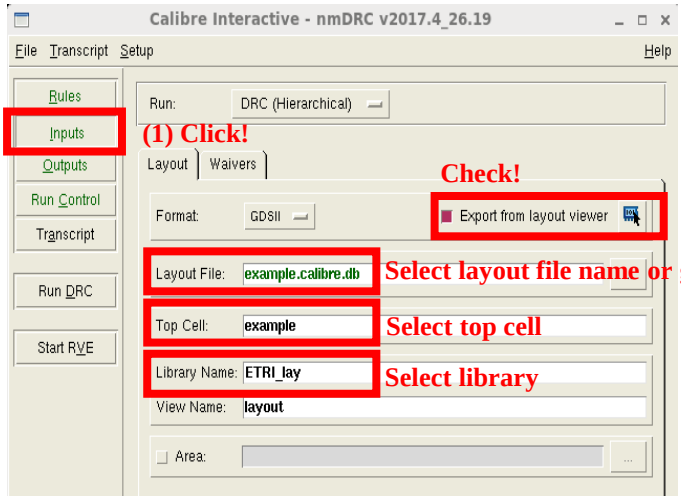
3 Load DRC rules file (ETRI_0p5um_Analog_CMOS_2P3M_5V_DRC.cal)



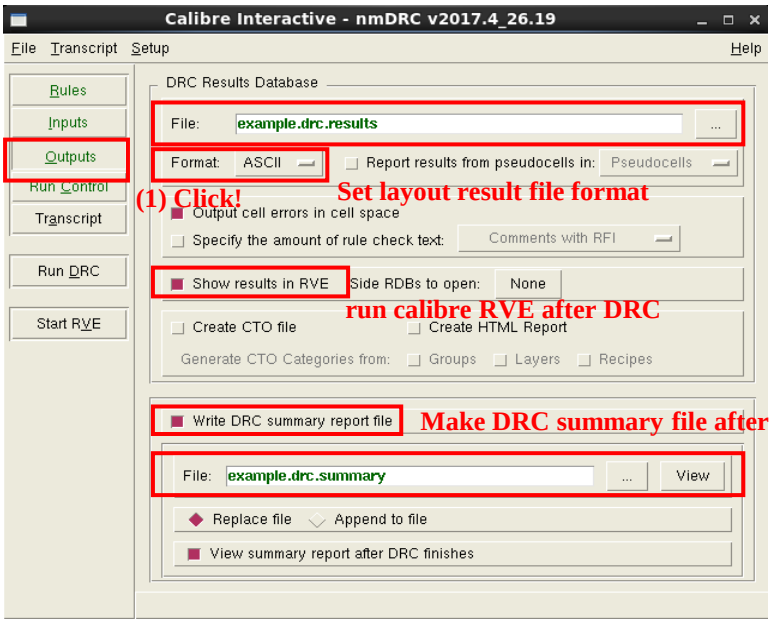
3 Load DRC rules file.



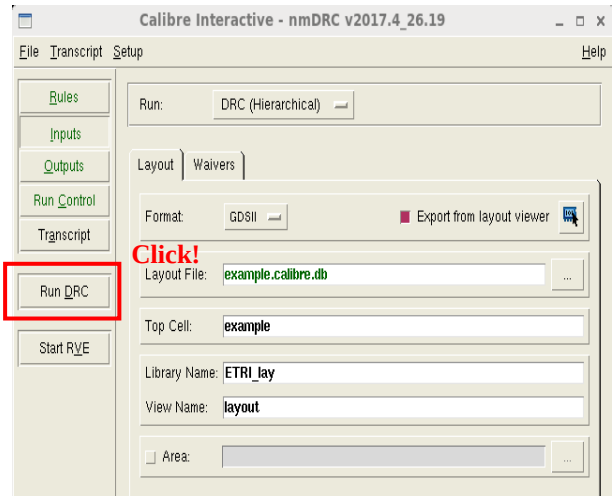
4 Set Input data. If you checked Export from layout viewer, insert layout file name to layout file. Not checked, Input your gds name want to run.



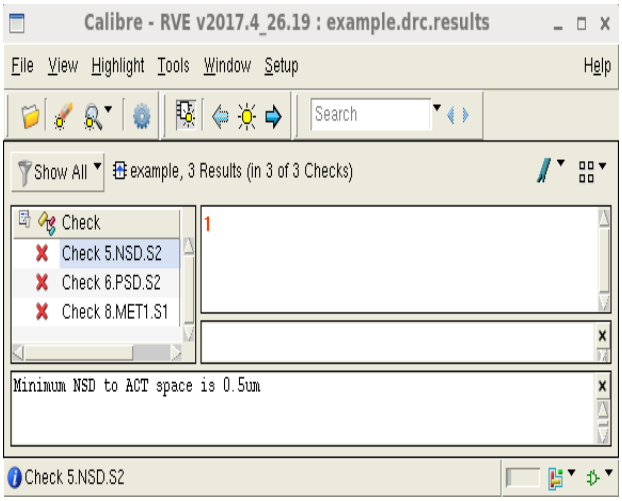
5 Set layout output data



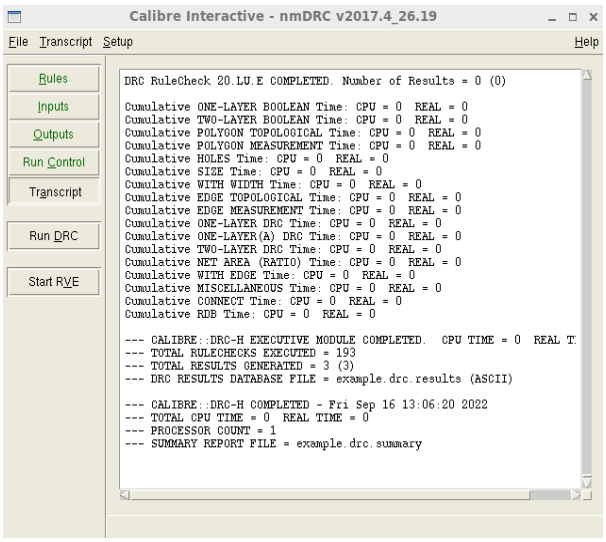
6 Run DRC



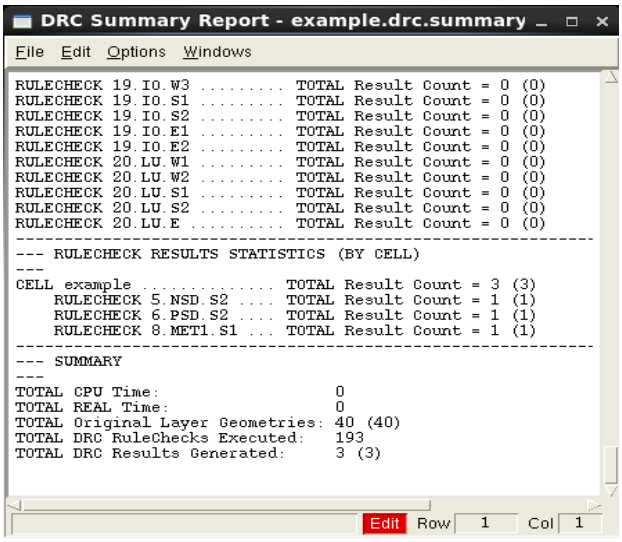
7 Get results (RVE)



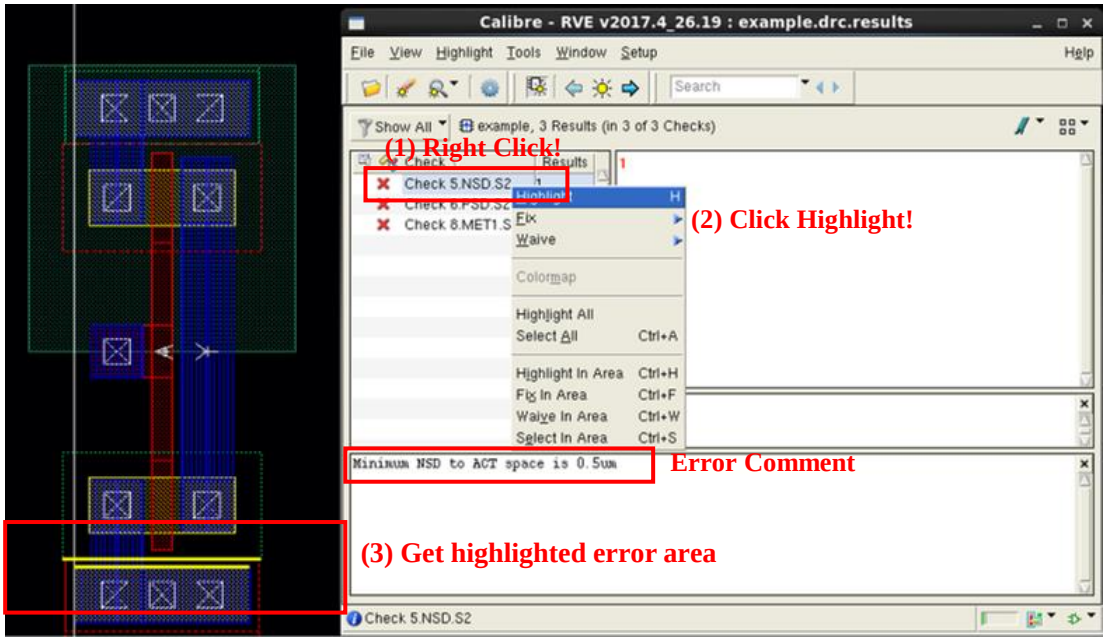
7 Get results (transcript)



7 Get results (summary)

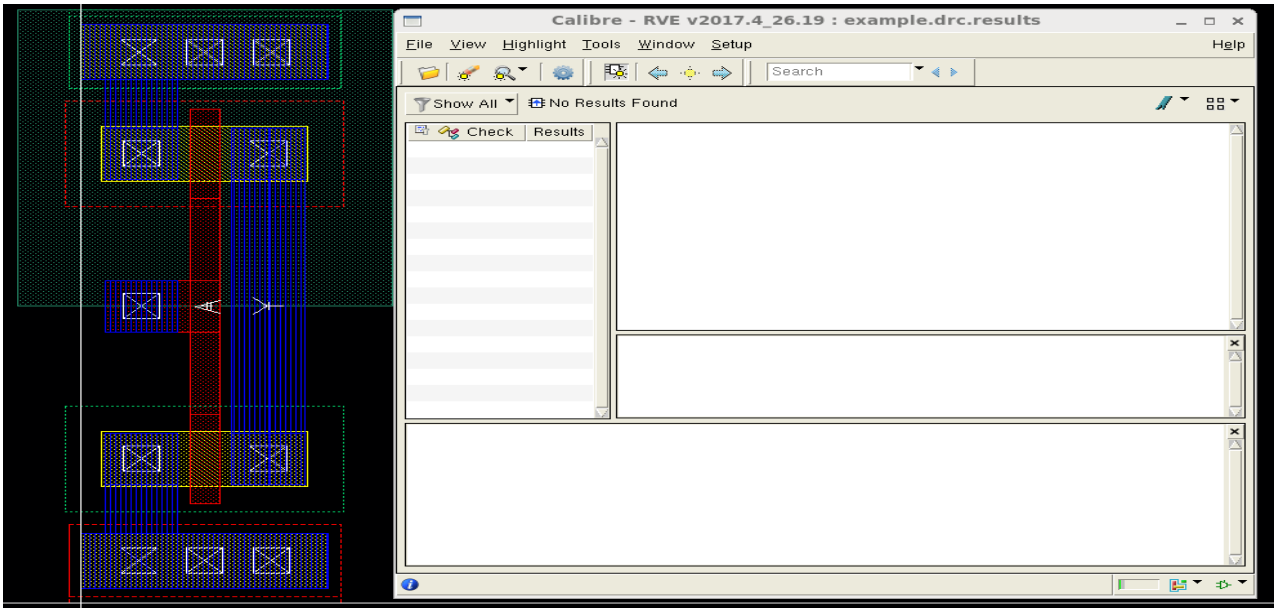


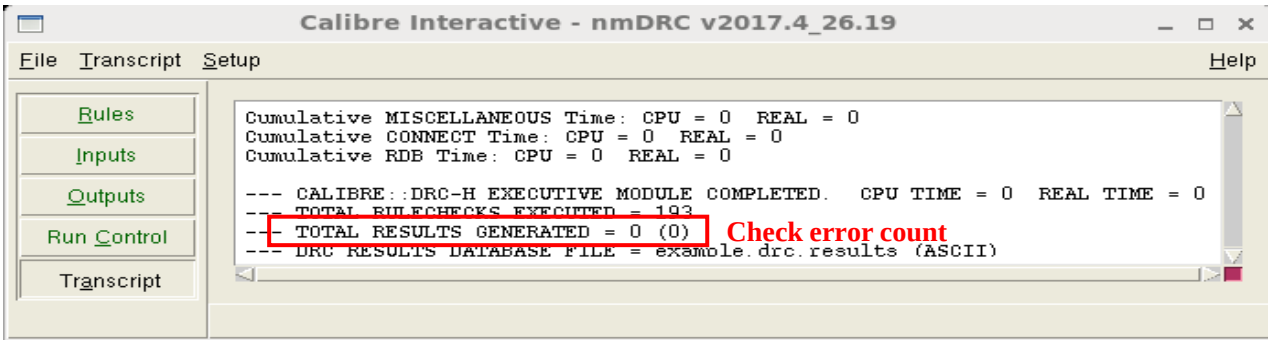
8 Run DRC

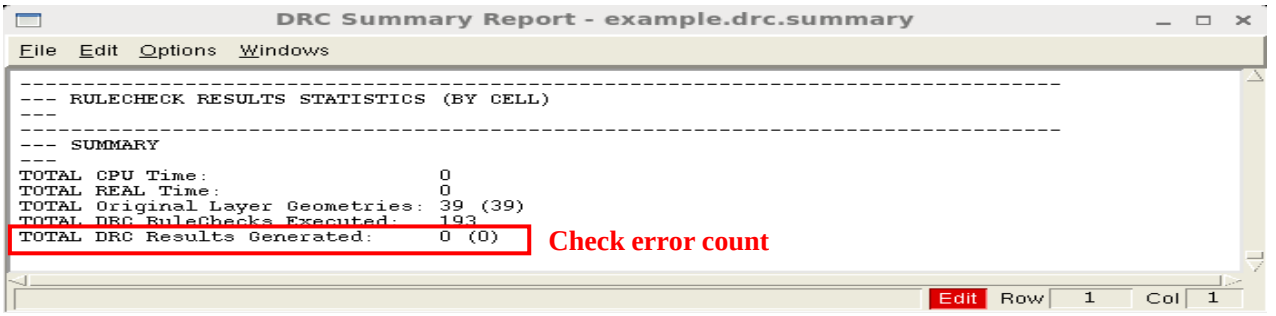


- After correct DRC errors, run again DRC.

9 Check Error Results







9.2 Script options

- In running DRC, you can use several options for convenience.
  if you need, modify this comment in the drc_header.cal

option	value	comment
LAYOUT SYSTEM	GDSII OASIS	Select layout data format GDSII or OASIS
DRC MAXIMUM RESULTS	ALL [Maxresults]	Select maximum result of errors in running drc. Non-negative integer can be Maxresults. Default value is 1000
DRC SELECT CHECK	[rule name] [group name]	Only check selected rules You can add other rules or groups by writing name after values
DRC UNSELECT CHECK	[rule name] [group name]	Running drc except selected rules You can add other rules or groups by writing name after values
EXCLUDE CELL	[cell name]	Select cells not to be processed by drc verification. You can add other cells by writing name after values

- Before run drc, you have to modify script file(drc_header.cal) some parts below.

LAYOUT PATH “[gds_path]/[CELLNAME.gds]“
  gds_path : the directory where layout gds file is exist
  CELLNAME.gds : put in your gds file
LAYOUT PRIMARY “[CELLPRIMARY]“
  Layout database topcell for running drc.
LAYOUT SYSTEM [GDSII or OASIS]
  You can choose layout data type GDSII or OASIS
INCLUDE “[rule_path]/ETRI_0p5um_Analog_CMOS_2P3M_5V_DRC.cal “
  path that rule file is exist.

- If you want to run drc in terminal, you can use command described below.

- Example drc_header.cal

```
LAYOUT PATH "temp.gds"   Layout gds file name for DRC
LAYOUT PRIMARY "temp"    Layout primary cell name
LAYOUT SYSTEM GDSII      Select layout system GDSII or OASIS
DRC RESULTS DATABASE "TOPCELL.db" ASCII  Set DRC result file name
DRC MAXIMUM RESULTS ALL  Set DRC maximum error counts
DRC SUMMARY REPORT "TOPCELL.rep"  Set DRC summary report name
//DRC SELECT CHECK rulename or groupname  Choose rules or groups want to check
//DRC UNSELECT CHECK rulename or groupname  Except rules or groups want to check
//Groups -> 1.NWL, 2.ACT, 3.PL1, 4.PL2, 5.NSD, 6.PSD, 7.CONT, 8.MET1, 9.VIA1, 10.MET2,
 11.VIA2, 12.MET3, 13.PAD, 14.PLN2R, 15.CAP, 16.PNP, 17.NPN, 19.IO, 20.LU  List of groups
//EXCLUDE CELL cellName1 cellName2  Set exclude cells in DRC
     Remove "//" before using these options

INCLUDE "/PROJECT DIRECTORY/ETRI/DRC/ETRI_0p5um_Analog_CMOS_2P3M_5V_DRC.cal"
                                                                  DRC rule path
```

- If you want to run drc in terminal, you can use command described below.

Command: calibre –drc –hier drc_header.cal

- If you want to see results at RVE in terminal, you can use command described below.

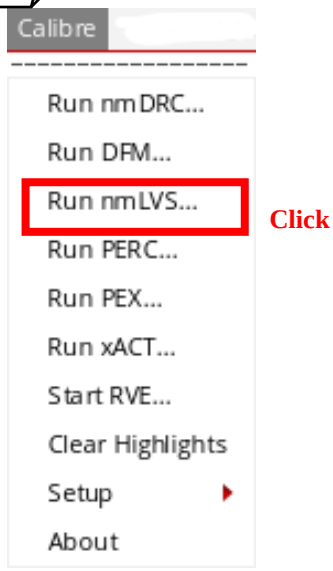
Command: calibre –rve –drc [DRC RESULTS DATABASE]
ex) calibre –rve –drc TOPCELL.db

10. Calibre LVS

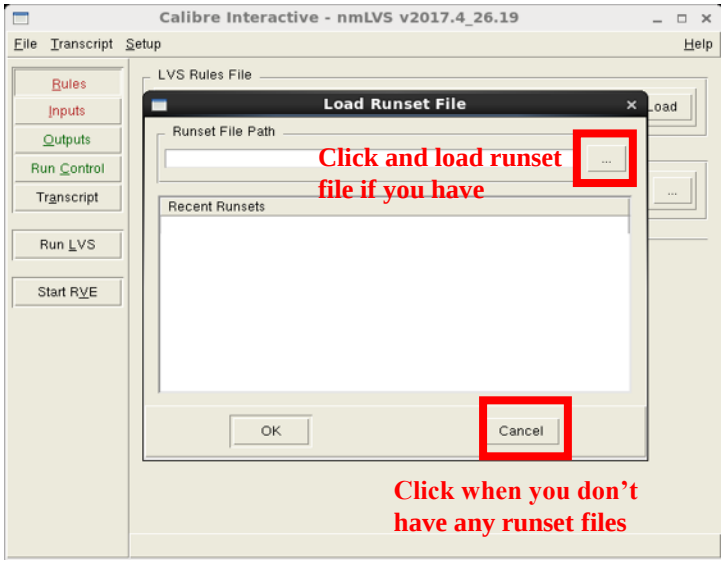
10.1 Run for LVS at GUI

- For running LVS(Layout VS Schematic) at GUI after layout, need to several steps like below pictures

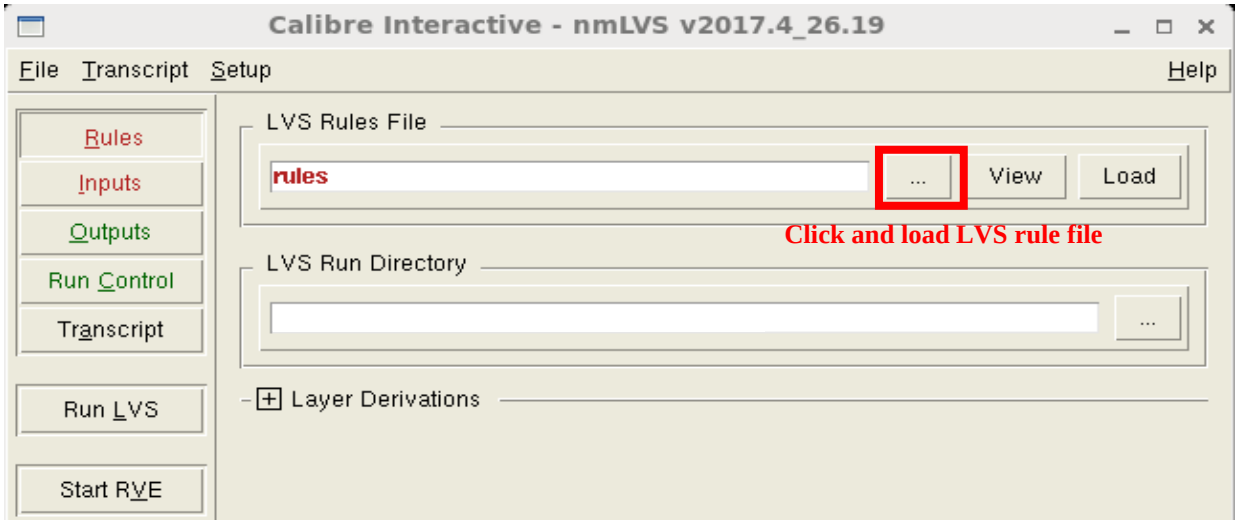
1 Click Run nmLVS in Calibre menu



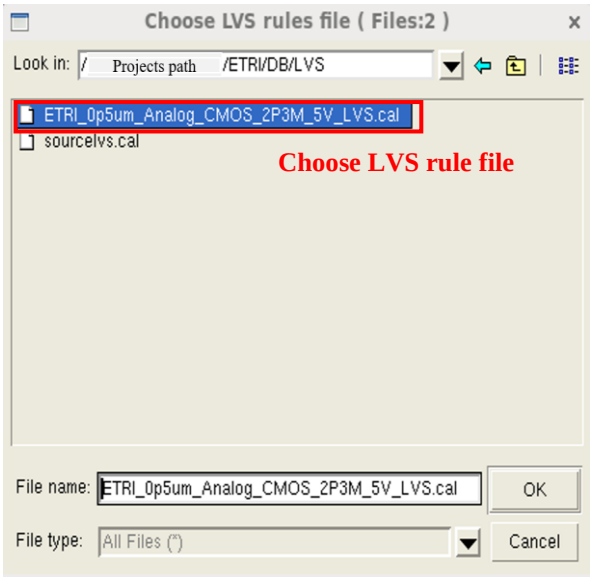
2 If runset file is exist, Load runset file. Runset file is not exist, click cancel



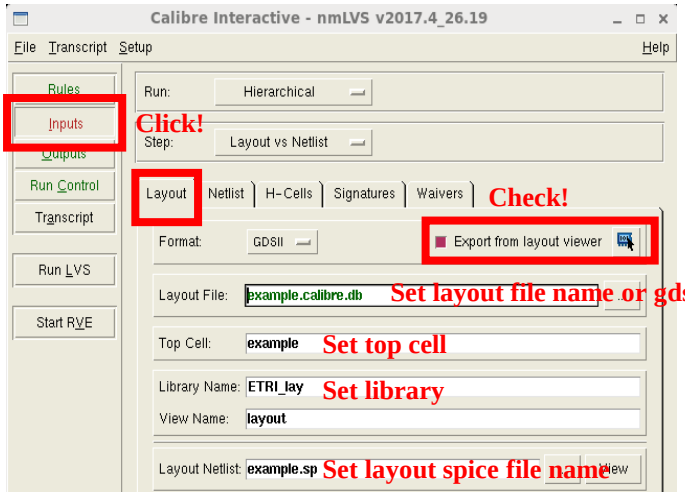
3 Load LVS rules file (ETRI_0p5um_Analog_CMOS_2P3M_5V_LVS.cal)



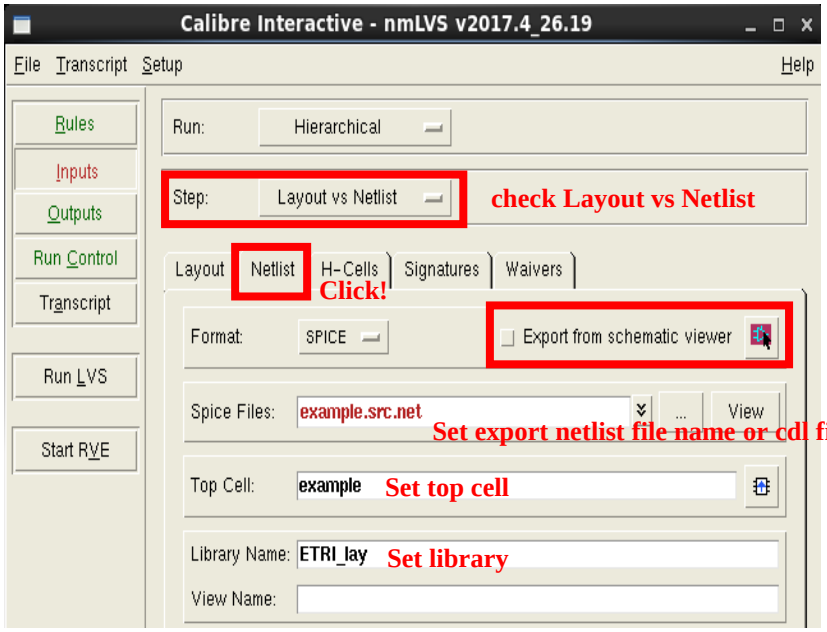
3 Load LVS rules file.



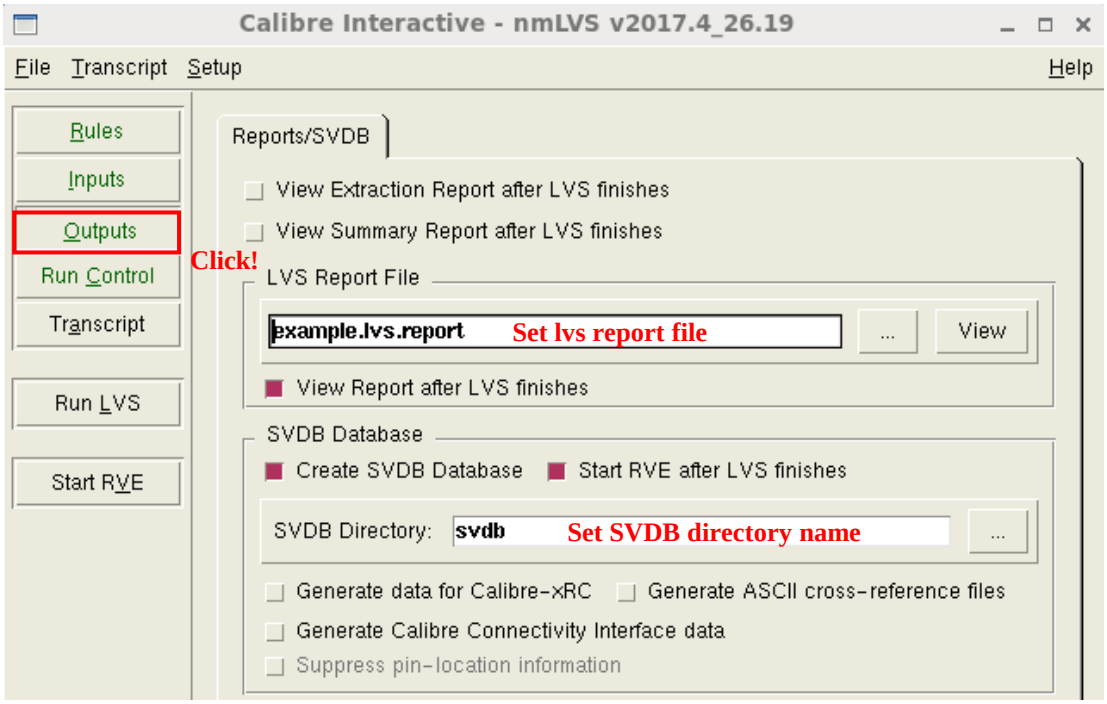
4 Set layout Input data. If you checked Export from layout viewer, insert layout file name to layout file. Not checked, Input your gds name want to run.



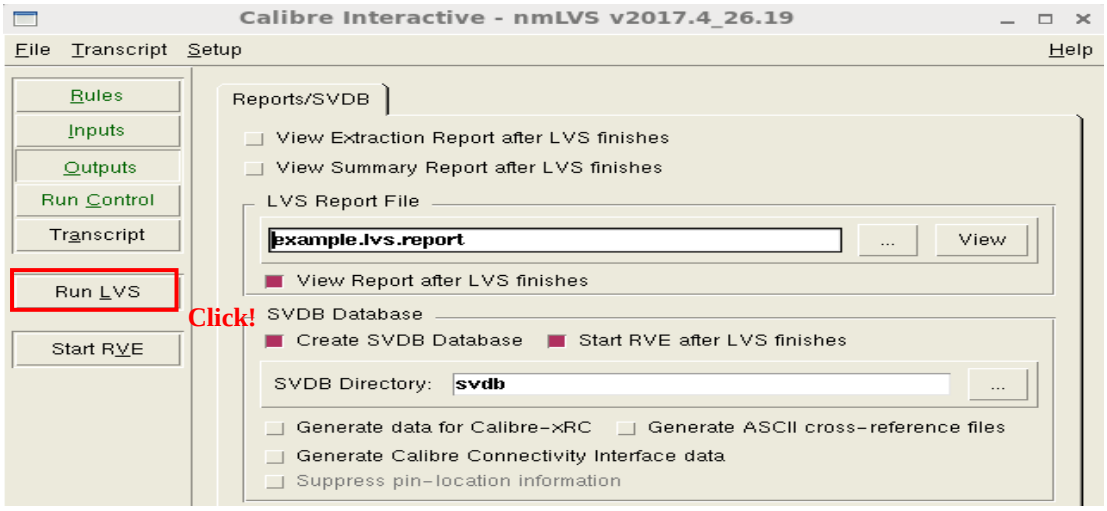
4 Set schematic Input data. If you checked Export from schematic viewer, insert layout file name to Sice files.
Not checked, Input your netlist name want to run.



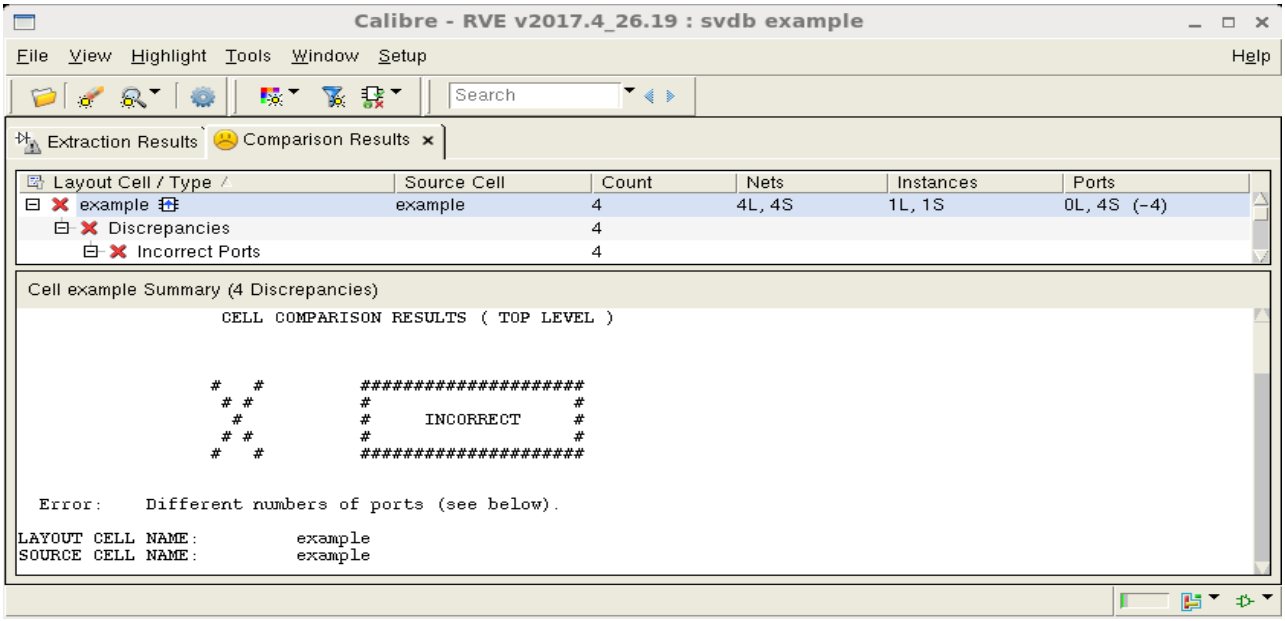
5 Set LVS outputs



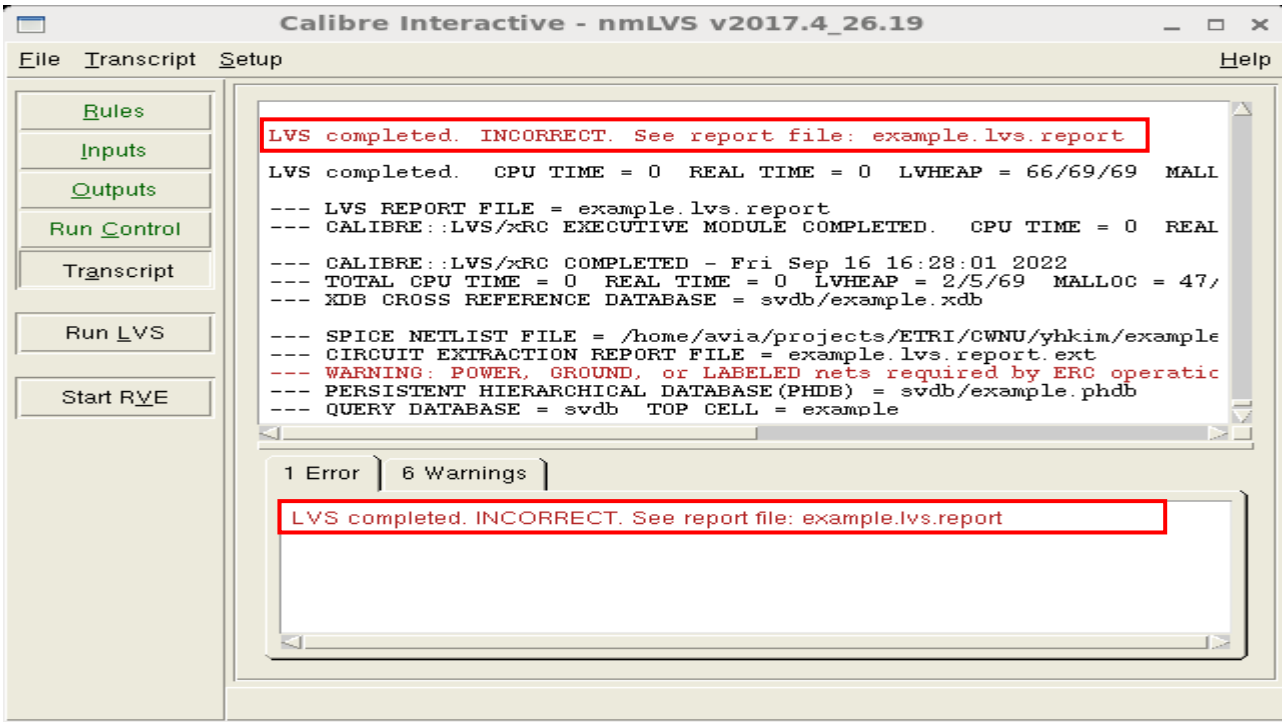
6 Run LVS



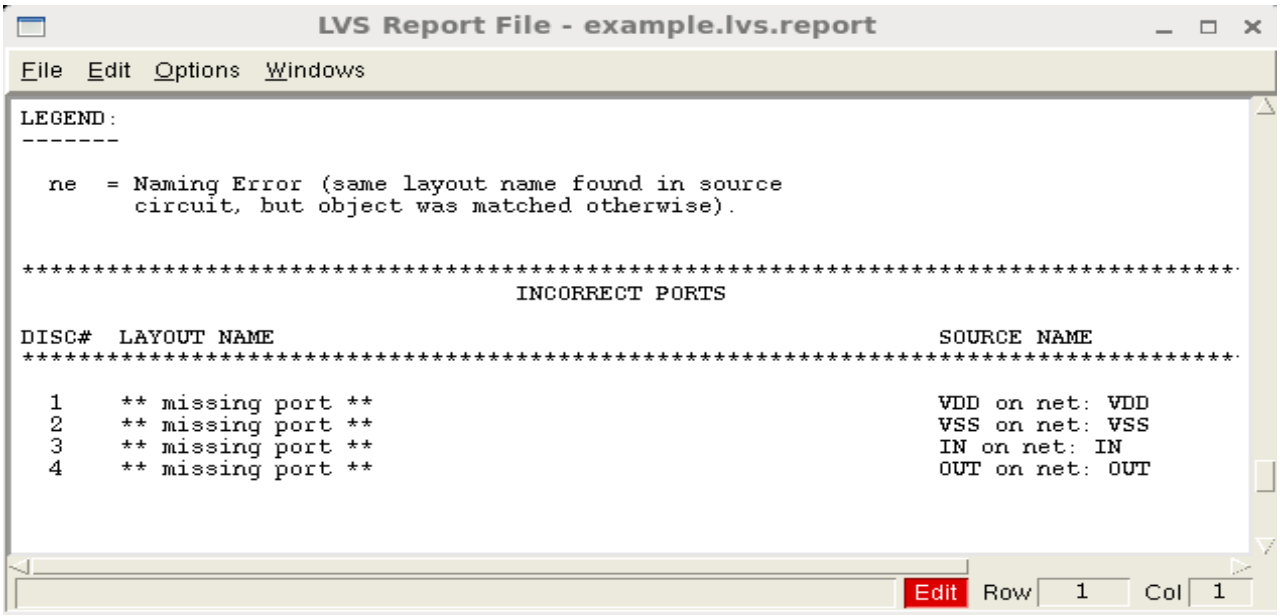
7 Get results(RVE)



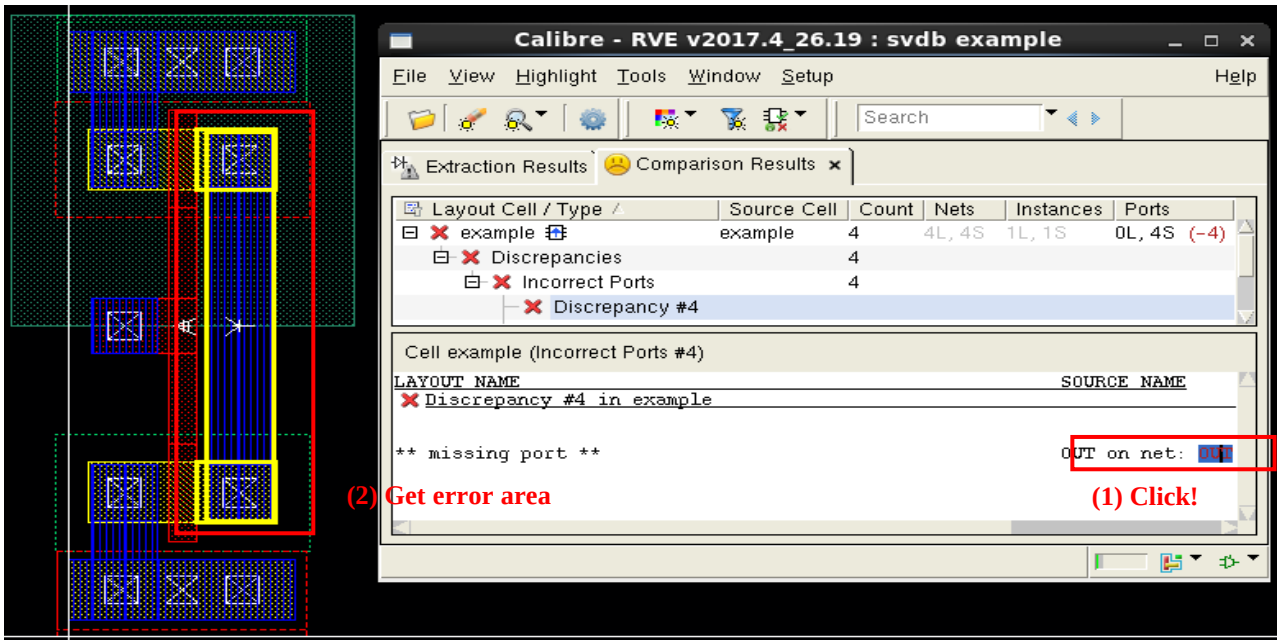
7 Get results(Transcript)



7 Get results(report)

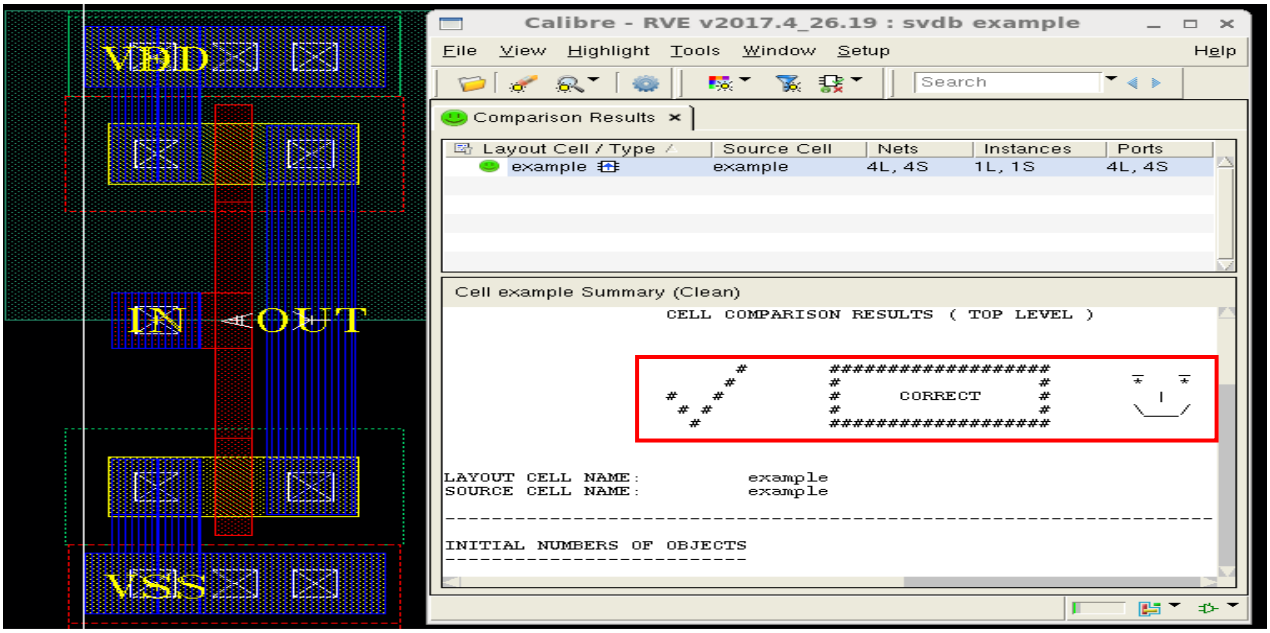


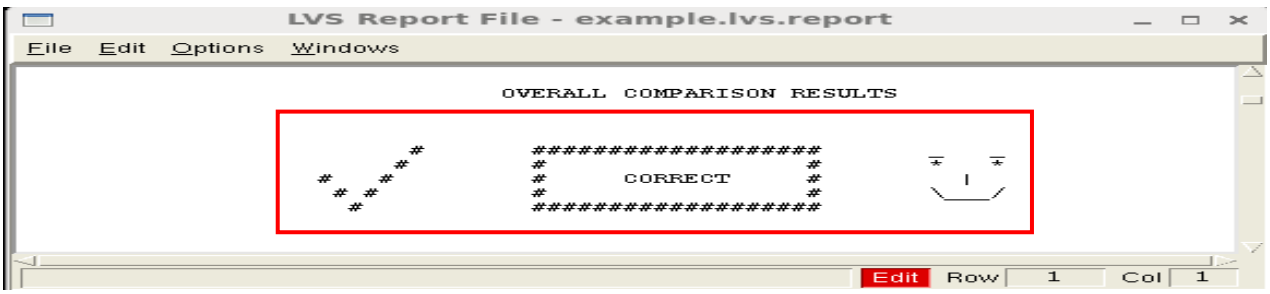
8 Run lvs

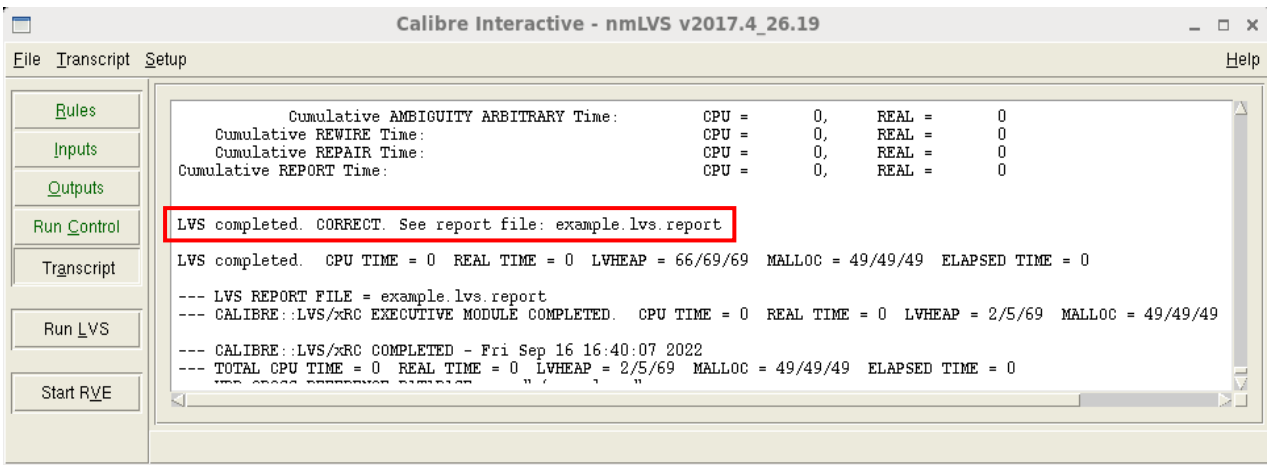


- After correct LVS errors, run again LVS.

9 Check error results







10.2 Script options

- In running LVS, you can use several options for convenience.
  if you need, modify this comment in the lvs_header.cal.

- Before run lvs, you have to modify script file(lvs_header.cal) some parts below.

LAYOUT PATH “[gds_path]/[CELLNAME.gds]“
    gds_path : the directory where layout gds file is existed.
    CELLNAME.gds : put in your gds file
LAYOUT PRIMARY “[CELLPRIMARY]“
    Layout database topcell for running lvs.
LAYOUT SYSTEM [GDSII or OASIS]
    You can choose layout data type GDSII or OASIS
SOURCE PATH “[cdl_path]/[CELLNAME.cdl]“
    cdl_path : the directory where schematic cdl file is exist
    CELLNAME.cdl : put in your cdl file
SOURCE PRIMARY “[CELLPRIMARY]“
    Schematic database topcell for running lvs.
SOURCE SYSTEM SPICE

ERC RESULTS DATABASE “[ERC_DB]" ASCII
  Set ERC DB name and format
ERC SUMMARY REPORT “[ERCSUMMARY]“
  Set ERC summary report name
ERC MAXIMUM RESULTS 100
    Set ERC maximum error counts

INCLUDE "[rule_path]/ETRI_0p5um_Analog_CMOS_2P3M_5V_LVS.cal “
  path that rule file is exist.

- Example lvs_header.cal

```
LAYOUT PRIMARY "test"  Layout primary cell name
LAYOUT PATH "test.gds"  Layout gds file name for LVS
LAYOUT SYSTEM GDSII  Select layout system GDSII or OASIS

SOURCE PRIMARY "test"  Schematic primary cell name
SOURCE PATH "test.cdl"  Schematic cdl file name for LVS
SOURCE SYSTEM SPICE  Select source system SPICE

DRC RESULTS DATABASE "drc.db" ASCII // ASCII or GDSII  Set DRC result file name
DRC SUMMARY REPORT "drc.sum"  Set DRC summary report name

LVS REPORT "lvs.rep"  List of groups
LVS REPORT MAXIMUM 1000 // ALL  Set LVS maximum error counts
LVS REPORT OPTION A B C D S V  Set LVS report option

ERC RESULTS DATABASE "erc.db" ASCII  Set ERC result file name
ERC SUMMARY REPORT "erc.sum"  Set ERC summary report name
ERC MAXIMUM RESULTS 100  Set ERC maximum error counts

INCLUDE "/   Project Directory   /ETRI/LVS/ETRI_0p5um_Analog_CMOS_2P3M_5V_LVS.cal"
                                                                  Include LVS rule path
```

- If you want to run lvs in terminal, you can use command described below.

Command: calibre –lvs –hier lvs_header.cal

- If you want to see results at RVE in terminal, you can use command described below.

Command: calibre –rve –lvs [SVDB directory]
ex) calibre –rve –lvs svdb

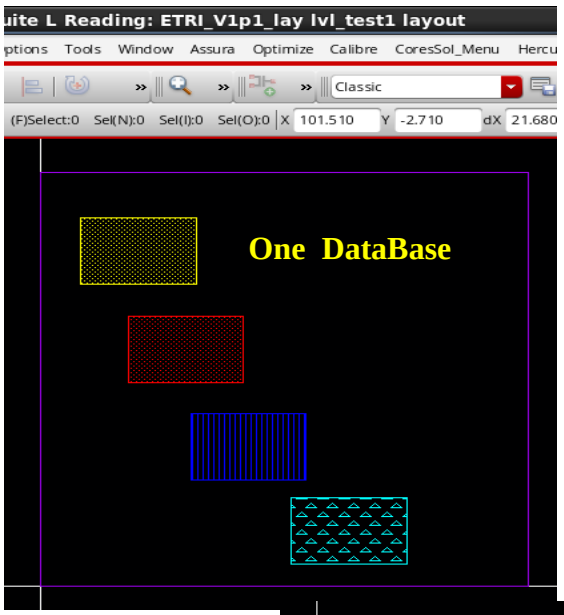
※ LVS virtual connection option is set Yes. If you don't want virtual connect, Please set "VIRTUAL CONNECT COLON" to "NO" in LVS rule file.
※ LVS REDUCE PARALLEL/SERIES CAPACITORS option is set NO in LVS rule file. please do not change this option for exact LVS verification.

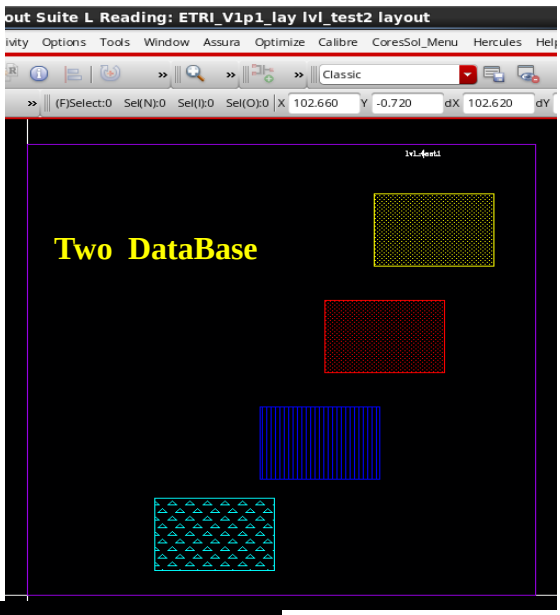
FILE NAME: ETRI_0p5um_Analog_CMOS_2P3M_5V_LVS.cal

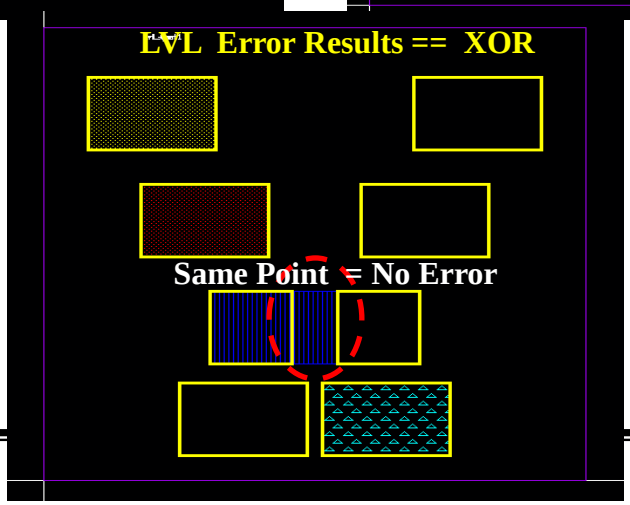
11. Calibre LVL

11.1 LVL (Layout Versus Layout) Verification

- Distributes of the two input data that are not equal to each other as errors.
- Calibre has the Capability to compare two separate Layout Database
- When comparing two layout database :
  * Specify One of the Database Using
    - LAYOUT SYSTEM
    - LAYOUT PATH
    - LAYOUT PRIMARY
  * Specify the other Database Using
    - LAYOUT SYSTEM2
    - LAYOUT PATH2
    - LAYOUT PRIMARY2







A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

11.2 Script Option

- In running LVL, you can use several options for convenience.
  if you need, modify this comment in the lvl_header.cal

option	value	comment
LAYOUT SYSTEM	GDSII OASIS	1st Input : Select layout data format GDSII or OASIS
LAYOUT SYSTEM2	GDSII OASIS	2nd Input : Select layout data format GDSII or OASIS
LAYOUT BUMP2	Number > 1st DB	Increments 2nd Layout Data Base Layer Number by Specified Value
DRC RESULTS DATABASE	*Filename*[*type*]	Specifies the filename and type of the results database
DRC SUMMARY REPORT	*Filename*	Specifies the DRC Summary report File

- Before run lvl, you have to modify script file(lvl_header.cal) some parts below.

LAYOUT PATH "[gds_path]/[CELLNAME.gds]"
  gds_path : the directory where layout 1st gds file is exist
  CELLNAME.gds : put in your gds file
LAYOUT PRIMARY "[CELLPRIMARY]"
  Layout database 1st topcell for running drc.
LAYOUT PATH**2** "[gds_path]/[CELLNAME.gds]"
  gds_path : the directory where layout 2nd gds file is exist
  CELLNAME.gds : put in your gds file
LAYOUT PRIMARY**2** "[CELLPRIMARY]"
  Layout database 2nd topcell for running drc

INCLUDE "[rule_path]/ETRI_0p5um_Analog_CMOS_2P3M_5V_LVL.cal "
  path that rule file is exist.

- If you want to run lvl in terminal, you can use command described below.

11.2 Script Option

- Example lvl_header.cal

```
LAYOUT SYSTEM GDSII                          1st : Select layout system GDSII or OASIS
LAYOUT PATH "lvl_test1.gds"                  1st : Layout gds file name for LVL
LAYOUT PRIMARY "lvl_test1"                   1st : Layout primary cell name

LAYOUT SYSTEM2 GDSII                         2nd : Select layout system GDSII or OASIS
LAYOUT PATH2 "lvl_test2.gds"                 2nd : Layout gds file name for LVL
LAYOUT PRIMARY2 "lvl_test2"                  2nd : Layout primary cell name
LAYOUT BUMP2 2500                            Set Number of 2nd GDS Number

DRC RESULTS DATABASE "lvl.db" ASCII          Set LVL result file name
DRC SUMMARY REPORT "lvl.sum"                 Set LVL summary report name

INCLUDE "./ETRI_0p5um_Analog_CMOS_2P3M_5V_LVL.cal"        LVL rule path
```

- If you want to run drc in terminal, you can use command described below.

Command: calibre –drc –hier lvl_header.cal

- If you want to see results at RVE in terminal, you can use command described below.

Command: calibre –rve –drc [DRC RESULTS DATABASE]
ex) calibre –rve –drc TOPCELL.db