

Built-in Steps and their Configuration Variables

These steps are included with OpenLane and are used by its various built-in flows.

This page documents these steps, how to get them and their configuration variables (if applicable).

If you're looking for documentation for the `Step` Python classes themselves, check the API reference [here](#).

Warnings

- Two steps in a given Flow may share a configuration variable name if-and-only-if the variables are otherwise identical, i.e., the name, type, and default value all match. Otherwise, the flow will not compile.
- Some steps have a variable prefixed with `RUN_` that enables or disables said step. This is a vestige from OpenLane 1 and it is recommended to explicitly specify your flow either by using the API or in your JSON configuration file's `meta` object.

Notes

- `?` indicates an optional variable, i.e., a value that may hold a value of `None`. OpenLane steps are expected to understand that these values are optional and behave accordingly.
- Variable names denoted ^(PDK) are expected to be declared by the PDK.
If a PDK does not define one of the required variables, it is considered to be incompatible with this step.

Tip

For a table of contents, press the following button on the top-right corner of the page: 

Checker

Disconnected Pins Checker

Raises an immediate error if critical disconnected pins (metric:

`design_critical_disconnected_pin_count`) are ≥ 0 . Doesn't raise an error depending on `error_on_var` if defined.

Importing



Configuration Variables

Variable Name	Type	Description	Default	Units
ERROR_ON_DISCONNECTED_PINS	bool	Checks for disconnected instance pins after detailed routing and quits immediately if so.	True	

Hold Timing Violations Checker

Raises a deferred error if NotImplemented (metric: `timing_hold_vio_count`) are ≥ 0 . Doesn't raise an error depending on `error_on_var` if defined.

Importing



Configuration Variables

Variable Name	Type	Description	Default	Units
TIMING_VIOLATION_CORNERS	List[str]	A list of wildcards matching IPVT corners to use during checking for timing violations.	['*tt*']	
HOLD_VIOLATION_CORNERS	List[str]?	A list of wildcards matching IPVT corners to use during checking for hold violations.	None	

Spice Extraction-based Illegal Overlap Checker

Raises a deferred error if Magic Illegal Overlap errors (metric: `magic_illegal_overlap_count`) are ≥ 0 . Doesn't raise an error depending on `error_on_var` if defined.

Importing



Configuration Variables

Variable Name	Type	Description	Default	Units
ERROR_ON_ILLEGAL_OVERLAPS	bool	Checks for illegal overlaps during Magic extraction. In some cases, these imply existing undetected shorts in the design. It raises an error at the end of the flow if so.	True	

KLayout Design Rule Checker

Raises a deferred error if KLayout DRC errors (metric: `klayout_drc_error_count`) are ≥ 0 . Doesn't raise an error depending on `error_on_var` if defined.

Importing



Configuration Variables

Variable Name	Type	Description	Default	Units
<code>ERROR_ON_KLAYOUT_DRC</code>	bool	Checks for DRC violations after KLayout DRC is executed and exits the flow if any was found.	True	

Layout vs. Schematic Error Checker

Raises a deferred error if LVS errors (metric: `design_lvs_error_count`) are ≥ 0 . Doesn't raise an error depending on `error_on_var` if defined.

Importing



Configuration Variables

Variable Name	Type	Description	Default	Units
<code>ERROR_ON_LVS_ERROR</code>	bool	Checks for LVS errors after Netgen is executed. If any exist, it raises an error at the end of the flow.	True	

Lint Errors Checker

Raises an immediate error if Lint errors (metric: `design_lint_error_count`) are ≥ 0 . Doesn't raise an error depending on `error_on_var` if defined.

Importing



Configuration Variables

Variable Name	Type	Description	Default	Units
<code>ERROR_ON_LINTER_ERRORS</code>	bool	Quit immediately on any linter errors.	True	

Lint Timing Errors Checker

Raises an immediate error if Lint Timing Errors (metric: `design_lint_timing_construct_count`) are ≥ 0 . Doesn't raise an error depending on `error_on_var` if defined.

Importing



Configuration Variables

Variable Name	Type	Description	Default	Units
<code>ERROR_ON_LINTER_TIMING_CONSTRUCTS</code>	bool	Quit immediately on any discovered timing constructs during linting.	True	

Lint Warnings Checker

Raises an immediate error if Lint warnings (metric: `design_lint_warning_count`) are ≥ 0 . Doesn't raise an error depending on `error_on_var` if defined.

Importing



Configuration Variables

Variable Name	Type	Description	Default	Units
<code>ERROR_ON_LINTER_WARNINGS</code>	bool	Raise an error immediately on any linter warnings.	False	

Magic Design Rule Checker

Raises a deferred error if Magic DRC errors (metric: `magic_drc_error_count`) are ≥ 0 . Doesn't raise an error depending on `error_on_var` if defined.

Importing



Configuration Variables

Variable Name	Type	Description	Default	Units
<code>ERROR_ON_MAGIC_DRC</code>	bool	Checks for DRC violations after magic DRC is executed and exits the flow if any was found.	True	

Maximum Capacitance Violations Checker

Raises a deferred error if NotImplemented (metric: `design_max_capViolationCount`) are ≥ 0 . Doesn't raise an error depending on `error_on_var` if defined.

Importing

Configuration Variables

Variable Name	Type	Description	Default	Units
<code>TIMING_VIOLATION_CORNERS</code>	List[str]	A list of wildcards matching IPVT corners to use during checking for timing violations.	<code>['*tt*']</code>	
<code>MAX_CAP_VIOLATION_CORNERS</code>	List[str]?	A list of wildcards matching IPVT corners to use during checking for max cap violations.	<code>['']</code>	

Maximum Slew Violations Checker

Raises a deferred error if NotImplemented (metric: `design_max_slewViolationCount`) are ≥ 0 . Doesn't raise an error depending on `error_on_var` if defined.

Importing

Configuration Variables

Variable Name	Type	Description	Default	Units
<code>TIMING_VIOLATION_CORNERS</code>	List[str]	A list of wildcards matching IPVT corners to use during checking for timing violations.	<code>['*tt*']</code>	
<code>MAX_SLEW_VIOLATION_CORNERS</code>	List[str]?	A list of wildcards matching IPVT corners to use during checking for max slew violations.	<code>['']</code>	

Netlist Assign Statement Checker

Raises a StepError if the Netlist has an `assign` statement in it.

`assign` statements are known to cause bugs in some PnR tools.

Importing

Inputs and Outputs

Inputs	Outputs
Verilog Netlist (.nl.v)	

Configuration Variables

Variable Name	Type	Description	Default	Units
ERROR_ON_NL_ASSIGN_STATEMENTS	bool	Whether to emit an error or simply warn about the existence	True	

Power Grid Violation Checker

Raises a deferred error if power grid violations (as reported by OpenROAD PSM- you may ignore these if LVS passes) (metric: `design_power_gridViolation_count`) are ≥ 0 . Doesn't raise an error depending on `error_on_var` if defined.

Importing



Configuration Variables

Variable Name	Type	Description	Default	Units
ERROR_ON_PDN_VIOLATIONS	bool	Checks for unconnected nodes in the power grid. If any exists, an error is raised at the end of the flow.	True	

Setup Timing Violations Checker

Raises a deferred error if `NotImplemented` (metric: `timing_setup_vio_count`) are ≥ 0 . Doesn't raise an error depending on `error_on_var` if defined.

Importing



Configuration Variables

Variable Name	Type	Description	Default	Units
TIMING_VIOLATION_CORNERS	List[str]	A list of wildcards matching IPVT corners to use during checking for timing violations.	['*tt*']	
SETUP_VIOLATION_CORNERS	List[str]?	A list of wildcards matching IPVT corners to use during checking for setup violations.	None	

Routing Design Rule Checker

Raises a deferred error if Routing DRC errors (metric: `route_drc_errors`) are ≥ 0 . Doesn't raise an error depending on `error_on_var` if defined.

Importing



Configuration Variables

Variable Name	Type	Description	Default	Units
ERROR_ON_TR_DRC	bool	Checks for DRC violations after routing and exits the flow if any was found.	True	

Wire Length Threshold Checker

Raises a deferred error if Threshold-surpassing long wires (metric: `route_wielength_max`) are \geq the threshold specified in the configuration file.. Doesn't raise an error depending on `error_on_var` if defined.

Importing



Configuration Variables

Variable Name	Type	Description	Default	Units
ERROR_ON_LONG_WIRE	bool	Checks if any wire length exceeds the threshold set in the PDK. If so, an error is raised at the end of the flow.	True	

Magic vs. KLayout XOR Difference Checker

Raises a deferred error if XOR differences (metric: `design_xor_difference_count`) are ≥ 0 . Doesn't raise an error depending on `error_on_var` if defined.

Importing

Configuration Variables

Variable Name	Type	Description	Default	Units
ERROR_ON_XOR_ERROR	bool	Checks for geometric differences between the Magic and KLayout stream-outs. If any exist, raise an error at the end of the flow.	True	

Yosys Synth Checks

Raises an immediate error if Yosys check errors (metric: `synthesis_check_error_count`) are ≥ 0 . Doesn't raise an error depending on `error_on_var` if defined.

Importing

Configuration Variables

Variable Name	Type	Description	Default	Units
ERROR_ON_SYNTH_CHECKS	bool	Quits the flow immediately if one or more synthesis check errors are flagged. This checks for combinational loops and/or wires with no drivers.	True	

Unmapped Cells Checker

Raises an immediate error if Unmapped Yosys instances (metric: `design_instance_unmapped_count`) are ≥ 0 . Doesn't raise an error depending on `error_on_var` if defined.

Importing

Configuration Variables

Variable Name	Type	Description	Default	Units
ERROR_ON_UNMAPPED_CELLS	bool	Checks for unmapped cells after synthesis and quits immediately if so.	True	

KLayout

Design Rule Check (KLayout)

Importing >

Inputs and Outputs

Inputs	Outputs
GDSII Stream (.gds)	

Configuration Variables

Variable Name	Type	Description	Default	Units
KLAYOUT_TECH ^{PDK}	Path	A path to the KLayout layer technology (.lyt) file.	None	
KLAYOUT_PROPERTIES ^{PDK}	Path	A path to the KLayout layer properties (.lyp) file.	None	
KLAYOUT_DEF_LAYER_MAP ^{PDK}	Path	A path to the KLayout LEF/DEF layer mapping (.map) file.	None	
KLAYOUT_DRC_RUNSET ^{PDK}	Path?	A path to KLayout DRC runset.	None	
KLAYOUT_DRC_OPTIONS ^{PDK}	Dict[str, (bool int)]?	Options passed directly to the KLayout DRC runset. They vary from one PDK to another.	None	
KLAYOUT_DRC_THREADS	int?	Specifies the number of threads to be used in KLayout DRCIf unset, this will be equal to your machine's thread count.	None	

Open In GUI

Opens the DEF view in the KLayout GUI, with layers loaded and mapped properly. Useful to inspect `.klayout.xml` database files and the like.

Importing >

Inputs and Outputs

Inputs	Outputs
Design Exchange Format (.def)	

Configuration Variables

Variable Name	Type	Description	Default	Units
<code>KLAYOUT_TECH</code> PDK	Path	A path to the KLayout layer technology (.lyt) file.	None	
<code>KLAYOUT_PROPERTIES</code> PDK	Path	A path to the KLayout layer properties (.lyp) file.	None	
<code>KLAYOUT_DEF_LAYER_MAP</code> PDK	Path	A path to the KLayout LEF/DEF layer mapping (.map) file.	None	
<code>KLAYOUT_EDITOR_MODE</code>	bool	Whether to run the KLayout GUI in editor mode or in viewer mode.	False	
<code>KLAYOUT_GUI_USE_GDS</code>	bool	Whether to prioritize GDS (if found) when running this step.	True	

Render Image (w/ KLayout)

Renders a PNG of the layout using KLayout.

DEF is required as an input, but if a GDS-II view exists in the input state, it will be used instead.

Importing >

Inputs and Outputs

Inputs	Outputs
Design Exchange Format (.def)	

Configuration Variables

Variable Name	Type	Description	Default	Units
<code>KLAYOUT_TECH</code> PDK	Path	A path to the KLayout layer technology (.lyt) file.	None	
<code>KLAYOUT_PROPERTIES</code> PDK	Path	A path to the KLayout layer properties (.lyp) file.	None	
<code>KLAYOUT_DEF_LAYER_MAP</code> PDK	Path	A path to the KLayout LEF/DEF layer mapping (.map) file.	None	

GDSII Stream Out (KLayout)

Converts DEF views into GDSII streams using KLayout.

The PDK must support KLayout for this step to work, otherwise it will be skipped.

If `PRIMARY_GDSII_STREAMOUT_TOOL` is set to "klayout", both GDS and KAYOUT_GDS will be updated, and if set to another tool, only `KAYOUT_GDS` will be updated.

Importing >

Inputs and Outputs

Inputs	Outputs
Design Exchange Format (.def)	GDSII Stream (.gds)
	GDSII Stream (KLayout) (.klayout.gds)

Configuration Variables

Variable Name	Type	Description	Default	Units
<code>KAYOUT_TECH</code> PDK	Path	A path to the KLayout layer technology (.lyt) file.	None	
<code>KAYOUT_PROPERTIES</code> PDK	Path	A path to the KLayout layer properties (.lyp) file.	None	
<code>KAYOUT_DEF_LAYER_MAP</code> PDK	Path	A path to the KLayout LEF/DEF layer mapping (.map) file.	None	

KLayout vs. Magic XOR

Performs an XOR operation on the Magic and KLayout GDS views. The idea is: if there's any difference between the GDSII streams between the two tools, one of them have it wrong and that may lead to ambiguity.

Importing >

Inputs and Outputs

Inputs	Outputs
GDSII Stream (Magic) (.magic.gds)	
GDSII Stream (KLayout) (.klayout.gds)	

Configuration Variables

Variable Name	Type	Description	Default	Units
<code>KLAYOUT_TECH</code> ^{PDK}	Path	A path to the KLayout layer technology (.lyt) file.	None	
<code>KLAYOUT_PROPERTIES</code> ^{PDK}	Path	A path to the KLayout layer properties (.lyp) file.	None	
<code>KLAYOUT_DEF_LAYER_MAP</code> ^{PDK}	Path	A path to the KLayout LEF/DEF layer mapping (.map) file.	None	
<code>KLAYOUT_XOR_THREADS</code>	int?	Specifies number of threads used in the KLayout XOR check. If unset, this will be equal to your machine's thread count.	None	
<code>KLAYOUT_XOR_IGNORE_LAYERS</code> ^{PDK}	List[str]?	KLayout layers to ignore during XOR operations.	None	
<code>KLAYOUT_XOR_TILE_SIZE</code> ^{PDK}	int?	A tile size for the XOR process in μm .	None	

Magic

Design Rule Checks

Performs [design rule checking](#) on the GDSII stream using Magic.

This also converts the results to a KLayout database, which can be loaded.

The metrics will be updated with `magic_drc_error_count`. You can use [the relevant checker](#) to quit if that number is nonzero.

Importing



Inputs and Outputs

Inputs	Outputs
Design Exchange Format (.def)	
GDSII Stream (.gds)	

Configuration Variables

Variable Name	Type	Description	Default	Units
MAGIC_DEF_LABELS	bool	A flag to choose whether labels are read with DEF files or not. From magic docs: "The '-labels' option to the 'def read' command causes each net in the NETS and SPECIALNETS sections of the DEF file to be annotated with a label having the net name as the label text." If LVS fails, try disabling this option.	True	
MAGIC_GDS_POLYGON_SUBCELLS	bool	A flag to enable polygon subcells in magic for gds read potentially speeding up magic. From magic docs: "Put non-Manhattan polygons. This prevents interactions with other polygons on the same plane and so reduces tile splitting."	False	
MAGIC_DEF_NO_BLOCKAGES	bool	If set to true, blockages in DEF files are ignored. Otherwise, they are read as sheets of metal by Magic.	True	
MAGIC_INCLUDE_GDS_POINTERS	bool	A flag to choose whether to include GDS pointers in the generated mag files or not.	False	
MAGICRC ^{PDK}	Path	A path to the <code>.magicrc</code> file which is sourced before running magic in the flow.	None	
MAGIC_TECH ^{PDK}	Path	A path to a Magic tech file which, mainly, has DRC rules.	None	
MAGIC_PDK_SETUP ^{PDK}	Path	A path to a PDK-specific setup file sourced by <code>.magicrc</code> .	None	
CELL_MAGS ^{PDK}	List[Path]?	A list of pre-processed concrete views for cells. Read as a fallback for undefined cells.	None	
CELL_MAGLEFS ^{PDK}	List[Path]?	A list of pre-processed abstract LEF views for cells. Read as a	None	

Variable Name	Type	Description	Default	Units
MAGIC_CAPTURE_ERRORS	bool	fallback for undefined cells in scripts where cells are black-boxed.	True	
MAGIC_DRC_USE_GDS	bool	Capture errors print by Magic and quit when a fatal error is encountered. Fatal errors are determined heuristically. It is not guaranteed that they are fatal errors. Hence this function is gated by a variable. This function is needed because Magic does not throw errors.	True	

Open In GUI

Opens the DEF view in the Magic GUI.

Importing >

Inputs and Outputs

Inputs	Outputs
Design Exchange Format (.def)	

Configuration Variables

Variable Name	Type	Description	Default	Units
MAGIC_DEF_LABELS	bool	A flag to choose whether labels are read with DEF files or not. From magic docs: "The '-labels' option to the 'def read' command causes each net in the NETS and SPECIALNETS sections of the DEF file to be annotated with a label having the net name as the label text." If LVS fails, try disabling this option.	True	
MAGIC_GDS_POLYGON_SUBCELLS	bool	A flag to enable polygon subcells in magic for gds read potentially speeding up magic. From magic docs: "Put non-Manhattan polygons. This prevents interactions with other polygons on the same plane and so reduces tile splitting."	False	
MAGIC_DEF_NO_BLOCKAGES	bool	If set to true, blockages in DEF files are ignored. Otherwise, they are read as sheets of metal by Magic.	True	
MAGIC_INCLUDE_GDS_POINTERS	bool	A flag to choose whether to include GDS pointers in the generated mag files or not.	False	
MAGICRC ^{PDK}	Path	A path to the <code>.magicrc</code> file which is sourced before running magic in the flow.	None	
MAGIC_TECH ^{PDK}	Path	A path to a Magic tech file which, mainly, has DRC rules.	None	
MAGIC_PDK_SETUP ^{PDK}	Path	A path to a PDK-specific setup file sourced by <code>.magicrc</code> .	None	
CELL_MAGS ^{PDK}	List[Path]?	A list of pre-processed concrete views for cells. Read as a fallback for undefined cells.	None	
CELL_MAGLEFS ^{PDK}	List[Path]?	A list of pre-processed abstract LEF views for cells. Read as a	None	

Variable Name	Type	Description	Default	Units
		fallback for undefined cells in scripts where cells are black-boxed.		
MAGIC_CAPTURE_ERRORS	bool	Capture errors print by Magic and quit when a fatal error is encountered. Fatal errors are determined heuristically. It is not guaranteed that they are fatal errors. Hence this function is gated by a variable. This function is needed because Magic does not throw errors.	True	
MAGIC_GUI_USE_GDS	bool	Whether to prioritize GDS (if found) when running this step.	True	

SPICE Model Extraction

Extracts a SPICE netlist from the GDSII stream. Used in Layout vs. Schematic checks.

Also, the metrics will be updated with `magic_illegal_overlap_count`. You can use [the relevant checker](#) to quit if that number is nonzero.

Importing >

Inputs and Outputs

Inputs	Outputs
GDSII Stream (.gds)	Simulation Program with Integrated Circuit Emphasis (.spice)
Design Exchange Format (.def)	

Configuration Variables

Variable Name	Type	Description	Default	Units
MAGIC_DEF_LABELS	bool	A flag to choose whether labels are read with DEF files or not. From magic docs: "The '-labels' option to the 'def read' command causes each net in the NETS and SPECIALNETS sections of the DEF file to be annotated with a label having the net name as the label text." If LVS fails, try disabling this option.	True	
MAGIC_GDS_POLYGON_SUBCELLS	bool	A flag to enable polygon subcells in magic for gds read potentially speeding up magic. From magic docs: "Put non-Manhattan polygons. This prevents interactions with other polygons on the same plane and so reduces tile splitting."	False	
MAGIC_DEF_NO_BLOCKAGES	bool	If set to true, blockages in DEF files are ignored. Otherwise, they are read as sheets of metal by Magic.	True	
MAGIC_INCLUDE_GDS_POINTERS	bool	A flag to choose whether to include GDS pointers in the generated mag files or not.	False	
MAGICRC ^{PDK}	Path	A path to the <code>.magicrc</code> file which is sourced before running magic in the flow.	None	
MAGIC_TECH ^{PDK}	Path	A path to a Magic tech file which, mainly, has DRC rules.	None	
MAGIC_PDK_SETUP ^{PDK}	Path	A path to a PDK-specific setup file sourced by <code>.magicrc</code> .	None	
CELL_MAGS ^{PDK}	List[Path]?	A list of pre-processed concrete views for cells. Read as a fallback for undefined cells.	None	
CELL_MAGLEFS ^{PDK}	List[Path]?	A list of pre-processed abstract LEF views for cells. Read as a	None	

Variable Name	Type	Description	Default	Units
		fallback for undefined cells in scripts where cells are black-boxed.		
MAGIC_CAPTURE_ERRORS	bool	Capture errors print by Magic and quit when a fatal error is encountered. Fatal errors are determined heuristically. It is not guaranteed that they are fatal errors. Hence this function is gated by a variable. This function is needed because Magic does not throw errors.	True	
MAGIC_EXT_USE_GDS	bool	A flag to choose whether to use GDS for spice extraction or not. If not, then the extraction will be done using the DEF/LEF, which is faster.	False	
MAGIC_EXT_ABSTRACT_CELLS	List[str]?	A list of regular expressions which are matched against the cells of a the design. Matches are abstracted (black-boxed) during SPICE extraction.	None	
MAGIC_NO_EXT_UNIQUE	bool	Enables connections by label in LVS by skipping <code>extract unique</code> in Magic extractions.	False	
MAGIC_EXT_SHORT_RESISTOR	bool	Enables adding resistors to shorts-resolves LVS issues if more than one top-level pin is connected to the same net, but may increase runtime and break some designs. Proceed with caution.	False	
MAGIC_EXT_ABSTRACT	bool	Extracts a SPICE netlist based on black-boxed standard cells and macros (basically, anything with a LEF) rather than transistors. An error will be thrown if both this and <code>MAGIC_EXT_USE_GDS</code> is set to True .	False	

GDSII Stream Out (Magic)

Converts DEF views into GDSII streams using Magic.

If `PRIMARY_GDSII_STREAMOUT_TOOL` is set to `"magic"`, both GDS and MAG_GDS will be updated, and if set to another tool, only `MAG_GDS` will be updated.

Importing >

Inputs and Outputs

Inputs	Outputs
Design Exchange Format (.def)	GDSII Stream (.gds)
	GDSII Stream (Magic) (.magic.gds)
	Magic VLSI View (.mag)

Configuration Variables

Variable Name	Type	Description	Default	Units
MAGIC_DEF_LABELS	bool	A flag to choose whether labels are read with DEF files or not. From magic docs: "The '-labels' option to the 'def read' command causes each net in the NETS and SPECIALNETS sections of the DEF file to be annotated with a label having the net name as the label text." If LVS fails, try disabling this option.	True	
MAGIC_GDS_POLYGON_SUBCELLS	bool	A flag to enable polygon subcells in magic for gds read potentially speeding up magic. From magic docs: "Put non-Manhattan polygons. This prevents interations with other polygons on the same plane and so reduces tile splitting."	False	
MAGIC_DEF_NO_BLOCKAGES	bool	If set to true, blockages in DEF files are ignored. Otherwise, they are read as sheets of metal by Magic.	True	
MAGIC_INCLUDE_GDS_POINTERS	bool	A flag to choose whether to include GDS pointers in the generated mag files or not.	False	
MAGICRC PDK	Path	A path to the <code>.magicrc</code> file which is sourced before running magic in the flow.	None	
MAGIC_TECH PDK	Path	A path to a Magic tech file which, mainly, has DRC rules.	None	
MAGIC_PDK_SETUP PDK	Path	A path to a PDK-specific setup file sourced by	None	

Variable Name	Type	Description	Default	Units
		.magicrc .		
CELL_MAGS PDK	List[Path]?	A list of pre-processed concrete views for cells. Read as a fallback for undefined cells.	None	
CELL_MAGLEFS PDK	List[Path]?	A list of pre-processed abstract LEF views for cells. Read as a fallback for undefined cells in scripts where cells are black-boxed.	None	
MAGIC_CAPTURE_ERRORS	bool	Capture errors print by Magic and quit when a fatal error is encountered. Fatal errors are determined heuristically. It is not guaranteed that they are fatal errors. Hence this function is gated by a variable. This function is needed because Magic does not throw errors.	True	
DIE_AREA	Tuple[Decimal, Decimal, Decimal, Decimal]?	Specific die area to be used in floorplanning when FP_SIZING is set to absolute . Specified as a 4-corner rectangle "x0 y0 x1 y1".	None	µm
MAGIC_ZEROIZE_ORIGIN	bool	A flag to move the layout such that its origin in the lef generated by magic is 0,0.	False	
MAGIC_DISABLE_CIF_INFO	bool	A flag to disable writing Caltech Intermediate Format (CIF) hierarchy and subcell array information to the GDSII file.	True	
MAGIC_MACRO_STD_CELL_SOURCE	'PDK' 'macro'	If set to PDK, magic will use the PDK definition of the	macro	

Variable Name	Type	Description	Default	Units
		STD cells for macros inside the design. Otherwise, the macro is completely treated as a blackbox and magic will use the existing cell definition inside the macro gds. This mode is only supported for macros specified in MACROS variable		

Write LEF (Magic)

Writes a LEF view of the design using the GDS using Magic.

Importing >

Inputs and Outputs

Inputs	Outputs
GDSII Stream (.gds)	Library Exchange Format (.lef)
Design Exchange Format (.def)	

Configuration Variables

Variable Name	Type	Description	Default	Units
MAGIC_DEF_LABELS	bool	A flag to choose whether labels are read with DEF files or not. From magic docs: "The '-labels' option to the 'def read' command causes each net in the NETS and SPECIALNETS sections of the DEF file to be annotated with a label having the net name as the label text." If LVS fails, try disabling this option.	True	
MAGIC_GDS_POLYGON_SUBCELLS	bool	A flag to enable polygon subcells in magic for gds read potentially speeding up magic. From magic docs: "Put non-Manhattan polygons. This prevents interactions with other polygons on the same plane and so reduces tile splitting."	False	
MAGIC_DEF_NO_BLOCKAGES	bool	If set to true, blockages in DEF files are ignored. Otherwise, they are read as sheets of metal by Magic.	True	
MAGIC_INCLUDE_GDS_POINTERS	bool	A flag to choose whether to include GDS pointers in the generated mag files or not.	False	
MAGICRC ^{PDK}	Path	A path to the <code>.magicrc</code> file which is sourced before running magic in the flow.	None	
MAGIC_TECH ^{PDK}	Path	A path to a Magic tech file which, mainly, has DRC rules.	None	
MAGIC_PDK_SETUP ^{PDK}	Path	A path to a PDK-specific setup file sourced by <code>.magicrc</code> .	None	
CELL_MAGS ^{PDK}	List[Path]?	A list of pre-processed concrete views for cells. Read as a fallback for undefined cells.	None	
CELL_MAGLEFS ^{PDK}	List[Path]?	A list of pre-processed abstract LEF views for cells. Read as a	None	

Variable Name	Type	Description	Default	Units
		fallback for undefined cells in scripts where cells are black-boxed.		
MAGIC_CAPTURE_ERRORS	bool	Capture errors print by Magic and quit when a fatal error is encountered. Fatal errors are determined heuristically. It is not guaranteed that they are fatal errors. Hence this function is gated by a variable. This function is needed because Magic does not throw errors.	True	
MAGIC_LEF_WRITE_USE_GDS	bool	A flag to choose whether to use GDS for LEF writing. If not, then the extraction will be done using abstract LEF views.	False	
MAGIC_WRITE_FULL_LEF	bool	A flag to specify whether or not the output LEF should include all shapes inside the macro or an abstracted view of the macro LEF view via magic.	False	
MAGIC_WRITE_LEF_PINONLY	bool	If true, the LEF write will mark only areas that are port labels as pins, while marking the rest of each related net as an obstruction. Otherwise, the labeled port and the any connected metal on the same layer are marked as a pin.	False	

Netgen

Netgen LVS

Performs [Layout vs. Schematic](#) checks on the extracted SPICE netlist versus a Verilog netlist with power connections.

This verifies the following:

- * There are no unexpected shorts in the final layout.
- * There are no unexpected opens in the final layout.
- * All signals are connected correctly.

Importing**Inputs and Outputs**

Inputs	Outputs
Simulation Program with Integrated Circuit Emphasis (.spice)	
Powered Verilog Netlist (.pnl.v)	

Configuration Variables

Variable Name	Type	Description	Default	Units
MAGIC_EXT_USE_GDS	bool	A flag to choose whether to use GDS for spice extraction or not. If not, then the extraction will be done using the DEF/LEF, which is faster.	False	
NETGEN_SETUP ^{PDK}	Path	A path to the setup file for Netgen used to configure LVS. If set to None, this PDK will not support Netgen-based steps.	None	
LVS_INCLUDE_MARCO_NETLISTS	bool	A flag that enables including the gate-level netlist of macros while running Netgen	False	
LVS_FLATTEN_CELLS	List[str]?	A list of cell names to be flattened while running LVS	None	

Odb**Add PDN obstructions****Importing****Inputs and Outputs**

Inputs	Outputs
OpenDB Database (.odb)	OpenDB Database (.odb)
	Design Exchange Format (.def)

Configuration Variables

Variable Name	Type	Description	Default	Units
PDN_OBSTRUCTIONS	List[str]?	Add routing obstructions to the design before PDN stage. If set to <code>None</code> , this step is skipped. Format of each obstruction item is: layer llx lly urx ury.	None	μm

Add Obstructions

Importing



Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	OpenDB Database (.odb)
	Design Exchange Format (.def)

Configuration Variables

Variable Name	Type	Description	Default	Units
ROUTING_OBSTRUCTIONS	List[str]?	Add routing obstructions to the design. If set to <code>None</code> , this step is skipped. Format of each obstruction item is: layer llx lly urx ury.	None	μm

Apply DEF Template

Copies the floorplan of a “template” DEF file for a new design, i.e., it will copy the die area, core area, and non-power pin names and locations.

Importing



Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	OpenDB Database (.odb)
	Design Exchange Format (.def)

Configuration Variables

Variable Name	Type	Description	Default	Units
FP_DEF_TEMPLATE	Path?	Points to the DEF file to be used as a template.	None	
FP_TEMPLATE_MATCH_MODE	'strict' 'permissive'	Whether to require that the pin set of the DEF template and the design should be identical. In permissive mode, pins that are in the design and not in the template will be excluded, and vice versa.	strict	
FP_TEMPLATE_COPY_POWER_PINS	bool	Whether to <i>always</i> copy all power pins from the DEF template to the design.	False	

Check Antenna Properties of Pins in The Generated Design LEF view

Importing >

Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	
Library Exchange Format (.lef)	

Check Antenna Properties of Macros Pins in Their LEF Views

Importing >

Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	

Custom I/O Pin Placement Script

Places I/O pins using a custom script, which uses a “pin order configuration” file.

Check the reference documentation for the structure of said file.

Importing >

Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	OpenDB Database (.odb)
	Design Exchange Format (.def)

Configuration Variables

Variable Name	Type	Description	Default	Units
FP_IO_VEXTEND	Decimal	Extends the vertical io pins outside of the die by the specified units.	0	µm
FP_IO_HEXTEND	Decimal	Extends the horizontal io pins outside of the die by the specified units.	0	µm
FP_IO_VTHICKNESS_MULT	Decimal	A multiplier for vertical pin thickness. Base thickness is the pins layer min width.	2	
FP_IO_HTHICKNESS_MULT	Decimal	A multiplier for horizontal pin thickness. Base thickness is the pins layer min width.	2	
FP_IO_VLENGTH ^{PDK}	Decimal?	The length of the pins with a north or south orientation. If unspecified by a PDK, the script will use whichever is higher of the following two values: * The pin width * The minimum value satisfying the minimum	None	µm

Variable Name	Type	Description	Default	Units
<code>FP_IO_HLENGTH</code> ^{PDK}	Decimal?	<p>area constraint given the pin width</p> <p>The length of the pins with an east or west orientation. If unspecified by a PDK, the script will use whichever is higher of the following two values:</p> <ul style="list-style-type: none"> * The pin width * The minimum value satisfying the minimum area constraint given the pin width 	None	μm
<code>FP_PIN_ORDER_CFG</code>	Path?	<p>Path to the configuration file. If set to <code>None</code>, this step is skipped.</p>	None	
<code>ERRORS_ON_UNMATCHED_IO</code>	'none' 'unmatched_design' 'unmatched_cfg' 'both'	<p>Controls whether to emit an error in: no situation, when pins exist in the design that do not exist in the config file, when pins exist in the config file that do not exist in the design, and both respectively.</p> <p><code>both</code> is</p>	unmatched_design	

Variable Name	Type	Description	Default	Units
		recommended, as the default is only for backwards compatibility with OpenLane 1.		

Diodes on Ports Protection Routine

Unconditionally inserts diodes on design ports diodes on ports, to mitigate the [antenna effect](#).

Useful for hardening macros, where ports may get long wires that are unaccounted for when hardening a top-level chip.

The placement is legalized by performing detailed placement and global routing after inserting the diodes.

Prior to beta 16, this step did not legalize its placement: if you would like to retain the old behavior without legalization, try `Odb.PortDiodePlacement`.

Importing

Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	Powered Verilog Netlist (.pnl.v)
	Design Constraints (.sdc)
	OpenDB Database (.odb)
	Verilog Netlist (.nl.v)
	Design Exchange Format (.def)

Configuration Variables

Variable Name	Type	Description	Default	Units
DIODE_ON_PORTS	'none' 'in' 'out' 'both'	Always insert diodes on ports with the specified polarities.	none	
GPL_CELL_PADDING <small>PDK</small>	Decimal	Cell padding value (in sites) for global placement. Used by this step only to emit a warning if it's 0.	None	sites
PDN_CONNECT_MACROS_TO_GRID	bool	Enables the connection of macros to the top level power grid.	True	
PDN_MACRO_CONNECTIONS	List[str]?	Specifies explicit power connections of internal macros to the top level power grid, in the format: regex matching macro instance names, power domain vdd and ground net names, and macro vdd and ground pin names <pre><instance_name_rx> <vdd_net> <gnd_net> <vdd_pin> <gnd_pin>.</pre>	None	
PDN_ENABLE_GLOBAL_CONNECTIONS	bool	Enables the creation of global connections in PDN generation.	True	
PNR_SDC_FILE	Path?	Specifies the SDC file used during all implementation (PnR) steps	None	
FP_DEF_TEMPLATE	Path?	Points to the DEF file to be used as a template.	None	
PL_OPTIMIZE_MIRRORING	bool	Specifies whether or not to run an optimize_mirroring pass whenever detailed placement happens. This pass will mirror the cells	True	

Variable Name	Type	Description	Default	Units
		whenever possible to optimize the design.		
PL_MAX_DISPLACEMENT_X	Decimal	Specifies how far an instance can be moved along the X-axis when finding a site where it can be placed during detailed placement.	500	μm
PL_MAX_DISPLACEMENT_Y	Decimal	Specifies how far an instance can be moved along the Y-axis when finding a site where it can be placed during detailed placement.	100	μm
DPL_CELL_PADDING ^{PDK}	Decimal	Cell padding value (in sites) for detailed placement. The number will be integer divided by 2 and placed on both sides. Should be <= global placement.	None	sites
RT_CLOCK_MIN_LAYER	str?	The name of lowest layer to be used in routing the clock net.	None	
RT_CLOCK_MAX_LAYER	str?	The name of highest layer to be used in routing the clock net.	None	
GRT_ADJUSTMENT	Decimal	Reduction in the routing capacity of the edges between the cells in the global routing graph for all layers. Values range from 0 to 1. 1 = most reduction, 0 = least reduction.	0.3	
GRT_MACRO_EXTENSION	int	Sets the number of GCells added to the blockages boundaries from macros. A GCell is typically defined in terms of Mx routing tracks. The default GCell size is 15 M3 pitches.	0	

Variable Name	Type	Description	Default	Units
GRT_LAYER_ADJUSTMENTS <small>PDK</small>	List[Decimal]	Layer-specific reductions in the routing capacity of the edges between the cells in the global routing graph, delimited by commas. Values range from 0 through 1.	None	
DIODE_PADDING	int?	Diode cell padding; increases the width of diode cells during placement checks..	None	sites
GRT_ALLOW_CONGESTION	bool	Allow congestion during global routing	False	
GRT_ANTENNA_ITERS	int	The maximum number of iterations for global antenna repairs.	3	
GRT_OVERFLOW_ITERS	int	The maximum number of iterations waiting for the overflow to reach the desired value.	50	
GRT_ANTENNA_MARGIN	int	The margin to over fix antenna violations.	10	%

Fuzzy Diode Placement

Runs a custom diode placement script to mitigate the [antenna effect](#).

This script uses the [Manhattan length](#) of a (non-existent) wire at the global placement stage, and places diodes if they exceed a certain threshold. This, however, requires some padding: `GPL_CELL_PADDING` and `DPL_CELL_PADDING` must be higher than 0 for this script to work reliably.

The placement is *not* legalized.

The original script was written by [Sylvain "tnt" Munaut](#).

Importing



Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	OpenDB Database (.odb)
	Design Exchange Format (.def)

Configuration Variables

Variable Name	Type	Description	Default	Units
<code>HEURISTIC_ANTENNA_THRESHOLD</code> PDK	Decimal	A Manhattan distance above which a diode is recommended to be inserted by the heuristic inserter. If not specified, the heuristic algorithm.	None	µm
<code>GPL_CELL_PADDING</code> PDK	Decimal	Cell padding value (in sites) for global placement. Used by this step only to emit a warning if it's 0.	None	sites

Heuristic Diode Insertion Routine

Runs a custom diode insertion routine to mitigate the [antenna effect](#).

This script uses the [Manhattan length](#) of a (non-existent) wire at the global placement stage, and places diodes if they exceed a certain threshold. This, however, requires some padding: `GPL_CELL_PADDING` and `DPL_CELL_PADDING` must be higher than 0 for this script to work reliably.

The placement is then legalized by performing detailed placement and global routing after inserting the diodes.

The original script was written by [Sylvain "tnt" Munaut](#).

Prior to beta 16, this step did not legalize its placement: if you would like to retain the old behavior without legalization, try `Odb.FuzzyDiodePlacement`.

Importing



Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	Powered Verilog Netlist (.pnl.v)
	Design Constraints (.sdc)
	OpenDB Database (.odb)
	Verilog Netlist (.nl.v)
	Design Exchange Format (.def)

Configuration Variables

Variable Name	Type	Description	Default	Units
<code>HEURISTIC_ANTENNA_THRESHOLD</code> ^{PDK}	Decimal	A Manhattan distance above which a diode is recommended to be inserted by the heuristic inserter. If not specified, the heuristic algorithm.	None	µm
<code>GPL_CELL_PADDING</code> ^{PDK}	Decimal	Cell padding value (in sites) for global placement. Used by this step only to emit a warning if it's 0.	None	sites
<code>PDN_CONNECT_MACROS_TO_GRID</code>	bool	Enables the connection of macros to the top level power grid.	True	
<code>PDN_MACRO_CONNECTIONS</code>	List[str]?	Specifies explicit power connections of internal macros to the top level power grid, in the format: regex matching macro instance names, power domain vdd and ground net names, and macro vdd and ground pin names <code><instance_name_rx></code> <code><vdd_net> <gnd_net></code> <code><vdd_pin> <gnd_pin>.</code>	None	
<code>PDN_ENABLE_GLOBAL_CONNECTIONS</code>	bool	Enables the creation of global connections in PDN generation.	True	
<code>PNR_SDC_FILE</code>	Path?	Specifies the SDC file used during all implementation (PnR) steps	None	
<code>FP_DEF_TEMPLATE</code>	Path?	Points to the DEF file to be used as a template.	None	
<code>PL_OPTIMIZE_MIRRORING</code>	bool	Specifies whether or not to run an optimize_mirroring pass whenever detailed placement happens. This	True	

Variable Name	Type	Description	Default	Units
		pass will mirror the cells whenever possible to optimize the design.		
PL_MAX_DISPLACEMENT_X	Decimal	Specifies how far an instance can be moved along the X-axis when finding a site where it can be placed during detailed placement.	500	μm
PL_MAX_DISPLACEMENT_Y	Decimal	Specifies how far an instance can be moved along the Y-axis when finding a site where it can be placed during detailed placement.	100	μm
DPL_CELL_PADDING ^{PDK}	Decimal	Cell padding value (in sites) for detailed placement. The number will be integer divided by 2 and placed on both sides. Should be <= global placement.	None	sites
RT_CLOCK_MIN_LAYER	str?	The name of lowest layer to be used in routing the clock net.	None	
RT_CLOCK_MAX_LAYER	str?	The name of highest layer to be used in routing the clock net.	None	
GRT_ADJUSTMENT	Decimal	Reduction in the routing capacity of the edges between the cells in the global routing graph for all layers. Values range from 0 to 1. 1 = most reduction, 0 = least reduction.	0.3	
GRT_MACRO_EXTENSION	int	Sets the number of GCells added to the blockages boundaries from macros. A GCell is typically defined in terms of Mx routing tracks.	0	

Variable Name	Type	Description	Default	Units
GRT_LAYER_ADJUSTMENTS <small>PDK</small>	List[Decimal]	The default GCell size is 15 M3 pitches.		
DIODE_PADDING	int?	Layer-specific reductions in the routing capacity of the edges between the cells in the global routing graph, delimited by commas. Values range from 0 through 1.	None	
GRT_ALLOW_CONGESTION	bool	Diode cell padding; increases the width of diode cells during placement checks..	None	sites
GRT_ANTENNA_ITERS	int	Allow congestion during global routing	False	
GRT_OVERFLOW_ITERS	int	The maximum number of iterations for global antenna repairs.	3	
GRT_ANTENNA_MARGIN	int	The maximum number of iterations waiting for the overflow to reach the desired value.	50	
		The margin to over fix antenna violations.	10	%

Manual Macro Placement

Performs macro placement using a simple configuration file. The file is defined as a line-break delimited list of instances and positions, in the format `instance_name X_pos Y_pos Orientation`.

If no macro instances are configured, this step is skipped.

Importing >

Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	OpenDB Database (.odb)
	Design Exchange Format (.def)

Configuration Variables

Variable Name	Type	Description	Default	Units
MACRO_PLACEMENT_CFG	Path?	Path to an optional override for instance placement instead of the <code>MACROS</code> object for compatibility with OpenLane 1. If both are <code>None</code> , this step is skipped.	None	

Port Diode Placement Script

Unconditionally inserts diodes on design ports diodes on ports, to mitigate the [antenna effect](#).

Useful for hardening macros, where ports may get long wires that are unaccounted for when hardening a top-level chip.

The placement is **not legalized**.

Importing

Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	OpenDB Database (.odb)
	Design Exchange Format (.def)

Configuration Variables

Variable Name	Type	Description	Default	Units
DIODE_ON_PORTS	'none' 'in' 'out' 'both'	Always insert diodes on ports with the specified polarities.	none	
GPL_CELL_PADDING ^{PDK}	Decimal	Cell padding value (in sites) for global placement. Used by this step only to emit a warning if it's 0.	None	sites

Remove PDN obstructions

Importing

Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	OpenDB Database (.odb)
	Design Exchange Format (.def)

Configuration Variables

Variable Name	Type	Description	Default	Units
PDN_OBSTRUCTIONS	List[str]?	Add routing obstructions to the design before PDN stage. If set to <code>None</code> , this step is skipped. Format of each obstruction item is: layer llx lly urx ury.	None	μm

Remove Obstructions

Importing



Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	OpenDB Database (.odb)
	Design Exchange Format (.def)

Configuration Variables

Variable Name	Type	Description	Default	Units
ROUTING_OBSTRUCTIONS	List[str]?	Add routing obstructions to the design. If set to <code>None</code> , this step is skipped. Format of each obstruction item is: layer llx lly urx ury.	None	μm

Report Disconnected Pins

Creates a table of disconnected pins in the design, updating metrics as appropriate.

Disconnected pins may be marked “critical” if they are very likely to result in a dead design. We determine if a pin is critical as follows:

- For the top-level macro: for these four kinds of pins: inputs, outputs, power inouts, and ground inouts, at least one of each kind must be connected or else all pins of a certain kind are counted as critical disconnected pins.
- For instances:**
 - Any unconnected input is a critical disconnected pin.
 - If there isn’t at least one output connected, all disconnected outputs are critical disconnected pins.
 - Any disconnected power inout pins are critical disconnected pins.

The metrics `design_DISCONNECTED_PIN_COUNT` and `design_CRITICAL_DISCONNECTED_PIN_COUNT` is updated. It is recommended to use the checker `Checker.DisconnectedPins` to check that there are no critical disconnected pins.

Importing >

Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	OpenDB Database (.odb)
	Design Exchange Format (.def)

Configuration Variables

Variable Name	Type	Description	Default	Units
<code>IGNORE_DISCONNECTED_MODULES</code> PDK	List[str]?	Modules (or cells) to ignore when checking for disconnected pins.	None	

Report Wire Length

Outputs a CSV of long wires, printed by length. Useful as a design aid to detect when one wire is connected to too many things.

Importing >

Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	

Set Power Connections

Uses JSON netlist and module information in Odb to add global power connections for macros in a design.

Importing >

Inputs and Outputs

Inputs	Outputs
Design JSON Header File (.h.json)	OpenDB Database (.odb)
OpenDB Database (.odb)	Design Exchange Format (.def)

Write Verilog Header

Writes a Verilog header of the module using information from the generated PDN, guarded by the value of `VERILOG_POWER_DEFINE`, and the JSON header.

Importing >

Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	Verilog Header (.vh)
Design JSON Header File (.h.json)	

Configuration Variables

Variable Name	Type	Description	Default	Units
<code>VERILOG_POWER_DEFINE</code>	str	Specifies the name of the define used to guard power and ground connections in the output Verilog header.	<code>USE_POWER_PINS</code>	

OpenROAD

Basic Macro Placement

Importing >

Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	OpenDB Database (.odb)
	Design Exchange Format (.def)
	Design Constraints (.sdc)
	Verilog Netlist (.nl.v)
	Powered Verilog Netlist (.pnl.v)

Configuration Variables

Variable Name	Type	Description	Default	Units
PDN_CONNECT_MACROS_TO_GRID	bool	Enables the connection of macros to the top level power grid.	True	
PDN_MACRO_CONNECTIONS	List[str]?	Specifies explicit power connections of internal macros to the top level power grid, in the format: regex matching macro instance names, power domain vdd and ground net names, and macro vdd and ground pin names <code><instance_name_rx> <vdd_net></code> <code><gnd_net> <vdd_pin> <gnd_pin>.</code>	None	
PDN_ENABLE_GLOBAL_CONNECTIONS	bool	Enables the creation of global connections in PDN generation.	True	
PNR_SDC_FILE	Path?	Specifies the SDC file used during all implementation (PnR) steps	None	
FP_DEF_TEMPLATE	Path?	Points to the DEF file to be used as a template.	None	
PL_MACRO_HALO	str	Macro placement halo. Format: <code>{Horizontal} {Vertical}</code> .	0 0	μm
PL_MACRO_CHANNEL	str	Channel widths between macros. Format: <code>{Horizontal} {Vertical}</code> .	0 0	μm

Clock Tree Synthesis

Creates a [Clock tree](#) for an ODB file with detailed-placed cells, using reasonably accurate resistance and capacitance estimations. Detailed Placement is then re-performed to accommodate the new cells.

Importing



Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	OpenDB Database (.odb)
	Design Exchange Format (.def)
	Design Constraints (.sdc)
	Verilog Netlist (.nl.v)
	Powered Verilog Netlist (.pnl.v)

Configuration Variables

Variable Name	Type	Description	Default	Units
PDN_CONNECT_MACROS_TO_GRID	bool	Enables the connection of macros to the top level power grid.	True	
PDN_MACRO_CONNECTIONS	List[str]?	Specifies explicit power connections of internal macros to the top level power grid, in the format: regex matching macro instance names, power domain vdd and ground net names, and macro vdd and ground pin names <pre><instance_name_rx> <vdd_net> <gnd_net> <vdd_pin> <gnd_pin> .</pre>	None	
PDN_ENABLE_GLOBAL_CONNECTIONS	bool	Enables the creation of global connections in PDN generation.	True	
PNR_SDC_FILE	Path?	Specifies the SDC file used during all implementation (PnR) steps	None	
FP_DEF_TEMPLATE	Path?	Points to the DEF file to be used as a template.	None	
PL_OPTIMIZE_MIRRORING	bool	Specifies whether or not to run an optimize_mirroring pass whenever detailed placement happens. This pass will mirror the cells whenever possible to optimize the design.	True	
PL_MAX_DISPLACEMENT_X	Decimal	Specifies how far an instance can be moved along the X-axis when finding a site where it can be placed during detailed placement.	500	μm
PL_MAX_DISPLACEMENT_Y	Decimal	Specifies how far an instance can be moved along the Y-	100	μm

Variable Name	Type	Description	Default	Units
DPL_CELL_PADDING ^{PDK}	Decimal	axis when finding a site where it can be placed during detailed placement.		
CTS_SINK_CLUSTERING_SIZE	int	Cell padding value (in sites) for detailed placement. The number will be integer divided by 2 and placed on both sides. Should be <= global placement.	None	sites
CTS_SINK_CLUSTERING_MAX_DIAMETER	Decimal	Specifies the maximum number of sinks per cluster.	25	
CTS_CLK_MAX_WIRE_LENGTH	Decimal	Specifies maximum diameter of the sink cluster.	50	μm
CTS_DISABLE_POST_PROCESSING	bool	Specifies the maximum wire length on the clock net.	0	μm
CTS_DISTANCE_BETWEEN_BUFFERS	Decimal	Specifies whether or not to disable post cts processing for outlier sinks.	False	
CTS_CORNERS	Decimal	Specifies the distance between buffers when creating the clock tree.	0	μm
CTS_ROOT_BUFFER ^{PDK}	List[str]?	A list of fully-qualified IPVT corners to use during clock tree synthesis. If unspecified, the value for STA_CORNERS from the PDK will be used.	None	
CTS_CLK_BUFFERS ^{PDK}	str	Defines the cell inserted at the root of the clock tree. Used in CTS.	None	
CTS_CLK_BUFFERS ^{PDK}	List[str]	Defines the list of clock buffers to be used in CTS.	None	
CTS_MAX_CAP	Decimal?	Overrides the maximum capacitance CTS characterization will test. If omitted, the capacitance is extracted from the lib information of the buffers in CTS_CLK_BUFFERS.	None	pF

Variable Name	Type	Description	Default	Units
CTS_MAX_SLEW	Decimal?	Overrides the maximum transition time CTS characterization will test. If omitted, the slew is extracted from the lib information of the buffers in CTS_CLK_BUFFERS.	None	ns

Check Antennas

Runs OpenROAD to check if one or more long nets may constitute an [antenna risk](#).

The metric `route_antennaViolationCount` will be updated with the number of violating nets.

Importing



Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	

Configuration Variables

Variable Name	Type	Description	Default	Units
PDN_CONNECT_MACROS_TO_GRID	bool	Enables the connection of macros to the top level power grid.	True	
PDN_MACRO_CONNECTIONS	List[str]?	Specifies explicit power connections of internal macros to the top level power grid, in the format: regex matching macro instance names, power domain vdd and ground net names, and macro vdd and ground pin names <code><instance_name_rx> <vdd_net></code> <code><gnd_net> <vdd_pin> <gnd_pin>.</code>	None	
PDN_ENABLE_GLOBAL_CONNECTIONS	bool	Enables the creation of global connections in PDN generation.	True	
PNR_SDC_FILE	Path?	Specifies the SDC file used during all implementation (PnR) steps	None	
FP_DEF_TEMPLATE	Path?	Points to the DEF file to be used as a template.	None	

Check Macro Instances

Checks if all macro instances declared in the configuration are, in fact, in the design, emitting an error otherwise.

Nested macros (macros within macros) are supported provided netlist views are available for the macro.

Importing



Inputs and Outputs

Inputs	Outputs
Verilog Netlist (.nl.v)	

Configuration Variables

Variable Name	Type	Description	Default	Units
PDN_CONNECT_MACROS_TO_GRID	bool	Enables the connection of macros to the top level power grid.	True	
PDN_MACRO_CONNECTIONS	List[str]?	Specifies explicit power connections of internal macros to the top level power grid, in the format: regex matching macro instance names, power domain vdd and ground net names, and macro vdd and ground pin names <instance_name_rx> <vdd_net> <gnd_net> <vdd_pin> <gnd_pin>.	None	
PDN_ENABLE_GLOBAL_CONNECTIONS	bool	Enables the creation of global connections in PDN generation.	True	
PNR_SDC_FILE	Path?	Specifies the SDC file used during all implementation (PnR) steps	None	
FP_DEF_TEMPLATE	Path?	Points to the DEF file to be used as a template.	None	

Check SDC Files

Checks that the two variables used for SDC files by OpenROAD steps, namely, `PNR_SDC_FILE` and `SIGNOFF_SDC_FILE`, are explicitly set to valid paths by the users, and emits a warning that the fallback will be utilized otherwise.

Importing



Configuration Variables

Variable Name	Type	Description	Default	Units
PNR_SDC_FILE	Path?	Specifies the SDC file used during all implementation (PnR) steps	None	
SIGNOFF_SDC_FILE	Path?	Specifies the SDC file for STA during signoff	None	

Cut Rows

Cut floorplan rows with respect to placed macros.

Importing >

Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	OpenDB Database (.odb)
	Design Exchange Format (.def)

Configuration Variables

Variable Name	Type	Description	Default	Units
PDN_CONNECT_MACROS_TO_GRID	bool	Enables the connection of macros to the top level power grid.	True	
PDN_MACRO_CONNECTIONS	List[str]?	Specifies explicit power connections of internal macros to the top level power grid, in the format: regex matching macro instance names, power domain vdd and ground net names, and macro vdd and ground pin names <code><instance_name_rx> <vdd_net></code> <code><gnd_net> <vdd_pin> <gnd_pin>.</code>	None	
PDN_ENABLE_GLOBAL_CONNECTIONS	bool	Enables the creation of global connections in PDN generation.	True	
PNR_SDC_FILE	Path?	Specifies the SDC file used during all implementation (PnR) steps	None	
FP_DEF_TEMPLATE	Path?	Points to the DEF file to be used as a template.	None	
FP_MACRO_HORIZONTAL_HALO	Decimal	Specify the horizontal halo size around macros while cutting rows.	10	μm
FP_MACRO_VERTICAL_HALO	Decimal	Specify the vertical halo size around macros while cutting rows.	10	μm

DEF to OpenDB

Converts a DEF view to an ODB view.

Useful if you have a custom step that manipulates the layout outside of OpenROAD, but you would like to update the OpenROAD database.

Importing



Inputs and Outputs

Inputs	Outputs
Design Exchange Format (.def)	OpenDB Database (.odb)

Configuration Variables

Variable Name	Type	Description	Default	Units
PDN_CONNECT_MACROS_TO_GRID	bool	Enables the connection of macros to the top level power grid.	True	
PDN_MACRO_CONNECTIONS	List[str]?	Specifies explicit power connections of internal macros to the top level power grid, in the format: regex matching macro instance names, power domain vdd and ground net names, and macro vdd and ground pin names <code><instance_name_rx> <vdd_net></code> <code><gnd_net> <vdd_pin> <gnd_pin>.</code>	None	
PDN_ENABLE_GLOBAL_CONNECTIONS	bool	Enables the creation of global connections in PDN generation.	True	
PNR_SDC_FILE	Path?	Specifies the SDC file used during all implementation (PnR) steps	None	
FP_DEF_TEMPLATE	Path?	Points to the DEF file to be used as a template.	None	

Detailed Placement

Performs “detailed placement” on an ODB file with global placement. This results in a concrete and legal placement of all cells.

Importing



Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	OpenDB Database (.odb)
	Design Exchange Format (.def)
	Design Constraints (.sdc)
	Verilog Netlist (.nl.v)
	Powered Verilog Netlist (.pnl.v)

Configuration Variables

Variable Name	Type	Description	Default	Units
PDN_CONNECT_MACROS_TO_GRID	bool	Enables the connection of macros to the top level power grid.	True	
PDN_MACRO_CONNECTIONS	List[str]?	Specifies explicit power connections of internal macros to the top level power grid, in the format: regex matching macro instance names, power domain vdd and ground net names, and macro vdd and ground pin names <code><instance_name_rx> <vdd_net></code> <code><gnd_net> <vdd_pin> <gnd_pin>.</code>	None	
PDN_ENABLE_GLOBAL_CONNECTIONS	bool	Enables the creation of global connections in PDN generation.	True	
PNR_SDC_FILE	Path?	Specifies the SDC file used during all implementation (PnR) steps	None	
FP_DEF_TEMPLATE	Path?	Points to the DEF file to be used as a template.	None	
PL_OPTIMIZE_MIRRORING	bool	Specifies whether or not to run an optimize_mirroring pass whenever detailed placement happens. This pass will mirror the cells whenever possible to optimize the design.	True	
PL_MAX_DISPLACEMENT_X	Decimal	Specifies how far an instance can be moved along the X-axis when finding a site where it can be placed during detailed placement.	500	μm
PL_MAX_DISPLACEMENT_Y	Decimal	Specifies how far an instance can be moved along the Y-axis when finding a site where it can be placed during detailed placement.	100	μm

Variable Name	Type	Description	Default	Units
DPL_CELL_PADDING ^{PDK}	Decimal	Cell padding value (in sites) for detailed placement. The number will be integer divided by 2 and placed on both sides. Should be <= global placement.	None	sites

Detailed Routing

The latter phase of routing. This transforms the abstract nets from global routing into wires on the metal layers that respect all design rules, avoids creating accidental shorts, and ensures all wires are connected.

This is by far the longest part of a typical flow, taking hours, days or weeks on larger designs.

After this point, all cells connected to a net can no longer be moved or removed without a custom-written step of some kind that will also rip up wires.

Importing



Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	OpenDB Database (.odb)
	Design Exchange Format (.def)
	Design Constraints (.sdc)
	Verilog Netlist (.nl.v)
	Powered Verilog Netlist (.pnl.v)

Configuration Variables

Variable Name	Type	Description	Default	Units
PDN_CONNECT_MACROS_TO_GRID	bool	Enables the connection of macros to the top level power grid.	True	
PDN_MACRO_CONNECTIONS	List[str]?	Specifies explicit power connections of internal macros to the top level power grid, in the format: regex matching macro instance names, power domain vdd and ground net names, and macro vdd and ground pin names <code><instance_name_rx> <vdd_net></code> <code><gnd_net> <vdd_pin> <gnd_pin>.</code>	None	
PDN_ENABLE_GLOBAL_CONNECTIONS	bool	Enables the creation of global connections in PDN generation.	True	
PNR_SDC_FILE	Path?	Specifies the SDC file used during all implementation (PnR) steps	None	
FP_DEF_TEMPLATE	Path?	Points to the DEF file to be used as a template.	None	
DRT_THREADS	int?	Specifies the number of threads to be used in OpenROAD Detailed Routing. If unset, this will be equal to your machine's thread count.	None	
DRT_MIN_LAYER	str?	An optional override to the lowest layer used in detailed routing. For example, in sky130, you may want global routing to avoid li1, but let detailed routing use li1 if it has to.	None	
DRT_MAX_LAYER	str?	An optional override to the highest layer used in detailed routing.	None	

Variable Name	Type	Description	Default	Units
DRT_OPT_ITERS	int	Specifies the maximum number of optimization iterations during Detailed Routing in TritonRoute.	64	

Fill Insertion

Fills gaps in the floorplan with filler and decap cells.

This is run after detailed placement. After this point, the design is basically completely hardened.

Importing



Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	OpenDB Database (.odb)
	Design Exchange Format (.def)
	Design Constraints (.sdc)
	Verilog Netlist (.nl.v)
	Powered Verilog Netlist (.pnl.v)

Configuration Variables

Variable Name	Type	Description	Default	Units
PDN_CONNECT_MACROS_TO_GRID	bool	Enables the connection of macros to the top level power grid.	True	
PDN_MACRO_CONNECTIONS	List[str]?	Specifies explicit power connections of internal macros to the top level power grid, in the format: regex matching macro instance names, power domain vdd and ground net names, and macro vdd and ground pin names <code><instance_name_rx> <vdd_net></code> <code><gnd_net> <vdd_pin> <gnd_pin>.</code>	None	
PDN_ENABLE_GLOBAL_CONNECTIONS	bool	Enables the creation of global connections in PDN generation.	True	
PNR_SDC_FILE	Path?	Specifies the SDC file used during all implementation (PnR) steps	None	
FP_DEF_TEMPLATE	Path?	Points to the DEF file to be used as a template.	None	

Floorplan Initialization

Creates DEF and ODB files with the initial floorplan based on the Yosys netlist.

Importing



Inputs and Outputs

Inputs	Outputs
Verilog Netlist (.nl.v)	OpenDB Database (.odb)
	Design Exchange Format (.def)
	Design Constraints (.sdc)
	Verilog Netlist (.nl.v)
	Powered Verilog Netlist (.pnl.v)

Configuration Variables

Variable Name	Type	Description	Default	Units
PDN_CONNECT_MACROS_TO_GRID	bool	Enables the connection of macros to the top level power grid.	True	
PDN_MACRO_CONNECTIONS	List[str]?	Specifies explicit power connections of internal macros to the top level power grid, in the format: regex matching macro instance names, power domain vdd and ground net names, and macro vdd and ground pin names <code><instance_name_rx></code> <code><vdd_net> <gnd_net></code> <code><vdd_pin> <gnd_pin>.</code>	None	
PDN_ENABLE_GLOBAL_CONNECTIONS	bool	Enables the creation of global connections in PDN generation.	True	
PNR_SDC_FILE	Path?	Specifies the SDC file used during all implementation (PnR) steps	None	
FP_DEF_TEMPLATE	Path?	Points to the DEF file to be used as a template.	None	
FP_SIZING	'absolute' 'relative'	Sizing mode for floorplanning	relative	
FP_ASPECT_RATIO	Decimal	The core's aspect ratio (height / width).	1	
FP_CORE_UTIL	Decimal	The core utilization percentage.	50	%

Variable Name	Type	Description	Default	Units
FP_OBSTRUCTIONS	List[Tuple[Decimal, Decimal, Decimal, Decimal]]?	Obstructions applied at floorplanning stage. Placement sites are never generated at these locations, which guarantees that it will remain empty throughout the entire flow.	None	μm
PL_SOFT_OBSTRUCTIONS	List[Tuple[Decimal, Decimal, Decimal, Decimal]]?	Soft placement blockages applied at the floorplanning stage. Areas that are soft-blocked will not be used by the initial placer, however, later phases such as buffer insertion or clock tree synthesis are still allowed to place cells in this area.	None	μm
CORE_AREA	Tuple[Decimal, Decimal, Decimal, Decimal]?	Specifies a core area (i.e. die area minus margins) to be used in floorplanning. It must be paired with DIE_AREA.	None	μm
BOTTOM_MARGIN_MULT	Decimal	The core margin, in multiples of site heights, from the bottom boundary. If DIE_AREA and CORE_AREA are set, this variable has no effect.	4	
TOP_MARGIN_MULT	Decimal	The core margin, in multiples of site heights, from the top	4	

Variable Name	Type	Description	Default	Units
		boundary. If <code>DIE_AREA</code> and <code>CORE_AREA</code> are set, this variable has no effect.		
<code>LEFT_MARGIN_MULT</code>	Decimal	The core margin, in multiples of site widths, from the left boundary. If <code>DIE_AREA</code> are <code>CORE_AREA</code> are set, this variable has no effect.	12	
<code>RIGHT_MARGIN_MULT</code>	Decimal	The core margin, in multiples of site widths, from the right boundary. If <code>DIE_AREA</code> are <code>CORE_AREA</code> are set, this variable has no effect.	12	
<code>EXTRA_SITES</code> PDK	List[str]?	Explicitly specify sites other than <code>PLACE_SITE</code> to create rows for. If the alternate-site standard cells properly declare the <code>SITE</code> property, you do not need to provide this explicitly.	None	

Power Distribution Network Generation

Creates a power distribution network on a floorplanned ODB file.

Importing



Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	OpenDB Database (.odb)
	Design Exchange Format (.def)
	Design Constraints (.sdc)
	Verilog Netlist (.nl.v)
	Powered Verilog Netlist (.pnl.v)

Configuration Variables

Variable Name	Type	Description	Default	Units
PDN_CONNECT_MACROS_TO_GRID	bool	Enables the connection of macros to the top level power grid.	True	
PDN_MACRO_CONNECTIONS	List[str]?	Specifies explicit power connections of internal macros to the top level power grid, in the format: regex matching macro instance names, power domain vdd and ground net names, and macro vdd and ground pin names <code><instance_name_rx> <vdd_net></code> <code><gnd_net> <vdd_pin> <gnd_pin>.</code>	None	
PDN_ENABLE_GLOBAL_CONNECTIONS	bool	Enables the creation of global connections in PDN generation.	True	
PNR_SDC_FILE	Path?	Specifies the SDC file used during all implementation (PnR) steps	None	
FP_DEF_TEMPLATE	Path?	Points to the DEF file to be used as a template.	None	
FP_PDN_SKIPTRIM	bool	Enables <code>-skip_trim</code> option during pdngen which skips the metal trim step, which attempts to remove metal stubs.	False	
FP_PDN_CORE_RING	bool	Enables adding a core ring around the design. More details on the control variables in the PDK config documentation.	False	
FP_PDN_ENABLE_RAILS	bool	Enables the creation of rails in the power grid.	True	
FP_PDN_HORIZONTAL_HALO	Decimal	Sets the horizontal halo around the macros during power grid insertion.	10	μm
FP_PDN_VERTICAL_HALO	Decimal	Sets the vertical halo around the macros during power grid insertion.	10	μm

Variable Name	Type	Description	Default	Units
FP_PDN_MULTILAYER	bool	Controls the layers used in the power grid. If set to false, only the lower layer will be used, which is useful when hardening a macro for integrating into a larger top-level design.	True	
FP_PDN_RAIL_OFFSET ^{PDK}	Decimal	The offset for the power distribution network rails for first metal layer.	None	μm
FP_PDN_VWIDTH ^{PDK}	Decimal	The strap width for the vertical layer in generated power distribution networks.	None	μm
FP_PDN_HWIDTH ^{PDK}	Decimal	The strap width for the horizontal layer in generated power distribution networks.	None	μm
FP_PDN_VSPACING ^{PDK}	Decimal	Intra-spacing (within a set) of vertical straps in generated power distribution networks.	None	μm
FP_PDN_HSPACING ^{PDK}	Decimal	Intra-spacing (within a set) of horizontal straps in generated power distribution networks.	None	μm
FP_PDN_VPITCH ^{PDK}	Decimal	Inter-distance (between sets) of vertical power straps in generated power distribution networks.	None	μm
FP_PDN_HPITCH ^{PDK}	Decimal	Inter-distance (between sets) of horizontal power straps in generated power distribution networks.	None	μm
FP_PDN_VOFFSET ^{PDK}	Decimal	Initial offset for sets of vertical power straps.	None	μm
FP_PDN_HOFFSET ^{PDK}	Decimal	Initial offset for sets of horizontal power straps.	None	μm
FP_PDN_CORE_RING_VWIDTH ^{PDK}	Decimal	The width for the vertical layer in the core ring of generated power distribution networks.	None	μm
FP_PDN_CORE_RING_HWIDTH ^{PDK}	Decimal	The width for the horizontal layer in the core ring of generated	None	μm

Variable Name	Type	Description	Default	Units
		power distribution networks.		
<code>FP_PDN_CORE_RING_VSPACING</code> PDK	Decimal	The spacing for the vertical layer in the core ring of generated power distribution networks.	None	μm
<code>FP_PDN_CORE_RING_HSPACING</code> PDK	Decimal	The spacing for the horizontal layer in the core ring of generated power distribution networks.	None	μm
<code>FP_PDN_CORE_RING_VOFFSET</code> PDK	Decimal	The offset for the vertical layer in the core ring of generated power distribution networks.	None	μm
<code>FP_PDN_CORE_RING_HOFFSET</code> PDK	Decimal	The offset for the horizontal layer in the core ring of generated power distribution networks.	None	μm
<code>FP_PDN_RAIL_LAYER</code> PDK	str	Defines the metal layer used for PDN rails.	None	
<code>FP_PDN_RAIL_WIDTH</code> PDK	Decimal	Defines the width of PDN rails on the <code>FP_PDN_RAILS_LAYER</code> layer.	None	μm
<code>FP_PDN_HORIZONTAL_LAYER</code> PDK	str	Defines the horizontal PDN layer.	None	
<code>FP_PDN_VERTICAL_LAYER</code> PDK	str	Defines the vertical PDN layer.	None	
<code>FP_PDN_CFG</code>	Path?	A custom PDN configuration file. If not provided, the default PDN config will be used.	None	

Global Placement

Performs a somewhat nebulous initial placement for standard cells in a floorplan. While the placement is not concrete, it is enough to start accounting for issues such as fanout, transition time, et cetera.

Importing



Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	OpenDB Database (.odb)
	Design Exchange Format (.def)
	Design Constraints (.sdc)
	Verilog Netlist (.nl.v)
	Powered Verilog Netlist (.pnl.v)

Configuration Variables

Variable Name	Type	Description
PDN_CONNECT_MACROS_TO_GRID	bool	Enables the connection of macros to the top level power grid.
PDN_MACRO_CONNECTIONS	List[str]?	Specifies explicit power connections of internal nets to the top level power grid, in the format: regex matching net names, power domain vdd and ground net names and ground pin names <instance_name_rx> <vdd_pin> <gnd_pin>.
PDN_ENABLE_GLOBAL_CONNECTIONS	bool	Enables the creation of global connections in PDN.
PNR_SDC_FILE	Path?	Specifies the SDC file used during all implementation steps.
FP_DEF_TEMPLATE	Path?	Points to the DEF file to be used as a template.
RT_CLOCK_MIN_LAYER	str?	The name of lowest layer to be used in routing tiles.
RT_CLOCK_MAX_LAYER	str?	The name of highest layer to be used in routing tiles.
GRT_ADJUSTMENT	Decimal	Reduction in the routing capacity of the edges belonging to the global routing graph for all layers. Values range from 0 to 1. 0 = most reduction, 1 = least reduction.
GRT_MACRO_EXTENSION	int	Sets the number of GCells added to the blockages around macros. A GCell is typically defined in terms of M3 pitch. Default GCell size is 15 M3 pitches.
GRT_LAYER_ADJUSTMENTS ^{PDK}	List[Decimal]	Layer-specific reductions in the routing capacity of the cells in the global routing graph, delimited by a range from 0 through 1.
PL_TARGET_DENSITY_PCT	Decimal?	The desired placement density of cells. If not specified, it will be equal to (FP_CORE_UTIL + 5 * GPL_CELL_PADDING) / 100.
PL_SKIP_INITIAL_PLACEMENT	bool	Specifies whether the placer should run initial placement.
PL_WIRE_LENGTH_COEF	Decimal	Global placement initial wirelength coefficient. Default value is 1.0. It will modify the initial placement of the standard wirelengths.
PL_MIN_PHI_COEFFICIENT	Decimal?	Sets a lower bound on the μ_k variable in the GP global placement diverges. See https://openroad.readthedocs.io/en/latest/main/gp.html
PL_MAX_PHI_COEFFICIENT	Decimal?	Sets an upper bound on the μ_k variable in the GP global placement diverges. See https://openroad.readthedocs.io/en/latest/main/gp.html
FP_CORE_UTIL	Decimal	The core utilization percentage.

Variable Name	Type	Description
GPL_CELL_PADDING ^{PDK}	Decimal	Cell padding value (in sites) for global placement integer divided by 2 and placed on both sides.
PL_TIME_DRIVEN	bool	Specifies whether the placer should use time driven placement.
PL_ROUTABILITY_DRIVEN	bool	Specifies whether the placer should use routability driven placement.

Global Placement Skip IO

Performs global placement without taking I/O into consideration.

This is useful for flows where the:

- * Cells are placed
- * I/Os are placed to match the cells
- * Cells are then re-placed for an optimal placement

Importing



Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	OpenDB Database (.odb)
	Design Exchange Format (.def)
	Design Constraints (.sdc)
	Verilog Netlist (.nl.v)
	Powered Verilog Netlist (.pnl.v)

Configuration Variables

Variable Name	Type	Description
PDN_CONNECT_MACROS_TO_GRID	bool	Enables the connection of macros to the power grid.
PDN_MACRO_CONNECTIONS	List[str]?	Specifies explicit power connections on a macro level power grid, in the format: regex instance names, power domain vdd and ground pin names <instance_name> <vdd_pin> <gnd_pin>.
PDN_ENABLE_GLOBAL_CONNECTIONS	bool	Enables the creation of global connections.
PNR_SDC_FILE	Path?	Specifies the SDC file used during all placement steps.
FP_DEF_TEMPLATE	Path?	Points to the DEF file to be used as a template.
RT_CLOCK_MIN_LAYER	str?	The name of lowest layer to be used in routing.
RT_CLOCK_MAX_LAYER	str?	The name of highest layer to be used in routing.
GRT_ADJUSTMENT	Decimal	Reduction in the routing capacity of the global routing graph for all layers. 0 = most reduction, 0 = least reduction.
GRT_MACRO_EXTENSION	int	Sets the number of GCells added to the macros. A GCell is typically defined in the PDK. The default GCell size is 15 M3 pitches.
GRT_LAYER_ADJUSTMENTS	List[Decimal] PDK	Layer-specific reductions in the routin the cells in the global routing graph, c range from 0 through 1.
PL_TARGET_DENSITY_PCT	Decimal?	The desired placement density of cells be equal to (<code>FP_CORE_UTIL</code> + 5 * <code>GPL_C</code>) / 100.
PL_SKIP_INITIAL_PLACEMENT	bool	Specifies whether the placer should run without initial placement.
PL_WIRE_LENGTH_COEF	Decimal	Global placement initial wirelength coefficient. This will modify the initial placement of the wirelengths.
PL_MIN_PHI_COEFFICIENT	Decimal?	Sets a lower bound on the μ_k variable for global placement diverges. See https://openroad.readthedocs.io/en/latest/config/variables.html#pl_min_phi_coefficient
PL_MAX_PHI_COEFFICIENT	Decimal?	Sets a upper bound on the μ_k variable for global placement diverges. See https://openroad.readthedocs.io/en/latest/config/variables.html#pl_max_phi_coefficient
FP_CORE_UTIL	Decimal	The core utilization percentage.

Variable Name	Type	Description
GPL_CELL_PADDING ^{PDK}	Decimal	Cell padding value (in sites) for global integer divided by 2 and placed on both sides of the cell.
FP_PPL_MODE	'matching' 'random_equidistant' 'annealing'	Decides the mode of the random IO placement.
FP_DEF_TEMPLATE	Path?	Points to the DEF file to be used as a template for the output DEF file.

Global Routing

The initial phase of routing. Given a detailed-placed ODB file, this phase starts assigning coarse-grained routing “regions” for each net so they may be later connected to wires.

Estimated capacitance and resistance values are much more accurate for global routing.

Importing >

Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	OpenDB Database (.odb)
	Design Exchange Format (.def)

Configuration Variables

Variable Name	Type	Description	Default	Units
PDN_CONNECT_MACROS_TO_GRID	bool	Enables the connection of macros to the top level power grid.	True	
PDN_MACRO_CONNECTIONS	List[str]?	Specifies explicit power connections of internal macros to the top level power grid, in the format: regex matching macro instance names, power domain vdd and ground net names, and macro vdd and ground pin names <pre><instance_name_rx> <vdd_net> <gnd_net> <vdd_pin> <gnd_pin>.</pre>	None	
PDN_ENABLE_GLOBAL_CONNECTIONS	bool	Enables the creation of global connections in PDN generation.	True	
PNR_SDC_FILE	Path?	Specifies the SDC file used during all implementation (PnR) steps	None	
FP_DEF_TEMPLATE	Path?	Points to the DEF file to be used as a template.	None	
RT_CLOCK_MIN_LAYER	str?	The name of lowest layer to be used in routing the clock net.	None	
RT_CLOCK_MAX_LAYER	str?	The name of highest layer to be used in routing the clock net.	None	
GRT_ADJUSTMENT	Decimal	Reduction in the routing capacity of the edges between the cells in the global routing graph for all layers. Values range from 0 to 1. 1 = most reduction, 0 = least reduction.	0.3	

Variable Name	Type	Description	Default	Units
GRT_MACRO_EXTENSION	int	Sets the number of GCells added to the blockages boundaries from macros. A GCell is typically defined in terms of Mx routing tracks. The default GCell size is 15 M3 pitches.	0	
GRT_LAYER_ADJUSTMENTS PDK	List[Decimal]	Layer-specific reductions in the routing capacity of the edges between the cells in the global routing graph, delimited by commas. Values range from 0 through 1.	None	
DIODE_PADDING	int?	Diode cell padding; increases the width of diode cells during placement checks..	None	sites
GRT_ALLOW_CONGESTION	bool	Allow congestion during global routing	False	
GRT_ANTENNA_ITERS	int	The maximum number of iterations for global antenna repairs.	3	
GRT_OVERFLOW_ITERS	int	The maximum number of iterations waiting for the overflow to reach the desired value.	50	
GRT_ANTENNA_MARGIN	int	The margin to over fix antenna violations.	10	%
PL_OPTIMIZE_MIRRORING	bool	Specifies whether or not to run an optimize_mirroring pass whenever detailed placement happens. This pass will mirror the cells whenever possible to optimize the design.	True	
PL_MAX_DISPLACEMENT_X	Decimal	Specifies how far an instance can be moved along the X-axis when finding a site	500	μm

Variable Name	Type	Description	Default	Units
PL_MAX_DISPLACEMENT_Y	Decimal	where it can be placed during detailed placement.		
DPL_CELL_PADDING PDK	Decimal	Specifies how far an instance can be moved along the Y-axis when finding a site where it can be placed during detailed placement.	100	μm
		Cell padding value (in sites) for detailed placement. The number will be integer divided by 2 and placed on both sides. Should be <= global placement.	None	sites

I/O Placement

Places I/O pins on a floor-planned ODB file using OpenROAD's built-in placer.

If `FP_PIN_ORDER_CFG` is not `None`, this step is skipped (for compatibility with OpenLane 1.).

Importing



Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	OpenDB Database (.odb)
	Design Exchange Format (.def)
	Design Constraints (.sdc)
	Verilog Netlist (.nl.v)
	Powered Verilog Netlist (.pnl.v)

Configuration Variables

Variable Name	Type	Description	Default	Units
PDN_CONNECT_MACROS_TO_GRID	bool	Enables the connection of macros to the top level power grid.	True	
PDN_MACRO_CONNECTIONS	List[str]?	Specifies explicit power connections of internal macros to the top level power grid, in the format: regex matching macro instance names, power domain vdd and ground net names, and macro vdd and ground pin names <code><instance_name_rx></code> <code><vdd_net></code> <code><gnd_net></code> <code><vdd_pin></code> <code><gnd_pin>.</code>	None	
PDN_ENABLE_GLOBAL_CONNECTIONS	bool	Enables the creation of global connections in PDN generation.	True	
PNR_SDC_FILE	Path?	Specifies the SDC file used during all implementation (PnR) steps	None	
FP_DEF_TEMPLATE	Path?	Points to the DEF file to be used as a template.	None	
FP_IO_VEXTEND	Decimal	Extends the vertical io pins outside of the die	0	μm

Variable Name	Type	Description	Default	Units
		by the specified units.		
FP_IO_HEXTEND	Decimal	Extends the horizontal io pins outside of the die by the specified units.	0	μm
FP_IO_VTHICKNESS_MULT	Decimal	A multiplier for vertical pin thickness. Base thickness is the pins layer min width.	2	
FP_IO_HTHICKNESS_MULT	Decimal	A multiplier for horizontal pin thickness. Base thickness is the pins layer min width.	2	
FP_PPL_MODE	'matching' 'random_equidistant' 'annealing'	Decides the mode of the random IO placement option.	matching	
FP_IO_MIN_DISTANCE ^{PDK}	Decimal?	The minimum distance between two pins. If unspecified by a PDK, OpenROAD will use the length of two routing tracks.	None	μm
FP_PIN_ORDER_CFG	Path?	Path to a custom pin configuration file.	None	
FP_DEF_TEMPLATE	Path?	Points to the DEF file to be used as a template.	None	
FP_IO_VLENGTH ^{PDK}	Decimal?	The length of the pins with a north	None	μm

Variable Name	Type	Description	Default	Units
		or south orientation. If unspecified by a PDK, OpenROAD will use whichever is higher of the following two values: * The pin width * The minimum value satisfying the minimum area constraint given the pin width		
<code>FP_IO_HLENGTH</code> ^{PDK}	Decimal?	The length of the pins with an east or west orientation. If unspecified by a PDK, OpenROAD will use whichever is higher of the following two values: * The pin width * The minimum value satisfying the minimum area constraint given the pin width	None	μm

Generate IR Drop Report

Performs static IR-drop analysis on the power distribution network. For power nets, this constitutes a decrease in voltage, and for ground nets, it constitutes an increase in voltage.

Importing



Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	
Standard Parasitics Extraction Format (.spf)	

Configuration Variables

Variable Name	Type	Description	Default	Units
PDN_CONNECT_MACROS_TO_GRID	bool	Enables the connection of macros to the top level power grid.	True	
PDN_MACRO_CONNECTIONS	List[str]?	Specifies explicit power connections of internal macros to the top level power grid, in the format: regex matching macro instance names, power domain vdd and ground net names, and macro vdd and ground pin names <code><instance_name_rx> <vdd_net></code> <code><gnd_net> <vdd_pin> <gnd_pin> .</code>	None	
PDN_ENABLE_GLOBAL_CONNECTIONS	bool	Enables the creation of global connections in PDN generation.	True	
PNR_SDC_FILE	Path?	Specifies the SDC file used during all implementation (PnR) steps	None	
FP_DEF_TEMPLATE	Path?	Points to the DEF file to be used as a template.	None	
VSRC_LOC_FILES	Dict[str, Path]?	Map of power and ground nets to OpenROAD PSM location files. See this for more info.	None	

Layout Static Timing Analysis

Performs [Static Timing Analysis](#) using OpenROAD on the ODB layout in its current state.

Importing



Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	

Configuration Variables

Variable Name	Type	Description	Default	Units
PDN_CONNECT_MACROS_TO_GRID	bool	Enables the connection of macros to the top level power grid.	True	
PDN_MACRO_CONNECTIONS	List[str]?	Specifies explicit power connections of internal macros to the top level power grid, in the format: regex matching macro instance names, power domain vdd and ground net names, and macro vdd and ground pin names <code><instance_name_rx> <vdd_net></code> <code><gnd_net> <vdd_pin> <gnd_pin>.</code>	None	
PDN_ENABLE_GLOBAL_CONNECTIONS	bool	Enables the creation of global connections in PDN generation.	True	
PNR_SDC_FILE	Path?	Specifies the SDC file used during all implementation (PnR) steps	None	
FP_DEF_TEMPLATE	Path?	Points to the DEF file to be used as a template.	None	

Open In GUI

Opens the ODB view in the OpenROAD GUI. Useful to inspect some parameters, such as routing density and whatnot.

Importing >

Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	

Parasitic Resistance/Capacitance Extraction

This extracts [parasitic](#) electrical values from a detailed-placed circuit. These can be used to create basically the highest accurate STA possible for a given design.

Importing >

Inputs and Outputs

Inputs	Outputs
Design Exchange Format (.def)	Standard Parasitics Extraction Format (.spef)

Configuration Variables

Variable Name	Type	Description	Default	Units
PDN_CONNECT_MACROS_TO_GRID	bool	Enables the connection of macros to the top level power grid.	True	
PDN_MACRO_CONNECTIONS	List[str]?	Specifies explicit power connections of internal macros to the top level power grid, in the format: regex matching macro instance names, power domain vdd and ground net names, and macro vdd and ground pin names <code><instance_name_rx> <vdd_net></code> <code><gnd_net> <vdd_pin> <gnd_pin>.</code>	None	
PDN_ENABLE_GLOBAL_CONNECTIONS	bool	Enables the creation of global connections in PDN generation.	True	
PNR_SDC_FILE	Path?	Specifies the SDC file used during all implementation (PnR) steps	None	
FP_DEF_TEMPLATE	Path?	Points to the DEF file to be used as a template.	None	
RCX_MERGE_VIA_WIRE_RES	bool	If enabled, the via and wire resistances will be merged.	True	
RCX_SDC_FILE	Path?	Specifies SDC file to be used for RCX-based STA, which can be different from the one used for implementation.	None	
RCX_RULESETS ^{PDK}	Dict[str, Path]	Map of corner patterns to OpenRCX extraction rules.	None	
STA_THREADS	int?	The maximum number of STA corners to run in parallel. If unset, this will be equal to your machine's thread count.	None	

Antenna Repair

Applies [antenna effect](#) mitigations using global-routing information, then re-runs detailed placement and global routing to legalize any inserted diodes.

An antenna check is once again performed, updating the `route_antennaViolationCount` metric.

Importing



Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	OpenDB Database (.odb)
	Design Exchange Format (.def)

Configuration Variables

Variable Name	Type	Description	Default	Units
PDN_CONNECT_MACROS_TO_GRID	bool	Enables the connection of macros to the top level power grid.	True	
PDN_MACRO_CONNECTIONS	List[str]?	Specifies explicit power connections of internal macros to the top level power grid, in the format: regex matching macro instance names, power domain vdd and ground net names, and macro vdd and ground pin names <pre><instance_name_rx> <vdd_net> <gnd_net> <vdd_pin> <gnd_pin>.</pre>	None	
PDN_ENABLE_GLOBAL_CONNECTIONS	bool	Enables the creation of global connections in PDN generation.	True	
PNR_SDC_FILE	Path?	Specifies the SDC file used during all implementation (PnR) steps	None	
FP_DEF_TEMPLATE	Path?	Points to the DEF file to be used as a template.	None	
RT_CLOCK_MIN_LAYER	str?	The name of lowest layer to be used in routing the clock net.	None	
RT_CLOCK_MAX_LAYER	str?	The name of highest layer to be used in routing the clock net.	None	
GRT_ADJUSTMENT	Decimal	Reduction in the routing capacity of the edges between the cells in the global routing graph for all layers. Values range from 0 to 1. 1 = most reduction, 0 = least reduction.	0.3	

Variable Name	Type	Description	Default	Units
GRT_MACRO_EXTENSION	int	Sets the number of GCells added to the blockages boundaries from macros. A GCell is typically defined in terms of Mx routing tracks. The default GCell size is 15 M3 pitches.	0	
GRT_LAYER_ADJUSTMENTS PDK	List[Decimal]	Layer-specific reductions in the routing capacity of the edges between the cells in the global routing graph, delimited by commas. Values range from 0 through 1.	None	
DIODE_PADDING	int?	Diode cell padding; increases the width of diode cells during placement checks..	None	sites
GRT_ALLOW_CONGESTION	bool	Allow congestion during global routing	False	
GRT_ANTENNA_ITERS	int	The maximum number of iterations for global antenna repairs.	3	
GRT_OVERFLOW_ITERS	int	The maximum number of iterations waiting for the overflow to reach the desired value.	50	
GRT_ANTENNA_MARGIN	int	The margin to over fix antenna violations.	10	%
PL_OPTIMIZE_MIRRORING	bool	Specifies whether or not to run an optimize_mirroring pass whenever detailed placement happens. This pass will mirror the cells whenever possible to optimize the design.	True	
PL_MAX_DISPLACEMENT_X	Decimal	Specifies how far an instance can be moved along the X-axis when finding a site	500	μm

Variable Name	Type	Description	Default	Units
		where it can be placed during detailed placement.		
PL_MAX_DISPLACEMENT_Y	Decimal	Specifies how far an instance can be moved along the Y-axis when finding a site where it can be placed during detailed placement.	100	μm
DPL_CELL_PADDING PDK	Decimal	Cell padding value (in sites) for detailed placement. The number will be integer divided by 2 and placed on both sides. Should be <= global placement.	None	sites

Repair Design (Post-Global Placement)

This is identical to OpenROAD.RepairDesignPostGPL. It is retained for backwards compatibility.

Importing



Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	OpenDB Database (.odb)
	Design Exchange Format (.def)
	Design Constraints (.sdc)
	Verilog Netlist (.nl.v)
	Powered Verilog Netlist (.pnl.v)

Configuration Variables

Variable Name	Type	Description	Default	Units
PDN_CONNECT_MACROS_TO_GRID	bool	Enables the connection of macros to the top level power grid.	True	
PDN_MACRO_CONNECTIONS	List[str]?	Specifies explicit power connections of internal macros to the top level power grid, in the format: regex matching macro instance names, power domain vdd and ground net names, and macro vdd and ground pin names <code><instance_name_rx></code> <code><vdd_net> <gnd_net></code> <code><vdd_pin> <gnd_pin>.</code>	None	
PDN_ENABLE_GLOBAL_CONNECTIONS	bool	Enables the creation of global connections in PDN generation.	True	
PNR_SDC_FILE	Path?	Specifies the SDC file used during all implementation (PnR) steps	None	
FP_DEF_TEMPLATE	Path?	Points to the DEF file to be used as a template.	None	
RT_CLOCK_MIN_LAYER	str?	The name of lowest layer to be used in routing the clock net.	None	
RT_CLOCK_MAX_LAYER	str?	The name of highest layer to be used in routing the clock net.	None	
GRT_ADJUSTMENT	Decimal	Reduction in the routing capacity of the edges between the cells in the global routing graph for all layers. Values range from 0 to 1. 1 = most	0.3	

Variable Name	Type	Description	Default	Units
GRT_MACRO_EXTENSION	int	reduction, 0 = least reduction.	0	
GRT_LAYER_ADJUSTMENTS	List[Decimal] PDK	Sets the number of GCells added to the blockages boundaries from macros. A GCell is typically defined in terms of Mx routing tracks. The default GCell size is 15 M3 pitches.	None	
DIODE_PADDING	int?	Layer-specific reductions in the routing capacity of the edges between the cells in the global routing graph, delimited by commas. Values range from 0 through 1.	None	sites
GRT_ALLOW_CONGESTION	bool	Diode cell padding; increases the width of diode cells during placement checks..	False	
GRT_ANTENNA_ITERS	int	Allow congestion during global routing	3	
GRT_OVERFLOW_ITERS	int	The maximum number of iterations for global antenna repairs.	50	
GRT_ANTENNA_MARGIN	int	The maximum number of iterations waiting for the overflow to reach the desired value.	10	%
PL_OPTIMIZE_MIRRORING	bool	The margin to over fix antenna violations.	True	
		Specifies whether or not to run an optimize_mirroring pass whenever detailed placement happens. This pass will mirror the cells		

Variable Name	Type	Description	Default	Units
		whenever possible to optimize the design.		
PL_MAX_DISPLACEMENT_X	Decimal	Specifies how far an instance can be moved along the X-axis when finding a site where it can be placed during detailed placement.	500	μm
PL_MAX_DISPLACEMENT_Y	Decimal	Specifies how far an instance can be moved along the Y-axis when finding a site where it can be placed during detailed placement.	100	μm
DPL_CELL_PADDING ^{PDK}	Decimal	Cell padding value (in sites) for detailed placement. The number will be integer divided by 2 and placed on both sides. Should be <= global placement.	None	sites
RSZ_DONT_TOUCH_RX	str	A single regular expression designating nets or instances as "don't touch" by design repairs or resizer optimizations.	\$^	
RSZ_DONT_TOUCH_LIST	List[str]?	A list of nets and instances as "don't touch" by design repairs or resizer optimizations.	None	
RSZ_CORNERS	List[str]?	A list of fully-qualified IPVT corners to use during resizer optimizations. If unspecified, the value for STA_CORNERS from the PDK will be used.	None	

Variable Name	Type	Description	Default	Units
DESIGN_REPAIR_BUFFER_INPUT_PORTS	bool	Specifies whether or not to insert buffers on input ports when design repairs are run.	True	
DESIGN_REPAIR_BUFFER_OUTPUT_PORTS	bool	Specifies whether or not to insert buffers on output ports when design repairs are run.	True	
DESIGN_REPAIR_TIE_FANOUT	bool	Specifies whether or not to repair tie cells fanout when design repairs are run.	True	
DESIGN_REPAIR_TIE_SEPARATION	bool	Allows tie separation when performing design repairs.	False	
DESIGN_REPAIR_MAX_WIRE_LENGTH	Decimal	Specifies the maximum wire length cap used by resizer to insert buffers during design repair. If set to 0, no buffers will be inserted.	0	μm
DESIGN_REPAIR_MAX_SLEW_PCT	Decimal	Specifies a margin for the slews during design repair.	20	%
DESIGN_REPAIR_MAX_CAP_PCT	Decimal	Specifies a margin for the capacitances during design repair.	20	%
DESIGN_REPAIR_REMOVE_BUFFERS	bool	Invokes OpenROAD's remove_buffers command to remove buffers from synthesis, which gives OpenROAD more flexibility when buffering nets.	False	

Repair Design (Post-Global Placement)

Runs a number of design "repairs" on a global-placed ODB file.

Importing



Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	OpenDB Database (.odb)
	Design Exchange Format (.def)
	Design Constraints (.sdc)
	Verilog Netlist (.nl.v)
	Powered Verilog Netlist (.pnl.v)

Configuration Variables

Variable Name	Type	Description	Default	Units
PDN_CONNECT_MACROS_TO_GRID	bool	Enables the connection of macros to the top level power grid.	True	
PDN_MACRO_CONNECTIONS	List[str]?	Specifies explicit power connections of internal macros to the top level power grid, in the format: regex matching macro instance names, power domain vdd and ground net names, and macro vdd and ground pin names <code><instance_name_rx></code> <code><vdd_net> <gnd_net></code> <code><vdd_pin> <gnd_pin>.</code>	None	
PDN_ENABLE_GLOBAL_CONNECTIONS	bool	Enables the creation of global connections in PDN generation.	True	
PNR_SDC_FILE	Path?	Specifies the SDC file used during all implementation (PnR) steps	None	
FP_DEF_TEMPLATE	Path?	Points to the DEF file to be used as a template.	None	
RT_CLOCK_MIN_LAYER	str?	The name of lowest layer to be used in routing the clock net.	None	
RT_CLOCK_MAX_LAYER	str?	The name of highest layer to be used in routing the clock net.	None	
GRT_ADJUSTMENT	Decimal	Reduction in the routing capacity of the edges between the cells in the global routing graph for all layers. Values range from 0 to 1. 1 = most	0.3	

Variable Name	Type	Description	Default	Units
GRT_MACRO_EXTENSION	int	reduction, 0 = least reduction.	0	
GRT_LAYER_ADJUSTMENTS	List[Decimal] PDK	Sets the number of GCells added to the blockages boundaries from macros. A GCell is typically defined in terms of Mx routing tracks. The default GCell size is 15 M3 pitches.	None	
DIODE_PADDING	int?	Layer-specific reductions in the routing capacity of the edges between the cells in the global routing graph, delimited by commas. Values range from 0 through 1.	None	sites
GRT_ALLOW_CONGESTION	bool	Diode cell padding; increases the width of diode cells during placement checks..	False	
GRT_ANTENNA_ITERS	int	Allow congestion during global routing	3	
GRT_OVERFLOW_ITERS	int	The maximum number of iterations for global antenna repairs.	50	
GRT_ANTENNA_MARGIN	int	The maximum number of iterations waiting for the overflow to reach the desired value.	10	%
PL_OPTIMIZE_MIRRORING	bool	The margin to over fix antenna violations.	True	
		Specifies whether or not to run an optimize_mirroring pass whenever detailed placement happens. This pass will mirror the cells		

Variable Name	Type	Description	Default	Units
		whenever possible to optimize the design.		
PL_MAX_DISPLACEMENT_X	Decimal	Specifies how far an instance can be moved along the X-axis when finding a site where it can be placed during detailed placement.	500	μm
PL_MAX_DISPLACEMENT_Y	Decimal	Specifies how far an instance can be moved along the Y-axis when finding a site where it can be placed during detailed placement.	100	μm
DPL_CELL_PADDING ^{PDK}	Decimal	Cell padding value (in sites) for detailed placement. The number will be integer divided by 2 and placed on both sides. Should be <= global placement.	None	sites
RSZ_DONT_TOUCH_RX	str	A single regular expression designating nets or instances as "don't touch" by design repairs or resizer optimizations.	\$^	
RSZ_DONT_TOUCH_LIST	List[str]?	A list of nets and instances as "don't touch" by design repairs or resizer optimizations.	None	
RSZ_CORNERS	List[str]?	A list of fully-qualified IPVT corners to use during resizer optimizations. If unspecified, the value for STA_CORNERS from the PDK will be used.	None	

Variable Name	Type	Description	Default	Units
DESIGN_REPAIR_BUFFER_INPUT_PORTS	bool	Specifies whether or not to insert buffers on input ports when design repairs are run.	True	
DESIGN_REPAIR_BUFFER_OUTPUT_PORTS	bool	Specifies whether or not to insert buffers on output ports when design repairs are run.	True	
DESIGN_REPAIR_TIE_FANOUT	bool	Specifies whether or not to repair tie cells fanout when design repairs are run.	True	
DESIGN_REPAIR_TIE_SEPARATION	bool	Allows tie separation when performing design repairs.	False	
DESIGN_REPAIR_MAX_WIRE_LENGTH	Decimal	Specifies the maximum wire length cap used by resizer to insert buffers during design repair. If set to 0, no buffers will be inserted.	0	μm
DESIGN_REPAIR_MAX_SLEW_PCT	Decimal	Specifies a margin for the slews during design repair.	20	%
DESIGN_REPAIR_MAX_CAP_PCT	Decimal	Specifies a margin for the capacitances during design repair.	20	%
DESIGN_REPAIR_REMOVE_BUFFERS	bool	Invokes OpenROAD's remove_buffers command to remove buffers from synthesis, which gives OpenROAD more flexibility when buffering nets.	False	

Repair Design (Post-Global Routing)

Runs a number of design "repairs" on a global-routed ODB file.

Importing



Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	OpenDB Database (.odb)
	Design Exchange Format (.def)
	Design Constraints (.sdc)
	Verilog Netlist (.nl.v)
	Powered Verilog Netlist (.pnl.v)

Configuration Variables

Variable Name	Type	Description	Default	Units
PDN_CONNECT_MACROS_TO_GRID	bool	Enables the connection of macros to the top level power grid.	True	
PDN_MACRO_CONNECTIONS	List[str]?	Specifies explicit power connections of internal macros to the top level power grid, in the format: regex matching macro instance names, power domain vdd and ground net names, and macro vdd and ground pin names <code><instance_name_rx></code> <code><vdd_net> <gnd_net></code> <code><vdd_pin> <gnd_pin>.</code>	None	
PDN_ENABLE_GLOBAL_CONNECTIONS	bool	Enables the creation of global connections in PDN generation.	True	
PNR_SDC_FILE	Path?	Specifies the SDC file used during all implementation (PnR) steps	None	
FP_DEF_TEMPLATE	Path?	Points to the DEF file to be used as a template.	None	
RT_CLOCK_MIN_LAYER	str?	The name of lowest layer to be used in routing the clock net.	None	
RT_CLOCK_MAX_LAYER	str?	The name of highest layer to be used in routing the clock net.	None	
GRT_ADJUSTMENT	Decimal	Reduction in the routing capacity of the edges between the cells in the global routing graph for all layers. Values range from 0 to 1. 1 = most	0.3	

Variable Name	Type	Description	Default	Units
GRT_MACRO_EXTENSION	int	reduction, 0 = least reduction.	0	
GRT_LAYER_ADJUSTMENTS	List[Decimal] PDK	Sets the number of GCells added to the blockages boundaries from macros. A GCell is typically defined in terms of Mx routing tracks. The default GCell size is 15 M3 pitches.	None	
DIODE_PADDING	int?	Layer-specific reductions in the routing capacity of the edges between the cells in the global routing graph, delimited by commas. Values range from 0 through 1.	None	sites
GRT_ALLOW_CONGESTION	bool	Diode cell padding; increases the width of diode cells during placement checks..	False	
GRT_ANTENNA_ITERS	int	Allow congestion during global routing	3	
GRT_OVERFLOW_ITERS	int	The maximum number of iterations for global antenna repairs.	50	
GRT_ANTENNA_MARGIN	int	The maximum number of iterations waiting for the overflow to reach the desired value.	10	%
PL_OPTIMIZE_MIRRORING	bool	The margin to over fix antenna violations.	True	
		Specifies whether or not to run an optimize_mirroring pass whenever detailed placement happens. This pass will mirror the cells		

Variable Name	Type	Description	Default	Units
		whenever possible to optimize the design.		
PL_MAX_DISPLACEMENT_X	Decimal	Specifies how far an instance can be moved along the X-axis when finding a site where it can be placed during detailed placement.	500	μm
PL_MAX_DISPLACEMENT_Y	Decimal	Specifies how far an instance can be moved along the Y-axis when finding a site where it can be placed during detailed placement.	100	μm
DPL_CELL_PADDING ^{PDK}	Decimal	Cell padding value (in sites) for detailed placement. The number will be integer divided by 2 and placed on both sides. Should be <= global placement.	None	sites
RSZ_DONT_TOUCH_RX	str	A single regular expression designating nets or instances as "don't touch" by design repairs or resizer optimizations.	\$^	
RSZ_DONT_TOUCH_LIST	List[str]?	A list of nets and instances as "don't touch" by design repairs or resizer optimizations.	None	
RSZ_CORNERS	List[str]?	A list of fully-qualified IPVT corners to use during resizer optimizations. If unspecified, the value for STA_CORNERS from the PDK will be used.	None	

Variable Name	Type	Description	Default	Units
GRT_DESIGN_REPAIR_MAX_WIRE_LENGTH	Decimal	Specifies the maximum wire length cap used by resizer to insert buffers during post-grt design repair. If set to 0, no buffers will be inserted.	0	μm
GRT_DESIGN_REPAIR_MAX_SLEW_PCT	Decimal	Specifies a margin for the slews during post-grt design repair.	10	%
GRT_DESIGN_REPAIR_MAX_CAP_PCT	Decimal	Specifies a margin for the capacitances during design post-grt repair.	10	%

Resizer Timing Optimizations (Post-Clock Tree Synthesis)

First attempt to meet timing requirements for a cell based on basic timing information after clock tree synthesis.

Standard cells may be resized, and buffer cells may be inserted to ensure that no hold violations exist and no setup violations exist at the current clock.

Importing



Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	OpenDB Database (.odb)
	Design Exchange Format (.def)
	Design Constraints (.sdc)
	Verilog Netlist (.nl.v)
	Powered Verilog Netlist (.pnl.v)

Configuration Variables

Variable Name	Type	Description	Default	Units
PDN_CONNECT_MACROS_TO_GRID	bool	Enables the connection of macros to the top level power grid.	True	
PDN_MACRO_CONNECTIONS	List[str]?	Specifies explicit power connections of internal macros to the top level power grid, in the format: regex matching macro instance names, power domain vdd and ground net names, and macro vdd and ground pin names <instance_name_rx> <vdd_net> <gnd_net> <vdd_pin> <gnd_pin>.	None	
PDN_ENABLE_GLOBAL_CONNECTIONS	bool	Enables the creation of global connections in PDN generation.	True	
PNR_SDC_FILE	Path?	Specifies the SDC file used during all implementation (PnR) steps	None	
FP_DEF_TEMPLATE	Path?	Points to the DEF file to be used as a template.	None	
RT_CLOCK_MIN_LAYER	str?	The name of lowest layer to be used in routing the clock net.	None	
RT_CLOCK_MAX_LAYER	str?	The name of highest layer to be used in routing the clock net.	None	
GRT_ADJUSTMENT	Decimal	Reduction in the routing capacity of the edges between the cells in the global routing graph for all layers. Values range from 0 to 1. 1 = most reduction, 0 = least reduction.	0.3	

Variable Name	Type	Description	Default	Units
GRT_MACRO_EXTENSION	int	Sets the number of GCells added to the blockages boundaries from macros. A GCell is typically defined in terms of Mx routing tracks. The default GCell size is 15 M3 pitches.	0	
GRT_LAYER_ADJUSTMENTS PDK	List[Decimal]	Layer-specific reductions in the routing capacity of the edges between the cells in the global routing graph, delimited by commas. Values range from 0 through 1.	None	
DIODE_PADDING	int?	Diode cell padding; increases the width of diode cells during placement checks..	None	sites
GRT_ALLOW_CONGESTION	bool	Allow congestion during global routing	False	
GRT_ANTENNA_ITERS	int	The maximum number of iterations for global antenna repairs.	3	
GRT_OVERFLOW_ITERS	int	The maximum number of iterations waiting for the overflow to reach the desired value.	50	
GRT_ANTENNA_MARGIN	int	The margin to over fix antenna violations.	10	%
PL_OPTIMIZE_MIRRORING	bool	Specifies whether or not to run an optimize_mirroring pass whenever detailed placement happens. This pass will mirror the cells whenever possible to optimize the design.	True	
PL_MAX_DISPLACEMENT_X	Decimal	Specifies how far an instance can be moved	500	μm

Variable Name	Type	Description	Default	Units
		along the X-axis when finding a site where it can be placed during detailed placement.		
PL_MAX_DISPLACEMENT_Y	Decimal	Specifies how far an instance can be moved along the Y-axis when finding a site where it can be placed during detailed placement.	100	μm
DPL_CELL_PADDING PDK	Decimal	Cell padding value (in sites) for detailed placement. The number will be integer divided by 2 and placed on both sides. Should be <= global placement.	None	sites
RSZ_DONT_TOUCH_RX	str	A single regular expression designating nets or instances as “don’t touch” by design repairs or resizer optimizations.	\$^	
RSZ_DONT_TOUCH_LIST	List[str]?	A list of nets and instances as “don’t touch” by design repairs or resizer optimizations.	None	
RSZ_CORNERS	List[str]?	A list of fully-qualified IPVT corners to use during resizer optimizations. If unspecified, the value for STA_CORNERS from the PDK will be used.	None	
PL_RESIZER_HOLD_SLACK_MARGIN	Decimal	Specifies a time margin for the slack when fixing hold violations. Normally the resizer will stop when it reaches zero slack. This option allows you to overfix.	0.1	ns

Variable Name	Type	Description	Default	Units
PL_RESIZER_SETUP_SLACK_MARGIN	Decimal	Specifies a time margin for the slack when fixing setup violations.	0.05	ns
PL_RESIZER_HOLD_MAX_BUFFER_PCT	Decimal	Specifies a max number of buffers to insert to fix hold violations. This number is calculated as a percentage of the number of instances in the design.	50	
PL_RESIZER_SETUP_MAX_BUFFER_PCT	Decimal	Specifies a max number of buffers to insert to fix setup violations. This number is calculated as a percentage of the number of instances in the design.	50	%
PL_RESIZER_ALLOW_SETUP_VIOS	bool	Allows the creation of setup violations when fixing hold violations. Setup violations are less dangerous as they simply mean a chip may not run at its rated speed, however, chips with hold violations are essentially dead-on-arrival.	False	
PL_RESIZER_GATE_CLONING	bool	Enables gate cloning when attempting to fix setup violations	True	

Resizer Timing Optimizations (Post-Global Routing)

Second attempt to meet timing requirements for a cell based on timing information after estimating resistance and capacitance values based on global routing.

Standard cells may be resized, and buffer cells may be inserted to ensure that no hold violations exist and no setup violations exist at the current clock.

Importing



Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	OpenDB Database (.odb)
	Design Exchange Format (.def)
	Design Constraints (.sdc)
	Verilog Netlist (.nl.v)
	Powered Verilog Netlist (.pnl.v)

Configuration Variables

Variable Name	Type	Description	Default	Units
PDN_CONNECT_MACROS_TO_GRID	bool	Enables the connection of macros to the top level power grid.	True	
PDN_MACRO_CONNECTIONS	List[str]?	Specifies explicit power connections of internal macros to the top level power grid, in the format: regex matching macro instance names, power domain vdd and ground net names, and macro vdd and ground pin names <code><instance_name_rx></code> <code><vdd_net> <gnd_net></code> <code><vdd_pin> <gnd_pin>.</code>	None	
PDN_ENABLE_GLOBAL_CONNECTIONS	bool	Enables the creation of global connections in PDN generation.	True	
PNR_SDC_FILE	Path?	Specifies the SDC file used during all implementation (PnR) steps	None	
FP_DEF_TEMPLATE	Path?	Points to the DEF file to be used as a template.	None	
RT_CLOCK_MIN_LAYER	str?	The name of lowest layer to be used in routing the clock net.	None	
RT_CLOCK_MAX_LAYER	str?	The name of highest layer to be used in routing the clock net.	None	
GRT_ADJUSTMENT	Decimal	Reduction in the routing capacity of the edges between the cells in the global routing graph for all layers. Values range from 0 to 1. 1 = most	0.3	

Variable Name	Type	Description	Default	Units
GRT_MACRO_EXTENSION	int	reduction, 0 = least reduction.		
GRT_LAYER_ADJUSTMENTS PDK	List[Decimal]	Sets the number of GCells added to the blockages boundaries from macros. A GCell is typically defined in terms of Mx routing tracks. The default GCell size is 15 M3 pitches.	0	
DIODE_PADDING	int?	Layer-specific reductions in the routing capacity of the edges between the cells in the global routing graph, delimited by commas. Values range from 0 through 1.	None	
GRT_ALLOW_CONGESTION	bool	Diode cell padding; increases the width of diode cells during placement checks..	None	sites
GRT_ANTENNA_ITERS	int	Allow congestion during global routing	False	
GRT_OVERFLOW_ITERS	int	The maximum number of iterations for global antenna repairs.	3	
GRT_ANTENNA_MARGIN	int	The maximum number of iterations waiting for the overflow to reach the desired value.	50	
PL_OPTIMIZE_MIRRORING	bool	The margin to over fix antenna violations.	10	%
		Specifies whether or not to run an optimize_mirroring pass whenever detailed placement happens. This pass will mirror the cells	True	

Variable Name	Type	Description	Default	Units
		whenever possible to optimize the design.		
PL_MAX_DISPLACEMENT_X	Decimal	Specifies how far an instance can be moved along the X-axis when finding a site where it can be placed during detailed placement.	500	μm
PL_MAX_DISPLACEMENT_Y	Decimal	Specifies how far an instance can be moved along the Y-axis when finding a site where it can be placed during detailed placement.	100	μm
DPL_CELL_PADDING ^{PDK}	Decimal	Cell padding value (in sites) for detailed placement. The number will be integer divided by 2 and placed on both sides. Should be <= global placement.	None	sites
RSZ_DONT_TOUCH_RX	str	A single regular expression designating nets or instances as “don’t touch” by design repairs or resizer optimizations.	\$^	
RSZ_DONT_TOUCH_LIST	List[str]?	A list of nets and instances as “don’t touch” by design repairs or resizer optimizations.	None	
RSZ_CORNERS	List[str]?	A list of fully-qualified IPVT corners to use during resizer optimizations. If unspecified, the value for STA_CORNERS from the PDK will be used.	None	

Variable Name	Type	Description	Default	Units
GRT_RESIZER_HOLD_SLACK_MARGIN	Decimal	Specifies a time margin for the slack when fixing hold violations. Normally the resizer will stop when it reaches zero slack. This option allows you to overfix.	0.05	ns
GRT_RESIZER_SETUP_SLACK_MARGIN	Decimal	Specifies a time margin for the slack when fixing setup violations.	0.025	ns
GRT_RESIZER_HOLD_MAX_BUFFER_PCT	Decimal	Specifies a max number of buffers to insert to fix hold violations. This number is calculated as a percentage of the number of instances in the design.	50	%
GRT_RESIZER_SETUP_MAX_BUFFER_PCT	Decimal	Specifies a max number of buffers to insert to fix setup violations. This number is calculated as a percentage of the number of instances in the design.	50	%
GRT_RESIZER_ALLOW_SETUP_VIOS	bool	Allows setup violations when fixing hold.	False	
GRT_RESIZER_GATE_CLONING	bool	Enables gate cloning when attempting to fix setup violations	True	

Static Timing Analysis (Mid-PnR)

Performs [Static Timing Analysis](#) using OpenROAD on an OpenROAD database, mid-PnR, with estimated values for parasitics.

Importing



Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	

Configuration Variables

Variable Name	Type	Description	Default	Units
PDN_CONNECT_MACROS_TO_GRID	bool	Enables the connection of macros to the top level power grid.	True	
PDN_MACRO_CONNECTIONS	List[str]?	Specifies explicit power connections of internal macros to the top level power grid, in the format: regex matching macro instance names, power domain vdd and ground net names, and macro vdd and ground pin names <code><instance_name_rx> <vdd_net></code> <code><gnd_net> <vdd_pin> <gnd_pin>.</code>	None	
PDN_ENABLE_GLOBAL_CONNECTIONS	bool	Enables the creation of global connections in PDN generation.	True	
PNR_SDC_FILE	Path?	Specifies the SDC file used during all implementation (PnR) steps	None	
FP_DEF_TEMPLATE	Path?	Points to the DEF file to be used as a template.	None	

Static Timing Analysis (Post-PnR)

Performs multi-corner [Static Timing Analysis](#) using OpenSTA on the post-PnR Verilog netlist, with extracted parasitics for both the top-level module and any associated macros.

Importing



Inputs and Outputs

Inputs	Outputs
Verilog Netlist (.nl.v)	Standard Delay Format (.sdf)
Standard Parasitics Extraction Format (.spf)	Design Constraints (.sdc)
OpenDB Database (.odb)	LIB Timing Library Format (.lib)

Configuration Variables

Variable Name	Type	Description	Default	Units
PDN_CONNECT_MACROS_TO_GRID	bool	Enables the connection of macros to the top level power grid.	True	
PDN_MACRO_CONNECTIONS	List[str]?	Specifies explicit power connections of internal macros to the top level power grid, in the format: regex matching macro instance names, power domain vdd and ground net names, and macro vdd and ground pin names <instance_name_rx> <vdd_net> <gnd_net> <vdd_pin> <gnd_pin>.	None	
PDN_ENABLE_GLOBAL_CONNECTIONS	bool	Enables the creation of global connections in PDN generation.	True	
PNR_SDC_FILE	Path?	Specifies the SDC file used during all implementation (PnR) steps	None	
FP_DEF_TEMPLATE	Path?	Points to the DEF file to be used as a template.	None	
STA_MACRO_PRIORITIZE_NL	bool	Prioritize the use of Netlists + SPEF files over LIB files if available for Macros. Useful if extraction was done using OpenROAD, where SPEF files are far more accurate.	True	
STA_MAX_VIOLATOR_COUNT	int?	Maximum number of violators to list in violator_list.rpt	None	
EXTRA_SPEFS	List[(str Path)]?	A variable that only exists for backwards compatibility with OpenLane <2.0.0 and should not be used by new designs.	None	
STA_THREADS	int?	The maximum number of STA corners to run in parallel. If unset, this will be equal to your machine's thread count.	None	

Variable Name	Type	Description	Default	Units
SIGNOFF_SDC_FILE	Path?	Specifies the SDC file for STA during signoff	None	

Static Timing Analysis (Pre-PnR)

Performs hierarchical [Static Timing Analysis](#) using OpenSTA on the pre-PnR Verilog netlist, with all available timing information for standard cells and macros for multiple corners.

If timing information is not available for a Macro, the macro in question will be black-boxed.

Importing



Inputs and Outputs

Inputs	Outputs
Verilog Netlist (.nl.v)	Standard Delay Format (.sdf)
	Design Constraints (.sdc)

Configuration Variables

Variable Name	Type	Description	Default	Units
PDN_CONNECT_MACROS_TO_GRID	bool	Enables the connection of macros to the top level power grid.	True	
PDN_MACRO_CONNECTIONS	List[str]?	Specifies explicit power connections of internal macros to the top level power grid, in the format: regex matching macro instance names, power domain vdd and ground net names, and macro vdd and ground pin names <instance_name_rx> <vdd_net> <gnd_net> <vdd_pin> <gnd_pin>.	None	
PDN_ENABLE_GLOBAL_CONNECTIONS	bool	Enables the creation of global connections in PDN generation.	True	
PNR_SDC_FILE	Path?	Specifies the SDC file used during all implementation (PnR) steps	None	
FP_DEF_TEMPLATE	Path?	Points to the DEF file to be used as a template.	None	
STA_MACRO_PRIORITIZE_NL	bool	Prioritize the use of Netlists + SPEF files over LIB files if available for Macros. Useful if extraction was done using OpenROAD, where SPEF files are far more accurate.	True	
STA_MAX_VIOLATOR_COUNT	int?	Maximum number of violators to list in violator_list.rpt	None	
EXTRA_SPEFS	List[(str Path)]?	A variable that only exists for backwards compatibility with OpenLane <2.0.0 and should not be used by new designs.	None	
STA_THREADS	int?	The maximum number of STA corners to run in parallel. If unset, this will be equal to your machine's thread count.	None	

Tap/Decap Insertion

Places well TAP cells across a floorplan, as well as end-cap cells at the edges of the floorplan.

Importing >

Inputs and Outputs

Inputs	Outputs
OpenDB Database (.odb)	OpenDB Database (.odb)
	Design Exchange Format (.def)
	Design Constraints (.sdc)
	Verilog Netlist (.nl.v)
	Powered Verilog Netlist (.pnl.v)

Configuration Variables

Variable Name	Type	Description	Default	Units
PDN_CONNECT_MACROS_TO_GRID	bool	Enables the connection of macros to the top level power grid.	True	
PDN_MACRO_CONNECTIONS	List[str]?	Specifies explicit power connections of internal macros to the top level power grid, in the format: regex matching macro instance names, power domain vdd and ground net names, and macro vdd and ground pin names <code><instance_name_rx> <vdd_net></code> <code><gnd_net> <vdd_pin> <gnd_pin>.</code>	None	
PDN_ENABLE_GLOBAL_CONNECTIONS	bool	Enables the creation of global connections in PDN generation.	True	
PNR_SDC_FILE	Path?	Specifies the SDC file used during all implementation (PnR) steps	None	
FP_DEF_TEMPLATE	Path?	Points to the DEF file to be used as a template.	None	
FP_MACRO_HORIZONTAL_HALO	Decimal	Specify the horizontal halo size around macros while cutting rows.	10	μm
FP_MACRO_VERTICAL_HALO	Decimal	Specify the vertical halo size around macros while cutting rows.	10	μm

Verilator

Verilator Lint

Lints inputs RTL Verilog files.

The linting is done with the defines for power and ground inputs on, as more macros are available with powered netlists than unpowered netlists.

Importing**Configuration Variables**

Variable Name	Type	Description	Default	Units
VERILOG_FILES	List[Path]	The paths of the design's Verilog files.	None	
VERILOG_POWER_DEFINE	str	Specifies the name of the define used to guard power and ground connections in the input RTL.	USE_POWER_PINS	
LINTER_INCLUDE_PDK_MODELS	bool	Include Verilog models of the PDK	False	
LINTER_RELATIVE_INCLUDES	bool	When a file references an include file, resolve the filename relative to the path of the referencing file, instead of relative to the current directory.	True	
LINTER_ERROR_ON_LATCH	bool	When a latch is inferred by an <code>always</code> block that is not explicitly marked as <code>always_latch</code> , report this as a linter error.	True	
VERILOG_DEFINES	List[str]?	Preprocessor defines for input Verilog files	None	
LINTER_DEFINES	List[str]?	Linter-specific preprocessor definitions; overrides VERILOG_DEFINES for the lint step if exists	None	

Yosys**RTL/Netlist Equivalence Check****Importing**

Inputs and Outputs

Inputs	Outputs
Verilog Netlist (.nl.v)	

Configuration Variables

Variable Name	Type	Description	Default	Units
<code>SYNTH_LATCH_MAP</code> PDK	Path?	A path to a file containing the latch mapping for Yosys.	None	
<code>SYNTH_TRISTATE_MAP</code> PDK	Path?	A path to a file containing the tri-state buffer mapping for Yosys.	None	
<code>SYNTH_CSA_MAP</code> PDK	Path?	A path to a file containing the carry-select adder mapping for Yosys.	None	
<code>SYNTH_RCA_MAP</code> PDK	Path?	A path to a file containing the ripple-carry adder mapping for Yosys.	None	
<code>SYNTH_FA_MAP</code> PDK	Path?	A path to a file containing the full adder mapping for Yosys.	None	
<code>SYNTH_MUX_MAP</code> PDK	Path?	A path to a file containing the mux mapping for Yosys.	None	
<code>SYNTH_MUX4_MAP</code> PDK	Path?	A path to a file containing the mux4 mapping for Yosys.	None	
<code>USE_LIGHTER</code>	bool	Activates Lighter, an experimental plugin that attempts to optimize clock-gated flip-flops.	False	
<code>LIGHTER_DFF_MAP</code>	Path?	An override to the custom DFF map file provided for the given SCL by Lighter.	None	
<code>YOSYS_LOG_LEVEL</code>	'ALL' 'WARNING' 'ERROR'	Which log level for Yosys. At WARNING or higher, the initialization splash is also disabled.	ALL	
<code>EQY_SCRIPT</code>	Path?	An optional override for the automatically generated EQY script for more complex designs.	None	
<code>MACRO_PLACEMENT_CFG</code>	Path?	This step will warn if this deprecated variable is used, as it indicates Macros are used without the new Macro object.	None	
<code>EQY_FORCE_ACCEPT_PDK</code>	bool	Attempt to run EQY even if the PDK's Verilog models are supported	False	

Variable Name	Type	Description	Default	Units
		by this step. Will likely result in a failure.		

Generate JSON Header

Importing >

Inputs and Outputs

Inputs	Outputs
	Design JSON Header File (.h.json)

Configuration Variables

Variable Name	Type	Description	Default	Units
<code>SYNTH_LATCH_MAP</code> ^{PDK}	Path?	A path to a file containing the latch mapping for Yosys.	None	
<code>SYNTH_TRISTATE_MAP</code> ^{PDK}	Path?	A path to a file containing the tri-state buffer mapping for Yosys.	None	
<code>SYNTH_CSA_MAP</code> ^{PDK}	Path?	A path to a file containing the carry-select adder mapping for Yosys.	None	
<code>SYNTH_RCA_MAP</code> ^{PDK}	Path?	A path to a file containing the ripple-carry adder mapping for Yosys.	None	
<code>SYNTH_FA_MAP</code> ^{PDK}	Path?	A path to a file containing the full adder mapping for Yosys.	None	
<code>SYNTH_MUX_MAP</code> ^{PDK}	Path?	A path to a file containing the mux mapping for Yosys.	None	
<code>SYNTH_MUX4_MAP</code> ^{PDK}	Path?	A path to a file containing the mux4 mapping for Yosys.	None	
<code>USE_LIGHTER</code>	bool	Activates Lighter, an experimental plugin that attempts to optimize clock-gated flip-flops.	False	
<code>LIGHTER_DFF_MAP</code>	Path?	An override to the custom DFF map file provided for the given SCL by Lighter.	None	
<code>YOSYS_LOG_LEVEL</code>	'ALL' 'WARNING' 'ERROR'	Which log level for Yosys. At WARNING or higher, the initialization splash is also disabled.	ALL	
<code>VERILOG_FILES</code>	List[Path]	The paths of the design's Verilog files.	None	
<code>VERILOG_DEFINES</code>	List[str]?	Preprocessor defines for input Verilog files.	None	

Variable Name	Type	Description	Default	Units
VERILOG_POWER_DEFINE	str	Specifies the name of the define used to guard power and ground connections in the input RTL.	USE_POWER_PINS	
VERILOG_INCLUDE_DIRS	List[str]?	Specifies the Verilog <code>include</code> directories.	None	
USE_SYNLIG	bool	Use the Synlig plugin to process files, which has better SystemVerilog parsing capabilities but may not be compatible with all Yosys commands and attributes.	False	
SYNLIG_DEFER	bool	Uses -defer flag when reading files the Synlig plugin, which may improve performance by reading each file separately, but is experimental.	False	

Synthesis

Performs synthesis and technology mapping on Verilog RTL files using Yosys and ABC, emitting a netlist.

Some metrics will also be extracted and updated, namely:

- `design_instance_count`
- `design_instance_unmapped_count`
- `design_instance_area`

Importing



Inputs and Outputs

Inputs	Outputs
	Verilog Netlist (.nl.v)

Configuration Variables

Variable Name	Type	Description	Default	Units
<code>SYNTH_LATCH_MAP</code> ^{PDK}	Path?	A path to a file containing the latch mapping for Yosys.	None	
<code>SYNTH_TRISTATE_MAP</code> ^{PDK}	Path?	A path to a file containing the tri-state buffer mapping for Yosys.	None	
<code>SYNTH_CSA_MAP</code> ^{PDK}	Path?	A path to a file containing the carry-select adder mapping for Yosys.	None	
<code>SYNTH_RCA_MAP</code> ^{PDK}	Path?	A path to a file containing the ripple-carry adder mapping for Yosys.	None	
<code>SYNTH_FA_MAP</code> ^{PDK}	Path?	A path to a file containing the full adder mapping for Yosys.	None	
<code>SYNTH_MUX_MAP</code> ^{PDK}	Path?	A path to a file containing the mux mapping for Yosys.	None	
<code>SYNTH_MUX4_MAP</code> ^{PDK}	Path?	A path to a file containing the mux4 mapping for Yosys.	None	
<code>USE_LIGHTER</code>	bool	Activates Lighter, an experimental plugin that attempts to optimize clock-gated flip-flops.	False	
<code>LIGHTER_DFF_MAP</code>	Path?	An override to the custom DFF map file provided for the given SCL by Lighter.	None	
<code>YOSYS_LOG_LEVEL</code>	'ALL' 'WARNING'	Which log level for Yosys. At WARNING or	ALL	

Variable Name	Type	Description	Default	Units
	'ERROR'	higher, the initialization splash is also disabled.		
SYNTH_CHECKS_ALLOW_TRISTATE	bool	Ignore multiple-driver warnings if they are connected to tri-state buffers on a best-effort basis.	True	
SYNTH_AUTONAME	bool	Generates names for netlist instances. This results in instance names that can be extremely long, but are more human-readable.	False	
SYNTH_STRATEGY	'AREA 0' 'AREA 1' 'AREA 2' 'AREA 3' 'DELAY 0' 'DELAY 1' 'DELAY 2' 'DELAY 3' 'DELAY 4'	Strategies for abc logic synthesis and technology mapping. AREA strategies usually result in a more compact design, while DELAY strategies usually result in a design that runs at a higher frequency. Please note that there is no way to know which strategy is the best before trying them.	AREA 0	
SYNTH_ABC_BUFFERING	bool	Enables abc cell buffering.	False	
SYNTH_ABC_LEGACY_REFATOR	bool	Replaces the ABC command <code>drf -1</code> with <code>refactor</code> which matches older versions of OpenLane but is more unstable.	False	
SYNTH_ABC_LEGACY_REWRITE	bool	Replaces the ABC command <code>drw -1</code> with	False	

Variable Name	Type	Description	Default	Units
		rewrite which matches older versions of OpenLane but is more unstable.		
SYNTH_DIRECT_WIRE_BUFFERING	bool	Enables inserting buffer cells for directly connected wires.	True	
SYNTH_SPLITNETS	bool	Splits multi-bit nets into single-bit nets. Easier to trace but may not be supported by all tools.	True	
SYNTH_SIZING	bool	Enables abc cell sizing (instead of buffering).	False	
SYNTH_NO_FLAT	bool	A flag that disables flattening the hierarchy during synthesis, only flattening it after synthesis, mapping and optimizations.	False	
SYNTH_SHARE_RESOURCES	bool	A flag that enables yosys to reduce the number of cells by determining shareable resources and merging them.	True	
SYNTH_ADDER_TYPE	'YOSYS' 'FA' 'RCA' 'CSA'	Adder type to which the <i>add</i> and <i>sub</i> operators are mapped to. Possible values are YOSYS/FA/RCA/CSA ; where YOSYS refers to using Yosys internal adder definition, FA refers to full-adder structure, RCA refers to ripple carry adder structure, and CSA	YOSYS	

Variable Name	Type	Description	Default	Units
		refers to carry select adder.		
SYNTH_EXTRA_MAPPING_FILE	Path?	Points to an extra techmap file for yosys that runs right after yosys <code>synth</code> before generic techmap.	None	
SYNTH_PARAMETERS	List[str]?	Key-value pairs to be <code>chparam</code> ed in Yosys, in the format <code>key1=value1</code> .	None	
SYNTH_ELABORATE_ONLY	bool	"Elaborate" the design only without attempting any logic mapping. Useful when dealing with structural Verilog netlists.	False	
SYNTH_ELABORATE_FLATTEN	bool	If <code>SYNTH_ELABORATE_ONLY</code> is specified, this variable controls whether or not the top level should be flattened.	True	
VERILOG_FILES	List[Path]	The paths of the design's Verilog files.	None	
VERILOG_DEFINES	List[str]?	Preprocessor defines for input Verilog files.	None	
VERILOG_POWER_DEFINE	str	Specifies the name of the define used to guard power and ground connections in the input RTL.	USE_POWER_PINS	
VERILOG_INCLUDE_DIRS	List[str]?	Specifies the Verilog <code>include</code> directories.	None	
USE_SYNLIB	bool	Use the Synlib plugin to process files, which has better	False	

Variable Name	Type	Description	Default	Units
		SystemVerilog parsing capabilities but may not be compatible with all Yosys commands and attributes.		
SYNLIG_DEFER	bool	Uses -defer flag when reading files the Synlig plugin, which may improve performance by reading each file separately, but is experimental.	False	

Synthesis (VHDL)

Performs synthesis and technology mapping on VHDL files using Yosys, GHDL and ABC, emitting a netlist.

Some metrics will also be extracted and updated, namely:

- `design_instance_count`
- `design_instance_unmapped_count`
- `design_instance_area`

Importing



Inputs and Outputs

Inputs	Outputs
	Verilog Netlist (.nl.v)

Configuration Variables

Variable Name	Type	Description	Default	Units
SYNTH_LATCH_MAP ^{PDK}	Path?	A path to a file containing the latch mapping for Yosys.	None	
SYNTH_TRISTATE_MAP ^{PDK}	Path?	A path to a file containing the tri-state buffer mapping for Yosys.	None	
SYNTH_CSA_MAP ^{PDK}	Path?	A path to a file containing the carry-select adder mapping for Yosys.	None	
SYNTH_RCA_MAP ^{PDK}	Path?	A path to a file containing the ripple-carry adder mapping for Yosys.	None	
SYNTH_FA_MAP ^{PDK}	Path?	A path to a file containing the full adder mapping for Yosys.	None	
SYNTH_MUX_MAP ^{PDK}	Path?	A path to a file containing the mux mapping for Yosys.	None	
SYNTH_MUX4_MAP ^{PDK}	Path?	A path to a file containing the mux4 mapping for Yosys.	None	
USE_LIGHTER	bool	Activates Lighter, an experimental plugin that attempts to optimize clock-gated flip-flops.	False	
LIGHTER_DFF_MAP	Path?	An override to the custom DFF map file provided for the given SCL by Lighter.	None	
YOSYS_LOG_LEVEL	'ALL' 'WARNING' 'ERROR'	Which log level for Yosys. At WARNING or higher, the initialization splash is also disabled.	ALL	
SYNTH_CHECKS_ALLOW_TRISTATE	bool	Ignore multiple-driver warnings if they are connected to tri-state buffers on a best-effort basis.	True	
SYNTH_AUTONAME	bool	Generates names for netlist instances. This results in instance names that can be	False	

Variable Name	Type	Description	Default	Units
SYNTH_STRATEGY	'AREA 0' 'AREA 1' 'AREA 2' 'AREA 3' 'DELAY 0' 'DELAY 1' 'DELAY 2' 'DELAY 3' 'DELAY 4'	extremely long, but are more human-readable. Strategies for abc logic synthesis and technology mapping. AREA strategies usually result in a more compact design, while DELAY strategies usually result in a design that runs at a higher frequency. Please note that there is no way to know which strategy is the best before trying them.	AREA 0	
SYNTH_ABC_BUFFERING	bool	Enables abc cell buffering.	False	
SYNTH_ABC_LEGACY_REFATOR	bool	Replaces the ABC command drf -1 with refactor which matches older versions of OpenLane but is more unstable.	False	
SYNTH_ABC_LEGACY_REWRITE	bool	Replaces the ABC command drw -1 with rewrite which matches older versions of OpenLane but is more unstable.	False	
SYNTH_DIRECT_WIRE_BUFFERING	bool	Enables inserting buffer cells for directly connected wires.	True	
SYNTH_SPLITNETS	bool	Splits multi-bit nets into single-bit nets. Easier to trace but may not be supported by all tools.	True	
SYNTH_SIZING	bool	Enables abc cell sizing (instead of buffering).	False	
SYNTH_NO_FLAT	bool	A flag that disables flattening the hierarchy during synthesis, only flattening it after synthesis, mapping and optimizations.	False	

Variable Name	Type	Description	Default	Units
SYNTH_SHARE_RESOURCES	bool	A flag that enables yosys to reduce the number of cells by determining shareable resources and merging them.	True	
SYNTH_ADDER_TYPE	'YOSYS' 'FA' 'RCA' 'CSA'	Adder type to which the <code>add</code> and <code>sub</code> operators are mapped to. Possible values are <code>YOSYS/FA/RCA/CSA</code> ; where <code>yosys</code> refers to using Yosys internal adder definition, <code>FA</code> refers to full-adder structure, <code>RCA</code> refers to ripple carry adder structure, and <code>CSA</code> refers to carry select adder.	YOSYS	
SYNTH_EXTRA_MAPPING_FILE	Path?	Points to an extra techmap file for yosys that runs right after yosys <code>synth</code> before generic techmap.	None	
SYNTH_PARAMETERS	List[str]?	Key-value pairs to be chparamed in Yosys, in the format <code>key1=value1</code> .	None	
SYNTH_ELABORATE_ONLY	bool	"Elaborate" the design only without attempting any logic mapping. Useful when dealing with structural Verilog netlists.	False	
SYNTH_ELABORATE_FLATTEN	bool	If <code>SYNTH_ELABORATE_ONLY</code> is specified, this variable controls whether or not the top level should be flattened.	True	
VHDL_FILES	List[Path]	The paths of the design's VHDL files.	None	

Misc

Load Base Design Constraints File

Loads an SDC file specified as a configuration variable into the state object unaltered.

This Step exists for legacy compatibility and should not be used in new flows.

Importing >

Inputs and Outputs

Inputs	Outputs
	Design Constraints (.sdc)

Report Manufacturability (DRC, LVS, Antenna)

Importing >



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