MOSIS Submission Tutorial for ON Semiconductor 0.5u C5F CMOS

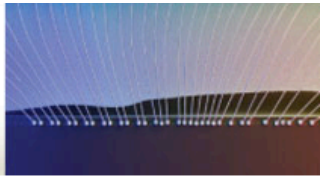
Version 7.0

Example
design
and
project details

MOSIS Project Management

Logged in as Project: 86820 - xtal_chip

To view a project status report, update or cancel an existing project, queue an IC design for fabrication, queue a previously fabricated design for refabrication or submit a test results report.



Project Information

Design Number	86820
Date Submitted	13-JAN-12 09:43:59 am
Project Status	Shipped
Design Layout	Final layout
Fab ID	V21GBX
Project Document(s)	Download
Fabrication Options	EPI
Run Date Requested	23-JAN-2012
Area	2.223 sq millimeters
Checksum	Binary CRC checksum: 3317540580, Binary CRC byte count: 8839168

Administrative Information

Account Name	5695-MEP-INS/UTFSM-E
Account Contact Name	Agustín González
Account Contact E-mail	agustin.gonzalez@usm.cl
Design Contact E-mail	emac@utep.edu
Design Contact Phone	915-490-3488
Cost	V21G: 1 MEP unit(s) is used.
Quantity Ordered	5
ECCN	EAR99 -- student project for MEP Technology ECCN: EAR99
BIS 711 received	Yes
Approved for export	Yes

Design Details

Size in X	1482
Size in Y	1499.7
Wafer Technology	AMI_C5F
Fabrication Restricted to	AMI
Layout Format	GDS
Top Cell Name	final_chip
Fill	MOSIS
Bonding Pad Count (Customer)	28
Bonding Pad Count (MOSIS)	28
Maximum Die Size	7620.0 X 7620.0
Layers (Density)	ACTIVE, CONTACT, GLASS, METAL1(36.7%), METAL2(35.5%), METAL3, N_PLUS_SELECT, N_WELL, PADS, POLY(19.3%), P_PLUS_SELECT, VIA, VIA2
Needs Library Instantiation	N

Packaging Information

Quantity	Packaged	Package Id	Bonding Diagram Received	Bonding Diagram From	Die Thickness (mils)	Production ID Date Shipped
5	Y	DIP28	08-MAR-12	Customer	10	V21G 02-MAY-12

Special Handlings

Special Handling	13-JAN-12 09:43 AM	please package all 5 die in 28-pin ceramic DIP packages with taped lids

Overview

After being assigned a design name, number and password go to:

www.mosis.com/Webforms

Select “fabricate” and fill in the form for the secure https upload option

Secure Web Forms

Fabricate Form

Send WebForm comments and suggestions to: webmaster@mosis.com

Use this form to request fabrication of an IC project. You must know the project's Design Number and Design Password. When you have successfully submitted this form, MOSIS will either wait for you to send your layout to us via secure web form (HTTPS) or via FTP or will attempt to retrieve your layout file via FTP, depending on which Layout Transfer Method you selected. Once your layout file is received and the computed checksum matches the one you declared in this form, your design will be queued for manufacturability review. At the conclusion of the check, you will receive a separate e-mail message. If your design passes manufacturability review, it will be queued for fabrication on the next available run that is compatible with your technology code and meets any foundry restriction you have specified. See the MOSIS Fabrication Schedule for the dates of scheduled runs.

If your layout file has been successfully transferred to MOSIS and your project did not get into the fab queue due to missing or incorrect information (pad count, design size estimate, technology code, lambda, etc), you should use the Update Form to add missing information or correct wrong values.

If your project is already in the fab queue and you want to submit a revised design, you must first cancel fabrication with the Cancel Fabrication Form.

For more detailed information, see the Fabricate Documentation.

Required Parameters

Design Number: 86791 *(5-digit or 6-digit design number assigned to project by MOSIS)*

Design Password: ••••• *(Password you chose at project creation)*

Use your design number

Layout Parameters

Layout Status: (•) Final (ready for fabrication) ( ) Preliminary (not to be fabricated)

Layout Format: ( ) CIF (•) GDS (Select one - see MOSIS Layout Conventions)

Compression/Encryption: (•) Uncompressed ( ) Compressed ( ) PGP-encrypted

Checksum Type: (•) CRC ( ) Traditional "CIF"

Checksum: 2011636139

Count: 741376

Run the crc program on your gds for these two numbers

Top Structure: xtal_chip *(Required only for GDS format)*

Select Layout Transfer Method

Layout Transfer Method: I will upload layout via secure web form (HTTPS) *(Fill out corresponding section below)*

To Send Your Design to MOSIS via Secure Web Form (HTTPS)

HTTP Send Hours: 168 *(Optional hours until expiration - default is 8 hours)*

To Send Your Design to MOSIS via FTP

For help, see the Design File FTP Server FAQ. Server is at ftp.design.mosis.com.

FTP Send Host: *(Name or IP address of host you will send from)*

FTP Send Password: *(Password you will give to ftp server at login)*

Retype Send Password: *(Retype password for verification)*

FTP Send Filename: *(Name of file you will put on ftp server)*

FTP Send Hours: *(Optional hours until expiration - default is 8 hours)*

To Have MOSIS Retrieve Design from You via FTP

FTP Host: (See Submitting Designs Via FTP)

FTP Username: (User name for login, such as "anonymous")

FTP Password:

FTP Filename:

Project Packaging

Fill out this section only if you have not specified packaging parameters yet or if you want to change the previously specified parameters. A new bonding diagram will be generated (if applicable) if there are any non-blank fields in this section. See Project Packaging for detailed help for this section.

	Quantity	Package Name	Rotation in Package	Bonding Diagram Supplier	Downbond Locations
Quantity Packaged:	5	DIP28	Unchanged	Customer	Unchanged (or N/A)
Quantity Unpackaged:		N/A	N/A		

Required if Not Previously Provided

Run Type: Unchanged (Select one)

Run Date Requested: (For non-dedicated runs only. Must match a scheduled date. Example: 24-apr-2011)

Run Name: (Name of previously created dedicated run. See the Create Dedicated Run form.)

IP Included: (Vendor of licensed intellectual property in design (e.g., ARM). Select all that apply.)

☑ Unchanged ☐ None ☐ Aragio ☐ ARM ☐ Virage
☐ Other (Specify in Special Handling)

Fill Authorized: Unchanged (Only applicable to TSMC and ON Semi)

Technology Code: (See Technology Codes and Layer Maps for a list)

Lambda: Unchanged (Select one)

Foundry: Unchanged (Select one)

Substrate Options: Unchanged or N/A (Only for those processes that offer a substrate choice)

Top Metal Options: Unchanged or N/A (Only for TSMC 0.18 and 0.25 processes)

Bonding Options: Unchanged or N/A (Only for IBM processes)

Bumping Options: Unchanged or N/A (Only for IBM C4 (leaded or lead-free) processes)

Intended Disposition: Unchanged (Required by export control regulations)

Design Kit Version: (For IBM design technologies only)

Design Size X: 1500 (In microns)

Design Size Y: 1500 (In microns)

Pad Count: 28

PO Number: (For commercial accounts and MEP packaging)

Quote Id: (For assigned quote or MEP proposal ID only)

Add or Update Information (Optional)

E-mail Address: emac@utep.edu (For confirmations from MOSIS)

Phone Number: 915-490-3488

Design Name: xtal_chip (Name you choose for this project)

Quantity Ordered: 5

Description: (Paragraph describing project)

student project in the MOSIS educational program

Use your email address, phone number and design.

Add or Update Information (Optional)

E-mail Address: emac@utep.edu *(For confirmations from MOSIS)*

Phone Number: 915-490-3488

Design Name: xtal_chip *(Name you choose for this project)*

Quantity Ordered: 5

Description: *(Paragraph describing project)*
student project in the MOSIS educational program

Routing Label: *("Deliver-to" address WITHIN your company)*
Envia a Agustín Gonzalez en la departamento ingeniería electónica

Special Handling: *(Special packaging, shipping or die size requirements)*
package all 5 die in 28 pin ceramic Kyrocera DIP packages with taped lids

Put any information that will make receiving the chips easier

Submit Form Reset Form

Last Updated: September 19, 2005

Notes:

In the case that you have failed to meet minimum layer densities, you may need to introduce additional polygons into the design.

The design to the right failed on the poly layer density. Notice the four rectangles that were added to the dead space around the core but within the pad ring.