Additional Material

There are some cool tutorials and guides on using OpenLane to harden chips. Though do note, guides, especially video tutorials and webinars, tend to become out of date.

Additionally, we are also going to link to academic publications about OpenLane if you are interested in reading and/or citing it.

Text Guides

Official

- OpenLane ReadTheDocs
 - You are probably already here, though! Hi.
- Quick-Start Guide, Caravel User Project ReadTheDocs
 - If you are looking to submit a project for an OpenMPW or ChipIgnite shuttle, start here.
- Digital inverter with OpenLane and Colab, Build Custom Silicon with Google
 - This is a very simple introduction using Google Colab- you do not even need to install anything!

Community

English

- Introduction to OpenMPW, VLSI.jp
- RgGen X OpenMPW Walkthrough

日本語

- OpenMPW入門 改訂版, VLSI.jp
- RgGen × OpenMPWでLSIを焼こう!

Español

Tutoriales de OpenLane/OpenROAD

Videos

- Aboard Caravel, Ahmed Ghazy
- FOSSi Dial-Up Skywater PDK: Fully open source manufacturable PDK for a 130nm process, Tim Ansell
- FOSSi Dial-Up OpenLane, A Digital ASIC Flow for SkyWater 130nm Open PDK, Mohamed Shalan
- OpenLane Overview, Ahmed Ghazy
- Free VLSI Tutorial VSD A complete guide to install OpenLane and Sky130nm PDK
- Sky130 Exploring OpenLane and OpenDB to create a register file, Sylvain Munaut
- Skywater 130nm PDK Initial Discovery, Sylvain Munaut
- VLSI SoC EDA OpenLane with Skywater 130 PDK, Gary Huang

Publications

This is a list of publications about OpenLane, sorted from newest to oldest.

- R. Timothy Edwards, M. Shalan and M. Kassem, "Real Silicon using Open Source EDA," in IEEE Design & Test, doi: 10.1109/MDAT.2021.3050000. Paper
- M. Shalan and T. Edwards, "Building OpenLANE: A 130nm OpenROAD-based Tapeout-Proven Flow: Invited Paper," 2020 IEEE/ACM International Conference On Computer Aided Design (ICCAD), San Diego, CA, USA, 2020, pp. 1-6. Paper
- Ahmed Ghazy and Mohamed Shalan, "OpenLANE: The Open-Source Digital ASIC Implementation Flow", Article No.21, Workshop on Open-Source EDA Technology (WOSET), 2020. Paper



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