

# Universal Flow PDK Configuration Variables

These are variables that are to be defined by a process design kit's configuration files for *all* steps and flows. For a PDK to be compatible with OpenLane, all non-`Optional` variables *must* be given a value.

Like with flow configuration variables, configuration objects can freely override these values.

## Note

`?` indicates an optional variable, i.e., a value that does not need to be implemented by a PDK or an SCL. OpenLane steps are expected to understand that these values may hold a value of `None` in the input configuration and behave accordingly.

## PDK-Level

These are variables that affect the entire PDK.

Variable Name	Type	Description	Units
<code>STD_CELL_LIBRARY</code>	str	Specifies the default standard cell library to be used under the specified PDK. Must be a valid C identifier, i.e., matches the regular expression <code>[_a-zA-Z][_a-zA-Z0-9]+</code> .	
<code>VDD_PIN</code>	str	The power pin for the cells.	
<code>VDD_PIN_VOLTAGE</code>	Decimal	The voltage of the VDD pin.	
<code>GND_PIN</code>	str	The ground pin for the cells.	
<code>WIRE_LENGTH_THRESHOLD</code>	Decimal?	A value above which wire lengths generate warnings.	μm
<code>TECH_LEFS</code>	Dict[str, Path]	Map of corner patterns to technology LEF files. A corner not matched here will not be supported by OpenRCX in the default flow.	
<code>GPIO_PADS_LEF</code>	List[Path]?	Path(s) to GPIO pad LEF file(s).	
<code>GPIO_PADS_LEF_CORE_SIDE</code>	List[Path]?	Path(s) to GPIO pad LEF file(s) as used for routing (?).	
<code>GPIO_PADS_VERILOG</code>	List[Path]?	Path(s) to GPIO pad Verilog models.	
<code>GPIO_PAD_CELLS</code>	List[str]?	A list of pad cell name prefixes.	
<code>PRIMARY_GDSII_STREAMOUT_TOOL</code>	str	Specify the primary GDSII streamout tool for this PDK. For most open-source PDKs, that would be 'magic'.	
<code>DEFAULT_MAX_TRAN</code>	Decimal?	Defines the default maximum transition value used in Synthesis and CTS. A minimum of $0.1 * \text{CLOCK\_PERIOD}$ and this variable, if defined, is used.	ns
<code>SIGNAL_WIRE_RC_LAYERS</code>	List[str]?	Sets estimated signal wire RC values to the average of these layers'. If you provide more than two, the averages are grouped by preferred routing direction and you must provide at least one layer for each routing direction. If unset, tools should use the average of layers between <code>RT_MIN_LAYER</code> and <code>RT_MAX_LAYER</code> . This variable will be moved to the relevant step(s) in the next version of OpenLane.	
<code>CLOCK_WIRE_RC_LAYERS</code>	List[str]?	Sets estimated clock wire RC values to the average of these layers'. If you provide	

Variable Name	Type	Description	Units
		more than two, the averages are grouped by preferred routing direction and you must provide at least one layer for each routing direction. If unset, tools should use the average of layers between RT_MIN_LAYER and RT_MAX_LAYER. This variable will be moved to the relevant step(s) in the next version of OpenLane.	
DEFAULT_CORNER	str	The interconnect/process/voltage/temperature corner (IPVT) to use the characterized lib files compatible with by default.	
STA_CORNERS	List[str]	A list of fully qualified IPVT (Interconnect, transistor Process, Voltage, and Temperature) timing corners on which to conduct multi-corner static timing analysis.	
FP_TRACKS_INFO	Path	A path to the a classic OpenROAD .tracks file. Used by the floorplanner to generate tracks.	
FP_TAPCELL_DIST	Decimal	The distance between tap cell columns.	μm
FP_IO_HLAYER	str	The metal layer on which to place horizontal IO pins, i.e., the top and bottom of the die.	
FP_IO_VLAYER	str	The metal layer on which to place vertical IO pins, i.e., the top and bottom of the die.	
RT_MIN_LAYER	str	The lowest metal layer to route on.	
RT_MAX_LAYER	str	The highest metal layer to route on.	

## SCL-Level

These are variables that affect a specific standard-cell library.

Variable Name	Type	Description	Units
<code>SCL_GROUND_PINS</code>	List[str]	SCL-specific ground pins	
<code>SCL_POWER_PINS</code>	List[str]	SCL-specific power pins	
<code>TRISTATE_CELLS</code>	List[str]?	A list of cell names or wildcards of tri-state buffers.	
<code>FILL_CELL</code>	List[str]	A list of cell names or wildcards of fill cells to be used in fill insertion.	
<code>DECAP_CELL</code>	List[str]	A list of cell names or wildcards of decap cells to be used in fill insertion.	
<code>LIB</code>	Dict[str, List[Path]]	A map from corner patterns to a list of associated liberty files. Exactly one entry must match the <code>DEFAULT_CORNER</code> .	
<code>CELL_LEFS</code>	List[Path]	Path(s) to the cells' LEF file(s).	
<code>CELL_GDS</code>	List[Path]	Path(s) to the cells' GDSII file(s).	
<code>CELL_VERILOG_MODELS</code>	List[Path]?	Path(s) to cells' Verilog model(s)	
<code>CELL_BB_VERILOG_MODELS</code>	List[Path]?	Path(s) to cells' black-box Verilog model(s)	
<code>CELL_SPICE_MODELS</code>	List[Path]?	Path(s) to cells' SPICE model(s)	
<code>SYNTH_EXCLUDED_CELL_FILE</code>	Path	Path to a text file containing a list of (wildcards matching) cells to be excluded from the lib file in synthesis alone.	
<code>PNR_EXCLUDED_CELL_FILE</code>	Path	Path to a text file containing a list of undesirable or bad (DRC-failed or complex pinout) cells or wildcards matching cells to be excluded from synthesis AND PnR.	
<code>OUTPUT_CAP_LOAD</code>	Decimal	Defines the capacitive load on the output ports.	fF
<code>MAX_FANOUT_CONSTRAINT</code>	int	The max load that the output ports can drive to be used as a constraint on Synthesis and CTS.	cells
<code>MAX_TRANSITION_CONSTRAINT</code>	Decimal?	The max transition time (slew) from high to low or low to high on cell inputs in ns to be used as a constraint on Synthesis and CTS. If not provided, it is calculated at runtime as <code>10%</code> of the provided clock period, unless that exceeds the PDK's <code>DEFAULT_MAX_TRAN</code> value.	ns

Variable Name	Type	Description	Units
<code>MAX_CAPACITANCE_CONSTRAINT</code>	Decimal?	The maximum capacitance constraint. If not provided, the constraint is not set in the SDC file which will fall back to the value set by the liberty file	pF
<code>CLOCK_UNCERTAINTY_CONSTRAINT</code>	Decimal	Specifies a value for the clock uncertainty/jitter for timing analysis.	ns
<code>CLOCK_TRANSITION_CONSTRAINT</code>	Decimal	Specifies a value for the clock transition/slew for timing analysis.	ns
<code>TIME_DERATING_CONSTRAINT</code>	Decimal	Specifies a derating factor to multiply the path delays with. It specifies the upper and lower ranges of timing.	%
<code>IO_DELAY_CONSTRAINT</code>	Decimal	Specifies the percentage of the clock period used in the input/output delays.	%
<code>SYNTH_DRIVING_CELL</code>	str	The cell to drive the input ports, used in synthesis and static timing analysis, in the format <code>{cell}/{port}</code> .	
<code>SYNTH_CLK_DRIVING_CELL</code>	str?	The cell to drive the clock input ports, used in synthesis and static timing analysis, in the format <code>{cell}/{port}</code> . If not specified, <code>SYNTH_DRIVING_CELL</code> will be used.	
<code>SYNTH_TIEHI_CELL</code>	str	Defines the tie high cell followed by the port that implements the tie high functionality, in the format <code>{cell}/{port}</code> .	
<code>SYNTH_TIELO_CELL</code>	str	Defines the tie high cell followed by the port that implements the tie low functionality, in the format <code>{cell}/{port}</code> .	
<code>SYNTH_BUFFER_CELL</code>	str	Defines a buffer port to be used by yosys during synthesis: in the format <code>{cell}/{input_port}/{output_port}</code>	
<code>WELLTAP_CELL</code>	str	Defines the cell used for tap insertion.	
<code>ENDCAP_CELL</code>	str	Defines so-called 'end-cap' cells- decap cells placed at either sides of a design.	
<code>PLACE_SITE</code>	str	Defines the primary placement site in placement as specified in the technology LEF files, to generate the placement grid.	

Variable Name	Type	Description	Units
<code>CELL_PAD_EXCLUDE</code>	List[str]	Defines a list of cells to be excluded from cell padding.	
<code>DIODE_CELL</code>	str?	Defines a diode cell used to fix antenna violations, in the format {name}/{port}.	



Copyright © 2020-2023 Efabless Corporation and contributors

Made with [Sphinx](#) and @pradyunsg's [Furo](#)