
0.5um Analog CMOS 2P3M 5V Design Tutorial

Version 1.3

National Semiconductor Public Laboratory (NSPL)

- Electronics and Telecommunications Research Institute (ETRI)
- Seoul National University (SNU)
- Daegu Gyeongbuk Institute of Science & Technology (DGIST)



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1. Overview

1. Overview

1.1 Overview

The purpose of this paper is 0.5um Analog CMOS 2P3M 5V Design tutorial.

1.2 Tools and Software Version

- Virtuoso 6.1.7 version
- Calibre 2019.4_36.18

1.3 File Configuration

File : ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_V1p0.tar.gz

- ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_V1p0	
- ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_V1p0.tf	: tech file
- display.drf	: display file
- DRC	
- ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_V1.0_DRC.cal	: DRC rule file
- drc_header.cal	: with script file
- LVL	
- ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_V1.0_LVL.cal	: LVL rule file
- lvl_header.cal	: with script file
- LVS	
- ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_V1.0_LVS.cal	: LVS rule file
- lvs_header.cal	: with script file
- PEX	
- ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_V1.0_PEX.cal	: PEX rule file
- pex_header.cal	: with script file
- ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_V1p0_pcell	: Pcell library
- ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_V1p0_sch	: sch library
- ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_V1p0_std_lay	: std lay library
- ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_V1p0_std_sch	: std sch library

1.4 Documents

- 0.5um Analog CMOS 2P3M 5V Design Rule V1.0	: Design rule
- 0.5um Analog CMOS 2P3M 5V Design Guide V1.0	: Design Guide
- 0.5um Analog CMOS 2P3M 5V Design Guide V1.0	: Design Tutorial

1.5 Document history

Rev	Date	From	Description
1.0	2023.09.15	ETRI	Added Items 1. Overview 2. PDK Library 설정 3. 회로 설계 및 검증(Pre-simulation) 4. Layout 5. DRC 6. LVS 7. PEX
1.1	2023.10.10	ETRI	8. 회로 설계 및 검증(Post-simulation)
1.2	2023.10.24	ETRI	7. PEX – Calibreview 방식 8. 회로 설계 및 검증(Post-simulation) – Calibre 방식
1.3	2023.12.29	ETRI	5.2 Assura DRC 검토 6.2 Assura LVS 검토

		Title
		ETRI 0.5µm Analog CMOS 2P3M 5V Design Tutorial
		Division
		ETRI

2. PKD Library 설정

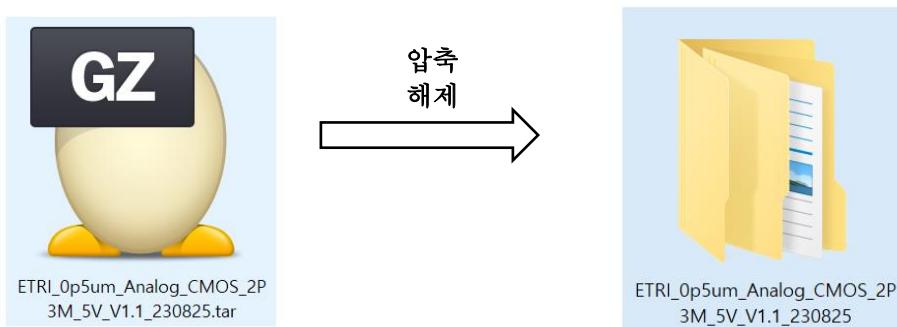
2. PDK Library 설정

- 목적 : 회로 설계 및 검증에 앞서 제공받은 PDK를 설정

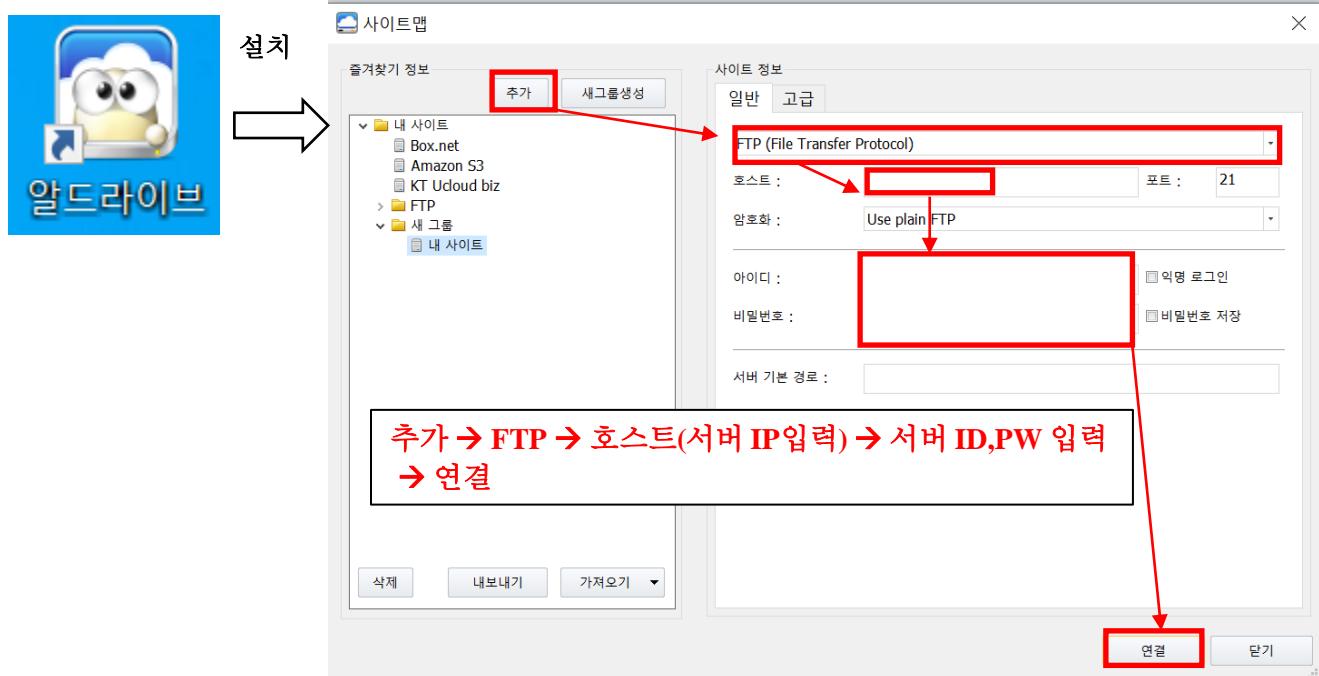
1) PDK Library 전송 (서버 기반의 워크스테이션 접속일 경우)

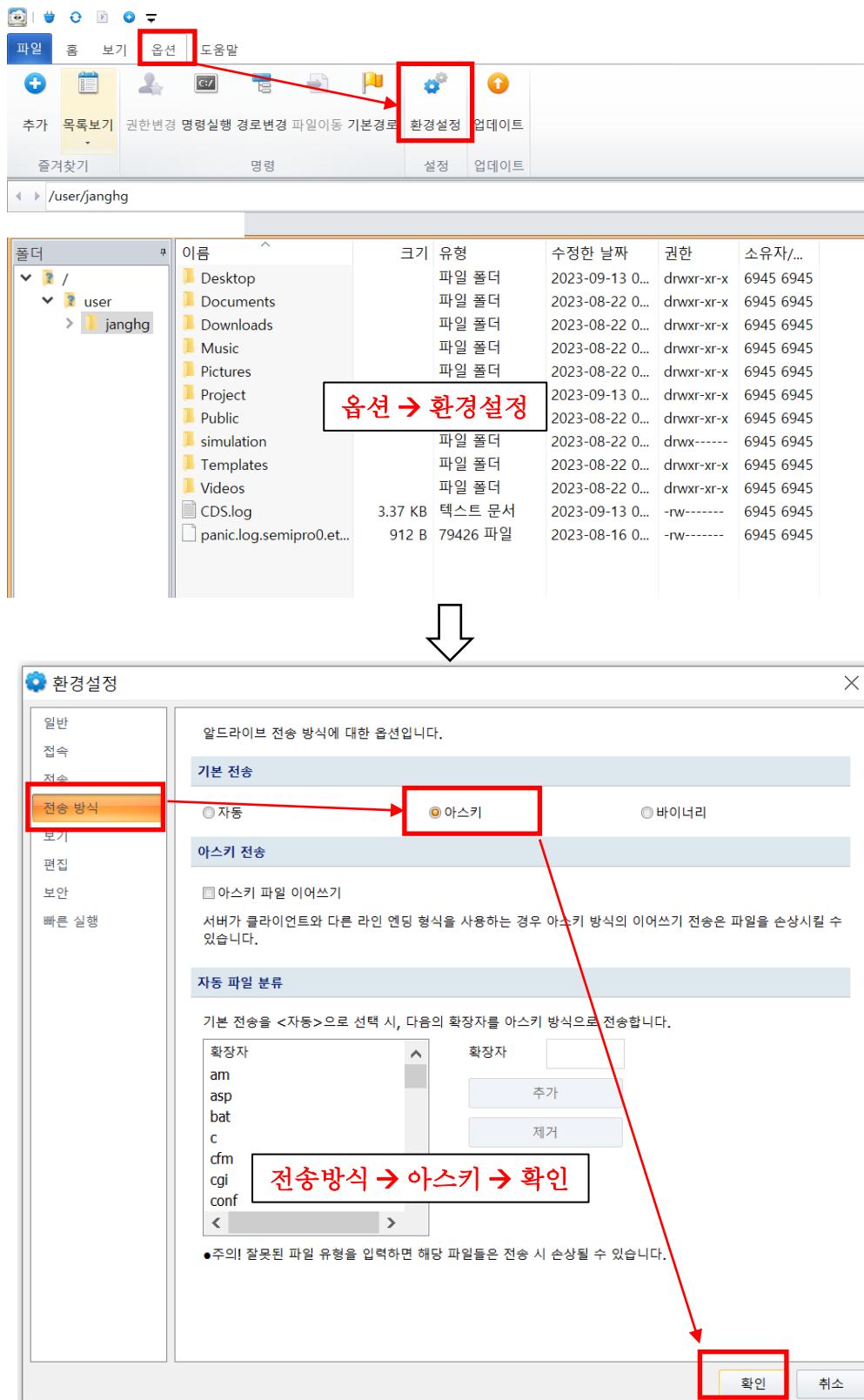
- 제공된 PDK를 FTP(File Transfer Protocol)을 이용하여 워크스테이션에 전송

① 제공된 PDK 파일 압축 해제

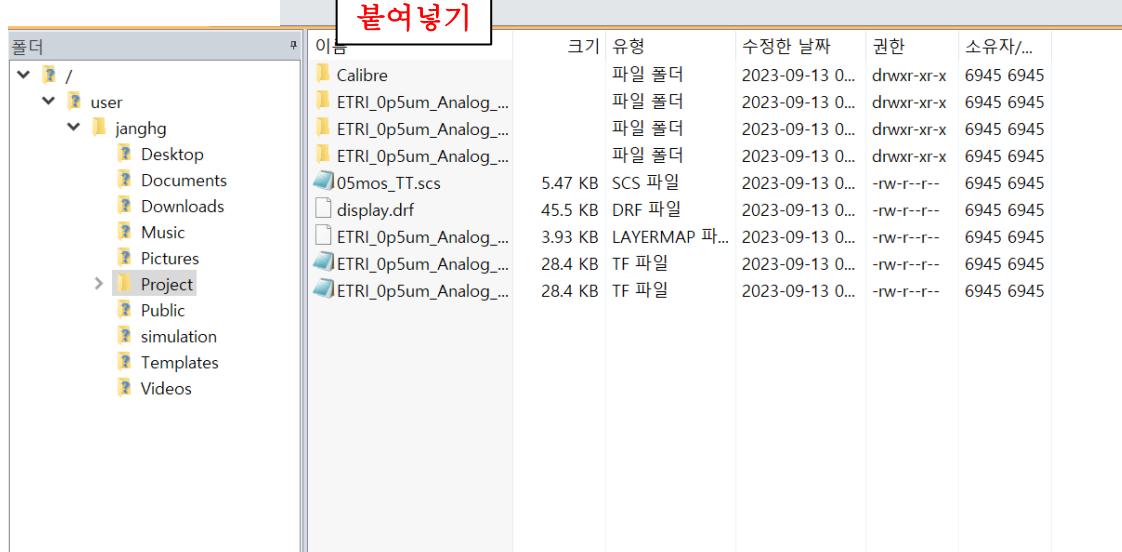
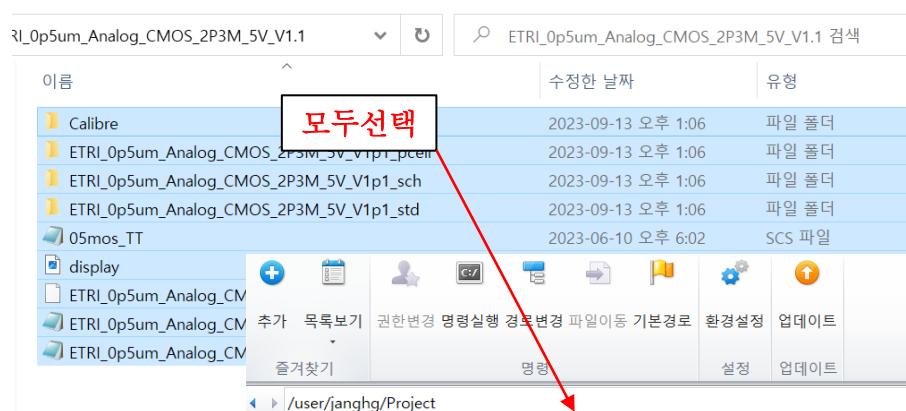
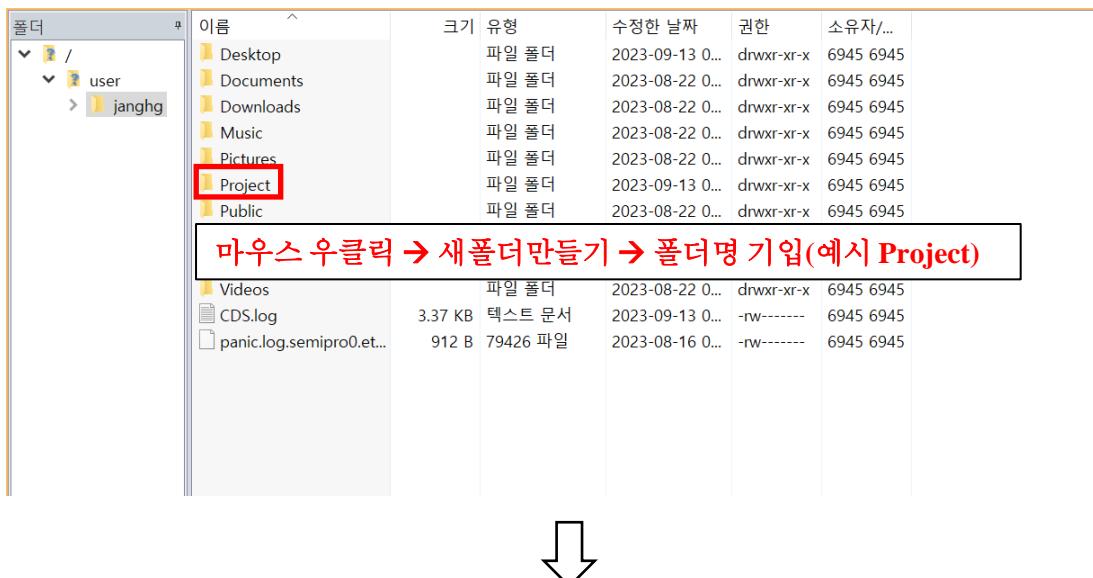


② FTP 프로그램 설치 및 설정 (예시로 알드라이브 사용)

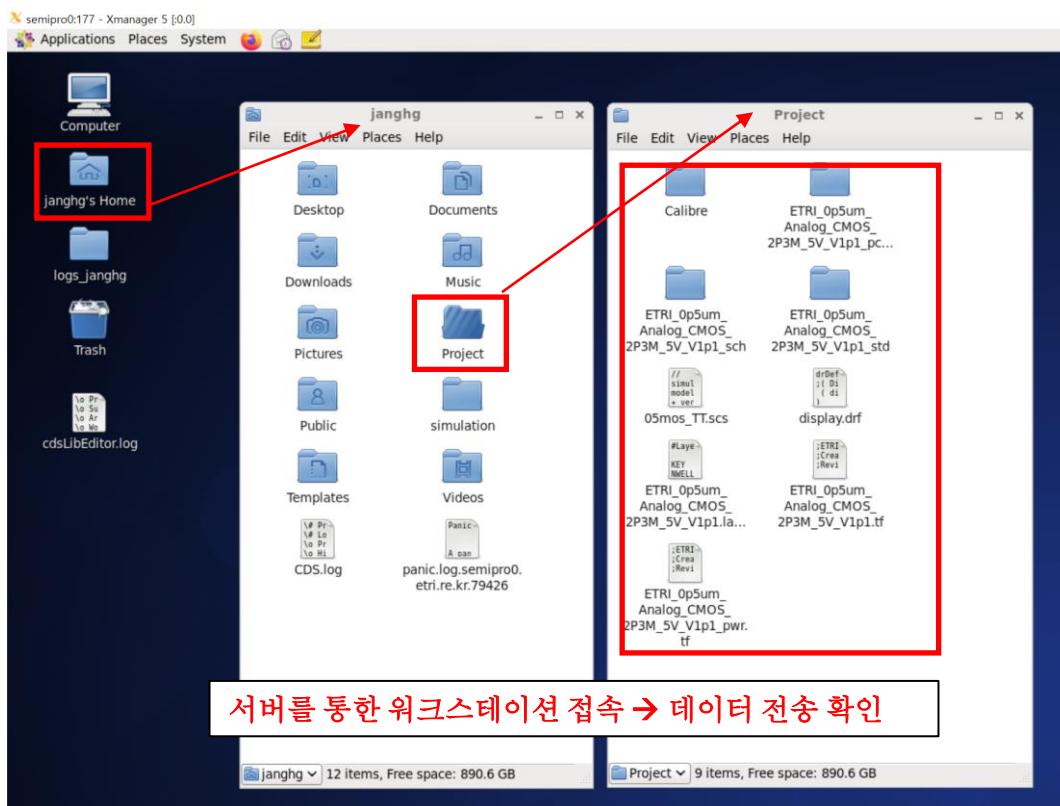




③ 폴더 설정 및 파일 전송

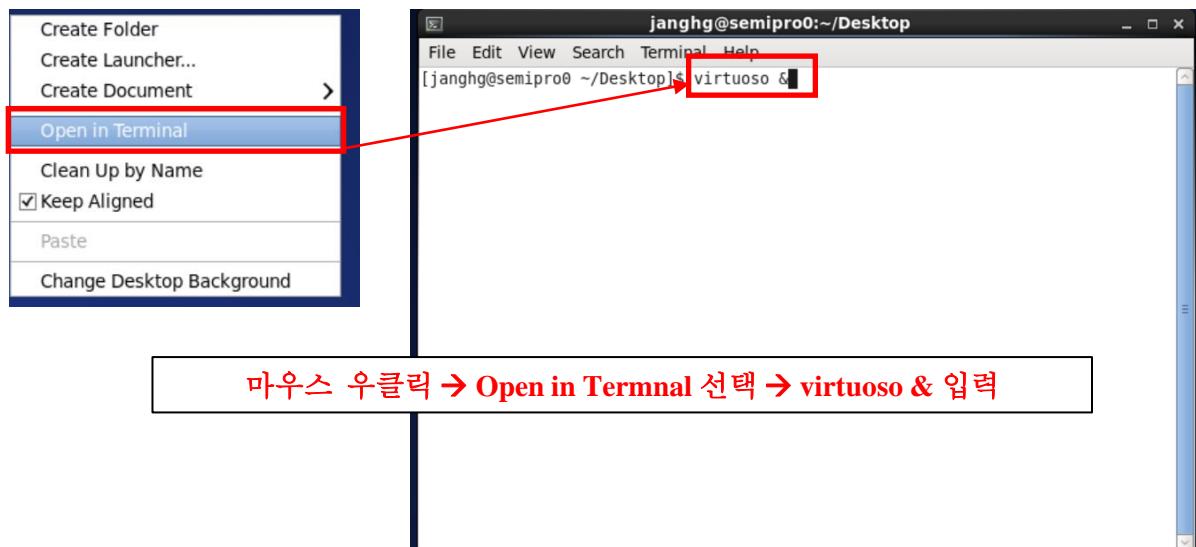


④ 전송된 파일 확인

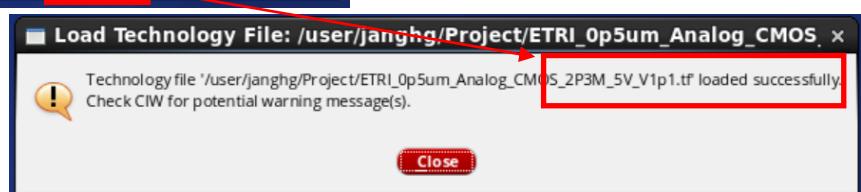
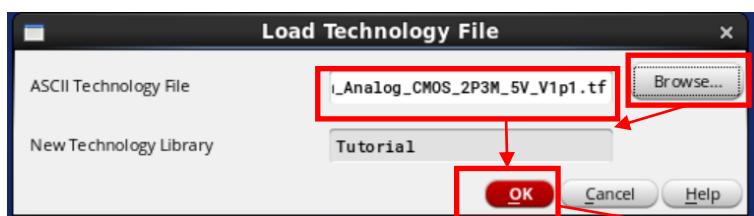
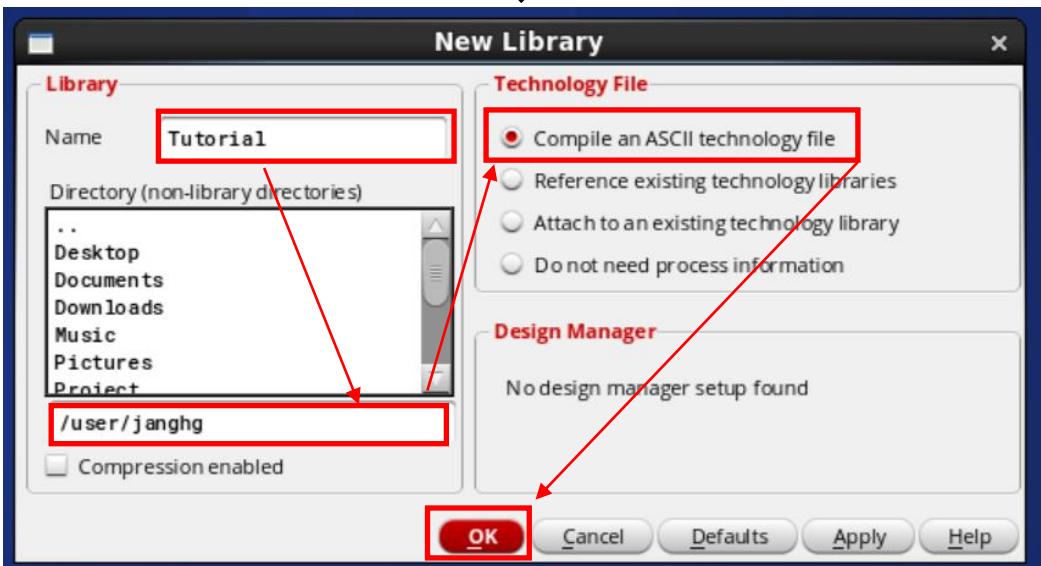
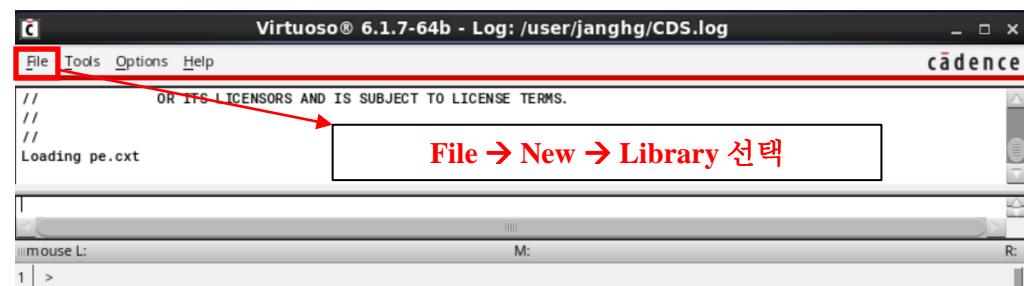


2) Library 생성 및 추가

① Cadence 실행

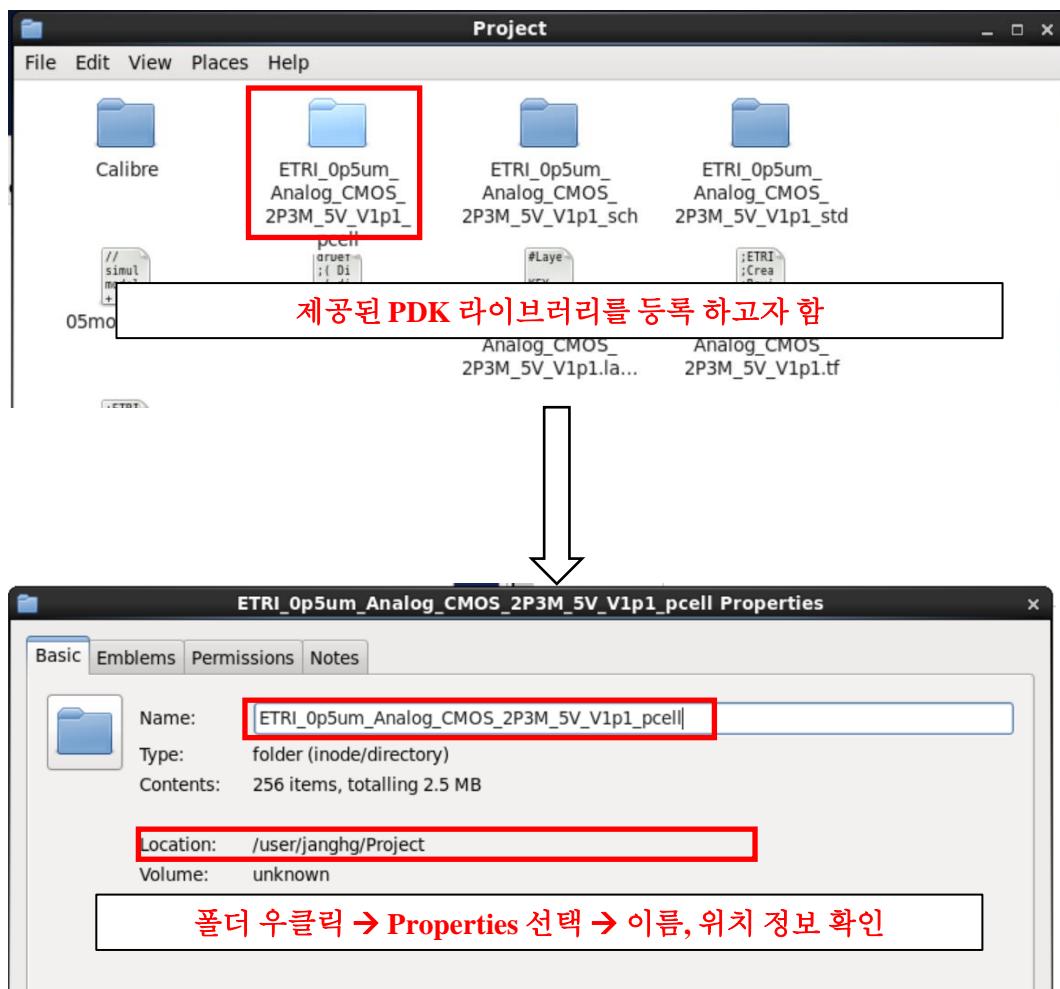


② 라이브러리 생성



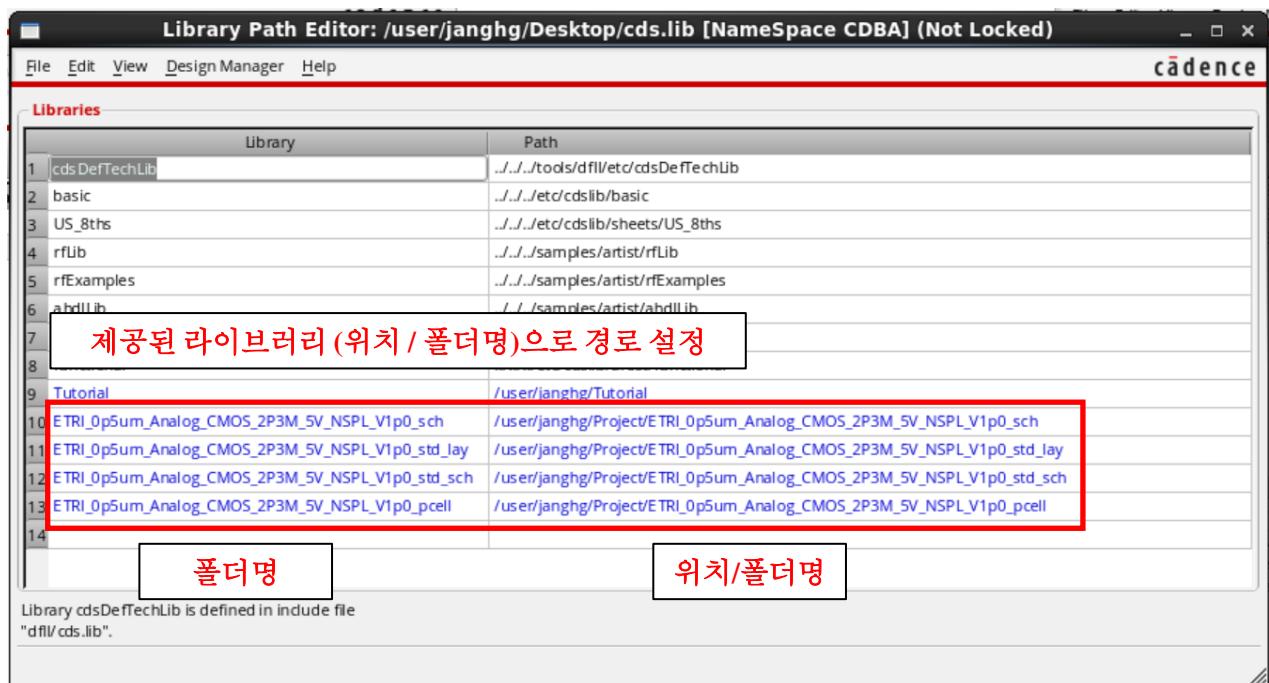
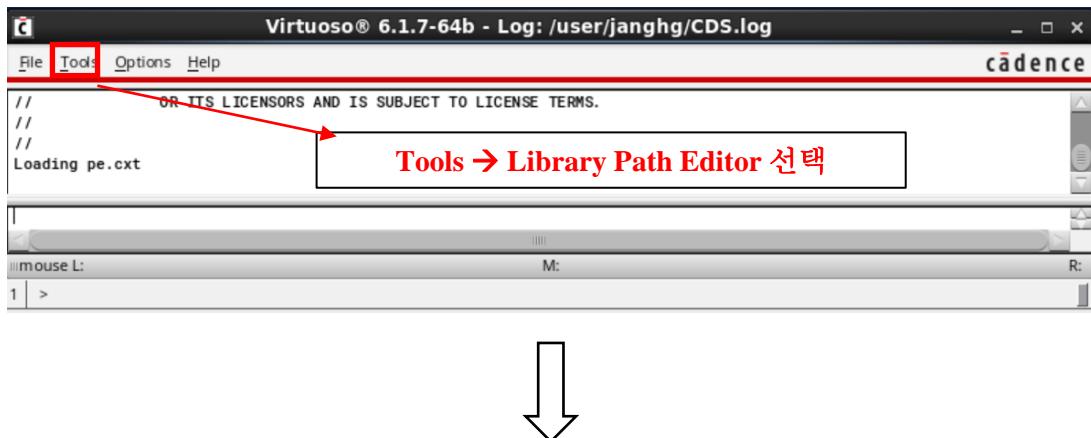
Browse 선택 → Project 폴더에 있는 xxx.tf 파일 선택 → OK
→ 문제없을 시 성공 메시지 확인 가능

③ 제공된 PDK 라이브러리 추가



- 이름 : ETRI_0p5um_Analog_CMOS_2p3M_5V_V1p1_pcell
- 위치 : /user/jang/Project

→ 라이브러리 추가에 따른 경로 설정에 필요함
→ 라이브러리 경로 설정시 위치/이름 삽입 필요! (뒷장 계속)



- 만일, 라이브러리 추가 오류 발생시 빨간색 글씨로 바뀜
→ 파란색일 경우 정상적인 등록

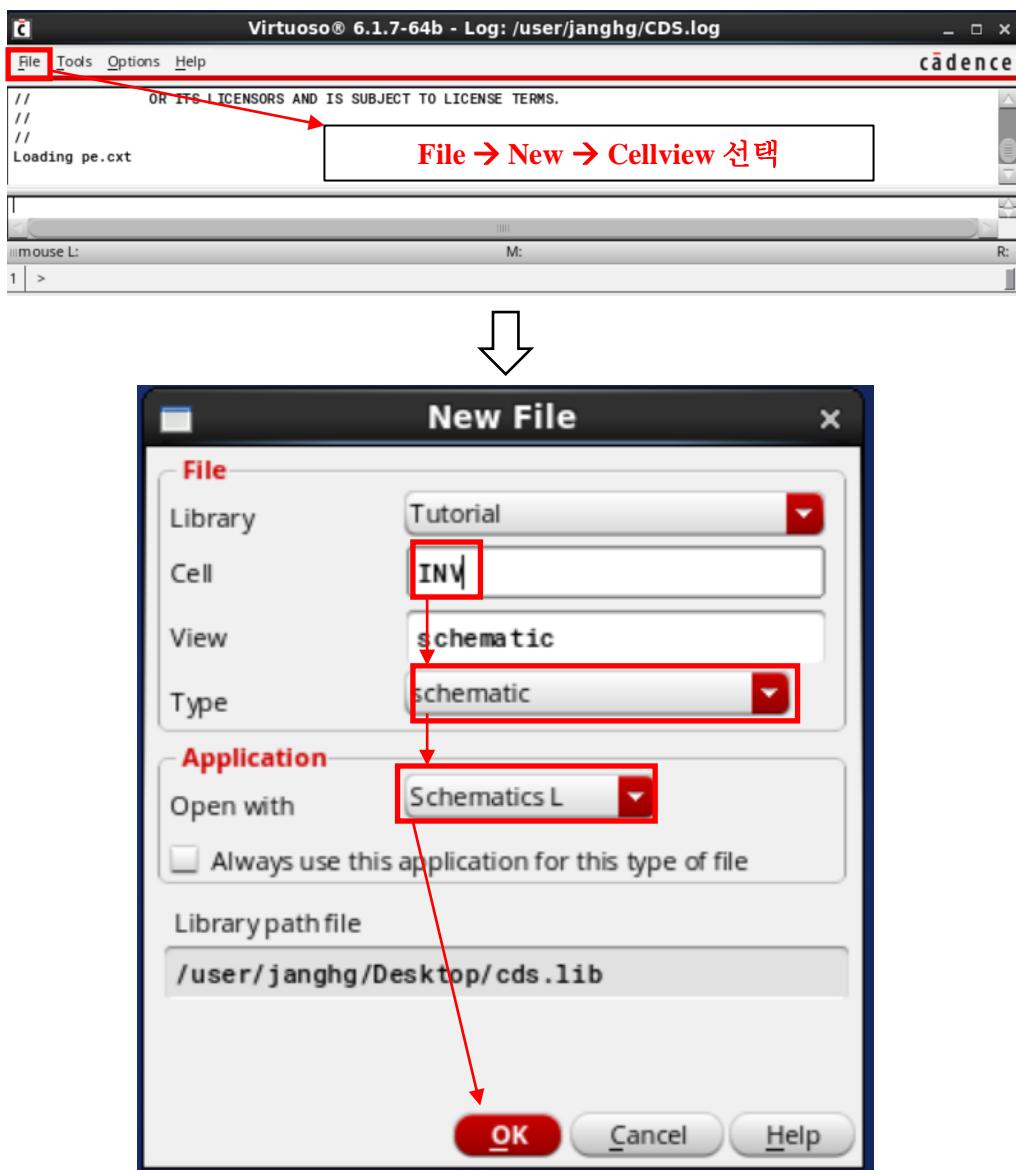
3. 회로 설계 및 검증 (Pre-simulation)

3. 회로 설계 및 검증(Pre-simulation)

- 목적 : 회로 설계 및 시뮬레이션을 통한 회로 검증
- 예: 인버터 회로 설계 및 검증

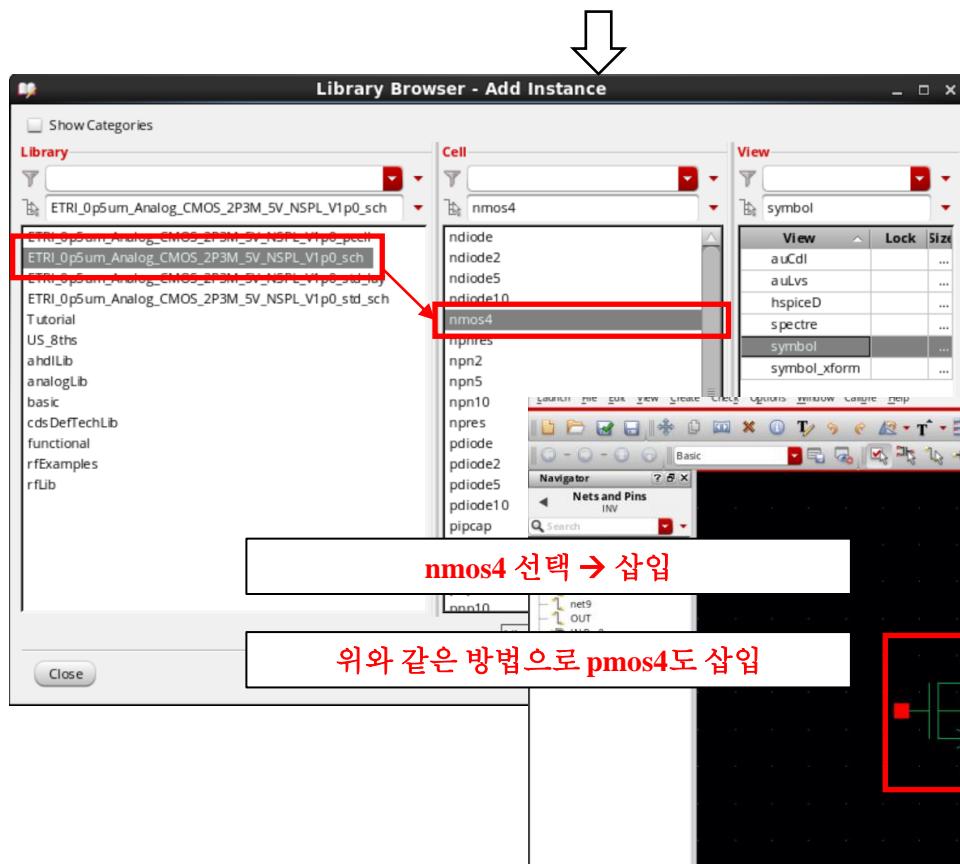
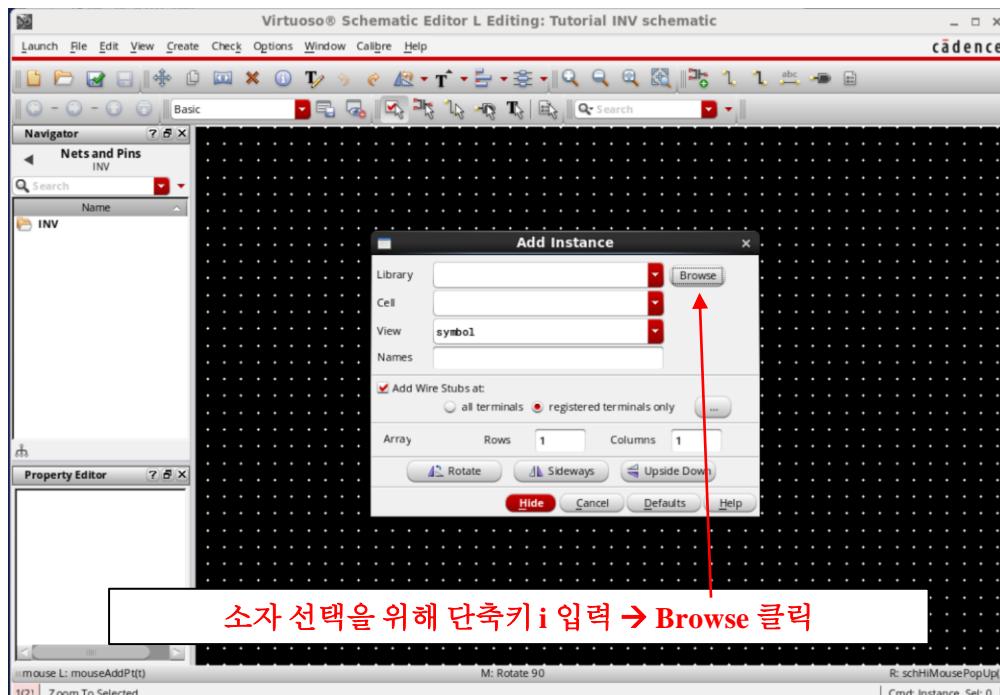
1) 인버터 설계

① Schematic 설계 프로그램 실행

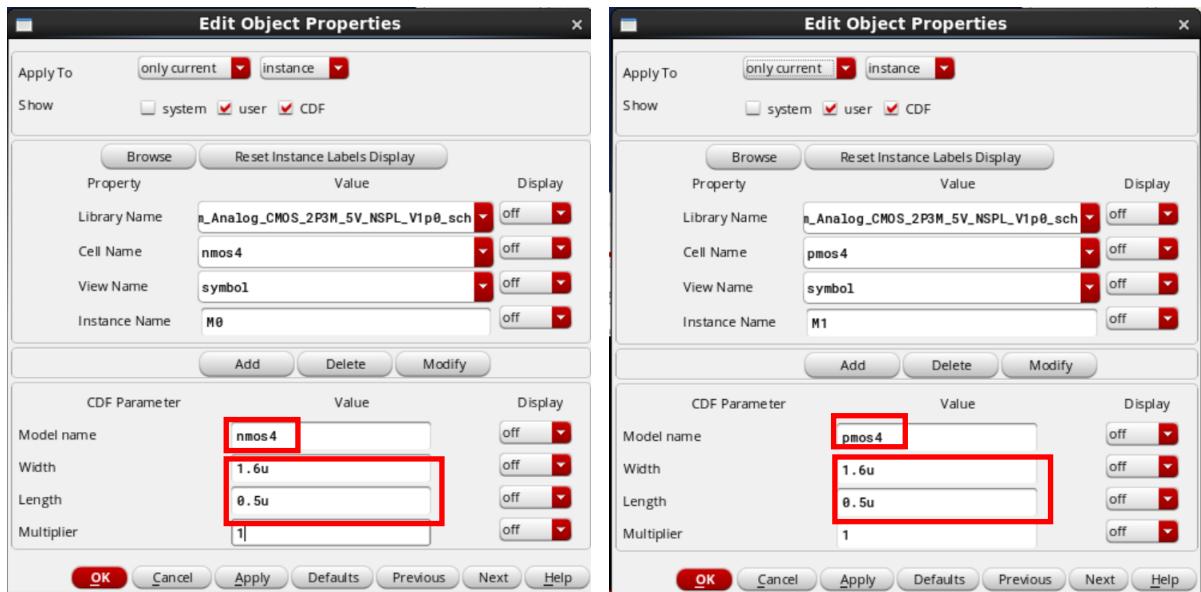


Cell 명 → Type 설정 → 실행 가능한 시뮬레이터 선정 → OK 클릭

② 소자 설정

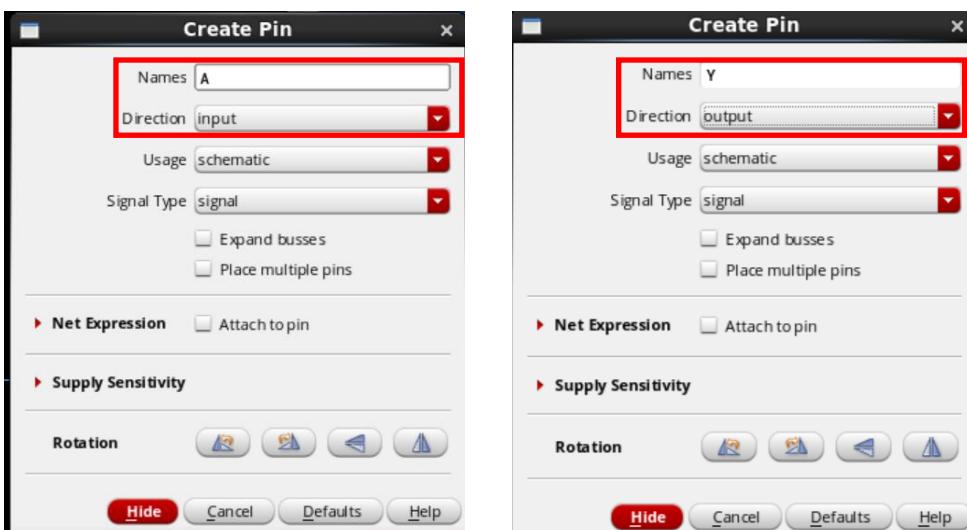


소자별 parameter 입력을 위해 소자 클릭 후 단축키 Q



- Model name은 시뮬레이션을 위해 모델파라미터 이름 입력 (pmos4, nmos4)
- Width, Length 값 기입

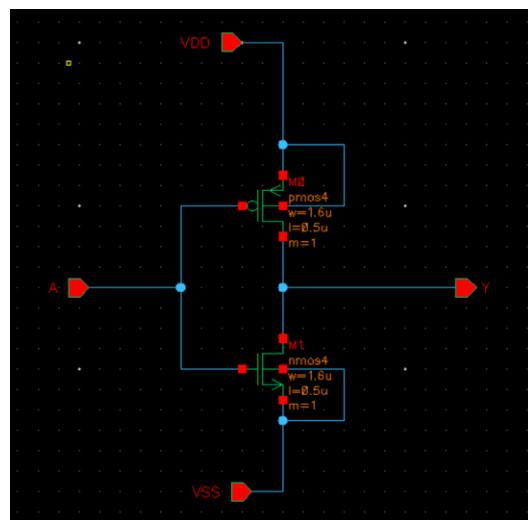
③ Pin 설정



포트 설정(단축키 P), 편명과 방향(Input, Output) 설정

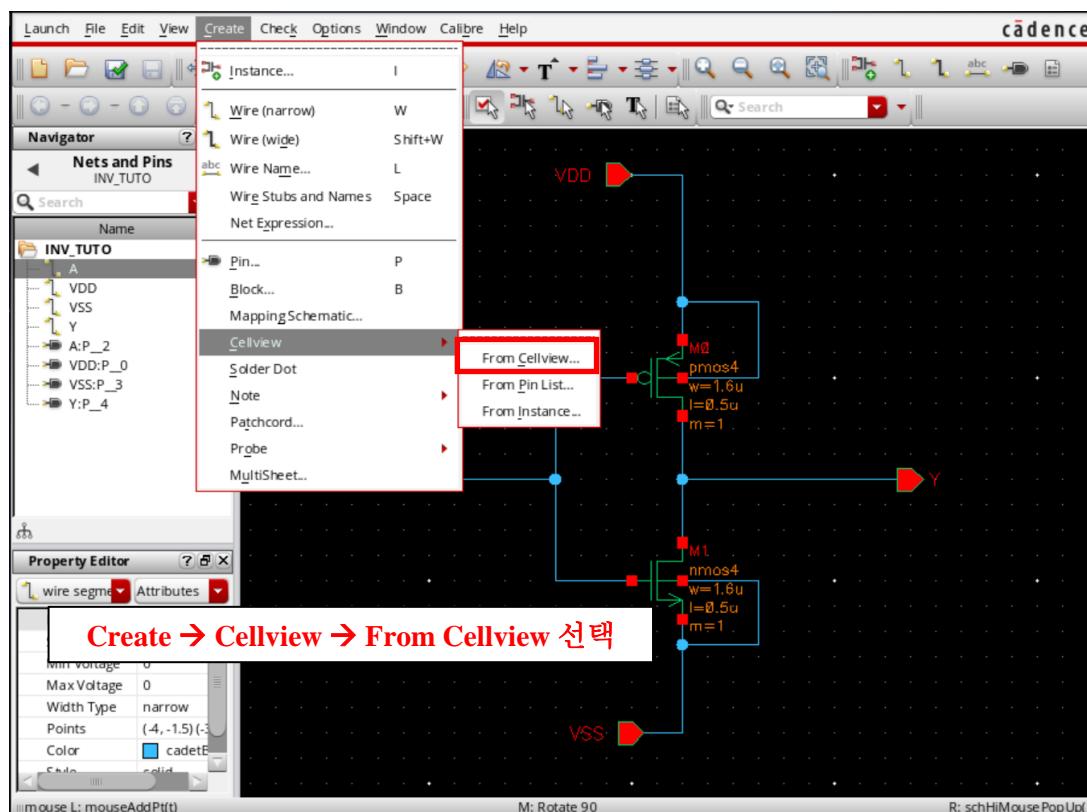
A, Y, VDD, VSS 포트 삽입

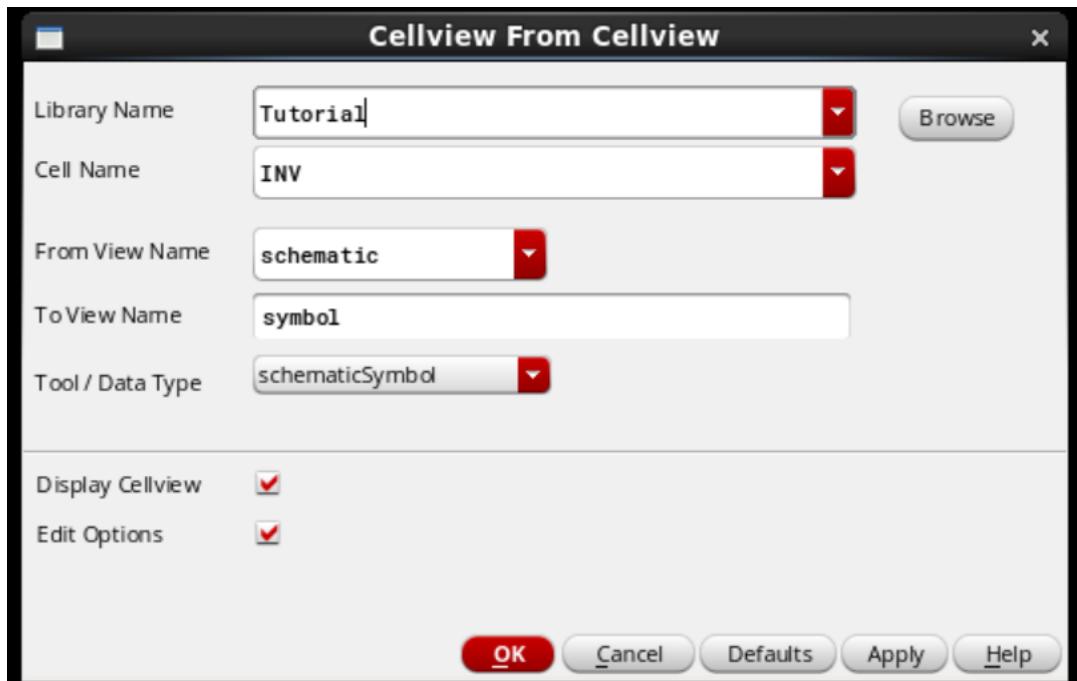
④ 와이어 연결



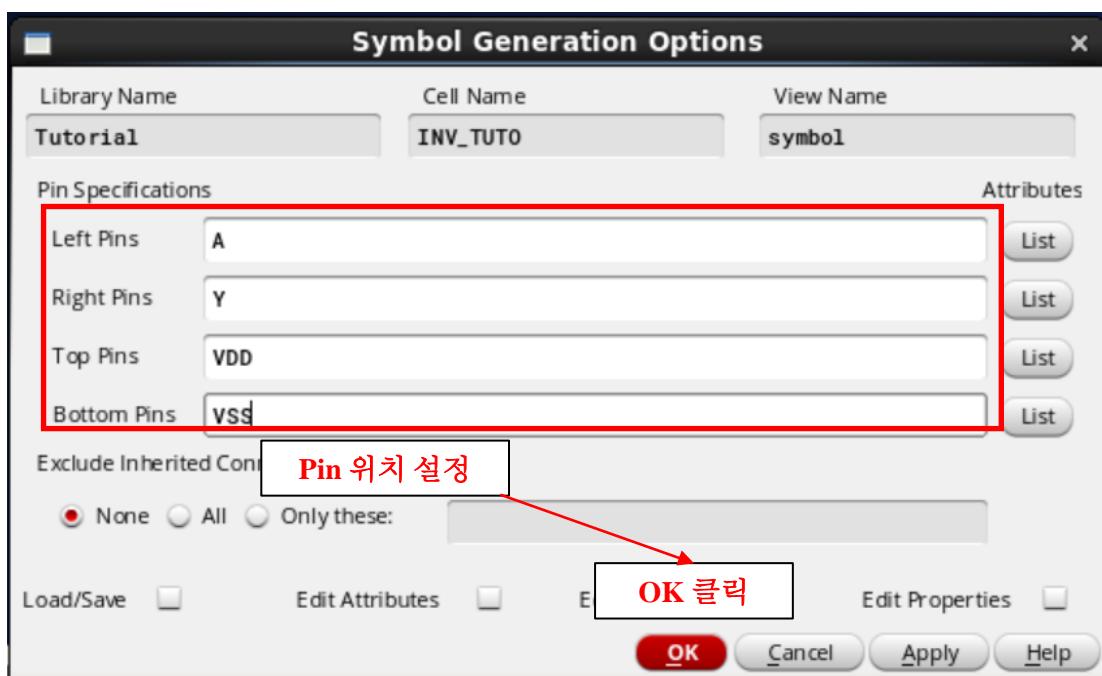
와이어 연결(단축키 w)

⑤ 심볼형성

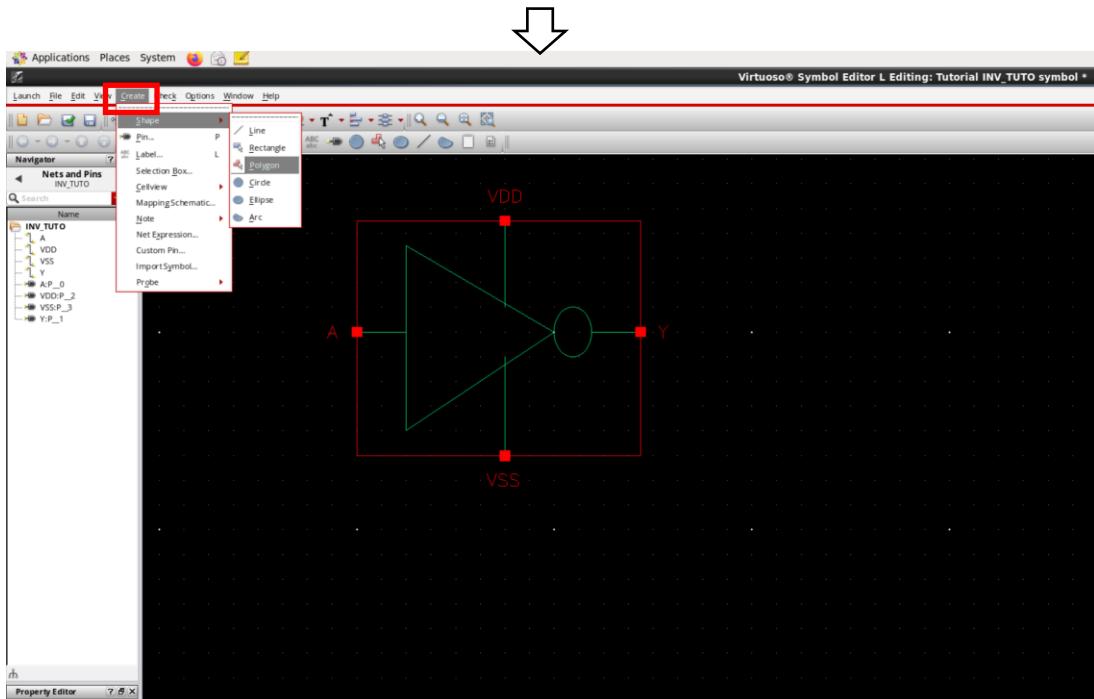
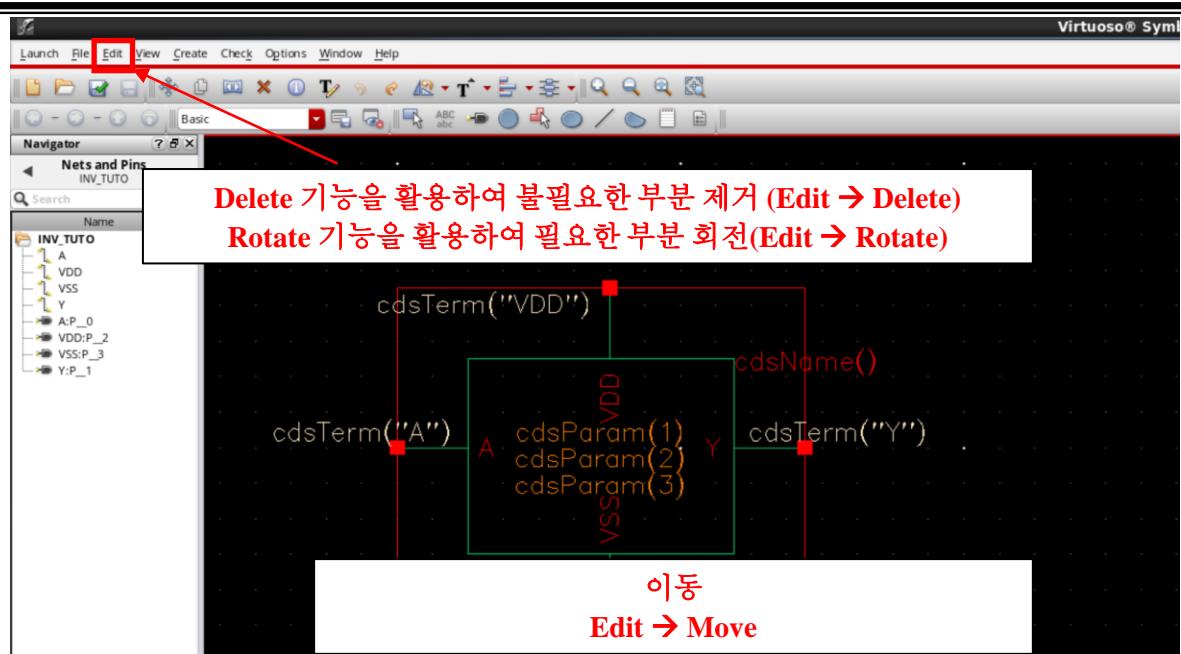




OK 선택

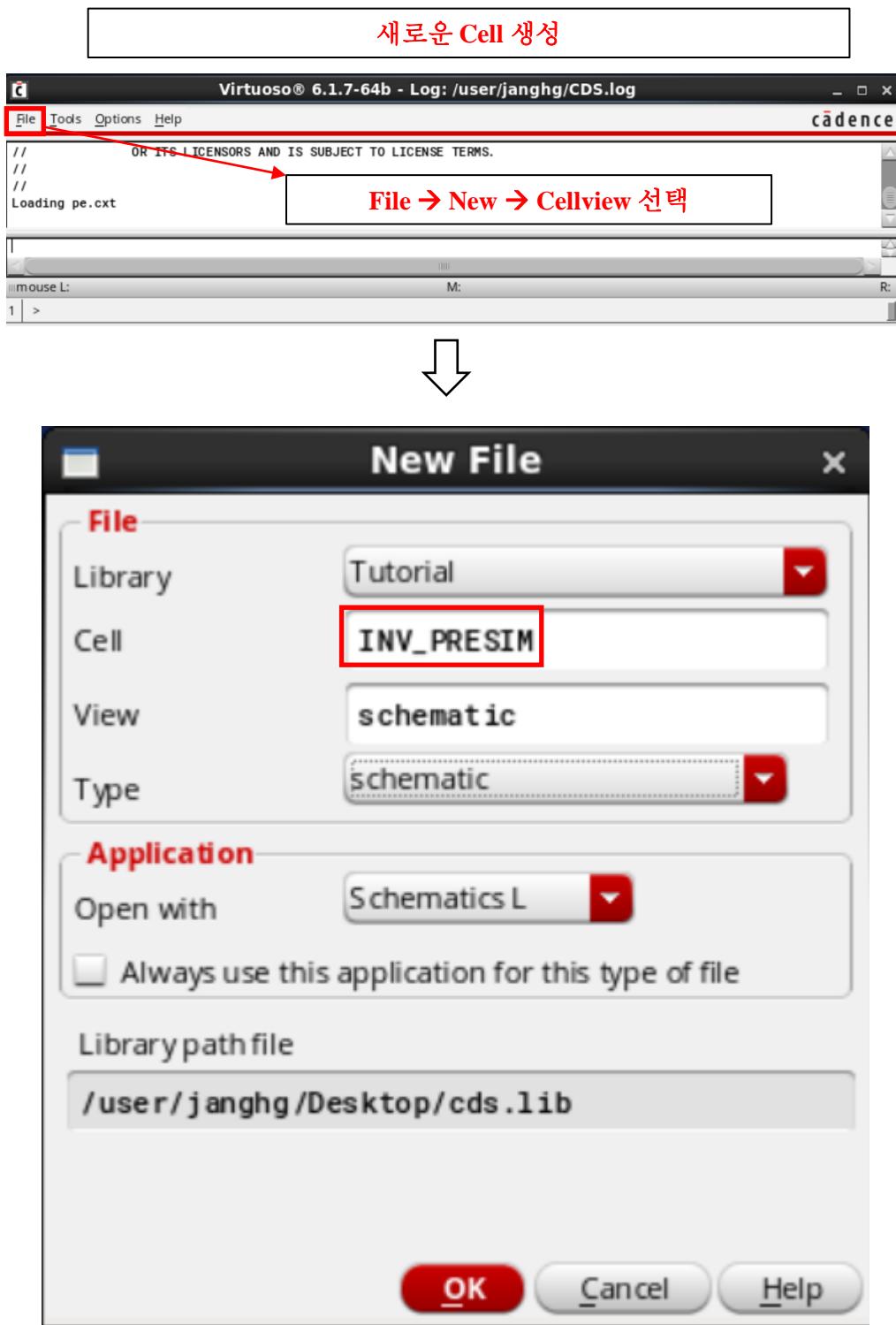


OK 클릭

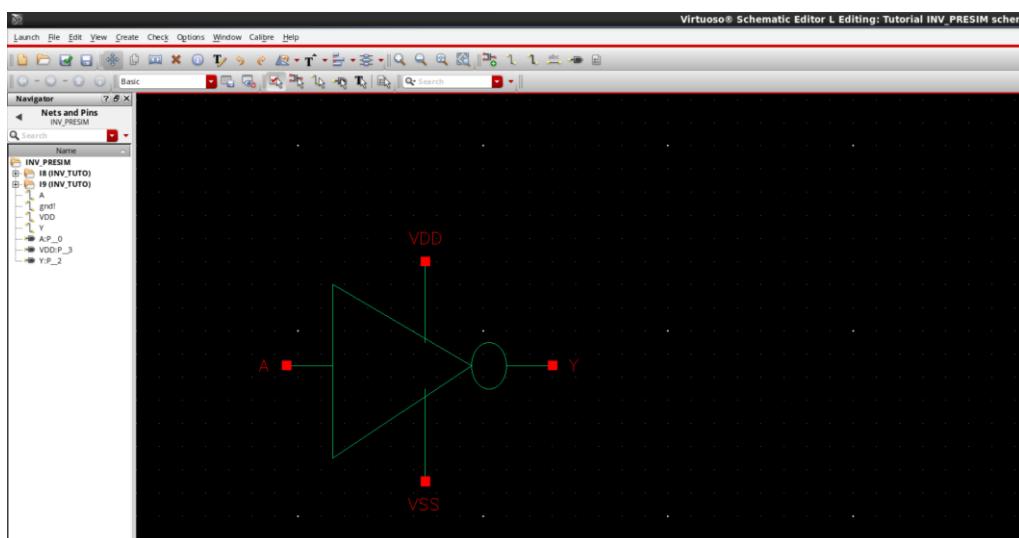
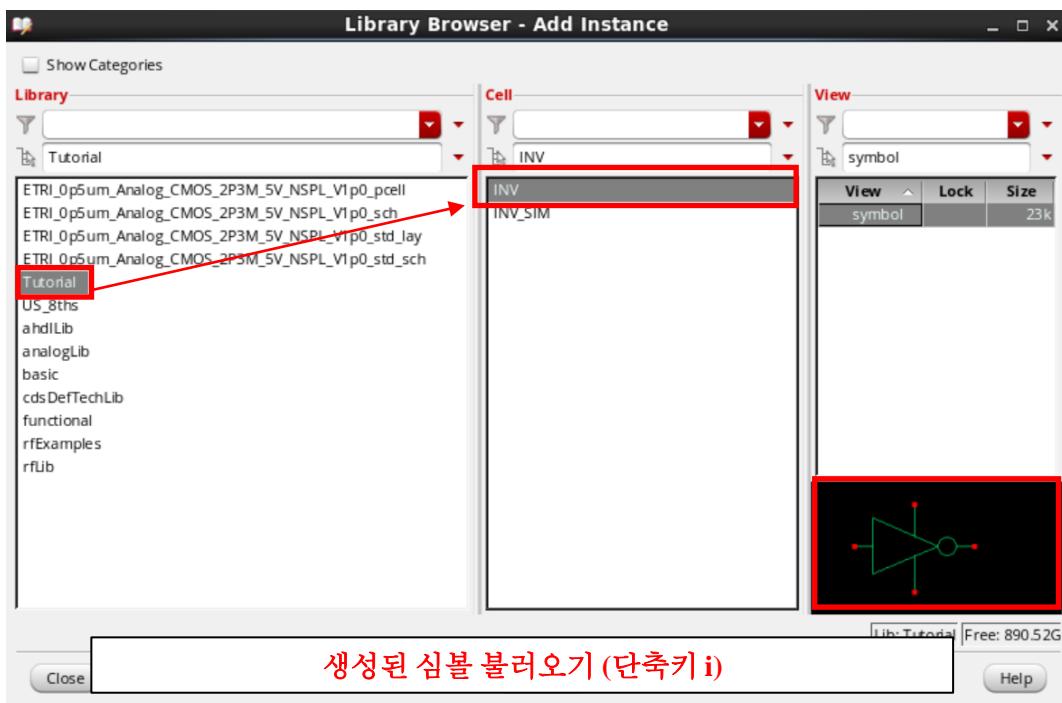


2) 시뮬레이션을 위한 회로 설계

① Schematic 설계 프로그램 실행

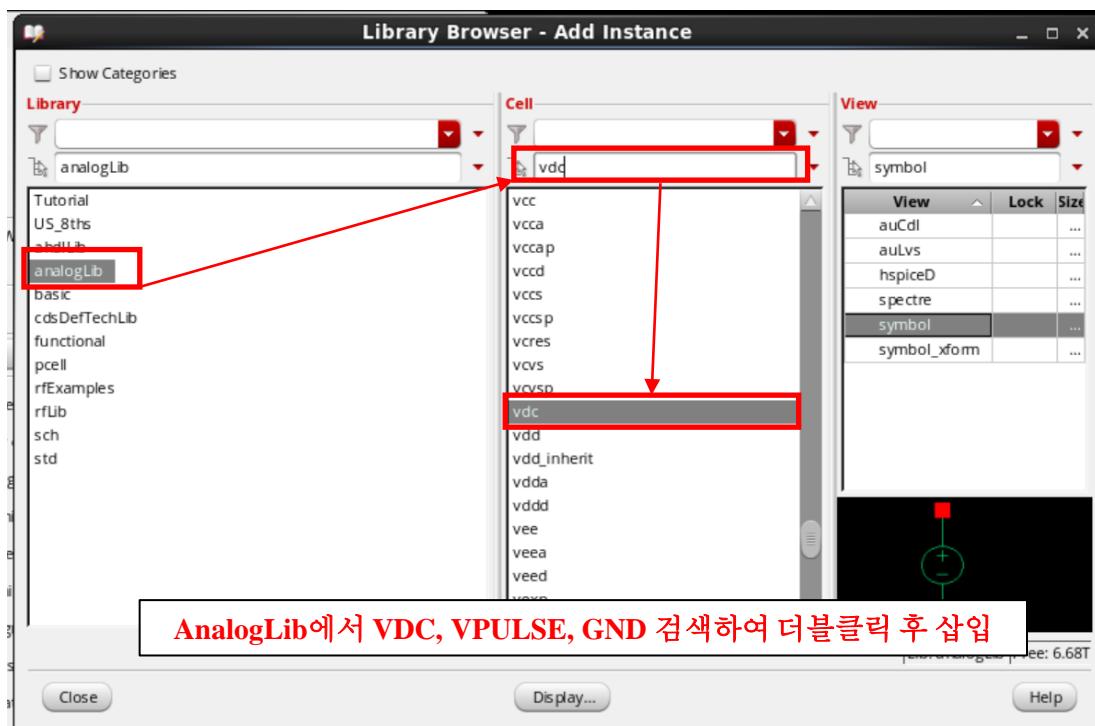


② 인버터 심볼 불러오기

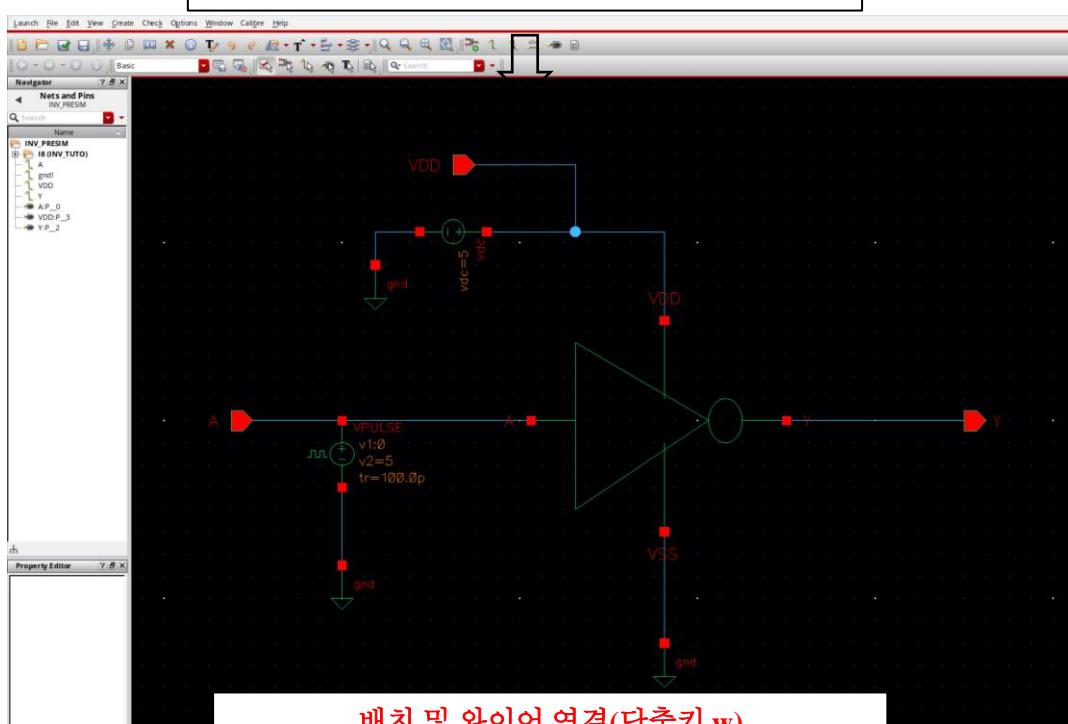


심볼 배치

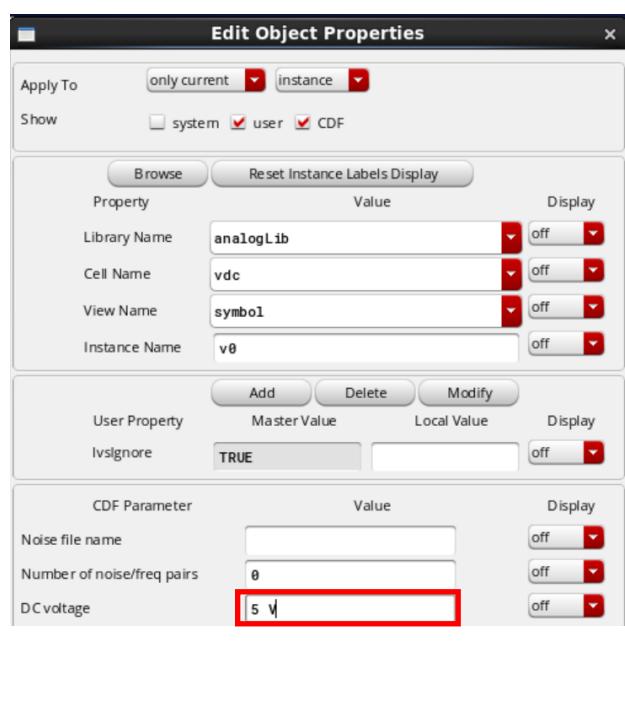
③ 소자 배치 및 와이어 연결



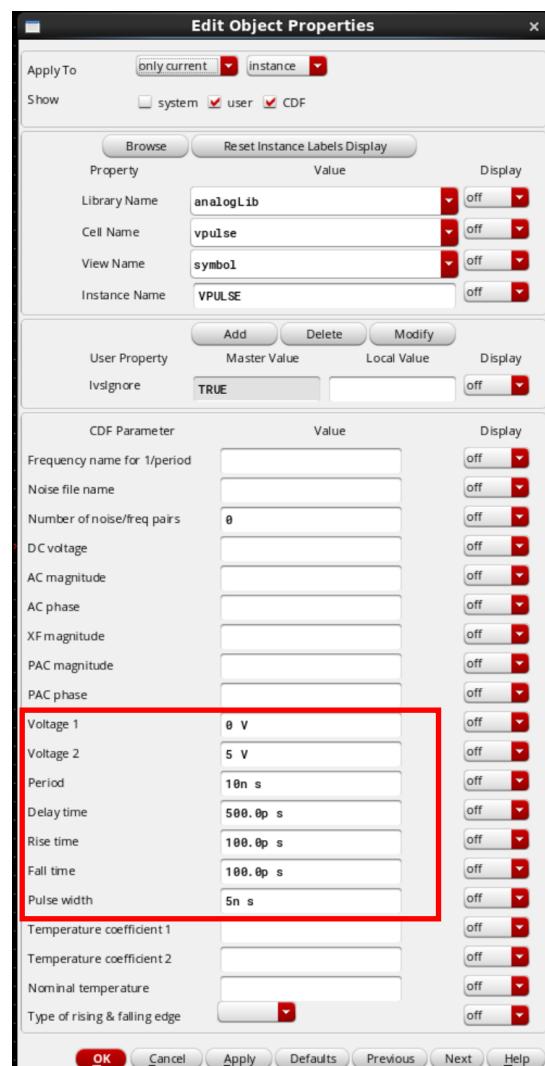
IN, OUT 포트 생성 (단축키 P)



④ 인가값 설정



시뮬레이션을 위해 VDC 및 VPULSE 핵 입력



⑤ 저장 및 검증



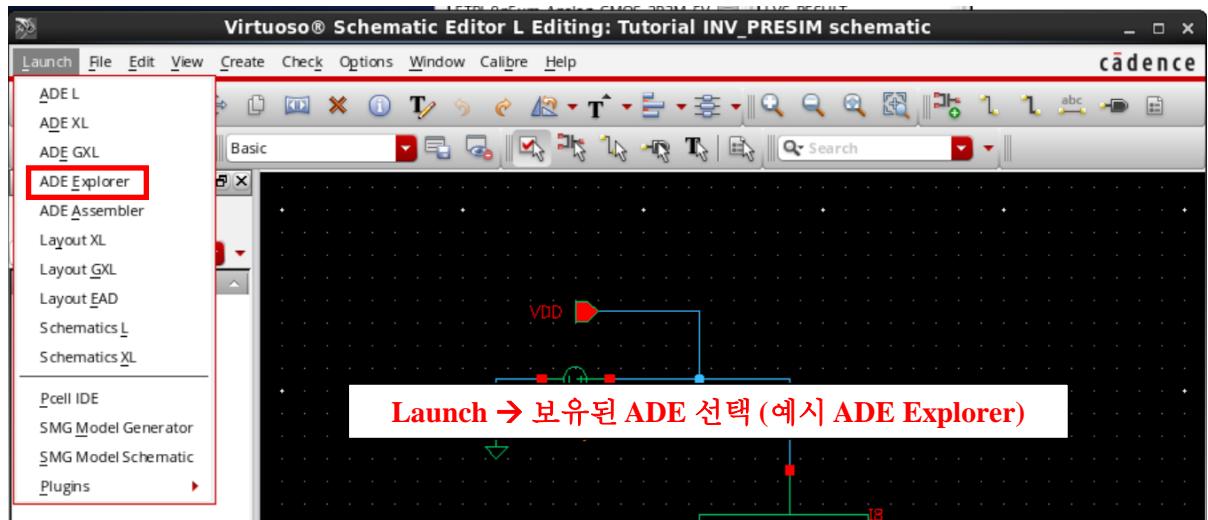
Check & save 버튼 클릭



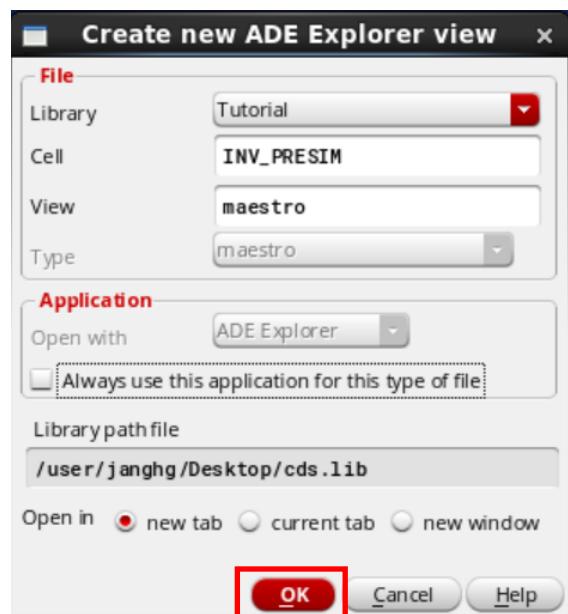
에러 및 경고 메시지 확인, 에러 0까지 수정 및 검증

3) 인버터 시뮬레이션

① Schematic 시뮬레이션 프로그램 실행

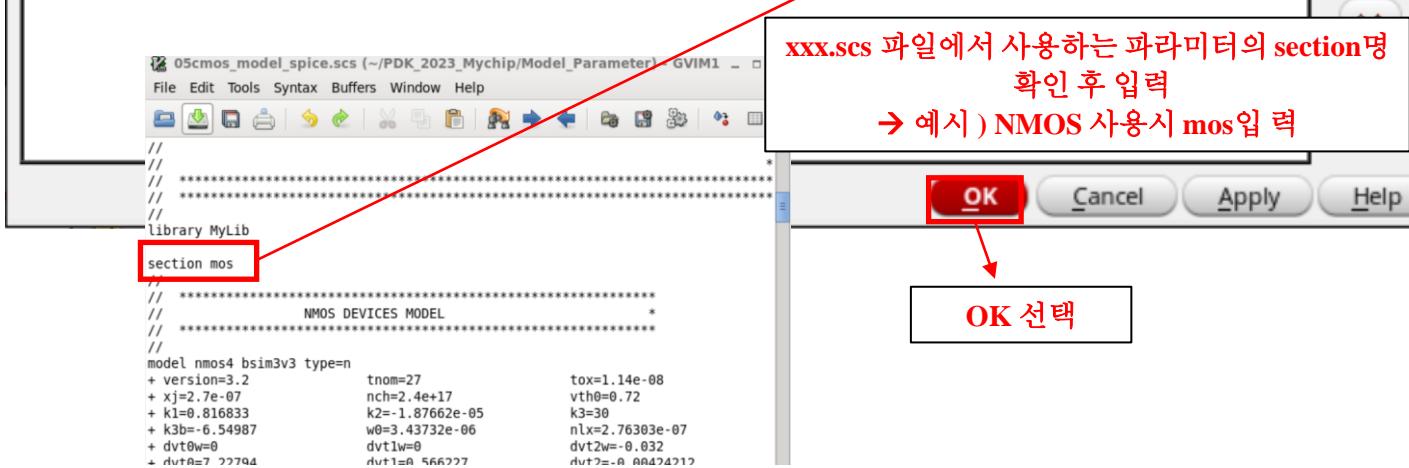
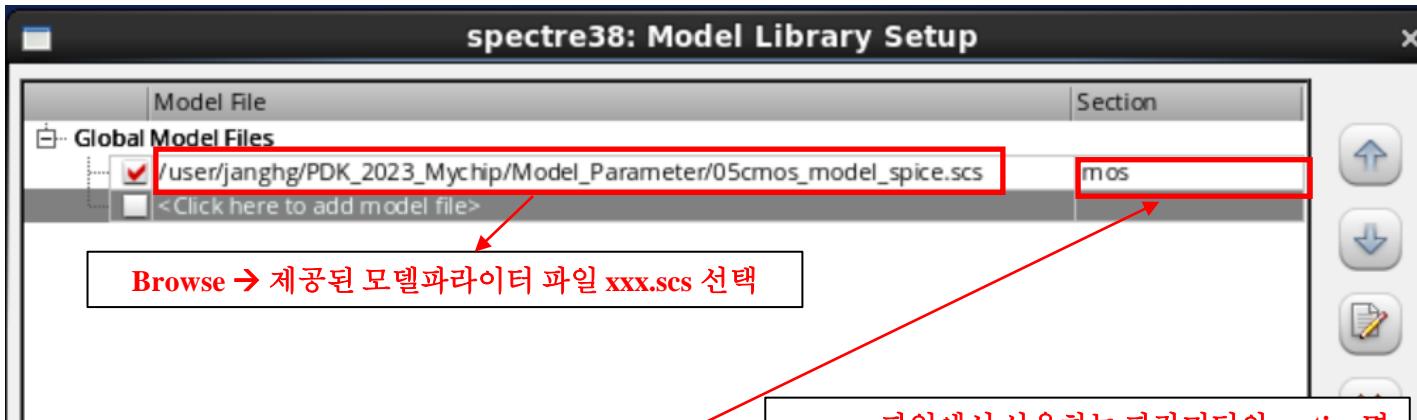
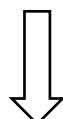
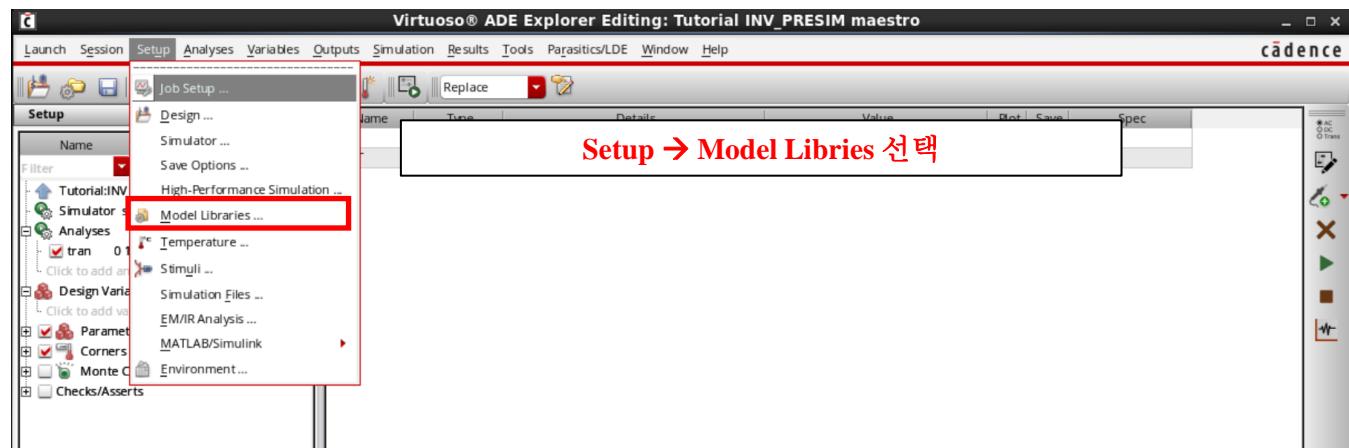


Create New View 선택
(시뮬레이션 완료 저장 후에는 Open Existing View 선택)



오픈 방식 설정 후 OK 클릭

② 회로 검증 시뮬레이션 환경 설정



xxx.scs 파일에서 사용하는 파라미터의 section명
확인 후 입력

→ 예시) NMOS 사용시 mos 입력

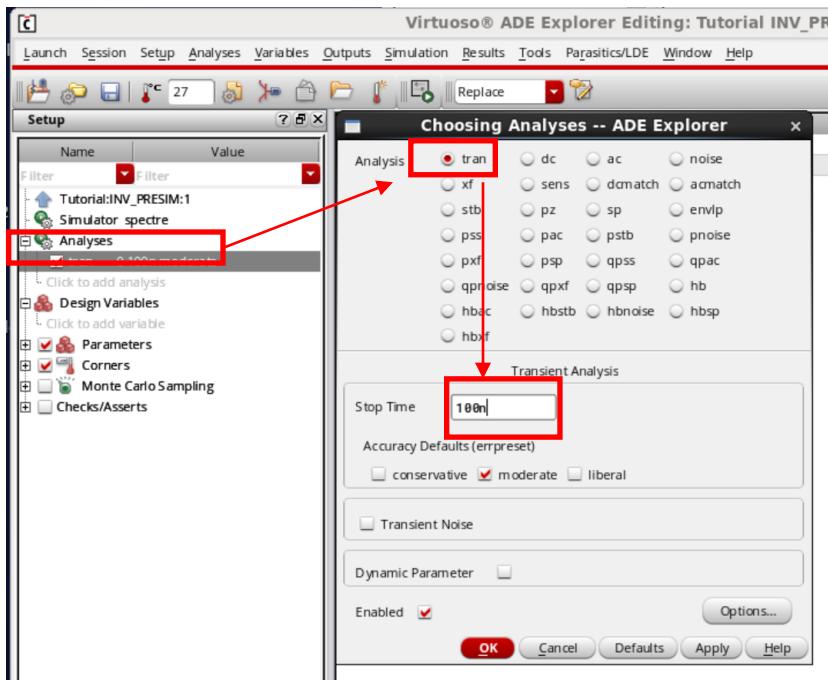
OK

Cancel

Apply

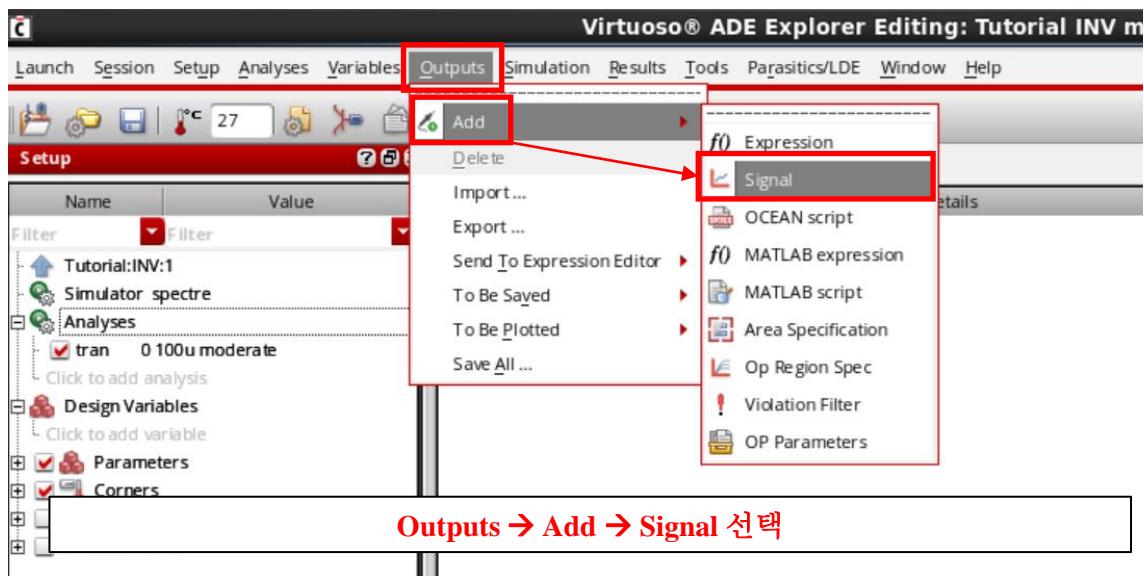
Help

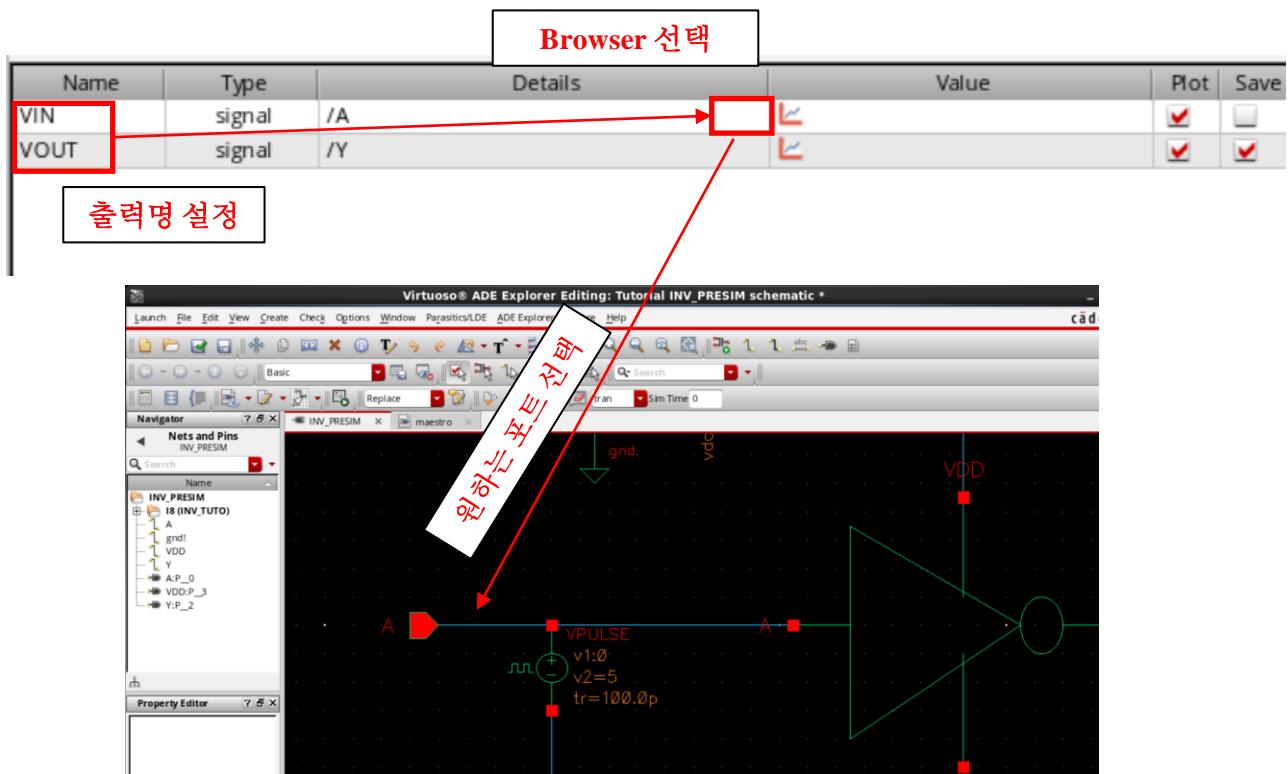
OK 선택



시뮬레이션 설정 : 분석 항목 선택 및 조건 기입 (예시에서는 Tran. 100ns로 기입)

③ 시뮬레이션 포트 설정

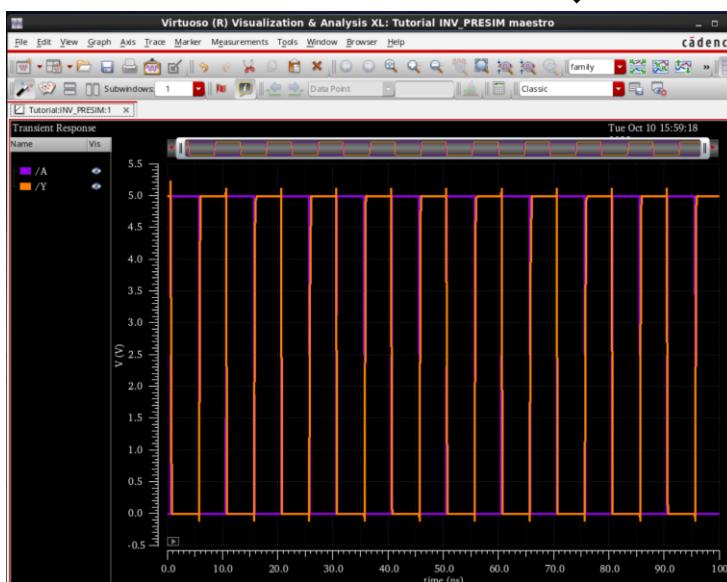
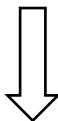




④ 시뮬레이션 실행



저장 및 시뮬레이션 실행



시뮬레이션 결과 출력

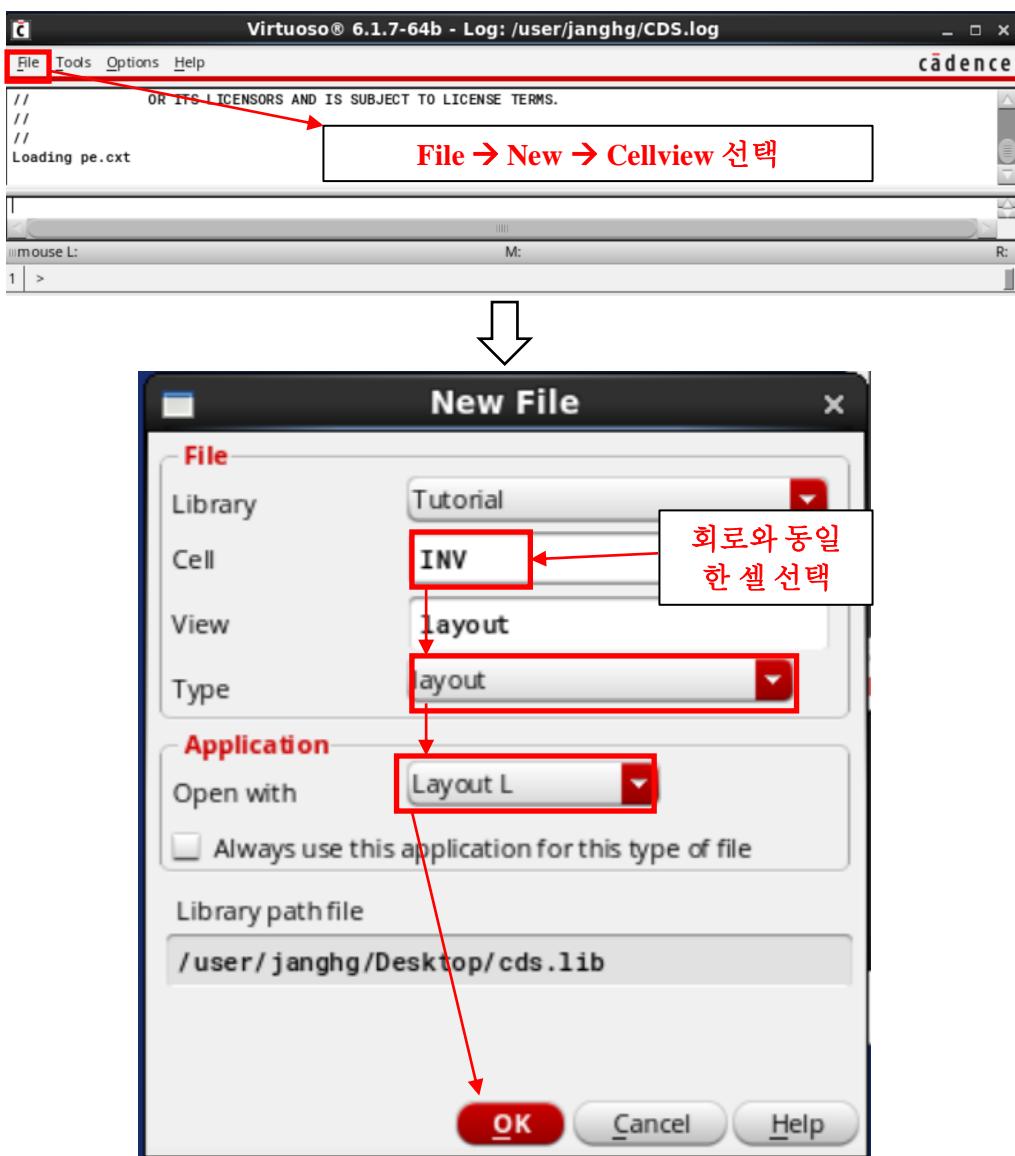
4. Layout

4. Layout

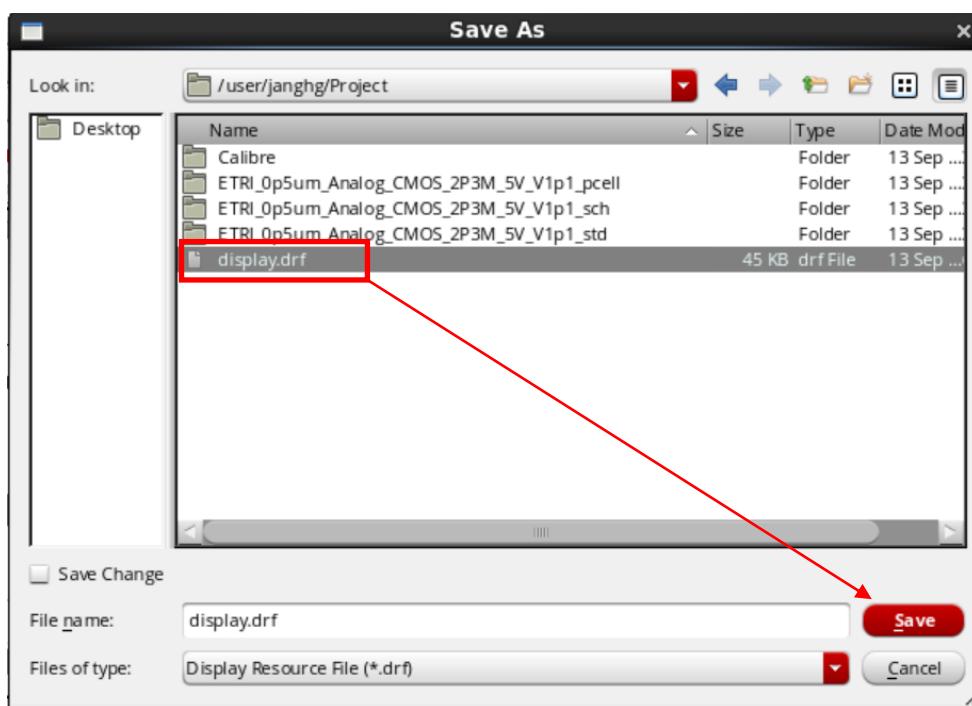
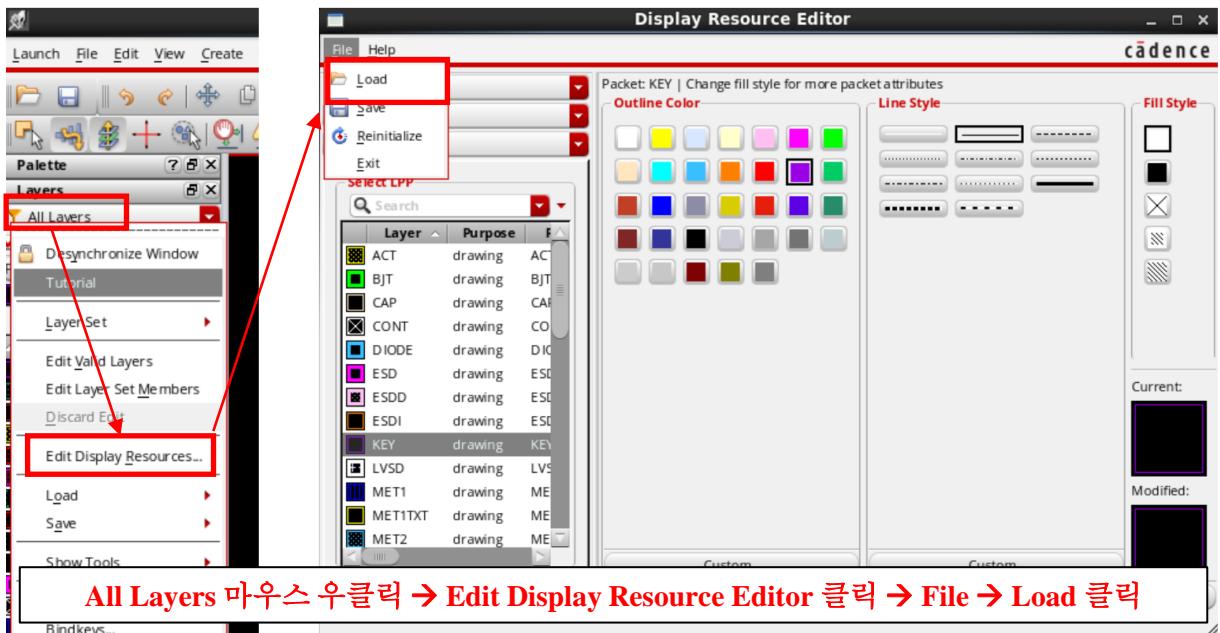
- 목적 : 반도체 회로 제작을 위한 레이아웃 설계
- 예: 설계된 인버터 회로로 적용

1) 인버터 회로의 레이아웃 설계

① 레이아웃 디자인 설계 프로그램 실행

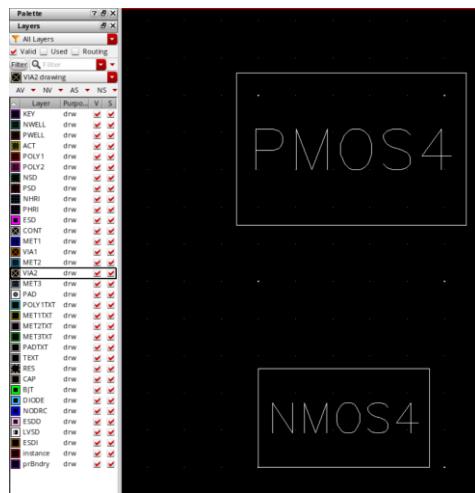
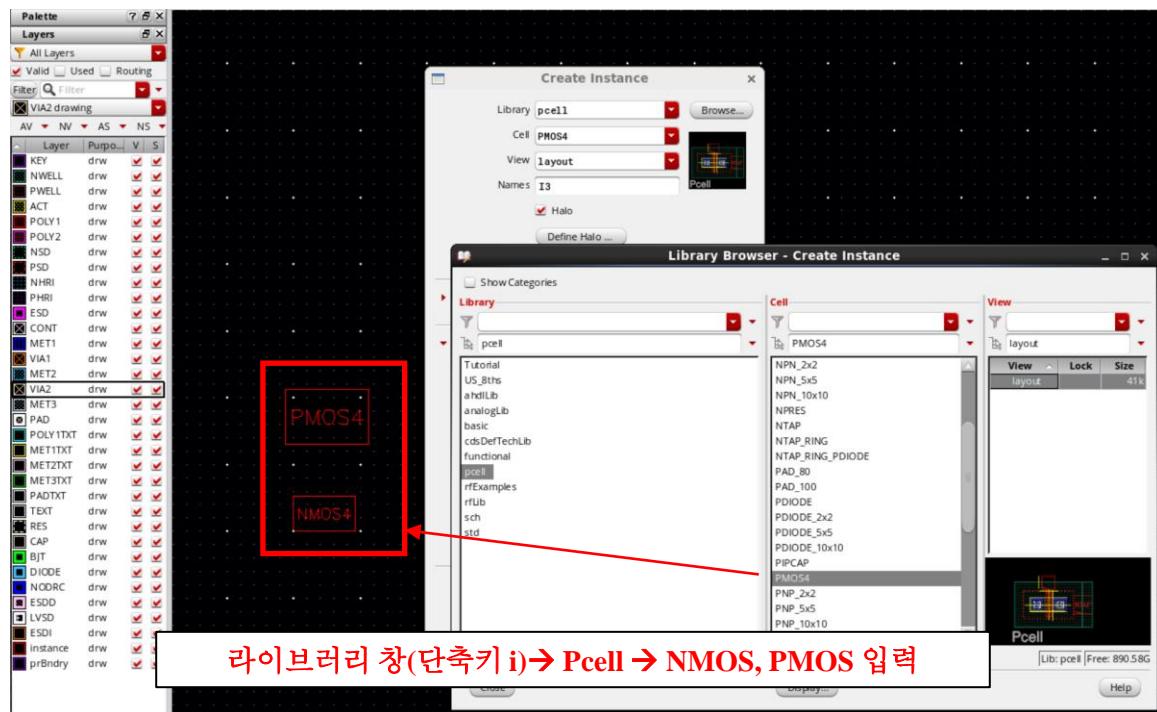


② Display resource 파일 불러오기

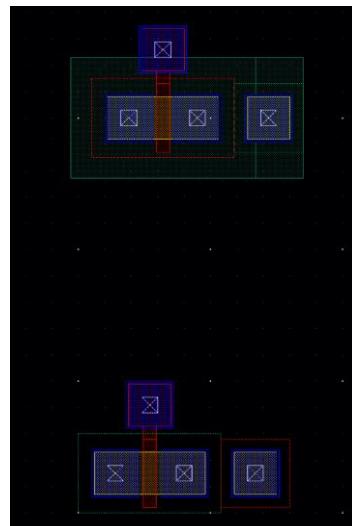
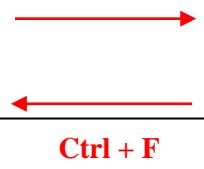


제공된 xxx.drf 선택 → 저장

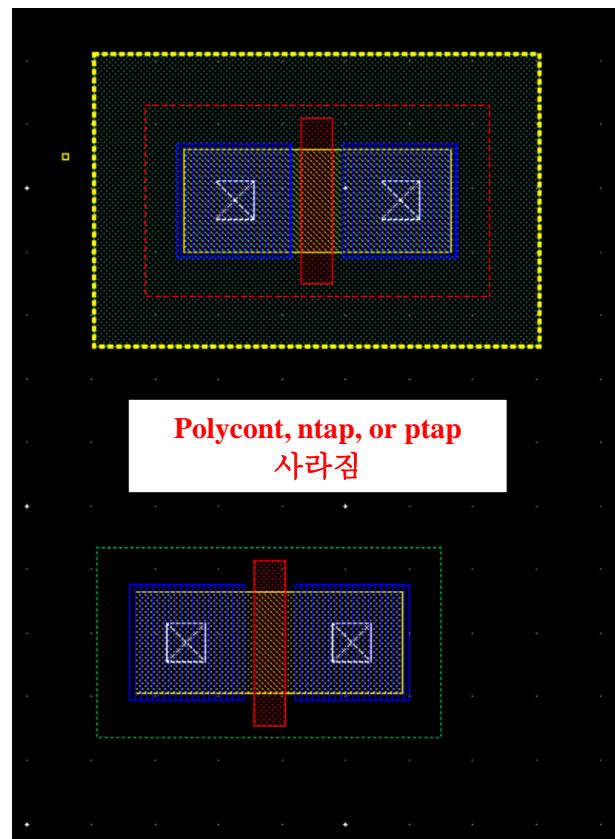
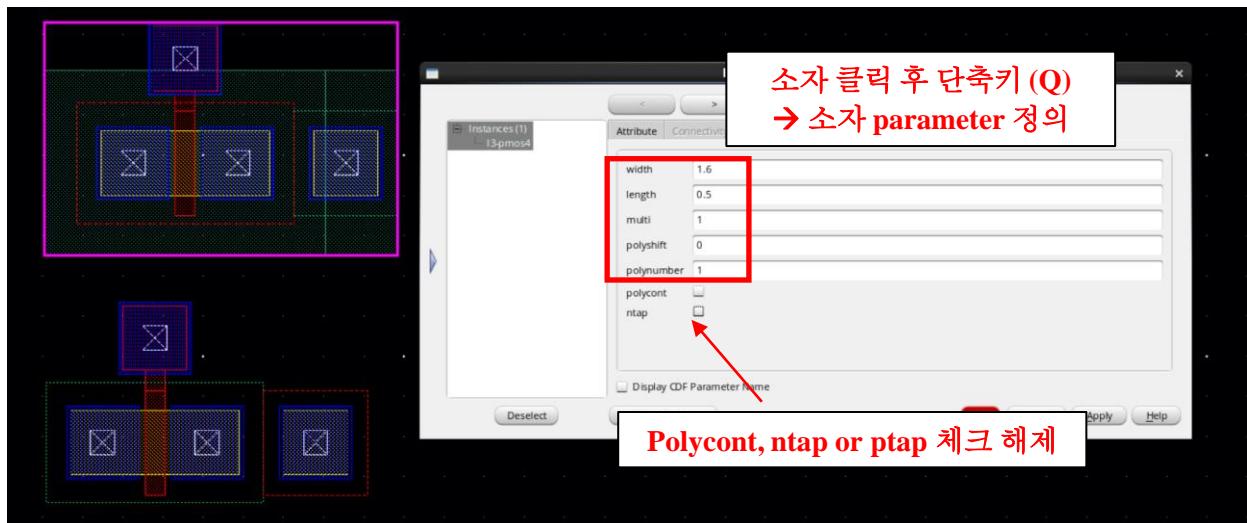
③ Pcell 불러오기



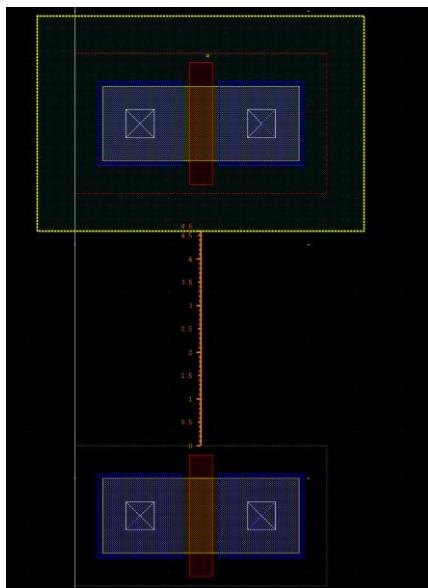
Shift + F



④ Pcell 파라미터 설정

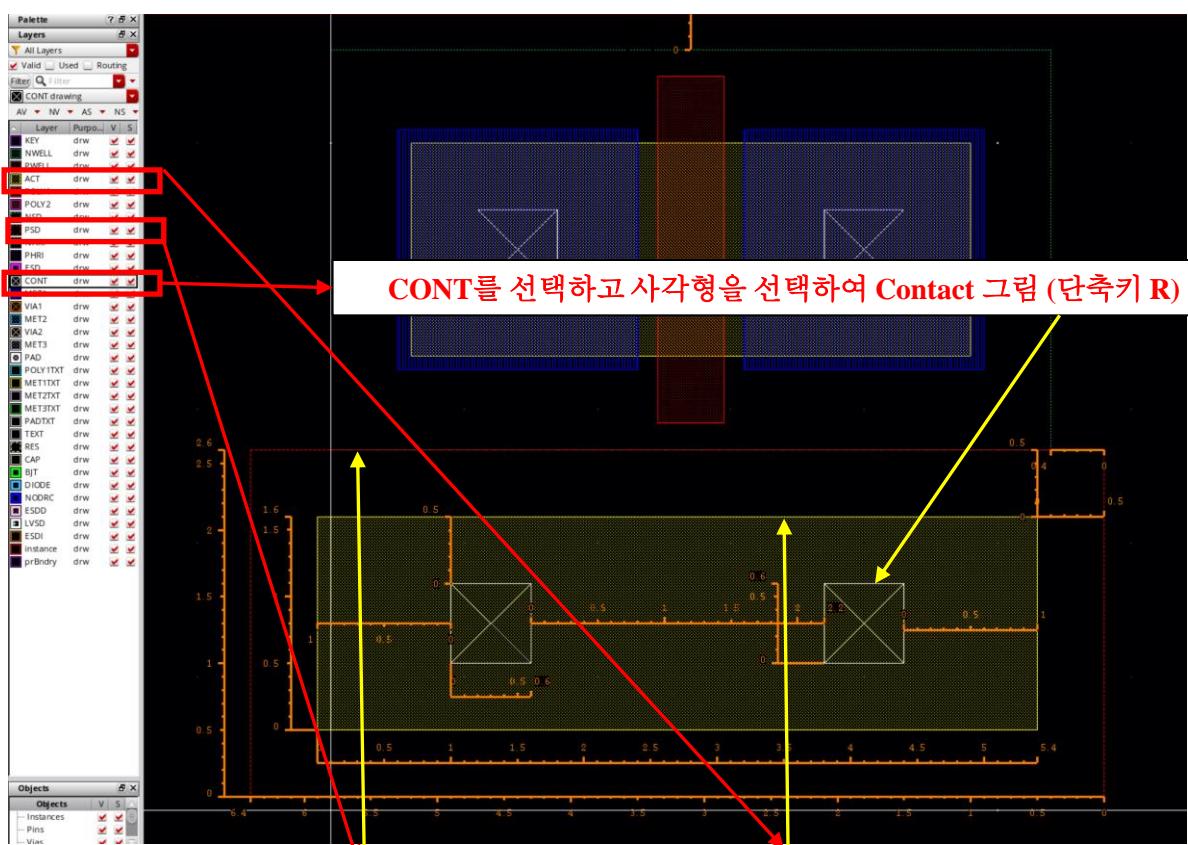


⑤ Layout 진행



Ruler를 이용하여 사이즈를 확인함(단축키 K)
모든 Ruler를 사라지게 하는 단축키 → Shift + K

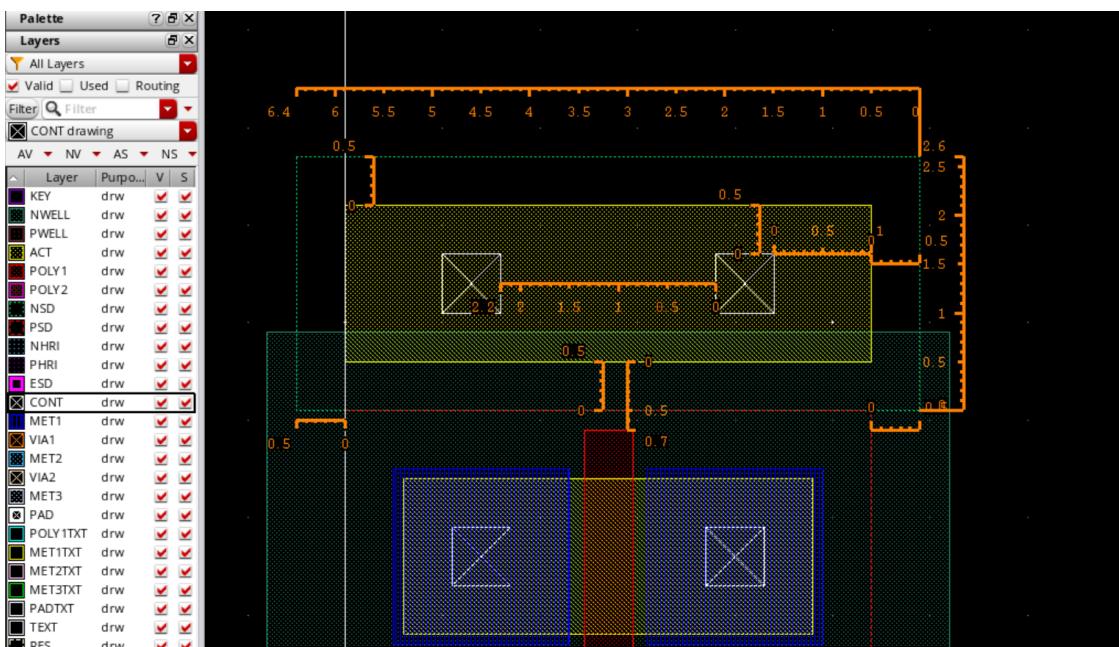
PMOS, NMOS 적절한 위치 배치



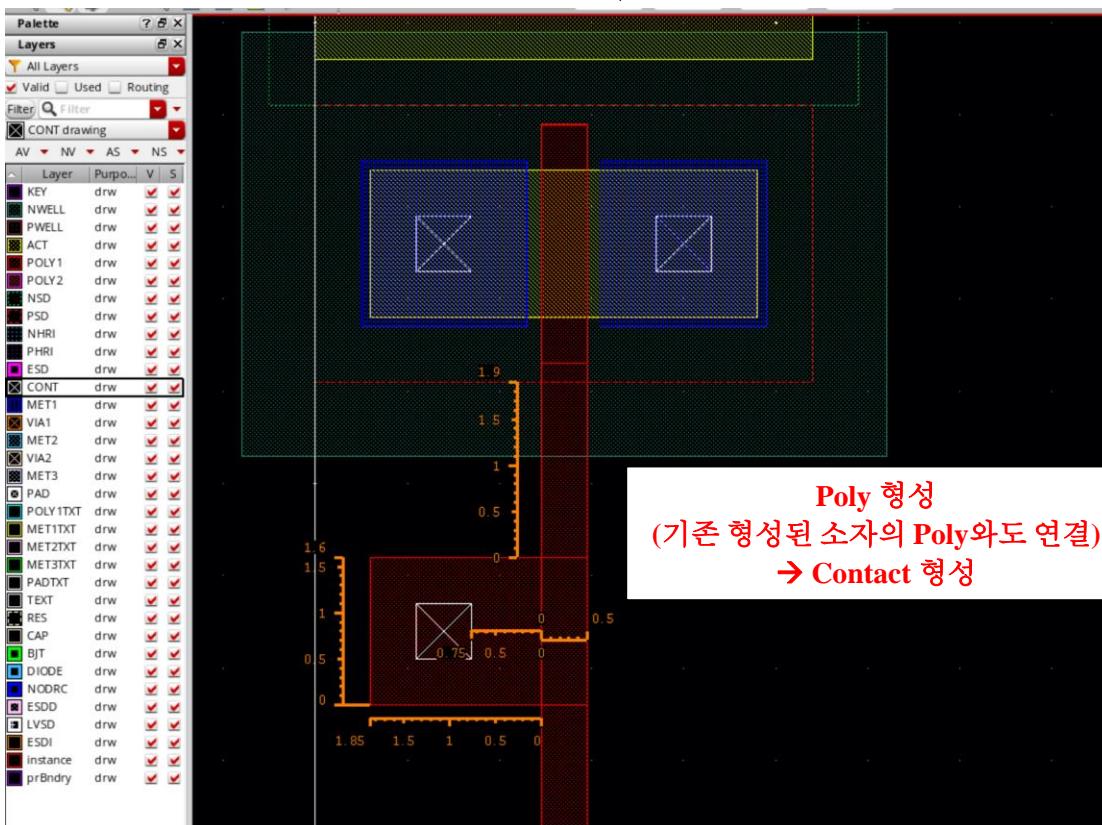
CONT를 선택하고 사각형을 선택하여 Contact 그림 (단축키 R)

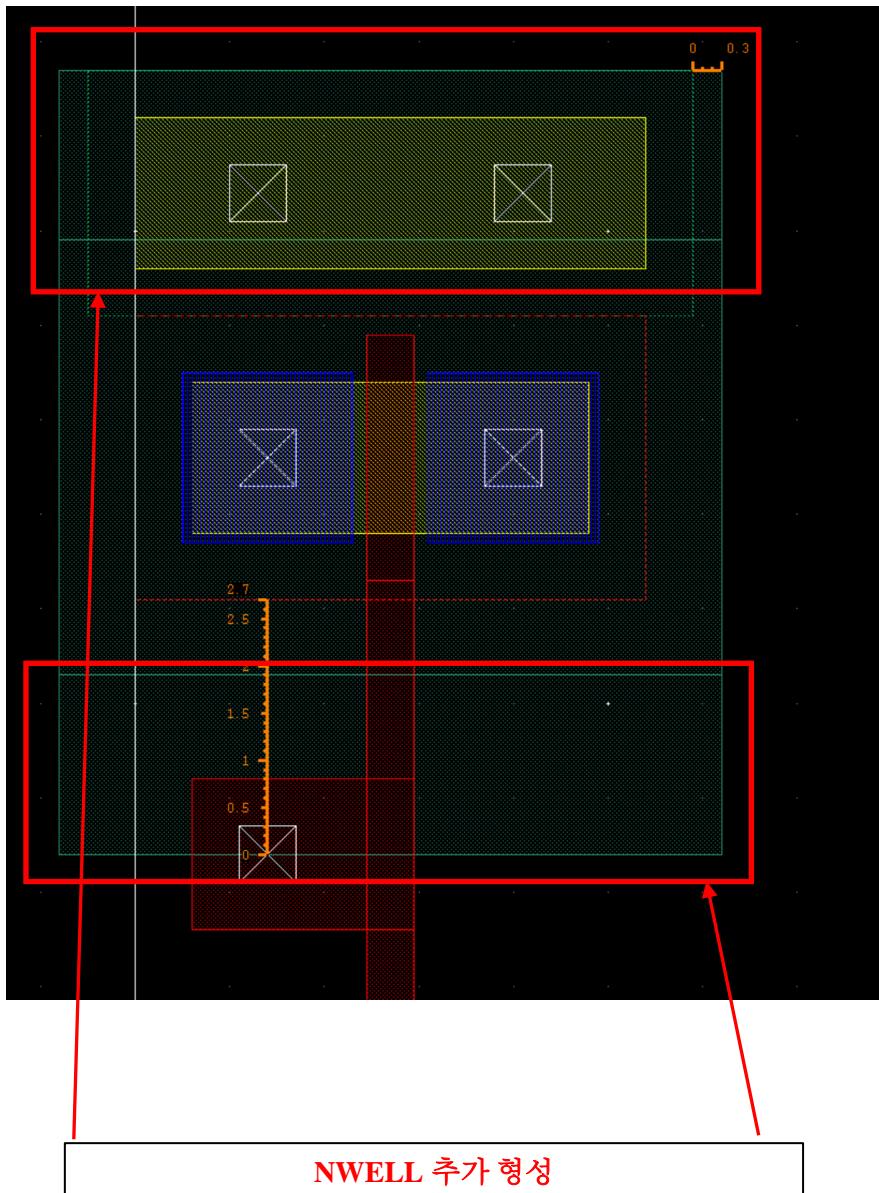
PSD 선택 → 단축키 R → PSD 그림

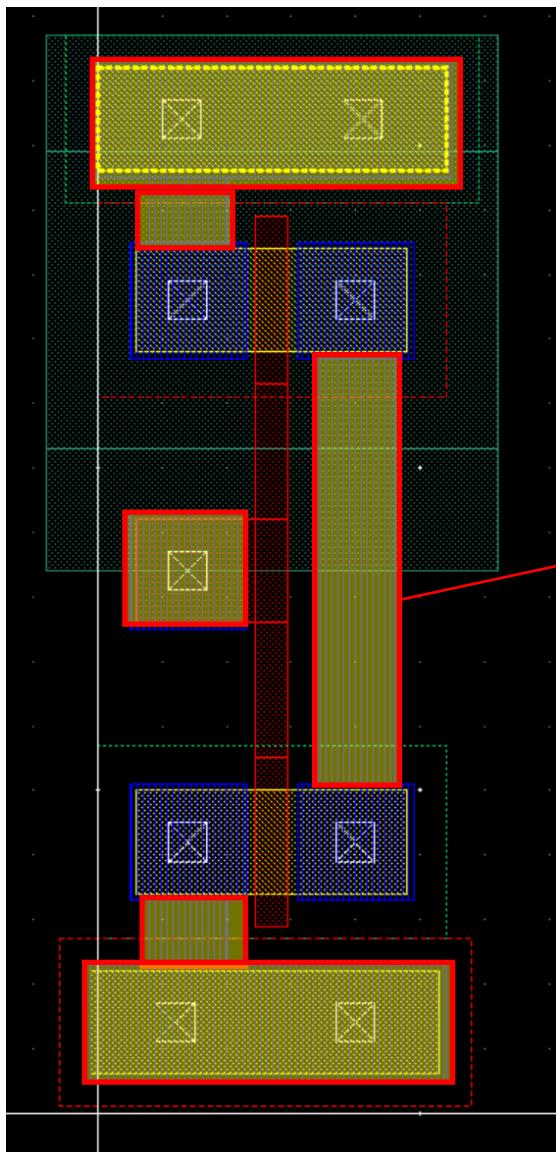
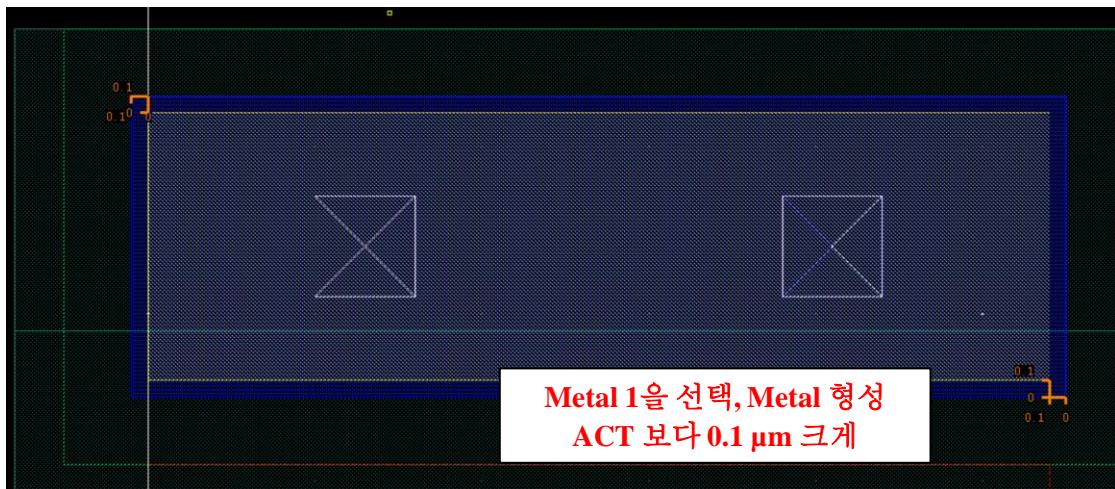
ACT 선택 → 단축키 R → ACT 그림



VDD : NSD → ACT → CONT 순서로 설계



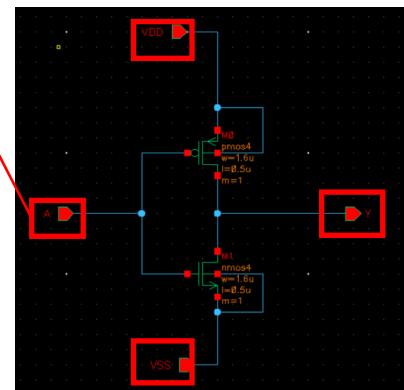
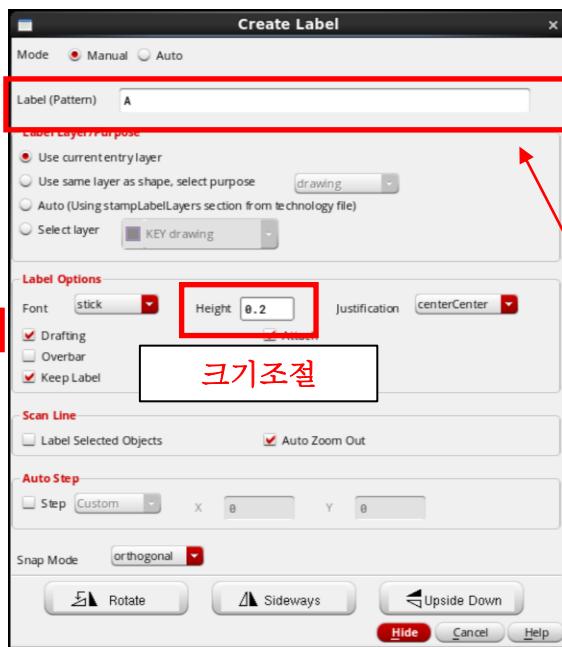




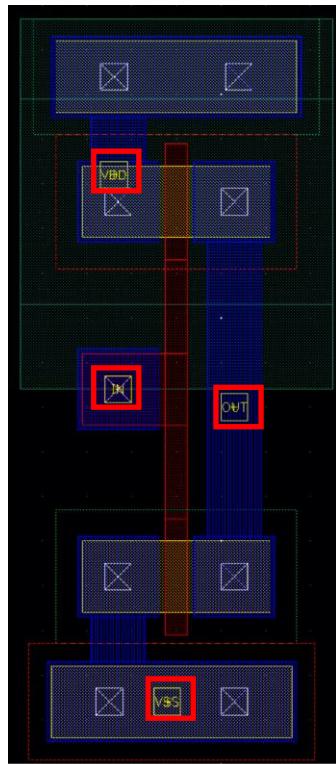
위와같은 방법으로 Metal 1을
이용하여 좌측과 같이 소자간
연결

⑥ Label 할당

MET3	drw	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
PAD	drw	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
POLY1TXT	drw	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
MET1TXT	drw	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
MET2TXT	drw	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
MET3TXT	drw	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>

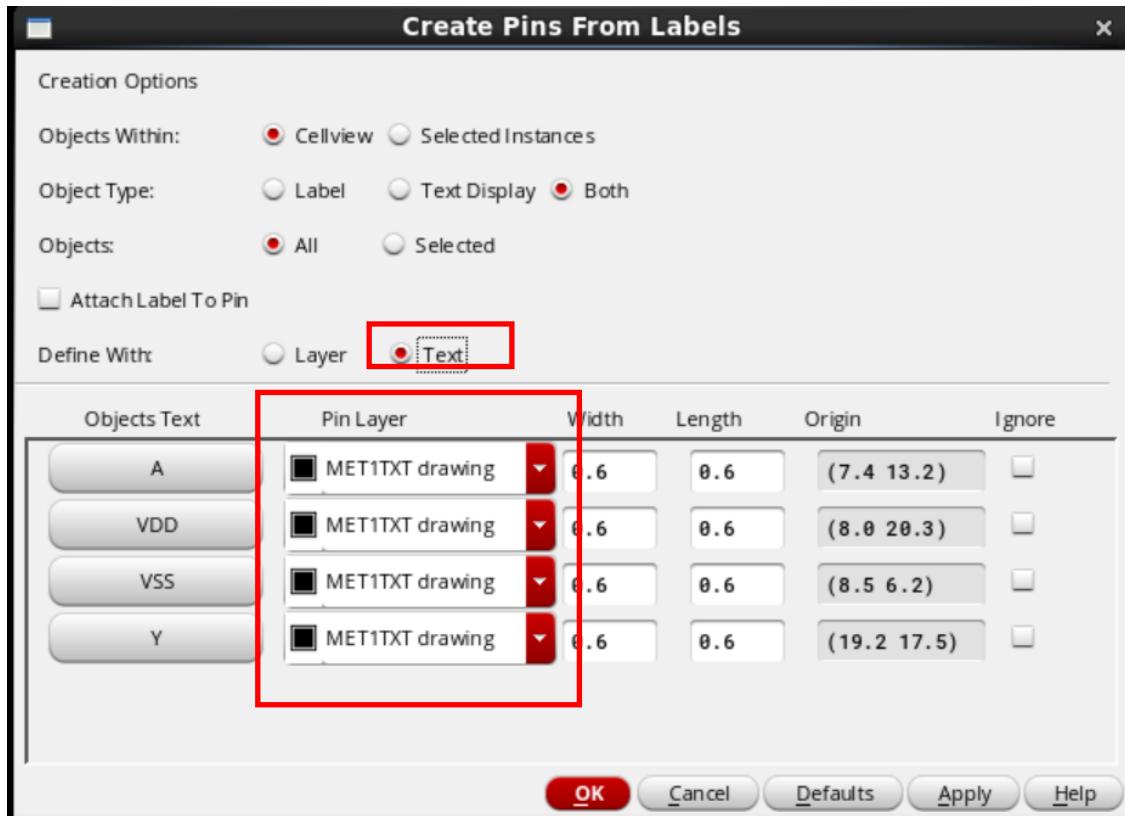


Label 설정 : MET1TXT Layer 선택 → Create → Label (단축키 L)
 → Label명은 회로도와 동일하게 할당



Metal1 안쪽으로 각각의
Label 배치

⑦ Label로 부터 Pin 할당



File → Save

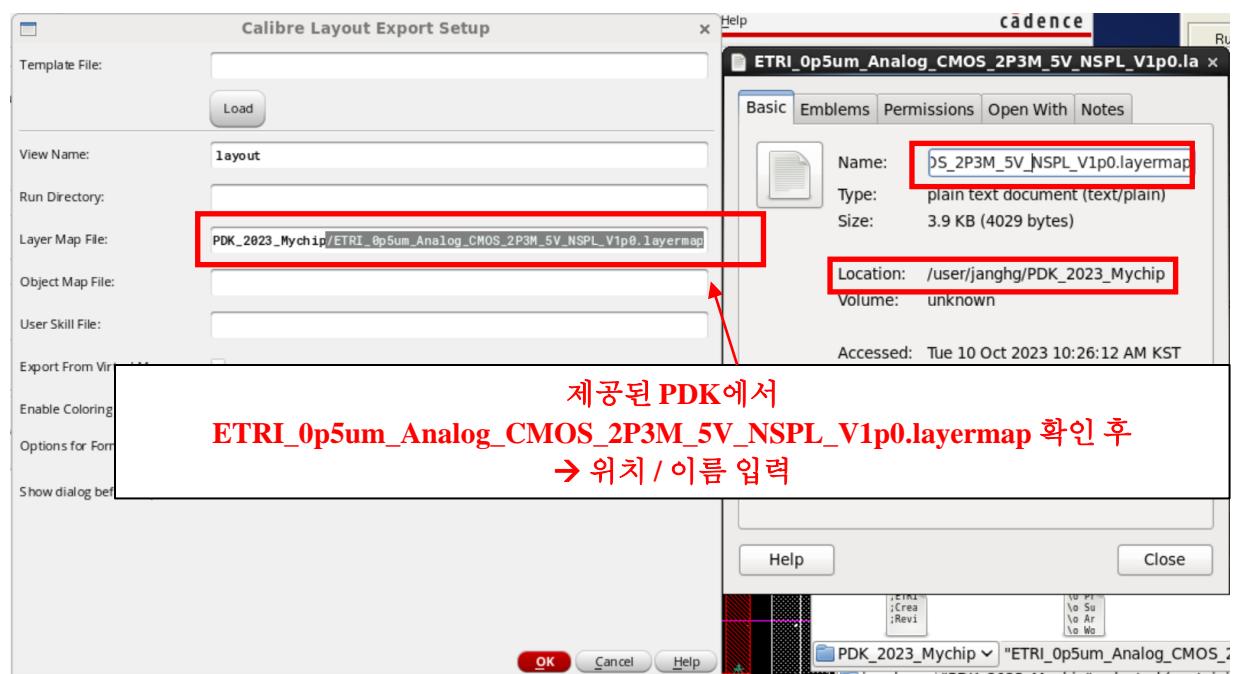
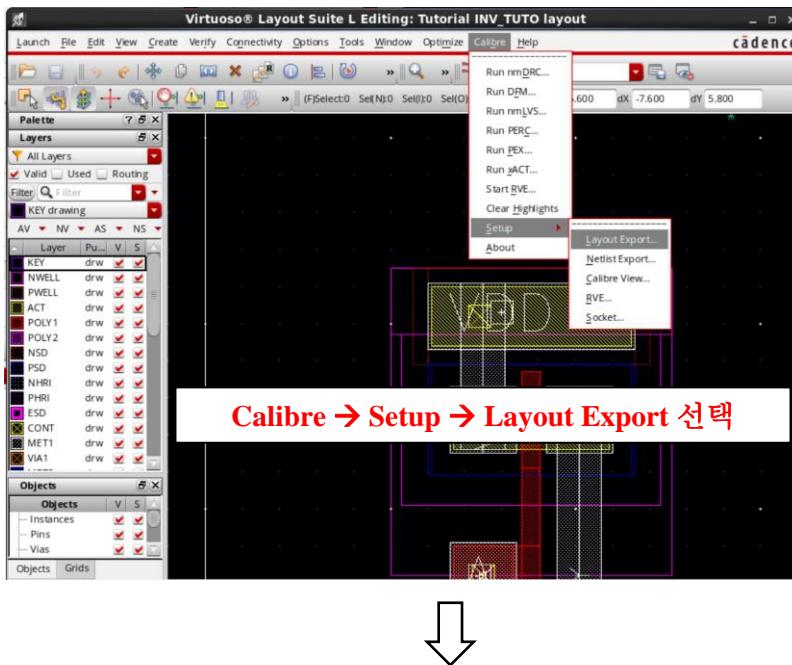
5. DRC (Design Rule Check)

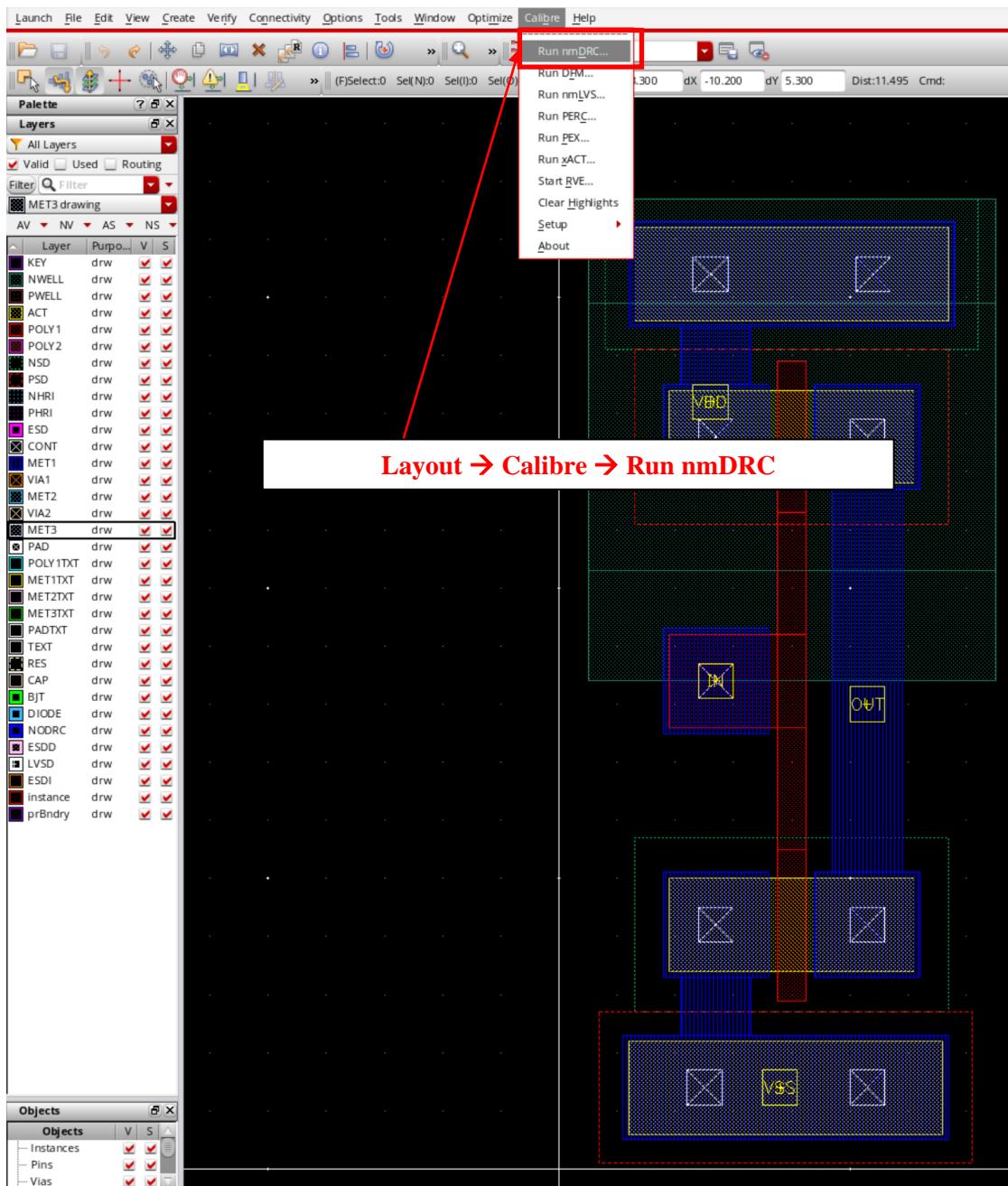
5. DRC

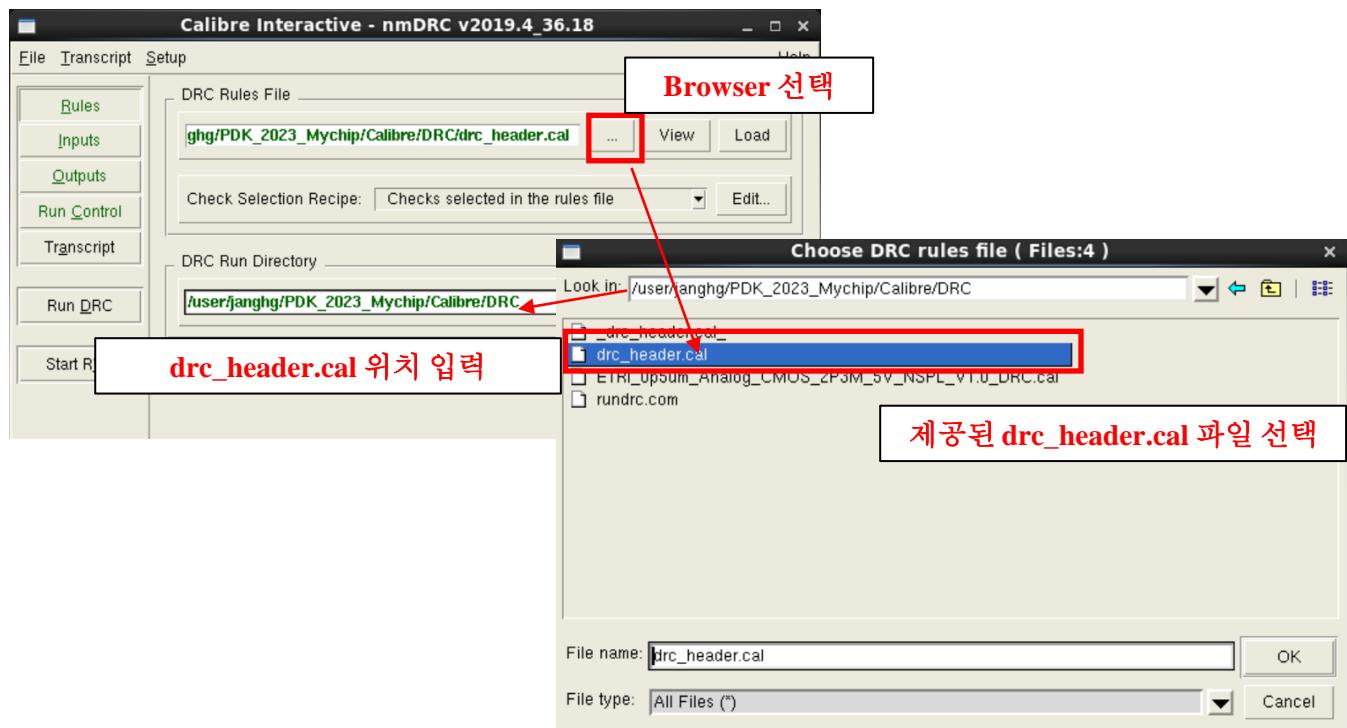
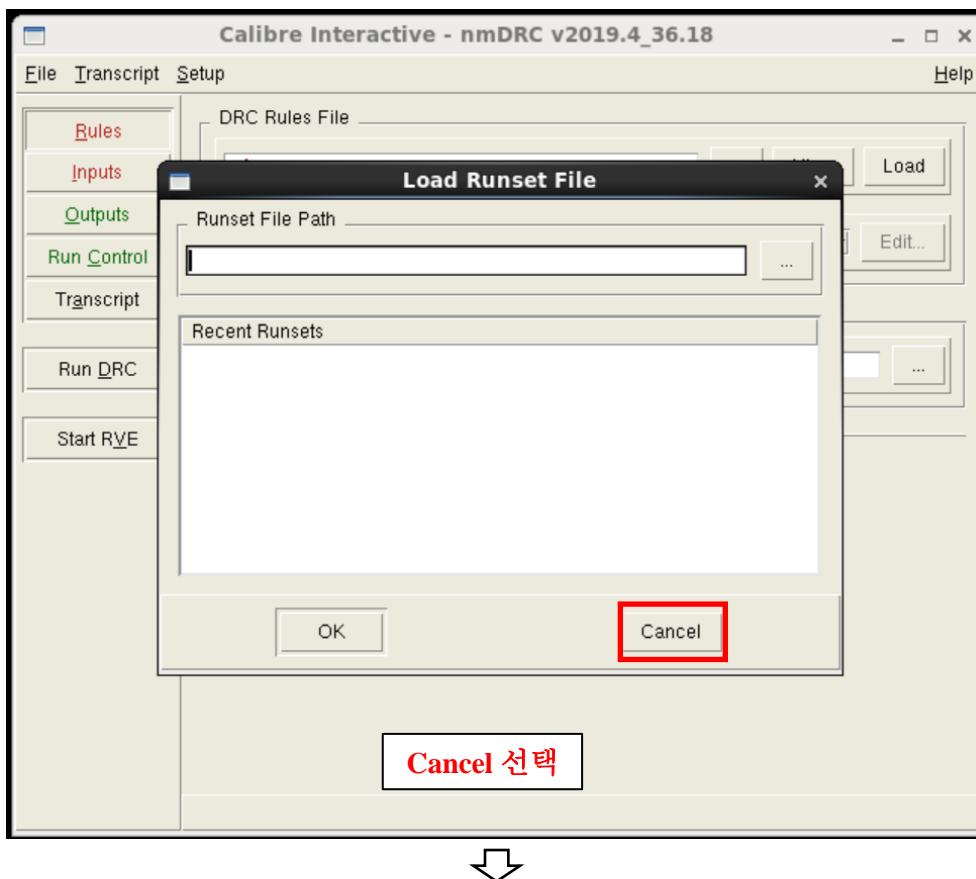
- 목적 : 설계된 레이아웃 디자인이 디자인룰에 적합한지 검토

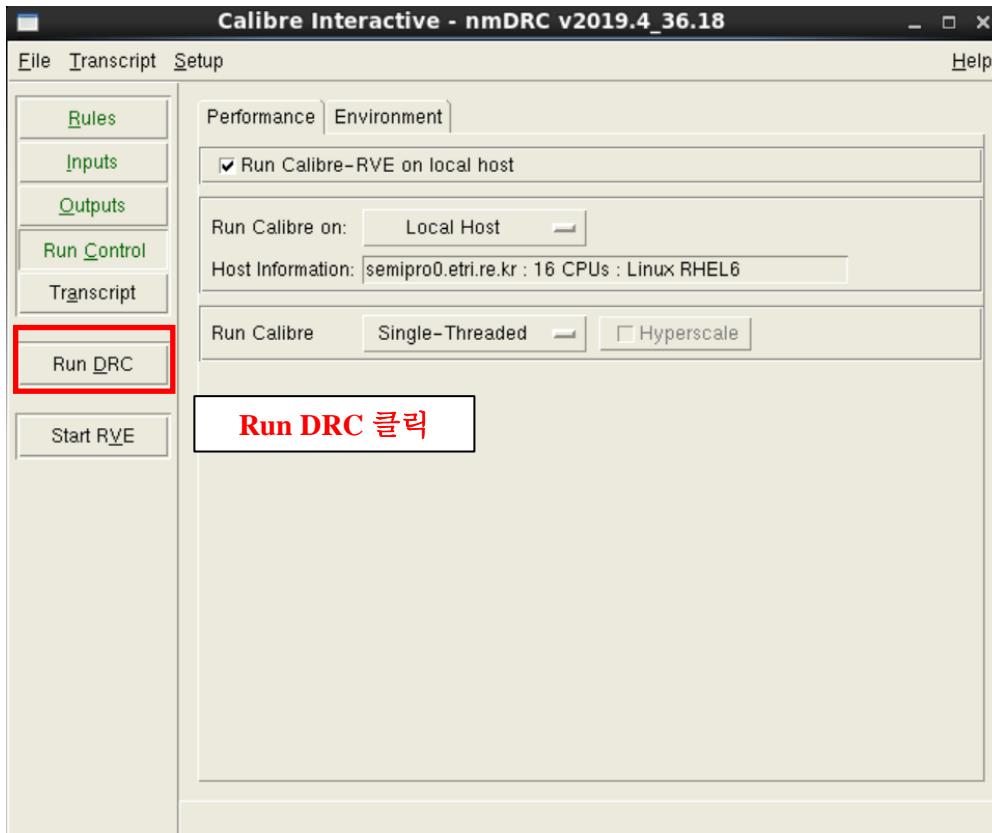
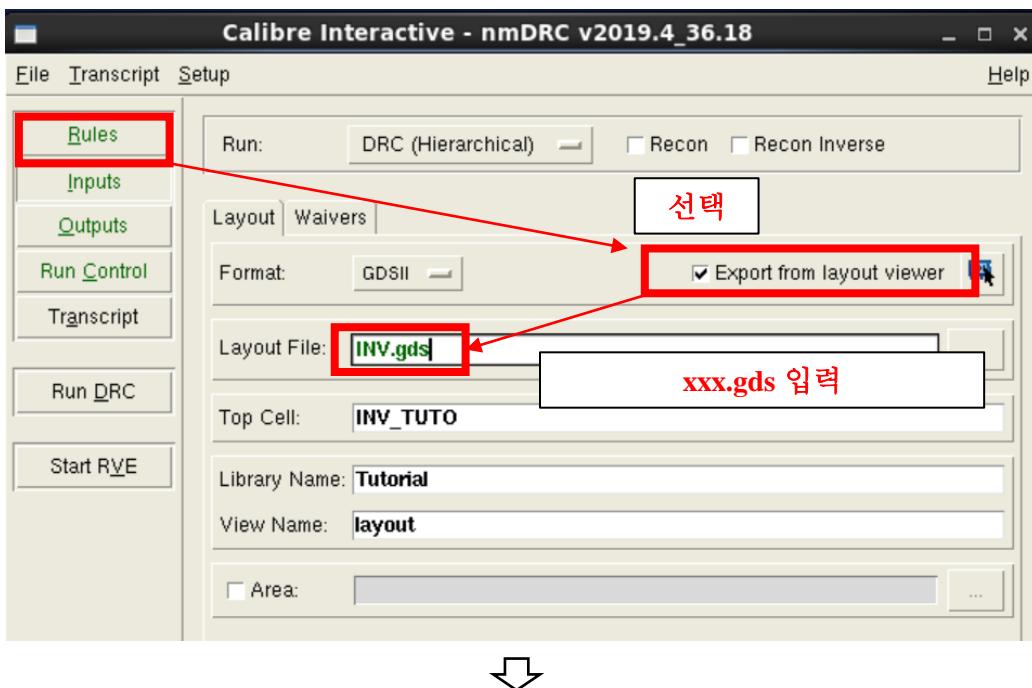
1) Calibre DRC 검토

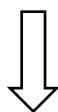
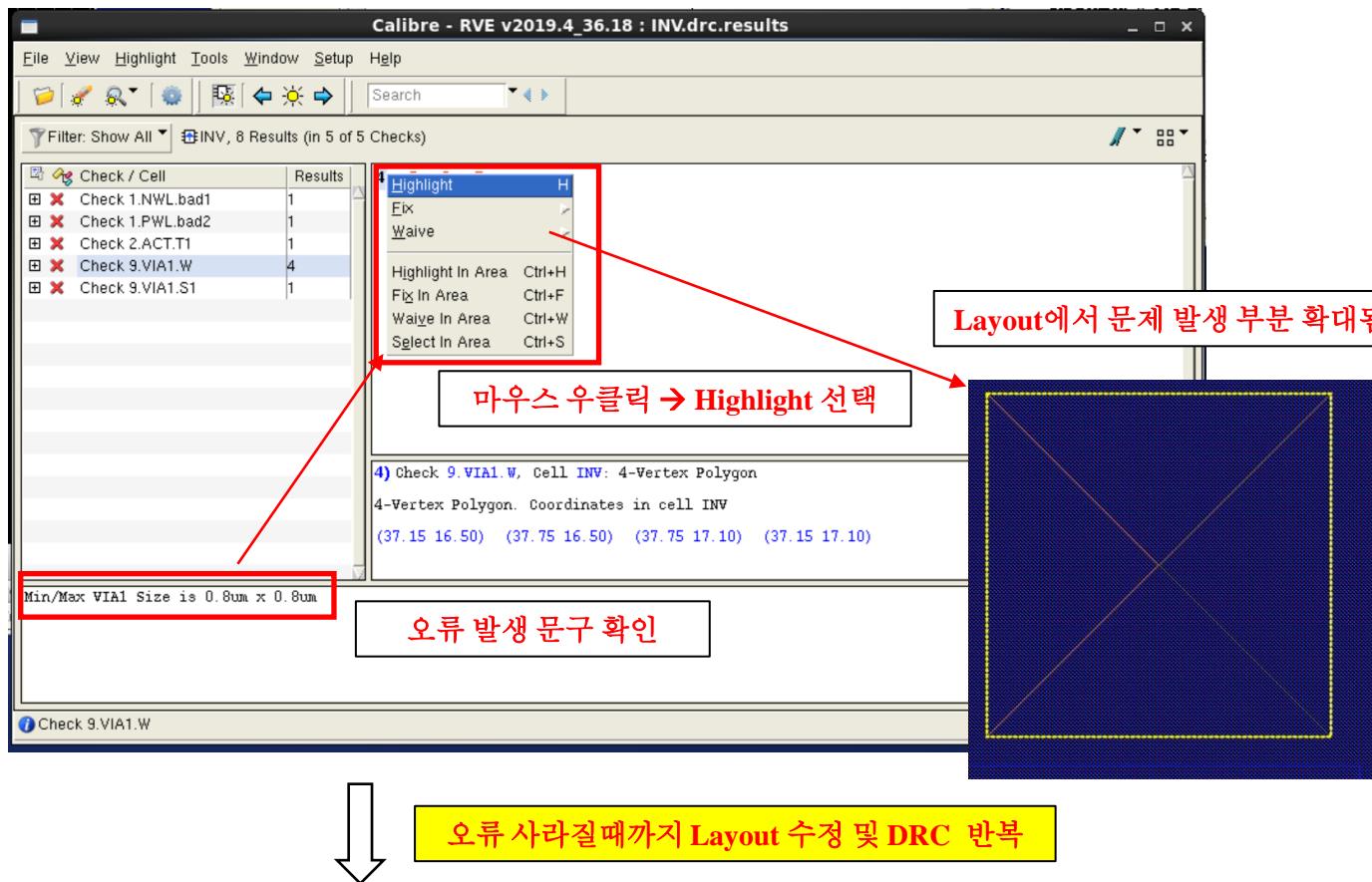
① DRC 검증 방법



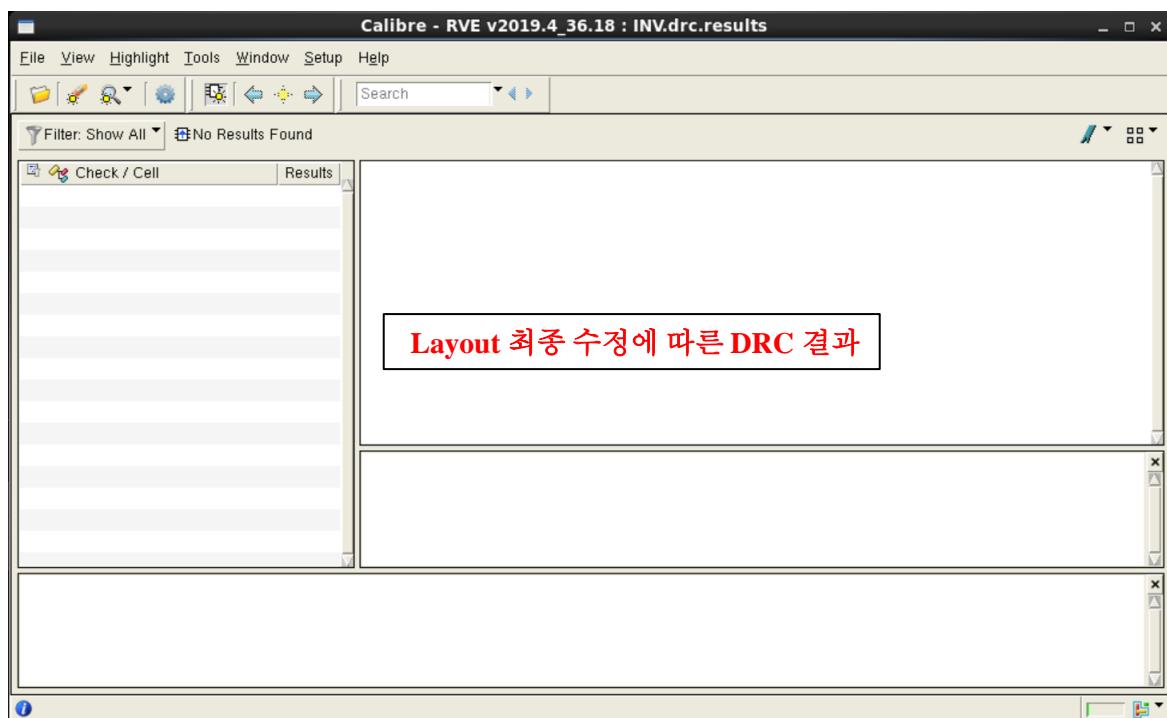






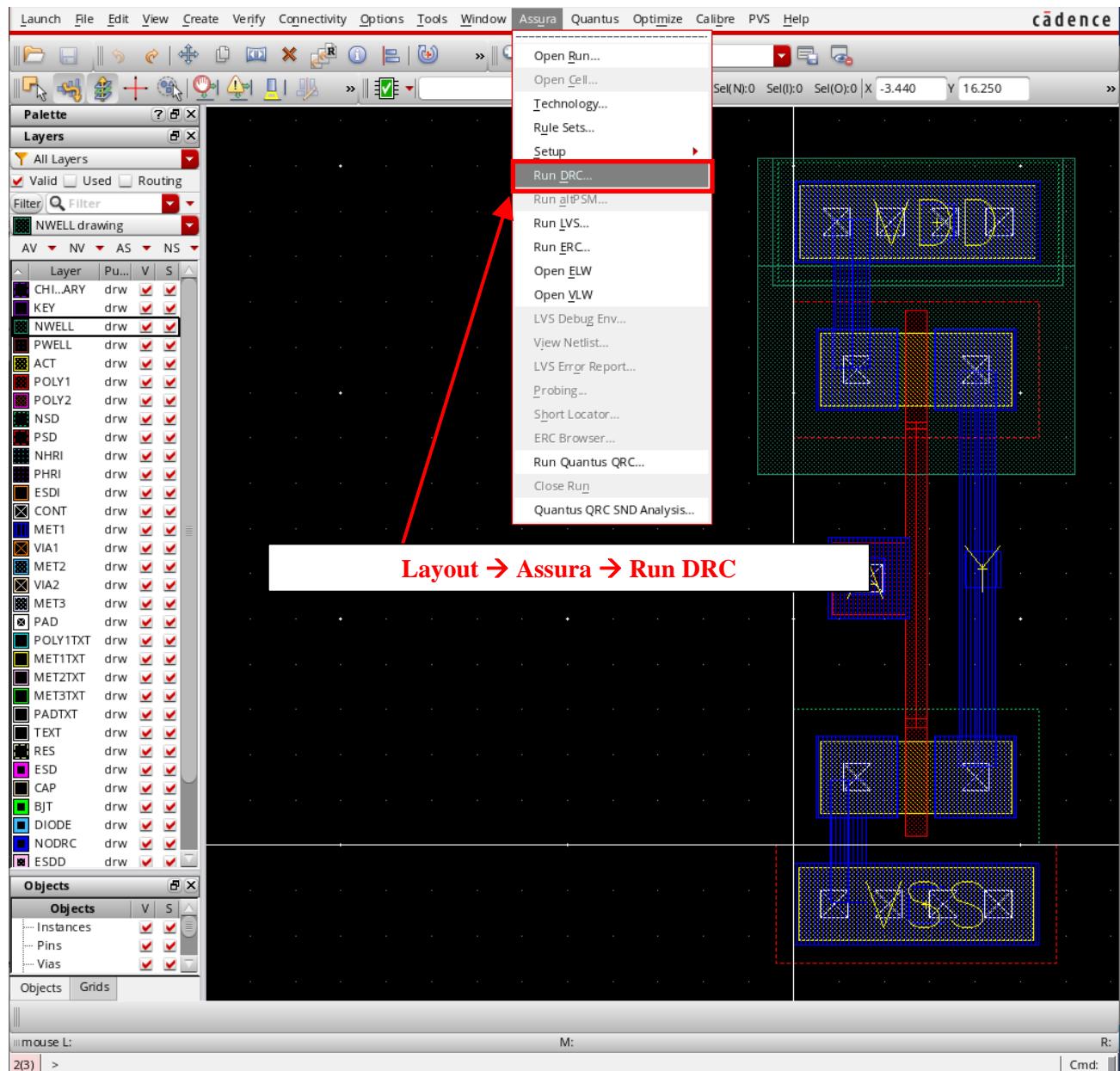


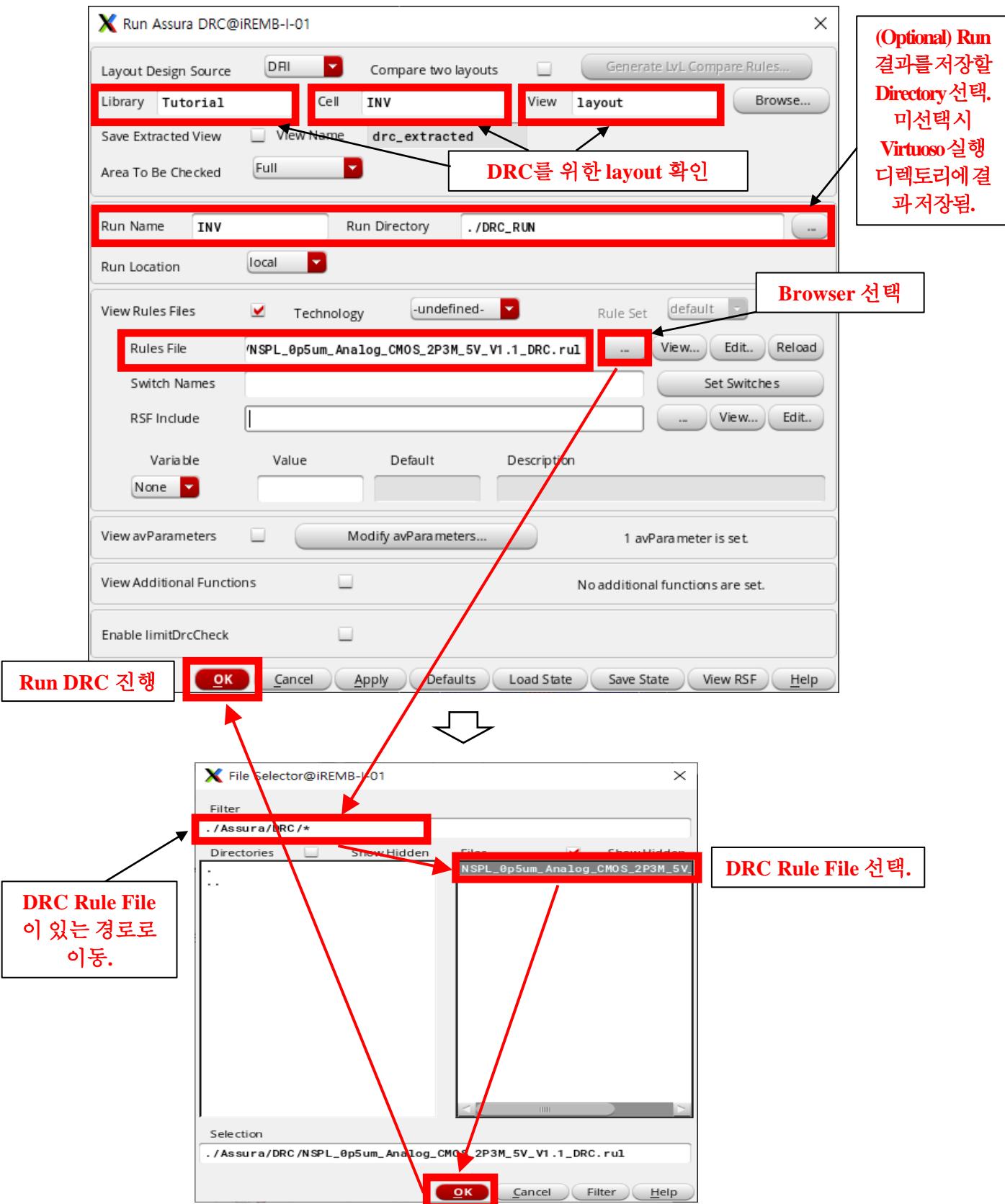
오류 사라질때까지 Layout 수정 및 DRC 반복

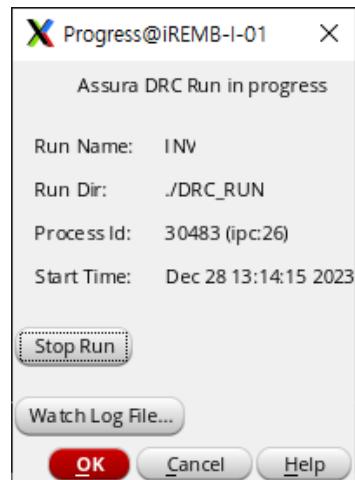


2) Assura DRC 검토

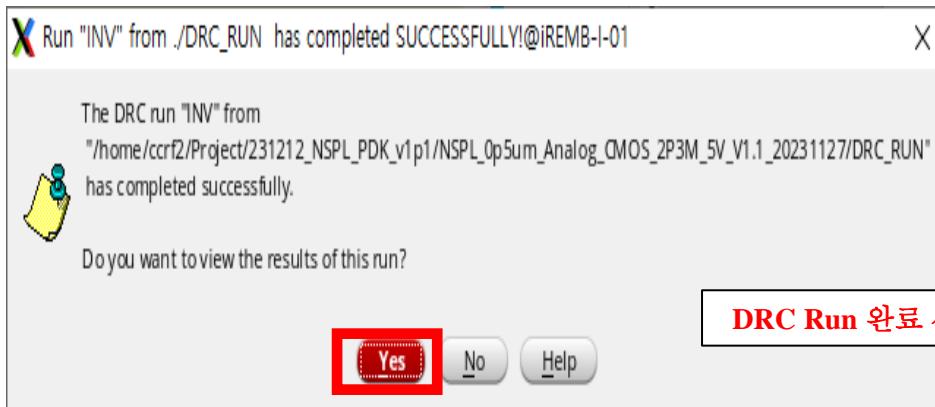
① DRC 검증 방법







**DRC Run Progress 화면.
(Run 완료 후 자동으로 화면 사라짐)**



DRC Run 완료 시, dialog box.

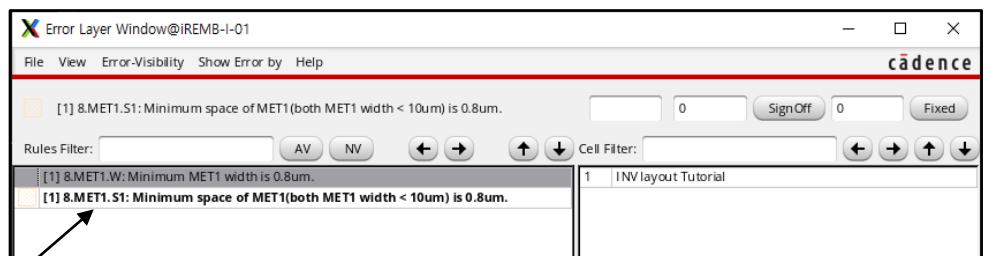
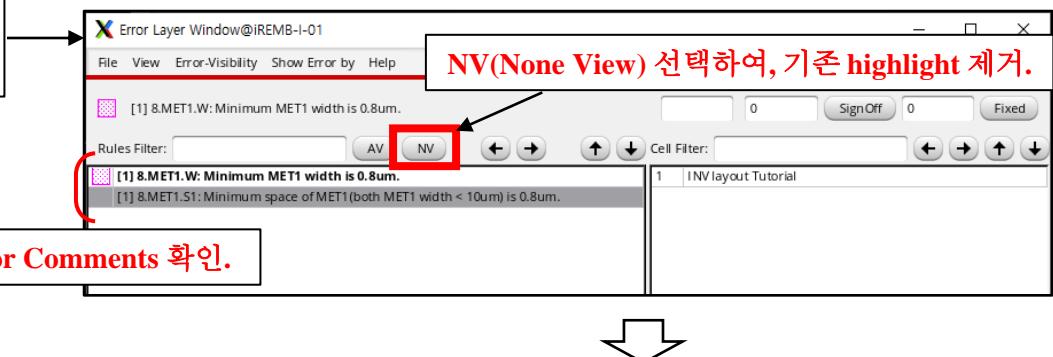


DRC pass

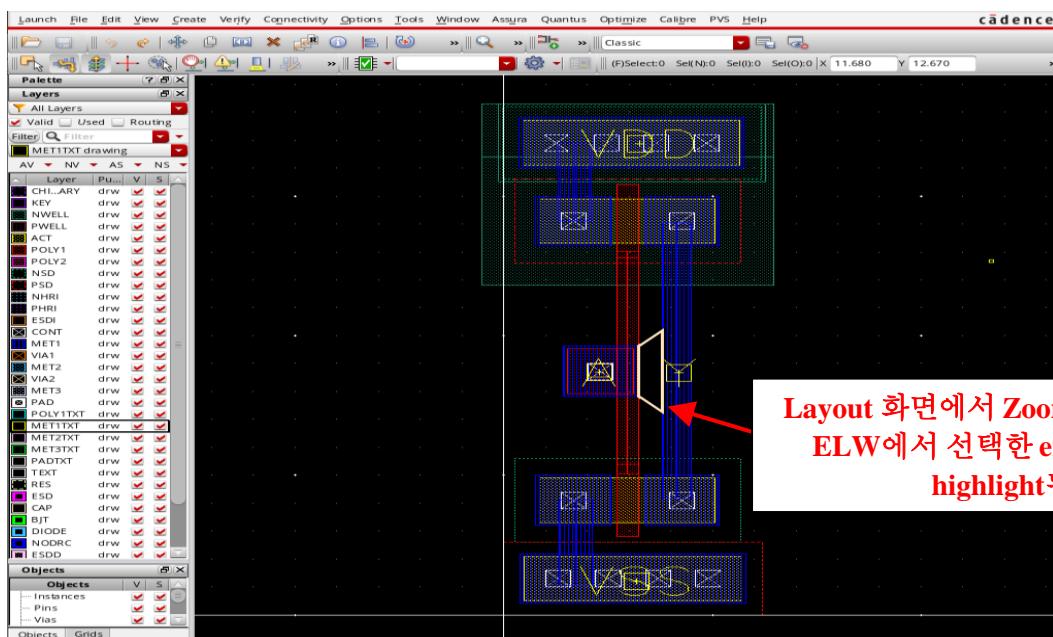
② DRC Debug

DRC error 발생 시,
ELW(Error Layer Window)
가 pop-up 됨.

DRC error 발생 예) Metal1 min. width / min. space error



수정할 DRC error item 선택.



오류 사라질 때까지 Layout 수정 및 DRC 반복

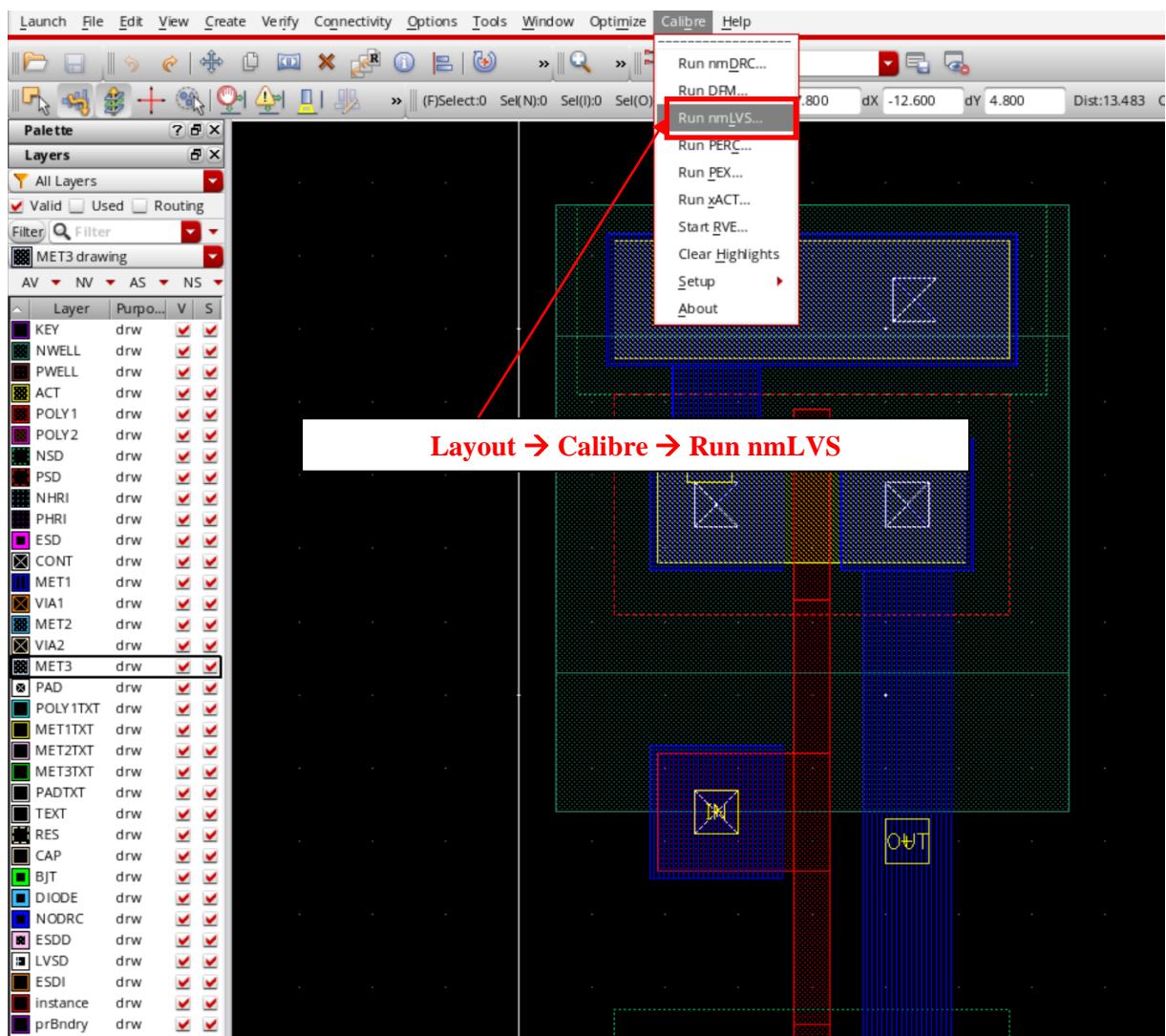
6. LVS (Layout Versus Schematic)

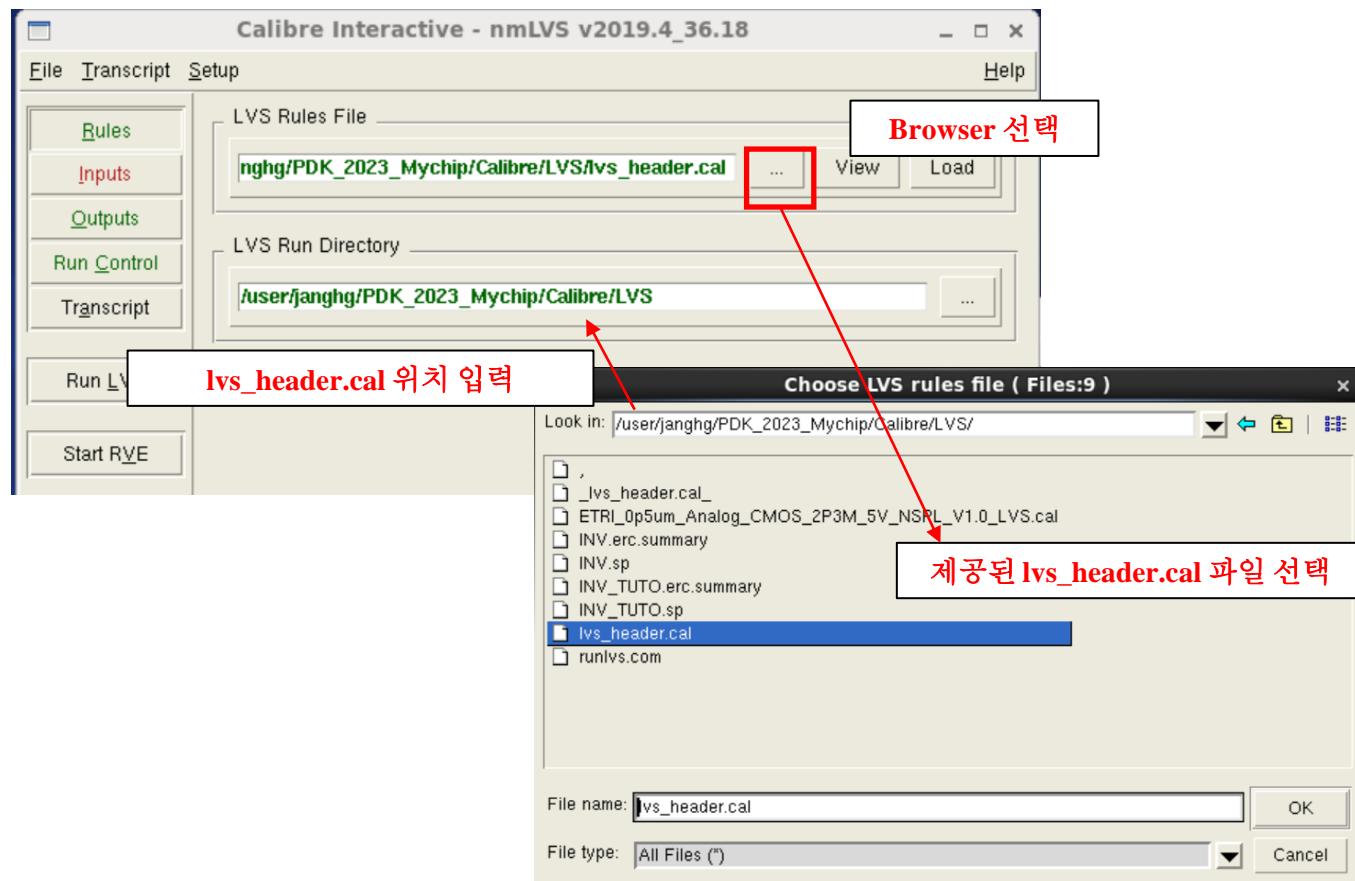
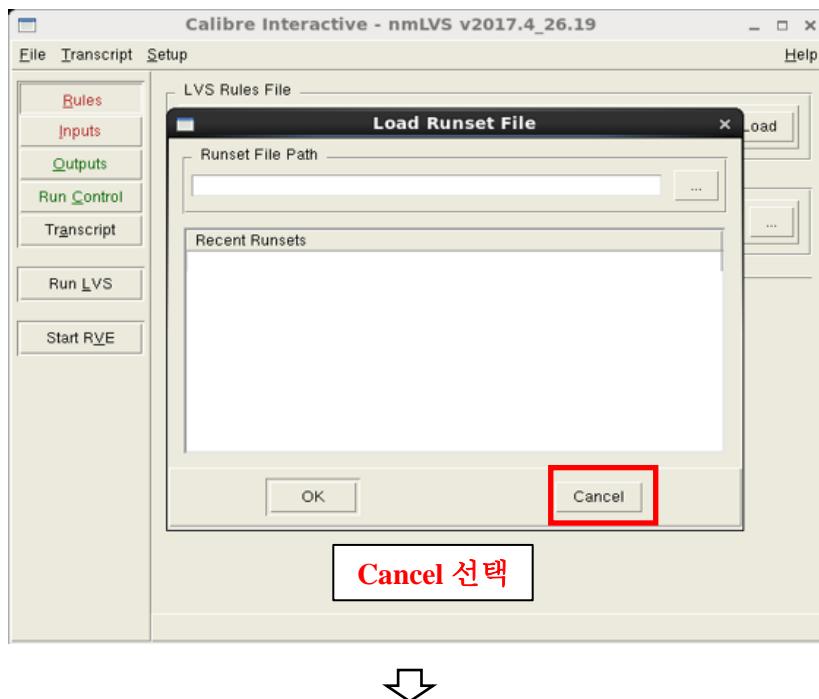
6. LVS

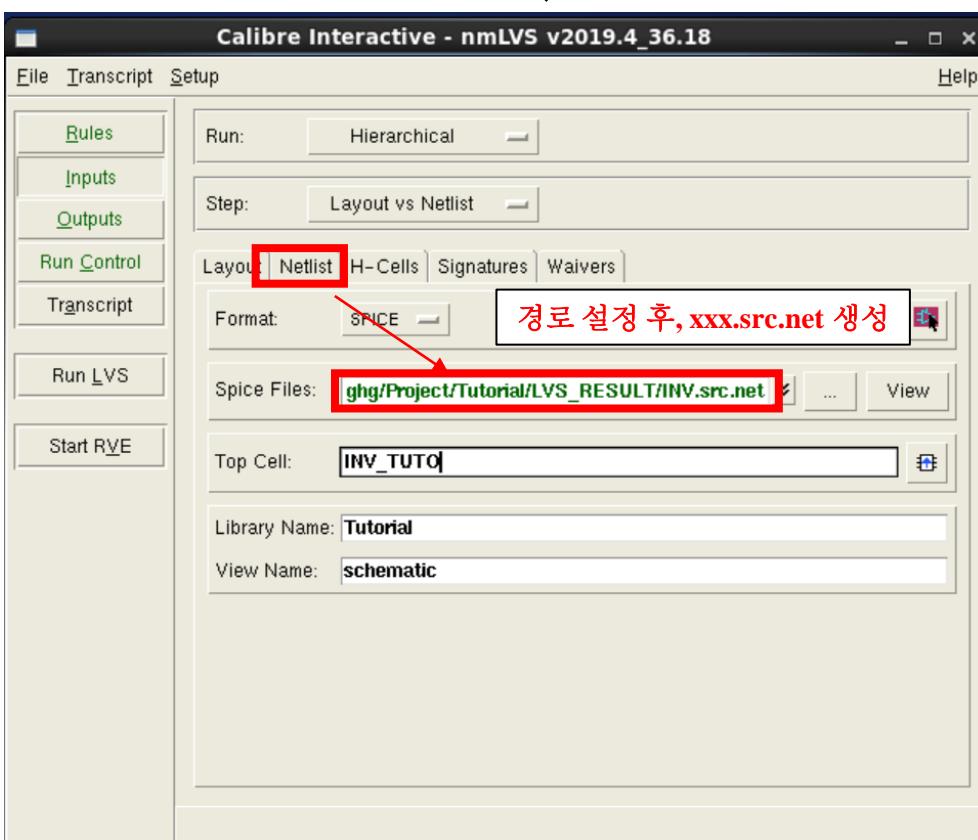
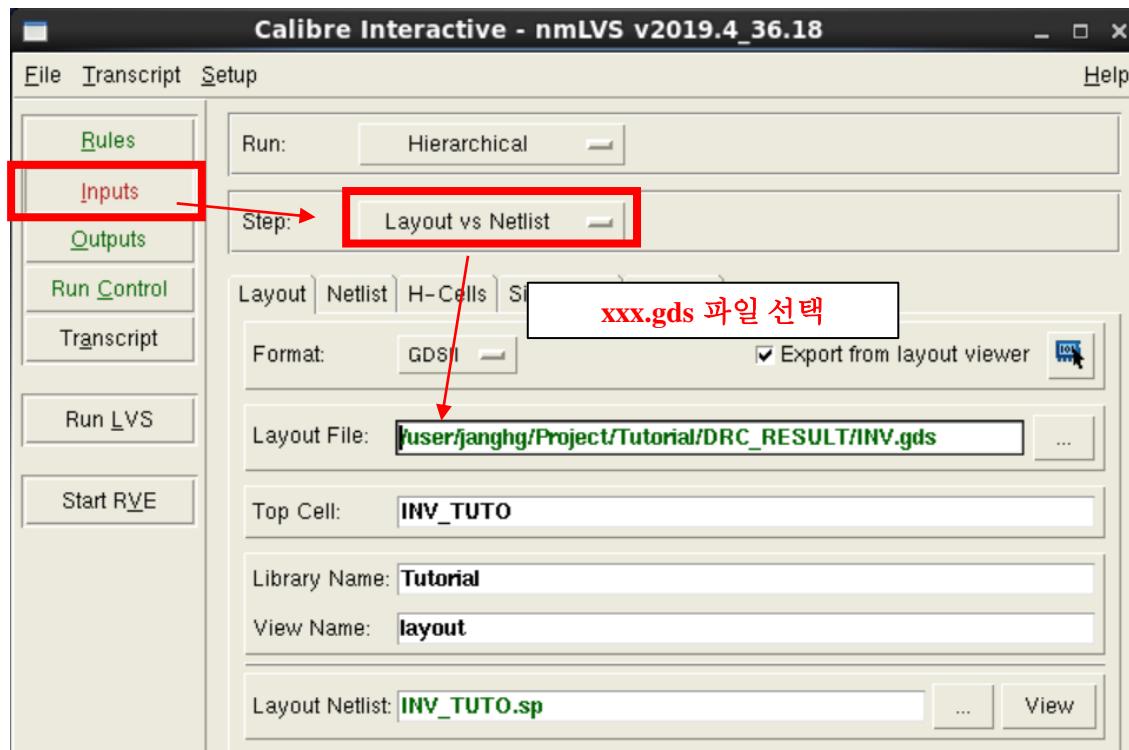
- 목적 : 설계한 Layout과 Schematic 비교

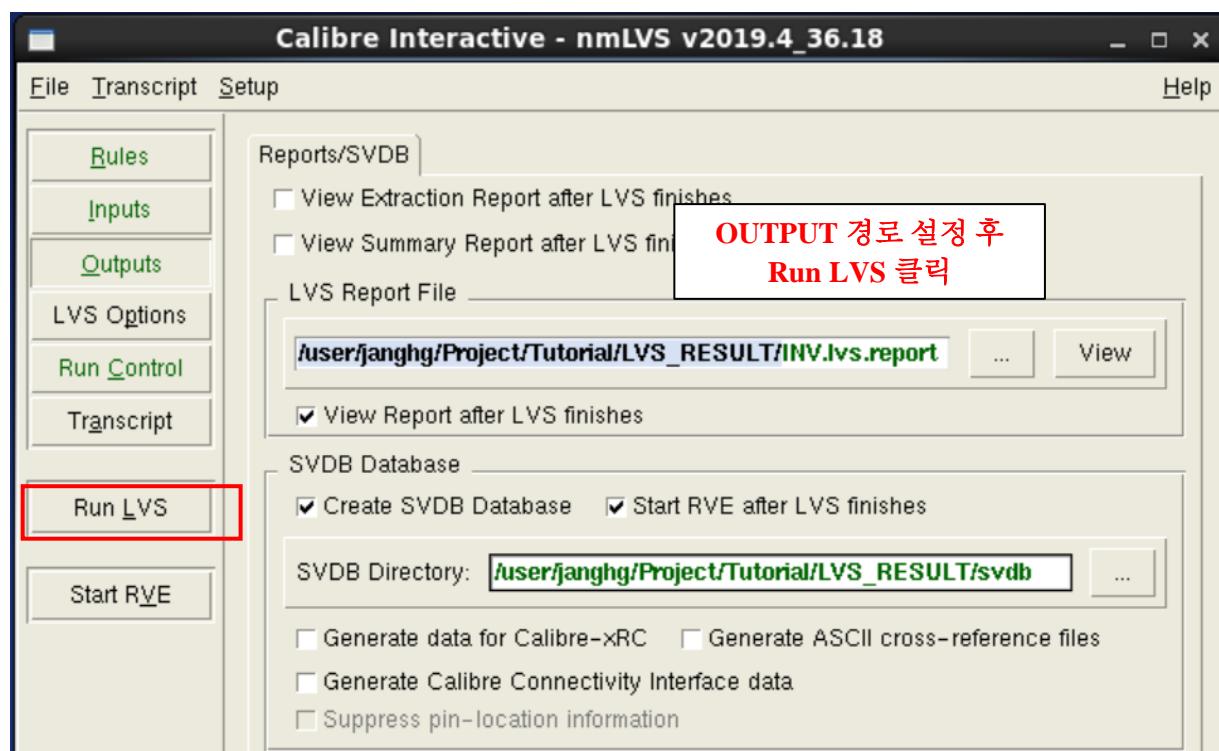
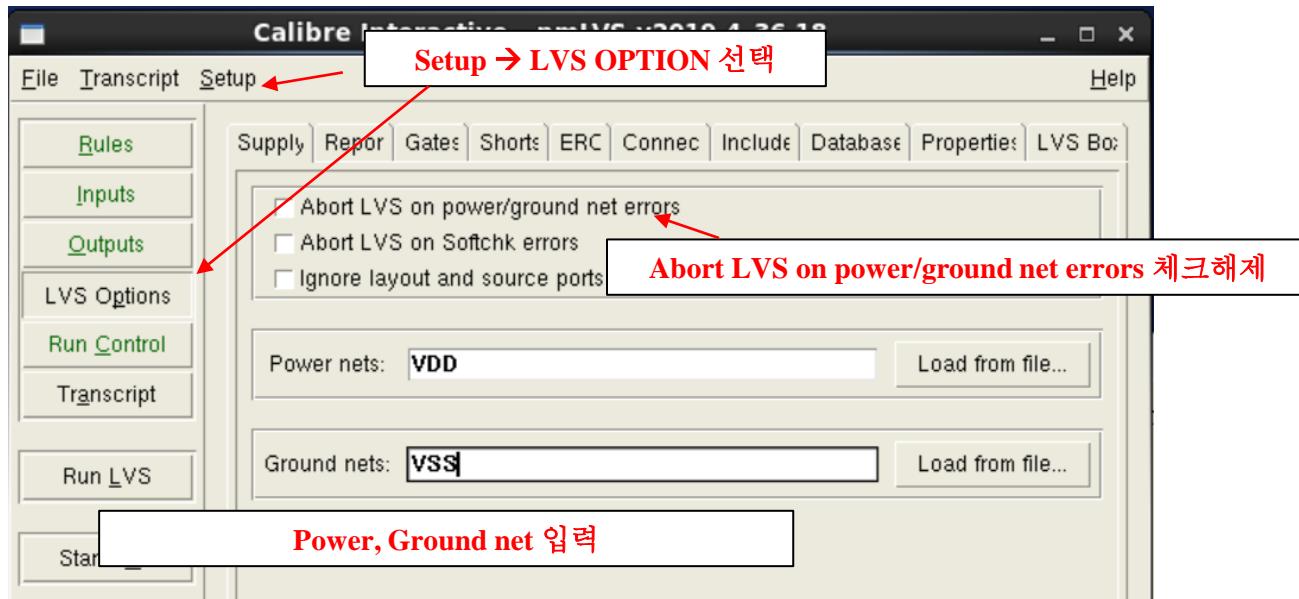
1) Calibre LVS 검토

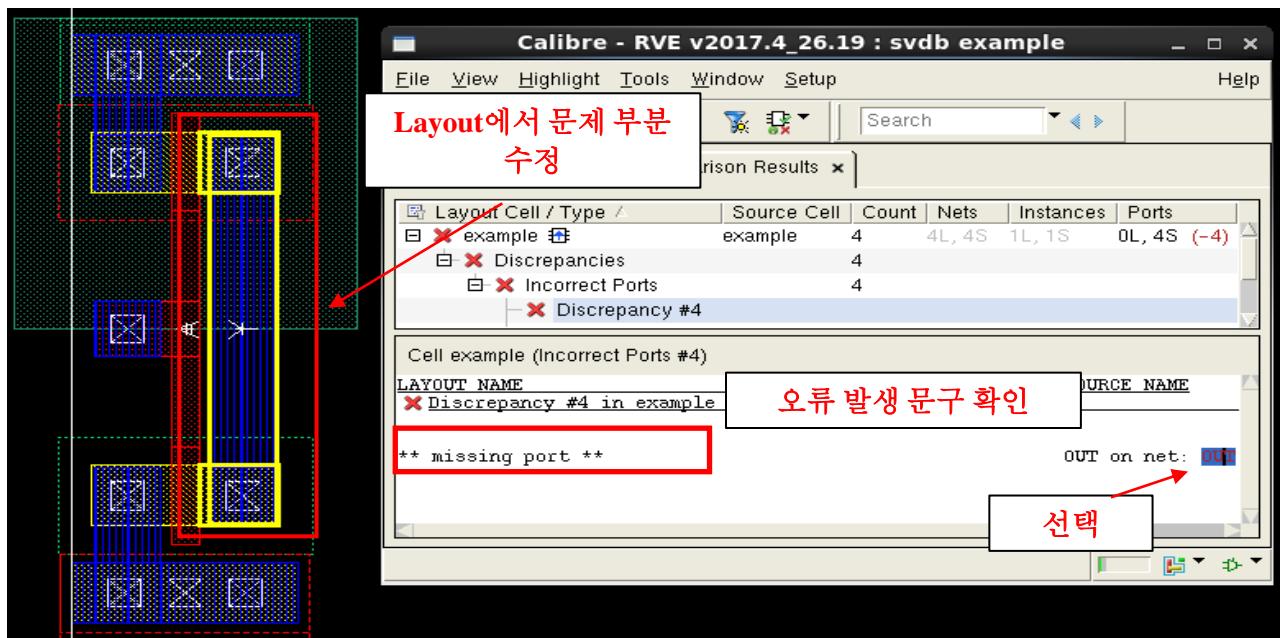
① LVS 검증 방법



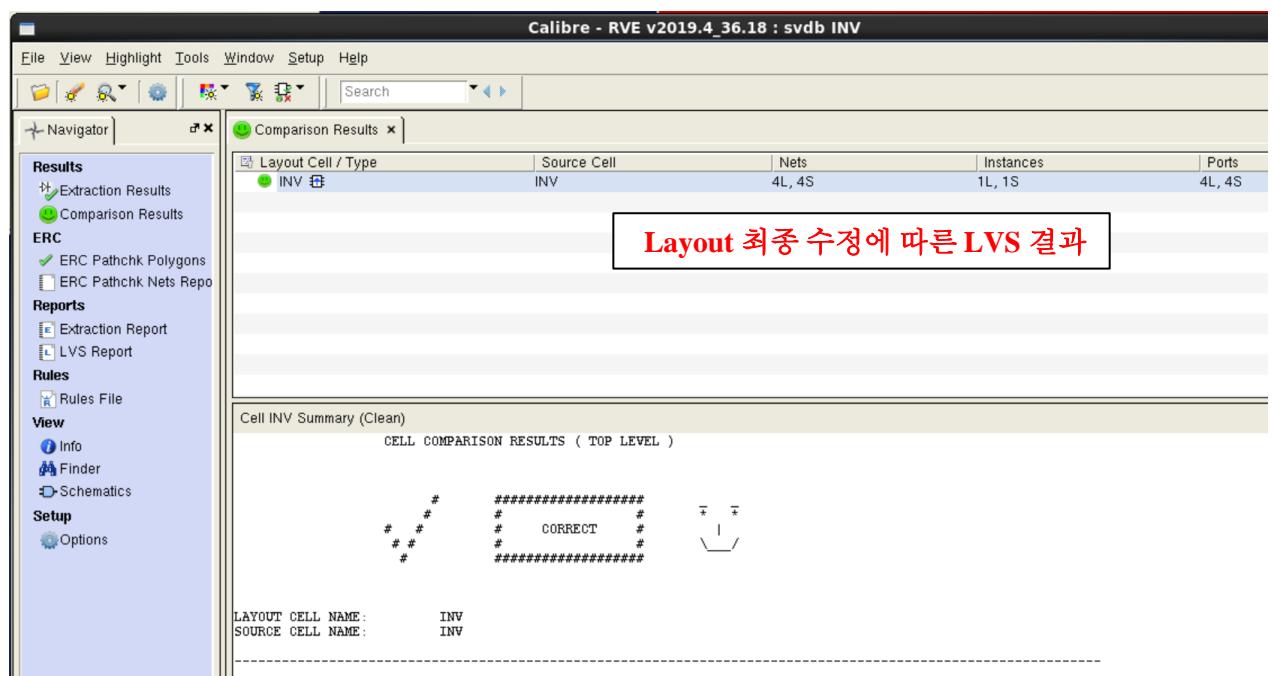






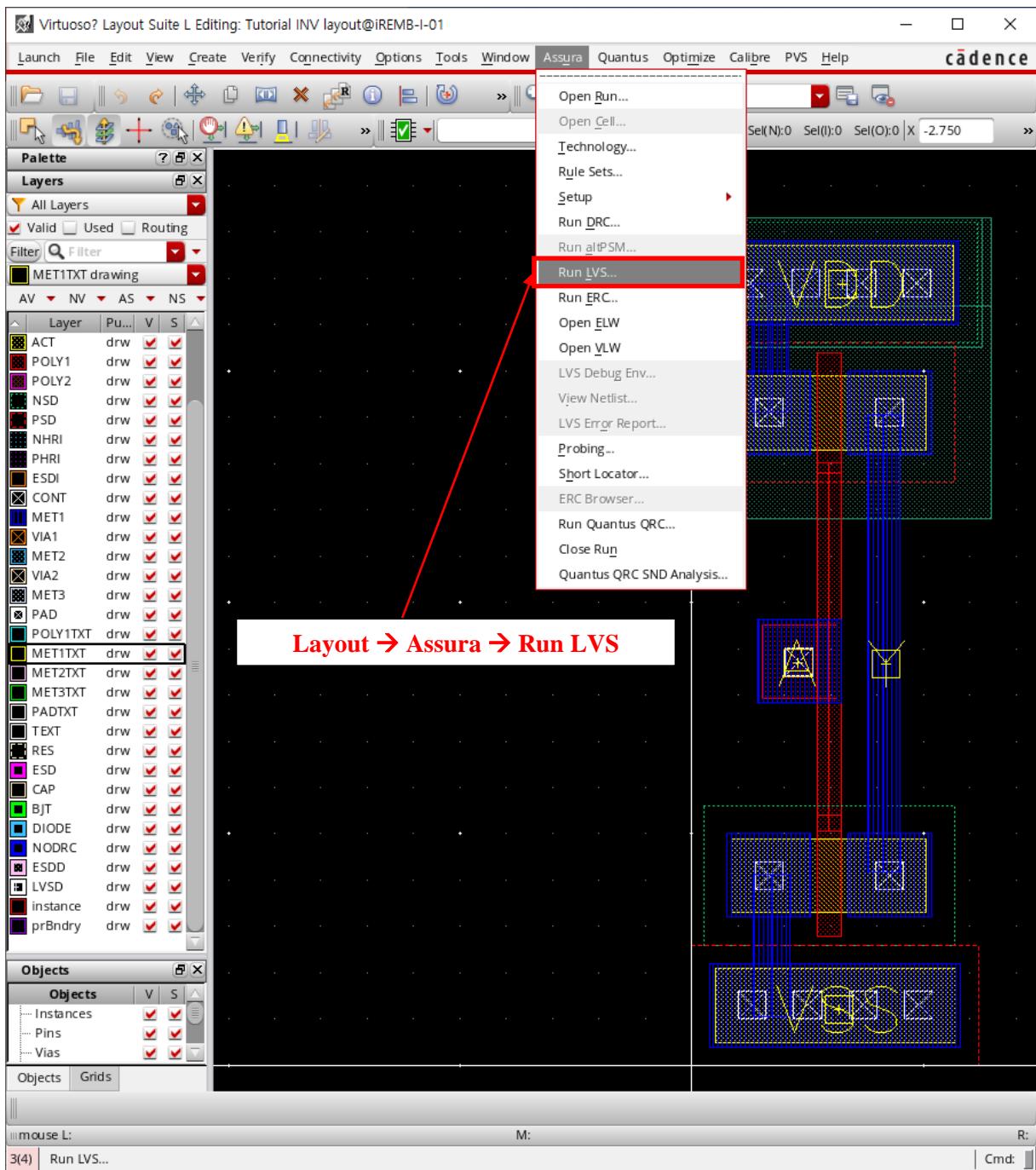


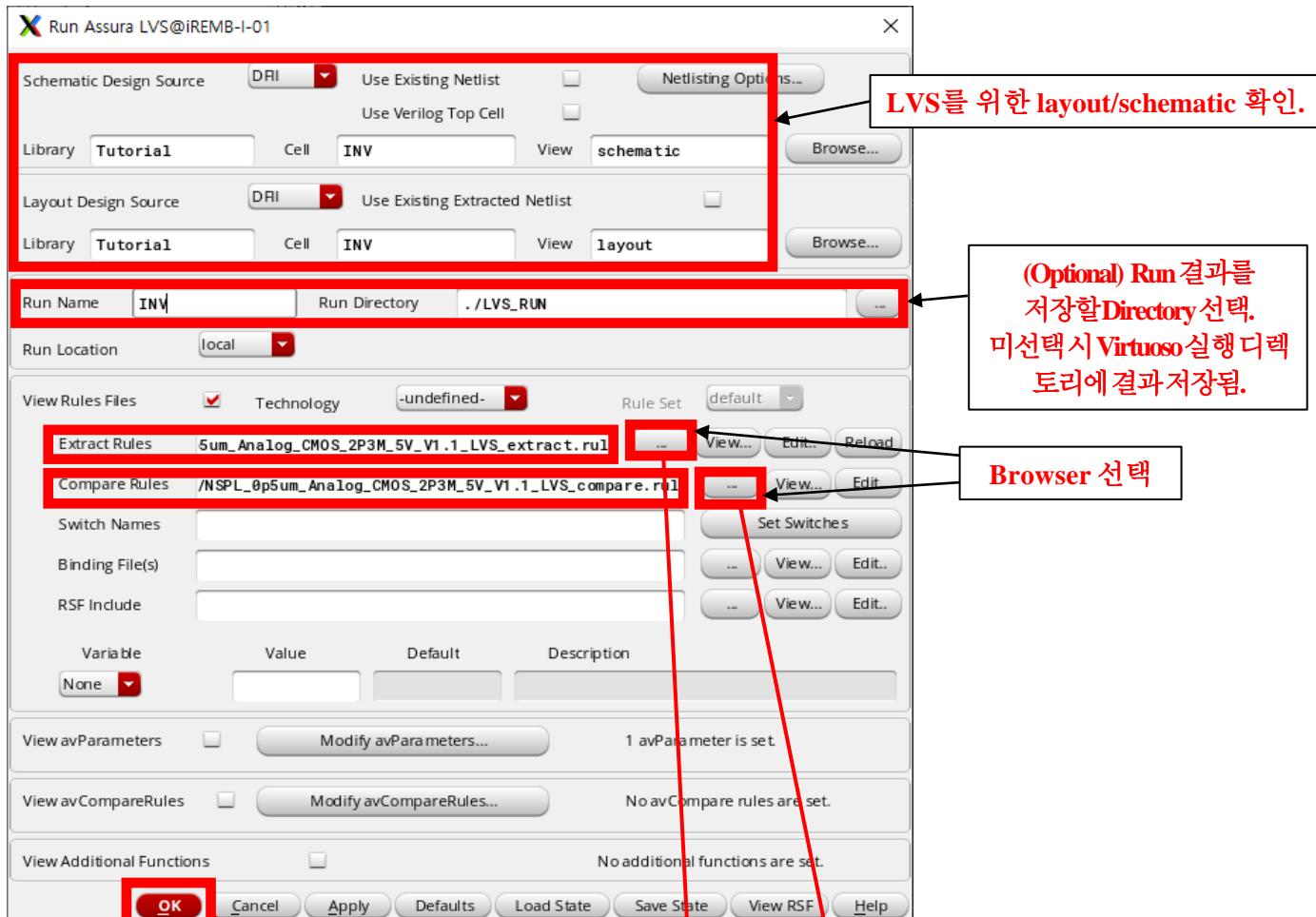
오류 사라질때까지 Layout 수정 및 LVS 반복



2) Assura LVS 검토

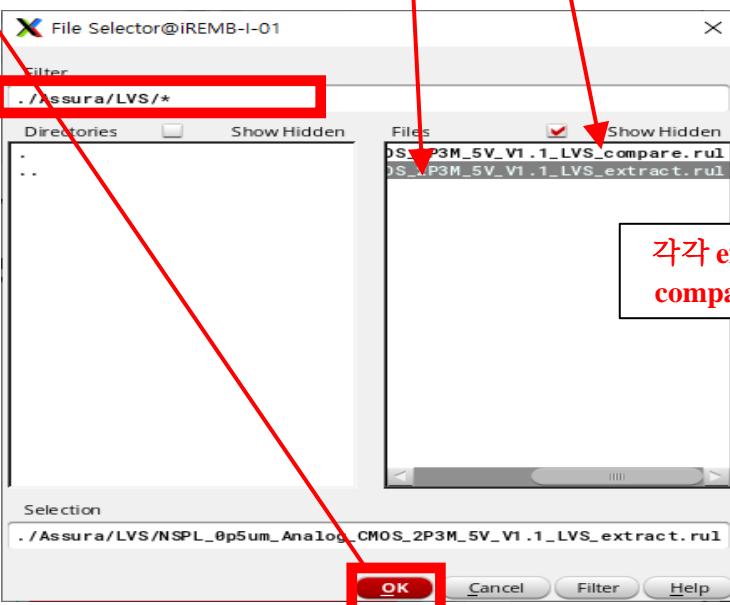
① LVS 검증 방법

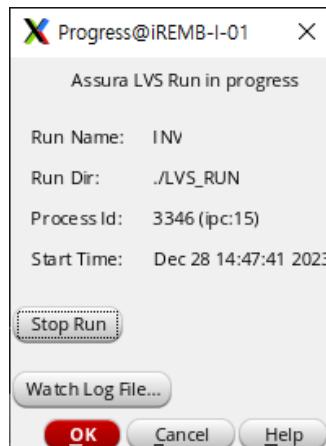




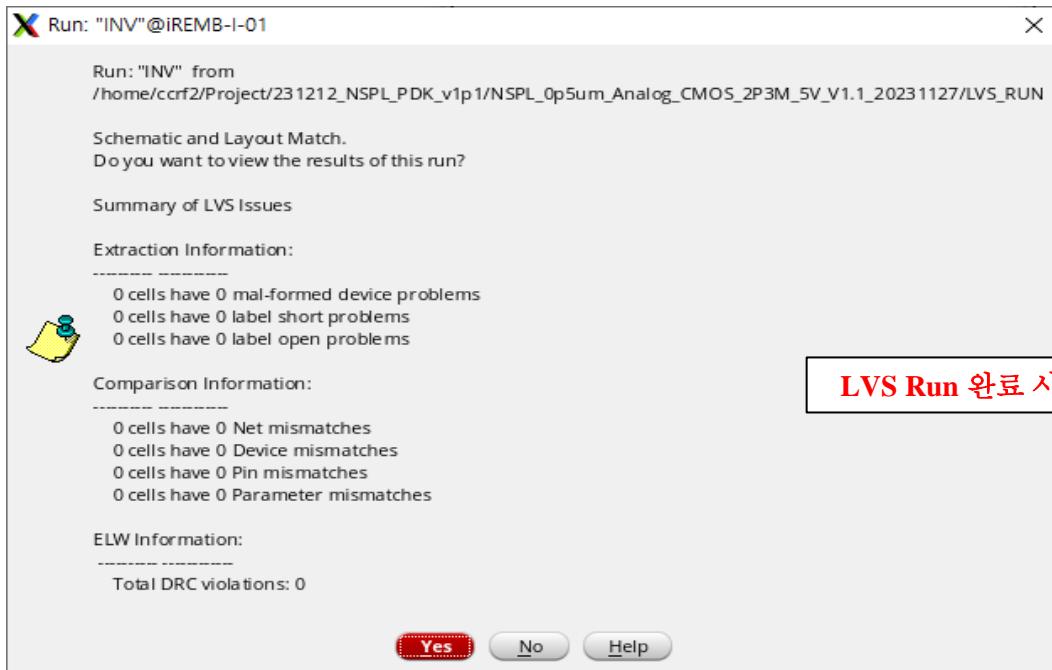
Run LVS 진행

LVS Rule File이 있는 경로로 이동.

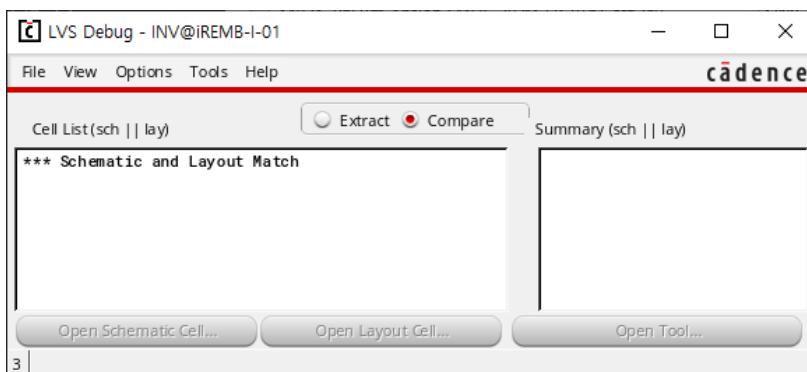




LVS Run Progress 화면.
(Run 완료 후 자동으로 화면 사라짐)



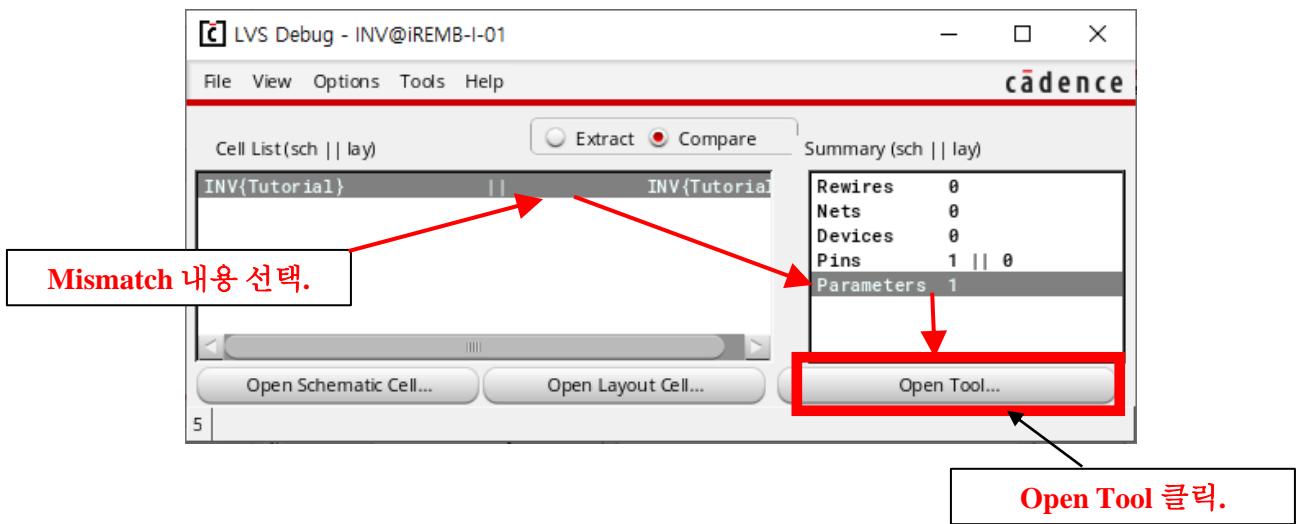
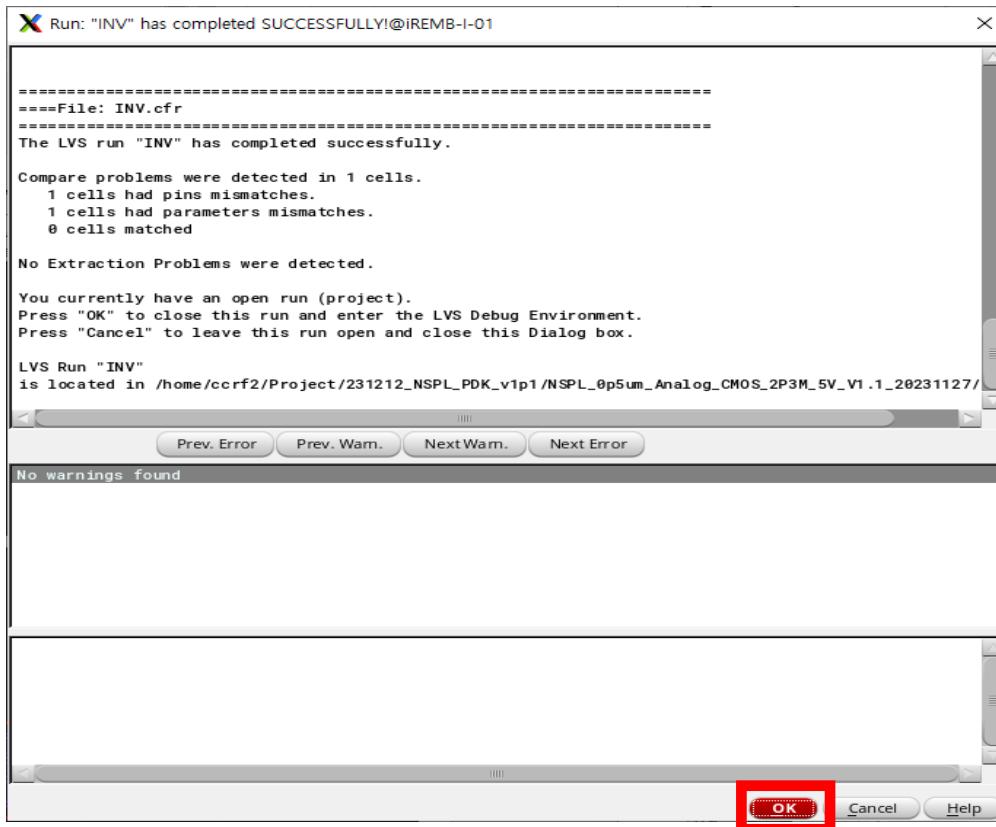
LVS Run 완료 시, dialog box.

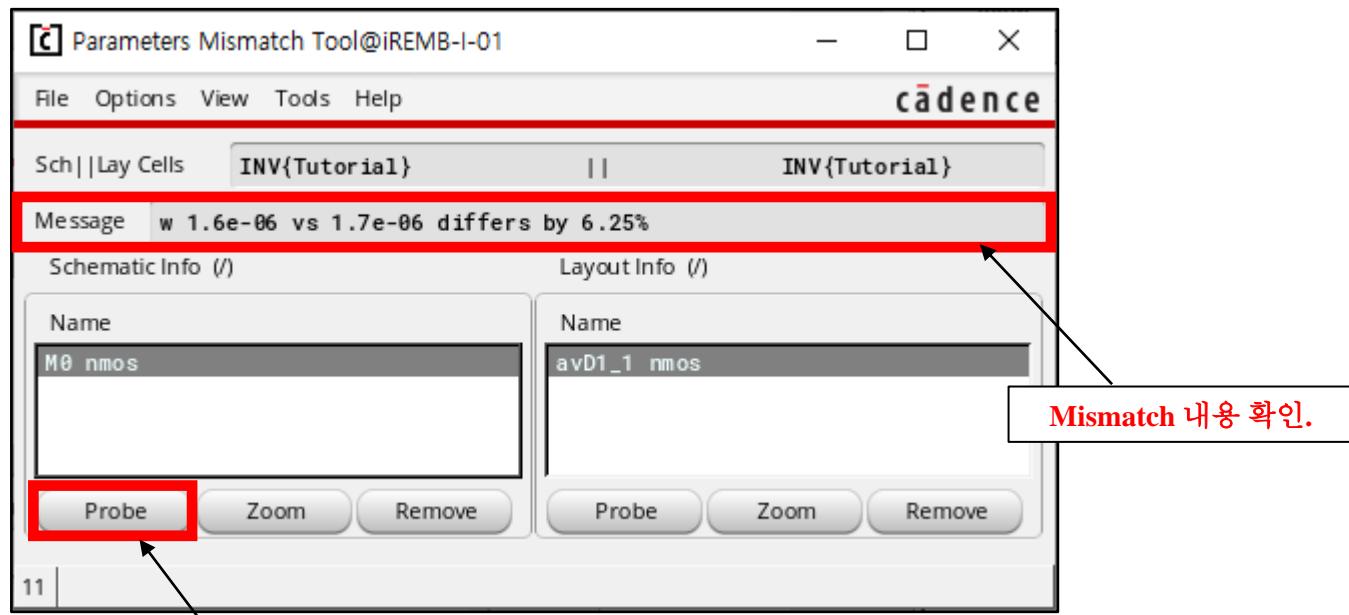


LVS pass

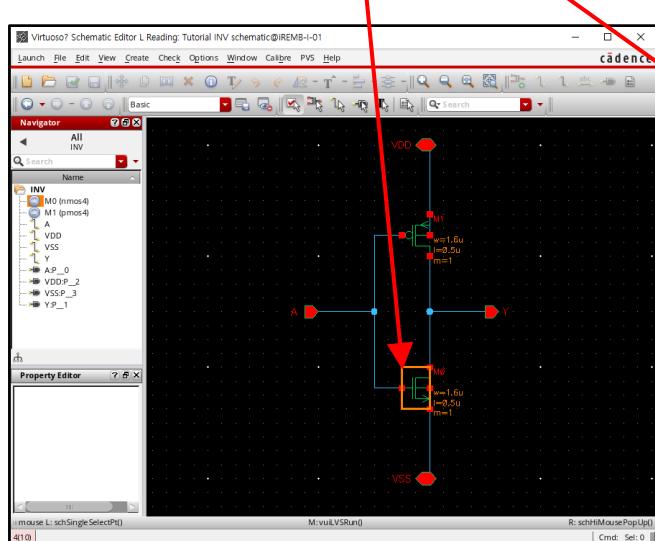
② LVS Debug

LVS mismatch 발생. 예) pin 및 parameter mismatch 발생.

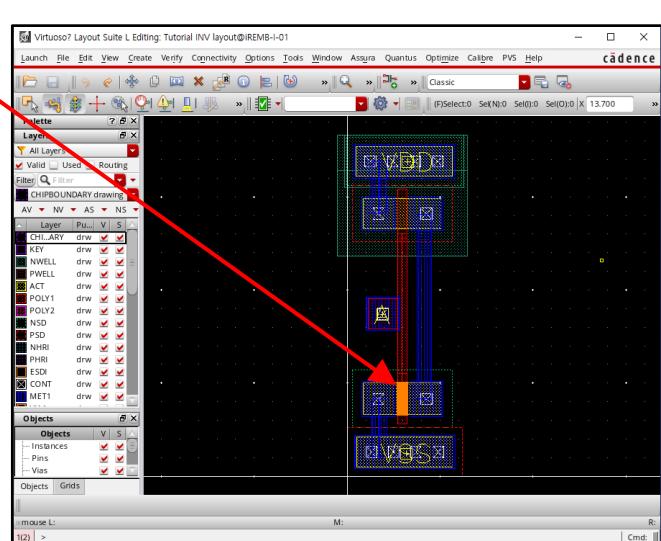




Probe 클릭하여, schematic 및 layout에서 해당 mismatch 부분을 highlight.



< Schematic >



< Layout >

오류 사라질때까지 Layout 설정 및 LVS 반복

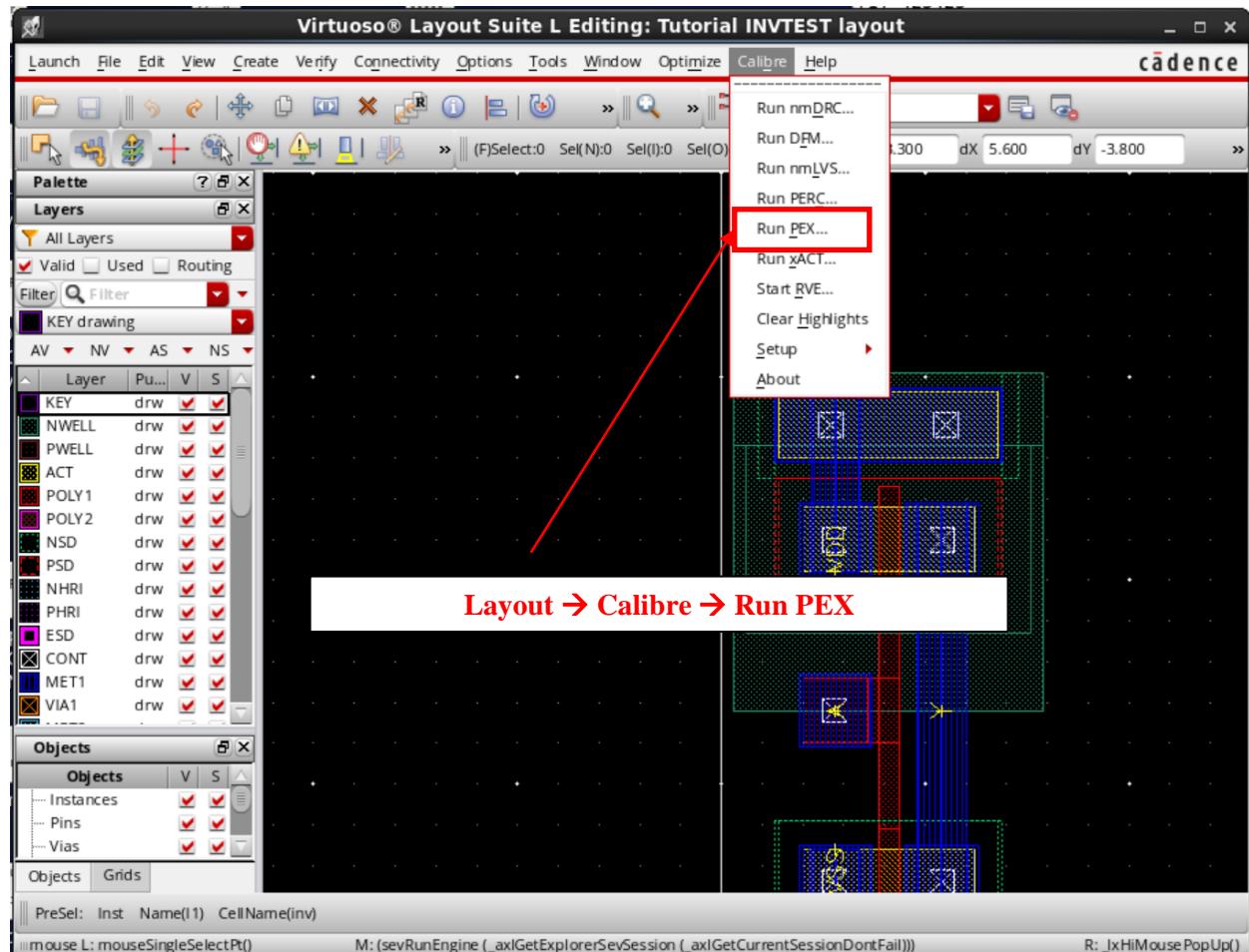
7. PEX (Parasitic EXtraction)

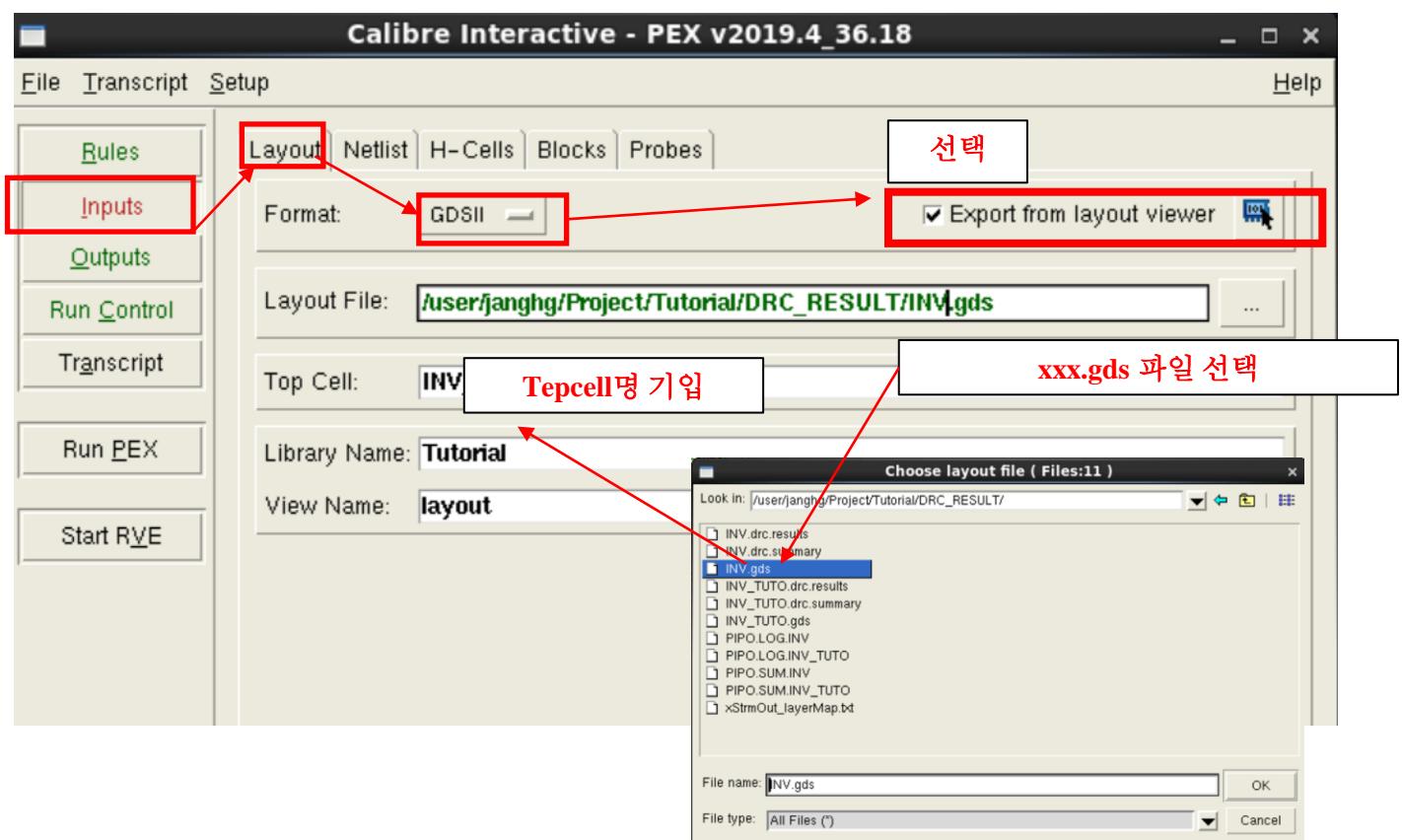
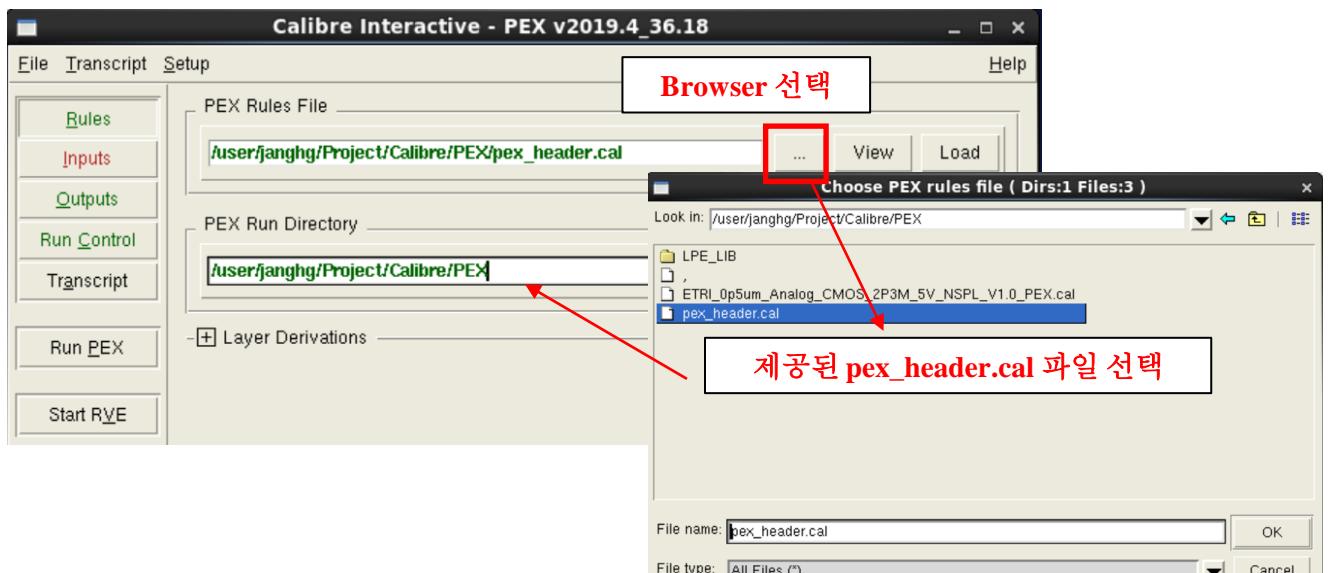
7. PEX

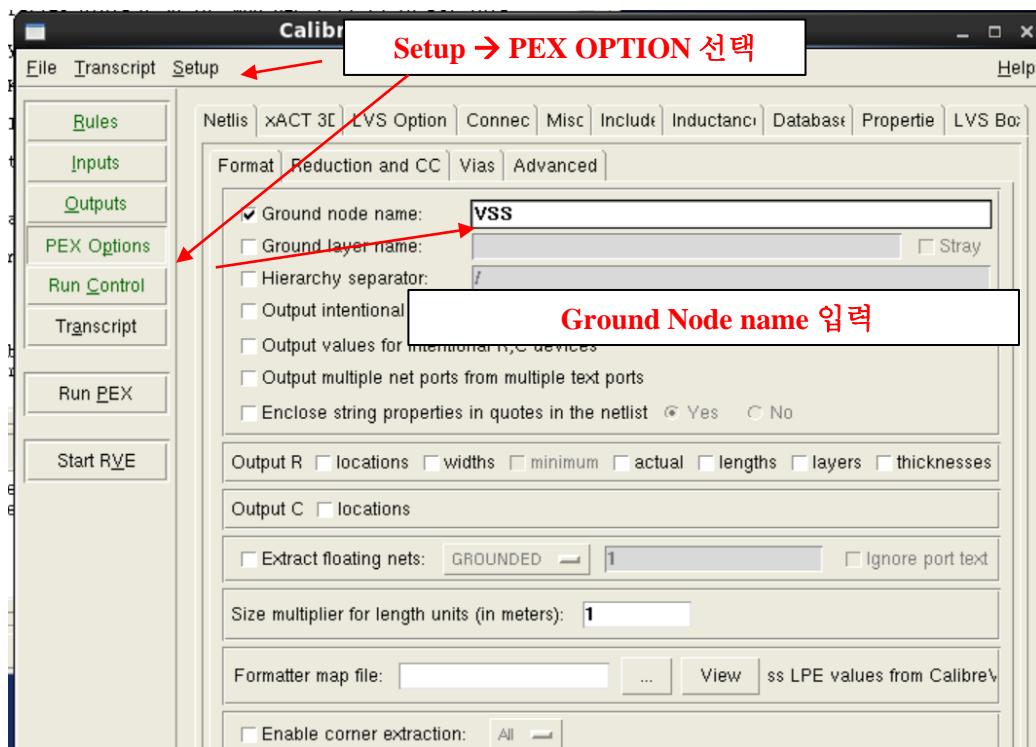
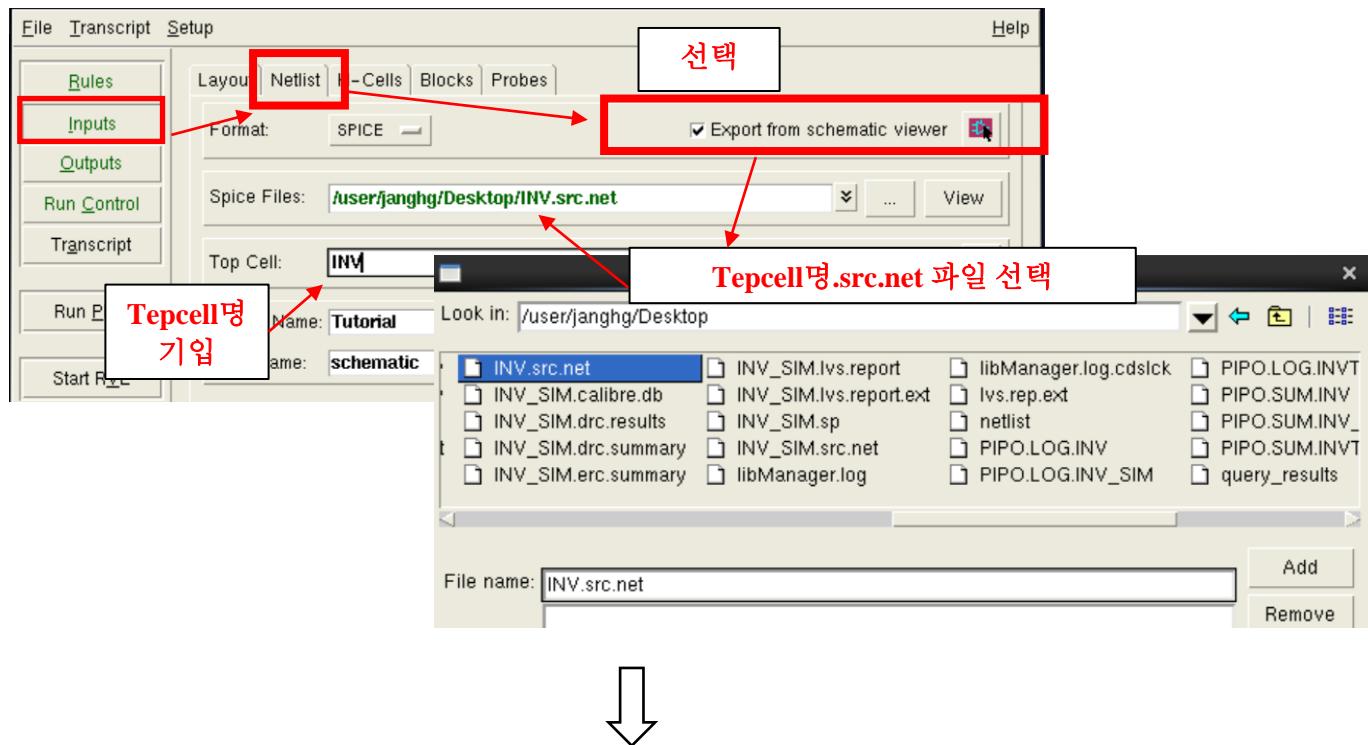
- 목적 : Parasitic 성분 추출

1) PEX 검토

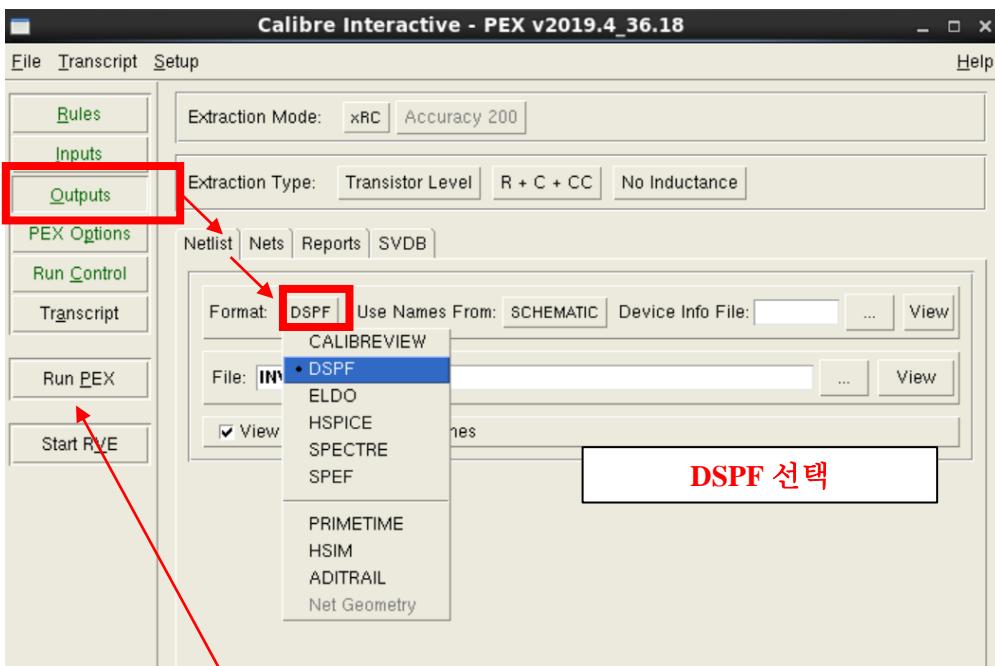
① PEX 진행 방법

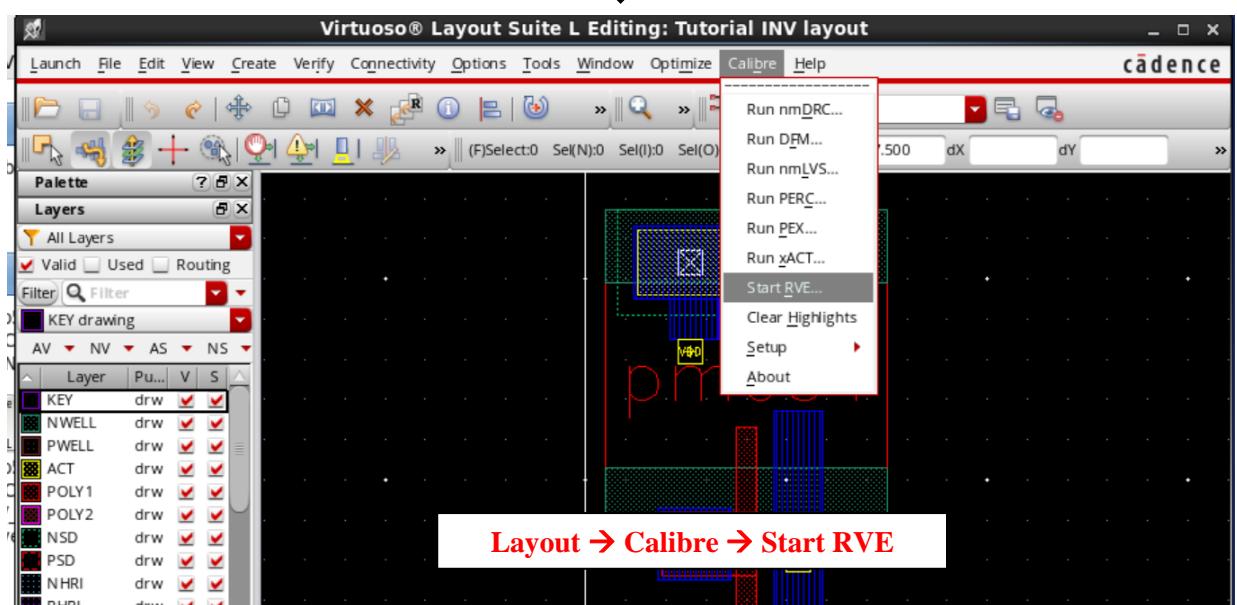
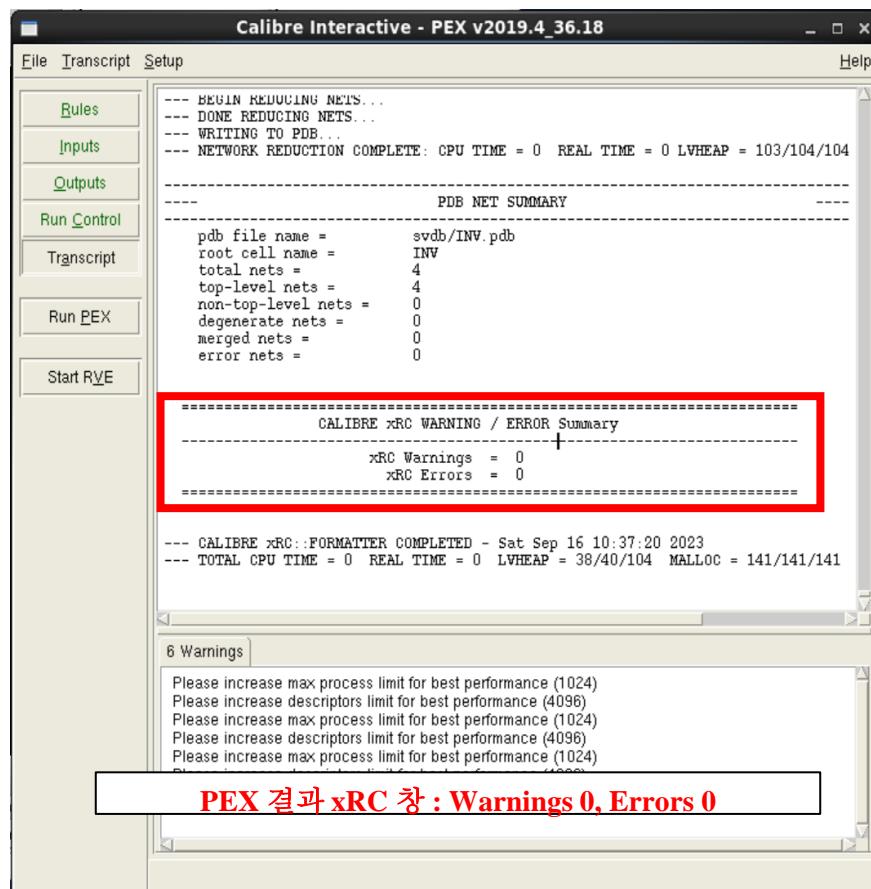


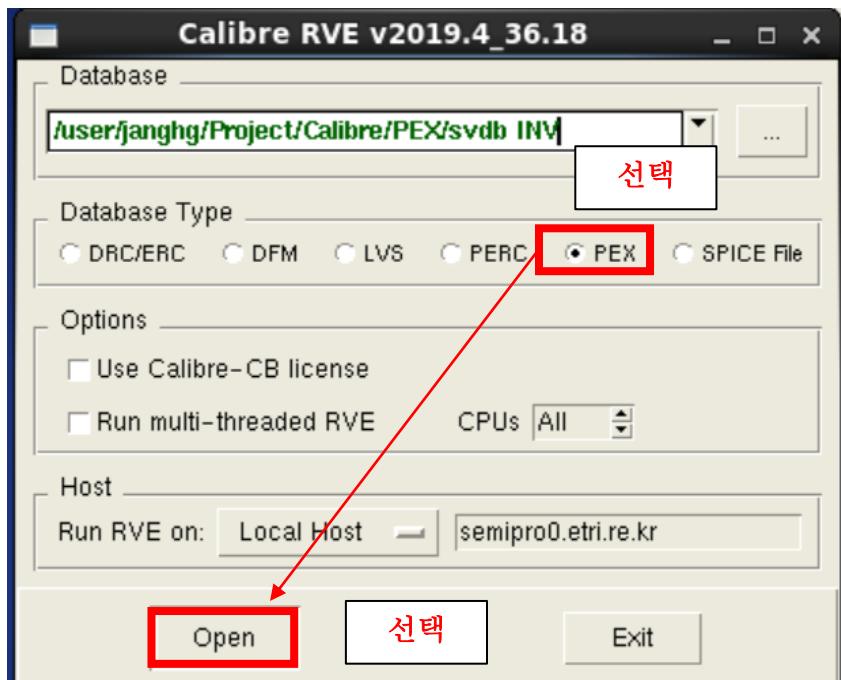




2) PEX-DSPF 방식



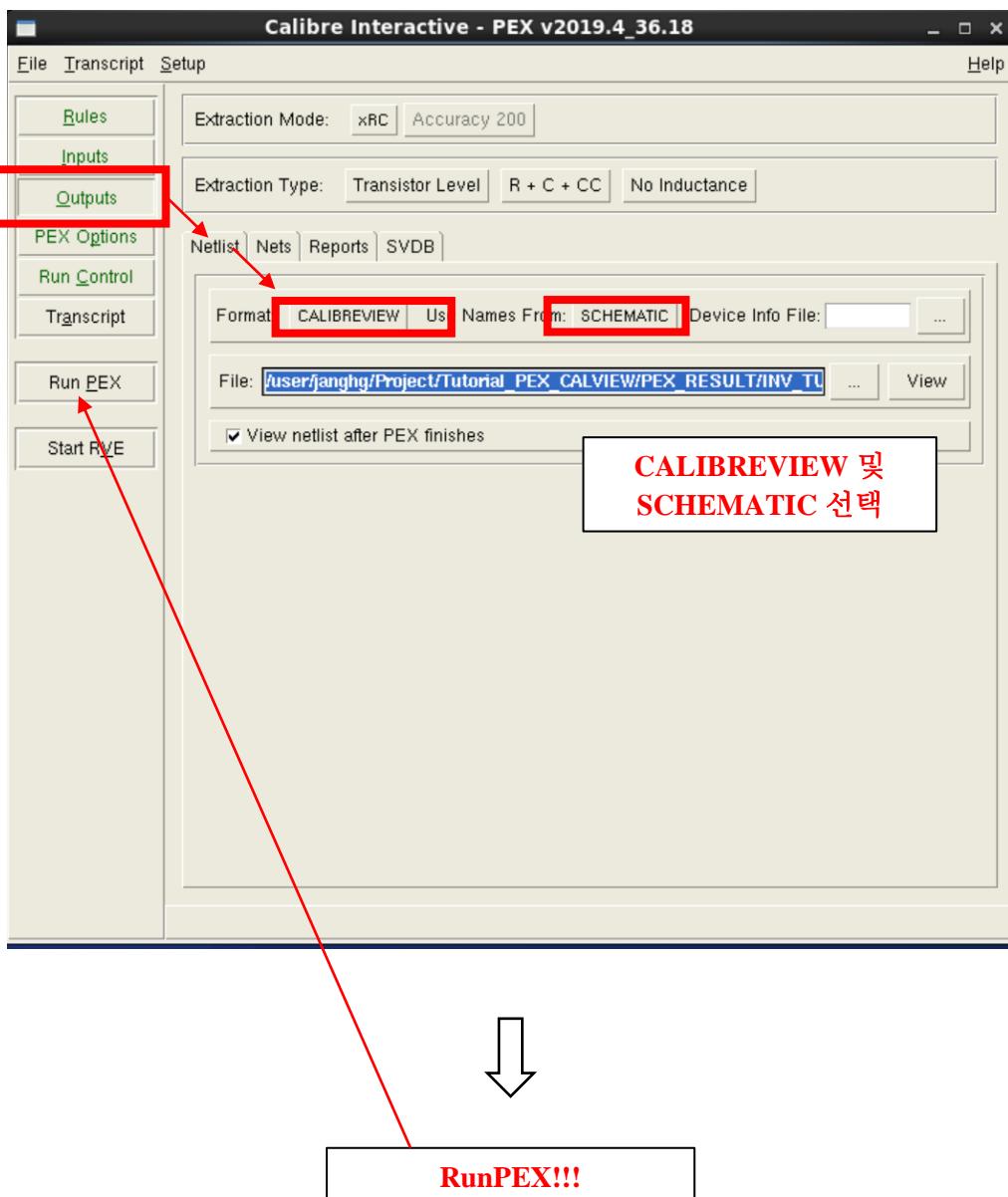


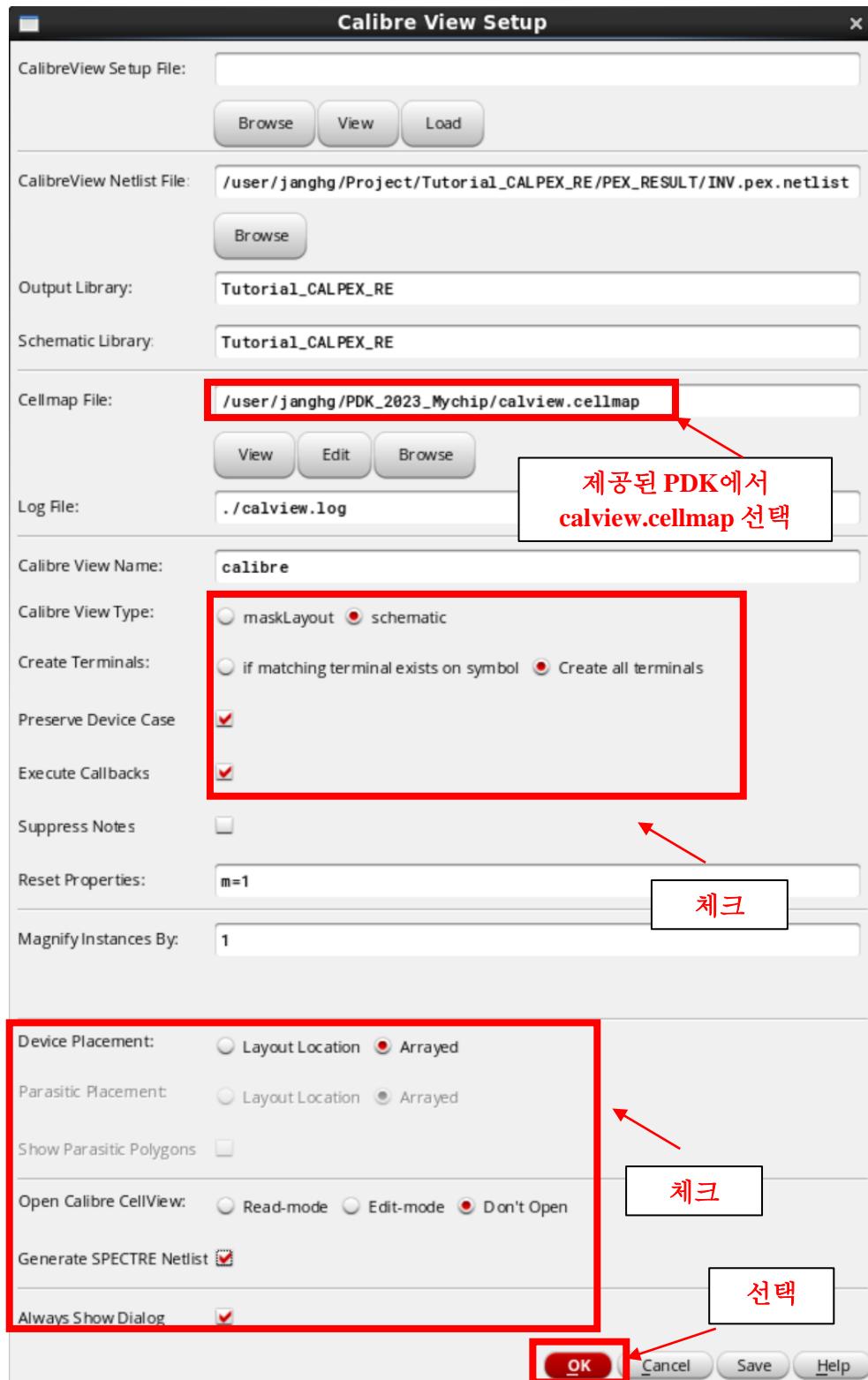


No.	Layout Net	R Count	C Total (F)	C+CC Total (F)
1	IN	15	1.62089E-15	1.62089E-15
2	VSS	8	4.45309E-14	4.45309E-14
3	VDD	7	4.44690E-14	4.44690E-14
4	OUT	8	2.42288E-14	2.42288E-14

A red box highlights the 'Results' section in the sidebar and the table in the central pane. A red box labeled '결과 출력' (Output Result) is overlaid on the bottom right of the central pane.

3) PEX-CALIBREVIEW 방식







```

c:/user/janghg/simulation/INV_TUTO/spectre/calibre/netlist -> x
File Edit View Help
                                         cadence

// Generated for: spectre
// Generated on: Oct 19 09:50:25 2023
// Design library name: Tutorial_CALPEX_RE
// Design cell name: INV_TUTO
// Design view name: calibre
simulator lang=spectre
global 0

// Library name: Tutorial_CALPEX_RE
// Cell name: INV_TUTO

MM1 (MM1_l MM1_g MM1_s MM1_b) nmos4 m=1 w=1.6e-06 l=5e-07
MM0 (MM0_d MM0_g MM0_m MM0_b) pmos4 m=1 w=1.6e-06 l=5e-07

cc_z0 (c_36_p MM1_g) capacitor c=8.74478e-19
cc_27 (c_26_n c_46_n) capacitor c=8.74478e-19
cc_26 (c_36_p c_46_n) capacitor c=1.15378e-16
cc_25 (c_40_p VSS) capacitor c=3.75809e-15
cc_24 (c_26_n VSS) capacitor c=7.17844e-19
cc_23 (c_36_p VSS) capacitor c=8.81661e-17
cc_22 (c_37_p VSS) capacitor c=2.33005e-16
cc_21 (c_36_p MM1_b) capacitor c=7.25193e-19
cc_20 (c_15_n c_46_n) capacitor c=8.72308e-19
cc_19 (MM0_s c_27_n) capacitor c=1.65126e-17
cc_18 (c_15_n c_27_n) capacitor c=8.74478e-19
cc_17 (VDD c_27_n) capacitor c=7.17844e-19
cc_16 (MM0_s c_29_n) capacitor c=8.74478e-19
cc_15 (c_15_n c_29_n) capacitor c=1.15378e-16
cc_14 (VDD c_29_n) capacitor c=8.79236e-17
cc_13 (MM0_b c_29_n) capacitor c=7.25193e-19
cc_12 (MM1_g MM1_s) capacitor c=3.51981e-17
cc_11 (A MM1_s) capacitor c=2.65446e-19
cc_10 (A c_46_n) capacitor c=4.1187e-17
cc_9 (A c_45_n) capacitor c=2.96264e-19
cc_8 (A c_28_n) capacitor c=7.89899e-17
cc_7 (MM0_g c_27_n) capacitor c=3.51981e-17
cc_6 (MM1_g c_26_n) capacitor c=3.51981e-17
cc_5 (MM0_g MM0_s) capacitor c=3.51981e-17
cc_4 (A MM0_s) capacitor c=2.65446e-19
cc_3 (A c_15_n) capacitor c=4.12889e-17
cc_2 (A VDD) capacitor c=2.95497e-19
cc_1 (A c_13_n) capacitor c=2.96264e-19
c1VSS_19 (MM1_b VSS) capacitor c=3.20851e-14
c1VSS_18 (c_45_n VSS) capacitor c=2.347e-16
c1VSS_17 (VSS_3 VSS) capacitor c=1.38282e-16
c1VSS_16 (VSS VSS) capacitor c=1.21307e-14
c1VSS_15 (c_46_n VSS) capacitor c=1.87226e-16
c1VSS_14 (MM1_s VSS) capacitor c=1.12232e-14
c1Y_28 (Y_2 VSS) capacitor c=1.11674e-16
c1Y_27 (Y_4 VSS) capacitor c=5.23929e-16
c1Y_26 (c_37_p VSS) capacitor c=1.15015e-15
c1Y_25 (Y VSS) capacitor c=1.13959e-15
c1Y_24 (c_36_p VSS) capacitor c=1.61822e-16
c1Y_23 (c_26_n VSS) capacitor c=1.12218e-14
c1Y_22 (c_29_n VSS) capacitor c=1.70118e-16
c1Y_21 (c_27_n VSS) capacitor c=1.11429e-14
c1Y_20 (c_28_n VSS) capacitor c=1.72679e-16
c1Y_19 (c_49_p VSS) capacitor c=9.69942e-16
c1VDD_17 (MM0_b VSS) capacitor c=3.20822e-14
c1VDD_16 (c_13_n VSS) capacitor c=3.72902e-16
c1VDD_15 (VDD VSS) capacitor c=3.73789e-16
c1VDD_14 (c_15_n VSS) capacitor c=1.78127e-16
c1VDD_13 (MM0_s VSS) capacitor c=1.11444e-14
c1A_18 (A_8 VSS) capacitor c=1.47512e-16
c1A_17 (A_13 VSS) capacitor c=1.47512e-16
c1A_16 (A_28 VSS) capacitor c=3.49264e-16
c1A_15 (A_23 VSS) capacitor c=9.44456e-17
c1A_14 (A VSS) capacitor c=2.88242e-16
c1A_13 (MM1_g VSS) capacitor c=1.88888e-16
c1A_12 (MM0_g VSS) capacitor c=1.88888e-16

rVSS_20 (c_45_n VSS_3) resistor r=0.0666667
rVSS_25 (c_45_n VSS_14) resistor r=0.0264734
rVSS_24 (VSS_3 c_46_n) resistor r=0.0489997
rVSS_23 (VSS_5 VSS) resistor r=0.0177778
rVSS_22 (VSS_5 VSS_14) resistor r=0.0205904
rVSS_21 (c_46_n VSS_18) resistor r=20.8333
rVSS_20 (VSS_18 MM1_s) resistor r=42.6562
rY_43 (Y_1 Y_2) resistor r=0.0533333

```

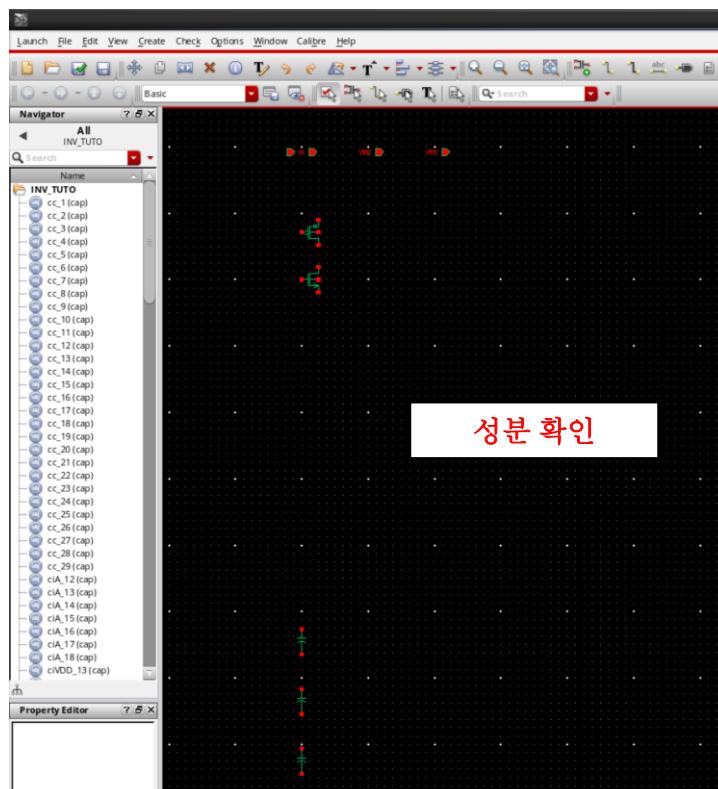
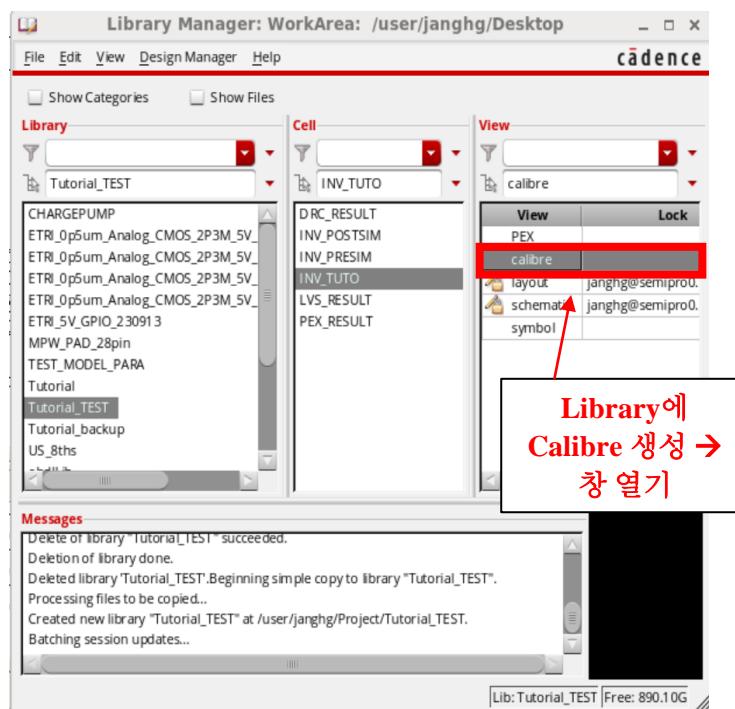
MOS

소자 및 기생 성분 포함 정보 팝업

기생 C

기생 R

4 L1 C1



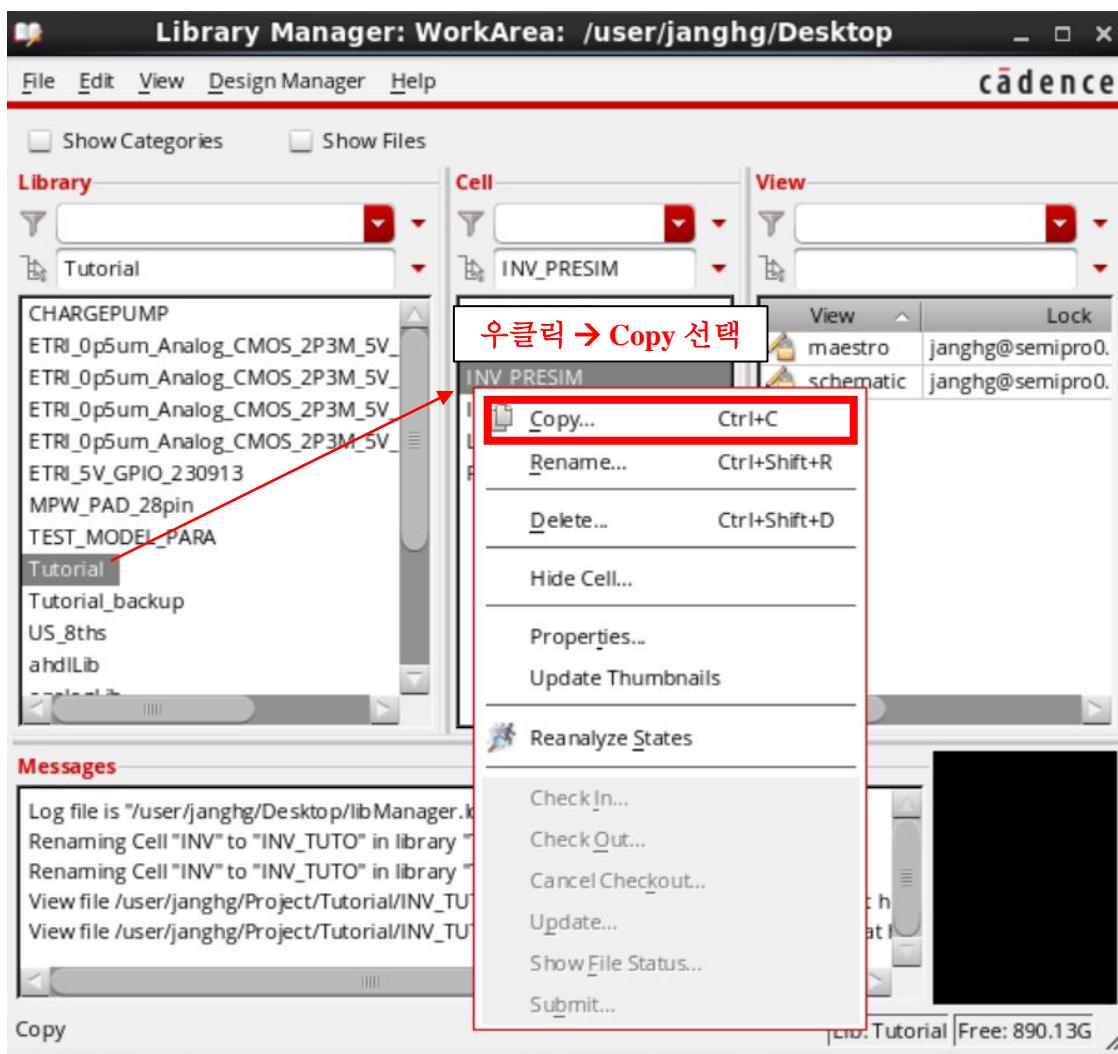
8. 회로 설계 및 검증 (Post-simulation)

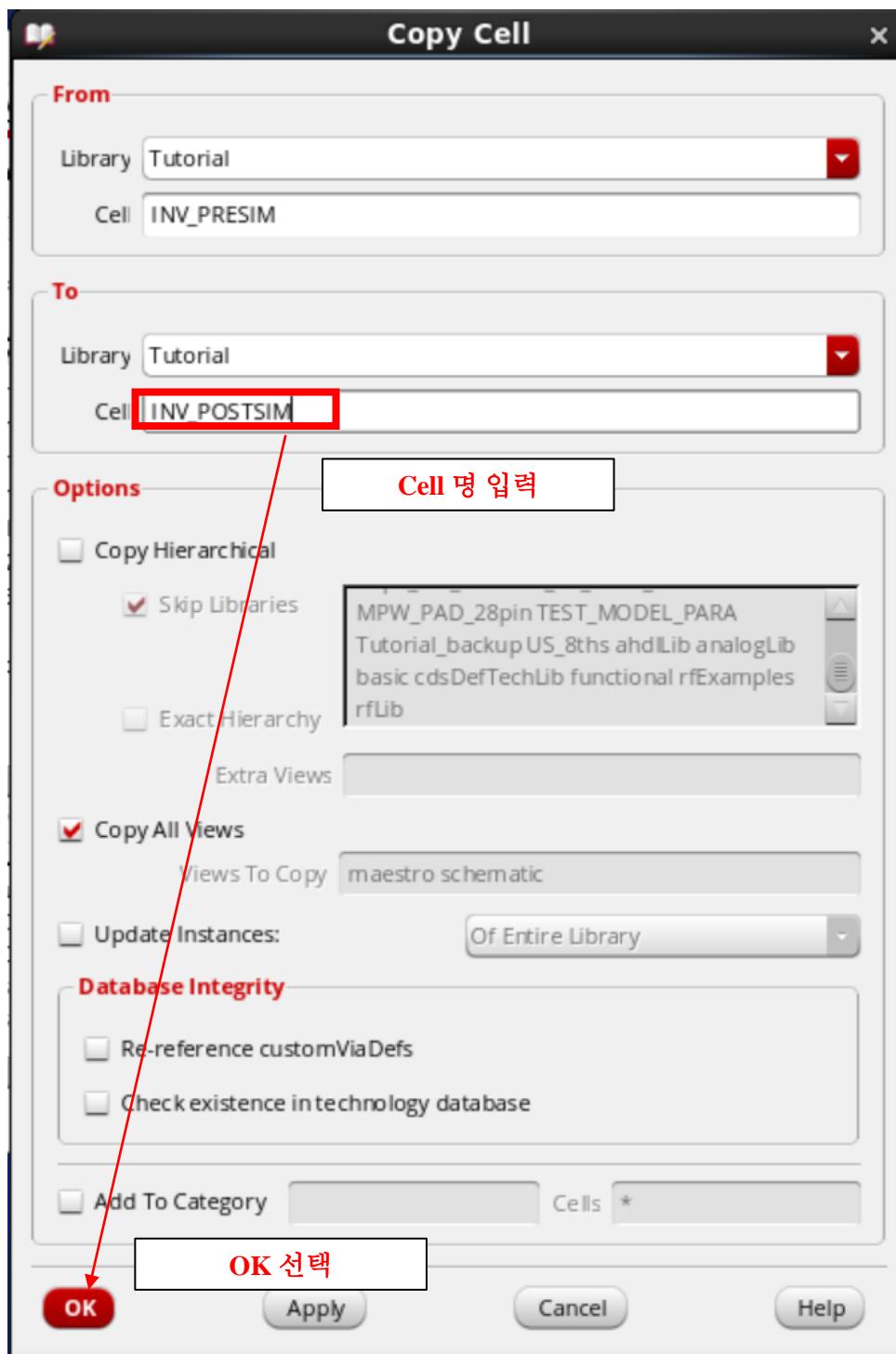
8. 회로 설계 및 검증 (Post-simulation)

- 목적 : Parasitic 성분 반영한 시뮬레이션을 통해 Pre-sim.과 결과 비교

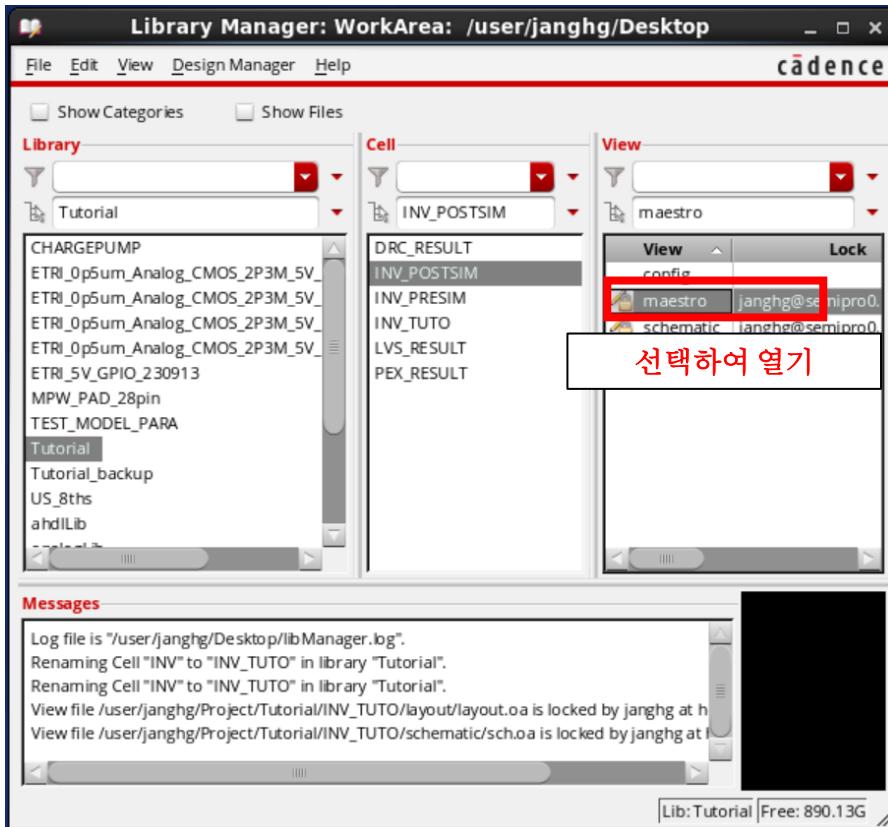
1) Post-simulation

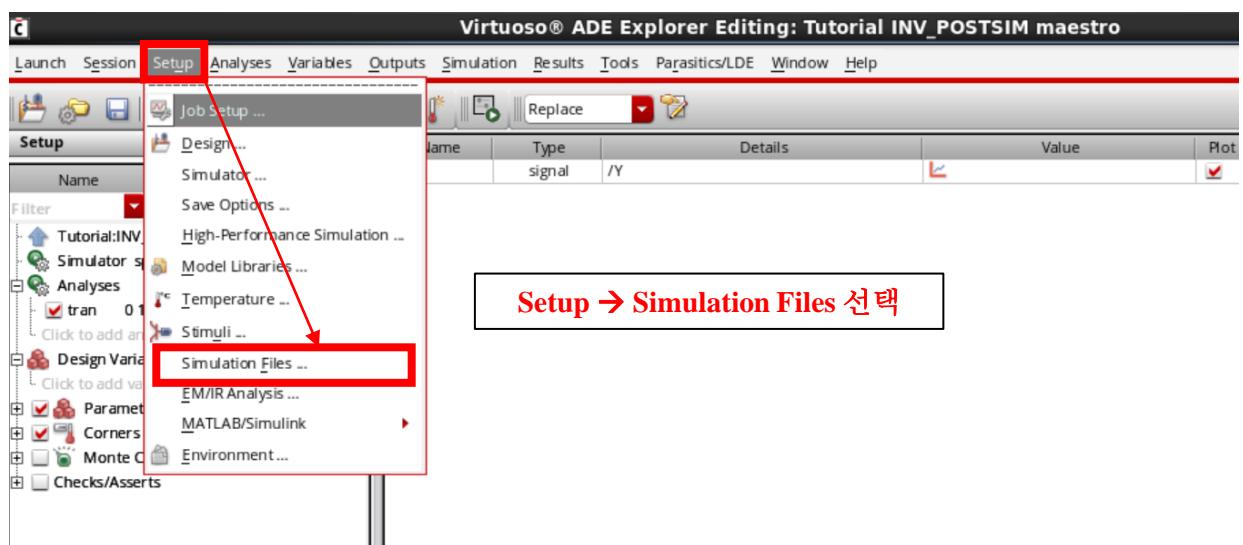
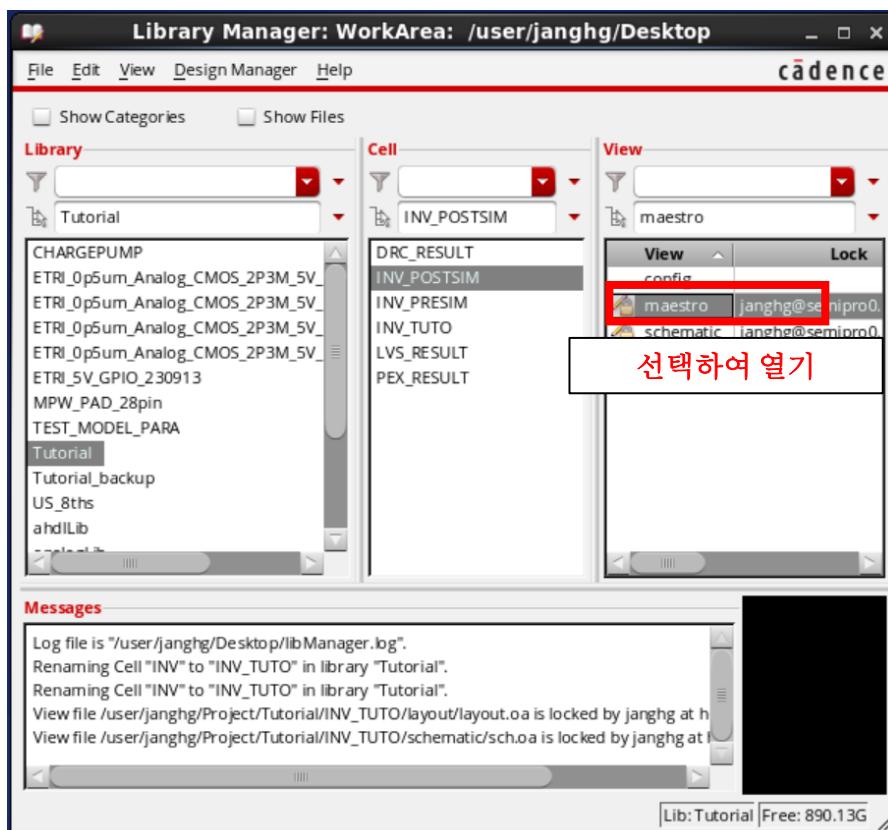
① Schematic 설계 프로그램 실행

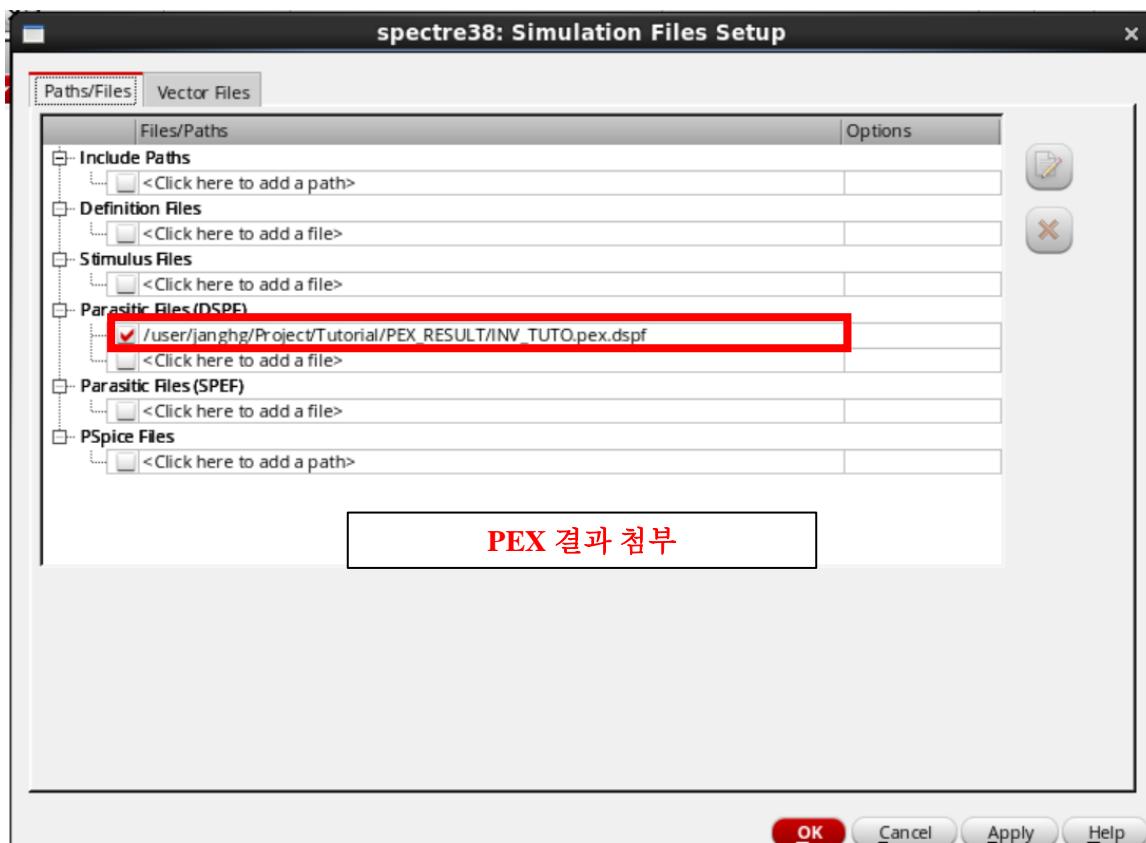




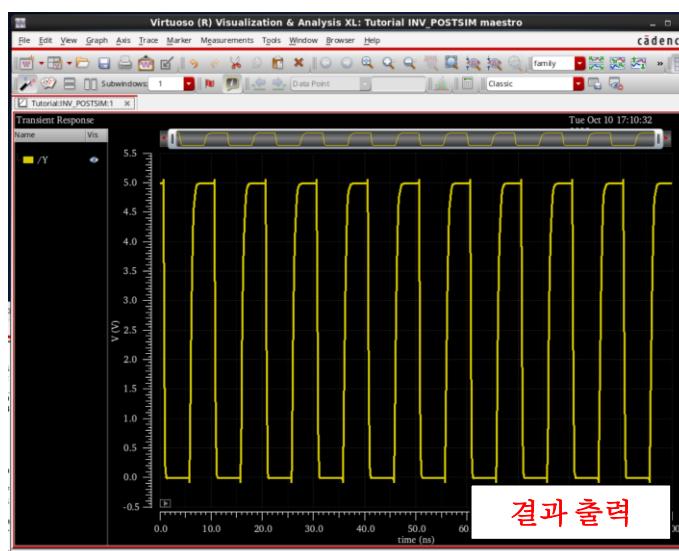
2) Post-simulation-DSPF 방식



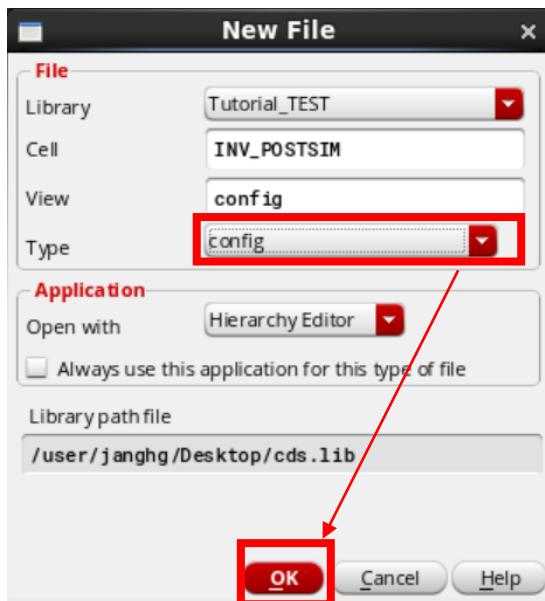
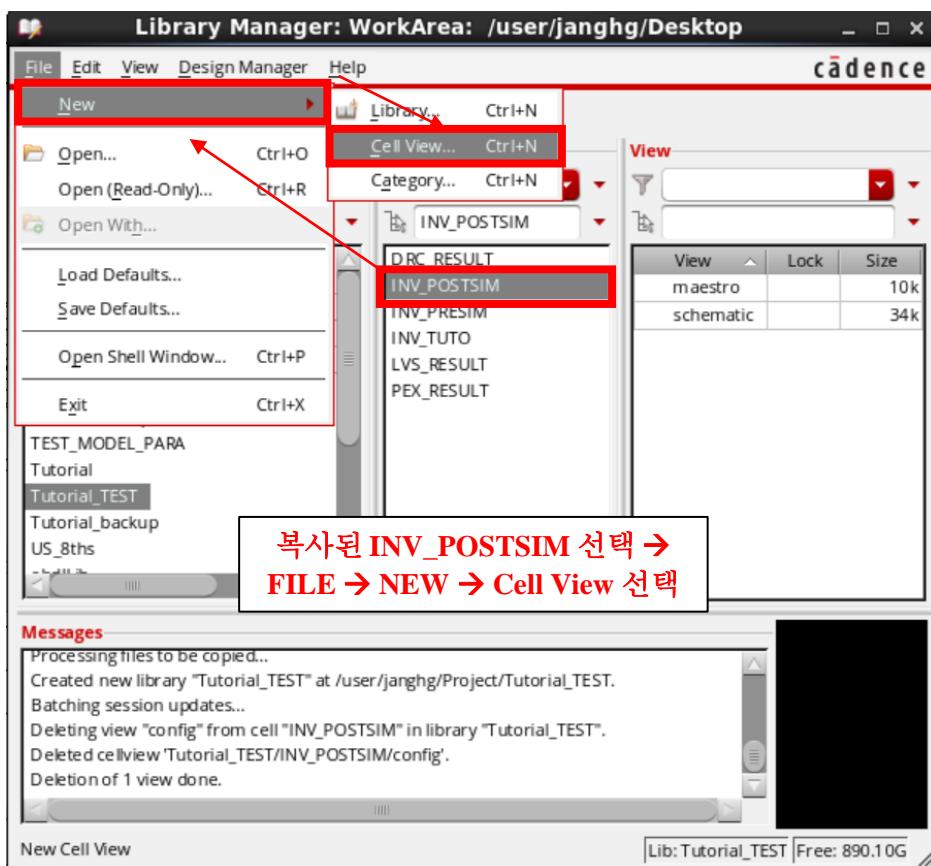




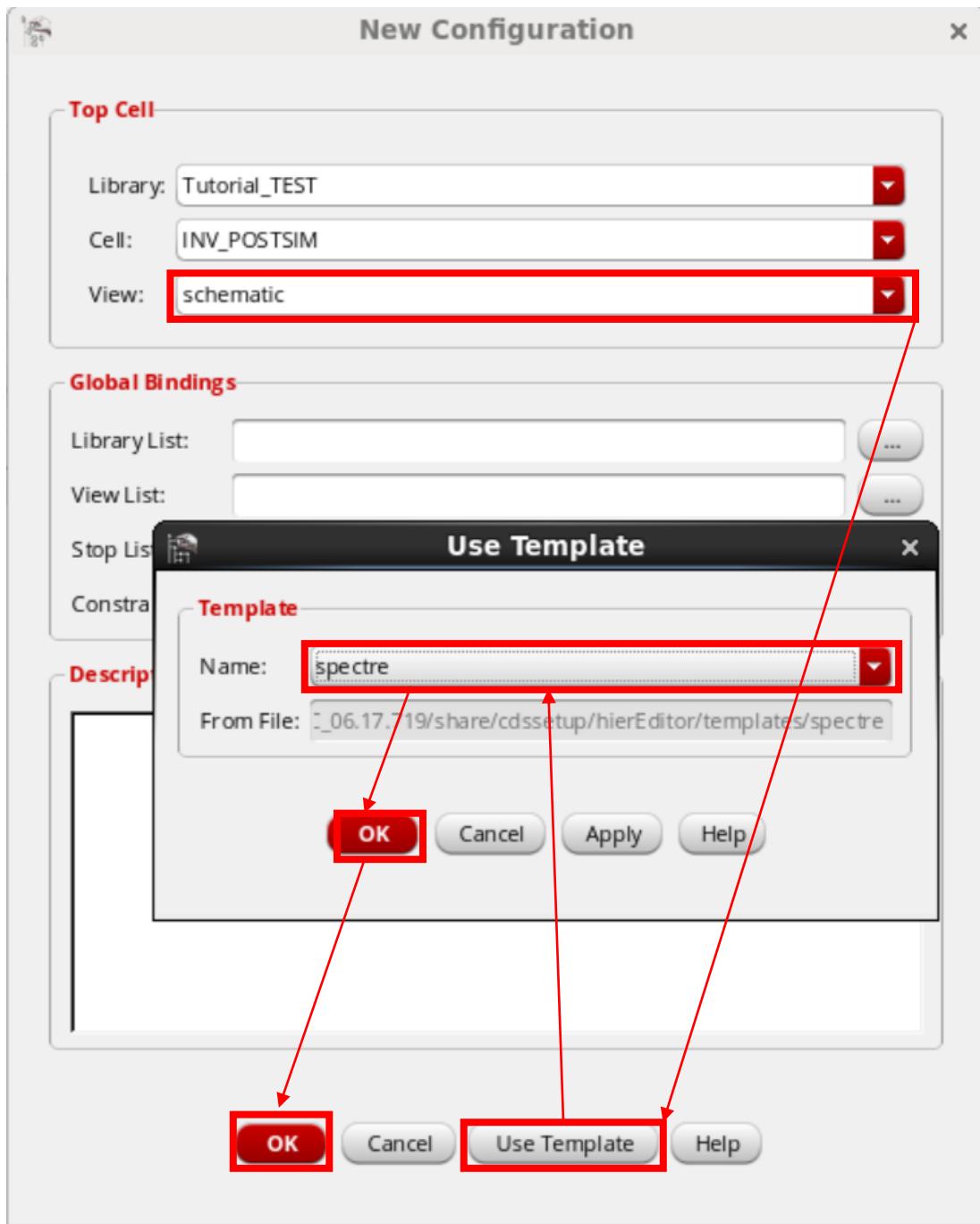
Run Simulation!!!



3) Post-simulation-Calibre 방식



Type에서 Config 선택
→ OK 클릭

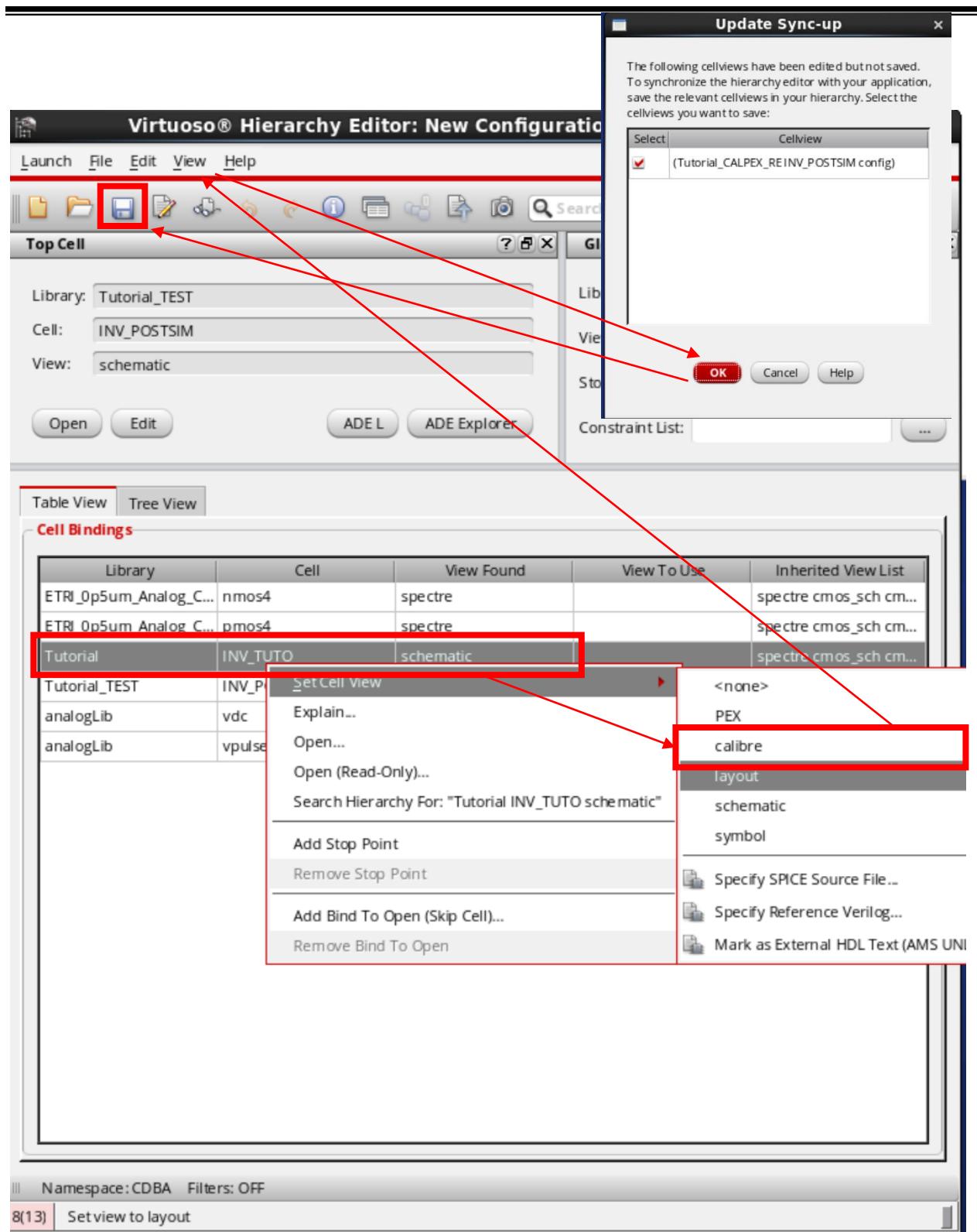


Top Cell / VIEW에서 Schematic 선택

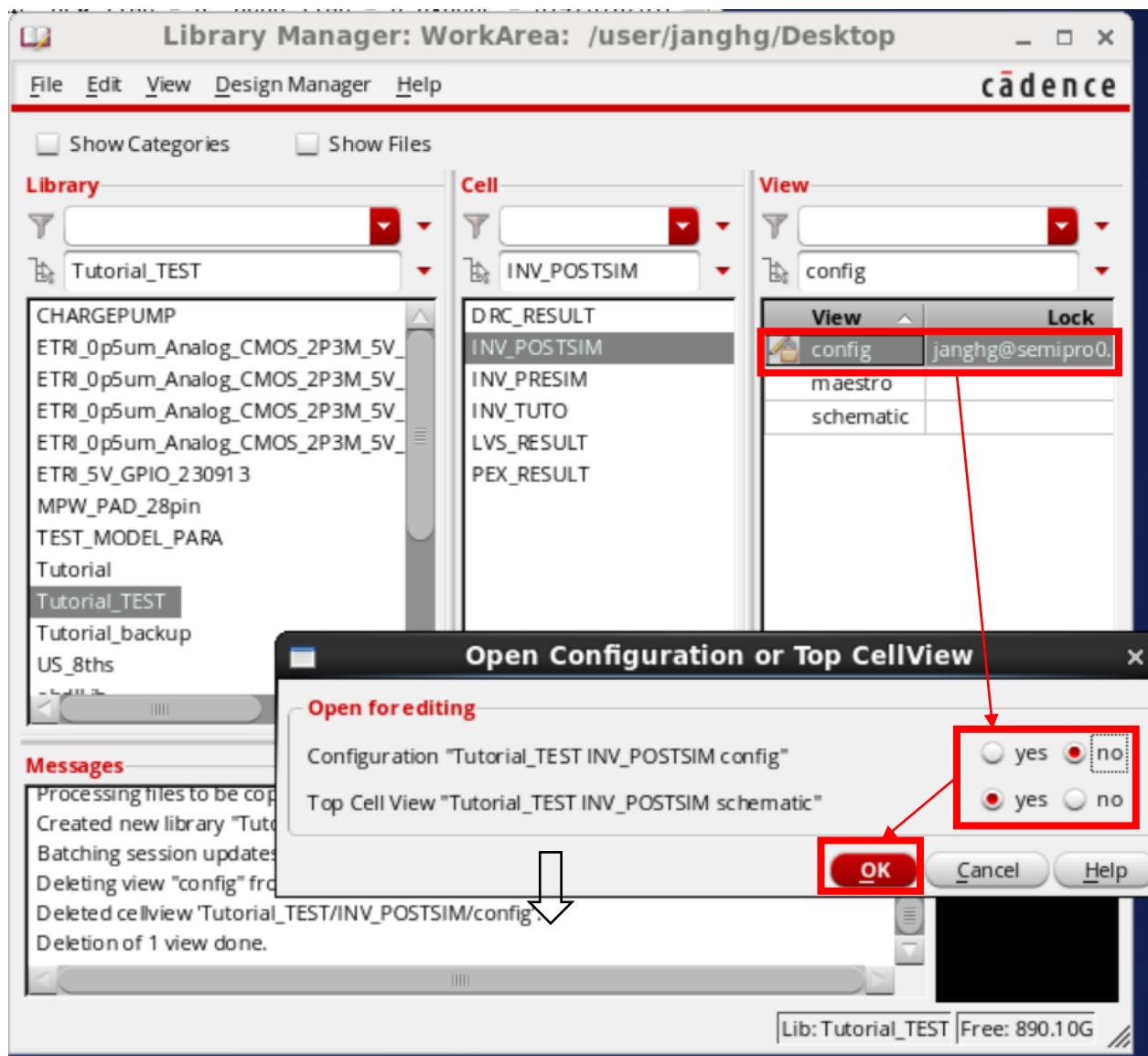
→ Use Template 선택

→ Tempalate / name에서 Spectre 선택

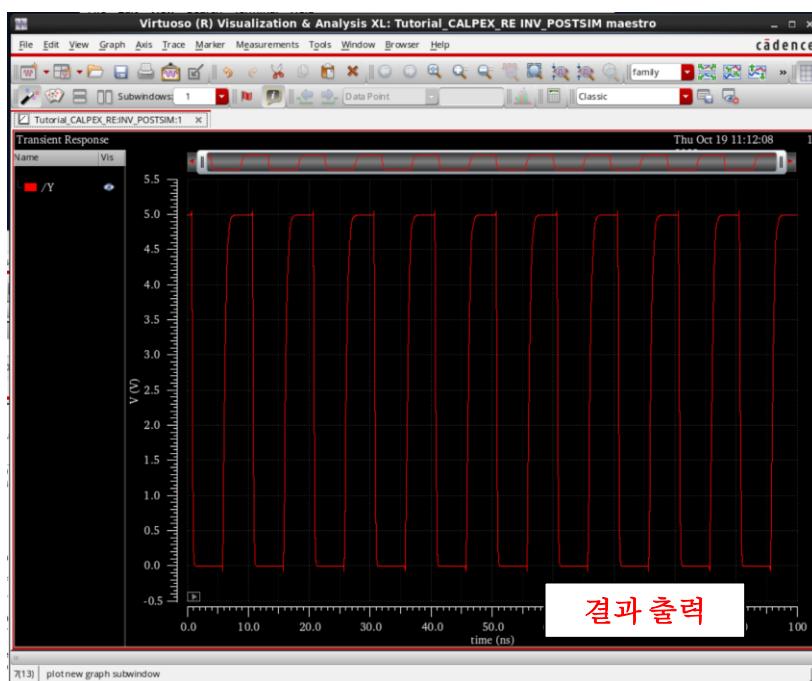
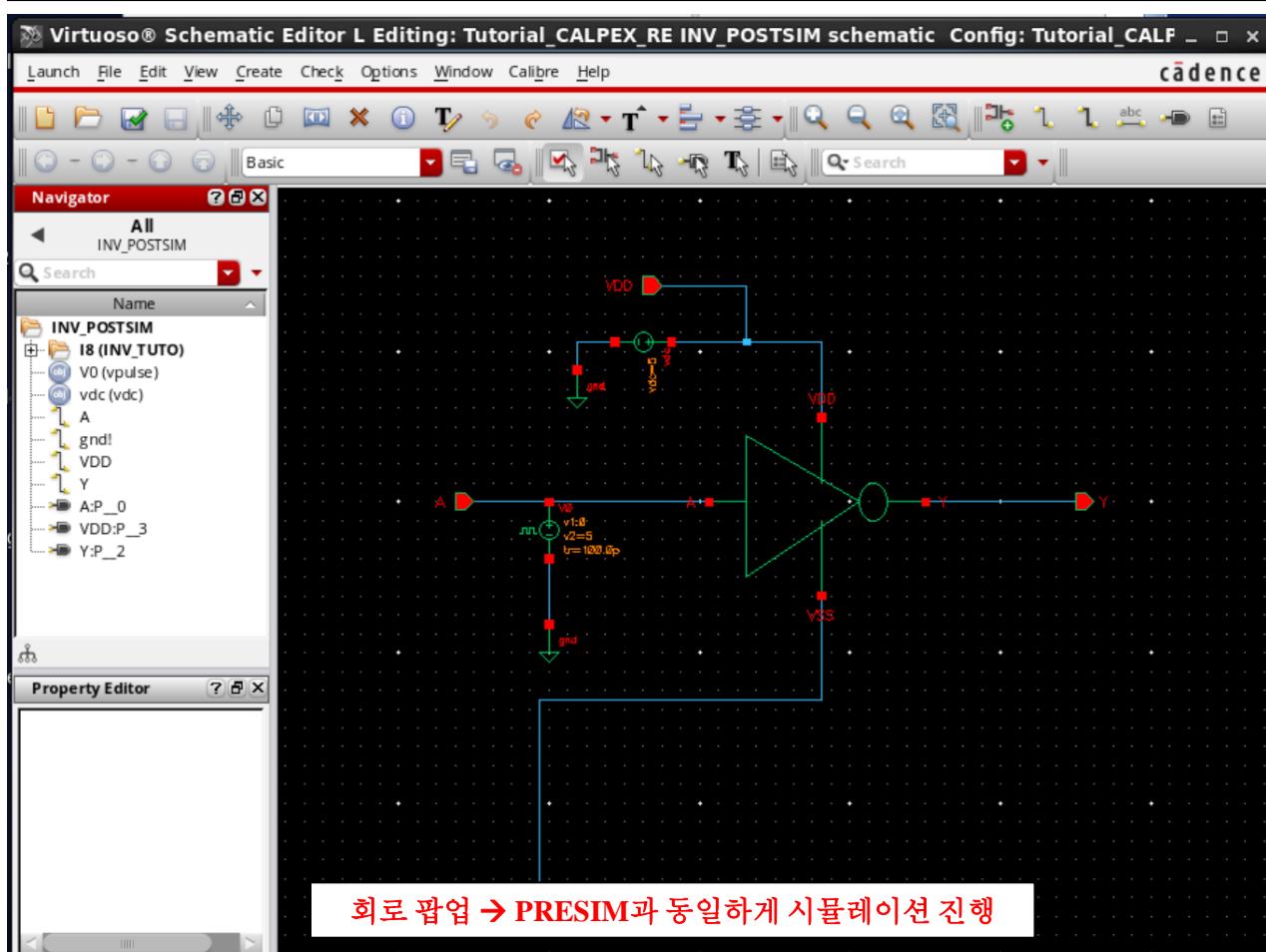
→ OK→ OK 클릭



Cell 우클릭 선택 → Setcell view 선택
 → Calibre 선택 → View / Update(needed)
 선택 → OK 선택 → Save



Library manager → Config 더블클릭
→ 설정 후 OK 클릭



4) 결과비교

