GOWIN

PROGRAMMING FOR THE FUTURE

GW5A series of FPGA Products

Schematic Manual

UG987-1.0.5E, 08/10/2023

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Revision History

Date	Version	Description
04/20/2023	1.0E	Initial version published.
05/06/2023	1.0.1E	The pin “DIN” updated to “MISO” in MSPI mode.
05/25/2023	1.0.2E	● “Figure 2-1 Isolate Wave Filtering” in “2.4 Schematic Design Considerations” updated. ● “Figure 3-1 RECONFIG_N, READY, DONE Schematic Reference Circuit” in “3.1.2 Schematic Design Considerations” updated. ● “Table 4-9 GW5A-25 Configuration Modes” in “4.8 Configuration Modes Supported by Each Device” updated.
06/08/2023	1.0.3E	The “Power-on Time and Sequence” removed.
06/30/2023	1.0.4E	● The “2.1 Overview” and “2.2 Power Index” in Chapter 2 “Power Supply” updated. ● LQ100 and PG256S packages added to “Table 4-9 GW5A-25 Configuration Modes” in “4.8 Configuration Modes Supported by Each Device”. ● The overview in “4.1 MODE” updated.
08/10/2023	1.0.5E	The overview of “4.1 MODE” optimized.

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1 About This Guide

1.1 Purpose

This manual describes the characteristics and special features of GW5A series of FPGA products and provides a comprehensive checklist to guide design processes.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- DS1103, GW5A series of FPGA Products Data Sheet
- UG985, GW5A-25 Pinout
- UG988, GW5A-138 Pinout
- UG1101, GW5A series of FPGA Products Package and Pinout Manual
- UG704, Arora V FPGA Products Programming and Configuration User Guide

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
CPU	Central Processing Unit
DDR	Double Data Rate
DQS	Bidirectional Data Strobe Circuit for DDR Memory
FPG	FCPBGA Package
FPGA	Field Programmable Gate Array
GCLK	Global Clock
GPA	Gowin Power analyzer
GPIO	Gowin Programmable Input/Output
HCLK	HCLK

Terminology and Abbreviations	Meaning
JTAG	Joint Test Action Group
LDO	Low Dropout Regulator
LVDS	Low-Voltage Differential Signaling
MIPI	Mobile Industry Processor Interface
MSPI	Master Serial Peripheral Interface
PLL	Phase-locked Loop
SPI	Serial Peripheral Interface
SSPI	Slave Serial Peripheral Interface

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Power Supply

2.1 Overview

GW5A series of FPGA products consist of two groups of voltage, as shown in Table 2-1.

Table 2-1 Arora V FPGA Products Voltage

Group	Name	Description
FPGA	VCC	Core voltage
	VCCX	Auxiliary voltage
	VCCIO	I/O Bank voltage
	VCC_EXT	VCC/VCCC Regulator and MIPI LP voltage
	VCC_REG	Regulator voltage
MIPI	M0_VDDA	MIPI M0 analog core voltage
	M0_VDDX	MIPI MO analog IO voltage
	M0_VDDD	MIPI M0 digital core voltage
	M0_VDD_12	MIPI voltage M0_VDD_12

2.2 Power Index

For the power supply requirements of the GW5A series devices, please refer to the Power section of the following document.

- UG985, GW5A-25 Pinout
- UG988, GW5A-138 Pinout

Note!

You should ensure GOWINSEMI products are always used within recommended operating conditions and range. Data beyond the working conditions and range are for reference only. GOWINSEMI does not guarantee that all devices will operate as expected beyond the standard operating conditions and range.

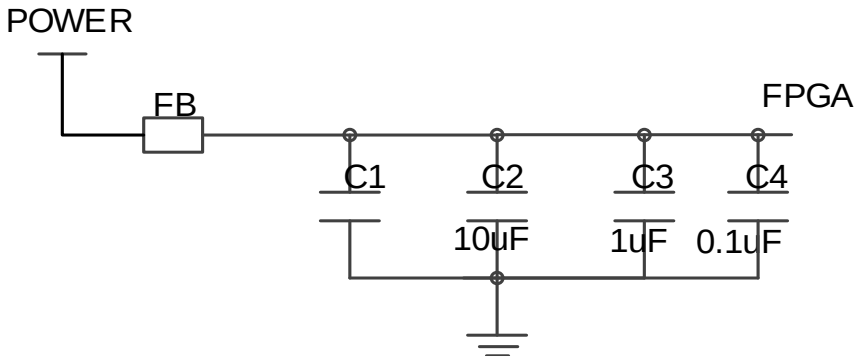
2.3 Total Power

For specific densities, packages, and resource utilizations, GPA tools can be used to evaluate and analyze the power consumption.

2.4 Schematic Design Considerations

1. GW5A series of FPGA products need to isolate the wave filtering for each voltage, as shown in Figure 2-1.

Figure 2-1 Isolate Wave Filtering



FB is a ferrite bead, C1, C2, C3 are ceramic capacitors with accuracy not less than ±10%. C1 determines the capacitance value according to the current magnitude.

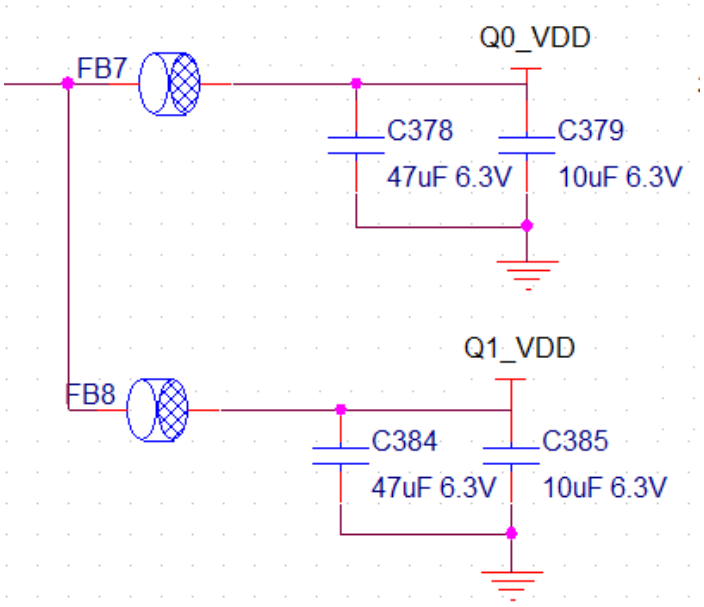
2. Combine power network and isolate ferrite bead.

Table 2-2 Recommendations for Power Combination

Group	Name	Recommendations for Power Combination
FPGA	VCC	If current is large, it is recommended to supply power independently.
	VCCX	With current requirements met, you can consider combining power supplies that are consistent with the supply voltage.
	VCCIO	It is recommended that the VCCIO of the bank where the configuration pin is located be powered separately. For other VCCIOs that meet current requirements, you can consider combining power supplies that are consistent with the supply voltage.
	VCC_REG	With current requirements met, you can consider combining power supplies that are consistent with the supply voltage.
MIPI	M0_VDDA	With current requirements met, you can consider combining it with M0_VDDD and M_VDD power supplies.
	M0_VDDD	With current requirements met, you can consider combining it with M0_VDDA and M_VDD power supplies.
	M0_VDDX	With current requirements met, you can consider combining power supplies that are consistent with the supply voltage.
	M_VDD	With current requirements met, you can consider combining it with M0_VDDA and M_VDDD power supplies.

If you want to combine power supplies, it is recommended that you use ferrite beads for isolation as follows.

Figure 2-2 Isolate with Ferrite Beads



3 Configuration Pins

3.1 READY, RECONFIG_N, DONE

3.1.1 Overview

Table 3-1 RECONFIG_N, READY, DONE Description

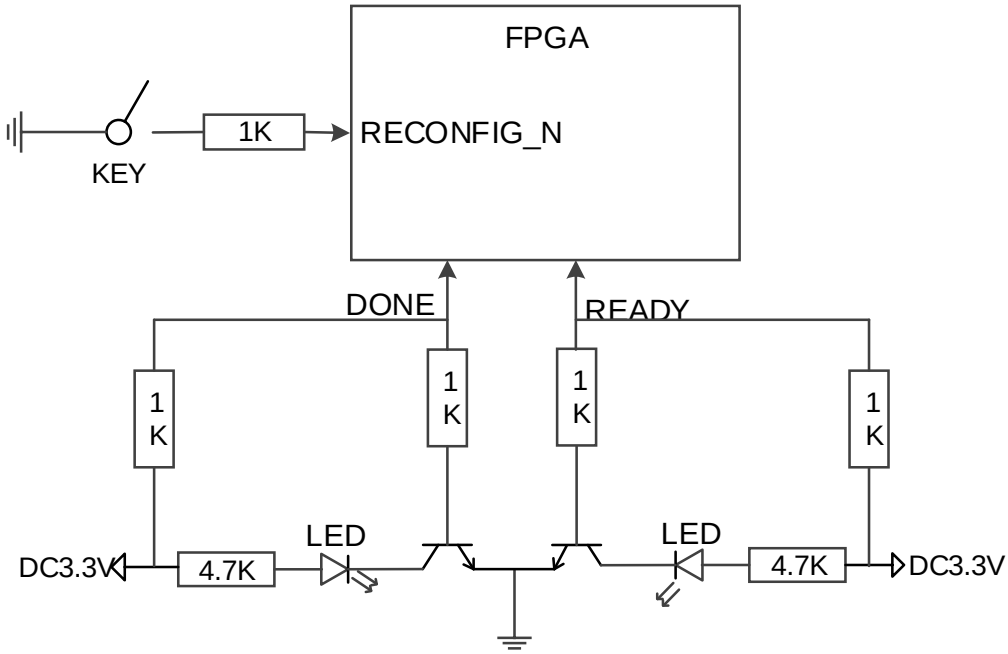
Name	I/O	Description
RECONFIG_N	I, internal weak pull-up	Active low is used as the reset function for the FPGA programming configuration. **FPGA can't be configured if RECONFIG_N is set to low**. Keep high-level during FPGA powering up until the powering up is stable for 1ms. As a configuration pin, a low level signal with pulse width no less than 25ns is required for GowinCONFIG to reload bitstream data according to the MODE setting value. You can control the pin by writing logic to trigger the device to reconfigure as required. As a GPIO, it can only be used as an output pin. To ensure a smooth configuration, set the initial value of RECONFIG_N to high.
READY	O	Active-high. FPGA can be configured only when the READY signal is pulled up. When the READY signal is pulled down, recover the status by powering up or triggering RECONFIG_N. As a configuration pin, it indicates that the FPGA can be configured or not. If the FPGA meets the configuration condition, the READY signal is high. If the configuration fails, READY signal is low.
DONE	I/O	A signal which indicates whether FPGA is configured successfully or not. DONE is pulled up after successfully configuring. As an output configuration pin, it indicates the current configuration of FPGA: if configured successfully, the DONE signal is high and the device enters into working state. if the configuration fails, the DONE signal keeps low. As an input configuration pin, the user can delay the entering of user mode via its own internal logic or by reducing the DONE signal. When RECONFIG_N or READY signals are low, DONE signal also keeps low. When configuring SRAM using JTAG circuit, it does not need

Name	I/O	Description
		to take DONE signal into account. As a GPIO, it can be used as an input or output pin. If DONE is used as an input GPIO, the initial value of DONE should be 1 before configuring. Otherwise, the FPGA will fail to enter the user mode after being configured.

3.1.2 Schematic Design Considerations

READY/DONE is open-drain output, external pull-up resistance is required.

Figure 3-1 RECONFIG_N, READY, DONE Schematic Reference Circuit



Note!

- The values of READY and DONE signals have no meaningful reference in JTAG configuration.
- The unbonded RECONFIG_N, READY, and DONE pins have been internally handled, with no influence on the configuration function.

3.2 CFGBVS

3.2.1 Overview

Table 3-2 CFGBVS Description

Name	I/O	Description
CFGBVS	I/O	CFGBVS (Configuration Banks Voltage Select) is a configuration bank voltage selection signal, which is an input pin. Configuration bank includes bank3, bank4, and bank10. When CFGBVS is 1, the bank voltage is 3.3V, 2.5V by default.

3.2.2 Schematic Design Considerations

This pin must be set to either High or Low.

3.3 PUDC_B

3.3.1 Overview

Table 3-3 PUDC_B Description

Name	I/O	Description
PUDC_B	I	As a configuration pin, PUDC_B (Pull-up During Configuration (bar)) is an input pin. The FPGA will determine the pin level during the configuration process after power on.When it is low, all GPIOs other than this pin will be weakly pull-up; when it is high, all GPIOs other than this pin will be high resistance.

3.3.2 Schematic Design Considerations

PUDC_B is not allowed to be floating during configuration and can be connected to the VCCIO or GND where it is located through a 1kΩ (or greater) resistor.

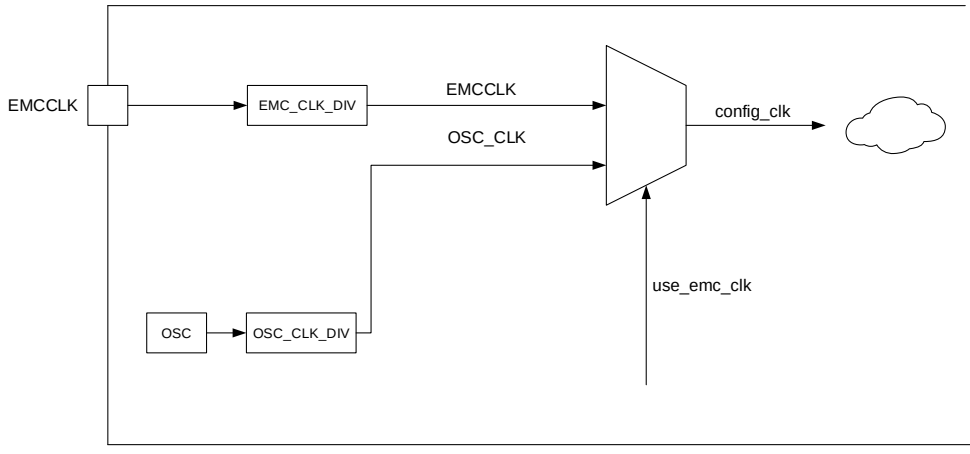
3.4 EMCCLK

3.4.1 Overview

Table 3-4 EMCCLK Description

Name	I/O	Description
EMCCLK	I	Used to configure the optional external clock input source in a master mode (versus the internal configuration oscillator). ● For master mode: FPGA can optionally switch to use EMCCLK as the clock source rather than internal oscillator. ● For slave mode: EMCCLK is not associated with slave mode.

Figure 3-2 EMCCLK and CCLK Diagram



4 Configuration Mode

4.1 MODE

4.1.1 Overview

MODE (MODE0, MODE1, MODE2) is GowinCONFIG configuration mode selection signal. When the FPGA powers on or a low pulse triggers the RECONFIG_N, the device enters the corresponding GowinCONFIG state according to the MODE value. MODE [1:0] and MODE [2:0] are used to select the GowinCONFIG programming configuration mode. The configuration mode can be fixed by using pull-up or pull-down resistors. It is recommended to use a 4.7K resistor for pull-up or a 1K resistor for pull-down. As the number of pins for each package is different, some MODE pins are not all bonded out for some devices, and the unbound MODE pins are internally grounded or internal-circuited to VCCIO by default. Please refer to the corresponding PINOUT manual for further details. As GPIOs, MODE pins can be used as an input or output. Note that when the MODE value changes, FPGA needs to be powered on again or provided with one low pulse for triggering RECONFIG_N to take effect.

GW5A series of FPGA products will automatically turn to SSPI mode after the program is loaded successfully. If SSPI mode is not used, make sure that SSPI_HOLDN has a pull-down resistor or SSPI_CSN has a pull-up resistor.

4.1.2 Signal Description

Table 4-1 MODE Signal Definition

Name	I/O	Description
MODE2	I, internal weak pull-down	GowinCONFIG mode selection pin port
MODE1	I, internal weak pull-down	GowinCONFIG mode selection pin port
MODE0	I, internal weak pull-down	GowinCONFIG mode selection pin port

4.1.3 Mode Selection

Table 4-2 GW5A Configuration Modes

Configuration Mode	MODE[1:0][1]	MODE[2:0][1]	Bus Width	Description
JTAG	XX[2]	XXX[2]	-	Arora V FPGA products are configured by external Host via JTAG interface
MSPI	01	010/011/101	x1,x2,x4	As a Master, FPGA reads data from external Flash (or other devices) via the SPI interface for configuration
Master SERIAL	01	010/011/101	x1	Before FPGA used as a Slave, FPGA reads data from external devices via the DIN interface for configuration
Slave SERIAL	11	000/100	x1	Arora V FPGA products are configured by external Host via DIN interface
Master CPU	00	001	x8,x16,x32	Before FPGA used as a Slave, FPGA reads data from external devices via the DBUS interface for configuration
Slave CPU	10	110/111		Arora V FPGA products are configured by external Host via DBUS interface

Note!

- [1] Please refer to the related Pinout manuals for the status of the unbound MODE pins.
- [2] The JTAG configuration mode is independent of the MODE [1:0] and MODE [2:0] values.

4.2 JTAG

4.2.1 Overview

In JTAG configuration mode, bitstream data is written to the SRAM of Gowin FPGA products. All configuration data is lost after the device is powered down. All Gowin FPGA products support the JTAG configuration mode.

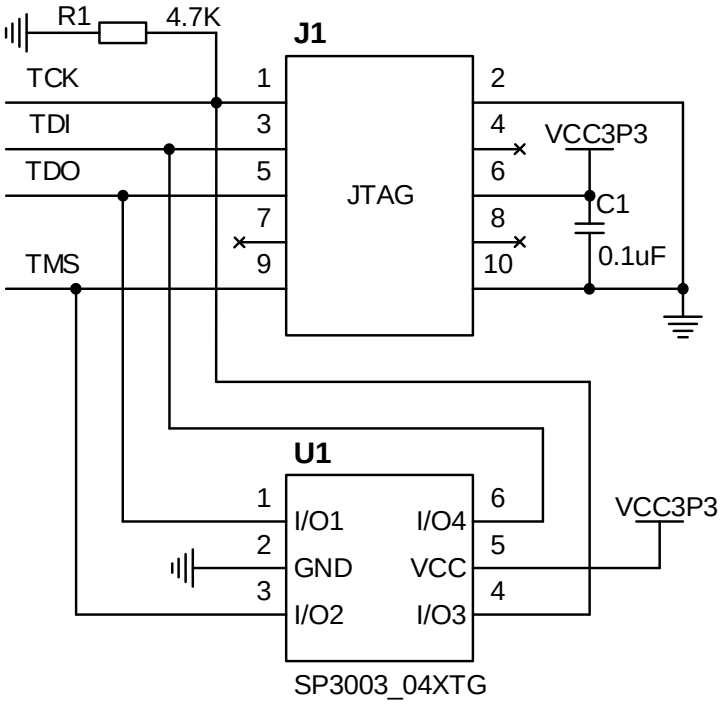
4.2.2 Signal Description

Table 4-3 Signal Definition of JTAG Configuration Mode

Name	I/O	Description
TCK	I	JTAG serial clock input
TMS	I, internal weak pull-up	JTAG serial mode input
TDI	I, internal weak pull-up	JTAG serial data input
TDO	O	JTAG serial data output

4.2.3 JTAG Circuit Reference

Figure 4-1 Connection Diagram for JTAG Configuration Mode



Note!

The clock frequency for JTAG configuration mode cannot be higher than 100MHz.

4.3 MSPI

4.3.1 Overview

In MSPI (Master SPI) mode, FPGA is as a Master and reads bitstream data from the external Flash via SPI interface to complete configuration.

4.3.2 Signal Definition

Table 4-4 Signal Definition of MSPI Configuration Mode

Name	I/O	Description
CCLK	I/O	Clock Configuration ● Slave mode: CCLK is an input and requires connection to an external clock source ● Master mode: CCLK is an output
MCSN	O	Enable signal in MSPI mode, active-low
MISO	I/O	MSPI Mode: Serial data input in X1 mode; In X2 and X4 modes, the input pin of parallel data bit 1 that connects to DQ1/Q/SO/IO1 pins of external Flash device
MOSI	I/O	MSPI Mode: Serial instruction and address output. in X2 and X4 modes, the input pin of parallel data bit 0 connects to pin DQ0/D/SI/IO0 of external Flash device.

4.3.3 Circuit Reference

The connection diagram for configuring Gowin FPGA products through MSPI is shown in Figure 4-2 ~ Figure 4-4.

Figure 4-2 Connection Diagram for MSPIx1 Configuration Mode

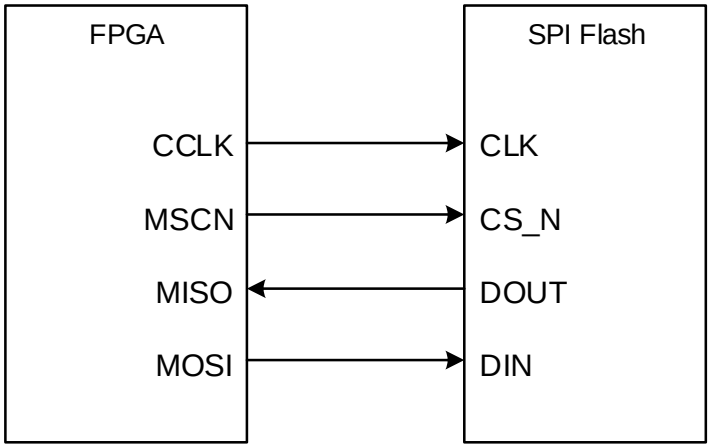


Figure 4-3 Connection Diagram for MSPIx2 Configuration Mode

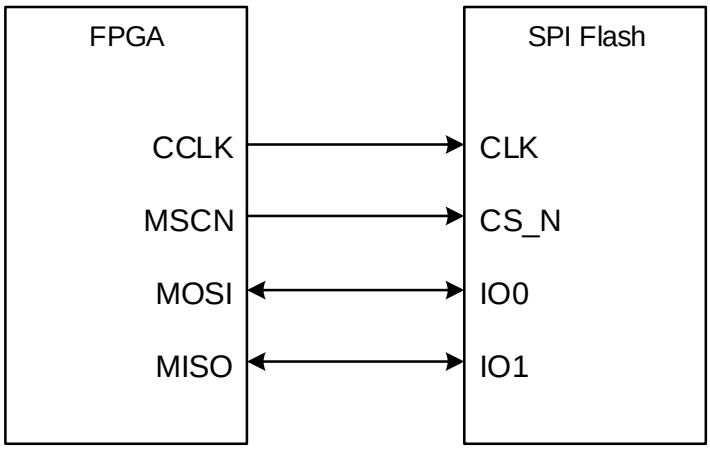
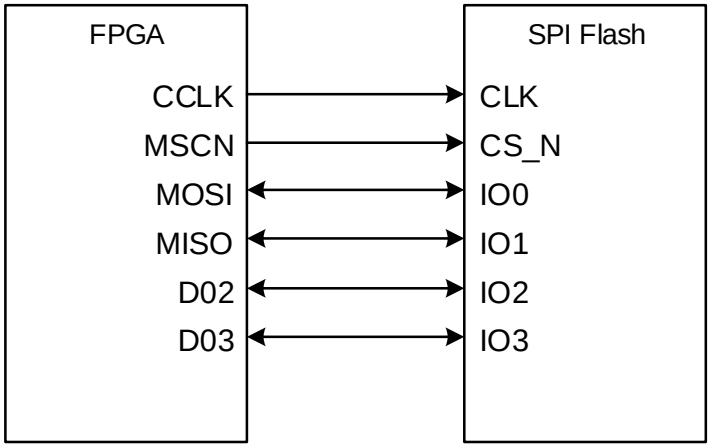


Figure 4-4 Connection Diagram for MSPIx4 Configuration Mode



4.4 SSPI

4.4.1 Overview

In SSPI (Slave SSPI) mode, FPGA is a slave device and is configured via SPI interface by an external Host.

4.4.2 Signal Definition

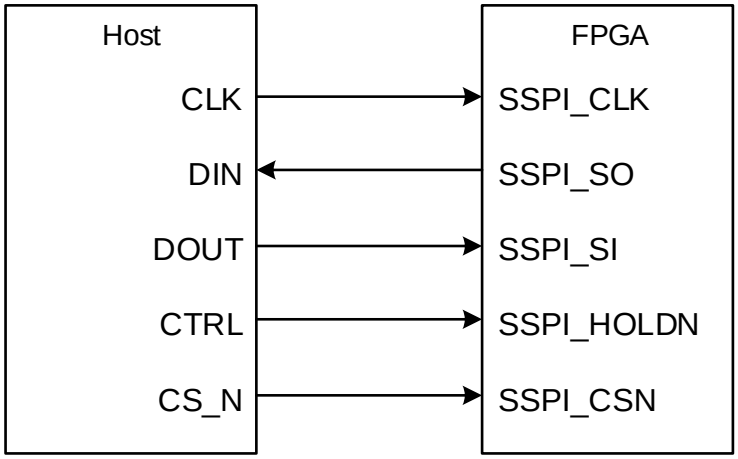
Table 4-5 Signal Definition of SSPI Configuration Mode

Name	Description
SSPI_HOLDN	As a configuration pin, it is an input pin with internal weak pull-up. SSPI clock lock pin: ● When the input is high level, the operation corresponding to SCLK is valid; ● When the input is low level, the operation corresponding to SCLK is invalid. As a GPIO, it can be used as an input or output pin.
SSPI_CSN	As a configuration pin, it is an input pin with internal weak pull-up. It is a chip selection signal in the SSPI configuration mode, active low. As a GPIO, it can be used as an input or output pin.
SSPI_CLK	As a configuration pin, it is an input pin. It is a clock input pin of SSPI configuration mode. As a GPIO, it can be used as an input or output pin.
SSPI_SI	As a configuration pin, it is an input pin. It is a serial data input pin in the SSPI configuration mode. As a GPIO, it can be used as an input or output pin.
SSPI_SO	As a configuration pin, it is an output pin. It is a serial data output pin in the SSPI configuration mode. As a GPIO, it can be used as an input or output pin.
SSPI_WPN	As a configuration pin, it is an input pin. A write protection pin in SSPI mode: SSPI operation is valid when the input is high, SSPI operation is invalid when the input is low. As a GPIO, it can be used as an input or output pin.

4.4.3 Circuit Reference

The connection diagram for configuring Gowin FPGA products via SSPI is shown in Figure 4-5.

Figure 4-5 Connection Diagram for SSPI Configuration Mode

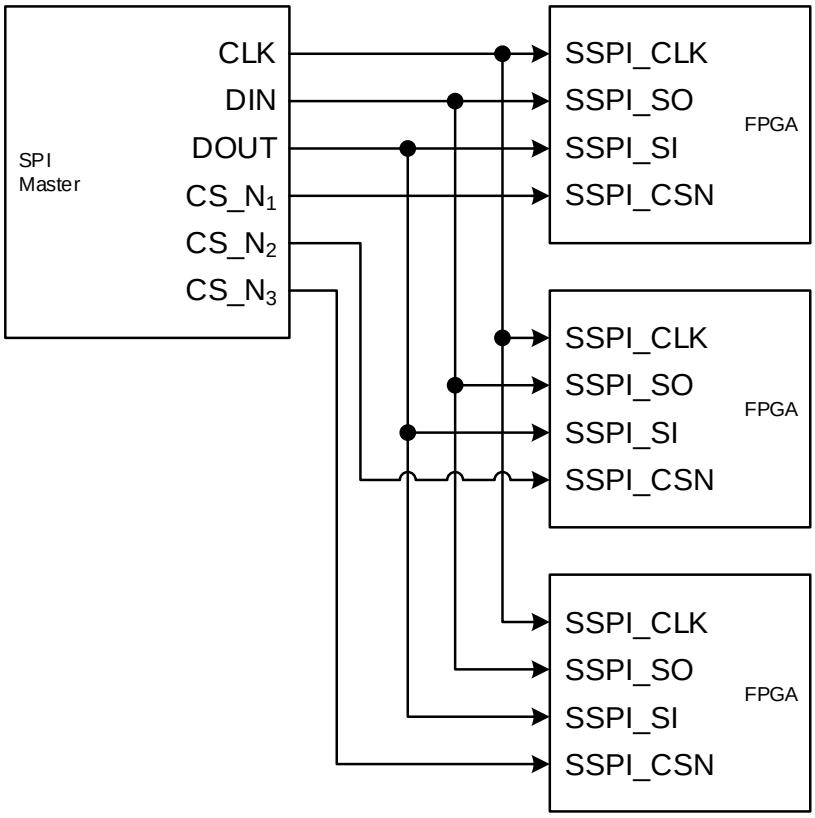


Note!

This figure is the connection diagram for SSPI configuration mode.

The connection diagram for configuring multiple FPGA products via SSPI is shown in Figure 4-6.

Figure 4-6 Multiple FPGA Connection Diagram



4.5 CPU

4.5.1 Overview

CPU mode consists of Master CPU and Slave CPU.

In Master CPU mode (i.e. FPGA is the master device), the configuration data is read from the external via the DBUS interface for configuration.

In Slave CPU mode, GW5A series of FPGA products are configured by external Host via DBUS interface.

4.5.2 Signal Definition

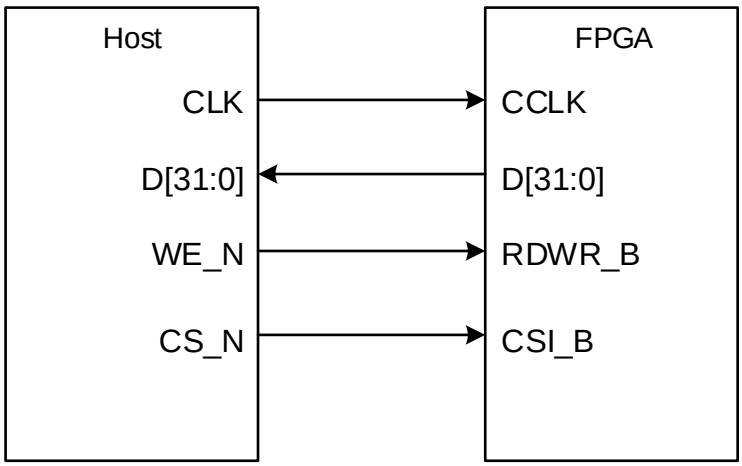
Table 4-6 Signal Definition of CPU Configuration Mode

Name	Description
D00~D31	Input/Output pins In CPU mode, D00~D31 are data input/output pins. The FPGA device will automatically detect the bus width of x8, x16, or x32. As a GPIO, it can be used as an input or output pin.
DIN	In CPU modes, DIN is a multi-function pin as D01 data pin. As a GPIO, it can be used as an input or output pin.
CSI_B[1]	As a configuration pin, it is an input pin. It is a chip selection input signal in the CPU mode, active low. ● In master CPU mode, connect to GND directly or via a 1 kΩ (or greater) resistor. ● In slave CPU mode: An external configuration controller can control CSI_B for selecting the devices to be configured on the bus, or in a daisy-chain configuration, connect to the CSO_B pin of the upstream devices.
RDWR_B	As a configuration pin, it is an input pin. Read/write enable signal selection pin in CPU configuration mode ● High, it indicates read operation ● Low, it indicates write operation As a GPIO, it can be used as an input or output pin.
CCLK[3]	As a configuration clock pin, CCLK runs the synchronous FPGA configuration sequence in all modes except JTAG mode. ● In slave mode: CCLK is an input and requires connection to an external clock source. ● In master mode: CCLK is an output as configuration source clock. **Note!** CCLK is the key clock signal, so good signal integrity must be ensured.
CSO_B	As a configuration pin, it is an output pin. It is a chip selection input signal in the CPU mode. It connects to the CSI_B pin of the downstream FPGA in a daisy-chain configuration.

4.5.3 Circuit Reference

The connection diagram for the CPU mode is shown in Figure 4-7.

Figure 4-7 Connection Diagram for CPU Mode



Note!

CCLK is an output in master mode and an input in slave mode.

Other than the power requirements, the following conditions need to be met to use the CPU configuration mode:

- CPU interface enable
  RECONFIG_N is not set as a GPIO during the first configuration after power up or the previous programming.
- Initiate new configuration
  Power-on again or trigger RECONFIG_N at one low pulse.

4.6 SERIAL

4.6.1 Overview

In SERIAL configuration mode, Host configures Gowin FPGA products through the serial interface. SERIAL is one of the configuration modes that use the least number of pins. It supports both master mode and slave mode. The only difference between the two modes is the different direction of the interface clock. The SERIAL mode can only write bitstream data to FPGA and cannot readback data from FPGA devices; as such, the SERIAL mode cannot read information on the ID CODE and USER CODE and status register.

4.6.2 Signal Definition

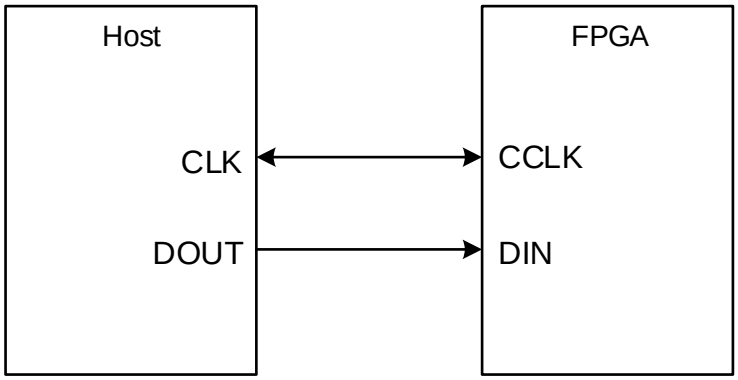
Table 4-7 Signal Definition of SERIAL Configuration Mode

Name	Description
DIN	As a configuration pin, it is an input pin. It is a serial data input pin. ● In SERIAL and MSPI modes: DIN receives serial data from the data source and samples data at the CCLK rising edge in the default configuration. ● In CPU mode, DIN is a multi-function pin as D01 data pin. As a GPIO, it can be used as an input or output pin.
CCLK	As a configuration clock pin, CCLK runs the synchronous FPGA configuration sequence in all modes except JTAG mode. ● In slave mode: CCLK is an input and requires connection to an external clock source. ● In master mode: CCLK is an output as configuration source clock. **Note!** CCLK is the key clock signal, so good signal integrity must be ensured.

4.6.3 Circuit Reference

The connection diagram for the SERIAL mode is shown in Figure 4-8.

Figure 4-8 Connection Diagram for SERIAL Configuration Mode



Note!

CCLK is an output in master mode and an input in slave mode.

4.7 Pin Multiplexing Configuration

4.7.1 Overview

To maximize the utilization of I/O, Gowin FPGA product support for setting the configuration pins as GPIO pins. Before any configuration operation is performed on all series of Gowin FPGA products after power up, all related configuration pins are used as configuration pins by default. After successful configuration, the device enters into user mode and pins are reassigned according to the options selected by users.

Note!

When setting the pin multiplexing options, ensure the external initial connection of the pins does not affect the device configuration. Isolate the connections that affect the configuration first, and then wait to modify them in user mode.

Table 4-8 Pin Multiplexing Options

Name	Options	Description
JTAG PORT	Default	TMS, TCK, TDI, and TDO are dedicated configuration pins.
	Set as GPIOs	TMS, TCK, TDI, and TDO are used as GPIOs after configuration.
CPU PORT	Default	CSI_B, CSO_B, RDWR_B, D[0-31], and CCLK are dedicated configuration pins.
	Set as GPIOs	CSI_B, CSO_B, RDWR_B, D[0-31], and CCLK are used as GPIOs after configuration.
SSPI PORT	Default	SSPI_CSN, SSPI_CLK, SSPI_SI, SSPI_SO, SSPI_HOLD, and SSPI_WPN are dedicated configuration pins.
	Set as GPIOs	SSPI_CSN, SSPI_CLK, SSPI_SI, SSPI_SO, SSPI_HOLD, and SSPI_WPN are used as GPIOs after configuration.
MSPI PORT	Default	MCSN, MISO, MOSI, D2, D3, and CCLK are dedicated configuration pins.
	Set as GPIOs	MCSN, MISO, MOSI, D2, D3, and CCLK are used as GPIOs after configuration.
SERIAL	Default	DIN, DOUT, and CCLK are dedicated configuration pins.
	Set as GPIOs	DIN, DOUT, and CCLK are used as GPIOs after configuration.
RECONFIG_N	Default	Dedicated configuration pins.
	Set as GPIOs	Used as GPIOs after configuration.
READY	Default	Dedicated configuration pins.
	Set as GPIOs	Used as GPIOs after configuration.
DONE	Default	Dedicated configuration pins.
	Set as GPIOs	Used as GPIOs after configuration.

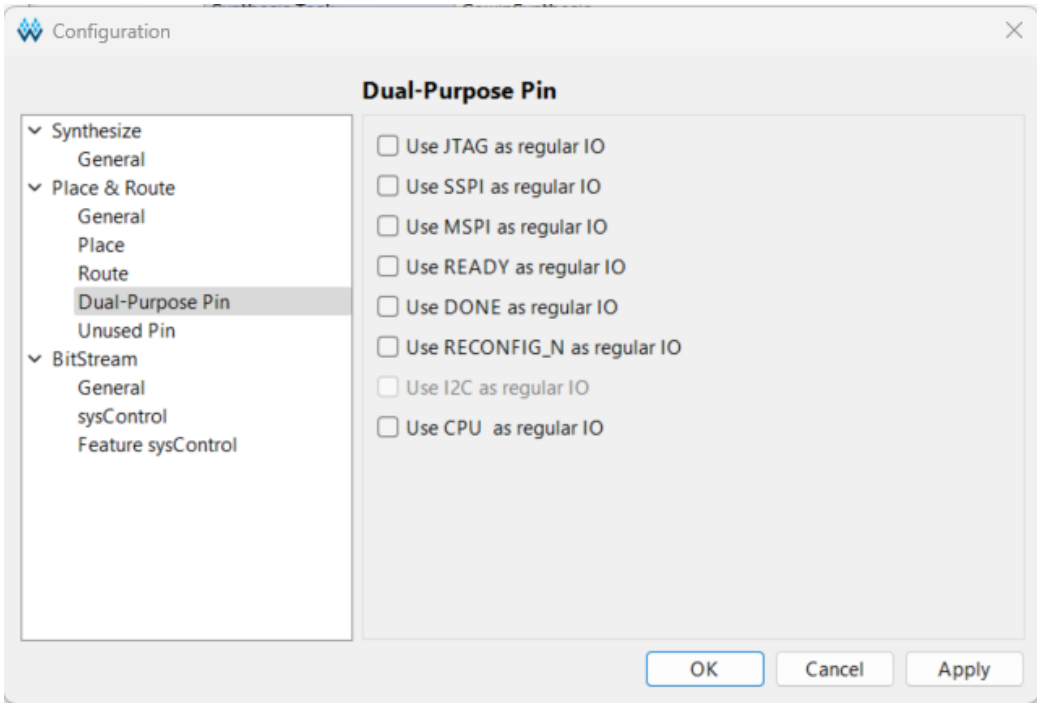
4.7.2 Pin Multiplexing

Pin Multiplexing Configuration

Users can configure pin multiplexing via Gowin Software.

1. Open the corresponding project in Gowin Software.
2. Select “Project > Configuration > Dual-Purpose Pin” in the menu bar, as shown in Figure 4-9;
3. Check the corresponding options to set the pin multiplexing.

Figure 4-9 Configuring Pin Multiplexing



4.8 Configuration Modes Supported by Each Device

GW5A-25

Table 4-9 GW5A-25 Configuration Modes

Configuration Mode	JTAG	MSPI	Master SERIAL	Slave SERIAL	Master CPU	Slave CPU
MG121N	Yes	No	No	No	No	No
UG324S	Yes	Yes	Yes	Yes	Yes	Yes
UG256C	Yes	Yes	Yes	Yes	No	No
PG256C	Yes	Yes	Yes	Yes	No	No
UG324	Yes	Yes	Yes	Yes	Yes	Yes
MG196S	Yes	Yes	Yes	Yes	Yes	Yes
UG225S	Yes	Yes	Yes	Yes	Yes	Yes
LQ100	Yes	Yes	Yes	Yes	No	No
PG256S	Yes	Yes	Yes	Yes	Yes	Yes

GW5A-138

Table 4-10 GW5A-138 Configuration Modes

Configuration Mode	JTAG	MSPI	Master SERIAL	Slave SERIAL	Master CPU	Slave CPU
UG324A	Yes	Yes	Yes	Yes	Yes	Yes

5 Clock Pin

5.1 Overview

GW5A series of FPGA products provide the global clock network (GCLK) which connects to all the device resources directly. In addition to the GCLK, PLL, HCLK, DDR memory interface DQS, etc. are also provided.

For more detailed information of GCLK, HCLK, PLL, and DDR memory interface DQS, see the following manuals.

- UG306, Arora V Clock User Guide
- DS1103, GW5A series of FPGA Products Data Sheet

GCLK: The GCLK is distributed as 8 clock regions in GW5A series of FPGA products. Each Clock provides 16 GCLKs. The clock sources of GCLK can be from dedicated clock pins, the output of the PLL, the output of HCLK, and common wiring resources. Using a dedicated clock input pin provides better clock performance.

HCLK: HCLK is the high-speed clock in GW5A series of FPGA products. It can support high-speed data transfer and is mainly suitable for source synchronous data transfer protocols.

PLL: PLL blocks in GW5A series of FPGA products can configure the parameters to adjust the frequency (multiplication and division), phase, and duty cycle.

DDR Memory Interface Clock DQS

CCLK: As a configuration signal clock, CCLK runs the synchronous FPGA configuration sequence in all modes except JTAG mode.

EMCCLK: EMCCLK as an external clock input, FPGA can optionally switch to use EMCCLK as the clock source rather than internal oscillator.

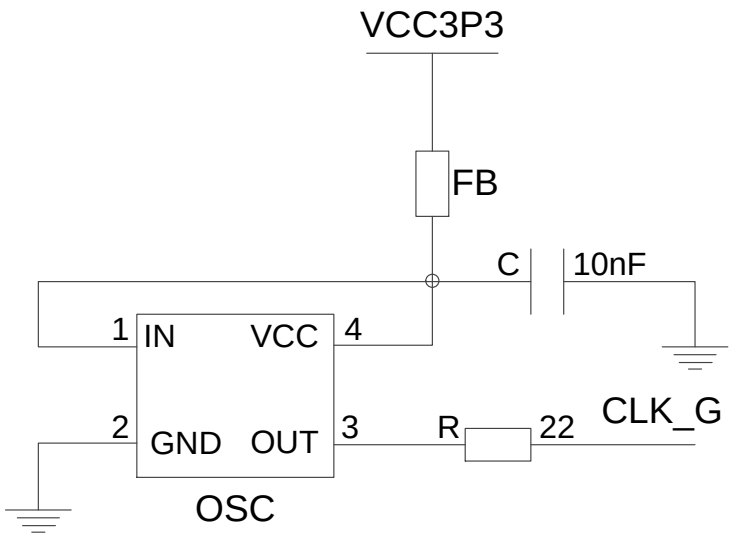
Table 5-1 Clock Overview

Name	I/O	Overview
SGCLKT_[x]	I	Dedicated clock input pin driving the same clock region, T (True), [x]: clock No.
SGCLKC_[x]	I	Differential input pin of SGCLKT_[x], C (Comp), [x]: clock No.
MGCLKT_[x]	I	Dedicated clock input pin driving multiple clock region, T (True), [x]: clock No.
MGCLKC_[x]	I	Differential input pin of MGCLKT_ x], C (Comp), [x]: clock No.
LPLL_C_fb/ RPLL_C_fb	I	Left/Right PLL feedback input pin, C(Comp)
LPLL_T_fb/R PLL_T_fb	I	Left/Right PLL feedback input pin, T(True)
LPLL_C_in/R PLL_C_in	I	Left/Right PLL clock input pin, C(Comp)
LPLL_C_in/R PLL_C_in	I	Left/Right PLL clock input pin, T(True)
EMCCLK	I	Used to configure the optional external clock input in a master mode (versus the internal configuration oscillator). ● In master mode: FPGA can optionally switch to use EMCCLK as the clock source rather than internal oscillator. ● In slave mode: EMCCLK is not associated with slave mode.
CCLK	I/O	As a configuration clock pin, CCLK runs the synchronous FPGA configuration sequence in all modes except JTAG mode. ● In master mode: CCLK is an output as configuration source clock. ● In slave mode: CCLK is an input and requires connection to an external clock source. **Note!** CCLK is the key clock signal, so good signal integrity must be ensured.
TCK	I	JTAG mode: Serial clock input

5.2 Schematic Design Considerations

1. System clock pins selection: GCLK is directly connected to all resources in the device. The GCLK_T end is advised if the GCLK inputs from the single-end. If the external clock as a PLL clock input, it is advised to input from the PLL dedicated pin. And the PLL_T end is selected if the external clock inputs from the single-end.
2. External Crystal Oscillator Circuit Reference

Figure 5-1 FPGA External Crystal Oscillator Circuit



FB is a ferrite bead, with MH2029-221Y reference model, more than ±5% resistance accuracy, and more than ±10% capacitance accuracy.

6 Differential Pins

1. Overview

Differential transmission is a form of signal transmission technology that operates according to differences between the signal line and the ground line. The differential transmission transmits signals on these two lines, the amplitude of the two signals are equal and have the same phase but demonstrate opposite polarity.

2. LVDS

LVDS is a low-voltage differential signal that offers low power consumption, low bit error rate, low crosstalk, and low radiation. It facilitates the transmission of data using a low-voltage swing high-speed differential. Different packages employ different signals. Please refer to the True LVDS section of the Package Pinout Manual for further details.

3. Schematic Design Considerations

All banks of GW5A series of FPGA products support true differential input.

The differential input requires an external 100 ohm termination resistor, which is laid out on the PCB as close as possible to the input pins. The PCB design needs to control the differential line impedance at around 100 ohms.

7 Pinout

Before designing circuits, users should take the overall FPGA pin distribution into consideration and make informed decisions related to the application of the device architecture features, including I/O LOGIC, global clock resources, PLL resources, etc.

All banks of the GW5A series of FPGA products support true LVDS output, please refer to GW5A series of FPGA Product Pinout to ensure that the corresponding pins support true LVDS output.

To support SSTL, HSTL, etc., each bank also provides one independent voltage source (V_{REF}) as the reference voltage. Users can choose V_{REF} from the internal reference voltage of the bank (0.5 * V_{CCIO}) or external reference voltage V_{REF} using any I/O from the bank.

For DDR related pinout, please see *TN662, Gowin FPGA-based DDR2 & DDR3 Hardware Design Reference Manual*.

Note!

Before and during configuration, all GPIOs of the device are internally weak pull-up. After the configuration is complete, the I/O state is None, which can be configured via the software. The state of CONFIG-related I/Os varies depending on the configuration mode.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