



GW5A series of FPGA Products

Package & Pinout User Guide

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Revision History

Date	Version	Description
04/20/2023	1.0E	Initial version published.
05/25/2023	1.1E	MG196S and UG225S packages added.
07/06/2023	1.1.1E	LQ100 and PG256S packages added.
08/10/2023	1.1.2E	The pin designator of VCC_REG in “Table 3-3 Other Pins in GW5A-25 UG256C (EV Version)” of “3.1.3 View of UG256C (EV Version) Pin Distribution” updated.

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1 About This Guide

1.1 Purpose

This manual introduces Gowin GW5A series of FPGA products package and provides pin definitions, a list of pin numbers, pin distribution view, and package diagrams.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- [DS1103, GW5A series of FPGA Products Data Sheet](#)
- [UG985, GW5A-25 Pinout](#)
- [UG988, GW5A-138 Pinout](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable Input/Output
LQ	LQFP Package
MG	MBGA Package
PG	PBGA Package
UG	UBGA Package

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

Gowin GW5A series of FPGA products are the fifth generation of Arora family with abundant internal resources, a new-architecture and high-performance DSP supporting AI operations, high-speed LVDS interfaces, and abundant BSRAM resources. At the same time, GW5A series of products integrate self-developed DDR3 and provide a variety of packages. They are suitable for applications such as low power, high performance and compatibility design.

Gowin provides a new generation of FPGA hardware development environment that supports FPGA synthesis, placement & routing, bitstream generation and download, etc.

2.1 PB-Free Package

GW5A series of FPGA products are PB free in line with the EU RoHS environmental directives. The substances used in the GW5A series of FPGA products are in full compliance with the IPC-1752 standards.

2.2 Package and Max. User I/O Information

Table 2-1 Package, Max. User I/O Information, and LVDS Pairs

Package	Pitch (mm)	Size (mm)	E-pad Size (mm)	GW5A-25	GW5A-138
LQ100	0.5	14 x 14	-	80 (36)	-
MG121N	0.5	6 x 6	-	86 (38)	-
MG196S	0.5	8 x 8	-	114 (53)	-
PG256C	1.0	17 x 17	-	191 (90)	-
PG256S	1.0	17 x 17	-	194 (93)	-
UG225S	0.8	13 x 13	-	168 (80)	-
UG256C	0.8	14 x 14	-	191 (90)	-
UG324	0.8	15 x 15	-	222 (104)	-
UG324A	0.8	15 x 15	-	-	222 (106)
UG324S	0.8	15 x 15	-	239 (116)	-

Note!

For package type abbreviations employed in this manual, see 1.3 Terminology and Abbreviations.

2.3 Power Pins

Table 2-2 GW5A Power Pins

VCC	VCCIO0	VCCIO1	VCCIO2
VCCIO3	VCCIO4	VCCIO5	VCCIO6
VCCIO7	VCCIO10	VCCX	VSS
VCCC	VCC_REG	VQPS	VCC_EXT
M0_VDDA	M0_VDDD	M1_VDDA	M1_VDDD
M0_VDDX	M1_VDDX	M0_VDD_12	-

2.4 Pin Quantity

2.4.1 Quantity of GW5A-25 Pins

Table 2-3 Quantity of GW5A-25 Pins

Pin Type	GW5A-25									
	MG121N	UG324S	UG324	MG196S ^[1]	MG196S ^[2]	UG225S ^[1]	UG225S ^[2]	UG256C ^[1]	UG256C ^[2]	
Single-ended IO/ Differential pair/LVDS ^[3]	BANK0	6/3/3	30/15/15	30/15/15	12/6/6	12/6/6	22/11/11	22/11/11	25/12/12	25/12/12
	BANK1	10/5/5	30/15/15	29/14/14	14/7/7	14/7/7	18/9/9	18/9/9	27/13/13	27/13/13
	BANK2	12/6/6	28/14/14	27/13/13	14/7/7	14/7/7	24/12/12	24/12/12	26/13/13	26/13/13
	BANK3	4/2/2	28/14/14	27/13/13	12/6/6	12/6/6	16/8/8	16/8/8	19/9/9	19/9/9
	BANK4	11/4/4	35/17/17	35/17/17	20/9/9	20/9/9	28/13/13	28/13/13	20/8/8	20/8/8
	BANK5	13/5/5	27/13/13	25/11/11	11/5/5	11/5/5	13/6/6	13/6/6	26/13/13	26/13/13
	BANK6	10/5/5	28/14/14	17/8/8	14/7/7	14/7/7	24/12/12	24/12/12	26/13/13	26/13/13
	BANK7	16/8/8	28/14/14	27/13/13	12/6/6	12/6/6	18/9/9	18/9/9	18/9/9	18/9/9
	BANK10	4/2/0	4/2/0	4/2/0	4/2/0	4/2/0	4/2/0	4/2/0	4/2/0	4/2/0
	BANK11	0/0/0	1/0/0	1/0/0	1/0/0	1/0/0	1/0/0	0/0/0	0/0/0	0/0/0
Max. User I/O		86	239	222	114	114	168	168	191	191
Differential Pair		40	118	106	55	55	82	82	92	92
True LVDS Output		38	116	104	53	53	80	80	90	90
VCC		0	0	0	0	0	0	0	0	0
VCCX		0	0	0	0	0	0	0	2	2
VCCIO0		0	0	0	2	2	2	2	2	2
VCCIO1		0	0	0	2	2	2	2	3	3
VCCIO2		0	0	0	3	3	2	2	3	3
VCCIO3		0	0	0	3	3	2	2	2	2
VCCIO4		1	0	0	2	2	2	0	0	0
VCCIO5		0	0	0	2	2	2	3	3	3

Pin Type	GW5A-25								
	MG121N	UG324S	UG324	MG196S ^[1]	MG196S ^[2]	UG225S ^[1]	UG225S ^[2]	UG256C ^[1]	UG256C ^[2]
VCCIO6	0	0	0	3	3	2	2	3	3
VCCIO7	0	0	0	3	3	2	2	2	2
VCCIO10	0	0	0	0	0	0	0	0	0
VCC/VCCC	3	0	0	0	14	0	6	0	9
VCC_REG	1	1	1	1	1	1	1	1	1
VCC_EXT	0	10	6	14	0	6	0	9	0
VCC_EXT/VCC_REG/VCCI_O0	0	0	0	0	0	0	0	0	0
VCCIO0/VCCIO1	1	6	6	0	0	0	0	0	0
VCCIO2/VCCIO3	1	6	6	0	0	0	0	0	0
VCCIO3/VCCIO4/VCCIO5	0	0	0	0	0	0	0	0	0
VCCIO4/VCCIO5	0	6	6	0	0	0	0	0	0
VCCIO6/VCCIO7	1	6	6	0	0	0	0	0	0
VCCIO10/VCCIO5	1	0	0	0	0	0	0	0	0
VCCIO10/VCCIO4	0	0	0	0	0	0	0	2	2
M0_VDDX/VCCX	4	0	0	0	0	0	0	0	0
VCCIO10/VCCX	0	12	0	8	8	8	8	0	0
M0_VDD_12/VCC_EXT	1	0	0	0	0	0	0	0	0
M0_VDD_12	0	0	1	0	0	0	0	0	0
M0_VDDX/VCCIO10/VCCX	0	0	12	0	0	0	0	0	0
M0_VDDA/M0_VDDD/VCC/VCCC	0	0	10	0	0	0	0	0	0
M0_VDDD	1	0	0	0	0	0	0	0	0
M0_VDDA	1	0	0	0	0	0	0	0	0
VQPS	1	1	1	1	1	1	1	1	1

Pin Type	GW5A-25								
	MG121N	UG324S	UG324	MG196S [1]	MG196S [2]	UG225S [1]	UG225S [2]	UG256C [1]	UG256C [2]
VSS	10	36	36	38	38	24	24	32	32
MODE0	0	1	1	1	1	1	1	1	1
MODE1	0	1	0	1	1	1	1	1	1
MODE2	0	0	0	0	0	0	0	1	1
NC	2	1	1	0	0	1	1	0	0

Continued

Pin Type	GW5A-25				
	PG256C [1]	PG256C [2]	LQ100 [1]	PG256S [1]	
Single-ended IO/ Differential pair/LVDS ^[3]	BANK0	25/12/12	25/12/12	0/0/0	20/10/10
	BANK1	27/13/13	27/13/13	8/4/4	20/10/10
	BANK2	26/13/13	26/13/13	16/8/8	28/14/14
	BANK3	19/9/9	19/9/9	4/2/2	26/13/13
	BANK4	20/8/8	20/8/8	13/6/6	26/12/12
	BANK5	26/13/13	26/13/13	4/2/2	15/7/7
	BANK6	26/13/13	26/13/13	19/8/8	26/13/13
	BANK7	18/9/9	18/9/9	12/6/6	28/14/14
	BANK10	4/2/0	4/2/0	4/2/0	4/2/0
	BANK11	0/0/0	0/0/0	0/0/0	1/0/0
	Max. User I/O	191	191	80	194
	Differential Pair	92	92	38	95
True LVDS Output	90	90	36	93	
VCC	0	0	0	0	
VCCX	2	2	0	0	

Pin Type	GW5A-25			
	PG256C ^[1]	PG256C ^[2]	LQ100 ^[1]	PG256S ^[1]
VCCIO0	2	2	0	2
VCCIO1	3	3	1	3
VCCIO2	3	3	1	3
VCCIO3	2	2	0	3
VCCIO4	0	0	0	2
VCCIO5	3	3	0	2
VCCIO6	3	3	1	3
VCCIO7	2	2	1	2
VCCIO10	0	0	0	0
VCC/VCCC	0	9	0	0
VCC_REG	1	1	0	1
VCC_EXT	9	0	0	7
VCC_EXT/VCC_REG/VCCIO0	0	0	3	0
VCCIO0/VCCIO1	0	0	0	0
VCCIO2/VCCIO3	0	0	0	0
VCCIO3/VCCIO4/VCCIO5	0	0	2	0
VCCIO4/VCCIO5	0	0	0	0
VCCIO6/VCCIO7	0	0	0	0
VCCIO10/VCCIO5	0	0	0	0
VCCIO10/VCCIO4	2	2	0	0
M0_VDDX/VCCX	0	0	0	0
VCCIO10/VCCX	0	0	2	8
M0_VDD_12/VCC_EXT	0	0	0	0
M0_VDD_12	0	0	0	0

Pin Type	GW5A-25			
	PG256C ^[1]	PG256C ^[2]	LQ100 ^[1]	PG256S ^[1]
M0_VDDX/VCCIO10/VCCX	0	0	0	0
M0_VDDA/M0_VDDD/VCC/VCCC	0	0	0	0
M0_VDDD	0	0	0	0
M0_VDDA	0	0	0	0
VQPS	1	1	0	1
VSS	32	32	8	25
MODE0	1	1	1	1
MODE1	1	1	1	1
MODE2	1	1	0	0
NC	0	0	1	0

Note!

[1] EV version.

[2] LV version.

[3] Single-ended/Differential I/O quantity includes CLK pins and download pins.

2.4.2 Quantity of GW5A-138 Pins

Pin Type	GW5A-138	
	UG324A	
Single-ended IO/ Differential pair/LVDS ^[1]	BANK0	0/0/0
	BANK1	0/0/0
	BANK2	50/24/24
	BANK3	0/0/0
	BANK4	50/24/24
	BANK5	50/24/24
	BANK6	50/24/24
	BANK7	10/4/4
	BANK10	12/6/6
	BANK11	0/0/0
Max. User I/O	222	
Differential Pair	106	
True LVDS Output	106	
VCCIO2	6	
VCCIO4	6	
VCCIO5	6	
VCCIO6	6	
VCCIO7	1	
VCC/VCCC	14	
VCC_REG	1	
VCCIO10	1	
VCCX/M0_VDDX/M1_VDDX	4	
VSS	48	
MODE0	1	
MODE1	1	
MODE2	1	
NC	5	

Note!

[1] Single-ended/Differential I/O quantity includes CLK pins and download pins.

2.5 I/O BANK Introduction

GW5A-25 has eight GPIO Banks. Bank10 is a JTAG Bank with four IOs, Bank11 is a Config Bank with one IO

GW5A-138 has six GPIO Banks (Bank2~7) and a Bank for configuration (Bank 10).

See [DS1103, GW5A series of FPGA Products Data Sheet](#) for details.

This manual provides the pin distribution view of GW5A series of FPGA products. For details, please refer to [Chapter 3 View of Pin Distribution](#). The I/O Banks that form GW5A series of FPGA products are marked with different colors.

Various symbols and colors are used for the user I/O, power, and ground. The various symbols and colors used for the various pins are defined as follows:

- "  " denotes the I/O in BANK0.
- "  " denotes the I/O in BANK1.
- "  " denotes the I/O in BANK2.
- "  " denotes the I/O in BANK3.
- "  " denotes the I/O in BANK4.
- "  " denotes the I/O in BANK5.
- "  " denotes the I/O in BANK6.
- "  " denotes the I/O in BANK7.
- "  " denotes the I/O in BANK10.
- "  " denotes the I/O in BANK11
- "  " denotes the DIO in MIPI and ADC
- "  " denotes VCC, VCCX, VCCIO, and the filling color does not change.
- "  " denotes VSS, and the filling color does not change.
- "  " denotes NC.

3 View of Pin Distribution

3.1 View of GW5A-25 Pin Distribution

3.1.1 View of MG121N Pin Distribution

Figure 3-1 View of GW5A-25 MG121N Pin Distribution (Top View)

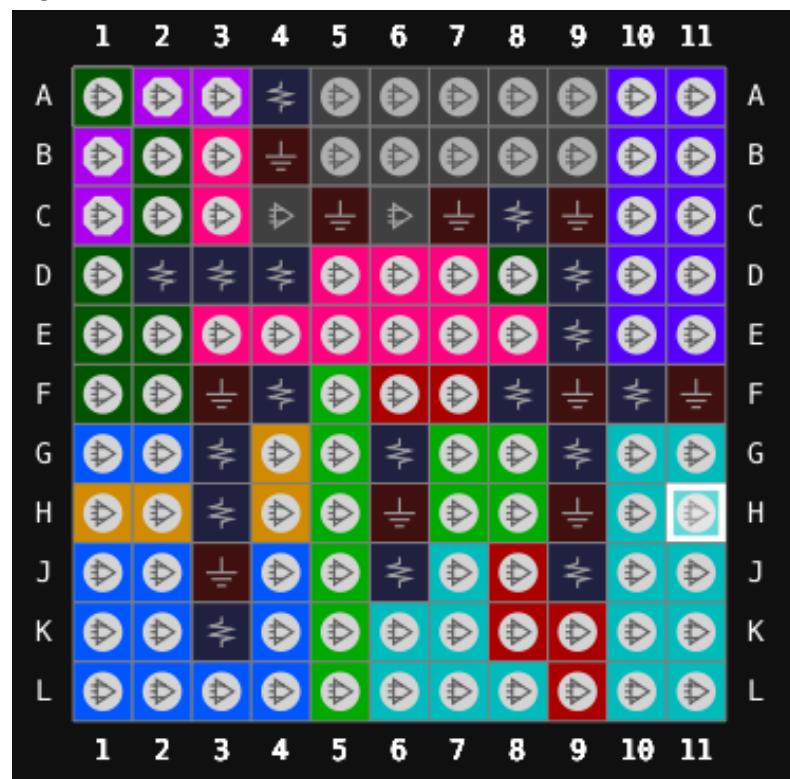


Table 3-1 Other Pins in GW5A-25 MG121N

VCC/VCCC	F8,F4,E9
VCCIO4	D4
VCCIO0/VCCIO1	J9
VCCIO2/VCCIO3	A4
VCCIO6/VCCIO7	F10

VCCIO10/VCCIO5	D2
M0_VDDX/VCCX	H3,G3,G9,G6
M0_VDD_12/VCC_EXT	K3
M0_VDDD	D9
M0_VDDA	C8
VCC_REG	J6
VQPS	D3
VSS	B4,C5,C7,C9,F11,F3,F9,H6,H9,J3

3.1.2 View of UG324S Pin Distribution

Figure 3-2 View of GW5A-25 UG324S Pin Distribution (Top View)



Table 3-2 Other Pins in GW5A-25 UG324S

VCCIO0/VCCIO1	B15,E10,D13,D7,B5,B10
VCCIO2/VCCIO3	G15,R17,J14,J17,M15,E17
VCCIO4/VCCIO5	P9,U4,R6,R12,U9,U14
VCCIO6/VCCIO7	J5,E2,G4,M4,J2,R2
VCC_EXT	J8,H9,K11,H11,K9,L10,M7,L8,M12,G7
VCCIO10/VCCX	P5,G10,K7,M9,E14,B1,E9,P14,B17,J12,P10,E5
VCC_REG	J10
VQPS	L11
VSS	A1,A18,B13,B7,C16,C3,D10,D5,E15,G12,G17,G2,G5,H10,H8,J11,J15,J4,J9,K10,K8,L9,M17,M2,M6,N13,R1,R14,R18,R4,R9,T16,U12,U6,V1,V18

3.1.3 View of UG256C (EV Version) Pin Distribution

Figure 3-3 View of GW5A-25 UG256C (EV Version) Pin Distribution (Top View)

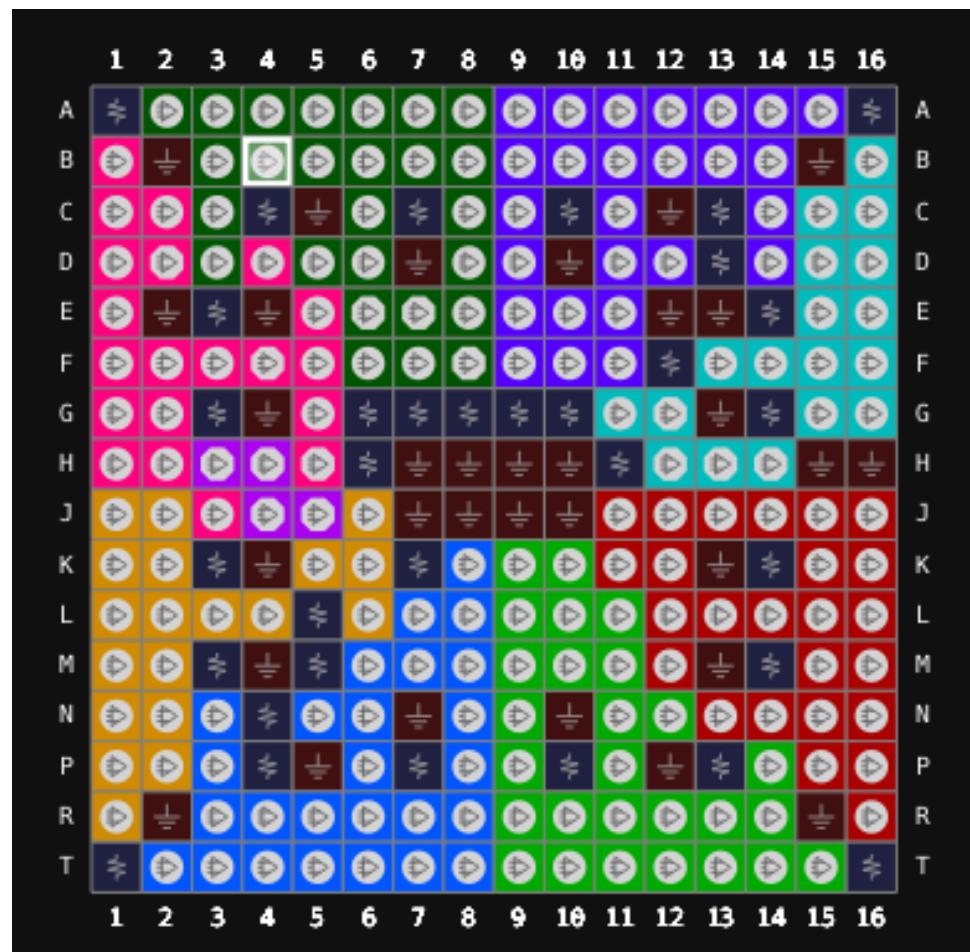


Table 3-3 Other Pins in GW5A-25 UG256C (EV Version)

VCCIO0	M14,K14
VCCIO1	P10,P13,T16
VCCIO2	P4,P7,T1
VCCIO3	K3,M3
VCCIO5	C7,A1,C4
VCCIO6	C13,A16,C10
VCCIO7	G14,E14
VCCIO10/VCCIO4	G3,E3
VCC_EXT	H11,H6,N4,G8,G7,D13,G10,K7,G6
VCC_REG	G9
VCCX	F12,L5
VQPS	L11
VSS	E12,H7,H8,H9,H10,J7,J8,J9,J10,B2,B15,C5,C12,D7,D10,E4,E13,G4,G13,K4,K13,M4,M13,N7,N10,P5,P12,R2,R15,E2,H16,H15

3.1.4 View of UG256C (LV Version) Pin Distribution

Figure 3-4 View of GW5A-25 UG256C (LV Version) Pin Distribution (Top View)

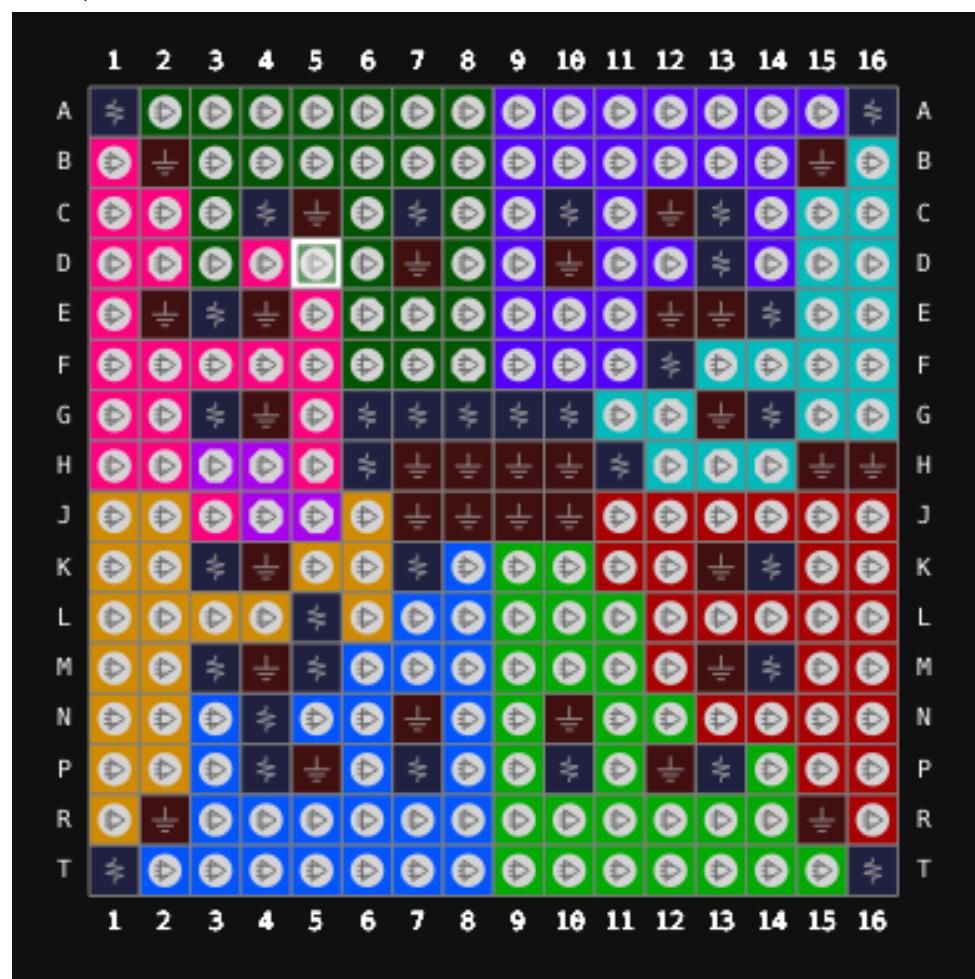


Table 3-4 Other Pins in GW5A-25 UG256C (LV Version)

VCCIO0	M14,K14
VCCIO1	P10,P13,T16
VCCIO2	P4,P7,T1
VCCIO3	K3,M3
VCCIO5	C7,A1,C4
VCCIO6	C13,A16,C10
VCCIO7	G14,E14
VCCIO10/VCCIO4	G3,E3
VCC/VCCC	H11,H6,N4,G8,G7,D13,G10,K7,G6
VCC_REG	J10
VCCX	F12,L5
VQPS	L11
VSS	E12,H7,H8,H9,H10,J7,J8,J9,J10,B2,B15,C5,C12,D7,D10,E4,E13,G4,G13,K4,K13,M4,M13,N7,N10,P5,P12,R2,R15,E2,H16,H15

3.1.5 View of PG256C (EV Version) Pin Distribution

Figure 3-5 View of GW5A-25 PG256C (EV Version) Pin Distribution (Top View)

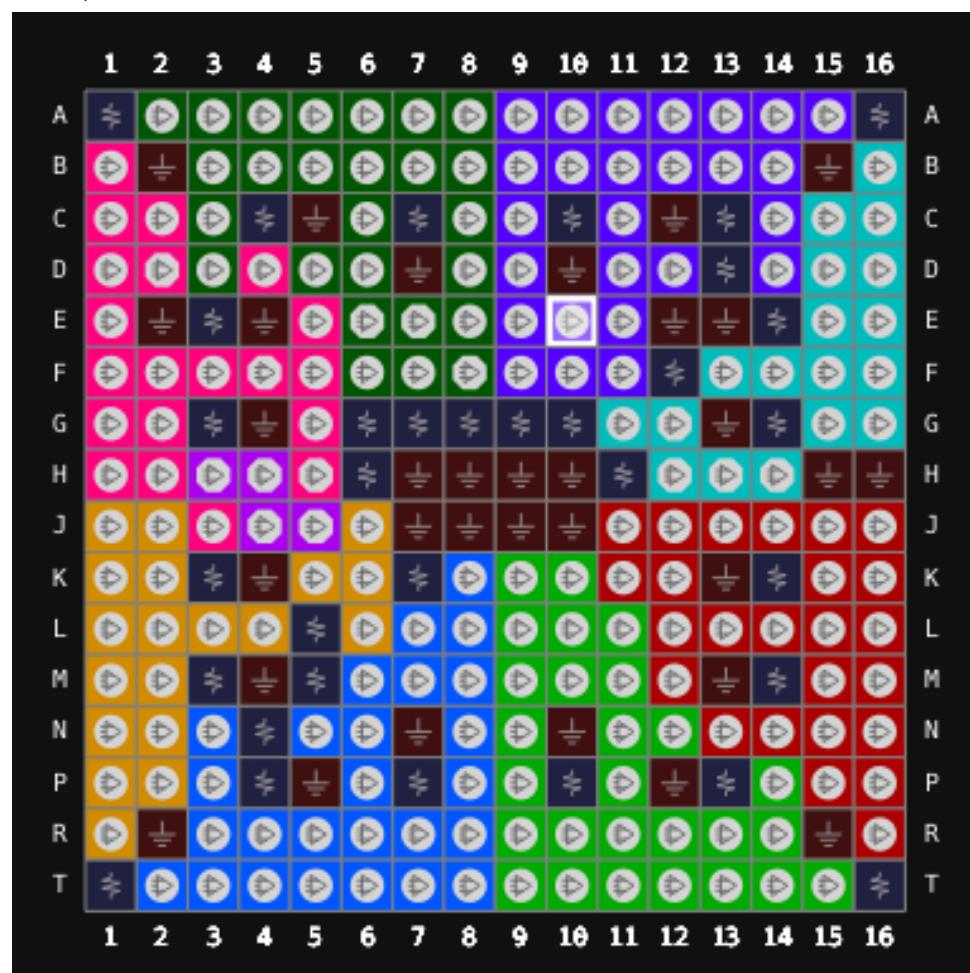


Table 3-5 Other Pins in GW5A-25 PG256C (EV Version)

VCCIO0	M14,K14
VCCIO1	P10,P13,T16
VCCIO2	P4,P7,T1
VCCIO3	K3,M3
VCCIO5	C7,A1,C4
VCCIO6	C13,A16,C10
VCCIO7	G14,E14
VCCIO10/VCCIO4	G3,E3
VCC_EXT	H11,H6,N4,G8,G7,D13,G10,K7,G6
VCC_REG	J10
VCCX	F12,L5
VQPS	L11
VSS	E12,H7,H8,H9,H10,J7,J8,J9,J10,B2,B15,C5,C12,D7,D10,E4,E13,G4,G13,K4,K13,M4,M13,N7,N10,P5,P12,R2,R15,E2,H16,H15

3.1.6 View of PG256C (LV Version) Pin Distribution

Figure 3-6 View of GW5A-25 PG256C (LV Version) Pin Distribution (Top View)

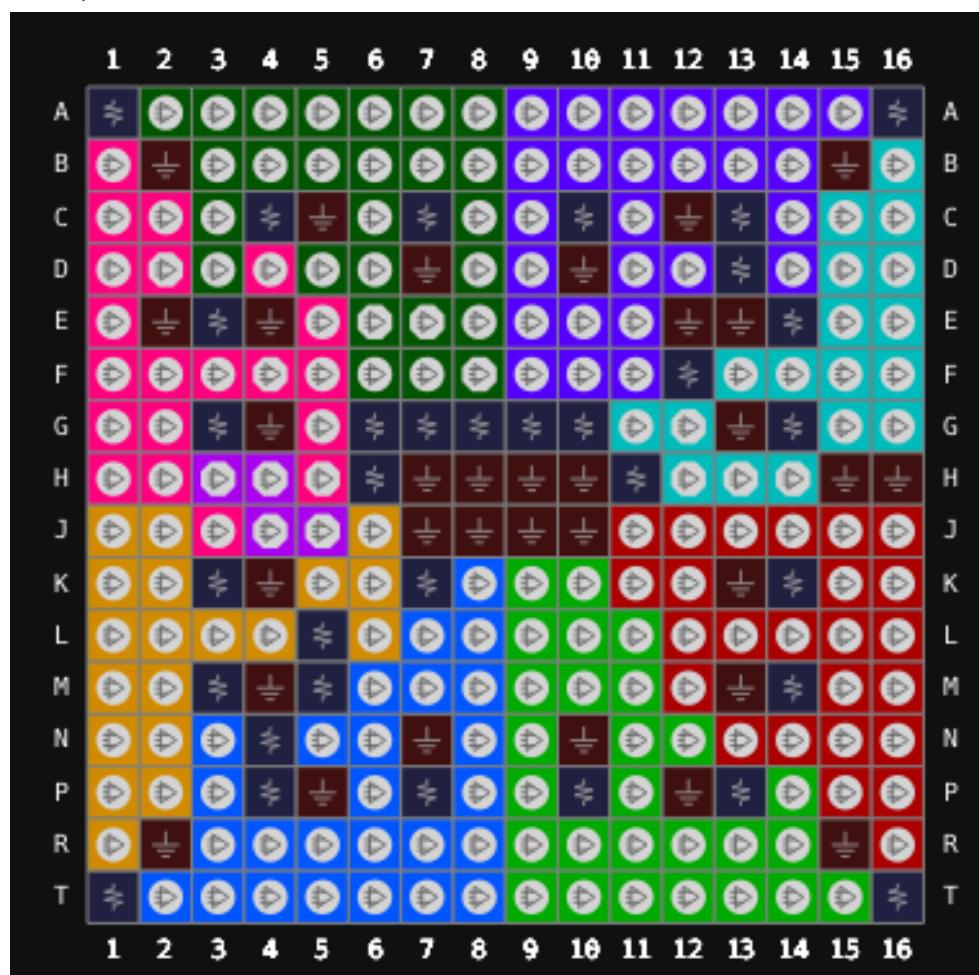


Table 3-6 Other Pins in GW5A-25 PG256C (LV Version)

VCCIO0	M14,K14
VCCIO1	P10,P13,T16
VCCIO2	P4,P7,T1
VCCIO3	K3,M3
VCCIO5	C7,A1,C4
VCCIO6	C13,A16,C10
VCCIO7	G14,E14
VCCIO10/VCCIO4	G3,E3
VCC/VCCC	H11,H6,N4,G8,G7,D13,G10,K7,G6
VCC_REG	J10
VCCX	F12,L5
VQPS	L11
VSS	E12,H7,H8,H9,H10,J7,J8,J9,J10,B2,B15,C5,C12,D7,D10,E4,E13,G4,G13,K4,K13,M4,M13,N7,N10,P5,P12,R2,R15,E2,H16,H15

3.1.7 View of UG324 Pin Distribution

Figure 3-7 View of GW5A-25 UG324 Pin Distribution (Top View)

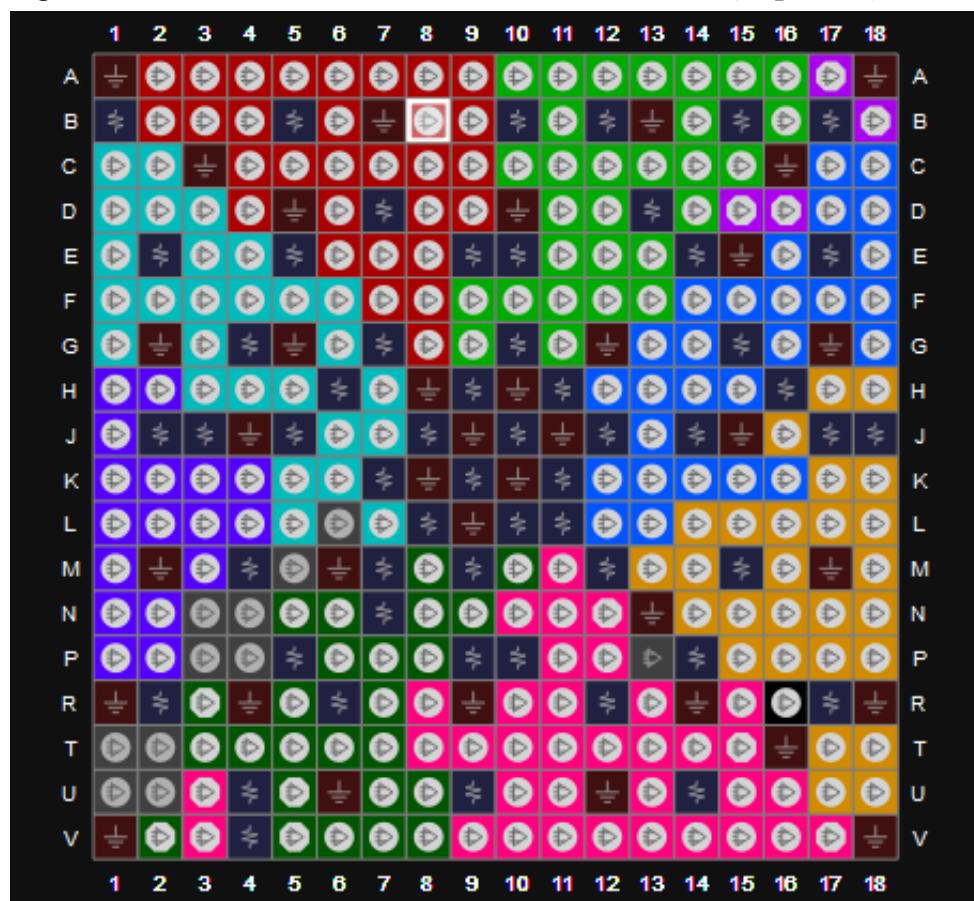


Table 3-7 Other Pins in GW5A-25 PG256C

VCCIO0/VCCIO1	B15,B10,E10,B5,D7,D13
VCCIO2/VCCIO3	J17,R17,E17,M15,G15,J14
VCCIO4/VCCIO5	U14,P9,U9,U4,R12,R6
VCCIO6/VCCIO7	R2,E2,J2,J5,G4,M4
M0_VDDA/M0_VDDD/VCC/VCCC	H9,G7,H11,J8,L8,M7,M12,L10,K9,K11
M0_VDDX/VCCIO10/VCCX	P5,M9,P10,E9,B1,E5,P14,B17,E14,J12,K7,G10
VQPS	L11
VCC_REG	J10
M0_VDD_12	V4
VCC_EXT	H6,J3,J18,B12,H16,N7
VSS	A18,B13,B7,C16,C3,D10,D5,E15,G12,G17,G2,G5, H10,H8,J11,J15,J4,J9,K10,K8,A1,L9,M17,M2,M6,N 13,R1,R14,R18,R4,R9,T16,U12,U6,V1,V18

3.1.8 View of MG196S (EV Version) Pin Distribution

Figure 3-8 View of GW5A-25 MG196S (EV Version) Pin Distribution (Top View)



Table 3-8 Other Pins in GW5A-25 MG196S (EV Version)

VCCIO0	C4,C5
VCCIO1	C10,C9
VCCIO2	E12,G11,D12
VCCIO3	G12,K12,K11
VCCIO4	M9,M10
VCCIO5	M6,M5
VCCIO6	G3,E3,E4
VCCIO7	K3,H3,K4
VCCIO10/VCCX	E7,L7,H5,G10,K7,D7,G9,H6
VQPS	L11
VCC_REG	J6
VCC_EXT	E9,K5,K6,E5,F6,K9,E10,K10,F5,F9,F10,J5,E6,J9
VSS	A1,A14,C2,C3,C6,C7,D10,D5,D6,D9,E11,E8,F7,F8,G5,G6,G7,G8,H10,H4,H7,H8,H9,J10,J7,J8,K8,L10,L3,L5,L6,L9,M11,M3,M7,P1,P14,G4

3.1.9 View of MG196S (LV Version) Pin Distribution

Figure 3-9 View of GW5A-25 MG196S (LV Version) Pin Distribution (Top View)

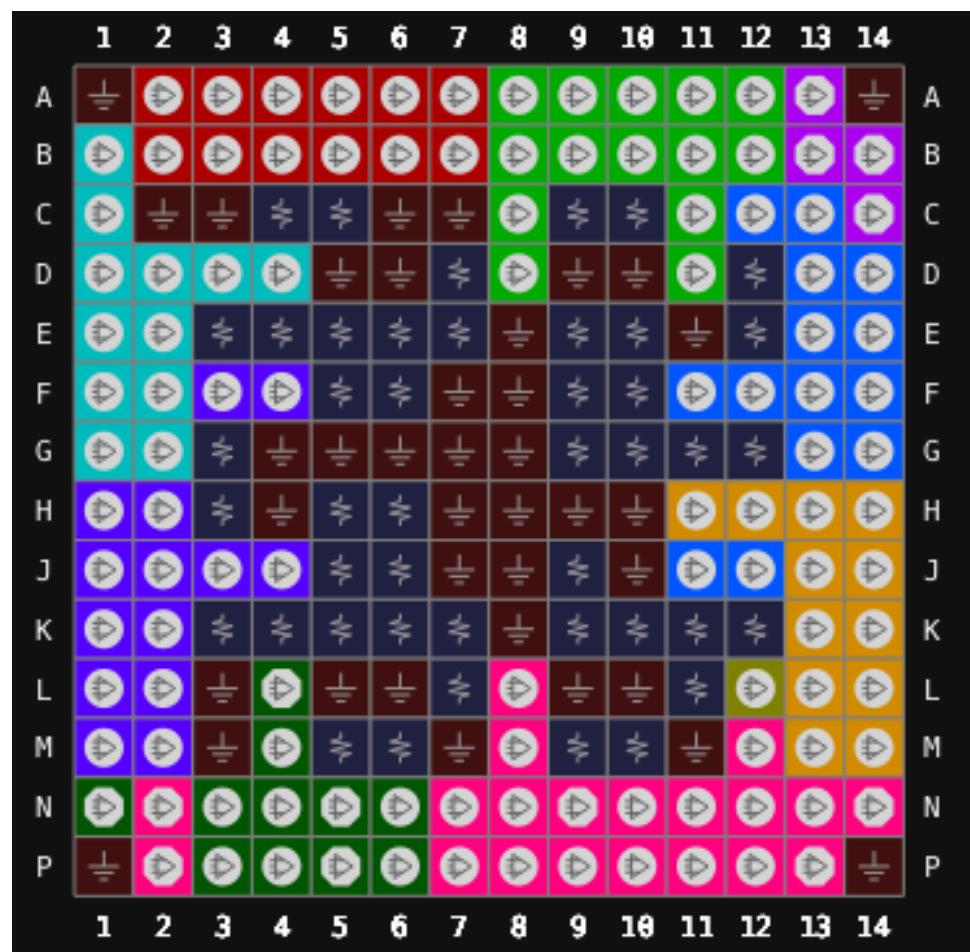


Table 3-9 Other Pins in GW5A-25 MG196S (LV Version)

VCCIO0	C4,C5
VCCIO1	C10,C9
VCCIO2	E12,G11,D12
VCCIO3	G12,K12,K11
VCCIO4	M9,M10
VCCIO5	M6,M5
VCCIO6	G3,E3,E4
VCCIO7	K3,H3,K4
VCCIO10/VCCX	E7,L7,H5,G10,K7,D7,G9,H6
VQPS	L11
VCC_REG	J6
VCC/VCCC	E9,K5,K6,E5,F6,K9,E10,K10,F5,F9,F10,J5,E6,J9
VSS	A1,A14,C2,C3,C6,C7,D10,D5,D6,D9,E11,E8,F7,F8,G5,G6,G7,G8,H10,H4,H7,H8,H9,J10,J7,J8,K8,L10,L3,L5,L6,L9,M11,M3,M7,P1,P14,G4

3.1.10 View of UG225S (EV Version) Pin Distribution

Figure 3-10 View of GW5A-25 UG225S (EV Version) Pin Distribution (Top View)



Table 3-10 Other Pins in GW5A-25 UG225S (EV Version)

VCCIO0	B8,B4
VCCIO1	D9,B12
VCCIO2	H14,D14
VCCIO3	M14,J12
VCCIO4	P8,P12
VCCIO5	M7,P4
VCCIO6	M2,H2
VCCIO7	G4,D2
VCCIO10/VCCX	F7,M12,E12,J6,B1,K9,G10,L4
VQPS	L11
VCC_REG	H7
VCC_EXT	K7,G8,H9,J8,F9,J10
VSS	A1,A15,B10,B6,C13,C3,E11,F14,F2,F6,G7,G9,H8,J7,J9,K14,K2,K6,N13,N3,P10,P6,R1,R15

3.1.11 View of UG225S (LV Version) Pin Distribution

Figure 3-11 View of GW5A-25 UG225S (LV Version) Pin Distribution (Top View)



Table 3-11 Other Pins in GW5A-25 UG225S (LV Version)

VCCIO0	B8,B4
VCCIO1	D9,B12
VCCIO2	H14,D14
VCCIO3	M14,J12
VCCIO4	P8,P12
VCCIO5	M7,P4
VCCIO6	M2,H2
VCCIO7	G4,D2
VCCIO10/VCCX	F7,M12,E12,J6,B1,K9,G10,L4
VQPS	L11
VCC_REG	H7
VCC/VCCC	K7,G8,H9,J8,F9,J10
VSS	A1,A15,B10,B6,C13,C3,E11,F14,F2,F6,G7,G9,H8,J7,J9,K14,K2,K6,N13,N3,P10,P6,R1,R15

3.1.12 View of LQ100 (EV Version) Pin Distribution

Figure 3-12 View of GW5A-25 LQ100 (EV Version) Pin Distribution (Top View)

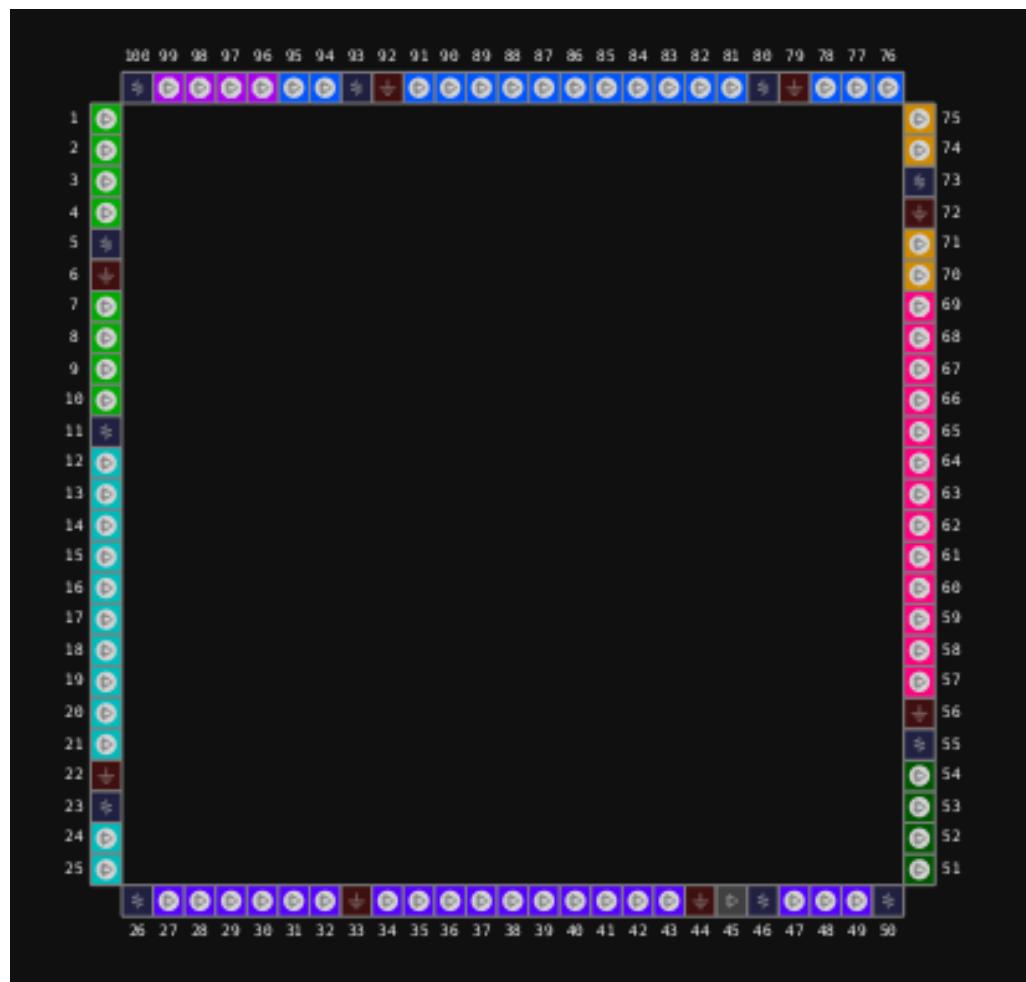


Table 3-12 Other Pins in GW5A-25 LQ100 (EV Version)

VCCIO1	5
VCCIO2	80
VCCIO6	46
VCCIO7	23
VCCIO10/VCCX	26,100
VCCIO3/VCCIO4/VCCIO5	73,55
VCC_EXT/VCC_REG/VCCIO0	93,50,11
VSS	6,22,33,44,56,72,79,92

3.1.13 View of PG256S (EV Version) Pin Distribution

Figure 3-13 View of GW5A-25 PG256S (EV Version) Pin Distribution (Top View)

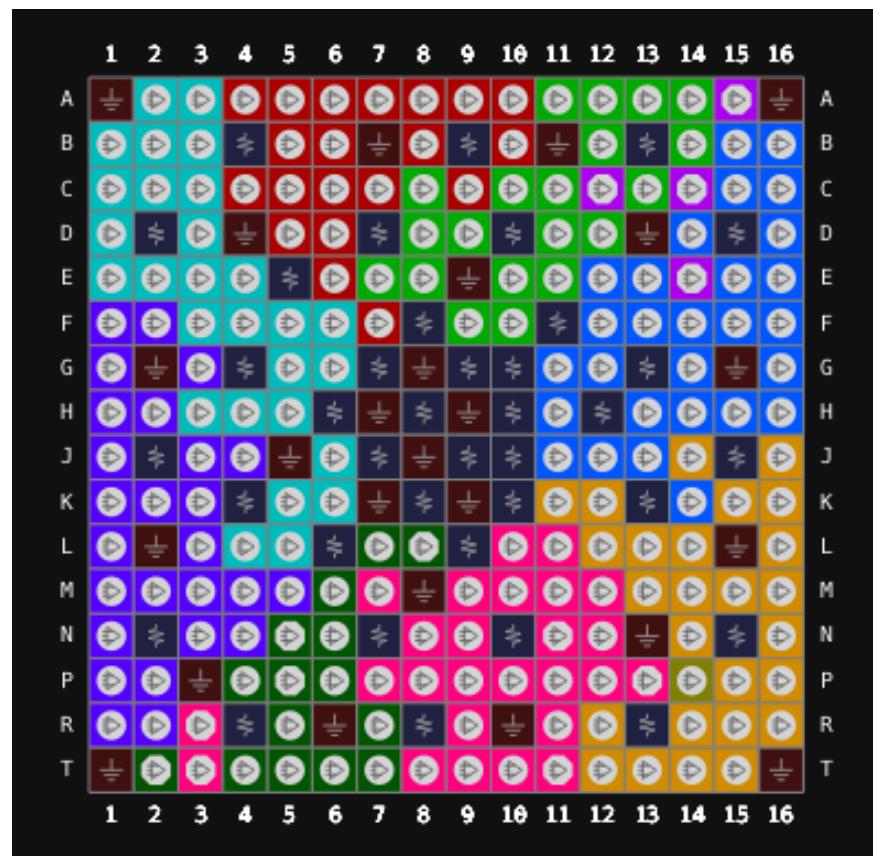


Table 3-13 Other Pins in GW5A-25 PG256S (EV Version)

VCCIO0	D7,B4
VCCIO1	B13,D10,B9
VCCIO2	J15,D15,G13
VCCIO3	K13,N15,R13
VCCIO4	N10,R8
VCCIO5	N7,R4
VCCIO6	N2,K4,J2
VCCIO7	D2,G4
VCCIO10/VCCX	G10,F11,J10,H6,L6,F8,L9,E5
VCC_REG	H8
VQPS	H12
VCC_EXT	J9,J7,G9,H10,G7,K8,K10
VSS	A1,A16,B11,B7,D13,D4,E9,G15,G2,G8,H7,H9,J5,J8,K7,K9,L15,L2,M8,N13,P3,R10,R6,T1,T16

3.2 View of GW5A-138 Pin Distribution

3.2.1 View of UG324A Pin Distribution

Figure 3-14 View of GW5A-138 UG324A Pin Distribution (Top View)



Table 3-14 Other Pins in GW5A-25 PG256C

VCCIO2	C13,H18,G15,K14,A17,D16
VCCIO4	N13,U15,T12,P16,L17,V18
VCCIO5	K4,V8,T2,N3,U5P6
VCCIO6	D6,F2,G5,A7,J1,C3
VCCIO7	B10
VCCIO10	R9
VCC/VCCC	N7,F8,G7,L7,H8,L11,N9,M10,J11,K8,J7,G9,N11,M8
VCC_REG	H10
VCCX/M0_VDDX/M1_VDDX	H12,K12,F12,M12
VSS	A12,A2,B15,B5,C18,C8,D11,D1,E14,E4,F17,F11,F9,F7,G12,G10,G8,H13,H11,H7,H3,J16,J12,J8,J6,K11,K7,L12,L8,L2,M15,M11,M9,M7,M5,N18,N12,N10,N8,P1,R14,R4,T17,T7,U10,V13,H9,V3

4 Package Diagram

4.1 MG121N Package Outline (6mm x 6mm, GW5A-25)

Figure 4-1 Package Outline MG121N

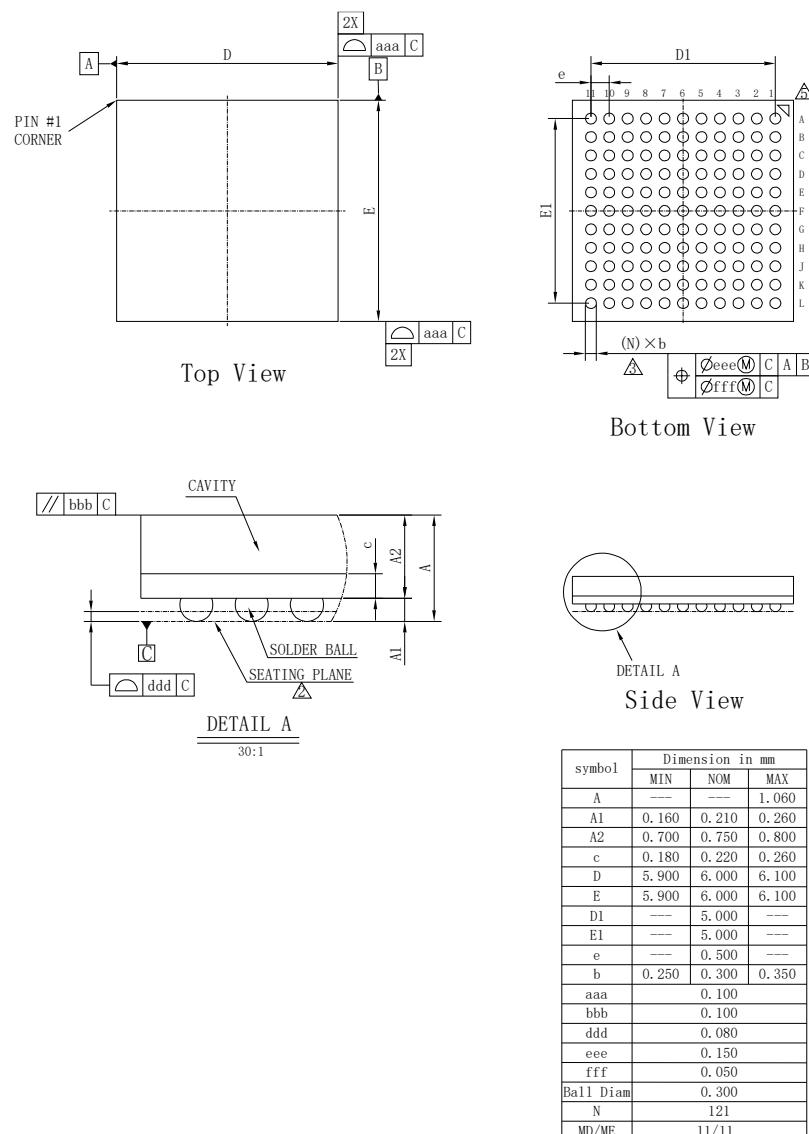
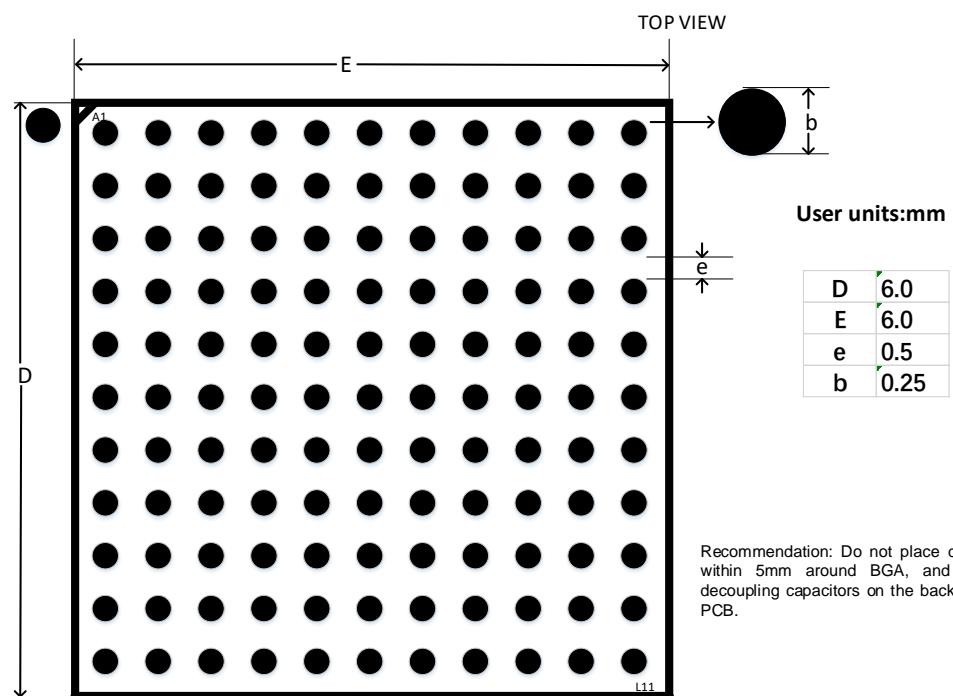


Figure 4-2 Recommended PCB Layout MG121N

4.2 UG324S Package Outline (15mm x 15mm, GW5A-25)

Figure 4-3 Package Outline UG324S

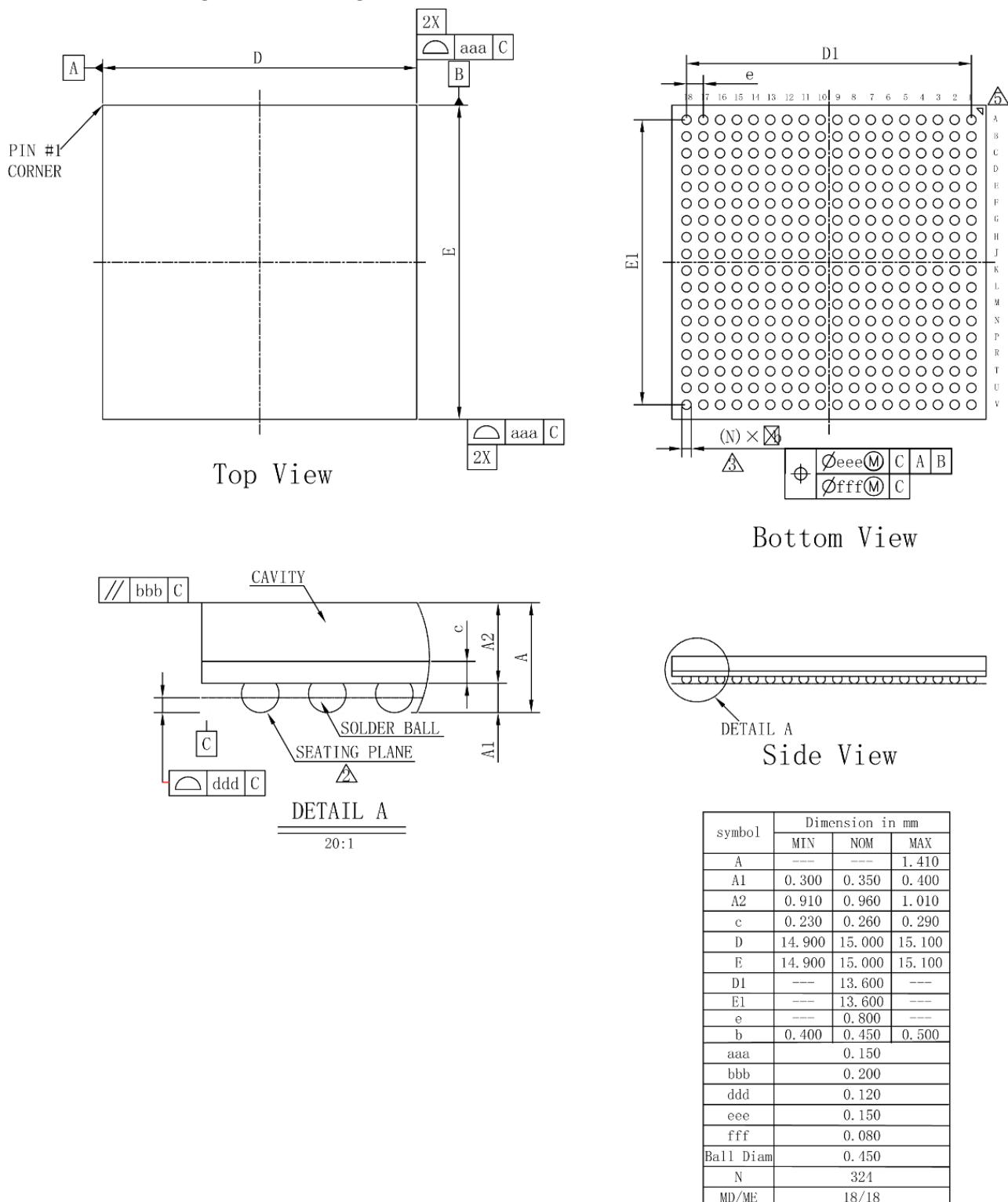
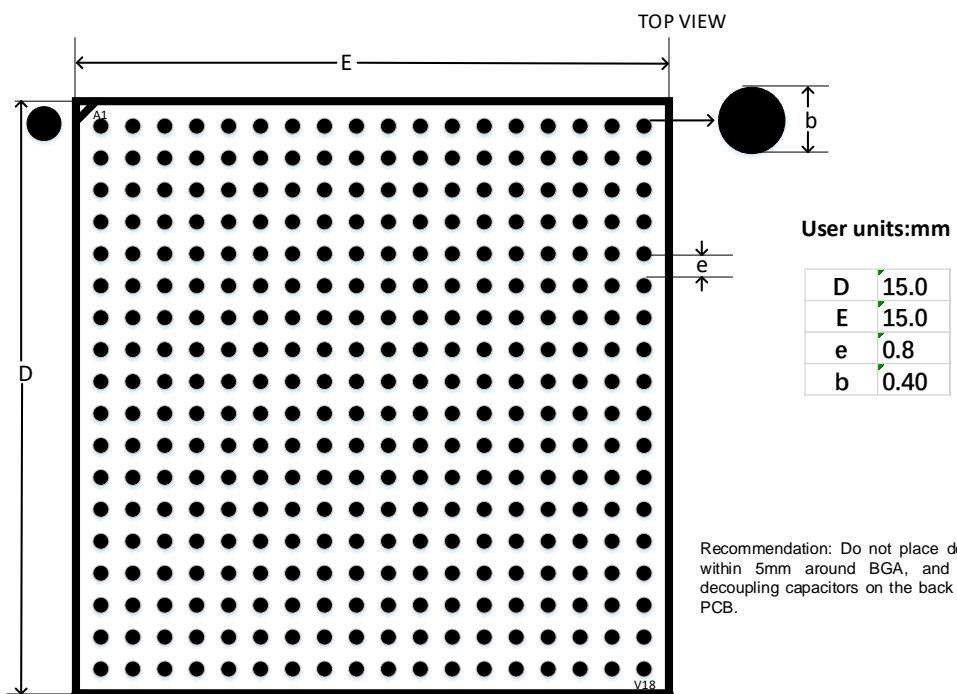


Figure 4-4 Recommended PCB Layout UG324S

4.3 UG256C Package Outline (14mm x 14mm, GW5A-25)

Figure 4-5 Package Outline UG256C

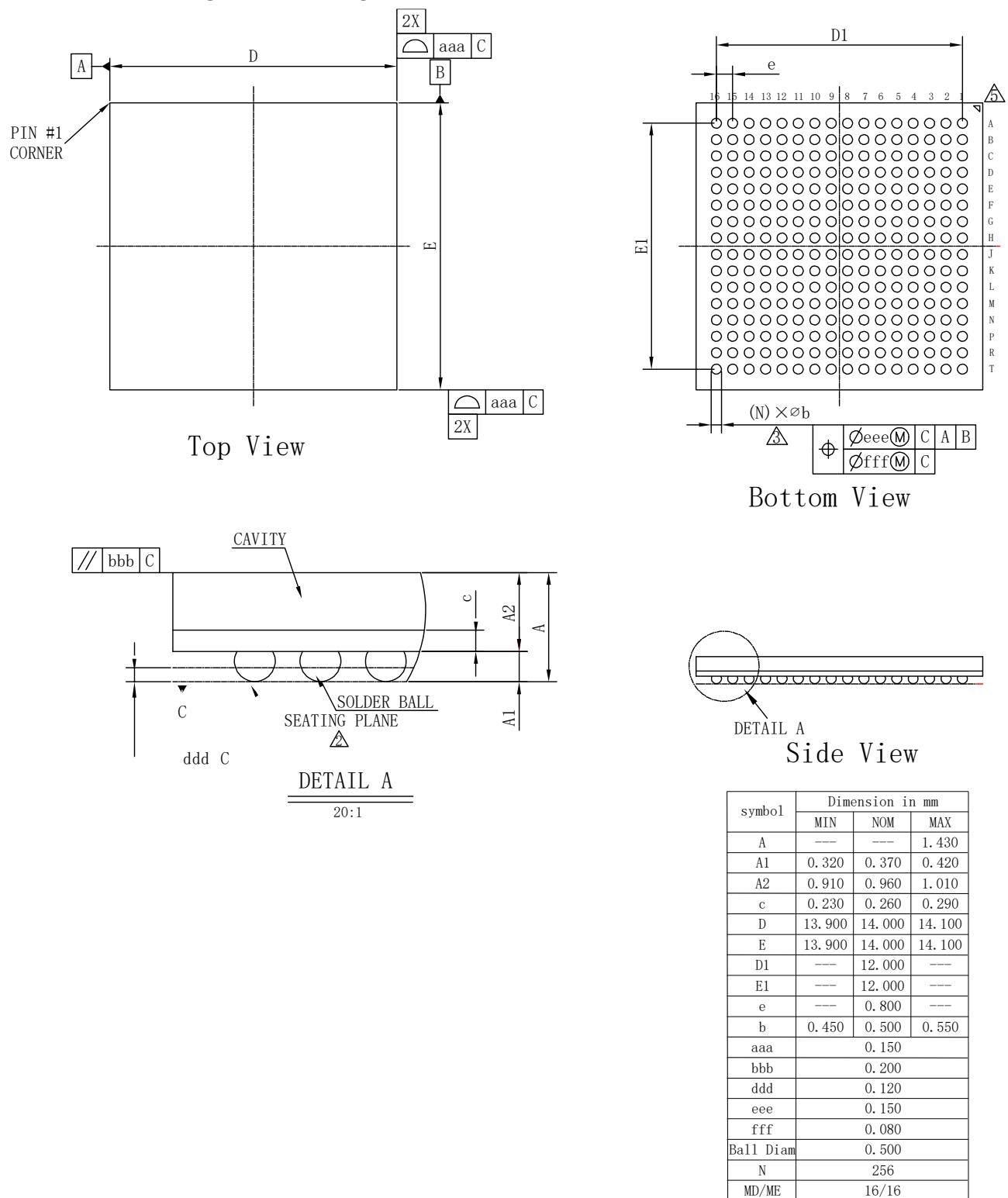
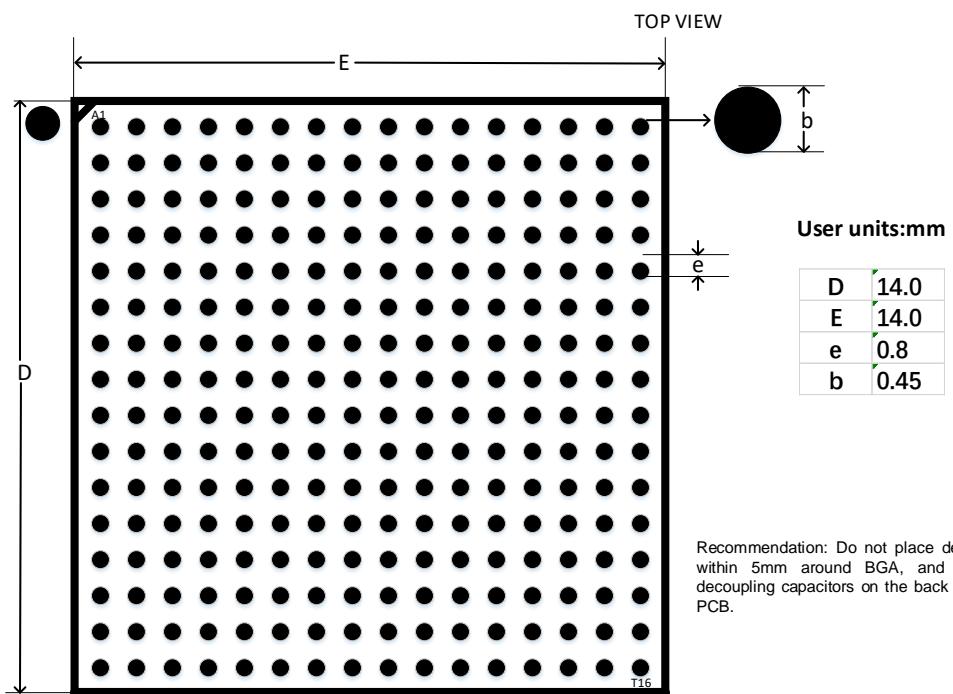


Figure 4-6 Recommended PCB Layout UG256C

4.4 PG256C Package Outline (17mm x 17mm, GW5A-25)

Figure 4-7 Package Outline PG256C

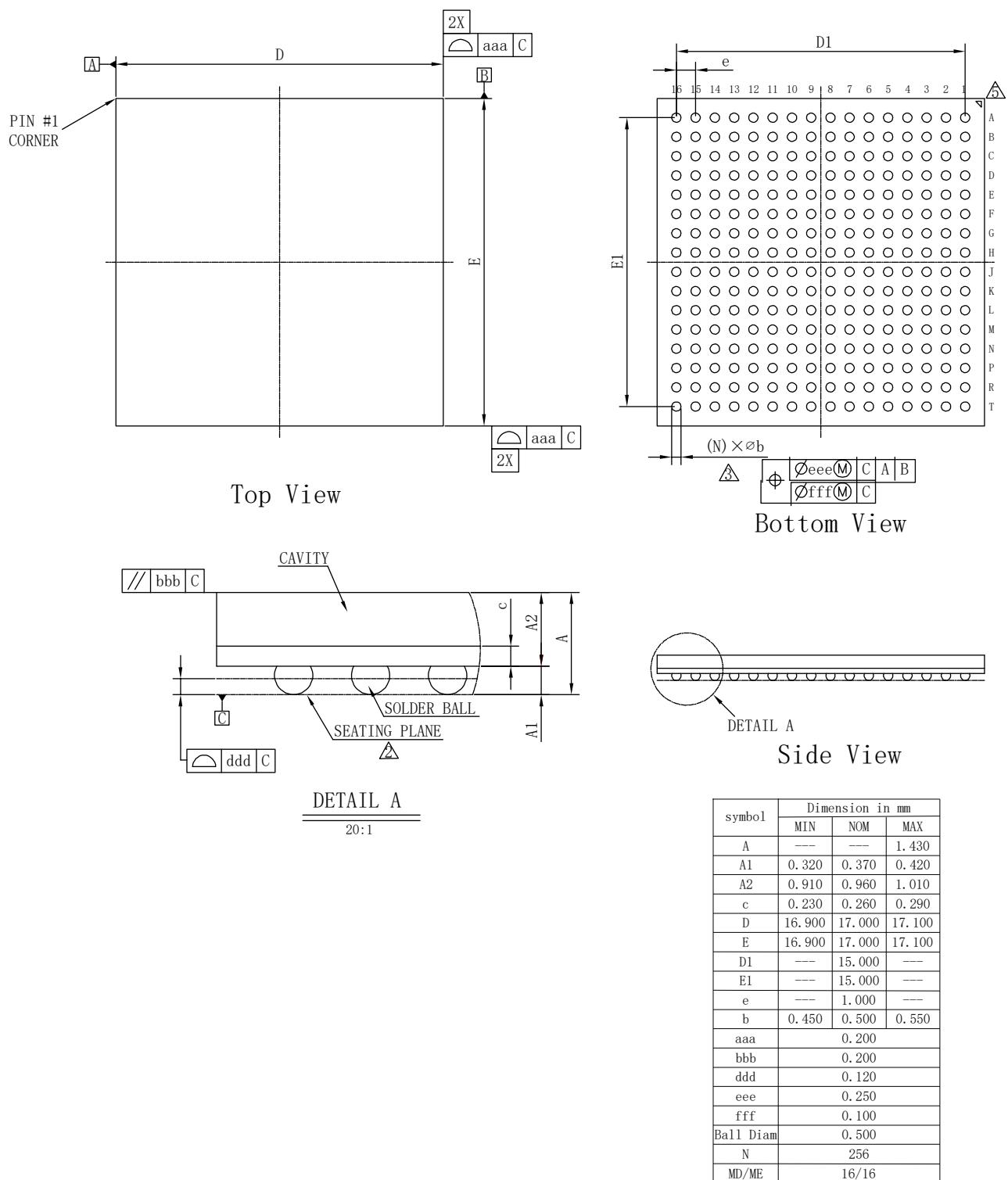
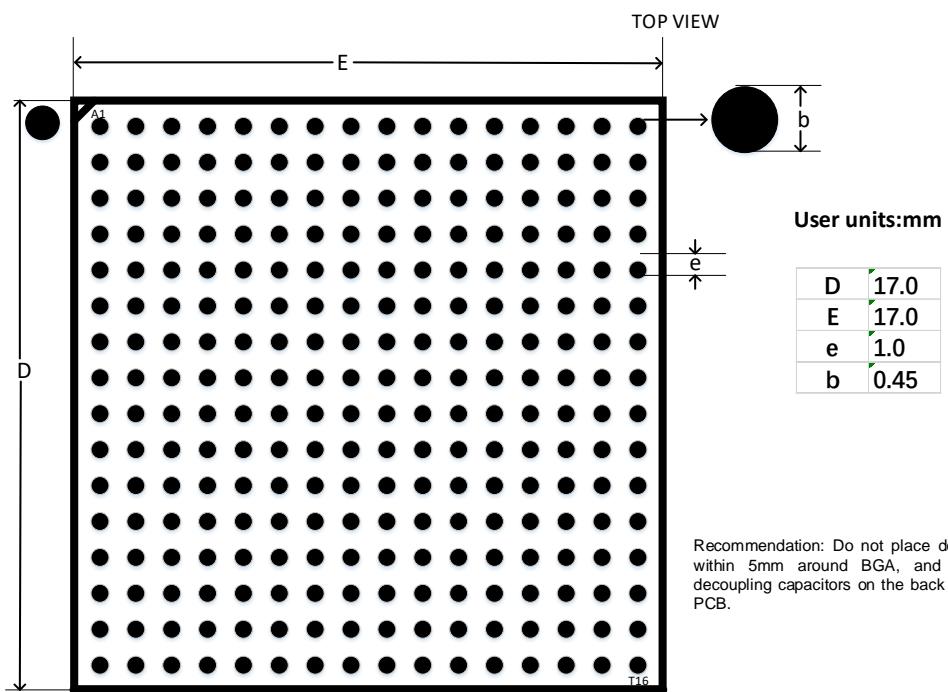
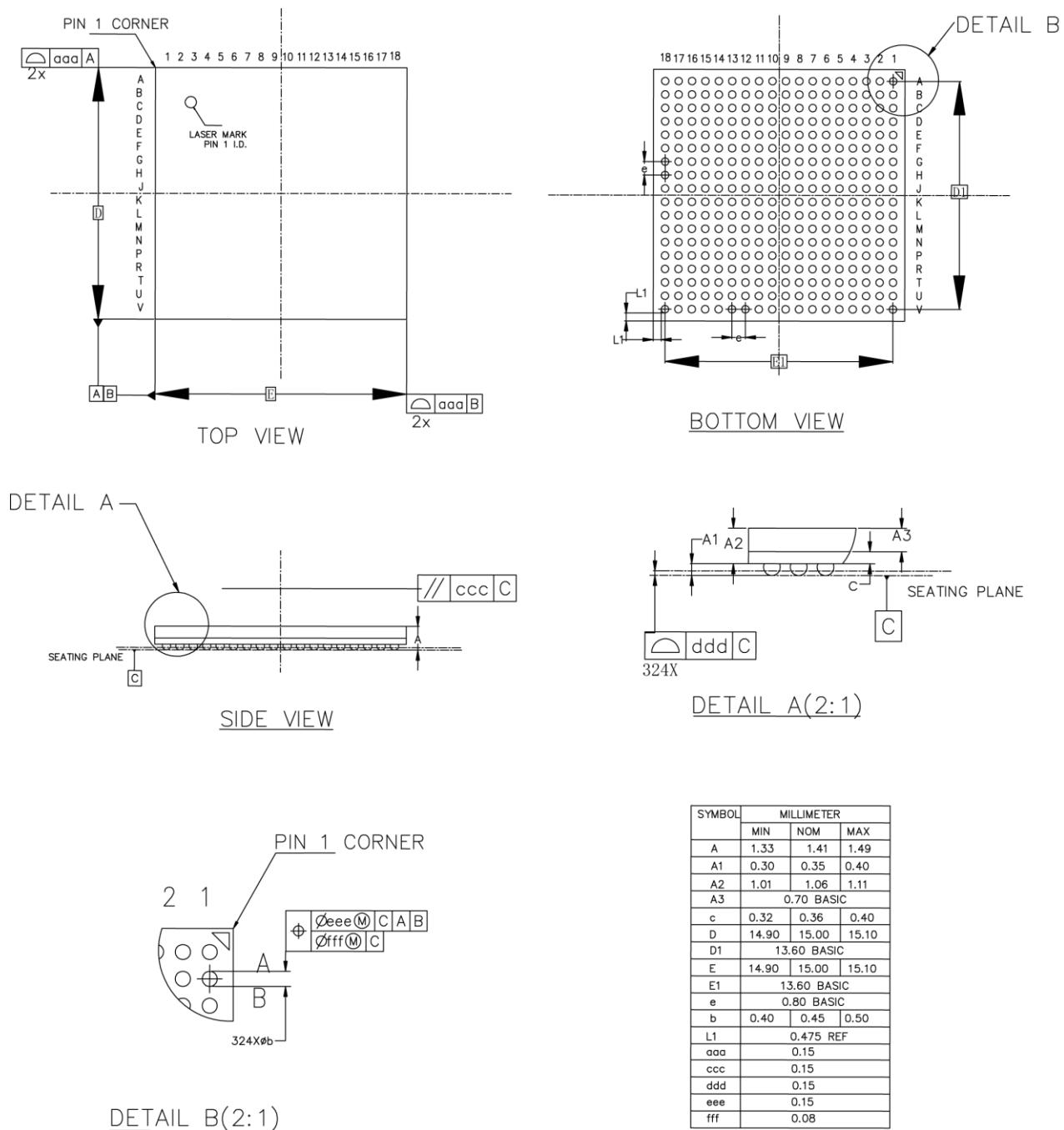


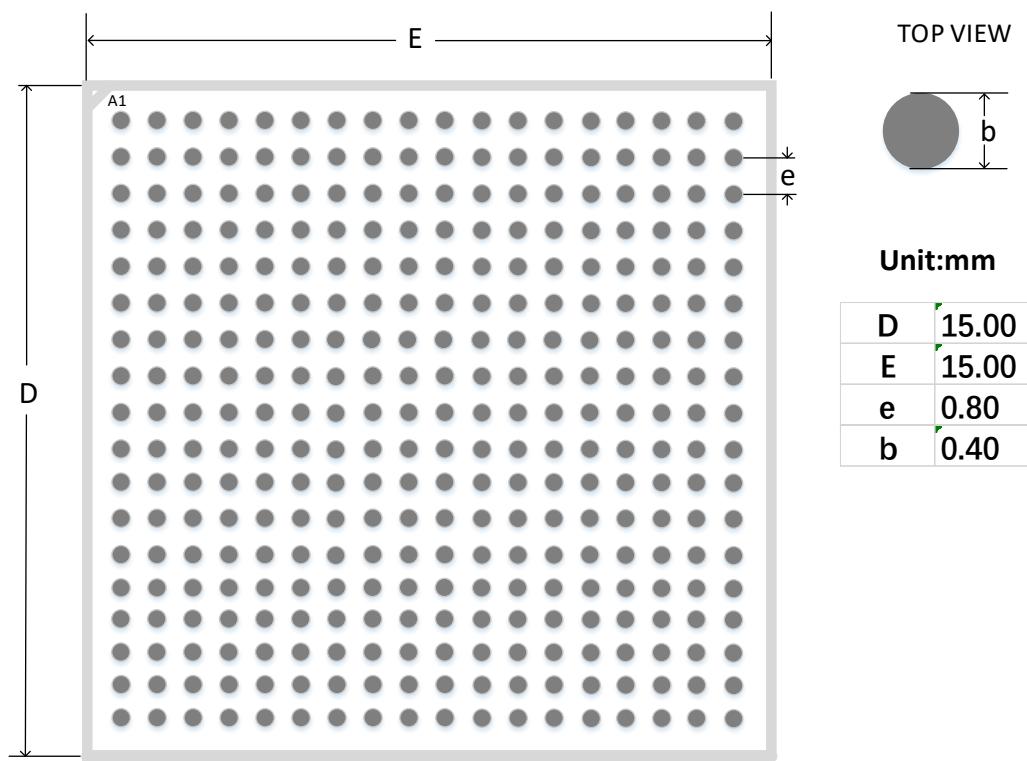
Figure 4-8 Recommended PCB Layout PG256C

4.5 UG324 Package Outline (15mm x 15mm, GW5A-25)

Figure 4-9 Package Outline UG324



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.33	1.41	1.49
A1	0.30	0.35	0.40
A2	1.01	1.06	1.11
A3	0.70 BASIC		
c	0.32	0.36	0.40
D	14.90	15.00	15.10
D1	13.60 BASIC		
E	14.90	15.00	15.10
E1	13.60 BASIC		
e	0.80 BASIC		
b	0.40	0.45	0.50
L1	0.475 REF		
aaa	0.15		
ccc	0.15		
ddd	0.15		
eee	0.15		
fff	0.08		

Figure 4-10 Recommended PCB Layout UG324

4.6 UG324A Package Outline (15mm x 15mm, GW5A-138)

Figure 4-11 Package Outline UG324A

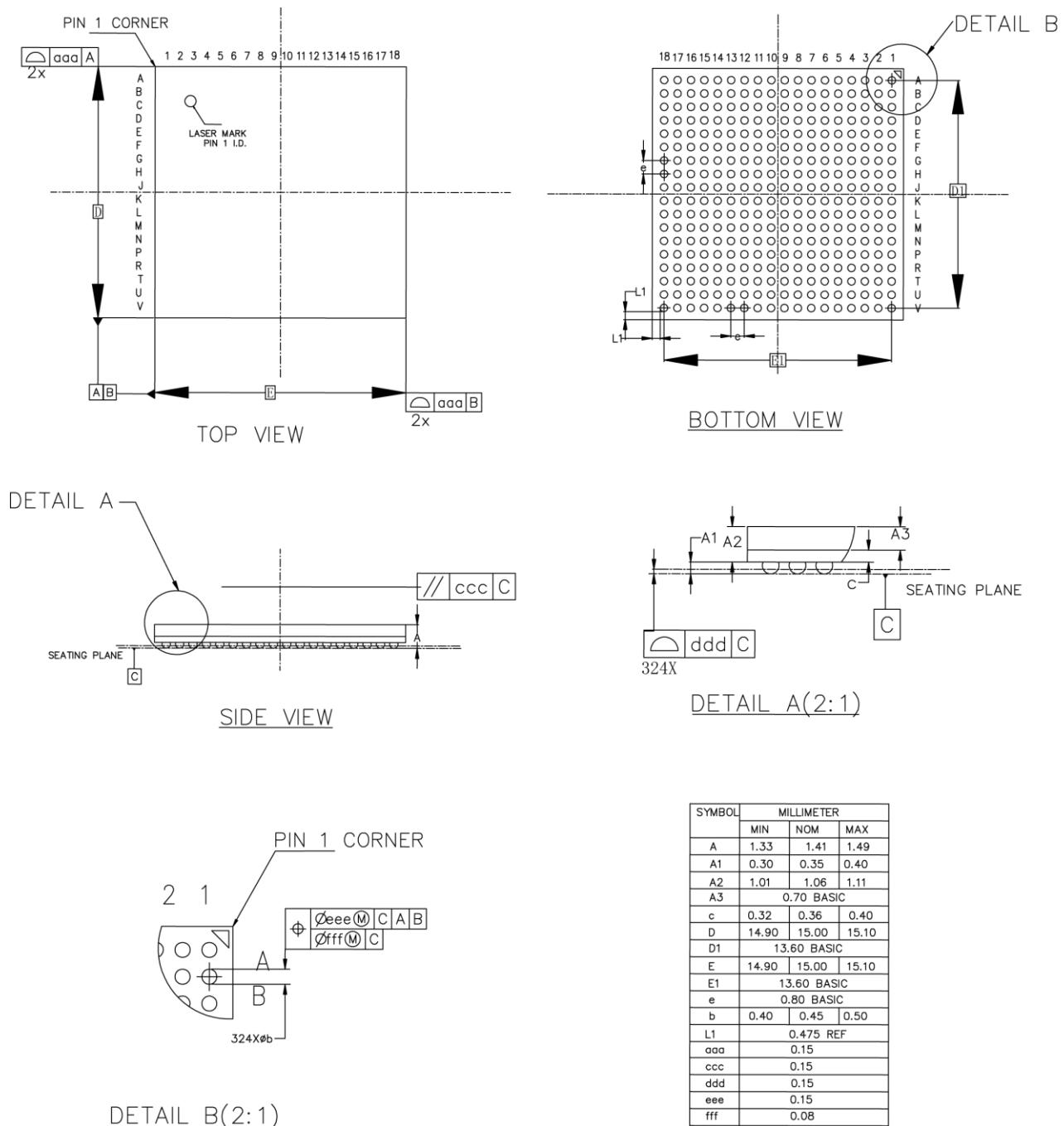
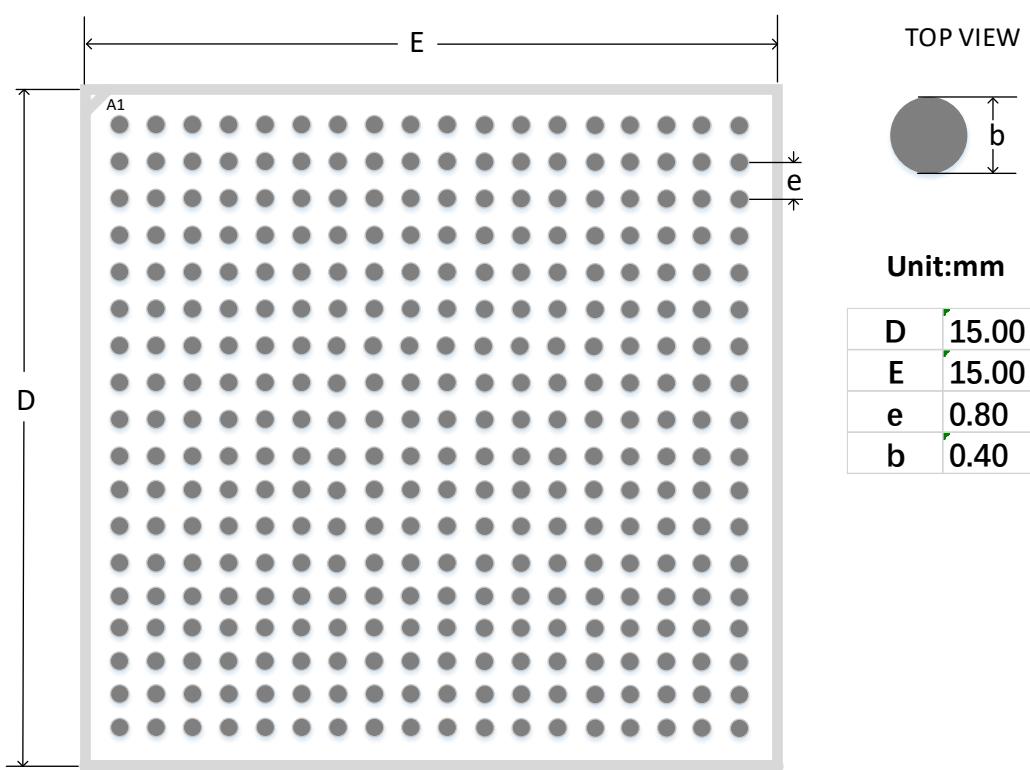
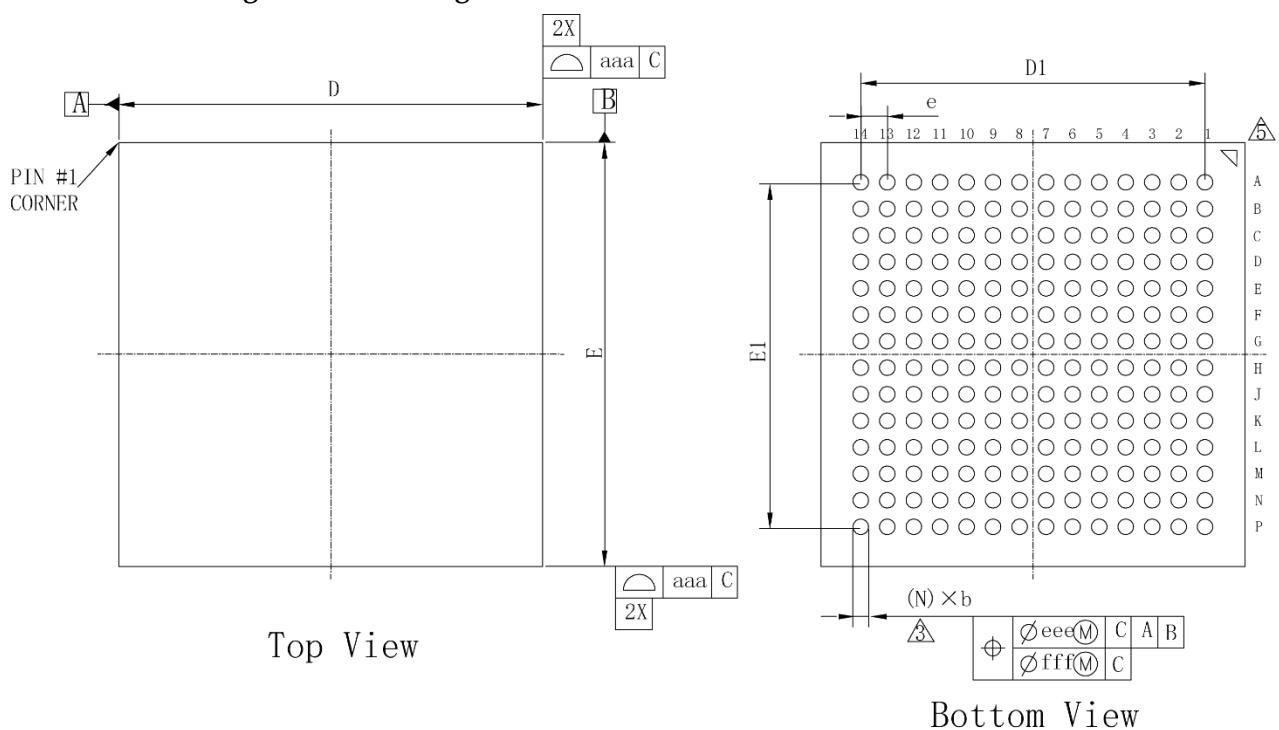


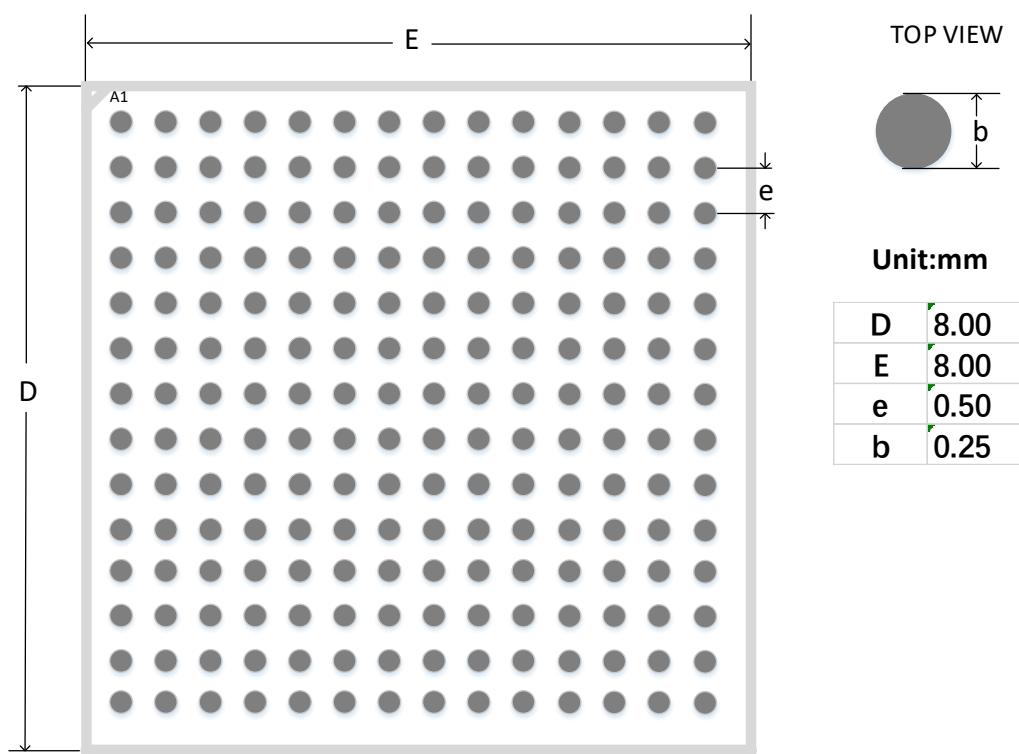
Figure 4-12 Recommended PCB Layout UG324A

4.7 MG196S Package Outline (8mm x 8mm, GW5A-25)

Figure 4-13 Package Outline MG196S



symbol	Dimension in mm		
	MIN	NOM	MAX
A	---	---	1.180
A1	0.160	0.210	0.260
A2	0.820	0.870	0.920
c	0.180	0.220	0.260
D	7.900	8.000	8.100
E	7.900	8.000	8.100
D1	---	6.500	---
E1	---	6.500	---
e	---	0.500	---
b	0.250	0.300	0.350
aaa	0.100		
bbb	0.100		
ddd	0.080		
eee	0.150		
fff	0.050		
Ball Diam		0.300	
N		196	
MD/ME		14/14	

Figure 4-14 Recommended PCB Layout MG196S

4.8 UG225S Package Outline (13mm x 13mm, GW5A-25)

Figure 4-15 Package Outline UG225S

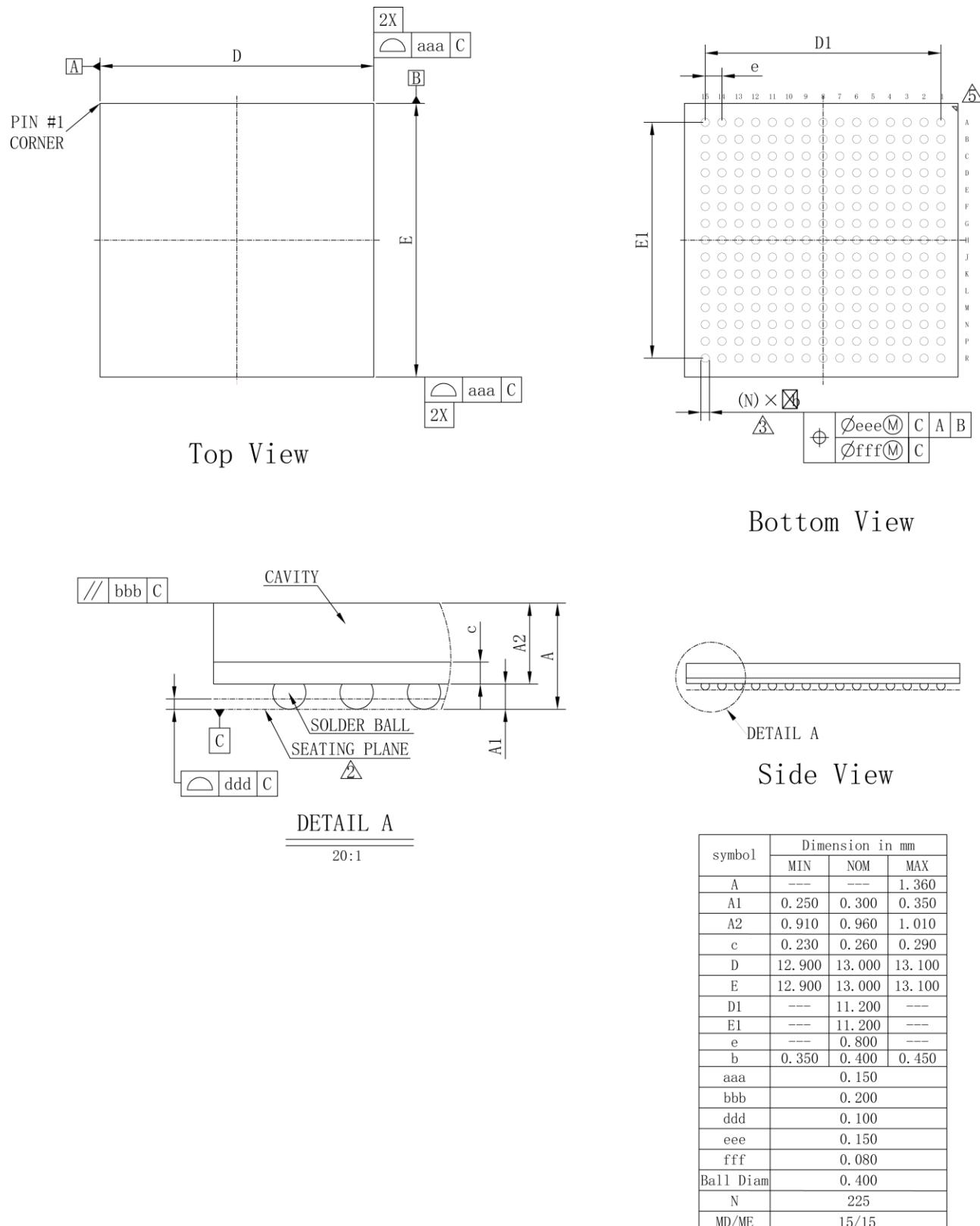
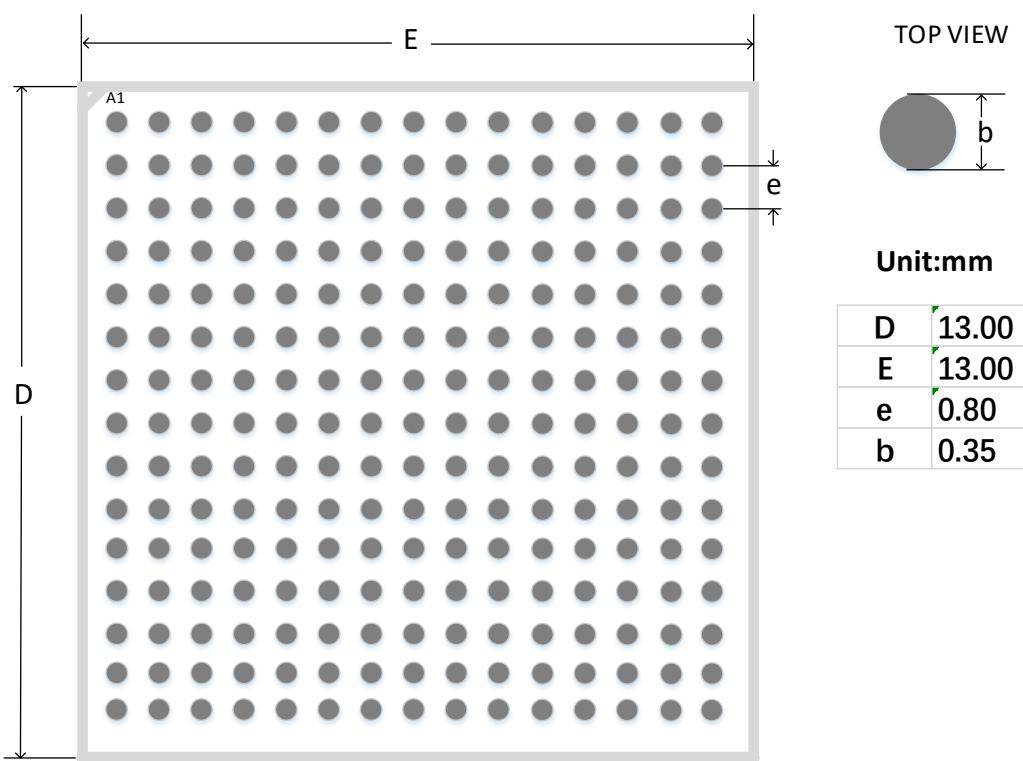


Figure 4-16 Recommended PCB Layout UG225S

4.9 LQ100 Package Outline (14mm x 14mm, GW5A-25)

Figure 4-17 Package Outline LQ100

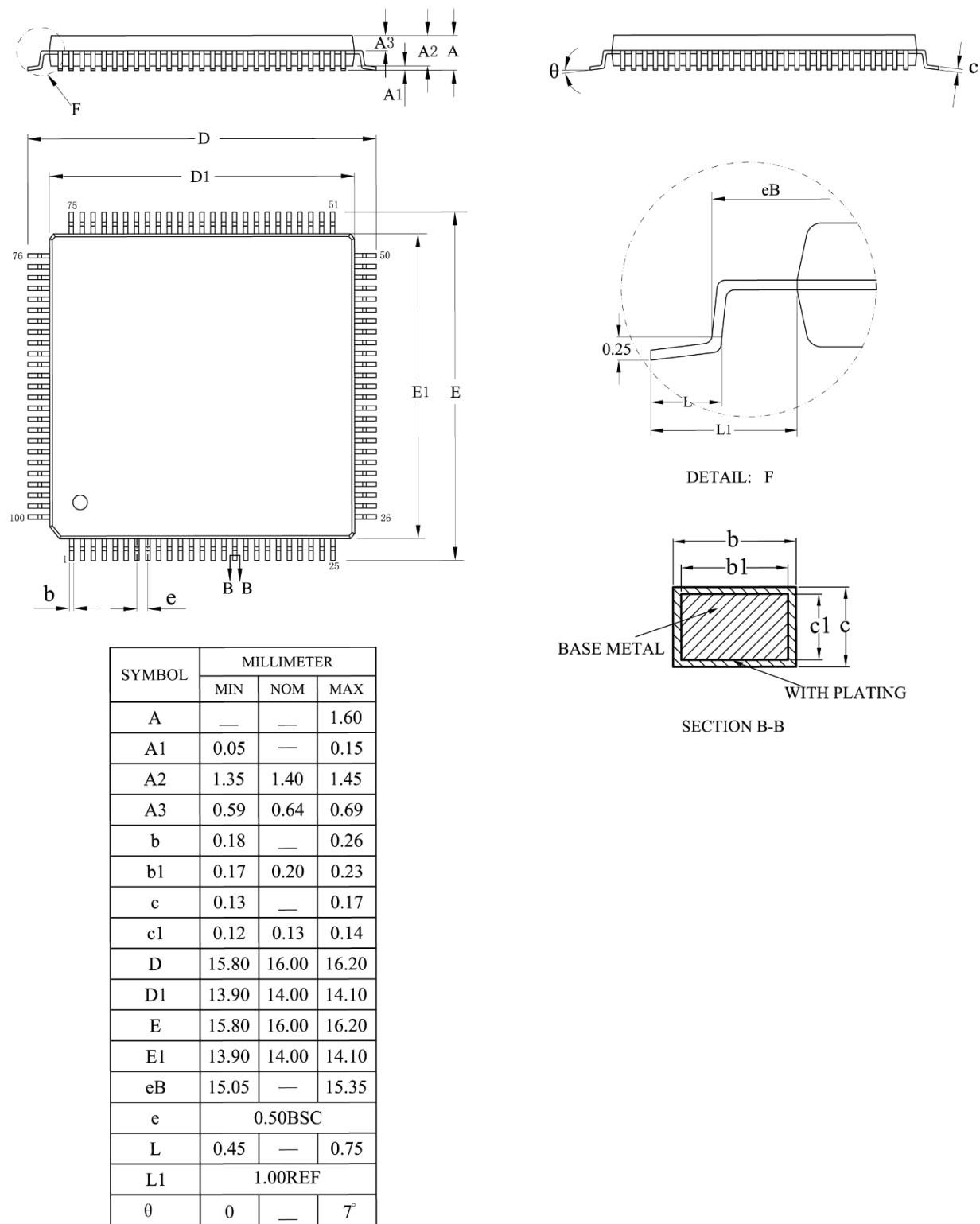
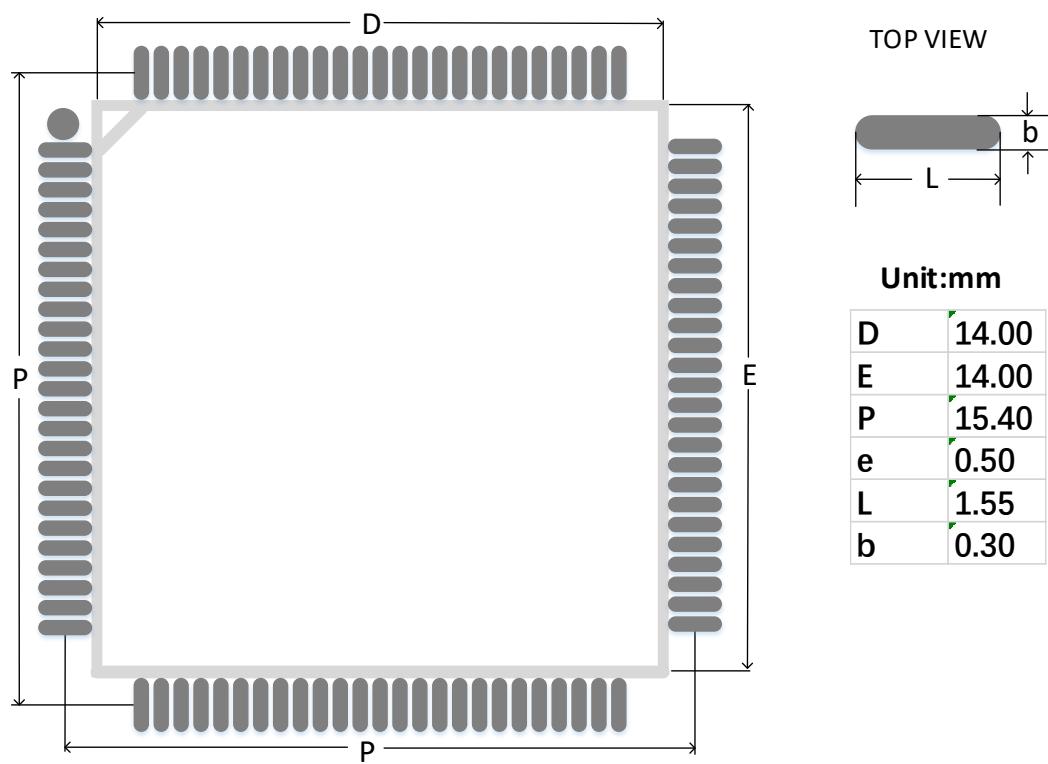


Figure 4-18 Recommended PCB Layout LQ100

4.10 PG256S Package Outline (17mm x 17mm, GW5A-25)

Figure 4-19 Package Outline PG256S

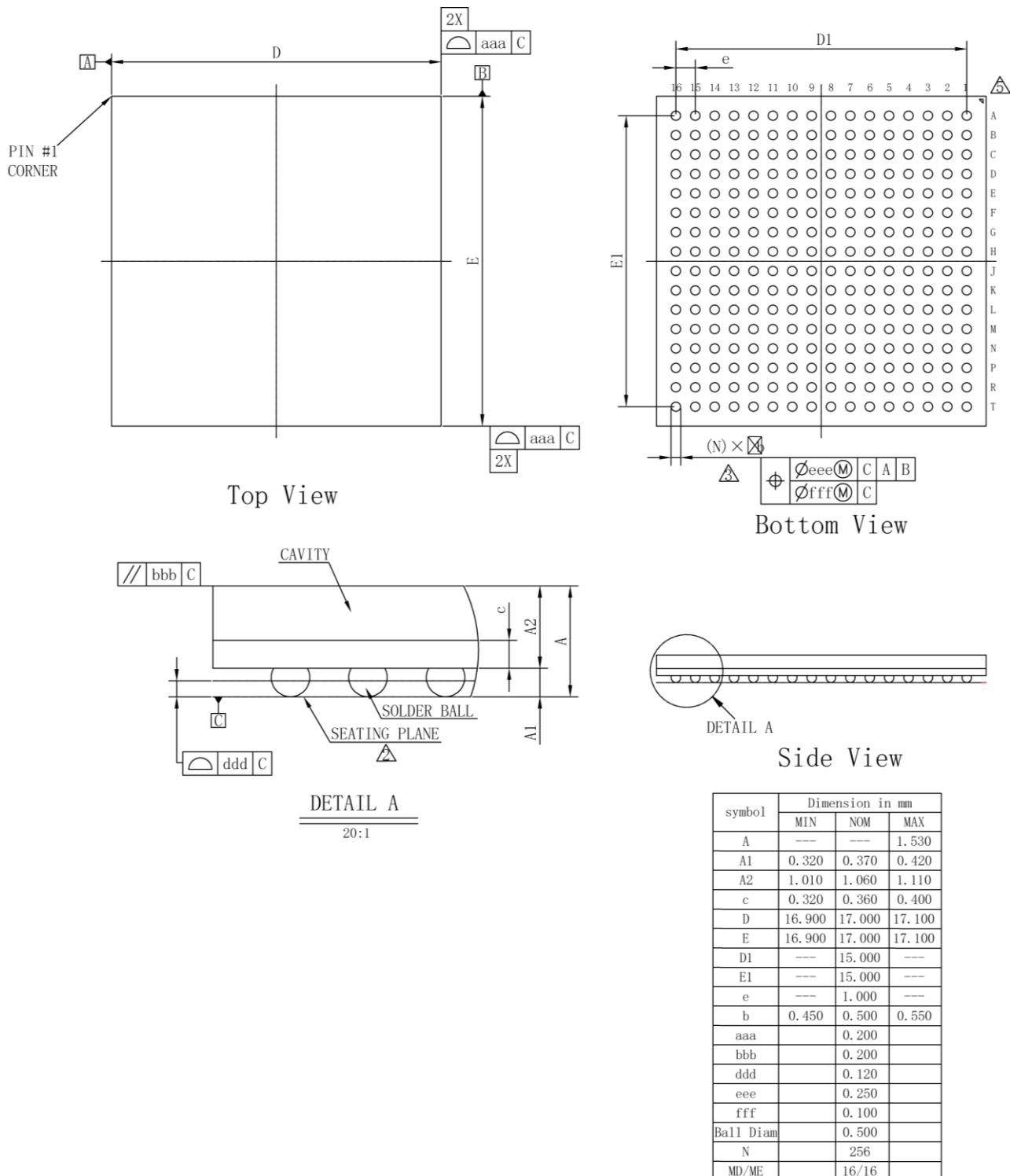


Figure 4-20 Recommended PCB Layout PG256S