
NSPL 0.5 μ m Analog CMOS 2P3M 5V Design Guide

Version 1.1

National Semiconductor Public Laboratory (NSPL)

- Electronics and Telecommunications Research Institute (ETRI)
- Seoul National University (SNU)
- Daegu Gyeongbuk Institute of Science & Technology (DGIST)



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1. Overview

1.1 Overview

The purpose of this guide is NSPL 0.5um Analog CMOS 2P3M 5V Design guide.

1.2 Software Version and Tools

- Virtuoso 6.1.8 version
- Calibre 2019.3_15.11

1.3 File Configuration

File : [NSPL_0p5um_Analog_CMOS_2P3M_5V.tar.gz](#)

- NSPL_0p5um_Analog_CMOS_2P3M_5V	: tech file
- NSPL_0p5um_Analog_CMOS_2P3M_5V.tf	: map file
- NSPL_0p5um_Analog_CMOS_2P3M_5V.layermap	: display file
- display.drf	: pcell library
- NSPL_0p5um_Analog_CMOS_2P3M_5V_pcell	: sch library
- NSPL_0p5um_Analog_CMOS_2P3M_5V_sch	: standard sch library
- NSPL_0p5um_Analog_CMOS_2P3M_5V_std_sch	: standard lay library
- NSPL_0p5um_Analog_CMOS_2P3M_5V_std_lay	
- Calibre/DRC	
- NSPL_0p5um_Analog_CMOS_2P3M_5V_DRC.cal	: drc rule file
- drc_header.cal , rundrc.com	: run command
-Calibre/ LVS	
- NSPL_0p5um_Analog_CMOS_2P3M_5V_LVS.cal	: lvs rule file
- lvs_header.cal , runlvs.com	: run command
- Calibre/LVL	
- NSPL_0p5um_Analog_CMOS_2P3M_5V_LVL.cal	: lvl rule file
- lvl_header.cal . runlvl.com	: run command
- Calibre/PEX	
- NSPL_0p5um_Analog_CMOS_2P3M_5V_PEX.cal	: pex rule file
- pex_header.cal	: run command
- LPE_LIB	: LPE Lib
- Assura/DRC	
- NSPL_0p5um_Analog_CMOS_2P3M_5V_DRC.rul	: drc rule file
- Assura/LVS	
- NSPL_0p5um_Analog_CMOS_2P3M_5V_LVS_compare.rul	: lvs rule file 1
- NSPL_0p5um_Analog_CMOS_2P3M_5V_LVS_extract.rul	: lvs rule file 2

1.4 Documents

- NSPL 0.5um Analog CMOS 2P3M 5V Design Rule : Design rule
- NSPL 0.5um Analog CMOS 2P3M 5V Design Guide : Design Guide

1.5 Document history

Rev	Date	From	Description
1.0	2023.08.21	Coressol	<p>Added Items</p> <ul style="list-style-type: none"> 1. Overview(version, file configuration, Documents) 2. Environment Files and About Use 3. Schematic Library 4. Parameter Cell Library 5. Standard Schematic Library 6. Standard Layout Library 7. Sealring 8. Calibre DRC 9. Calibre LVS 10. Calibre LVL
	2023.09.06	Coressol	<p>Added Items</p> <ul style="list-style-type: none"> 8. LVS Guide <p>Modify Items</p> <ul style="list-style-type: none"> 8.Calibre DRC → 9.Calibre DRC 9. Calibre LVS → 10.Calibre LVS 10. Calibre LVL → 11.Calibre LVL
1.1	2023.10.27	Coressol	<p>Added Layers</p> <ul style="list-style-type: none"> 2.2 Technology File : CHIPBOUNDARY Layer 2.3 Map File : CHIPBOUNDARY Layer <p>Modify Layer Numbers</p> <ul style="list-style-type: none"> 2.2 Technology File : ESDI(109→26) , ESD(26→52) Layer 2.3 Map File : ESDI(109→26) , ESD(26→52) Layer
		<p>Title NSPL 0.5μm Analog CMOS 2P3M 5V Design Guide</p>	
		<p>Division Coressol</p>	

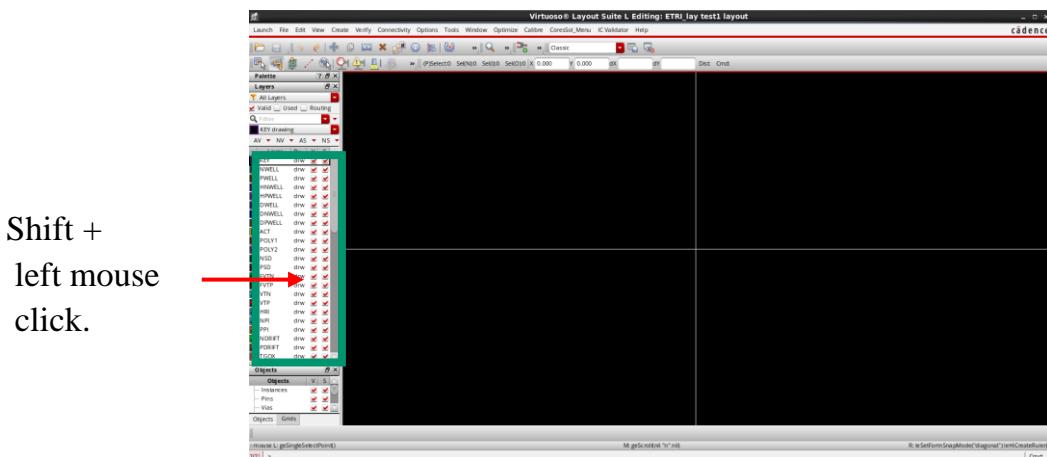
1.5 Document history

Rev	Date	From	Description
	2023.11.23	Coressol	<p>Modify Items.</p> <ul style="list-style-type: none">- PPRES/NPRES → Merged P2RES- PPHRES/NPHRES → Merged P2HRES- Schematic Library : Added Cell “3.2 .Device_ALL”- Symbol Update : 3.5 p2res, 3.6 p2hres, 3.7 pipcap- Pcell Changed : 4.5 p2res, 4.6 p2hres- Std_Sch Library : Added Cell “5.1 .SAMPLE” <p>Added Items.</p> <ul style="list-style-type: none">- 12. Assura DRC- 13. Assura LVS
		<p>Title NSPL 0.5μm Analog CMOS 2P3M 5V Design Guide</p>	
		<p>Division Coressol</p>	

2. Environment Files and About Use

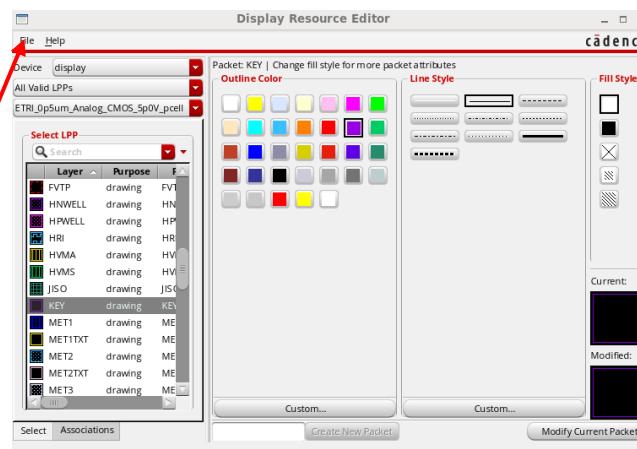
2.1 Display.drf File

- This file should exist in the location where virtuoso is run.
- This file the color of the layer is specified.
- If you want to change the color, you can do so in the following ways

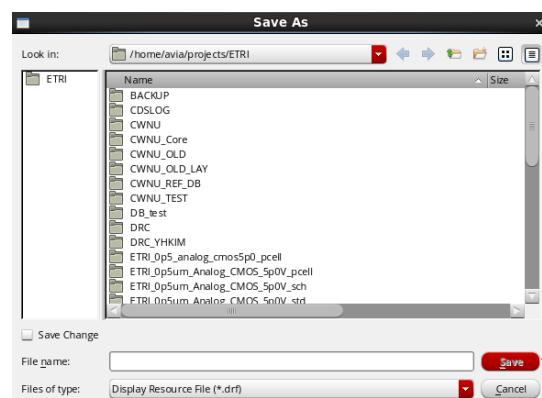


Layer Edit

Save at file



Select file or
New file name



2.2 Technology File

Layer Name	Layer No.	Function	Digitized Area
CHIPBOUNDARY	0	Define Chip Boundary	
KEY	1	Define Align key	C
NWELL	2	Define N-well for PMOS body	C
PWELL	3	Define P-well for NMOS body	C
ACT	11	Define Active area	D
POLY1	12	Define Poly-Si 1 for gate of transistor	D
POLY2	13	Define Poly-Si 2 for resistor and capacitor	D
NSD	14	Define N-type implant region for N-LDD and N+	C
PSD	15	Define N-type implant region for P-LDD and P+	C
NHRI	20	Define implant for N-type high resistance poly-Si resistor (poly)	C
PHRI	21	Define implant for P-type high resistance poly-Si resistor (poly)	C
ESDI	26	Define ESD Implnat	C
CONT	31	Define contact from MET1 to ACT, POLY1 and POLY2	C
MET1	32	Define Metal-1 for interconnection	D
VIA1	33	Define Via1 connecting MET1 and MET2	C
MET2	34	Define Metal-2 for interconnection	D
VIA2	35	Define Via2 connecting MET2 and MET3	C
MET3	36	Define Metal-3 for interconnection	D
PAD	37	Define open region of passivation for bonding pad	C
POLY1TXT	41	Poly1 Text	
MET1TXT	42	MET1 Text	
MET2TXT	44	MET2 Text	
MET3TXT	46	MET3 Text	
PADTXT	47	PAD Text	
TEXT	48	Text	
RES	51	Poly-Si Resistor for DRC & LVS	
ESD	52	Define ESD device region for DRC	
CAP	53	Poly-Si Capacitor for DRC & LVS	
BJT	56	BJT for DRC & LVS	
DIODE	57	Diode for DRC & LVS	
NODRC	58	DRC check blocking layer	
ESDD	59	Define ESD device drain electrode	
LVSD	60	Extract Poly-Si Resistor/PIP CAP Area	

2.3 Map File

Layer Name	Layer Purpose	Layer No.	Layer Data Type
CHIPBOUNDARY	drawing	0	0
KEY	drawing	1	0
NWELL	drawing	2	0
PWELL	drawing	3	0
ACT	drawing	11	0
POLY1	drawing	12	0
POLY2	drawing	13	0
NSD	drawing	14	0
PSD	drawing	15	0
NHRI	drawing	20	0
PHRI	drawing	21	0
ESDI	drawing	26	0
CONT	drawing	31	0
MET1	drawing	32	0
VIA1	drawing	33	0
MET2	drawing	34	0
VIA2	drawing	35	0
MET3	drawing	36	0
PAD	drawing	37	0
POLY1TXT	drawing	41	0
MET1TXT	drawing	42	0
MET2TXT	drawing	44	0
MET3TXT	drawing	46	0
PADTXT	drawing	47	0
TEXT	drawing	48	0
RES	drawing	51	0
ESD	drawing	52	0
CAP	drawing	53	0
BJT	drawing	56	0
DIODE	drawing	57	0
NODRC	drawing	58	0
ESDD	drawing	59	0
LVSD	drawing	60	0

2.4 How to Setup Library

- Bring the NSPL_0p5um_Analog_CMOS_2P3M_5V.tar.gz file to the location where you want to run virtuoso and release the component with a command like the following:

```
tar -zxvf NSPL_0p5um_Analog_CMOS_2P3M_5V.tar.gz
```

```
Nov 27 08:37 Assura/
Nov 27 08:37 Calibre/
Nov 27 08:37 NSPL_0p5um_Analog_CMOS_2P3M_5V_V1p1.layermap*
Nov 27 08:37 NSPL_0p5um_Analog_CMOS_2P3M_5V_V1p1.tf*
Nov 27 08:37 NSPL_0p5um_Analog_CMOS_2P3M_5V_pcell/
Nov 27 08:37 NSPL_0p5um_Analog_CMOS_2P3M_5V_sch/
Nov 27 08:37 NSPL_0p5um_Analog_CMOS_2P3M_5V_std_lay/
Nov 27 08:38 NSPL_0p5um_Analog_CMOS_2P3M_5V_std_sch/
Nov 27 08:37 display.drf*
```

- Define Library in cds.lib

```
NSPL_0p5um_Analog_CMOS_2P3M_5V_pcell
NSPL_0p5um_Analog_CMOS_2P3M_5V_sch
NSPL_0p5um_Analog_CMOS_2P3M_5V_std_lay
NSPL_0p5um_Analog_CMOS_2P3M_5V_std_sch
```

- DEFINE library_name library_path (following example – cds.lib)

```
DEFINE NSPL_0p5um_Analog_CMOS_2P3M_5V_pcell /home/avia/projects/ETRI_0p5um/NSPL_0p5um_Analog_CMOS_2P3M_5V_pcell
DEFINE NSPL_0p5um_Analog_CMOS_2P3M_5V_sch /home/avia/projects/ETRI_0p5um/NSPL_0p5um_Analog_CMOS_2P3M_5V_sch
DEFINE NSPL_0p5um_Analog_CMOS_2P3M_5V_std_lay /home/avia/projects/ETRI_0p5um/NSPL_0p5um_Analog_CMOS_2P3M_5V_std_lay
DEFINE NSPL_0p5um_Analog_CMOS_2P3M_5V_std_sch /home/avia/projects/ETRI_0p5um/NSPL_0p5um_Analog_CMOS_2P3M_5V_std_sch
```

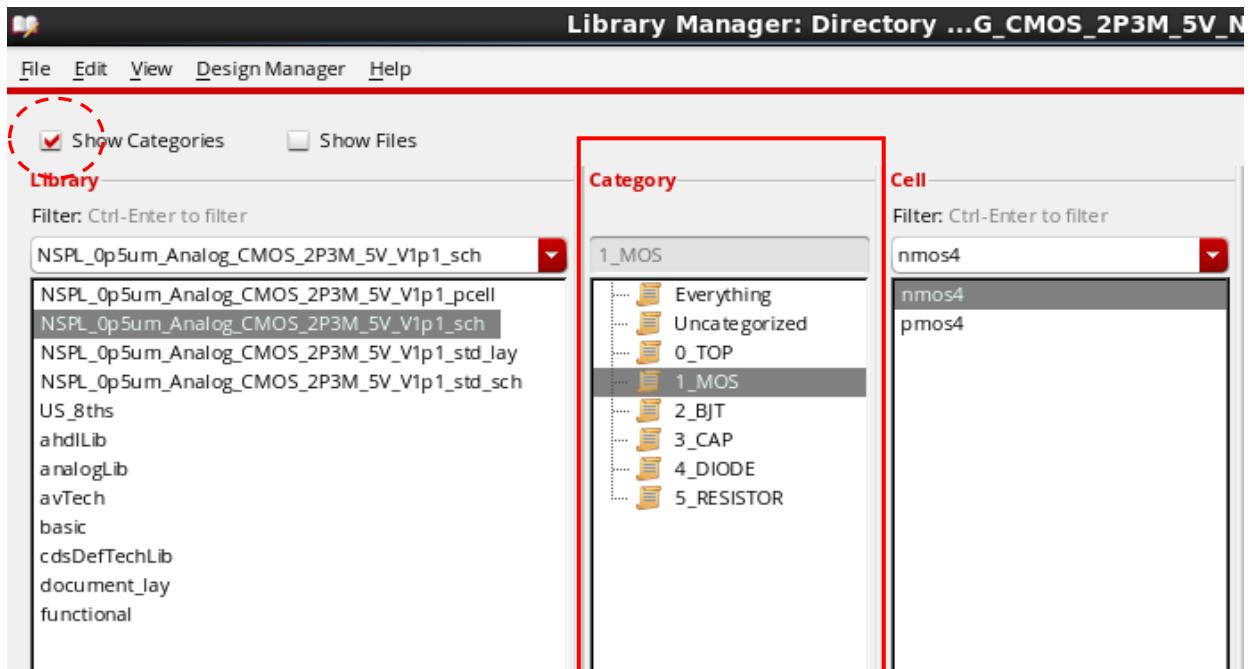
- Copy the files in the DRC Directory to the location where you want to run the DRC.
- Copy the files in the LVS Directory to the location where you want to run the LVS.
- Copy the files in the LVL Directory to the location where you want to run the LVL.
- display.drf file copy at virtuoso running.

2.5 How to Create a Library

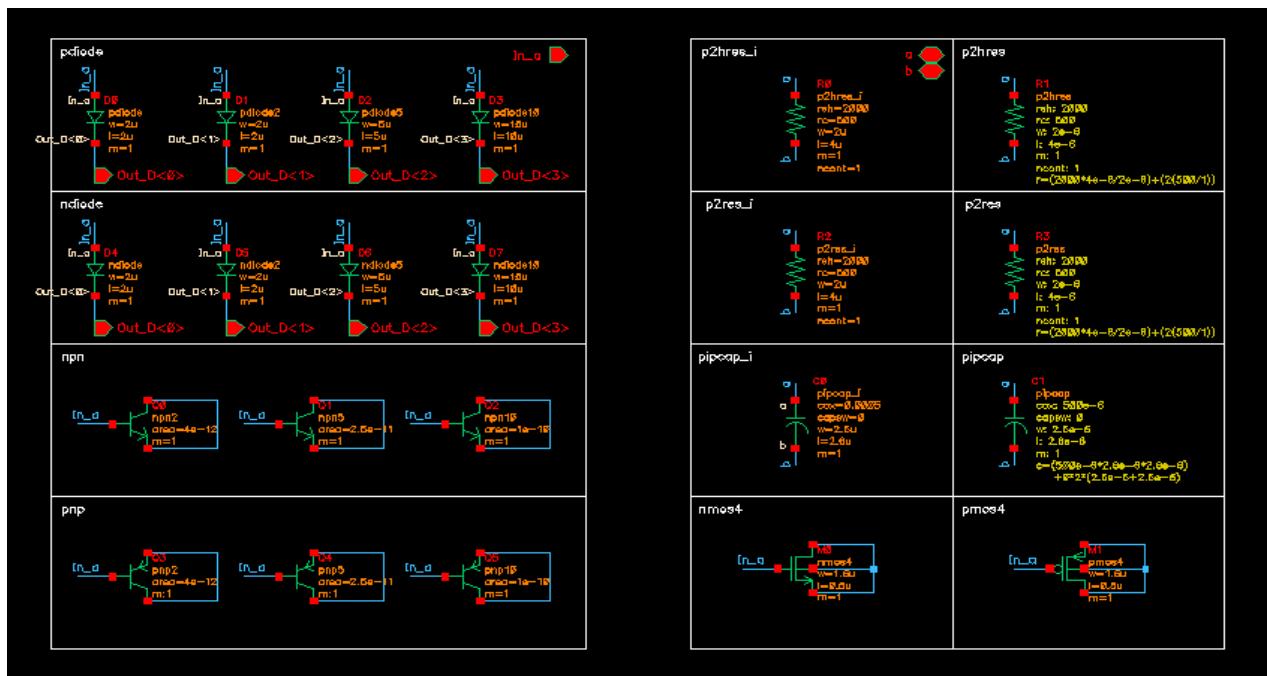


3. Schematic Library

3.1 Library Category

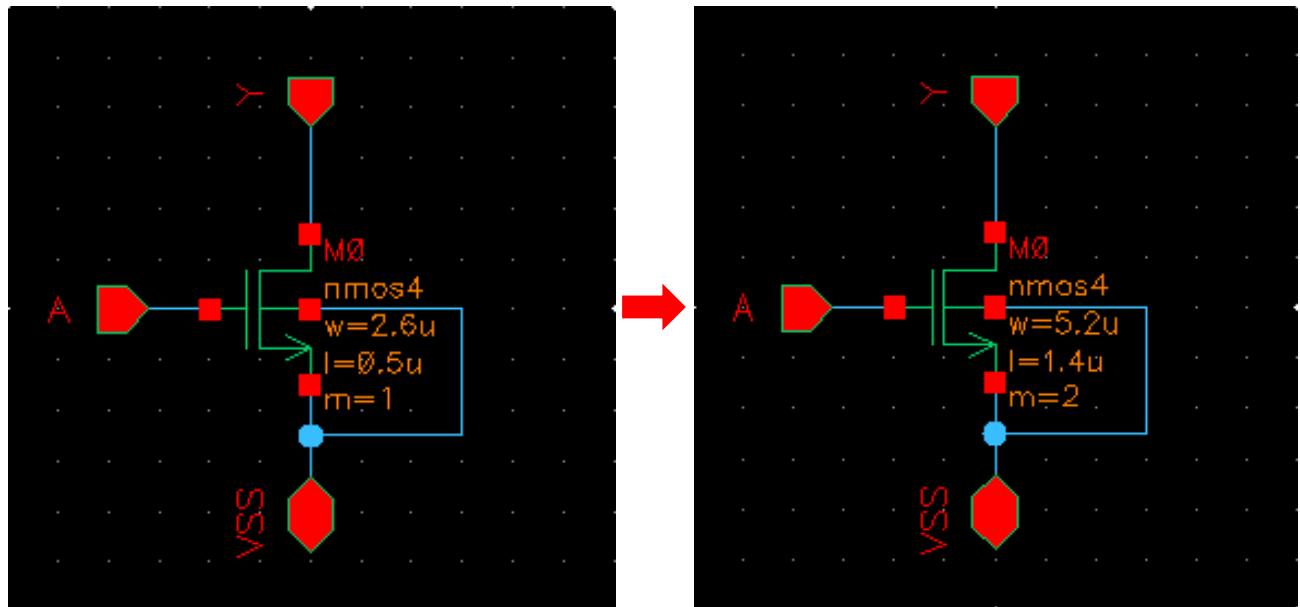


3.2 .Device_ALL



3.3 nmos4

Parameter					
Width	2.6u → 5.2u	Length	0.5u → 1.4u	multiplier	1 → 2



<Schematic parameter>

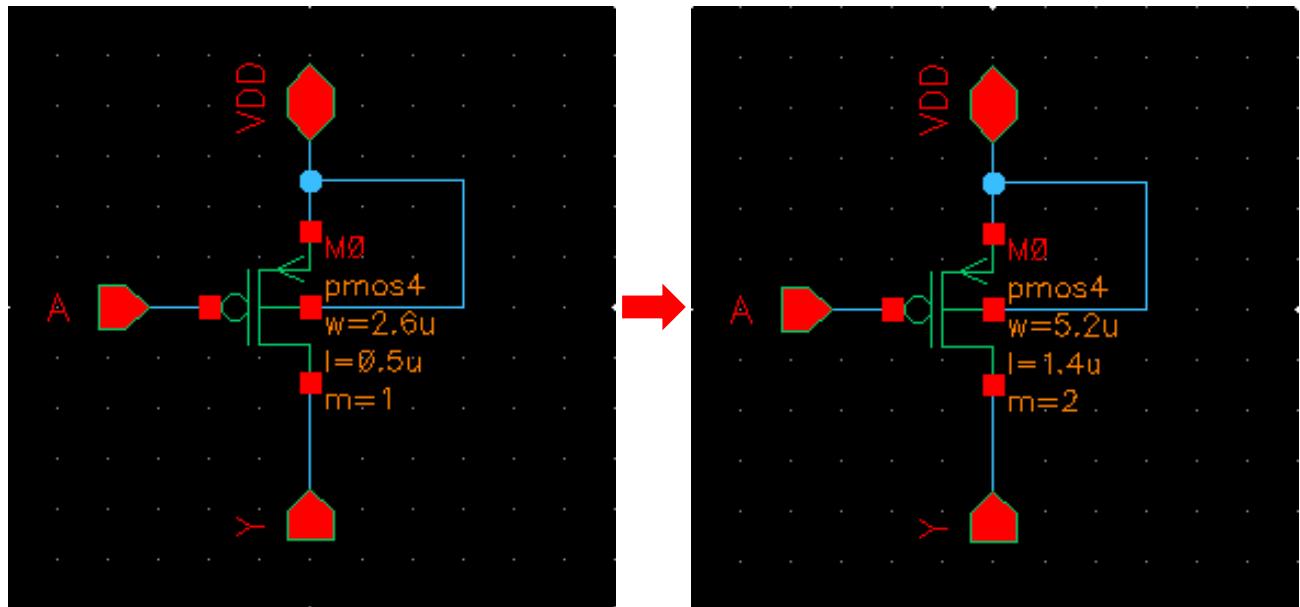
```
*****
* Library Name: ETRI_lay
* Cell Name: nmos4
* View Name: schematic
*****  
  
.SUBCKT nmos4 A VSS Y
*.PININFO A:I Y:O VSS:B
MM0 Y A VSS VSS nmos4 W=2.6u L=0.5u m=1
.ENDS
```

```
*****
* Library Name: ETRI_lay
* Cell Name: nmos4
* View Name: schematic
*****  
  
.SUBCKT nmos4 A VSS Y
*.PININFO A:I Y:O VSS:B
MM0 Y A VSS VSS nmos4 W=5.2u L=1.4u m=2
.ENDS
```

<cdl output>

3.4 pmos4

Parameter					
Width	2.6u → 5.2u	Length	0.5u → 1.4u	multiplier	1 → 2



<Schematic parameter>

```
*****
* Library Name: ETRI_lay
* Cell Name: pmos4
* View Name: schematic
*****
.SUBCKT pmos4 A VDD Y
*.PININFO A:I Y:O VDD:B
MM0 Y A VDD VDD pmos4 W=2.6u L=0.5u m=1
.ENDS
```

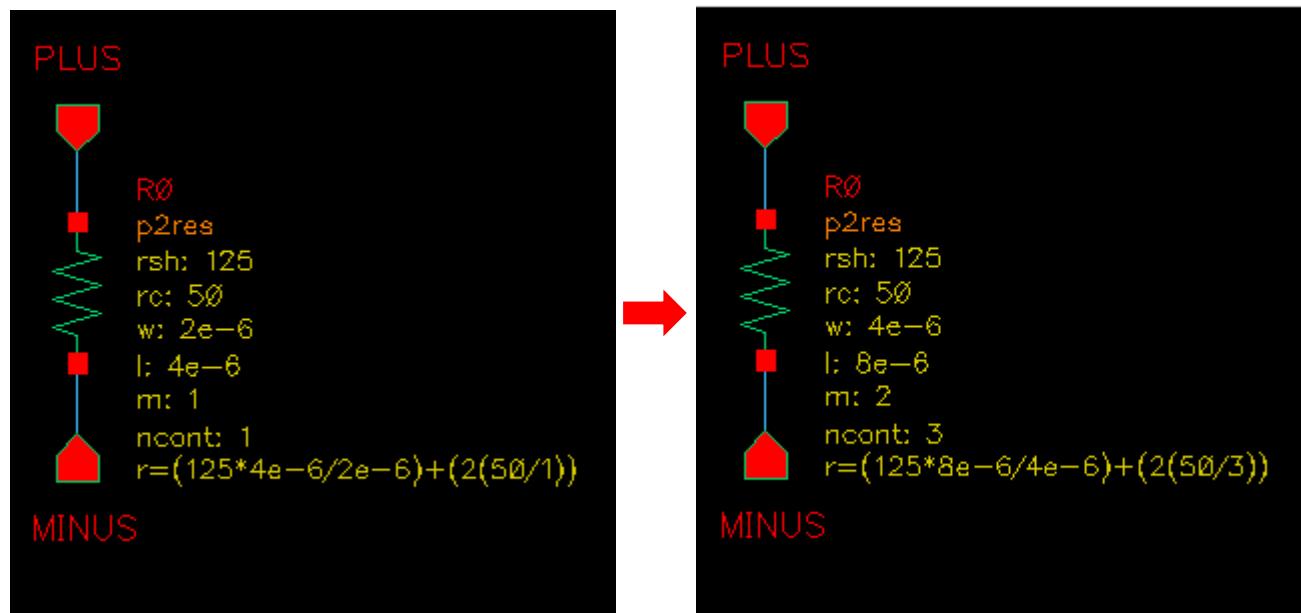
```
*****
* Library Name: ETRI_lay
* Cell Name: pmos4
* View Name: schematic
*****
.SUBCKT pmos4 A VDD Y
*.PININFO A:I Y:O VDD:B
MM0 Y A VDD VDD pmos4 W=5.2u L=1.4u m=2
.ENDS
```

<cdl output>

3.5 p2res (include p2res_i)

* Process Parameter : rsh, rc

Parameter							
Width	2u → 4u	Length	4u → 8u	multiplier	1 → 2	ncont	1 → 3



<Schematic parameter>

```
*****
* Library Name: ETRI_NSPL_lay
* Cell Name: p2res
* View Name: schematic
*****
.SUBCKT p2res MINUS PLUS
*.PININFO MINUS:I PLUS:I
XR0 MINUS PLUS / p2res rl=4u rw=2u rm=1
.ENDS
```

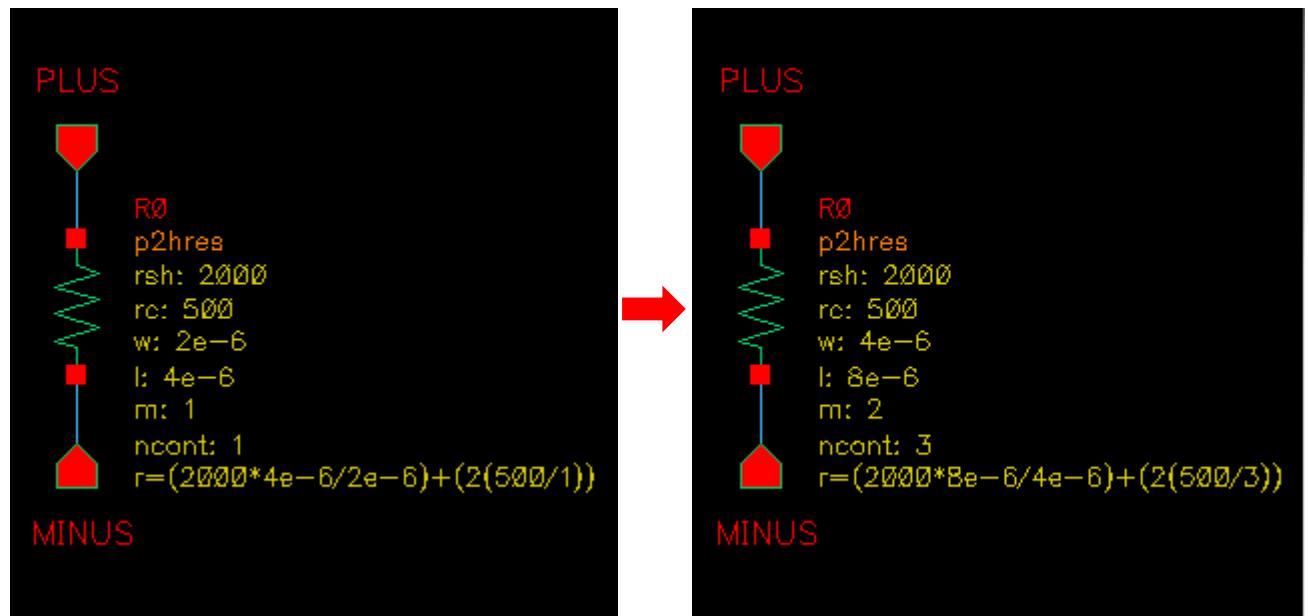
```
*****
* Library Name: ETRI_NSPL_lay
* Cell Name: p2res
* View Name: schematic
*****
.SUBCKT p2res MINUS PLUS
*.PININFO MINUS:I PLUS:I
XR0 MINUS PLUS / p2res rl=8u rw=4u rm=2
.ENDS
```

<cdl output>

3.6 p2hres (include p2hres_i)

* Process Parameter : rsh, rc

Parameter							
Width	2u → 4u	Length	4u → 8u	multiplier	1 → 2	ncont	1 → 3



<Schematic parameter>

```
*****
* Library Name: ETRI_NSPL_lay
* Cell Name: p2hres
* View Name: schematic
*****
.SUBCKT p2hres MINUS PLUS
*.PININFO MINUS:I PLUS:I
XR0 MINUS PLUS / p2hres rl=4u rw=2u rm=1
.ENDS
```

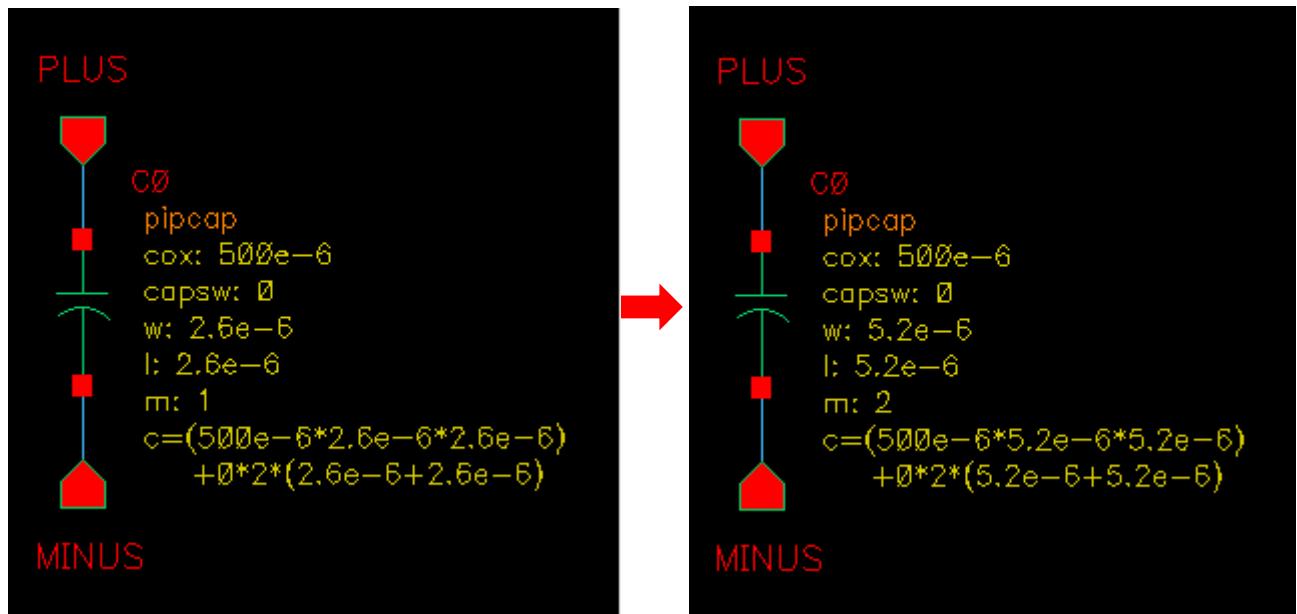
```
*****
* Library Name: ETRI_NSPL_lay
* Cell Name: p2hres
* View Name: schematic
*****
.SUBCKT p2hres MINUS PLUS
*.PININFO MINUS:I PLUS:I
XR0 MINUS PLUS / p2hres rl=8u rw=4u rm=2
.ENDS
```

<cdl output>

3.7 pipcap (include pipcap_i)

* Process Parameter : cox, capsaw

Parameter					
Width	2.6u → 5.2u	Length	2.6u → 5.2u	multiplier	1 → 2



<Schematic parameter>

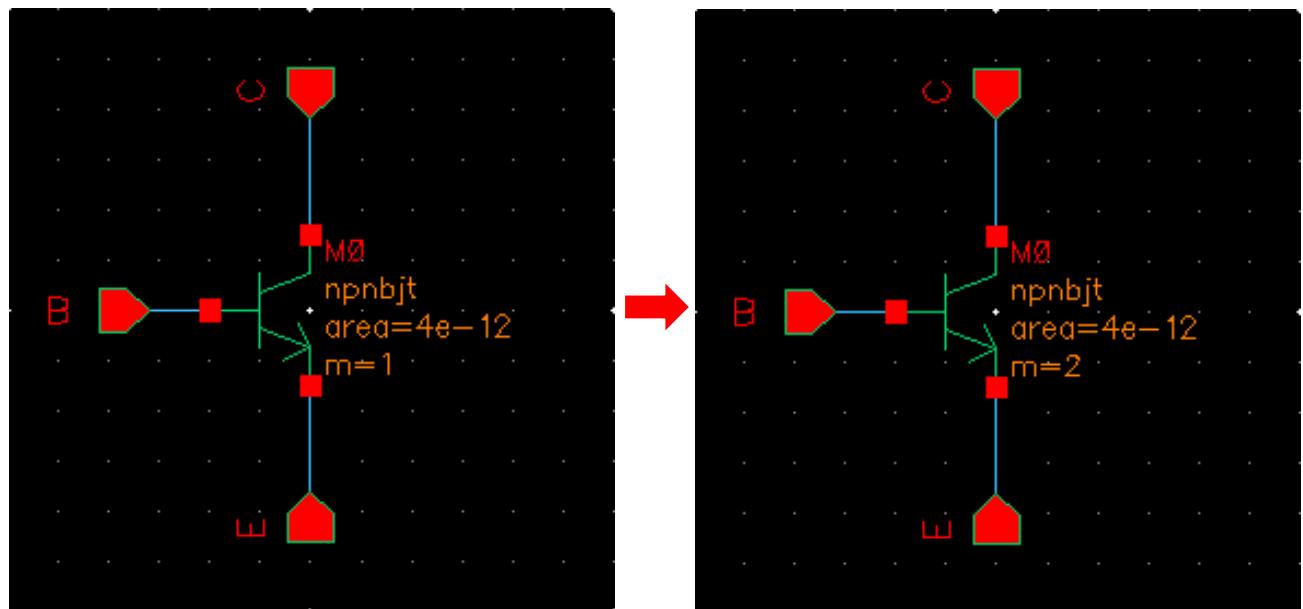
```
*****
* Library Name: ETRI_NSPL_lay
* Cell Name:    pipcap
* View Name:   schematic
*****
.SUBCKT pipcap MINUS PLUS
*.PININFO MINUS:I PLUS:I
X0 MINUS PLUS / pipcap cl=2.6u cw=2.6u cm=1
.ENDS
```

```
*****
* Library Name: ETRI_NSPL_lay
* Cell Name:    pipcap
* View Name:   schematic
*****
.SUBCKT pipcap MINUS PLUS
*.PININFO MINUS:I PLUS:I
X0 MINUS PLUS / pipcap cl=5.2u cw=5.2u cm=2
.ENDS
```

<cdl output>

3.8 npn2

Parameter			
Area	4e-12	multiplier	1 → 2



<Schematic parameter>

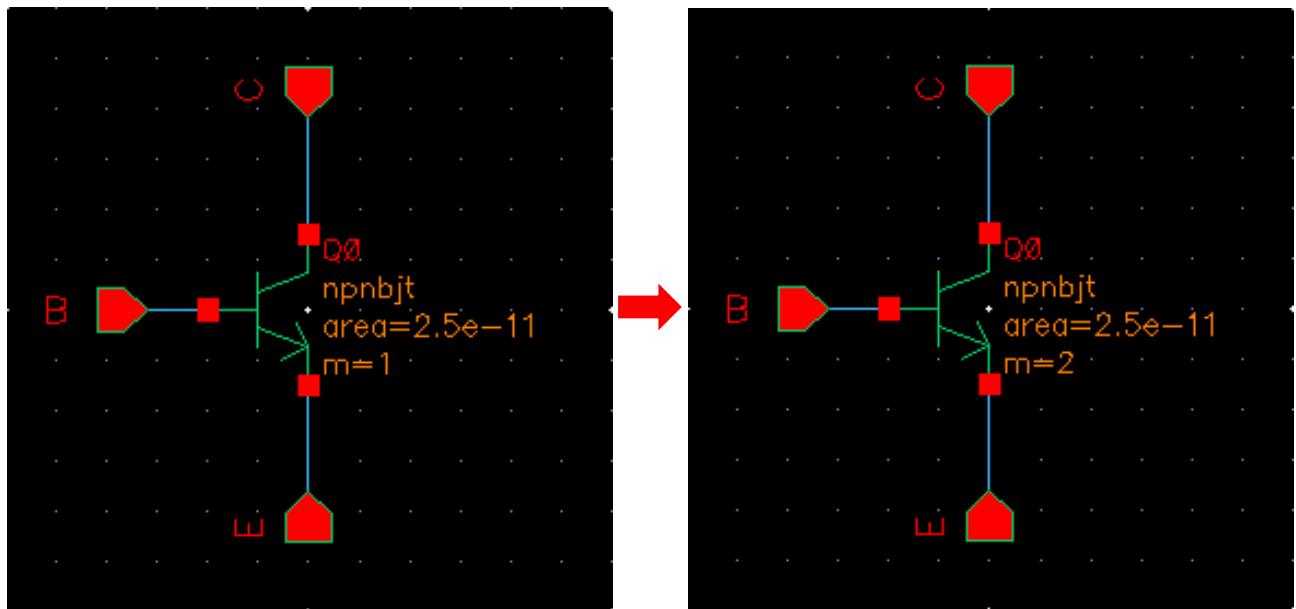
```
*****
* Library Name: ETRI_lay
* Cell Name: npn2
* View Name: schematic
*****
.SUBCKT npn2 B C E
*.PININFO B:I C:I E:O
QM0 C B E npnbjt m=1 area=4e-12
.ENDS
```

```
*****
* Library Name: ETRI_lay
* Cell Name: npn2
* View Name: schematic
*****
.SUBCKT npn2 B C E
*.PININFO B:I C:I E:O
QM0 C B E npnbjt m=2 area=4e-12
.ENDS
```

<cdl output>

3.9 npn5

Parameter			
Area	2.5e-11	multiplier	1 → 2



<Schematic parameter>

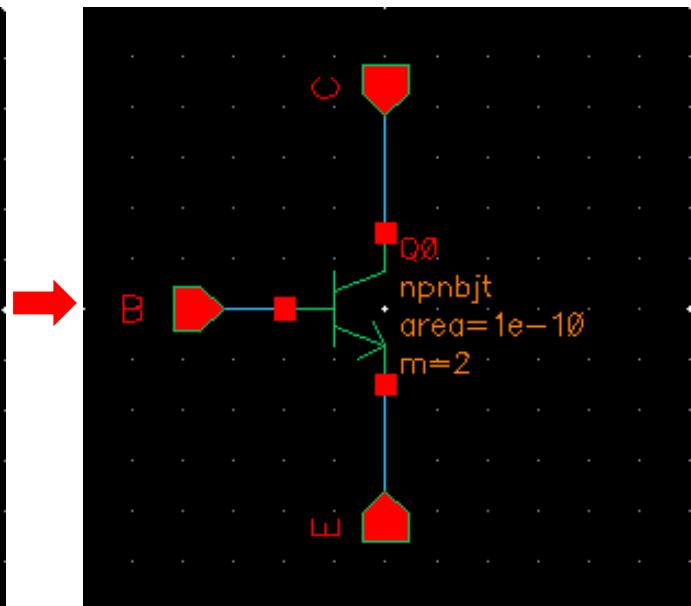
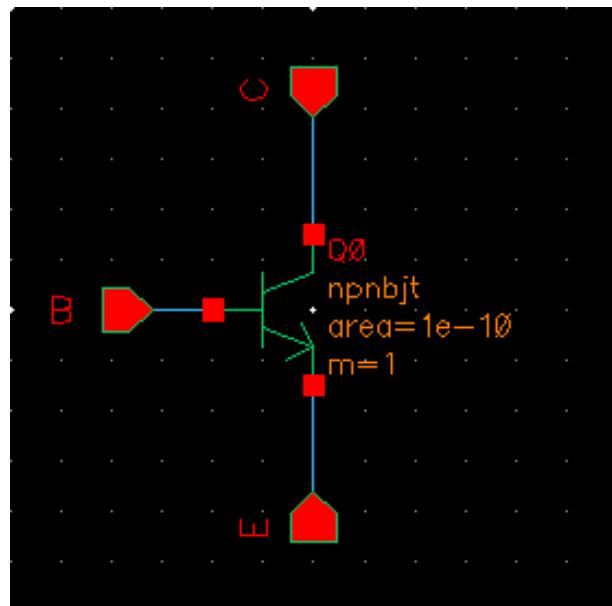
```
*****
* Library Name: ETRI_lay
* Cell Name: npn5
* View Name: schematic
*****
.SUBCKT npn5 B C E
*.PININFO B:I C:I E:0
Q0 C B E npnbjt m=1 area=2.5e-11
.ENDS
```

```
*****
* Library Name: ETRI_lay
* Cell Name: npn5
* View Name: schematic
*****
.SUBCKT npn5 B C E
*.PININFO B:I C:I E:0
Q0 C B E npnbjt m=2 area=2.5e-11
.ENDS
```

<cdl output>

3.10 npn10

Parameter			
Area	1e-10	multiplier	1 → 2



<Schematic parameter>

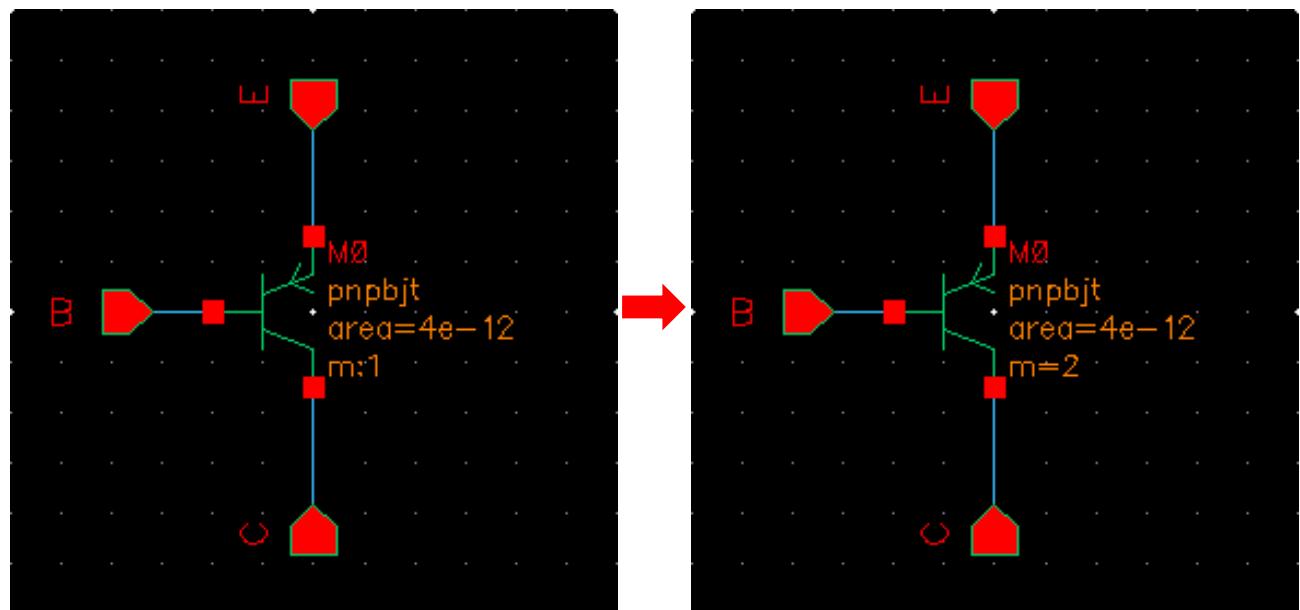
```
*****
* Library Name: ETRI_lay
* Cell Name: npn10
* View Name: schematic
*****
.SUBCKT npn10 B C E
*.PININFO B:I C:I E:0
Q0 C B E npnbjt m=1 area=1e-10
.ENDS
```

```
*****
* Library Name: ETRI_lay
* Cell Name: npn10
* View Name: schematic
*****
.SUBCKT npn10 B C E
*.PININFO B:I C:I E:0
Q0 C B E npnbjt m=2 area=1e-10
.ENDS
```

<cdl output>

3.11 pnp2

Parameter			
Area	4e-12	multiplier	1 → 2



<Schematic parameter>

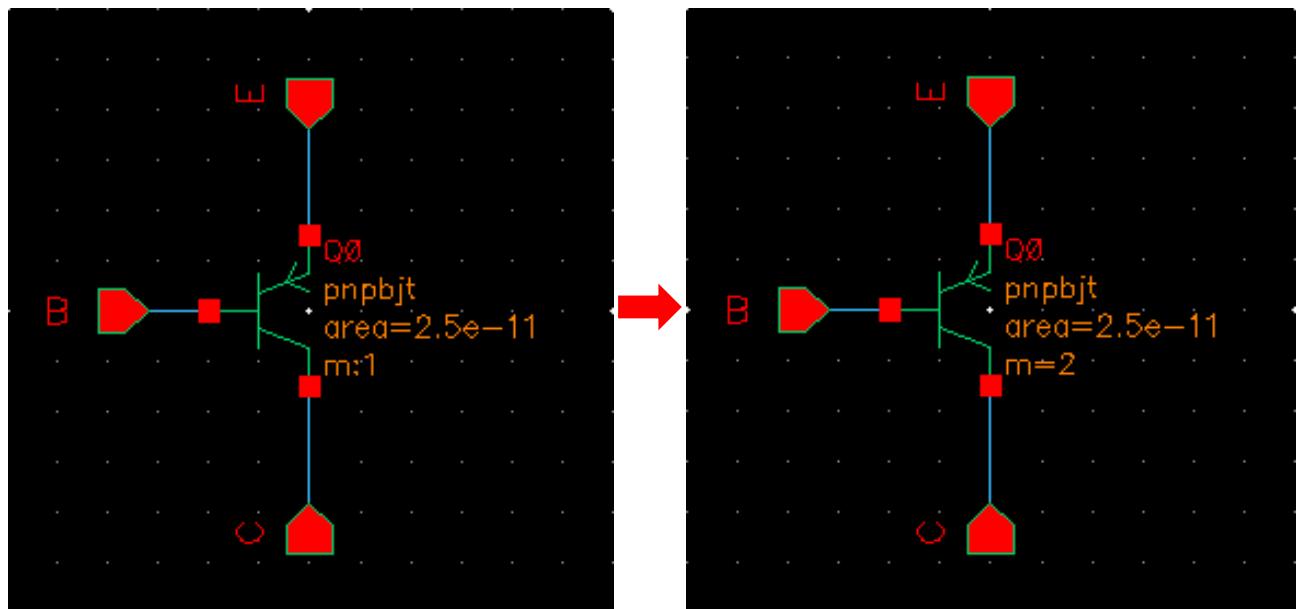
```
*****
* Library Name: ETRI_lay
* Cell Name: pnp2
* View Name: schematic
*****  
  
.SUBCKT pnp2 B C E
*.PININFO B:I C:I E:O
QM0 C B E pnpbjt m=1 area=4e-12
.ENDS
```

```
*****
* Library Name: ETRI_lay
* Cell Name: pnp2
* View Name: schematic
*****  
  
.SUBCKT pnp2 B C E
*.PININFO B:I C:I E:O
QM0 C B E pnpbjt m=2 area=4e-12
.ENDS
```

<cdl output>

3.12 pnp5

Parameter			
Area	2.5e-11	multiplier	1 → 2



<Schematic parameter>

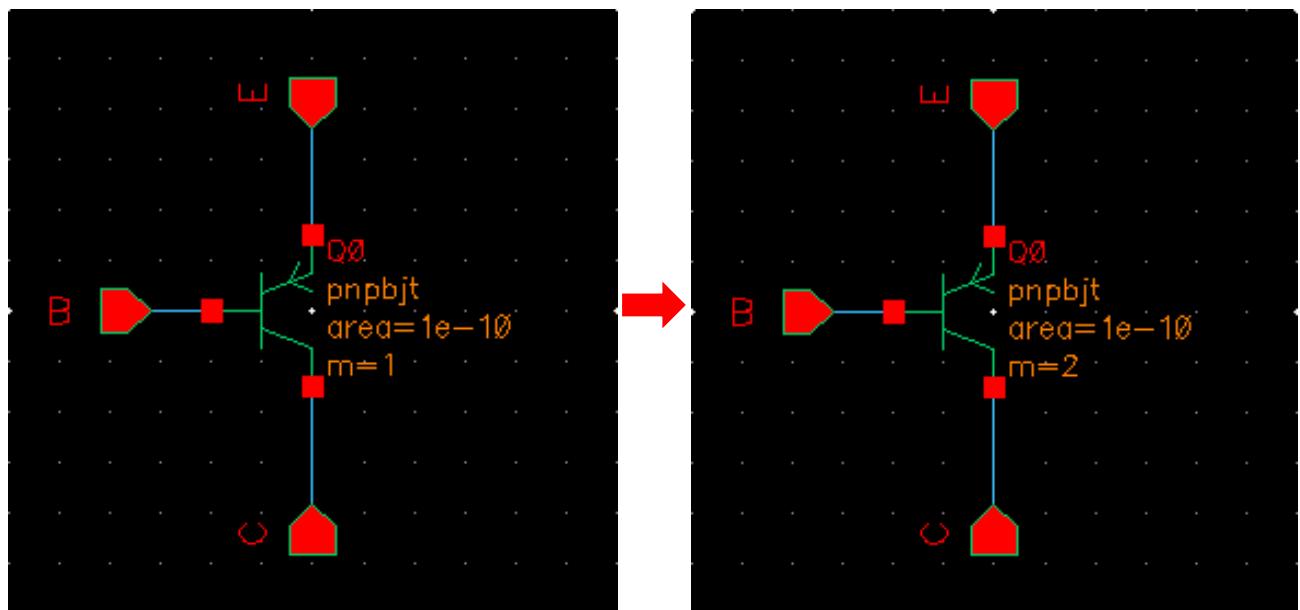
```
*****
* Library Name: ETRI_lay
* Cell Name: pnp5
* View Name: schematic
*****
.SUBCKT pnp5 B C E
*.PININFO B:I C:I E:O
QQ0 C B E pnpbjt m=1 area=2.5e-11
.ENDS
```

```
*****
* Library Name: ETRI_lay
* Cell Name: pnp5
* View Name: schematic
*****
.SUBCKT pnp5 B C E
*.PININFO B:I C:I E:O
QQ0 C B E pnpbjt m=2 area=2.5e-11
.ENDS
```

<cdl output>

3.13 pnp10

Parameter			
Area	1e-10	multiplier	1 → 2



<Schematic parameter>

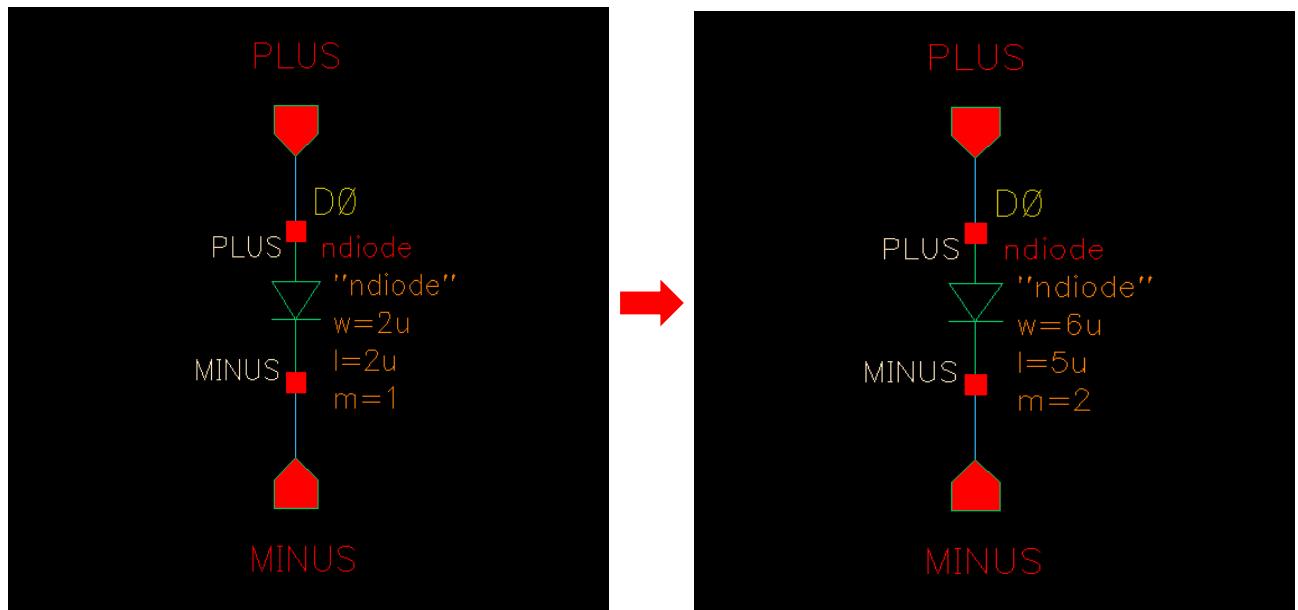
```
*****
* Library Name: ETRI_lay
* Cell Name: pnp10
* View Name: schematic
*****  
  
.SUBCKT pnp10 B C E
*.PININFO B:I C:I E:O
Q00 C B E pnpbjt m=1 area=1e-10
.ENDS
```

```
*****
* Library Name: ETRI_lay
* Cell Name: pnp10
* View Name: schematic
*****  
  
.SUBCKT pnp10 B C E
*.PININFO B:I C:I E:O
Q00 C B E pnpbjt m=2 area=1e-10
.ENDS
```

<cdl output>

3.14 ndiode

Parameter					
Width	2.0u → 6u	Length	2.0u → 5u	multiplier	1 → 2



<Schematic parameter>

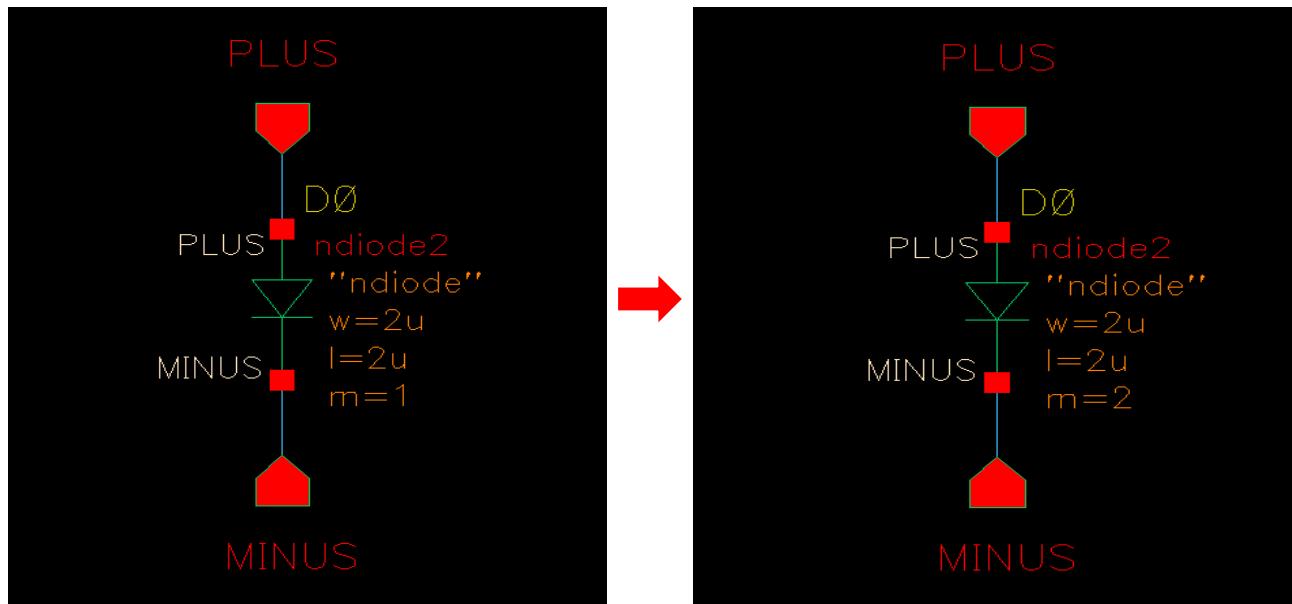
```
*****
* Library Name: ETRI_lay
* Cell Name: ndiode
* View Name: schematic
*****  
  
.SUBCKT ndiode MINUS PLUS
*.PININFO MINUS:I PLUS:I
DD0 PLUS MINUS ndiode m=1 w=2u l=2u
.ENDS
```

```
*****
* Library Name: ETRI_lay
* Cell Name: ndiode
* View Name: schematic
*****  
  
.SUBCKT ndiode MINUS PLUS
*.PININFO MINUS:I PLUS:I
DD0 PLUS MINUS ndiode m=2 w=6u l=5u
.ENDS
```

<cdl output>

3.15 ndiode2

Parameter					
Width	2.0u	Length	2.0u	multiplier	1 → 2



<Schematic parameter>

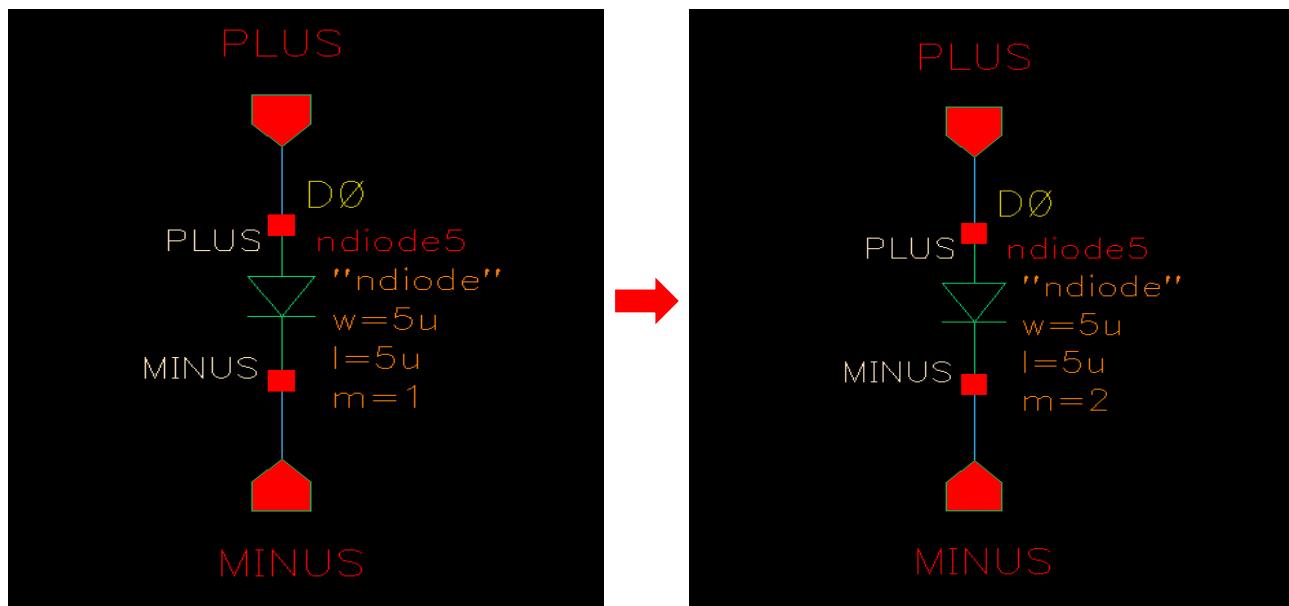
```
*****
* Library Name: ETRI_lay
* Cell Name: ndiode2
* View Name: schematic
*****
.SUBCKT ndiode2 MINUS PLUS
*.PININFO MINUS:I PLUS:I
DD0 PLUS MINUS ndiode m=1 w=2u l=2u
.ENDS
```

```
*****
* Library Name: ETRI_lay
* Cell Name: ndiode2
* View Name: schematic
*****
.SUBCKT ndiode2 MINUS PLUS
*.PININFO MINUS:I PLUS:I
DD0 PLUS MINUS ndiode m=2 w=2u l=2u
.ENDS
```

<cdl output>

3.16 ndiode5

Parameter					
Width	5.0u	Length	5.0u	multiplier	1 → 2



<Schematic parameter>

```
*****
* Library Name: ETRI_lay
* Cell Name: ndiode5
* View Name: schematic
*****
.SUBCKT ndiode5 MINUS PLUS
*.PININFO MINUS:I PLUS:I
DD0 PLUS MINUS ndiode m=1 w=5u l=5u
.ENDS
```

```
*****
* Library Name: ETRI_lay
* Cell Name: ndiode5
* View Name: schematic
*****
.SUBCKT ndiode5 MINUS PLUS
*.PININFO MINUS:I PLUS:I
DD0 PLUS MINUS ndiode m=2 w=5u l=5u
.ENDS
```

<cdl output>

3.17 ndiode10

Parameter					
Width	10.0u	Length	10.0u	multiplier	1 → 2



<Schematic parameter>

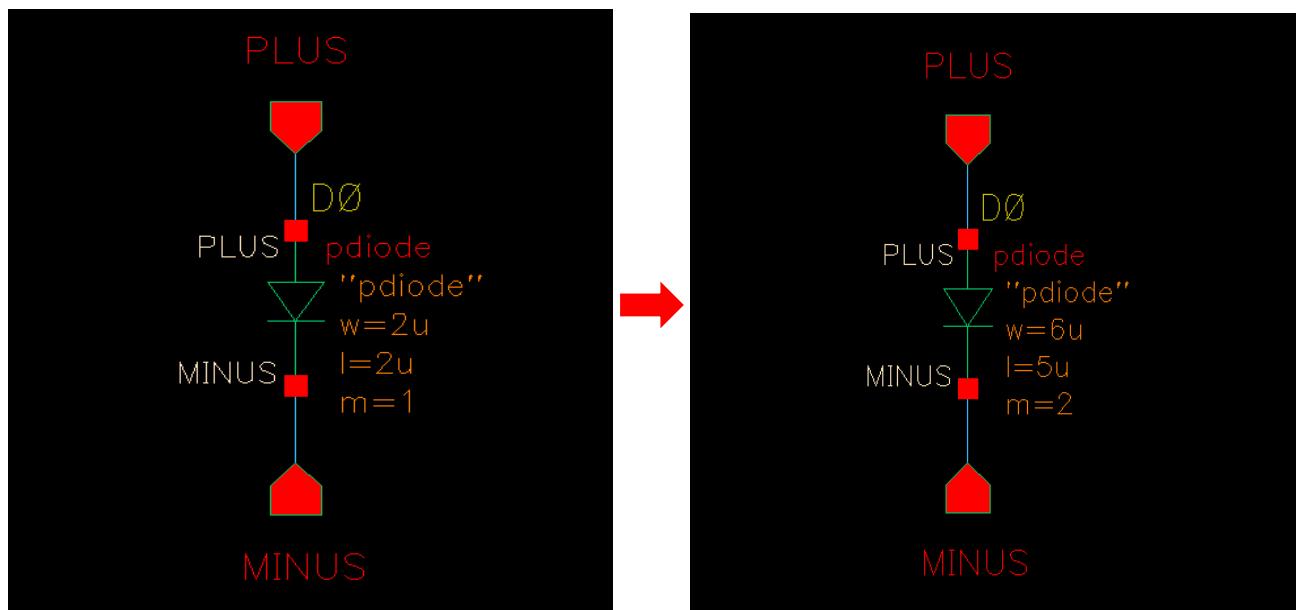
```
*****
* Library Name: ETRI_lay
* Cell Name: ndiode10
* View Name: schematic
*****  
  
.SUBCKT ndiode10 MINUS PLUS
*.PININFO MINUS:I PLUS:I
DD0 PLUS MINUS ndiode m=1 w=10u l=10u
.ENDS
```

```
*****
* Library Name: ETRI_ay
* Cell Name: ndiode10
* View Name: schematic
*****  
  
.SUBCKT ndiode10 MINUS PLUS
*.PININFO MINUS:I PLUS:I
DD0 PLUS MINUS ndiode m=2 w=10u l=10u
.ENDS
```

<cdl output>

3.18 pdiode

Parameter					
Width	2.0u → 6u	Length	2.0u → 5u	multiplier	1 → 2



<Schematic parameter>

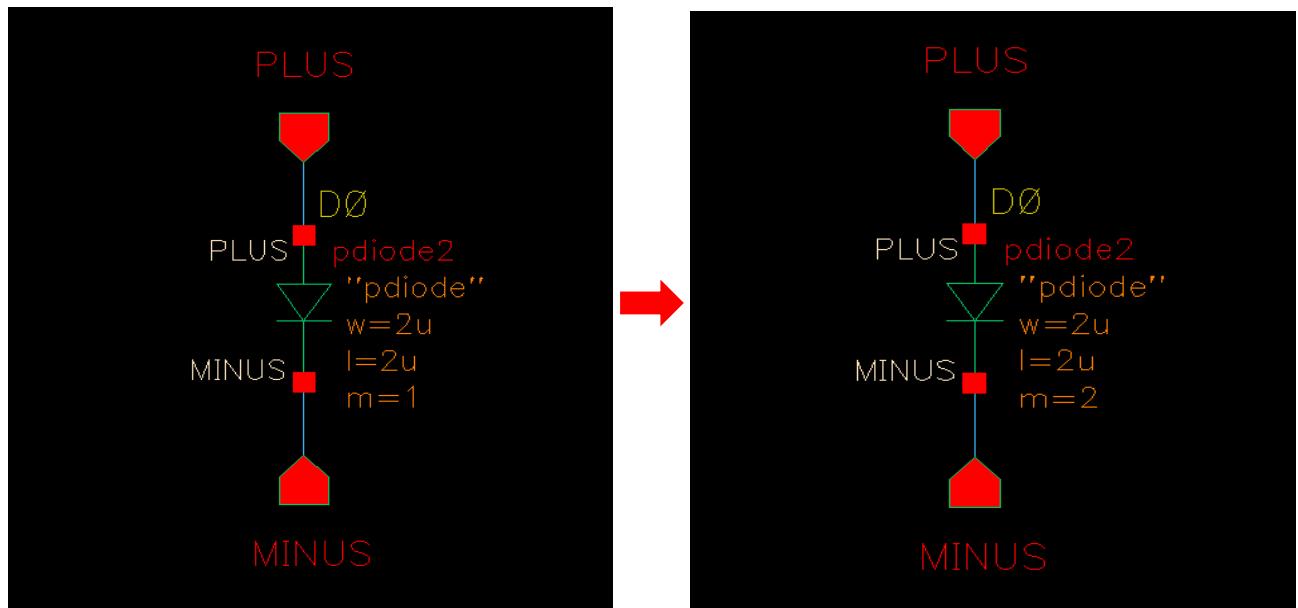
```
*****
* Library Name: ETRI_lay
* Cell Name: pdiode
* View Name: schematic
*****
.SUBCKT pdiode MINUS PLUS
*.PININFO MINUS:I PLUS:I
DD0 PLUS MINUS pdiode m=1 w=2u l=2u
.ENDS
```

```
*****
* Library Name: ETRI_lay
* Cell Name: pdiode
* View Name: schematic
*****
.SUBCKT pdiode MINUS PLUS
*.PININFO MINUS:I PLUS:I
DD0 PLUS MINUS pdiode m=2 w=6u l=5u
.ENDS
```

<cdl output>

3.19 pdiode2

Parameter					
Width	2.0u	Length	2.0u	multiplier	1 → 2



<Schematic parameter>

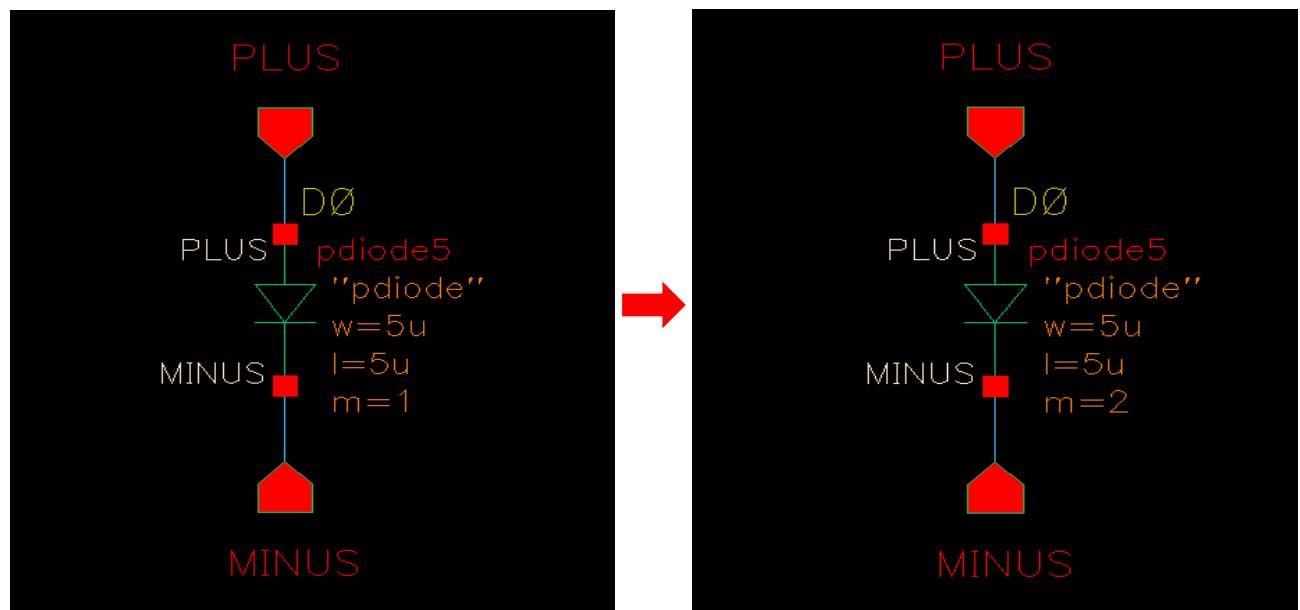
```
*****
* Library Name: ETRI_lay
* Cell Name: pdiode2
* View Name: schematic
*****  
  
.SUBCKT pdiode2 MINUS PLUS
*.PININFO MINUS:I PLUS:I
DD0 PLUS MINUS pdiode m=1 w=2u l=2u
.ENDS
```

```
*****
* Library Name: ETRI_lay
* Cell Name: pdiode2
* View Name: schematic
*****  
  
.SUBCKT pdiode2 MINUS PLUS
*.PININFO MINUS:I PLUS:I
DD0 PLUS MINUS pdiode m=2 w=2u l=2u
.ENDS
```

<cdl output>

3.20 pdiode5

Parameter					
Width	5.0u	Length	5.0u	multiplier	1 → 2



<Schematic parameter>

```
*****
* Library Name: ETRI_lay
* Cell Name: pdiode5
* View Name: schematic
*****  
  
.SUBCKT pdiode5 MINUS PLUS
*.PININFO MINUS:I PLUS:I
DD0 PLUS MINUS pdiode m=1 w=5u l=5u
.ENDS
```

```
*****
* Library Name: ETRI_lay
* Cell Name: pdiode5
* View Name: schematic
*****  
  
.SUBCKT pdiode5 MINUS PLUS
*.PININFO MINUS:I PLUS:I
DD0 PLUS MINUS pdiode m=2 w=5u l=5u
.ENDS
```

<cdl output>

3.21 pdiode10

Parameter					
Width	10.0u	Length	10.0u	multiplier	1 → 2



<Schematic parameter>

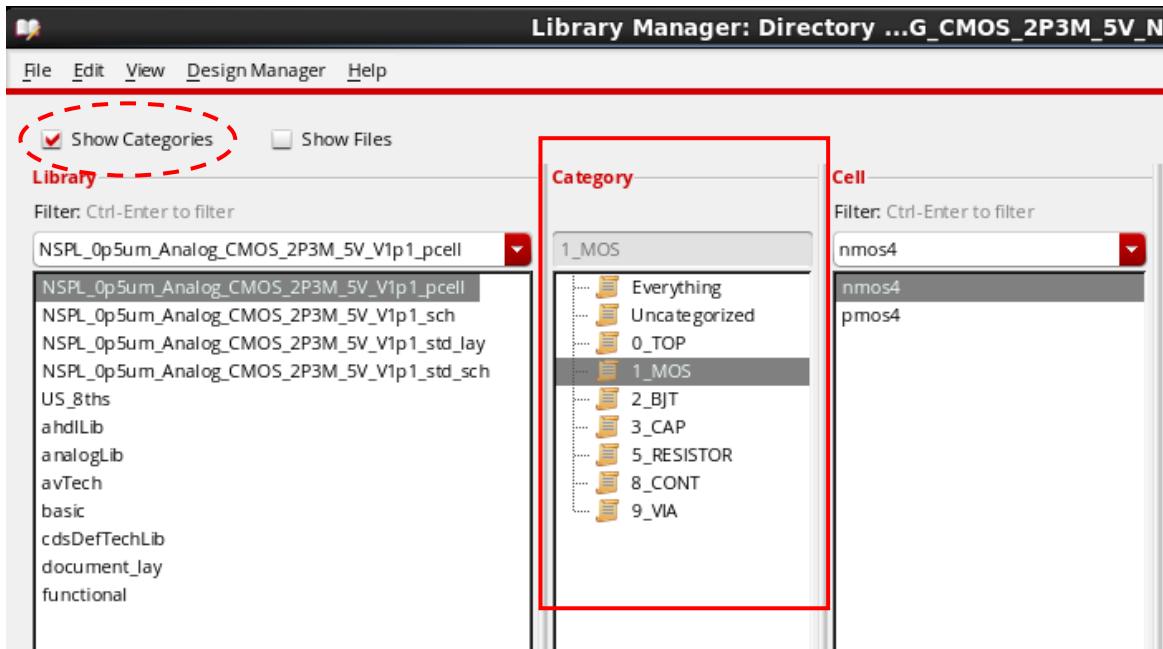
```
*****
* Library Name: ETRI_lay
* Cell Name: pdiode10
* View Name: schematic
*****
.SUBCKT pdiode10 MINUS PLUS
*.PININFO MINUS:I PLUS:I
DD0 PLUS MINUS pdiode m=1 w=10u l=10u
.ENDS
```

```
*****
* Library Name: ETRI_lay
* Cell Name: pdiode10
* View Name: schematic
*****
.SUBCKT pdiode10 MINUS PLUS
*.PININFO MINUS:I PLUS:I
DD0 PLUS MINUS pdiode m=2 w=10u l=10u
.ENDS
```

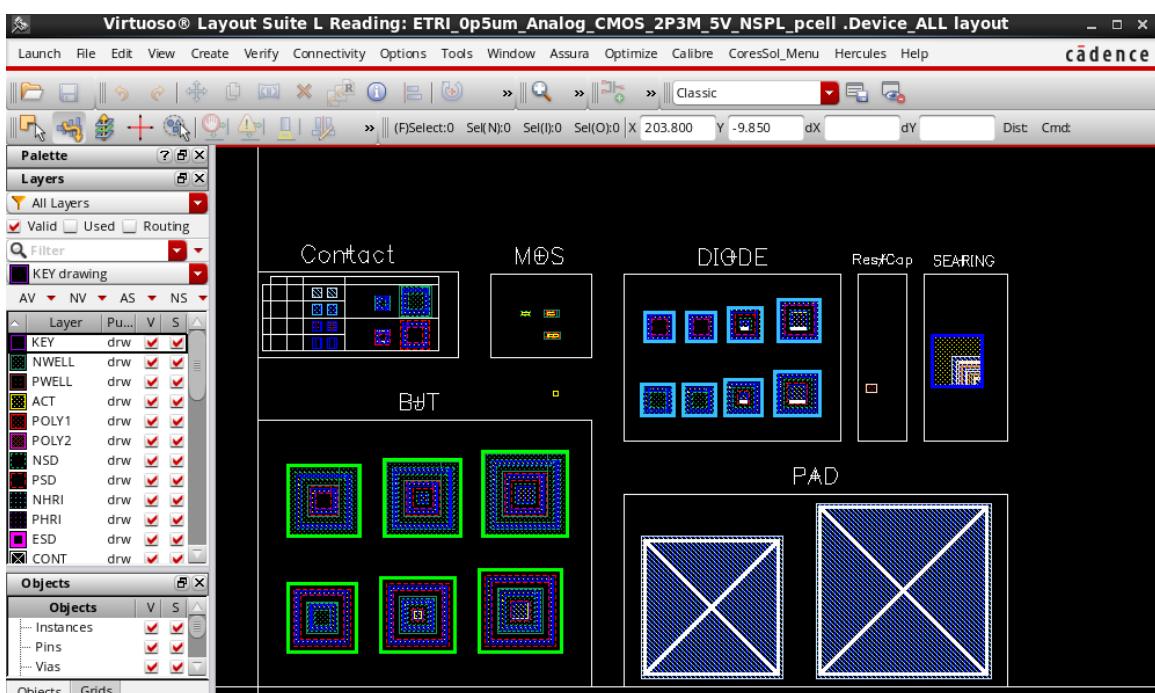
<cdl output>

4. PCELL Layout Library

4.1 Library Category

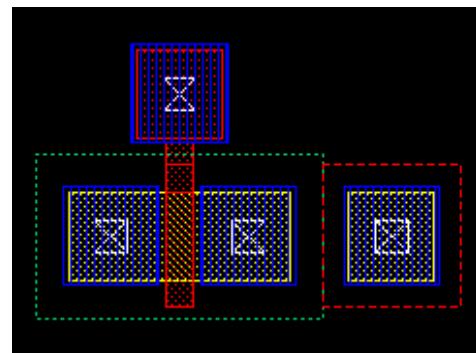


4.2 .Device_ALL

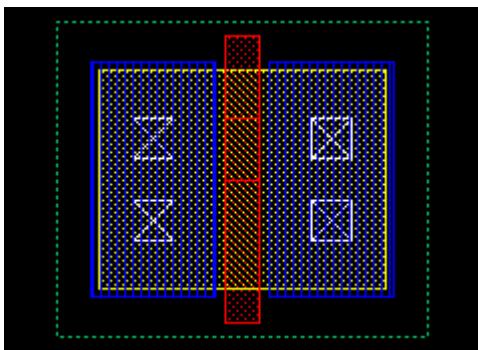


4.3 nmos4

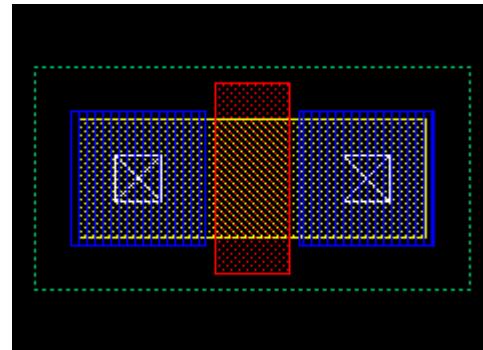
Parameter	Default	Change
width	1.6	<i>value</i>
length	0.5	<i>value</i>
multi	1	<i>value</i>
polyshift	0	<i>value</i>
polynumber	1	<i>value</i>
polycont	<input checked="" type="checkbox"/>	<input type="checkbox"/>
ptap	<input checked="" type="checkbox"/>	<input type="checkbox"/>



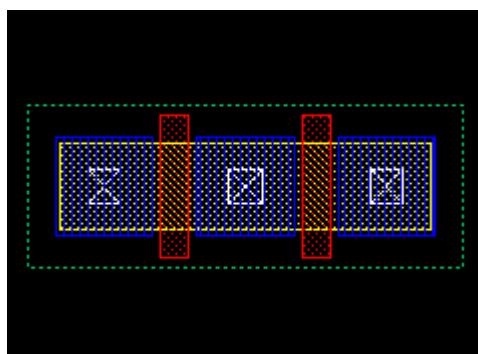
width	1.6	3.2
-------	-----	-----



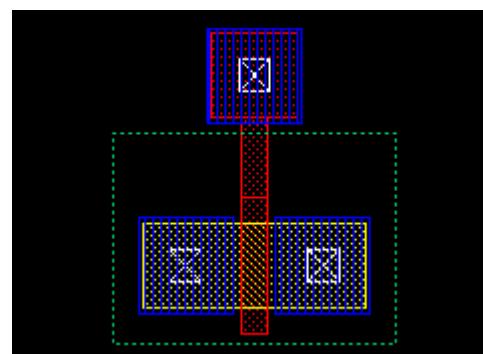
length	0.5	1.0
--------	-----	-----



multi	1	2
-------	---	---

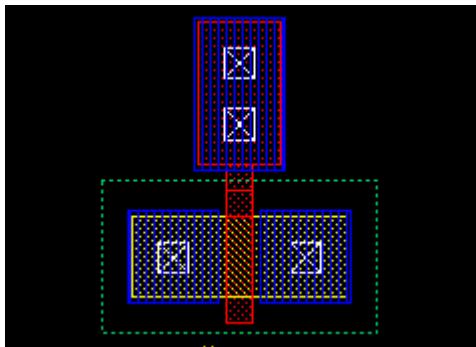


polyshift	0	1
-----------	---	---

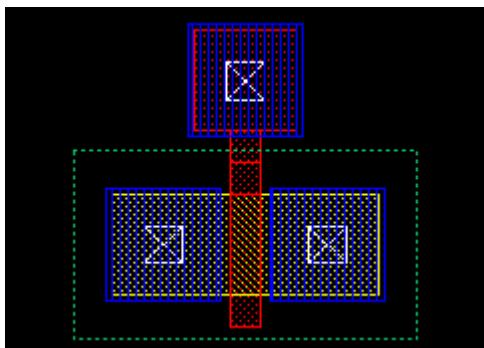


4.3 nmos4

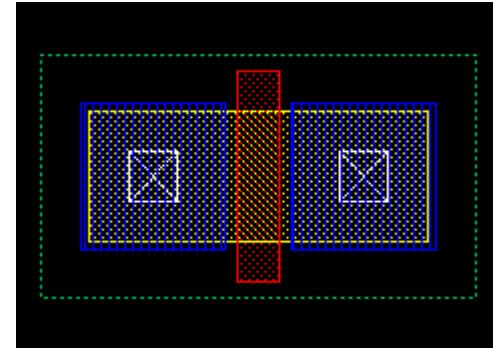
polynumber	1	2
------------	---	---



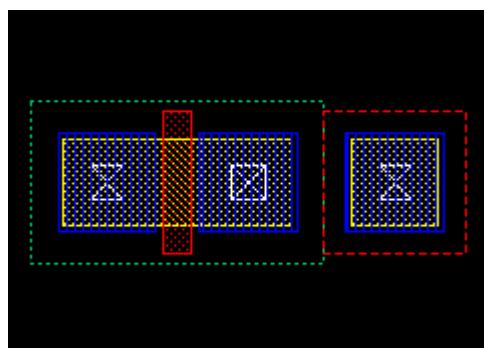
polycont	<input checked="" type="checkbox"/>
----------	-------------------------------------



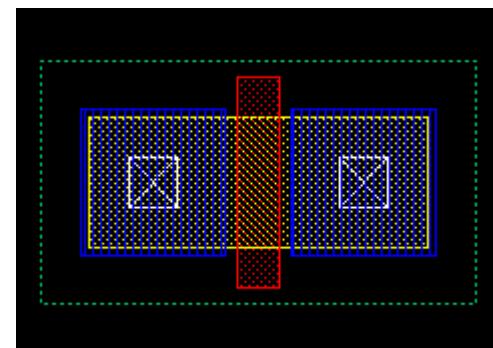
polycont	<input type="checkbox"/>
----------	--------------------------



ptap	<input checked="" type="checkbox"/>
------	-------------------------------------

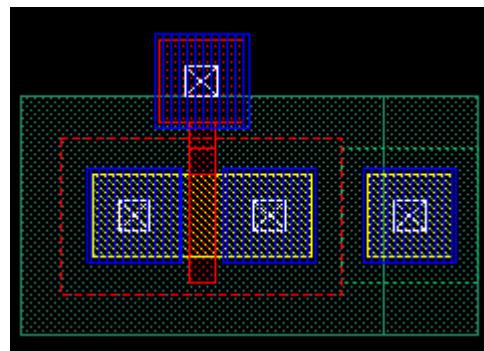


ptap	<input type="checkbox"/>
------	--------------------------

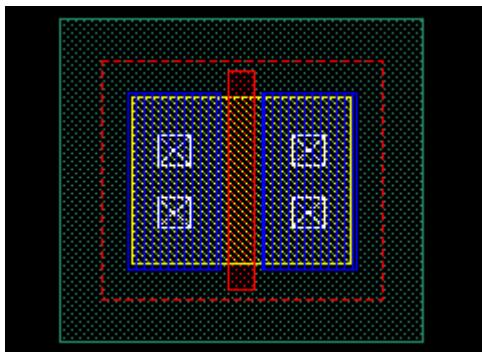


4.4 pmos4

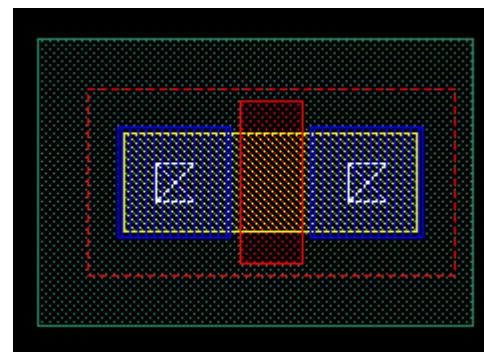
Parameter	Default	Change
width	1.6	<i>value</i>
length	0.5	<i>value</i>
multi	1	<i>value</i>
polyshift	0	<i>value</i>
polynumber	1	<i>value</i>
polycont	<input checked="" type="checkbox"/>	<input type="checkbox"/>
ntap	<input checked="" type="checkbox"/>	<input type="checkbox"/>



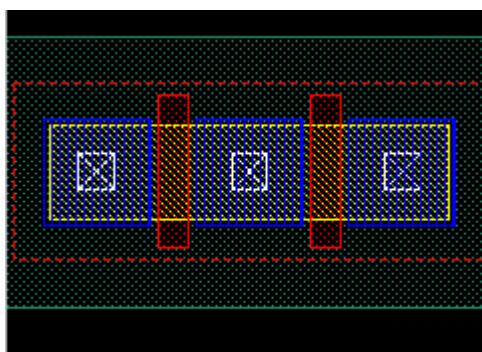
width	1.6	3.2
-------	-----	-----



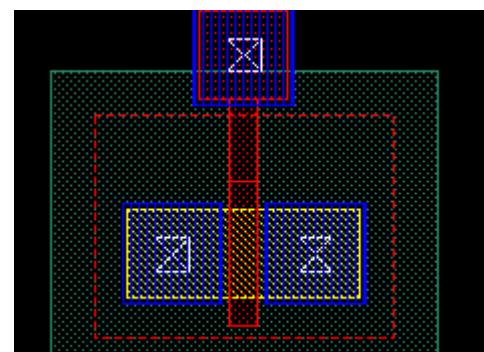
length	0.5	1.0
--------	-----	-----



multi	1	2
-------	---	---

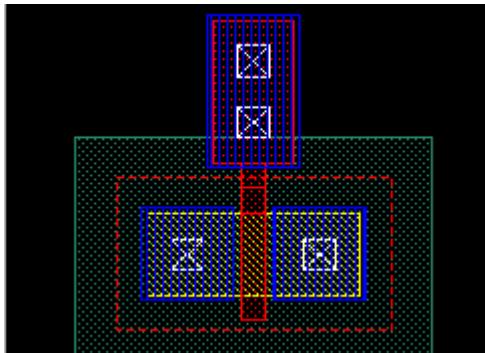


polyshift	0	1
-----------	---	---

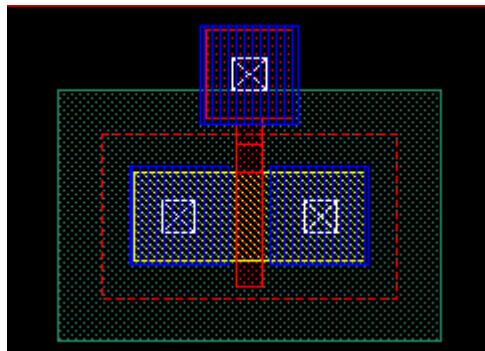


4.4 pmos4

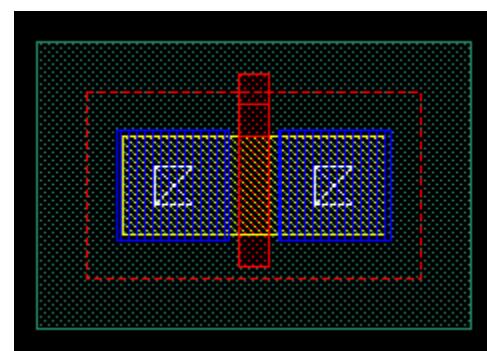
polynumber	1	2
------------	---	---



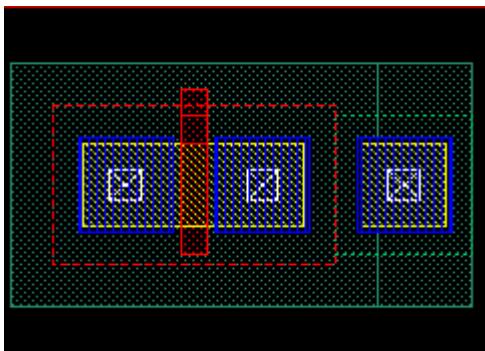
polycont	<input checked="" type="checkbox"/>
----------	-------------------------------------



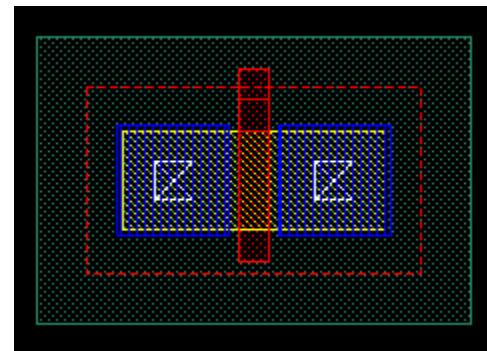
polycont	<input type="checkbox"/>
----------	--------------------------



ntap	<input checked="" type="checkbox"/>
------	-------------------------------------

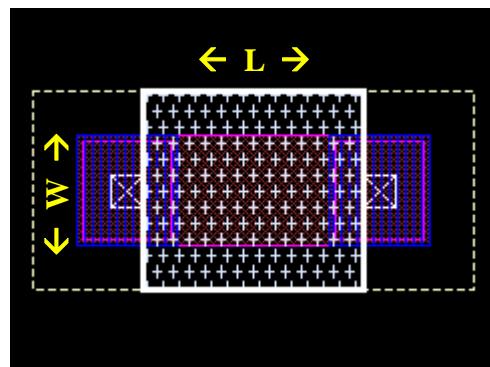


ntap	<input type="checkbox"/>
------	--------------------------

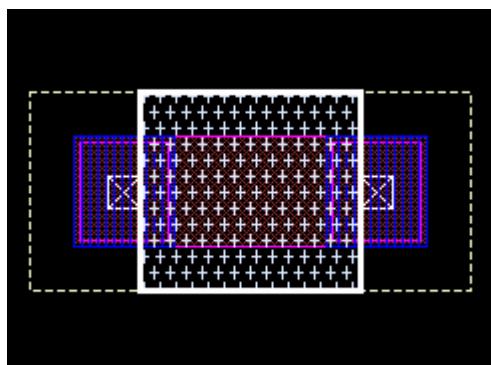


4.5 p2res

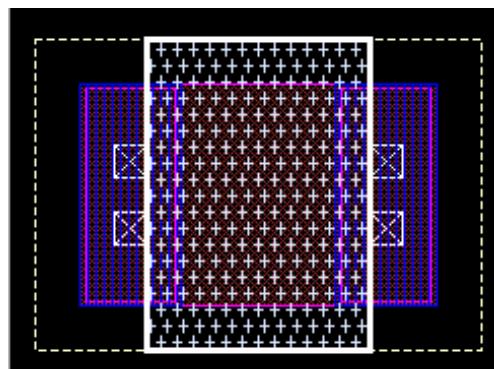
Parameter	Default	Change
W	2	value
L	4	value



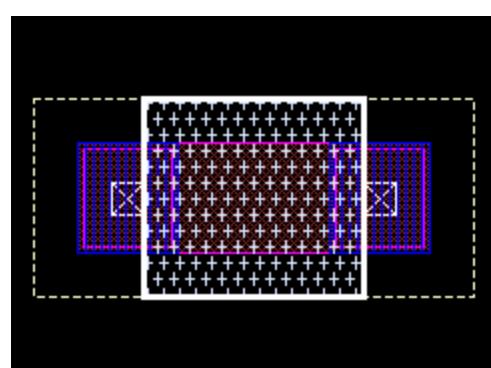
W	2
---	---



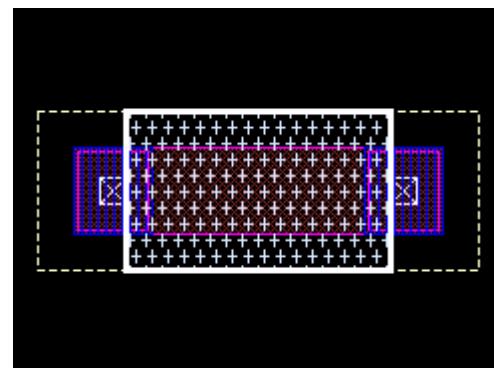
W	4
---	---



L	4
---	---

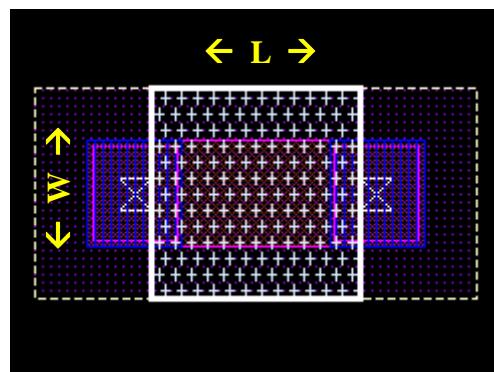


L	6
---	---

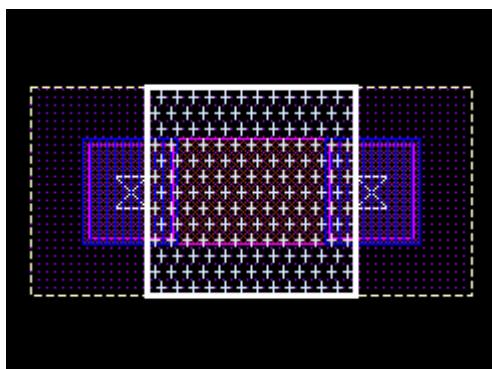


4.6 p2hres

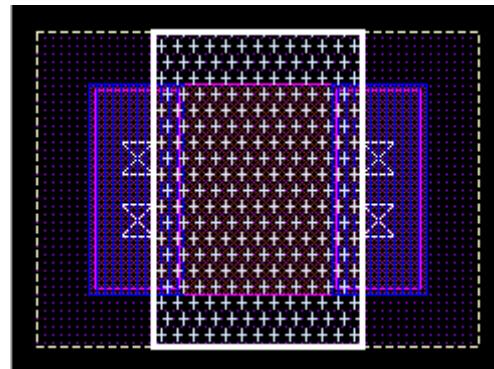
Parameter	Default	Change
W	2	value
L	4	value



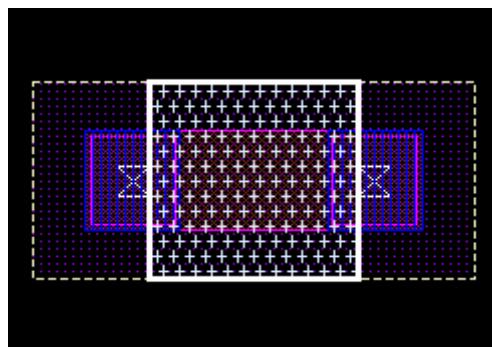
W	2
---	---



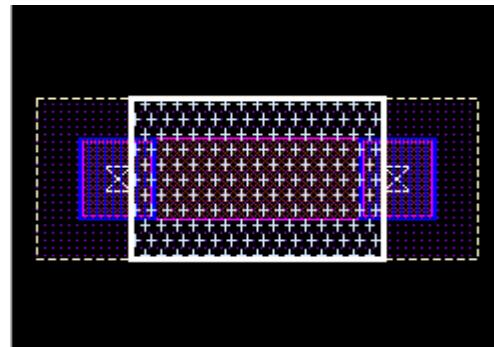
W	4
---	---



L	4
---	---

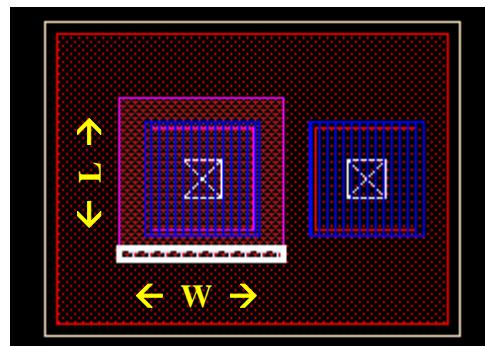


L	6
---	---

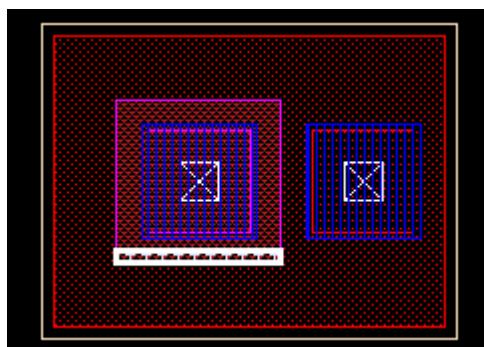


4.7 pipcap

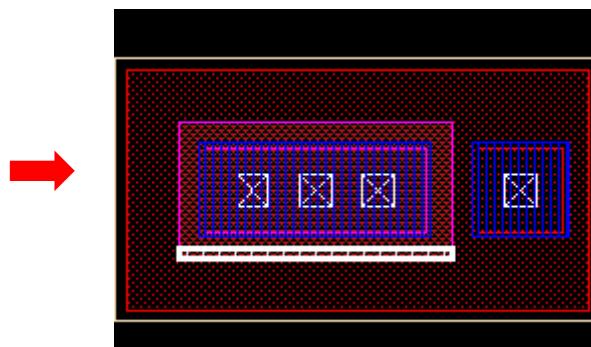
Parameter	Default	Change
W	2.6	<i>value</i>
L	2.6	<i>value</i>



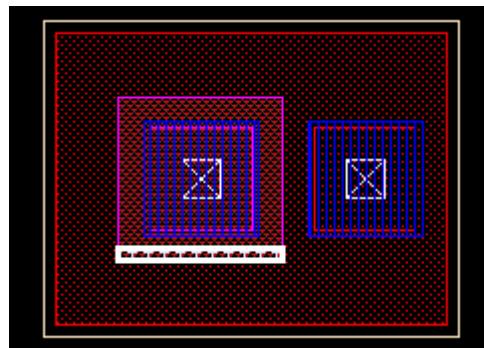
W	2.6
---	-----



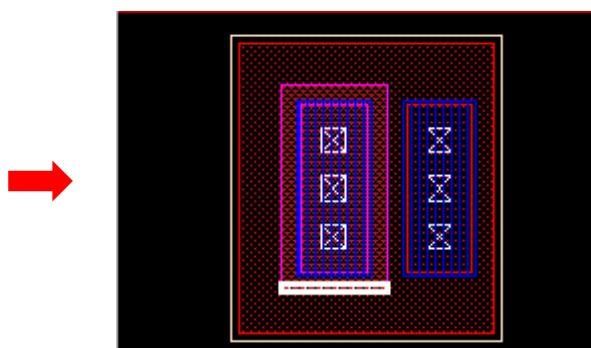
W	5.2
---	-----



L	2.6
---	-----

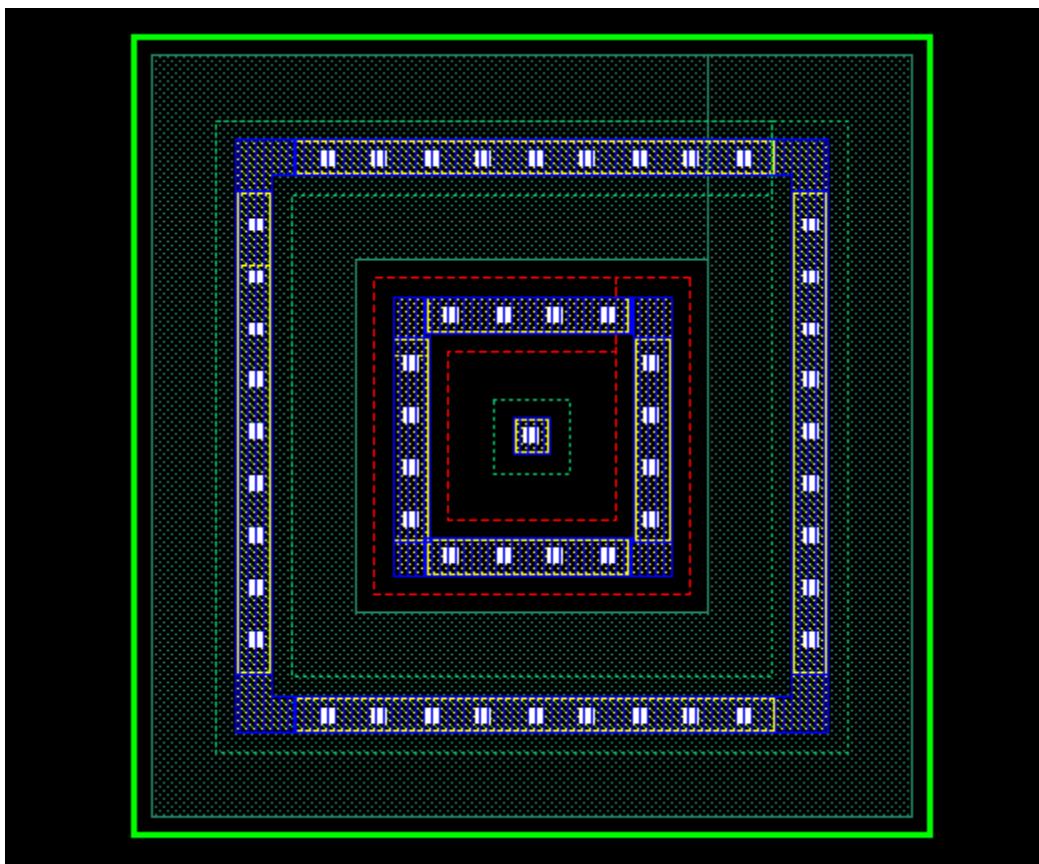


L	5.2
---	-----



4.8 npn2

Parameter	Default	Change
-	-	-

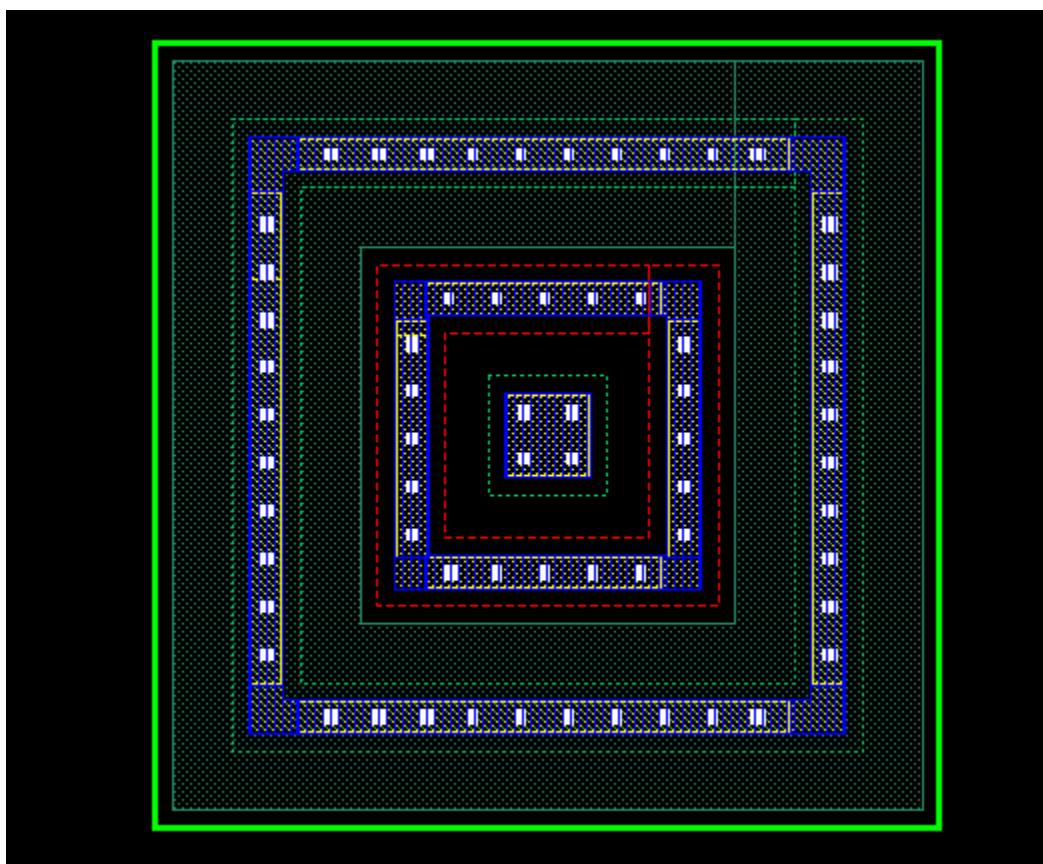


**BJT doesn't change PCELL
It must be used PCELL**

**BJT layer on BJT device
can't be overlapped each other**

4.9 npn5

Parameter	Default	Change
-	-	-

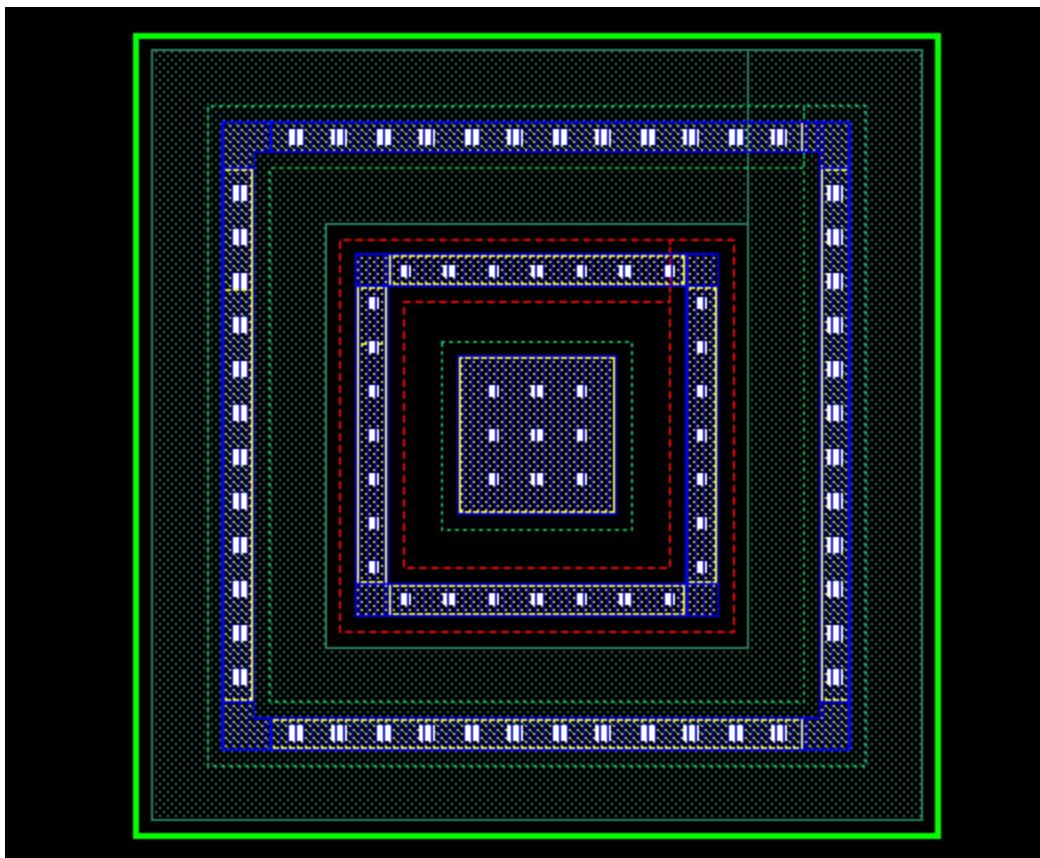


**BJT doesn't change PCELL
It must be used PCELL**

**BJT layer on BJT device
can't be overlapped each other**

4.10 npn10

Parameter	Default	Change
-	-	-

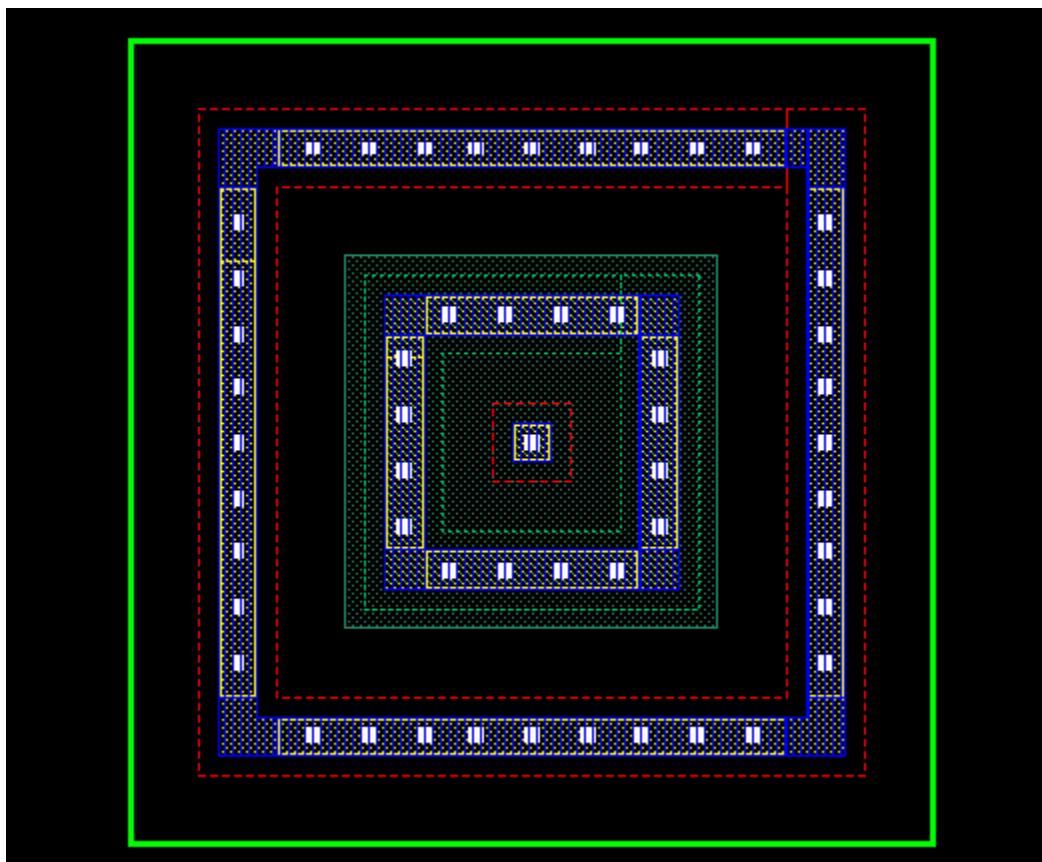


**BJT doesn't change PCELL
It must be used PCELL**

**BJT layer on BJT device
can't be overlapped each other**

4.11 pnp2

Parameter	Default	Change
-	-	-

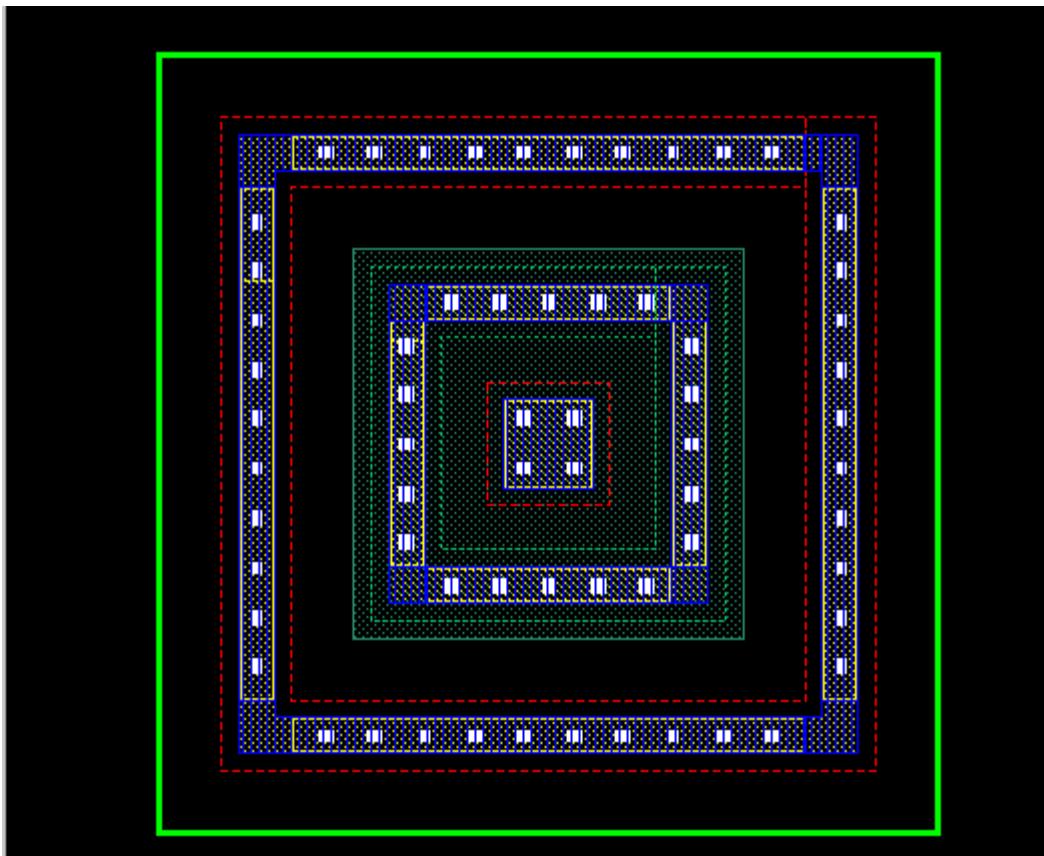


**BJT doesn't change PCELL
It must be used PCELL**

**BJT layer on BJT device
can't be overlapped each other**

4.12 pnp5

Parameter	Default	Change
-	-	-

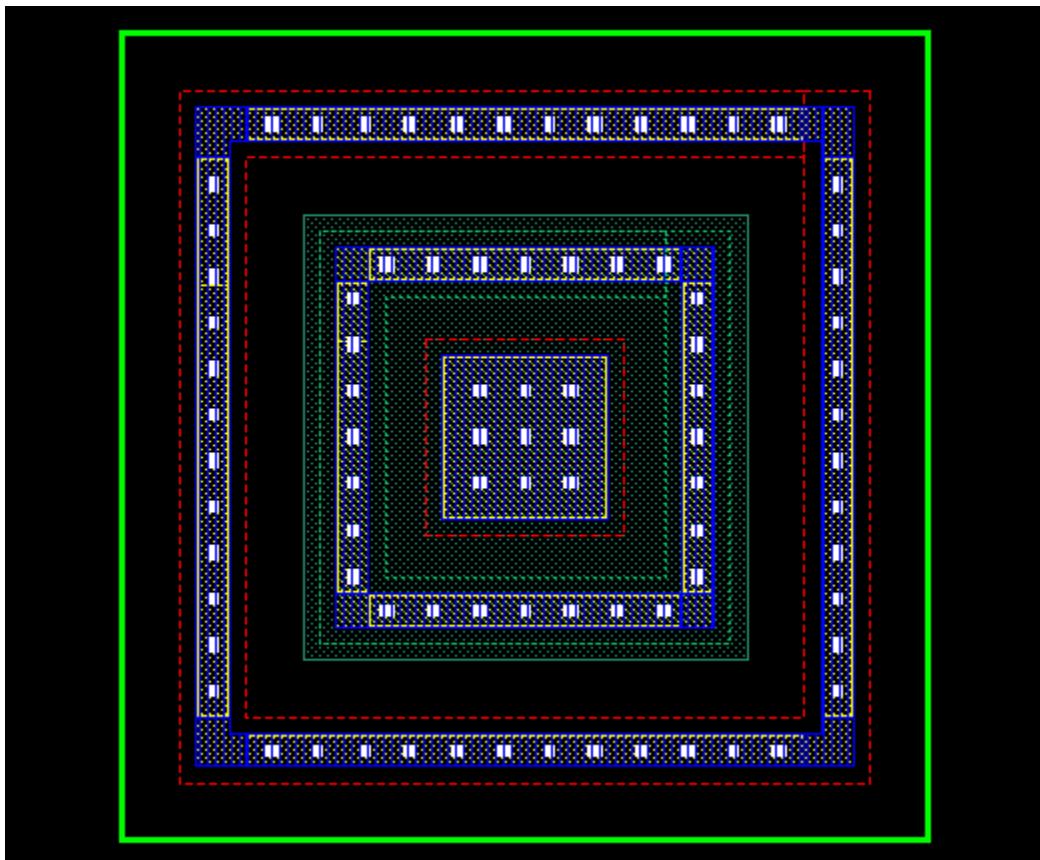


**BJT doesn't change PCELL
It must be used PCELL**

**BJT layer on BJT device
can't be overlapped each other**

4.13 pnp10

Parameter	Default	Change
-	-	-

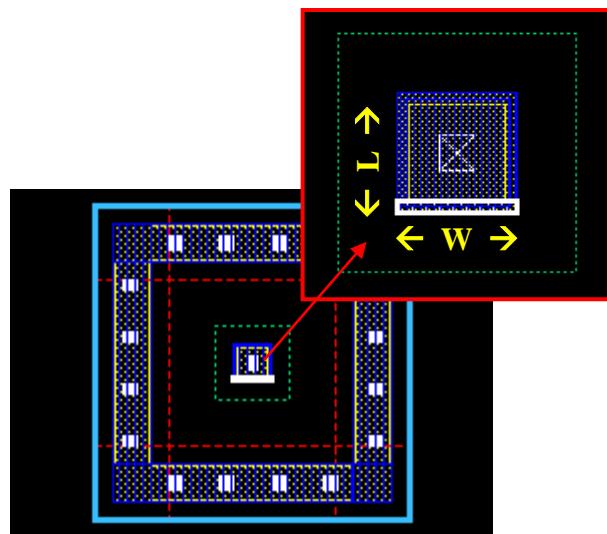


**BJT doesn't change PCELL
It must be used PCELL**

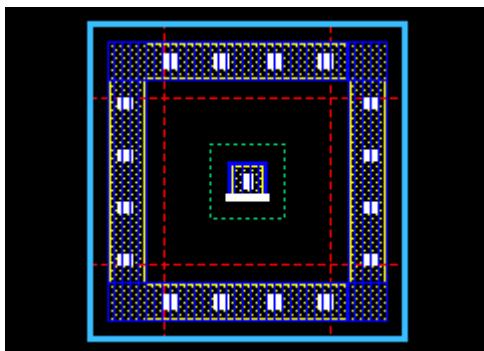
**BJT layer on BJT device
can't be overlapped each other**

4.14 n diode

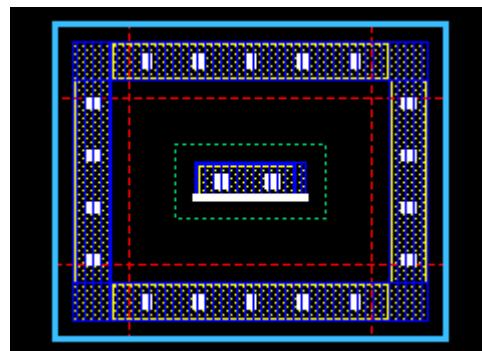
Parameter	Default	Change
W	2	value
L	2	value



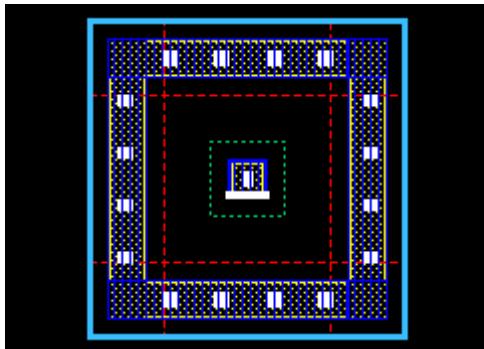
W	2
---	---



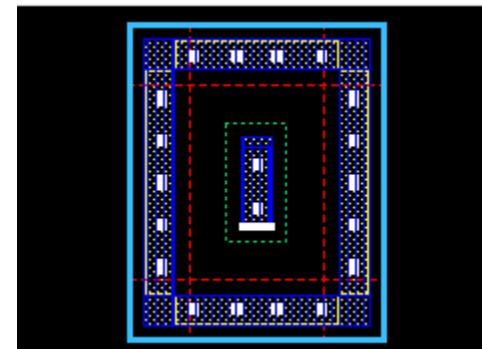
W	6
---	---



L	2
---	---

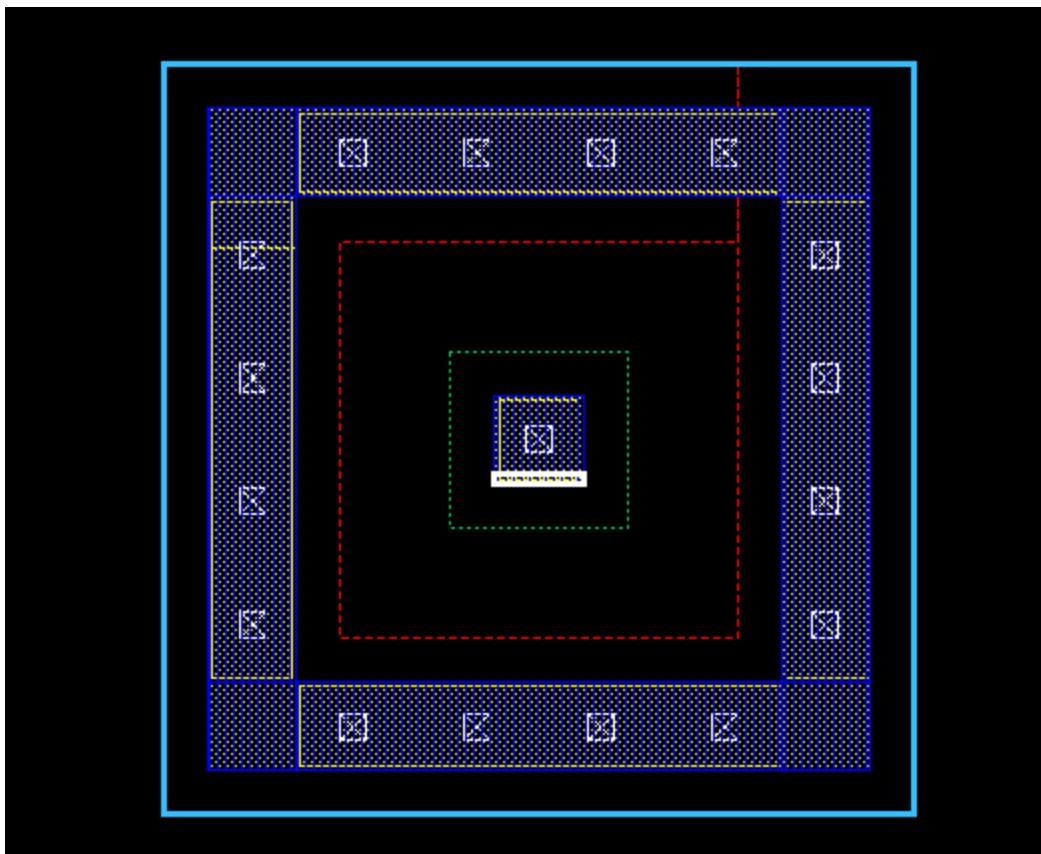


L	6
---	---



4.15 ndiode2

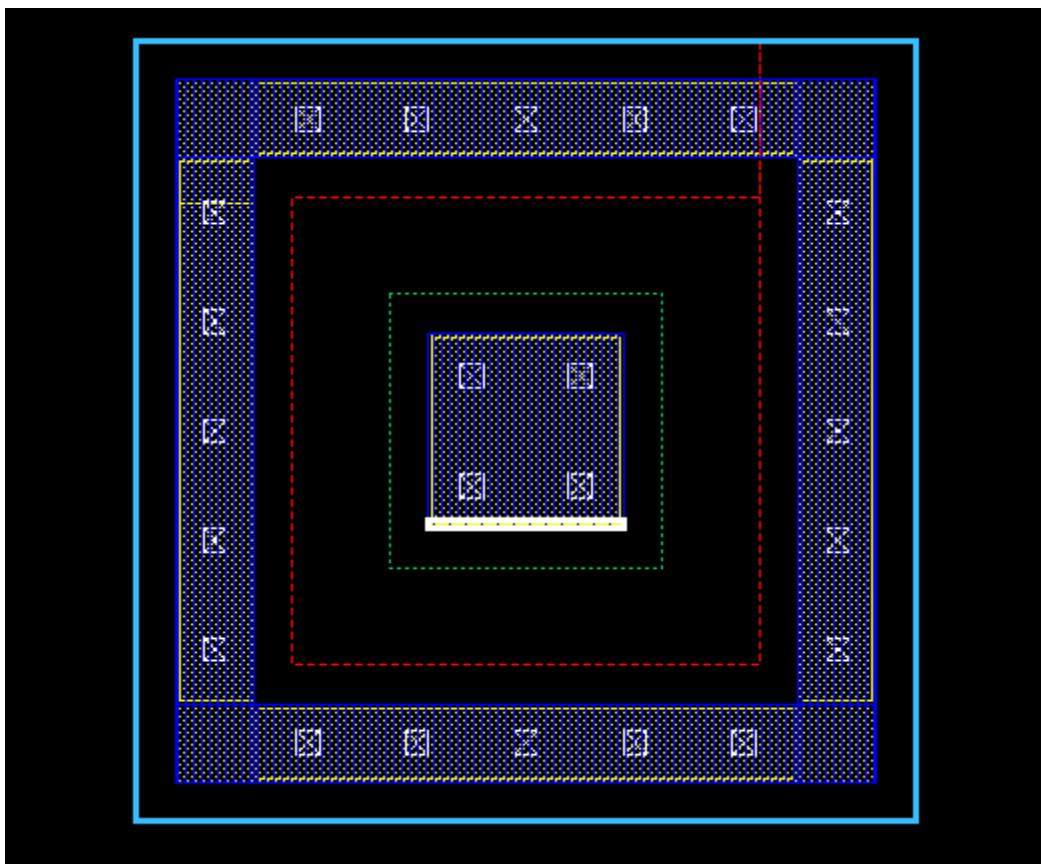
Parameter	Default	Change
-	-	-



NDIODE Fixed Size
→ doesn't provide parameter modification

4.16 ndiode5

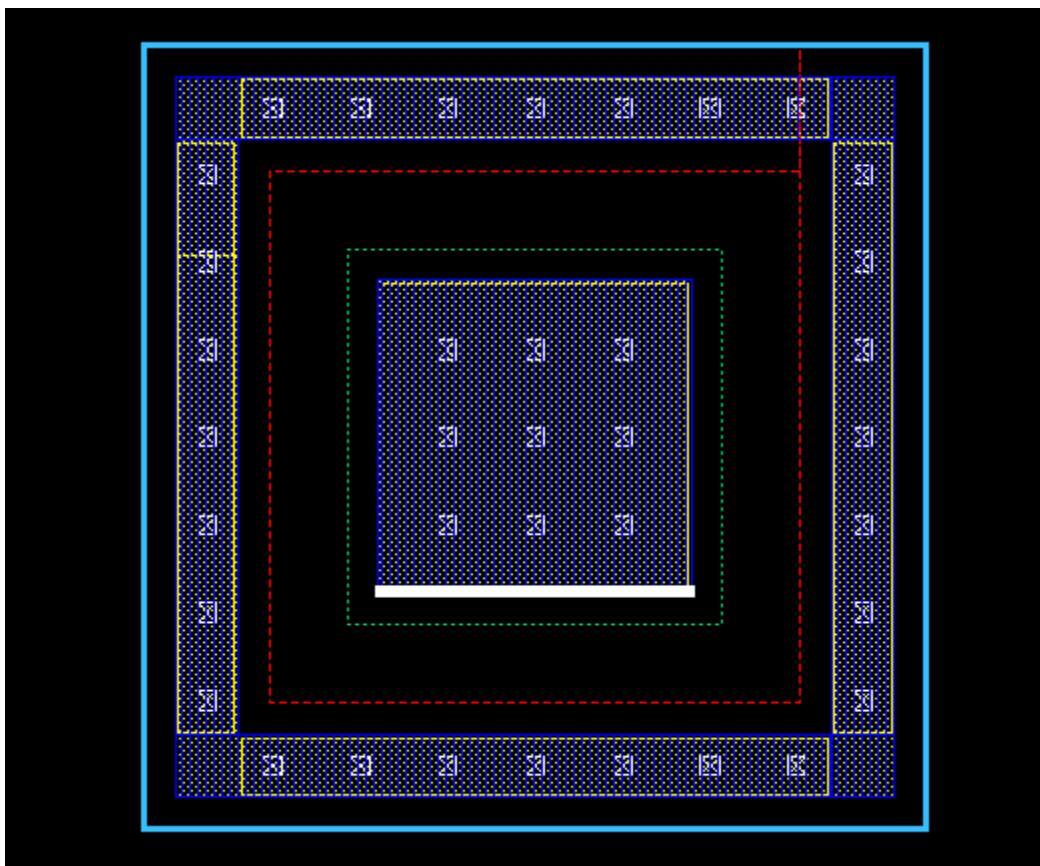
Parameter	Default	Change
-	-	-



NDIODE Fixed Size
→ doesn't provide parameter modification

4.17 ndiode10

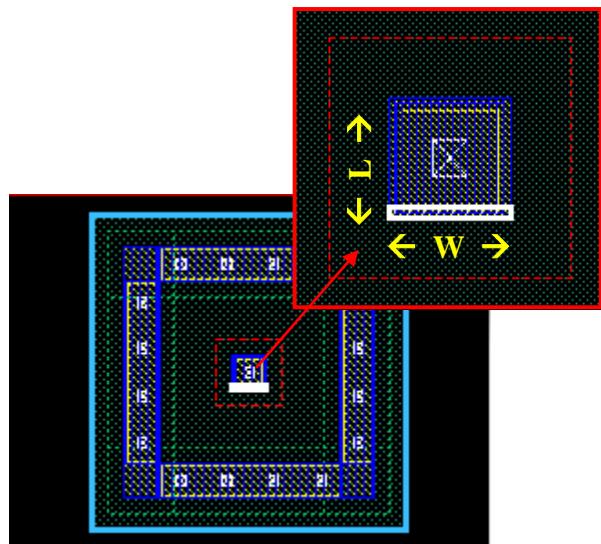
Parameter	Default	Change
-	-	-



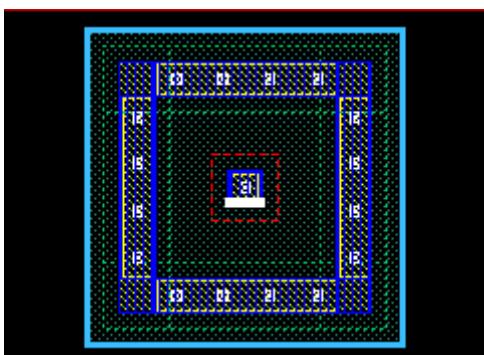
NDIODE Fixed Size
→ doesn't provide parameter modification

4.18 pdiode

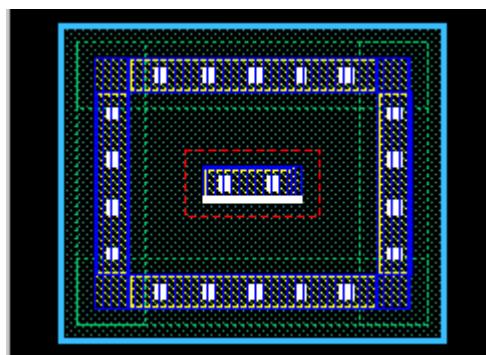
Parameter	Default	Change
W	2	value
L	2	value



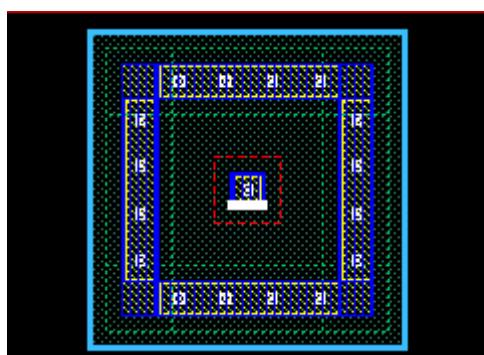
W	2
---	---



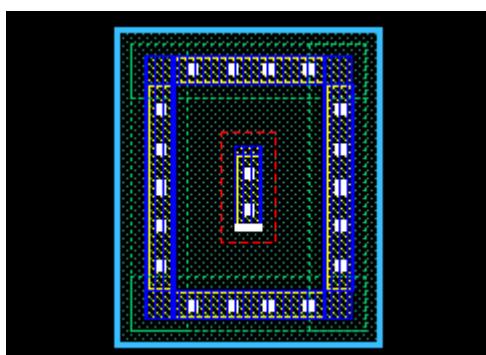
W	6
---	---



L	2
---	---

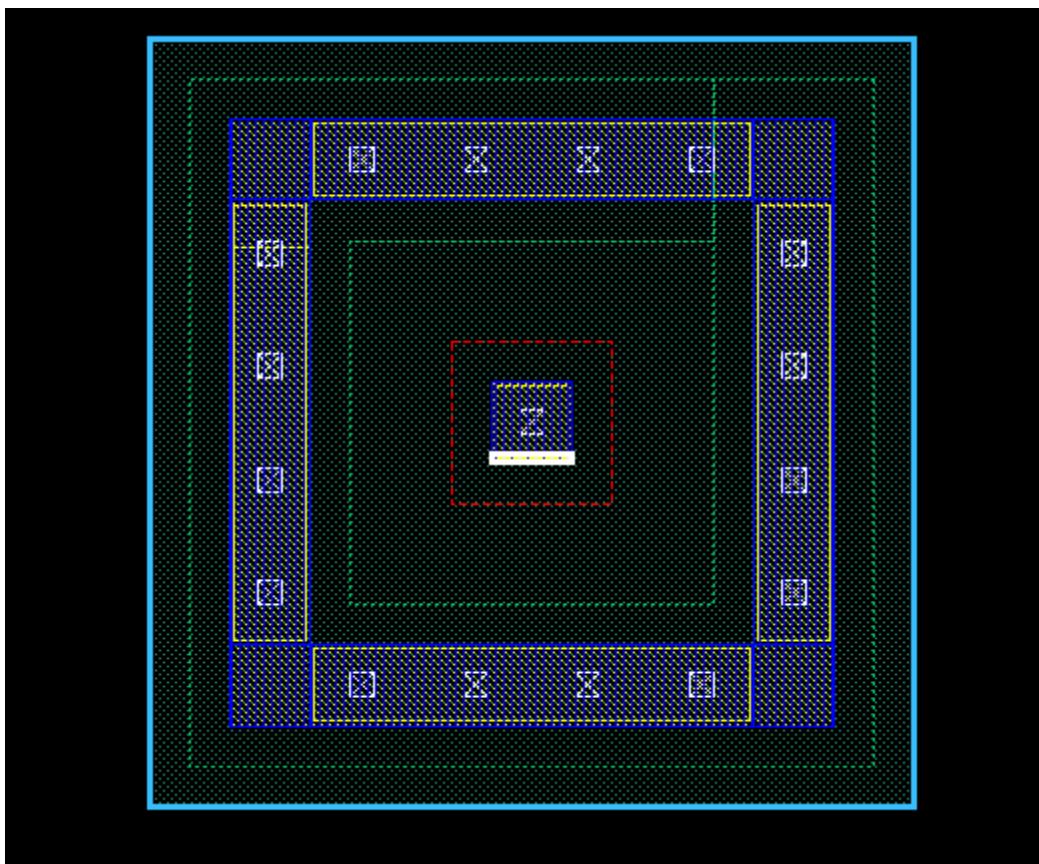


L	6
---	---



4.19 pdiode2

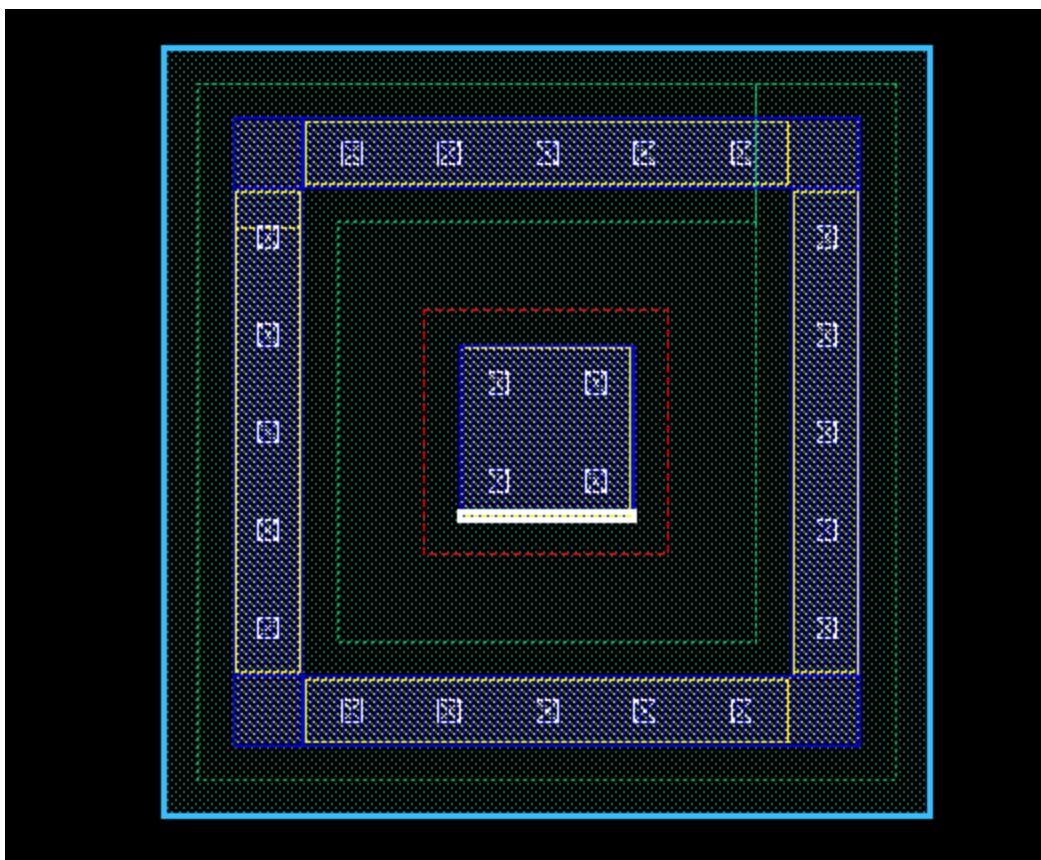
Parameter	Default	Change
-	-	-



PDIODE Fixed Size
→ doesn't provide parameter modification

4.20 pdiode5

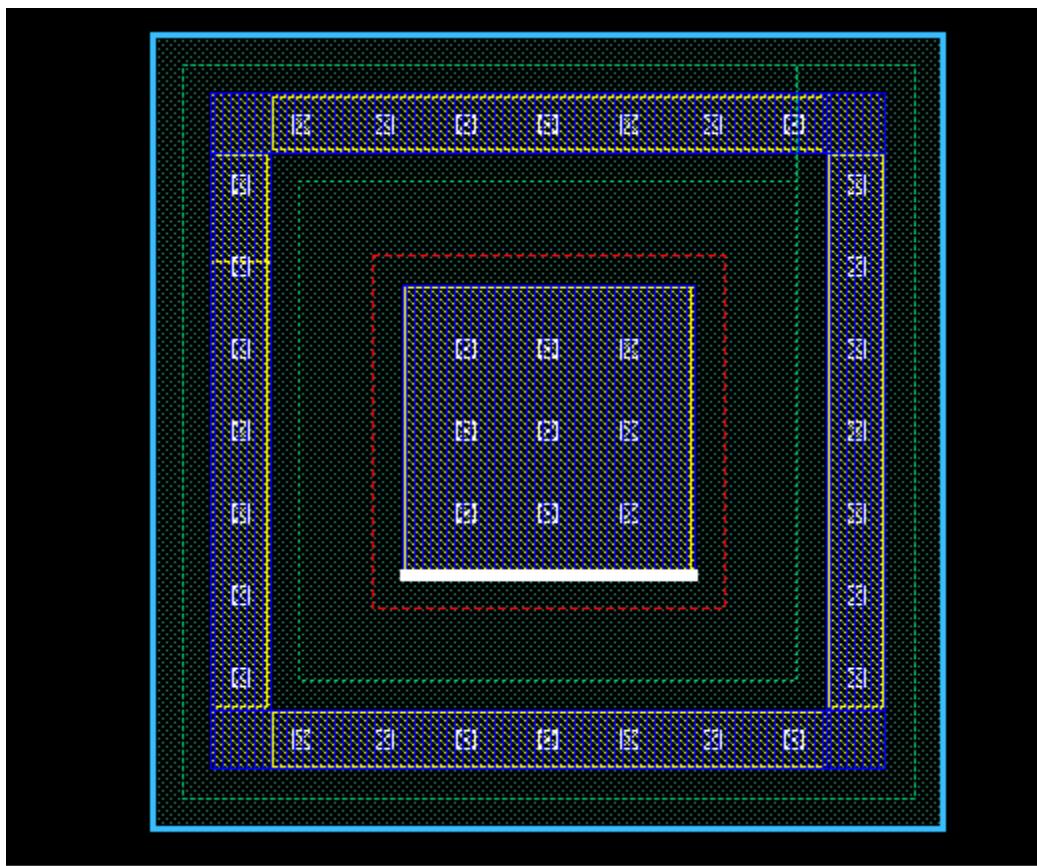
Parameter	Default	Change
-	-	-



PDIODE Fixed Size
→ doesn't provide parameter modification

4.21 pdiode10

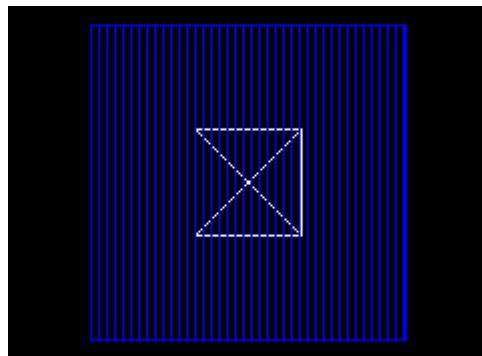
Parameter	Default	Change
-	-	-



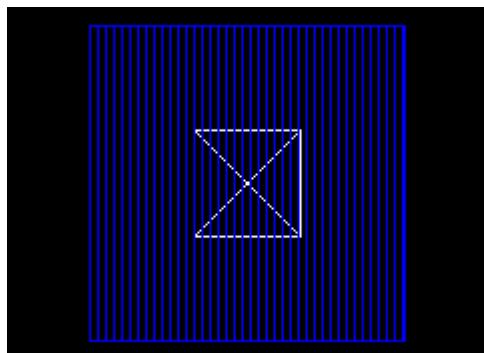
PDIODE Fixed Size
→ doesn't provide parameter modification

4.22 cont

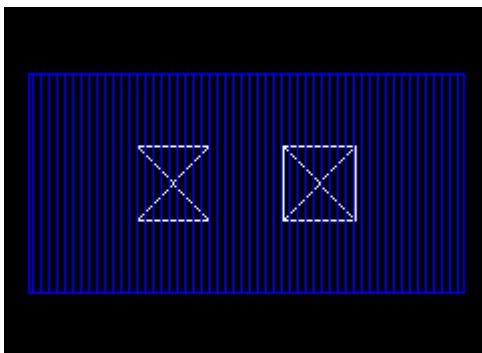
Parameter	Default	Change
x_size	1.8	<i>value</i>
y_size	1.8	<i>value</i>



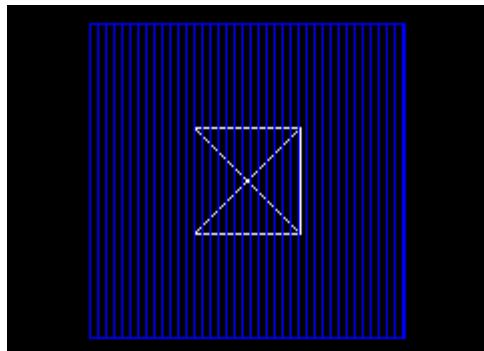
x_size	1.8
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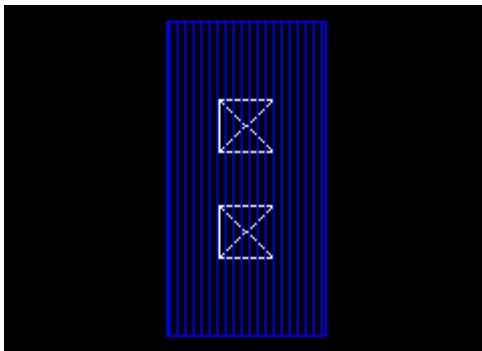
x_size	3.6
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y_size	1.8
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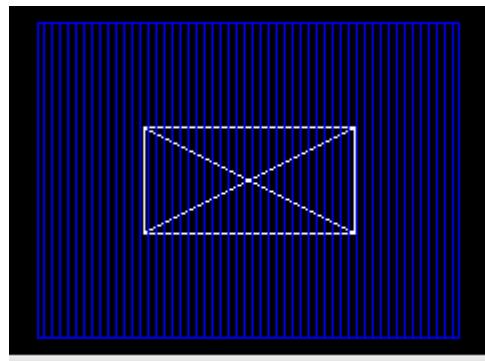


y_size	3.6
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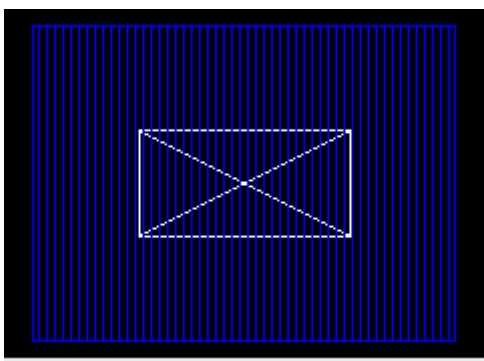


4.23 cont_bar

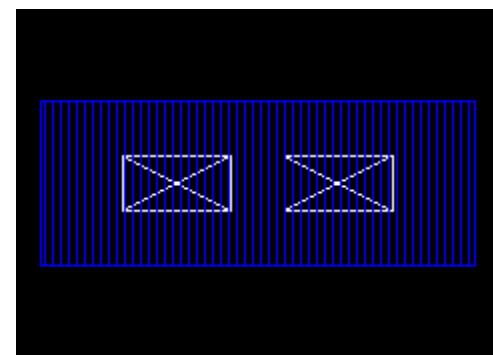
Parameter	Default	Change
x_size	2.4	<i>value</i>
y_size	1.8	<i>value</i>



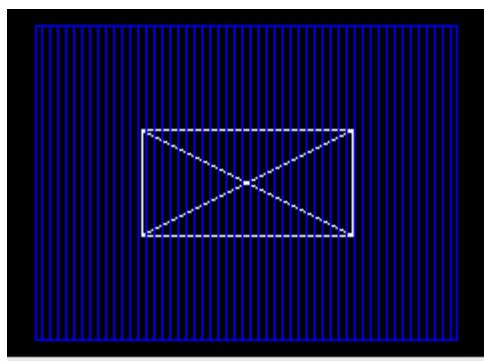
x_size	2.4
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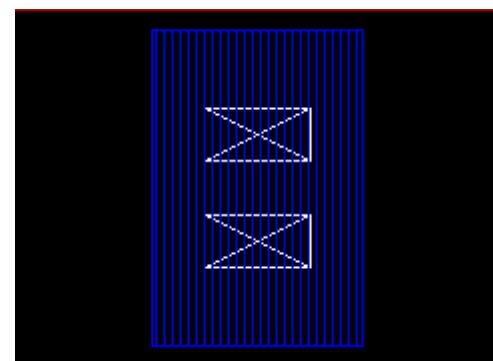
x_size	4.8
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y_size	1.8
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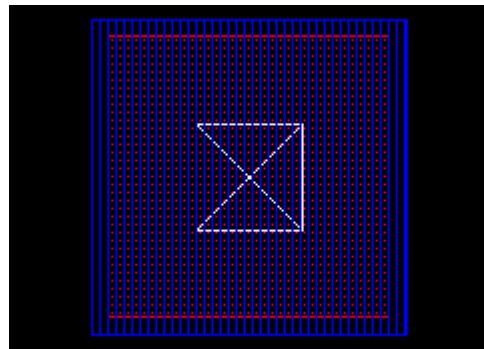


y_size	3.6
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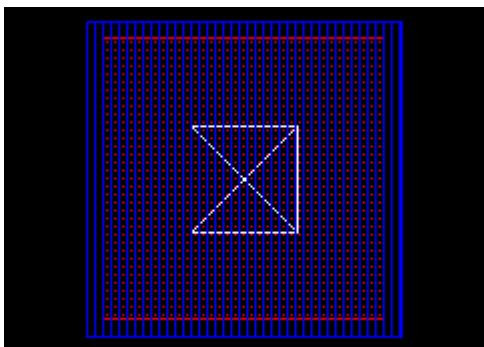


4.24 poly1cont

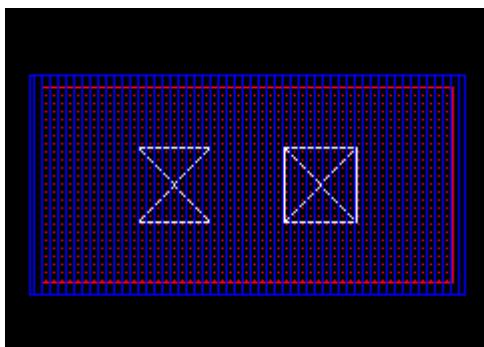
Parameter	Default	Change
x_size	1.8	<i>value</i>
y_size	1.8	<i>value</i>



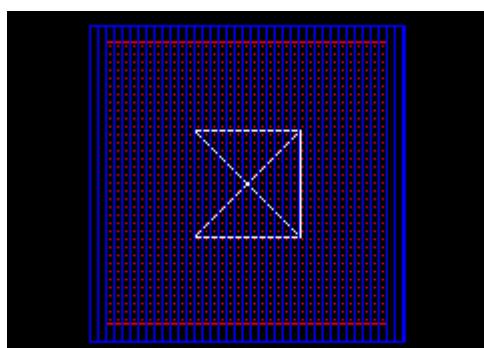
x_size	1.8
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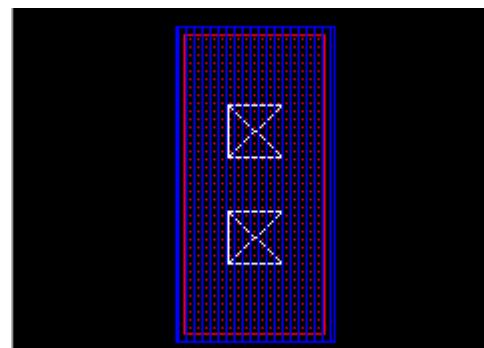
x_size	3.6
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y_size	1.8
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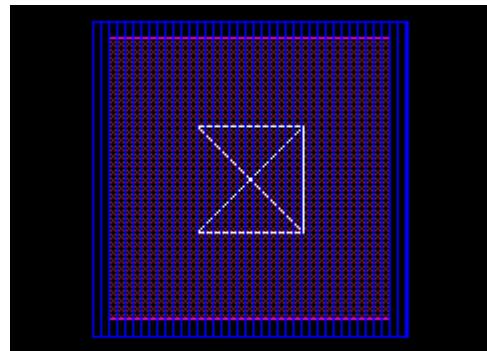


y_size	3.6
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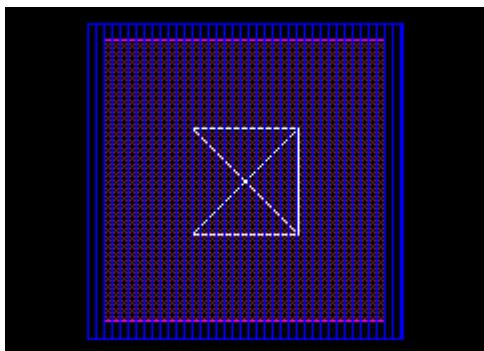


4.25 poly2cont

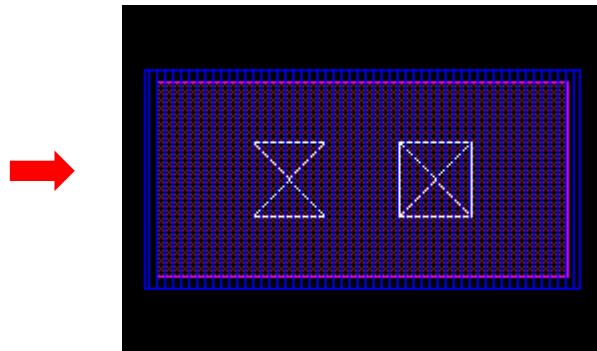
Parameter	Default	Change
x_size	1.8	<i>value</i>
y_size	1.8	<i>value</i>



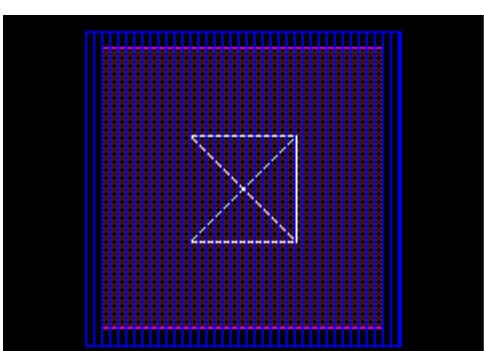
x_size	1.8
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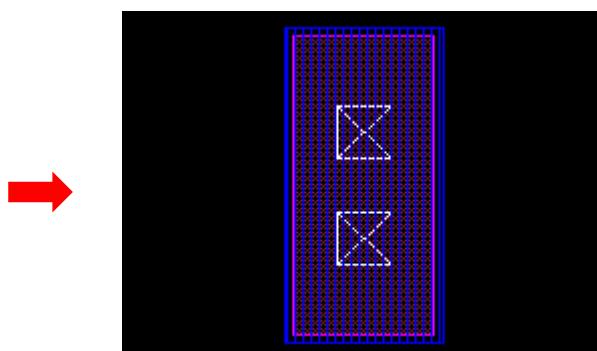
x_size	3.6
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y_size	1.8
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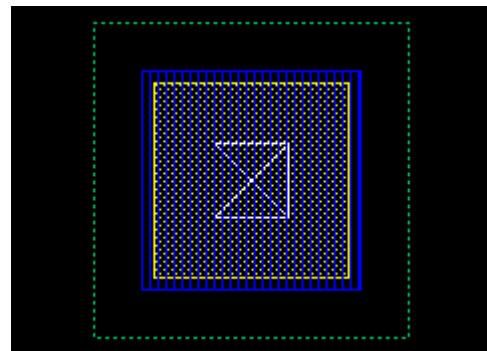


y_size	3.6
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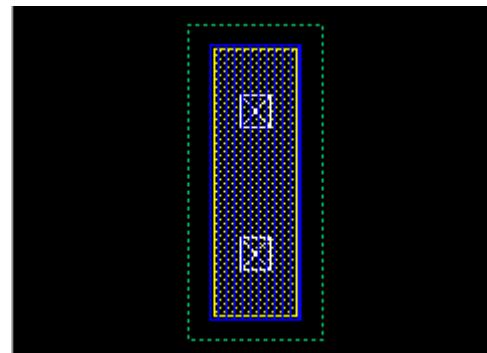
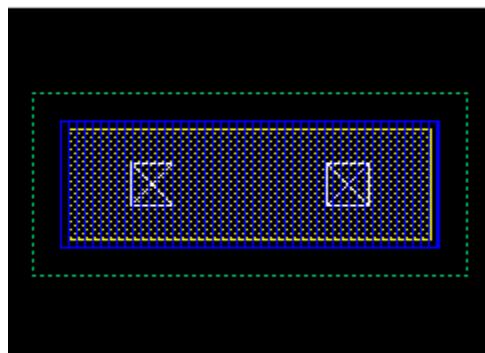
4.26 ntap

Parameter	Default	Change
x_size	1.8	<i>value</i>
y_size	1.8	<i>value</i>
NSD	<input checked="" type="checkbox"/>	<input type="checkbox"/>



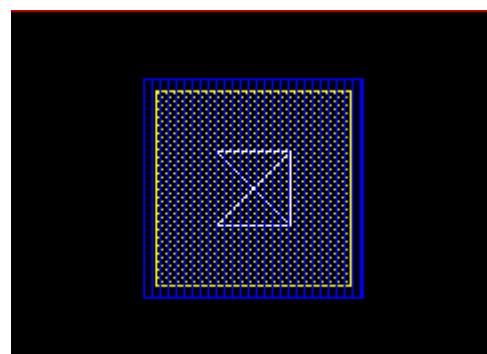
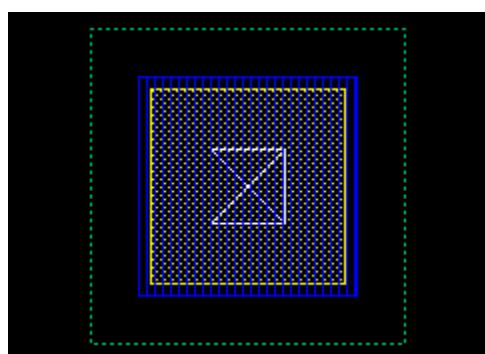
x_size	1.8	5.4
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y_size	1.8	5.4
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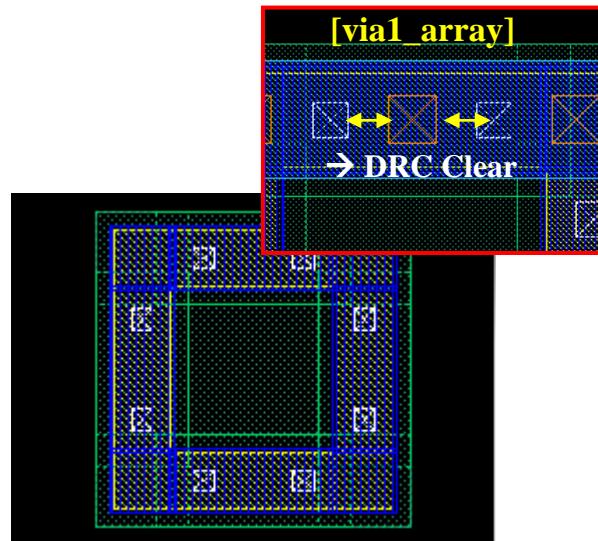
NSD	<input checked="" type="checkbox"/>
-----	-------------------------------------

NSD	<input type="checkbox"/>
-----	--------------------------

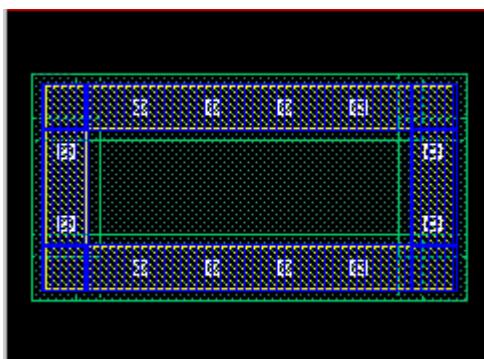


4.27 ntap_ring

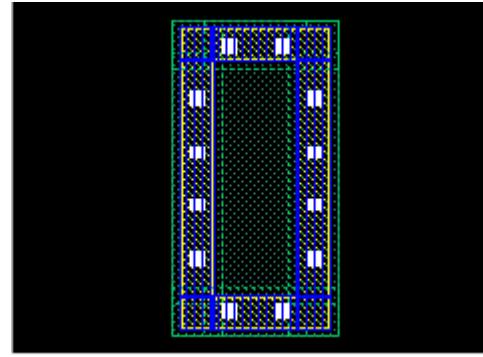
Parameter	Default	Change
x_size	8	<i>value</i>
y_size	8	<i>value</i>
TOP	<input checked="" type="checkbox"/>	<input type="checkbox"/>
BOTTOM	<input checked="" type="checkbox"/>	<input type="checkbox"/>
LEFT	<input checked="" type="checkbox"/>	<input type="checkbox"/>
RIGHT	<input checked="" type="checkbox"/>	<input type="checkbox"/>



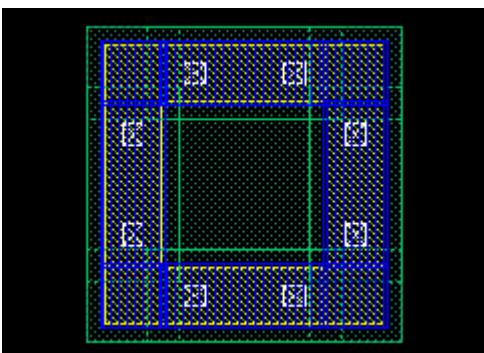
x_size	8	16
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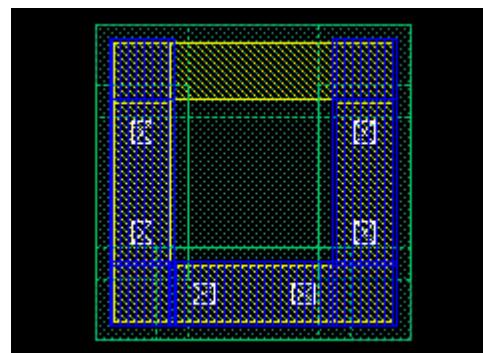
y_size	8	16
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TOP	<input checked="" type="checkbox"/>
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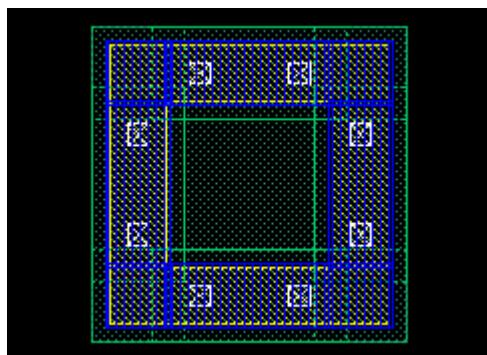


TOP	<input type="checkbox"/>
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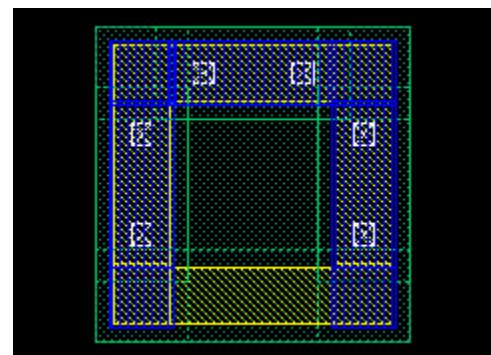


4.27 ntap_ring

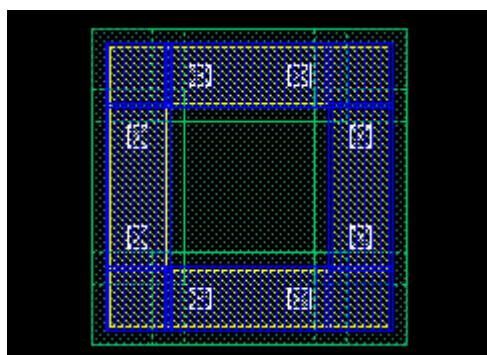
BOTTOM	<input checked="" type="checkbox"/>
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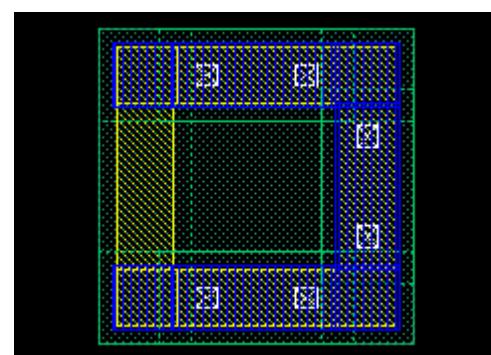
BOTTOM	<input type="checkbox"/>
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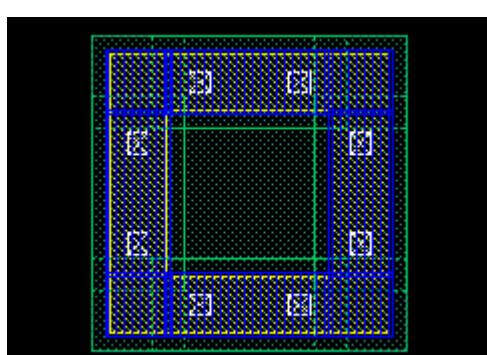
LEFT	<input checked="" type="checkbox"/>
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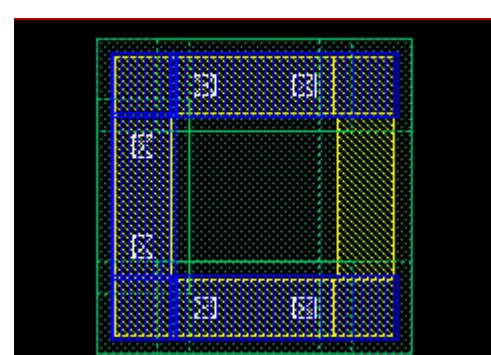
LEFT	<input type="checkbox"/>
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RIGHT	<input checked="" type="checkbox"/>
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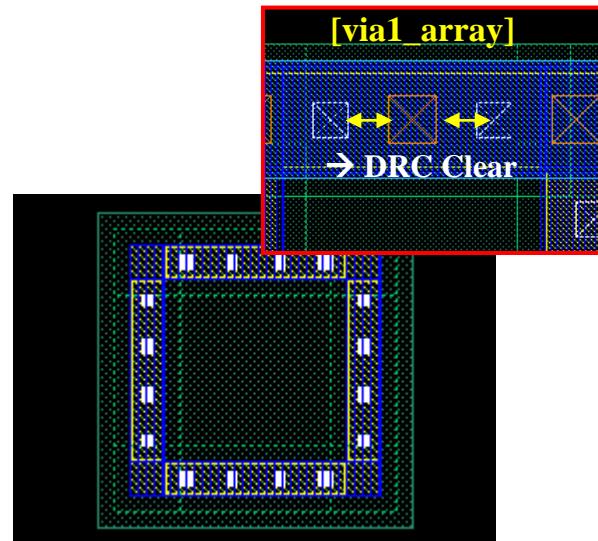


RIGHT	<input type="checkbox"/>
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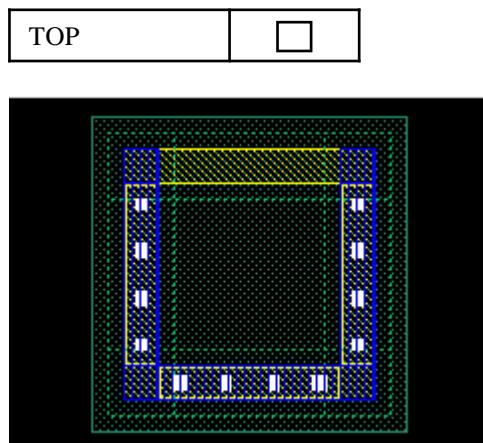
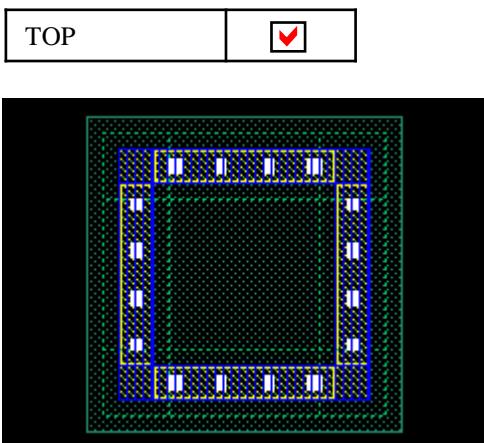
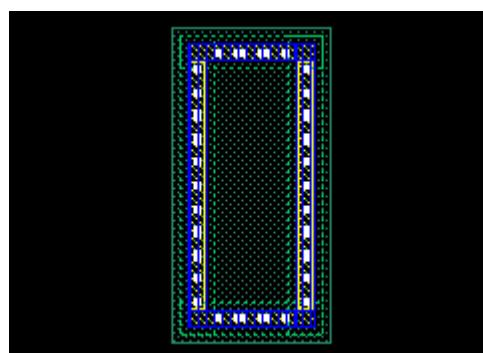
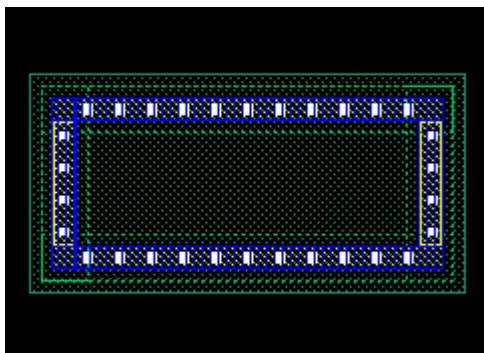
4.28 ntap_ring_pdiode

Parameter	Default	Change
x_size	19	<i>value</i>
y_size	19	<i>value</i>
TOP	<input checked="" type="checkbox"/>	<input type="checkbox"/>
BOTTOM	<input checked="" type="checkbox"/>	<input type="checkbox"/>
LEFT	<input checked="" type="checkbox"/>	<input type="checkbox"/>
RIGHT	<input checked="" type="checkbox"/>	<input type="checkbox"/>



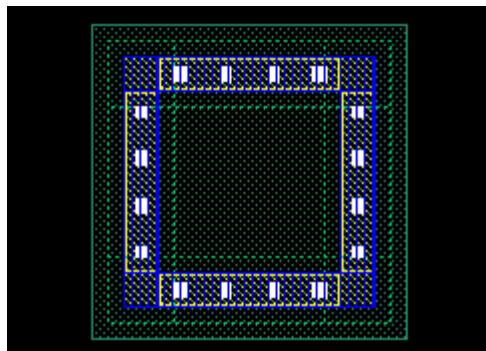
x_size	19	38
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y_size	19	38
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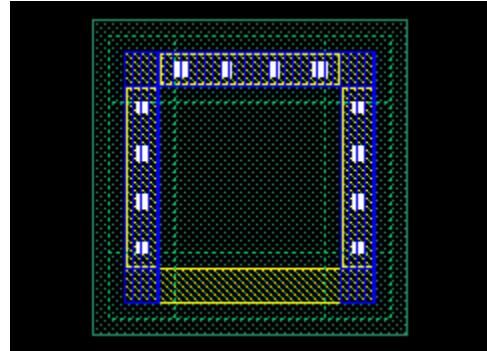


4.28 ntap_ring_pdiode

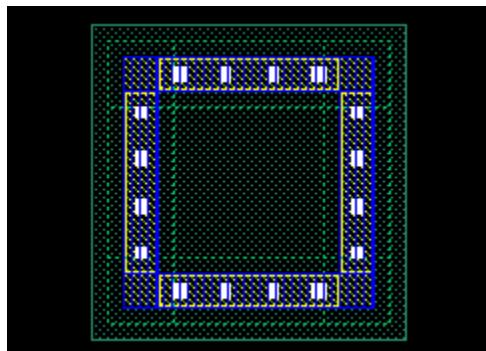
BOTTOM



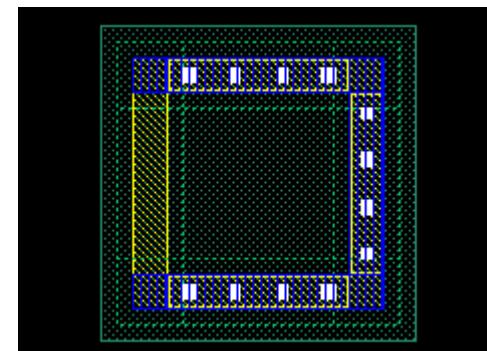
BOTTOM



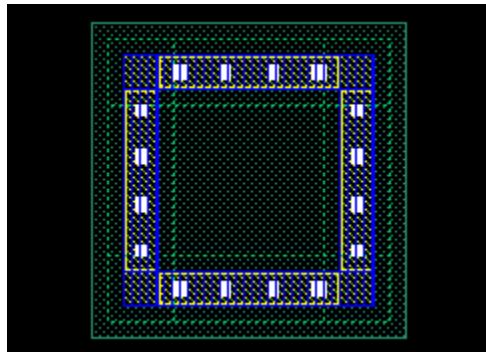
LEFT



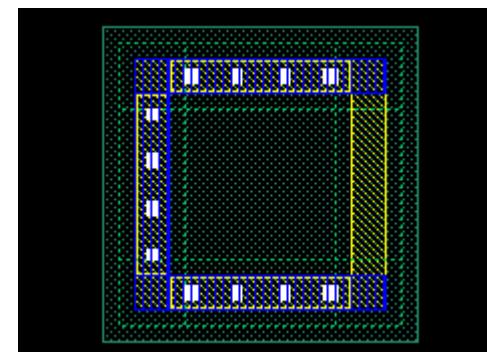
LEFT



RIGHT

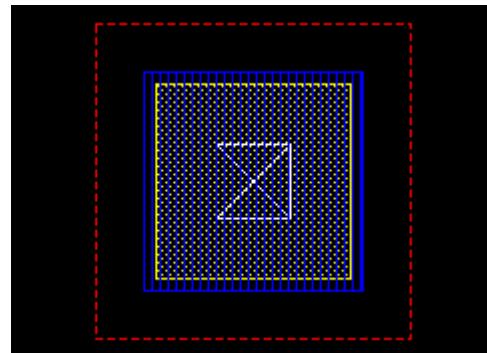


RIGHT

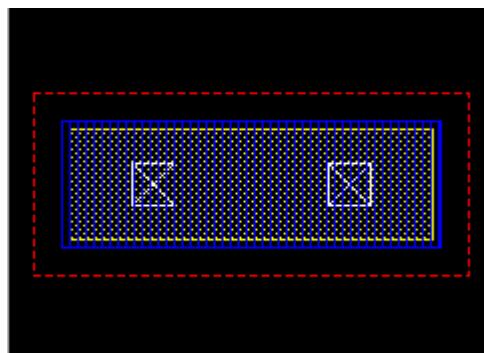


4.29 ptap

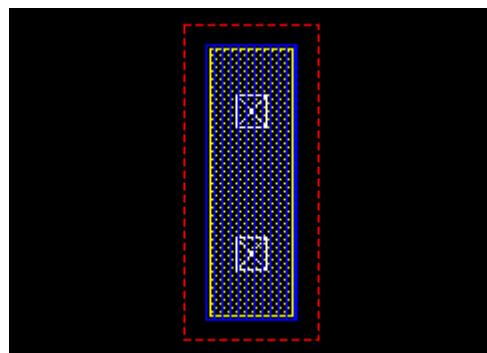
Parameter	Default	Change
x_size	1.8	<i>value</i>
y_size	1.8	<i>value</i>
PSD	<input checked="" type="checkbox"/>	<input type="checkbox"/>



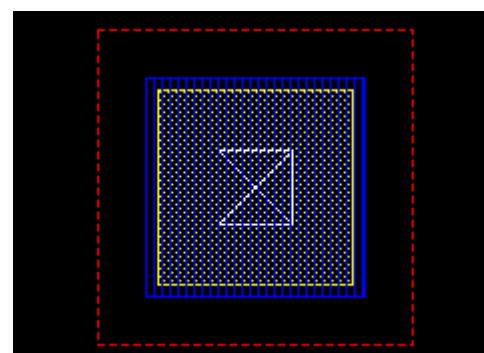
x_size	1.8	5.4
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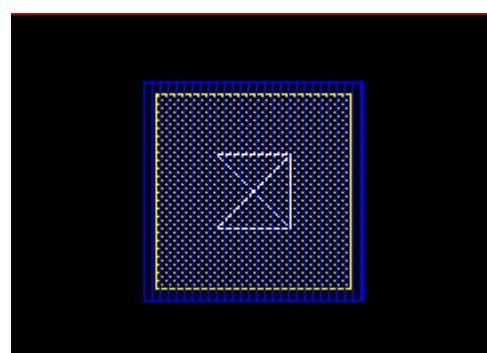
y_size	1.8	5.4
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PSD	<input checked="" type="checkbox"/>
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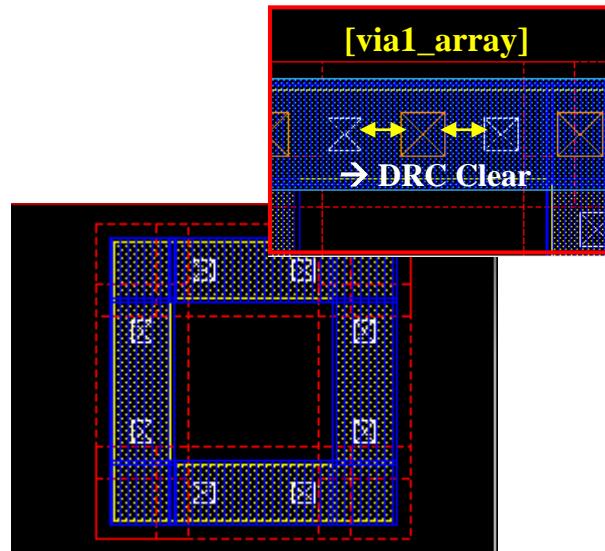


PSD	<input type="checkbox"/>
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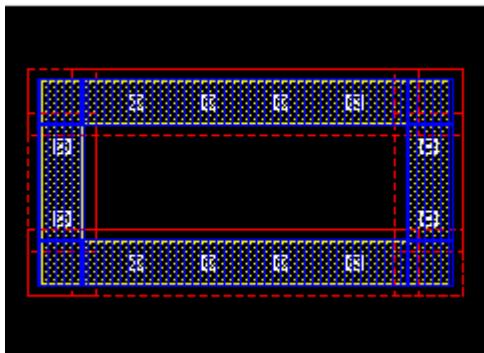


4.30 ptap_ring

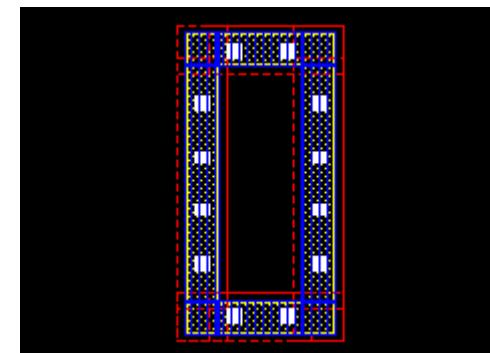
Parameter	Default	Change
x_size	8	value
y_size	8	value
TOP	<input checked="" type="checkbox"/>	<input type="checkbox"/>
BOTTOM	<input checked="" type="checkbox"/>	<input type="checkbox"/>
LEFT	<input checked="" type="checkbox"/>	<input type="checkbox"/>
RIGHT	<input checked="" type="checkbox"/>	<input type="checkbox"/>



x_size	8	16
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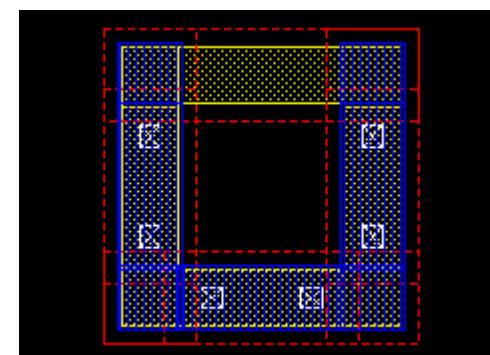
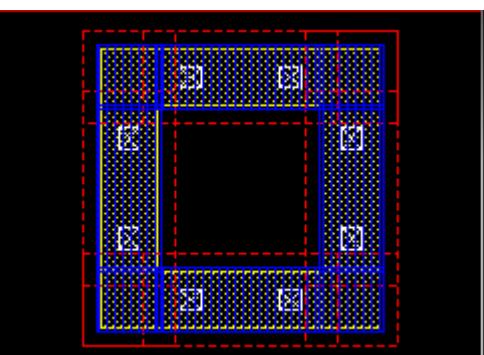


y_size	8	16
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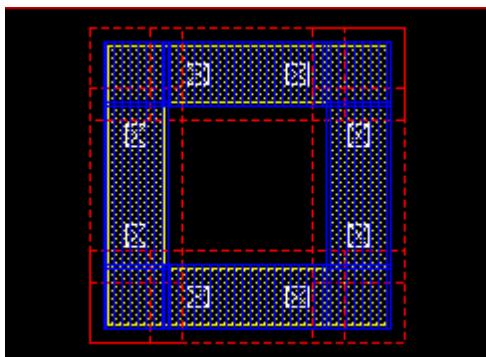
TOP	<input checked="" type="checkbox"/>
-----	-------------------------------------

TOP	<input type="checkbox"/>
-----	--------------------------

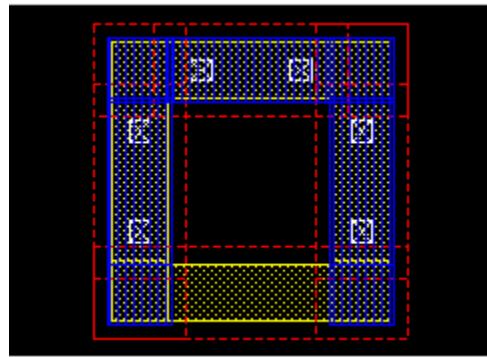


4.30 ptap_ring

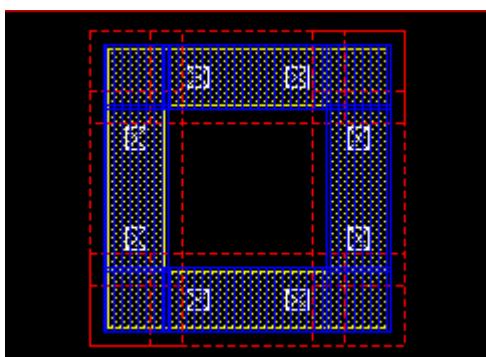
BOTTOM



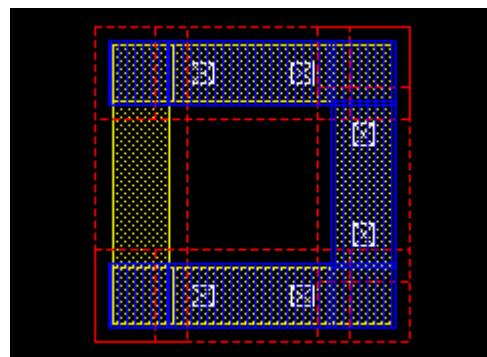
BOTTOM



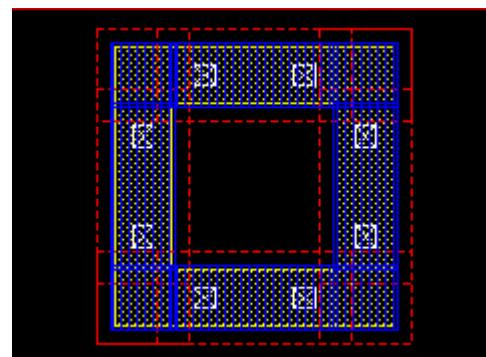
LEFT



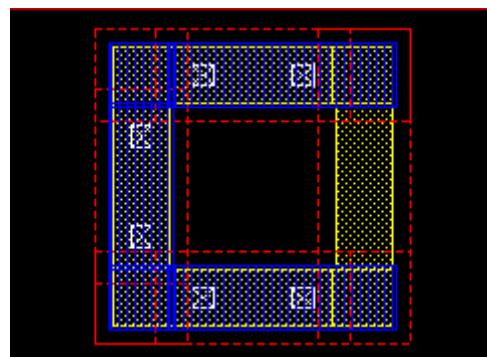
LEFT



RIGHT

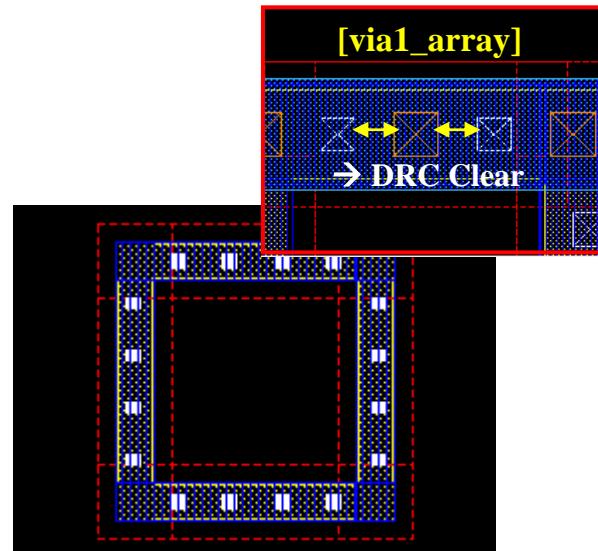


RIGHT



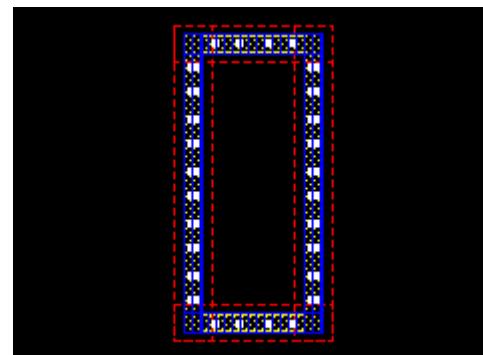
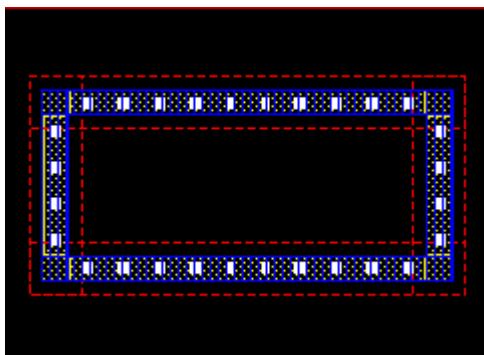
4.31 ptap_ring_ndiode

Parameter	Default	Change
x_size	17	<i>value</i>
y_size	17	<i>value</i>
TOP	<input checked="" type="checkbox"/>	<input type="checkbox"/>
BOTTOM	<input checked="" type="checkbox"/>	<input type="checkbox"/>
LEFT	<input checked="" type="checkbox"/>	<input type="checkbox"/>
RIGHT	<input checked="" type="checkbox"/>	<input type="checkbox"/>



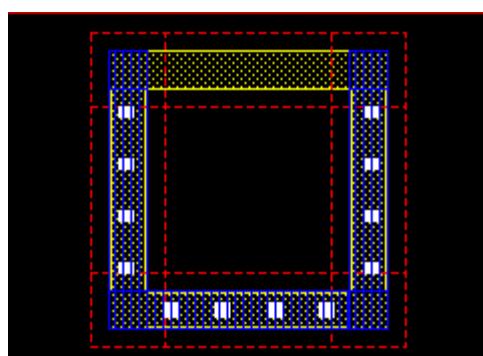
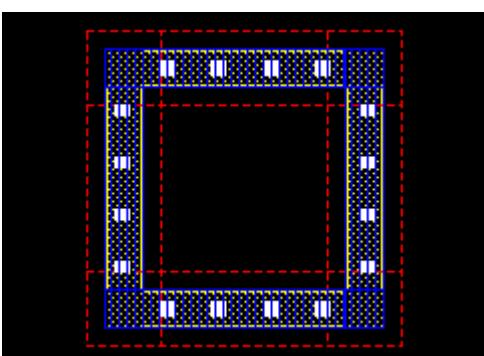
x_size	17	34
--------	----	----

y_size	17	34
--------	----	----



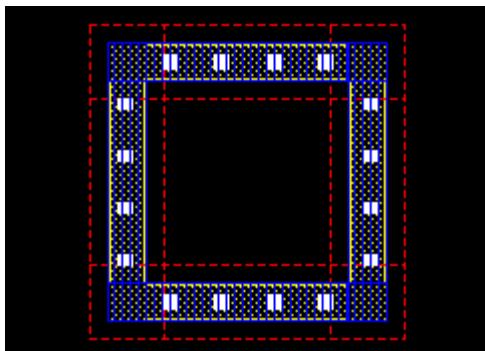
TOP	<input checked="" type="checkbox"/>
-----	-------------------------------------

TOP	<input type="checkbox"/>
-----	--------------------------

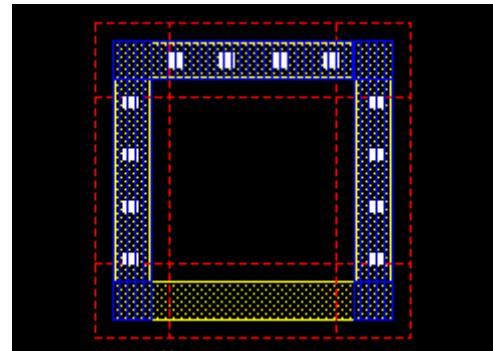


4.31 ptap_ring_ndiode

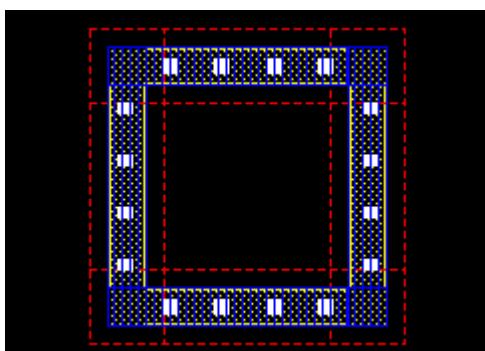
BOTTOM



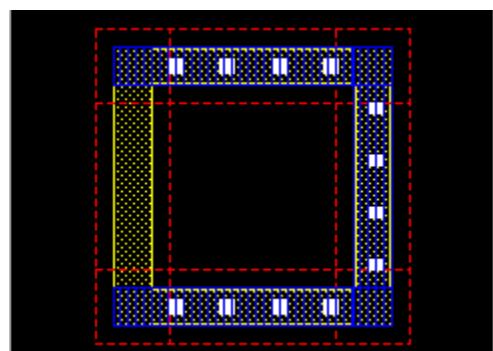
BOTTOM



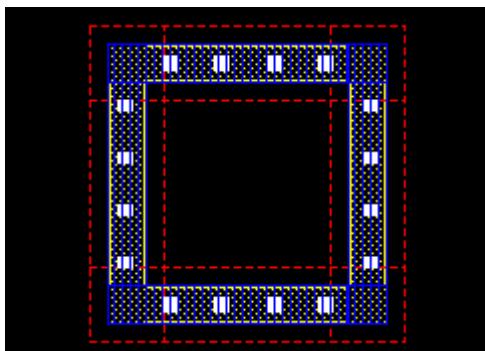
LEFT



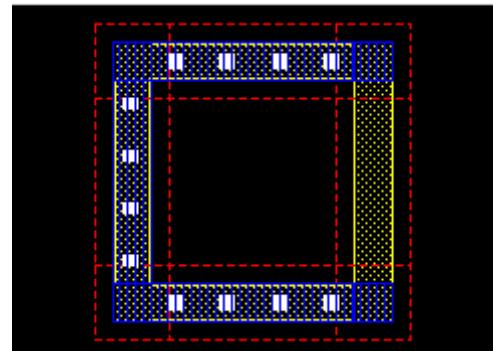
LEFT



RIGHT

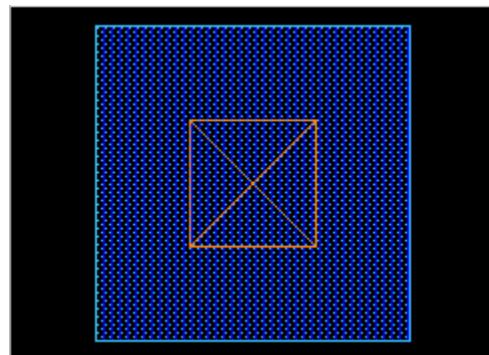


RIGHT

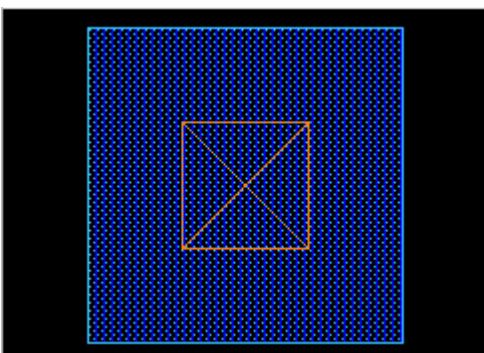


4.32 via1

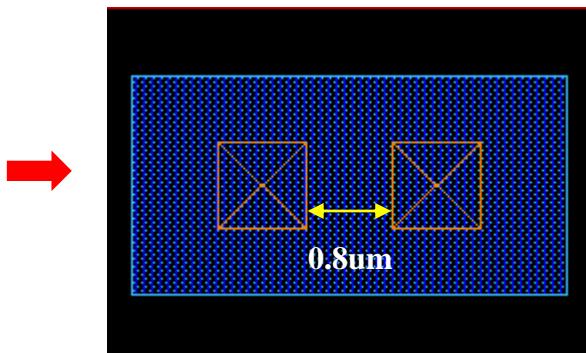
Parameter	Default	Change
x_size	2	<i>value</i>
y_size	2	<i>value</i>



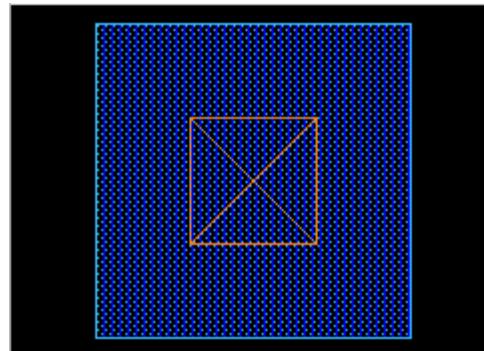
x_size	2
--------	---



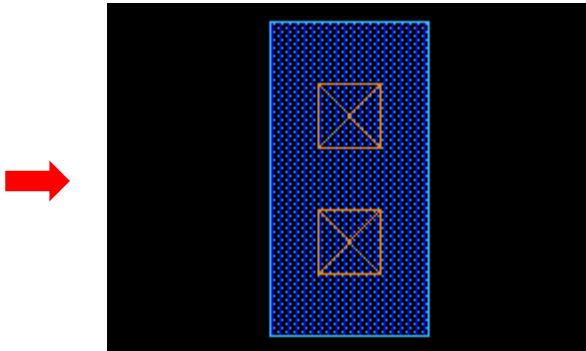
x_size	4
--------	---



y_size	2
--------	---

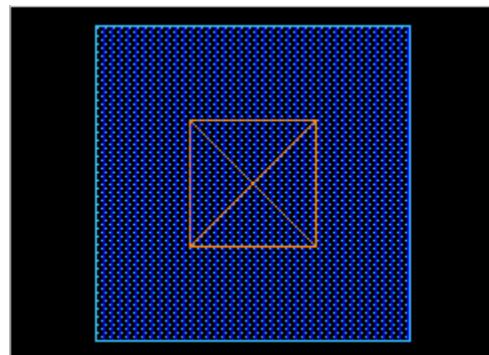


y_size	4
--------	---

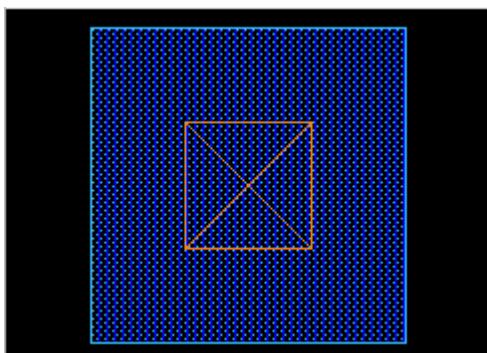


4.33 via1_array

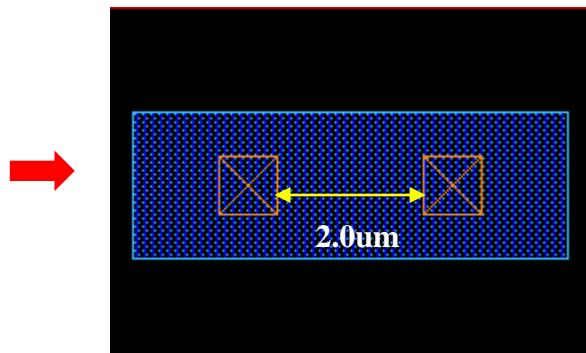
Parameter	Default	Change
x_size	2	<i>value</i>
y_size	2	<i>value</i>



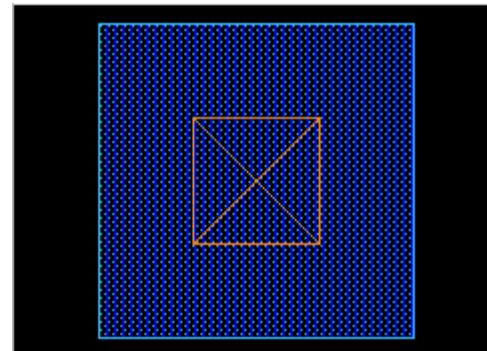
x_size	2
--------	---



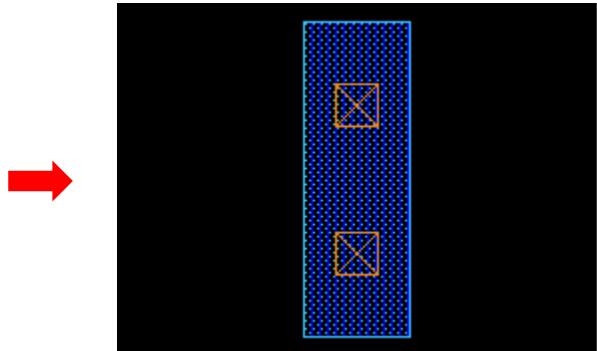
x_size	6
--------	---



y_size	2
--------	---

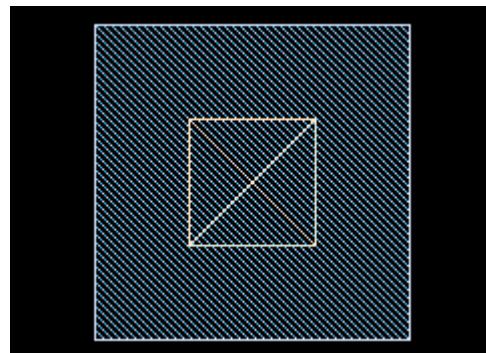


y_size	6
--------	---

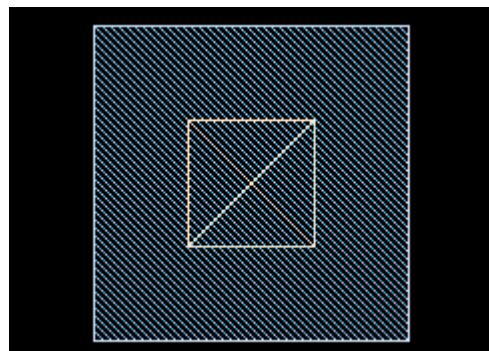


4.34 via2

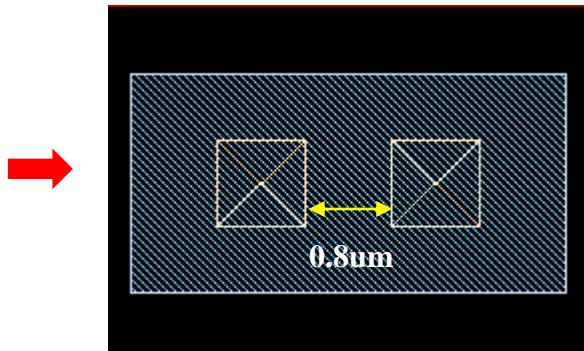
Parameter	Default	Change
x_size	2	<i>value</i>
y_size	2	<i>value</i>



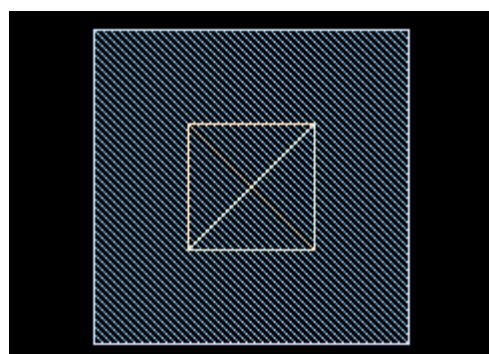
x_size	2
--------	---



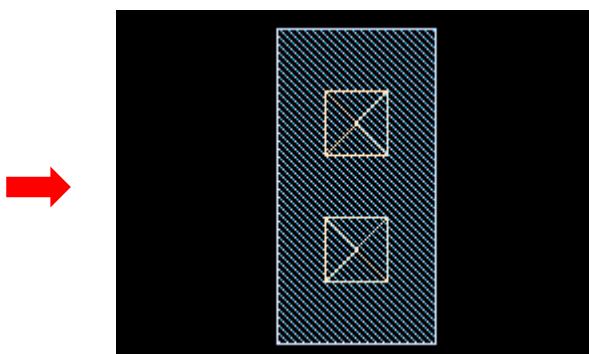
x_size	4
--------	---



y_size	2
--------	---

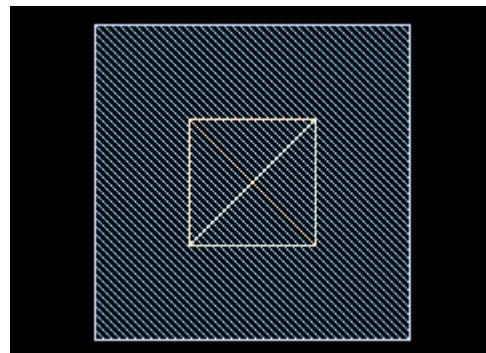


y_size	4
--------	---

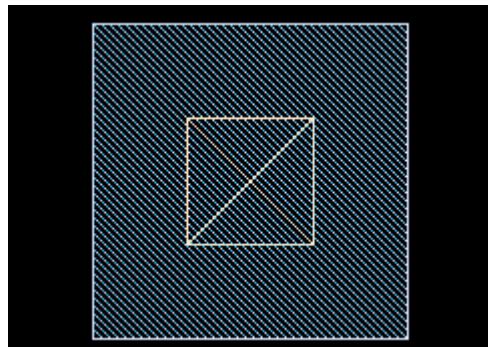


4.35 via2_array

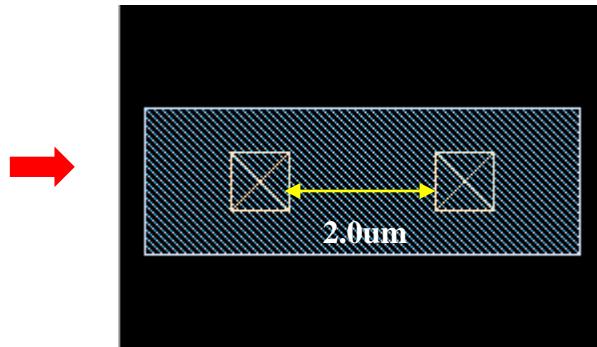
Parameter	Default	Change
x_size	2	<i>value</i>
y_size	2	<i>value</i>



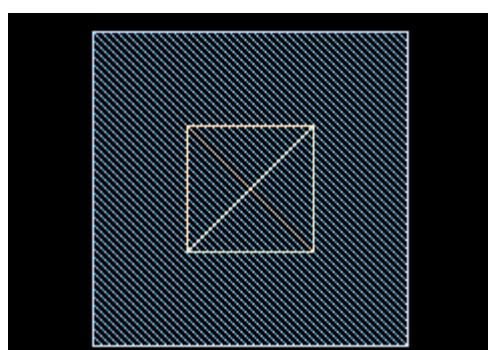
x_size	2
--------	---



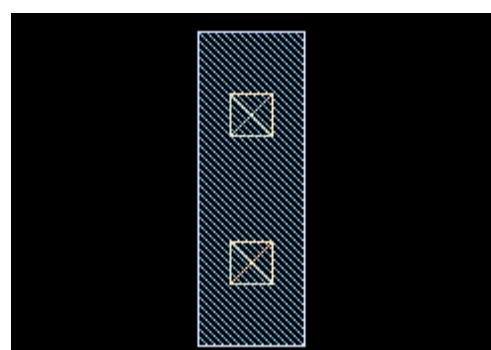
x_size	6
--------	---



y_size	2
--------	---



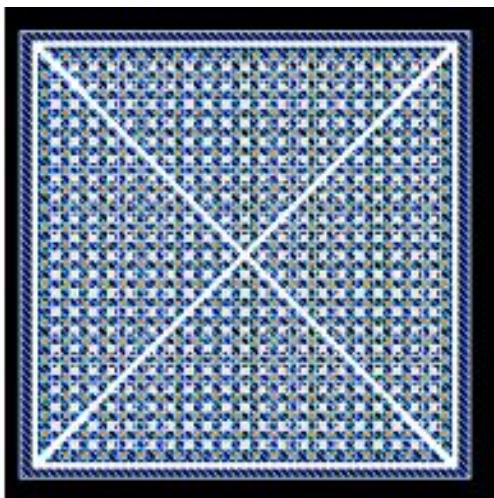
y_size	6
--------	---



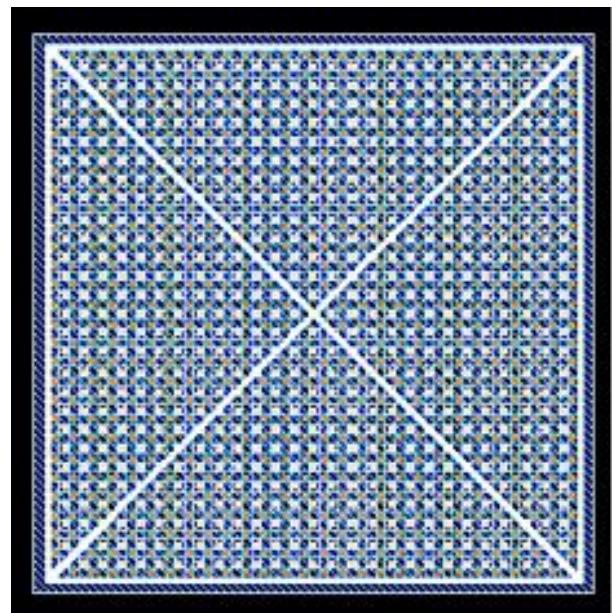
4.36 pad80 / pad100

Parameter	Default	Change
-	-	-

pad80



pad100



PAD Fixed Size (80um * 80um)

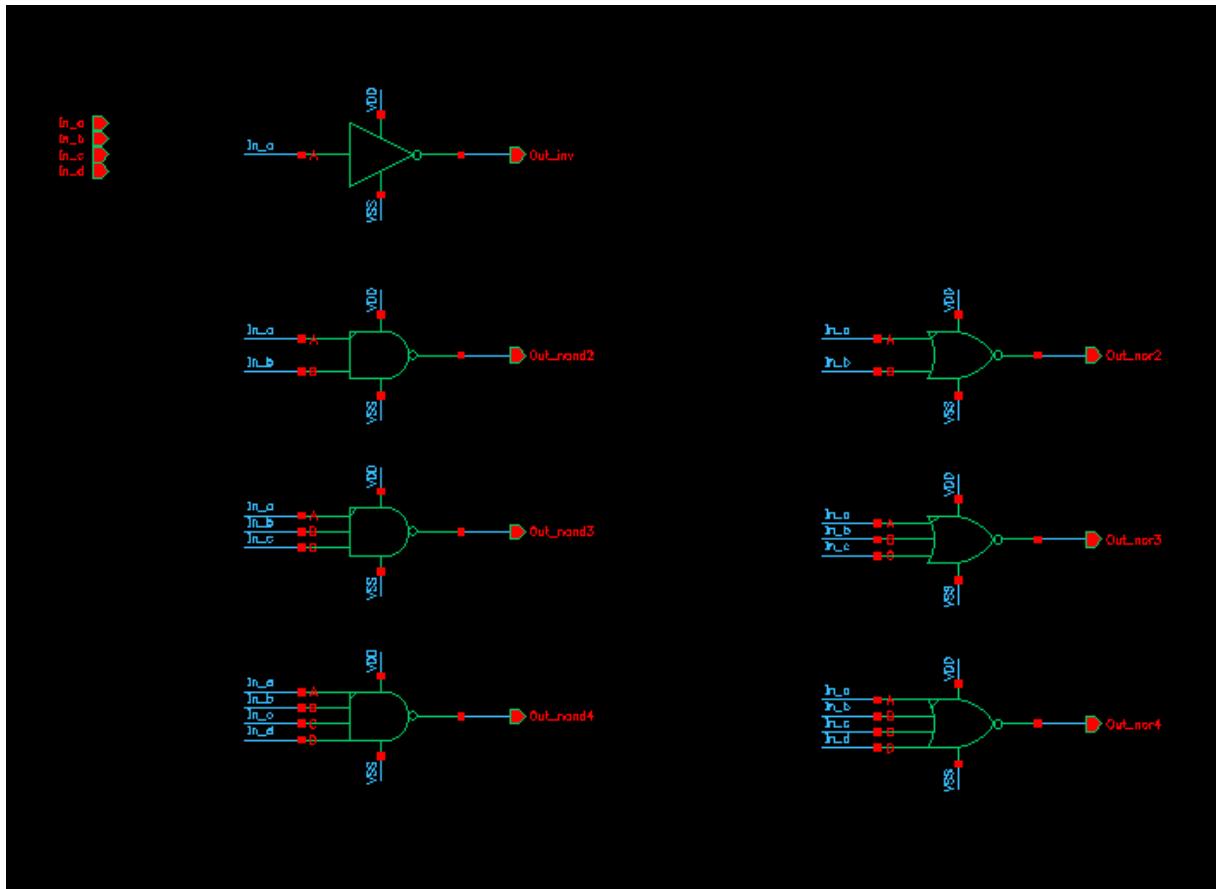
→ doesn't provide parameter modification

PAD Fixed Size (100um * 100um)

→ doesn't provide parameter modification

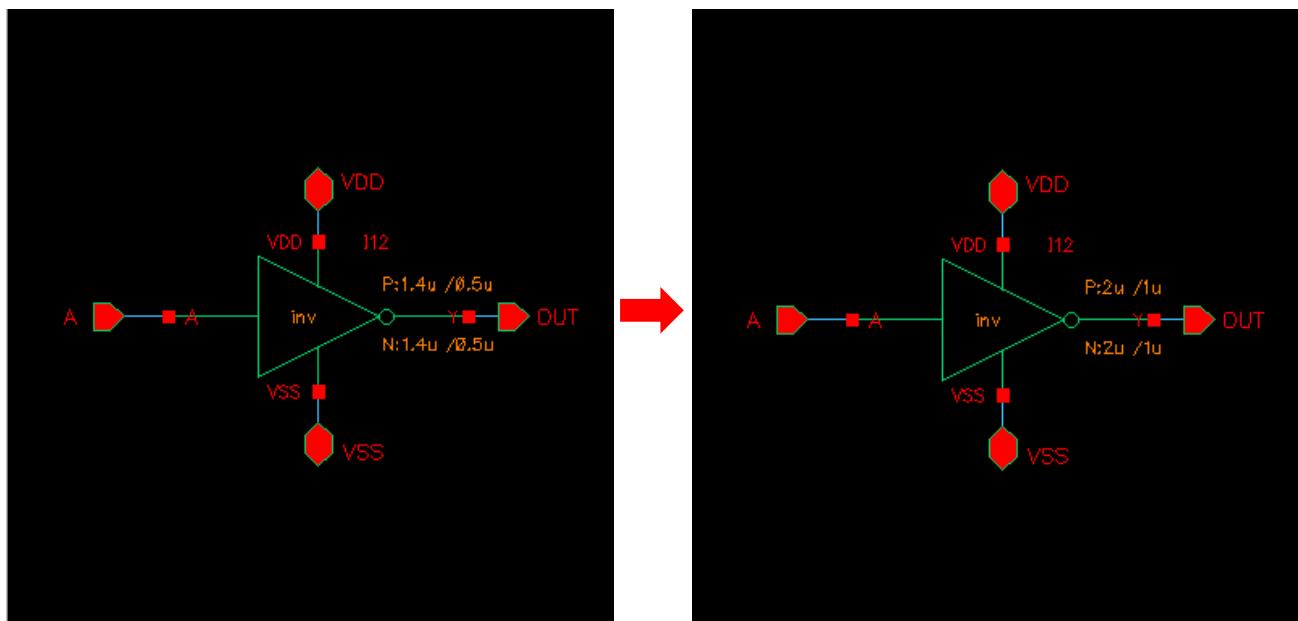
5. Standard Schematic Library

5.1 .SAMPLE



5.2 inv

Parameter							
pl		pw		nl		nw	
0.5u	1u	1.4u	2u	0.5u	1u	1.4u	2u



<Schematic parameter>

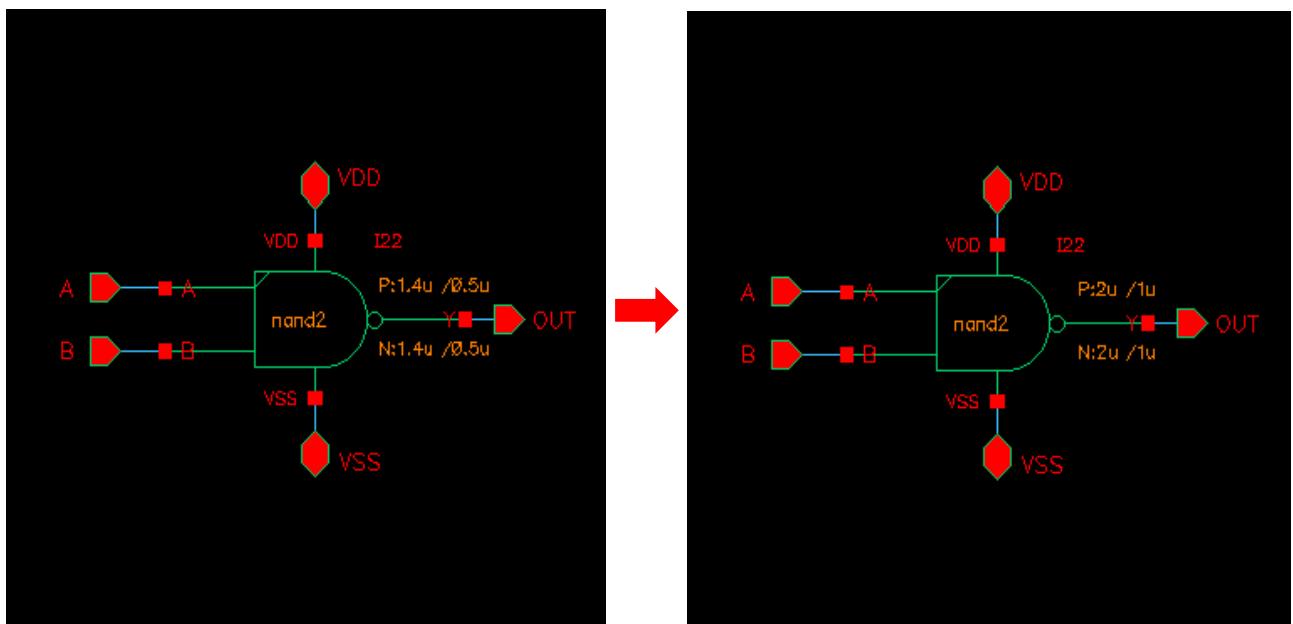
```
*****
* Library Name: ETRI_lay
* Cell Name: inv_schematic
* View Name: schematic
*****
.SUBCKT inv_schematic A OUT VDD VSS
*.PININFO A:I OUT:0 VDD:B VSS:B
XI12 A VDD VSS OUT / inv pl=0.5u pw=1.4u nl=0.5u nw=1.4u
.ENDS
```

```
*****
* Library Name: ETRI_lay
* Cell Name: inv_schematic
* View Name: schematic
*****
.SUBCKT inv_schematic A OUT VDD VSS
*.PININFO A:I OUT:0 VDD:B VSS:B
XI12 A VDD VSS OUT / inv pl=1u pw=2u nl=1u nw=2u
.ENDS
```

<cdl output>

5.3 nand2

Parameter							
pl		pw		nl		nw	
0.5u	1u	1.4u	2u	0.5u	1u	1.4u	2u



<Schematic parameter>

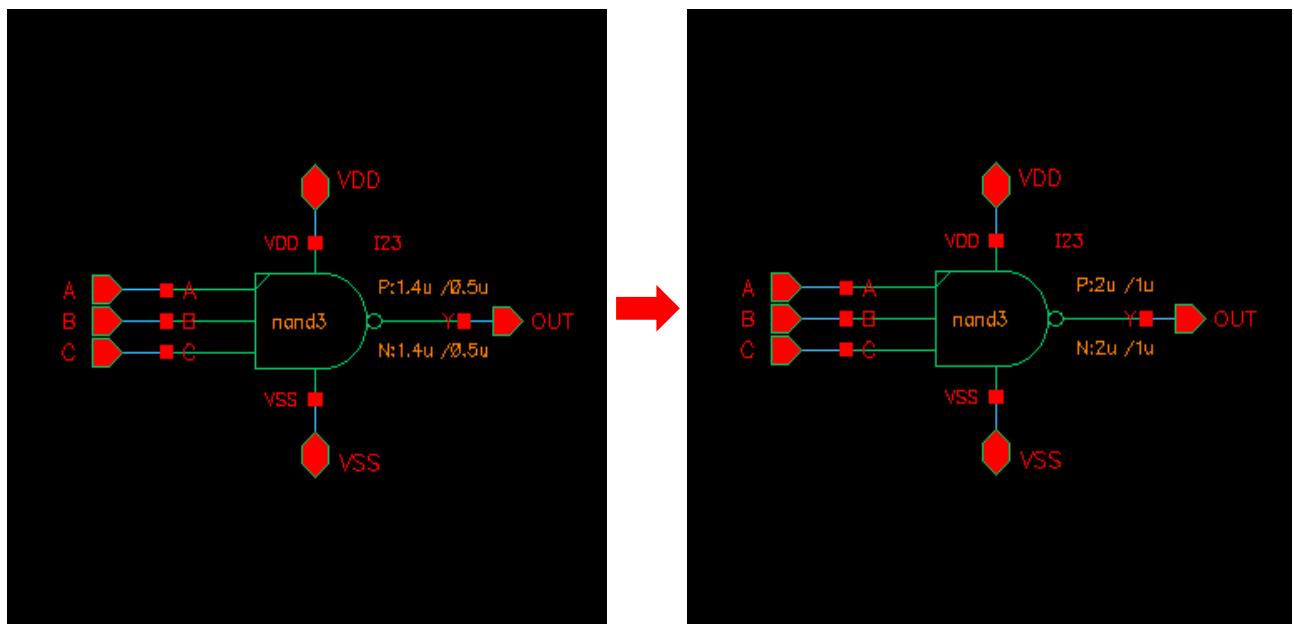
```
*****
* Library Name: ETRI_lay
* Cell Name: nand2_schematic
* View Name: schematic
*****
.SUBCKT nand2 schematic A B OUT VDD VSS
*.PININFO A:I B:I OUT:O VDD:B VSS:B
XI22 A B VDD VSS OUT / nand2 nl=0.5u nw=1.4u pl=0.5u pw=1.4u
.ENDS
```

```
*****
* Library Name: ETRI_lay
* Cell Name: nand2_schematic
* View Name: schematic
*****
.SUBCKT nand2 schematic A B OUT VDD VSS
*.PININFO A:I B:I OUT:O VDD:B VSS:B
XI22 A B VDD VSS OUT / nand2 nl=1u nw=2u pl=1u pw=2u
.ENDS
```

<cdl output>

5.4 nand3

Parameter							
pl		pw		nl		nw	
0.5u	1u	1.4u	2u	0.5u	1u	1.4u	2u



<Schematic parameter>

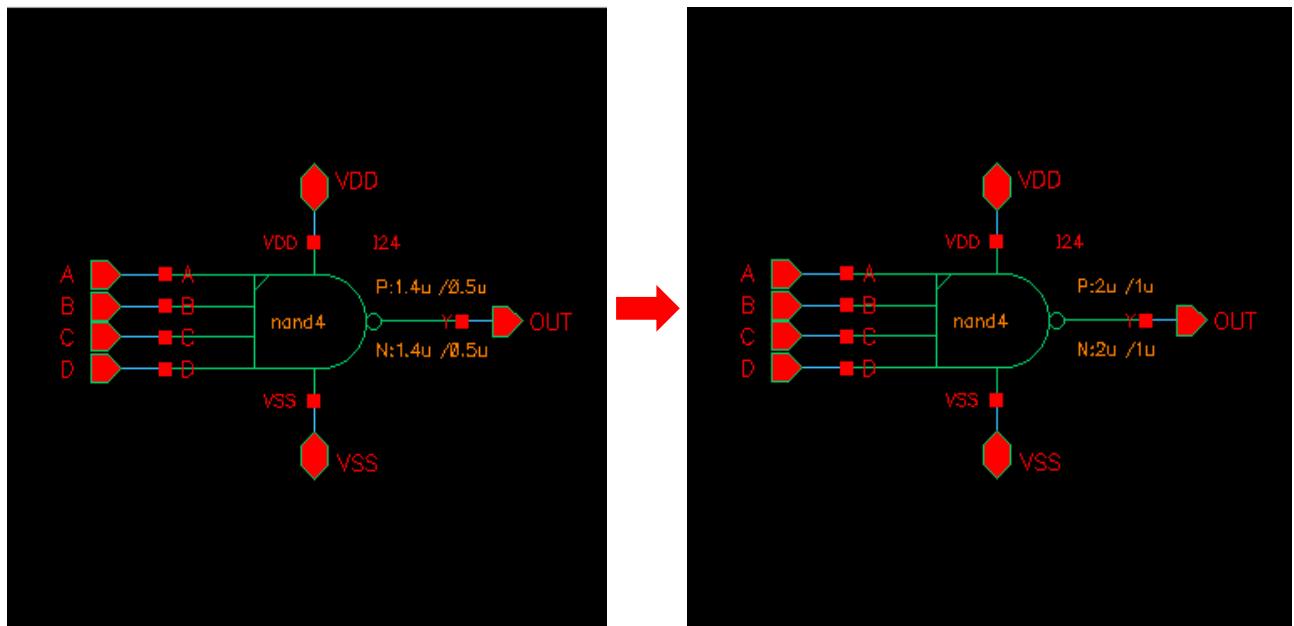
```
*****
* Library Name: ETRI_lay
* Cell Name:    nand3_schematic
* View Name:    schematic
*****
.SUBCKT nand3_schematic A B C OUT VDD VSS
*.PININFO A:I B:I C:I OUT:O VDD:B VSS:B
XI23 A B C VDD VSS OUT / nand3 pl=0.5u pw=1.4u nl=0.5u nw=1.4u
.ENDS
```

```
*****
* Library Name: ETRI_lay
* Cell Name:    nand3_schematic
* View Name:    schematic
*****
.SUBCKT nand3_schematic A B C OUT VDD VSS
*.PININFO A:I B:I C:I OUT:O VDD:B VSS:B
XI23 A B C VDD VSS OUT / nand3 pl=1u pw=2u nl=1u nw=2u
.ENDS
```

<cdl output>

5.5 nand4

Parameter							
pl		pw		nl		nw	
0.5u	1u	1.4u	2u	0.5u	1u	1.4u	2u



<Schematic parameter>

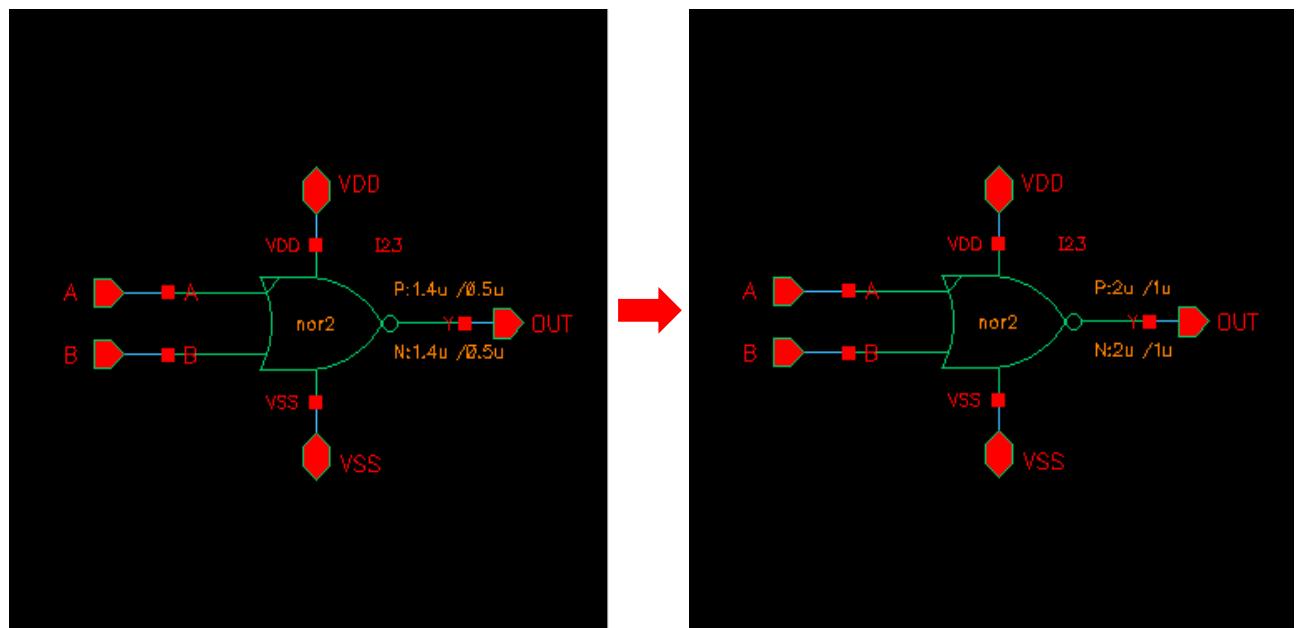
```
*****
* Library Name: ETRI_lay
* Cell Name: nand4_schematic
* View Name: schematic
*****
.SUBCKT nand4 schematic A B C D OUT VDD VSS
*.PININFO A:I B:I C:I D:I OUT:O VDD:B VSS:B
XI25 A B C D VDD VSS OUT / nand4 pl=0.5u pw=1.4u nl=0.5u nw=1.4u
.ENDS
```

```
*****
* Library Name: ETRI_lay
* Cell Name: nand4_schematic
* View Name: schematic
*****
.SUBCKT nand4 schematic A B C D OUT VDD VSS
*.PININFO A:I B:I C:I D:I OUT:O VDD:B VSS:B
XI24 A B C D VDD VSS OUT / nand4 pl=1u pw=2u nl=1u nw=2u
.ENDS
```

<cdl output>

5.6 nor2

Parameter							
pl		pw		nl		nw	
0.5u	1u	1.4u	2u	0.5u	1u	1.4u	2u



<Schematic parameter>

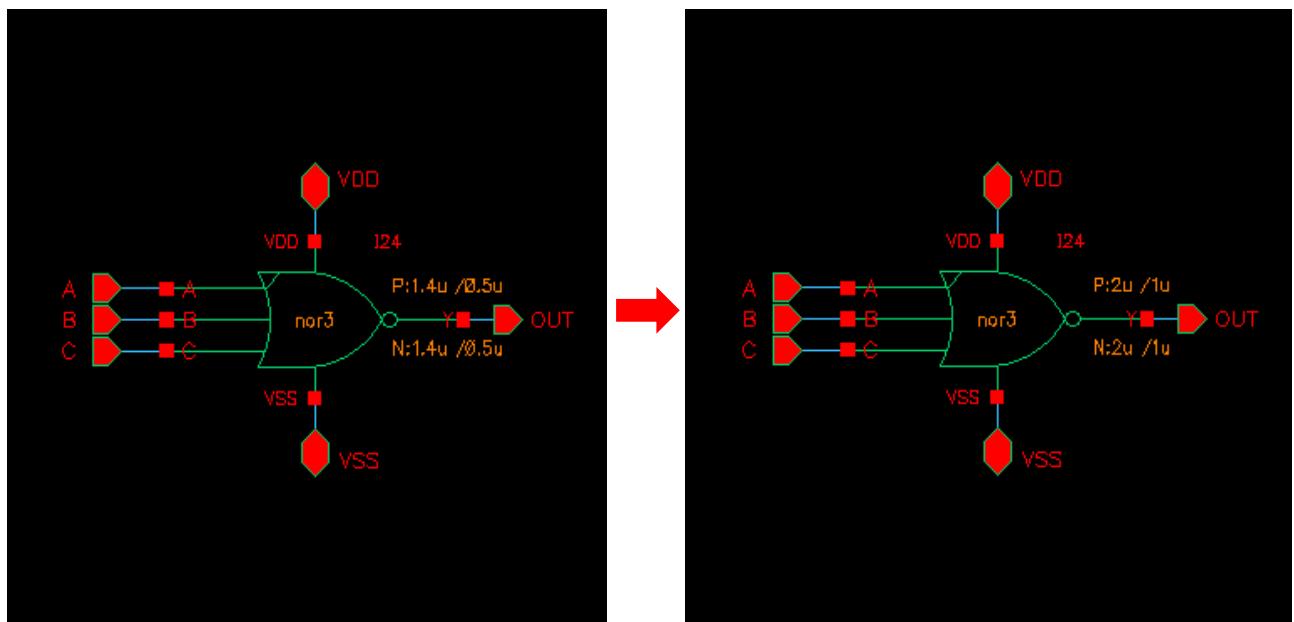
```
*****
* Library Name: ETRI_lay
* Cell Name: nor2_schematic
* View Name: schematic
*****
.SUBCKT nor2_schematic A B OUT VDD VSS
*.PININFO A:I B:I OUT:O VDD:B VSS:B
XI23 A B VDD VSS OUT / nor2 pl=0.5u pw=1.4u nl=0.5u nw=1.4u
.ENDS
```

```
*****
* Library Name: ETRI_lay
* Cell Name: nor2_schematic
* View Name: schematic
*****
.SUBCKT nor2_schematic A B OUT VDD VSS
*.PININFO A:I B:I OUT:O VDD:B VSS:B
XI23 A B VDD VSS OUT / nor2 pl=1u pw=2u nl=1u nw=2u
.ENDS
```

<cdl output>

5.7 nor3

Parameter							
pl		pw		nl		nw	
0.5u	1u	1.4u	2u	0.5u	1u	1.4u	2u



<Schematic parameter>

```
*****
* Library Name: ETRI_lay
* Cell Name: nor3_schematic
* View Name: schematic
*****
```

```
.SUBCKT nor3_schematic A B C OUT VDD VSS
*.PININFO A:I B:I C:I OUT:O VDD:B VSS:B
XI24 A B C VDD VSS OUT / nor3 pl=0.5u pw=1.4u nl=0.5u nw=1.4u
.ENDS
```

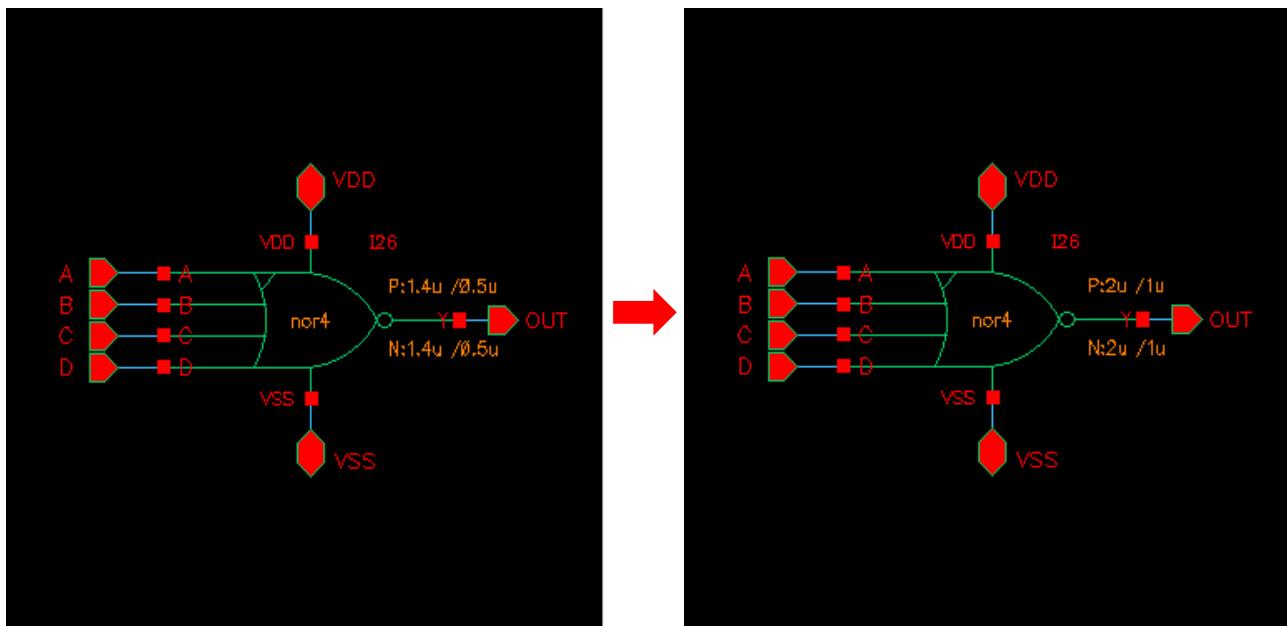
```
*****
* Library Name: ETRI_lay
* Cell Name: nor3_schematic
* View Name: schematic
*****
```

```
.SUBCKT nor3_schematic A B C OUT VDD VSS
*.PININFO A:I B:I C:I OUT:O VDD:B VSS:B
XI24 A B C VDD VSS OUT / nor3 pl=1u pw=2u nl=1u nw=2u
.ENDS
```

<cdl output>

5.8 nor4

Parameter							
pl		pw		nl		nw	
0.5u	1u	1.4u	2u	0.5u	1u	1.4u	2u



<Schematic parameter>

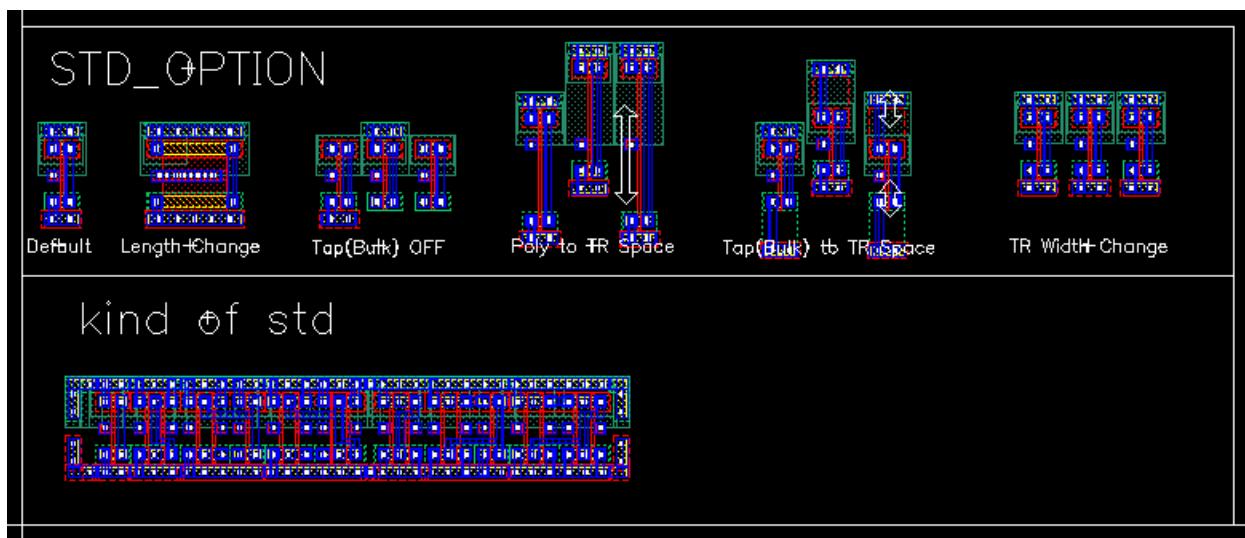
```
*****
* Library Name: ETRI_lay
* Cell Name:    nor4_schematic
* View Name:   schematic
*****
.SUBCKT nor4_schematic A B C D OUT VDD VSS
*.PININFO A:I B:I C:I D:I OUT:O VDD:B VSS:B
XI26 A B C D VDD VSS OUT / nor4 pl=0.5u pw=1.4u nl=0.5u nw=1.4u
.ENDS
```

```
*****
* Library Name: ETRI_lay
* Cell Name:    nor4_schematic
* View Name:   schematic
*****
.SUBCKT nor4_schematic A B C D OUT VDD VSS
*.PININFO A:I B:I C:I D:I OUT:O VDD:B VSS:B
XI26 A B C D VDD VSS OUT / nor4 pl=1u pw=2u nl=1u nw=2u
.ENDS
```

<cdl output>

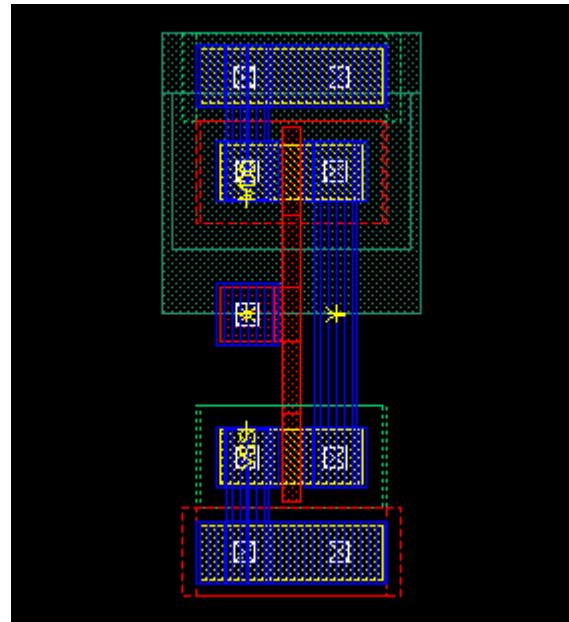
6. Standard Layout Library

6.1 .SAMPLE

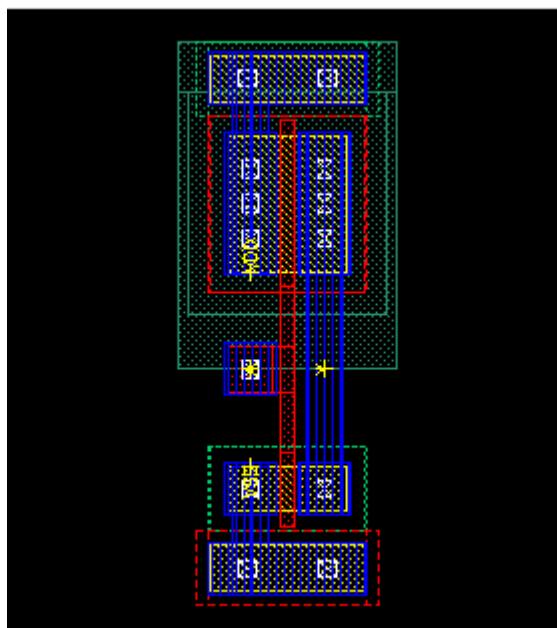


6.2 inv

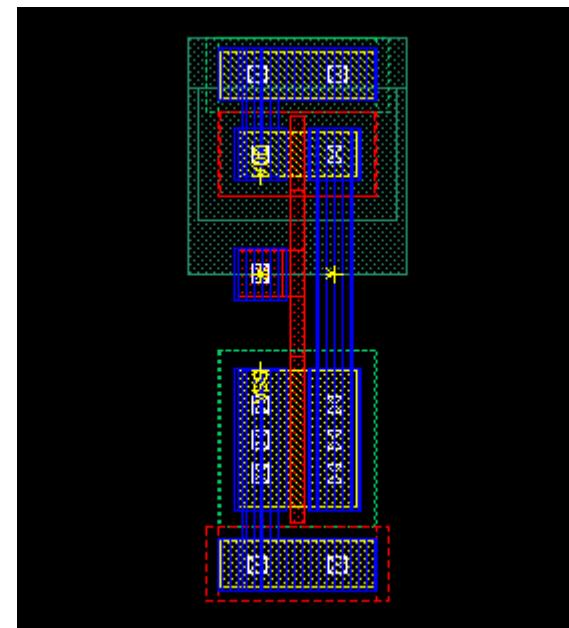
Parameter	Default	Change
P_WIDTH	1.6	<i>value</i>
N_WIDTH	1.6	<i>value</i>
LENGTH	0.5	<i>value</i>
POLY_TO_PTR_SPACE	2.6	<i>value</i>
POLY_TO_NTR_SPACE	2.6	<i>value</i>
PTAP_TO_TR_SPACE	0	<i>value</i>
NTAP_TO_TR_SPACE	0	<i>value</i>
PTAP	<input checked="" type="checkbox"/>	<input type="checkbox"/>
NTAP	<input checked="" type="checkbox"/>	<input type="checkbox"/>
POLY1CONT	<input checked="" type="checkbox"/>	<input type="checkbox"/>



P_WIDTH	1.6	4.8
---------	-----	-----

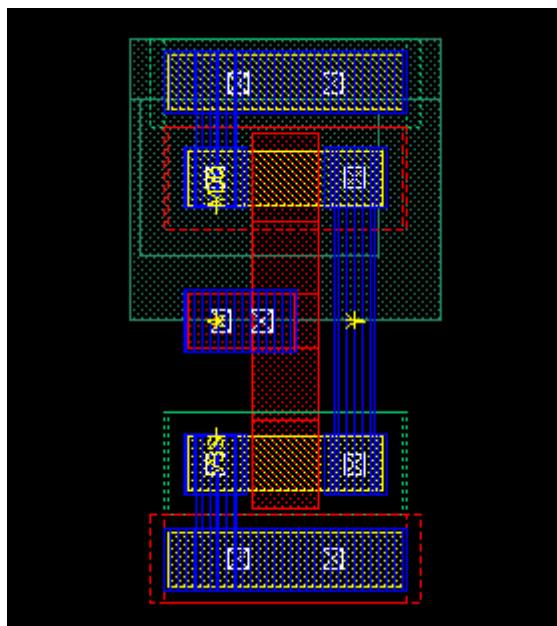


N_WIDTH	1.6	4.8
---------	-----	-----

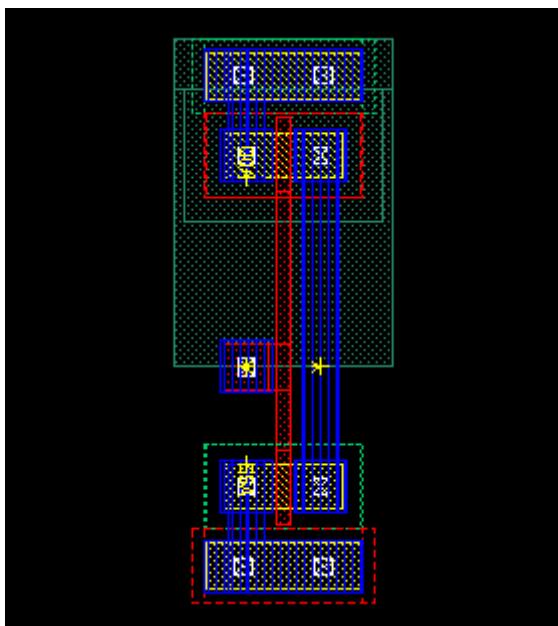


6.2 inv

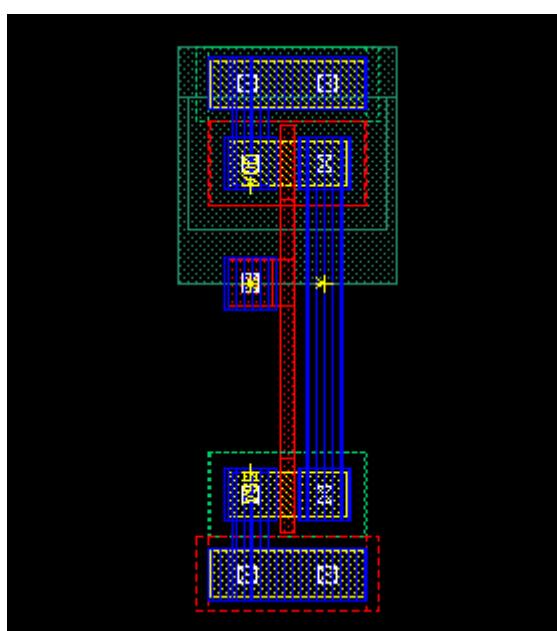
LENGTH	0.5	2
--------	-----	---



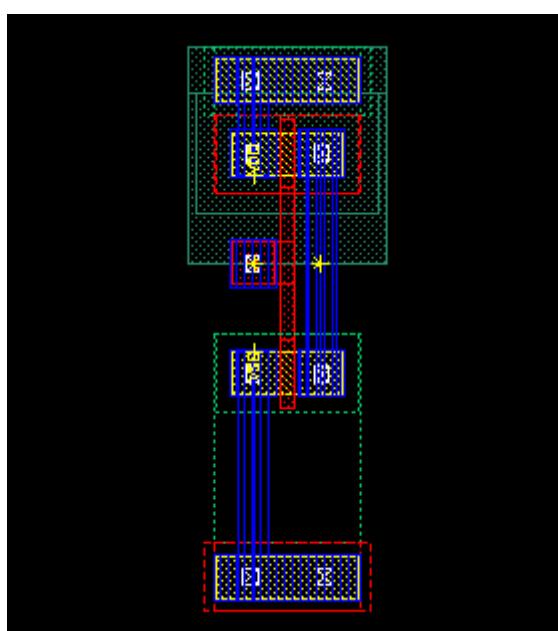
POLY_TO_PTR_SPACE	2.6	5.2
-------------------	-----	-----



POLY_TO_NTR_SPACE	2.6	5.2
-------------------	-----	-----

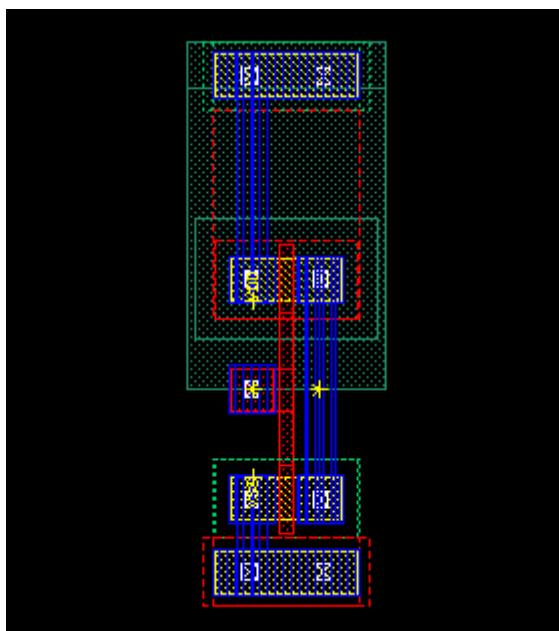


PTAP_TO_TR_SPACE	0	5.0
------------------	---	-----

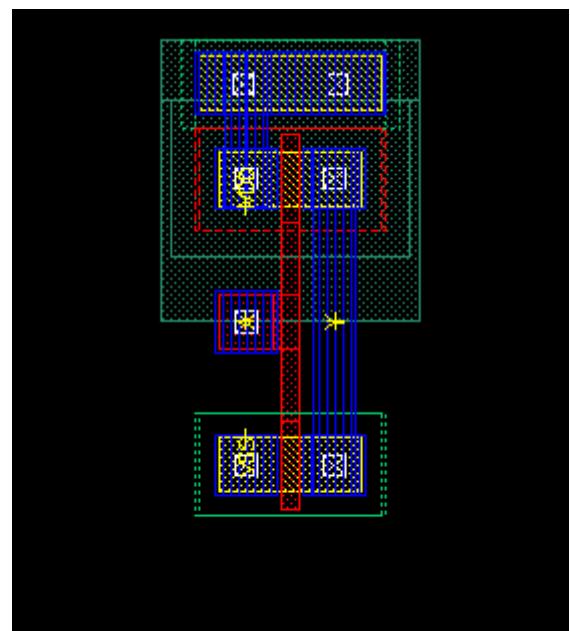


6.2 inv

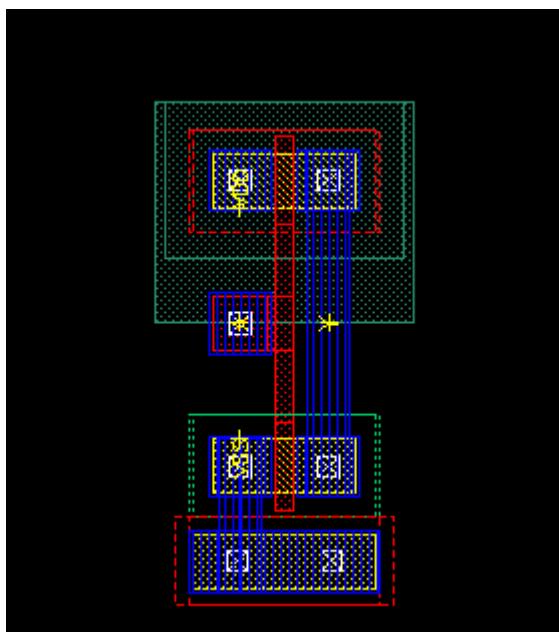
NTAP_TO_TR_SPACE	0	5
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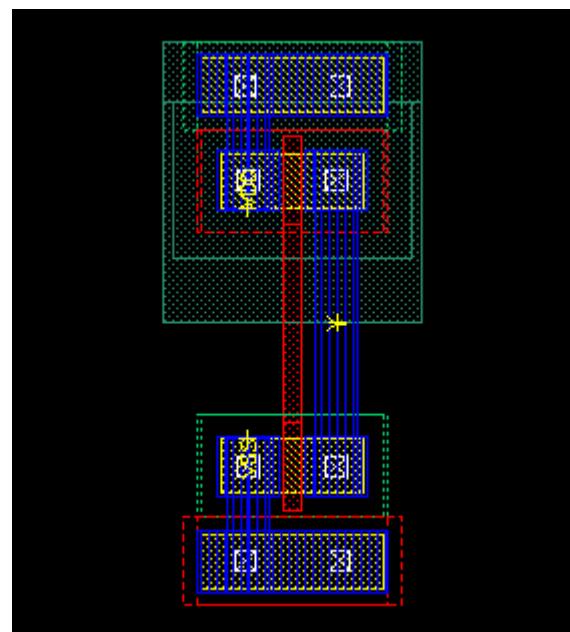
PTAP	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
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NTAP	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
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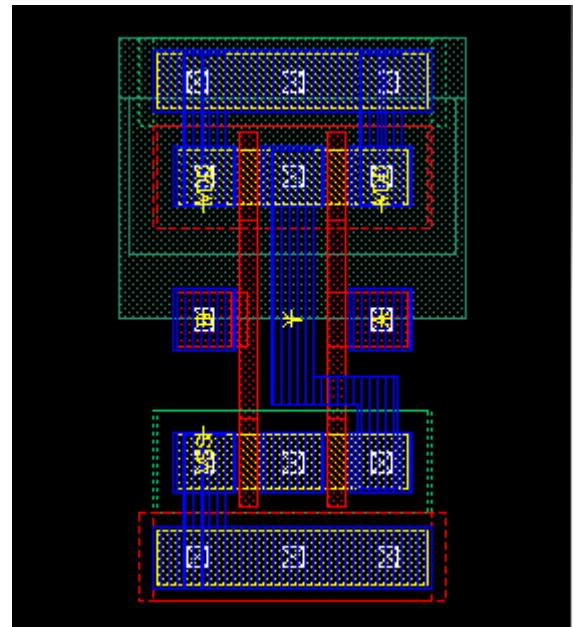


POLY1CONT	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
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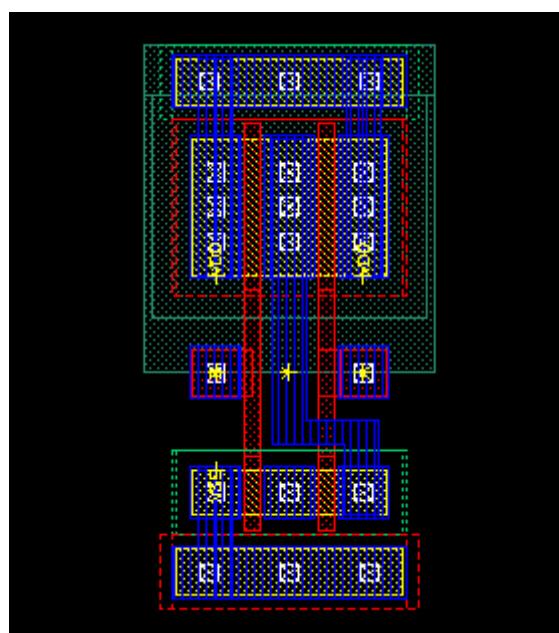


6.3 nand2

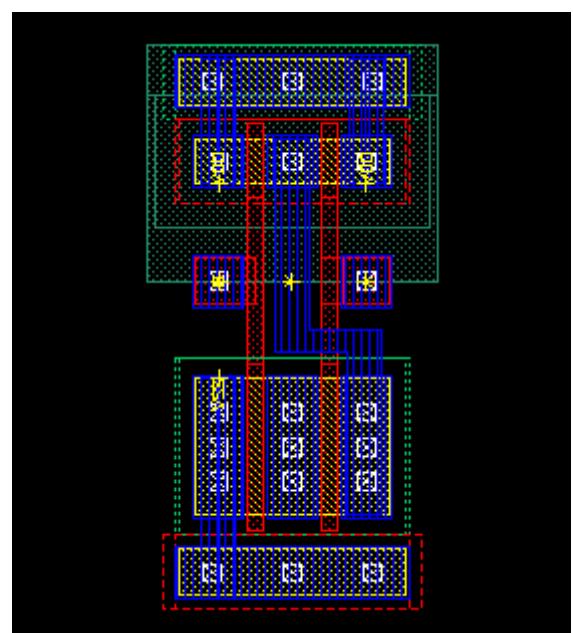
Parameter	Default	Change
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N_WIDTH	1.6	<i>value</i>
LENGTH	0.5	<i>value</i>
POLY_TO_PTR_SPACE	2.6	<i>value</i>
POLY_TO_NTR_SPACE	2.6	<i>value</i>
PTAP_TO_TR_SPACE	0	<i>value</i>
NTAP_TO_TR_SPACE	0	<i>value</i>
PTAP	<input checked="" type="checkbox"/>	<input type="checkbox"/>
NTAP	<input checked="" type="checkbox"/>	<input type="checkbox"/>
POLY1CONTA	<input checked="" type="checkbox"/>	<input type="checkbox"/>
POLY1CONTB	<input checked="" type="checkbox"/>	<input type="checkbox"/>



P_WIDTH	1.6	4.8
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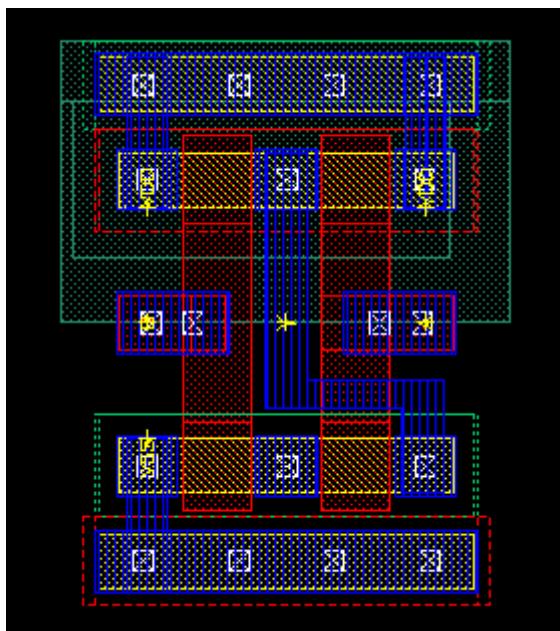


N_WIDTH	1.6	4.8
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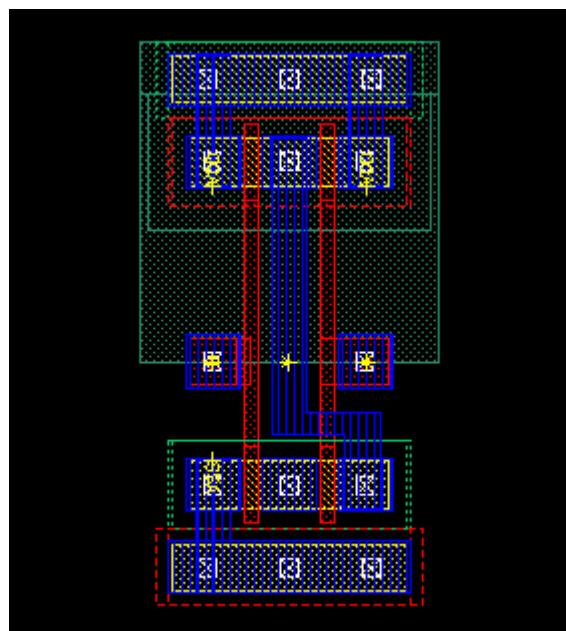


6.3 nand2

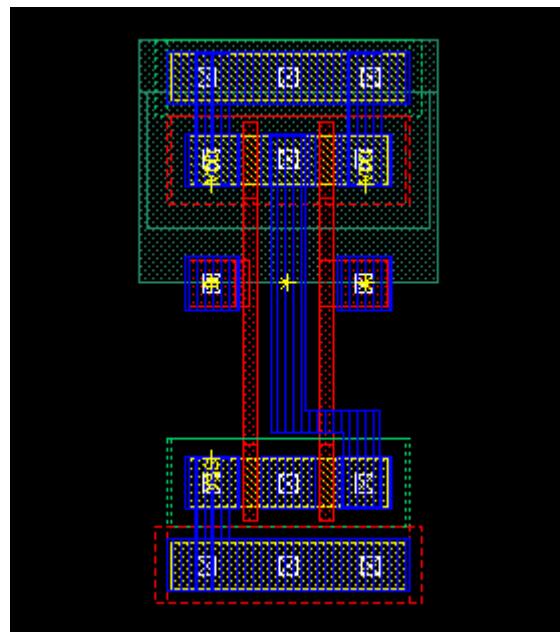
LENGTH	0.5	2
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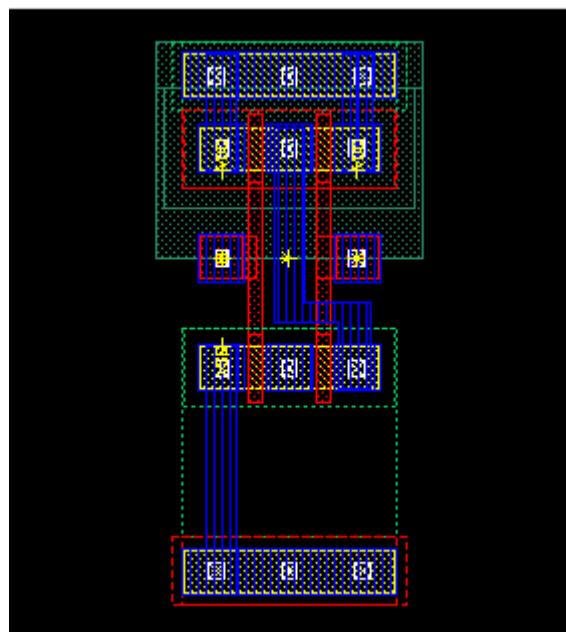
POLY_TO_PTR_SPACE	2.6	5.2
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POLY_TO_NTR_SPACE	2.6	5.2
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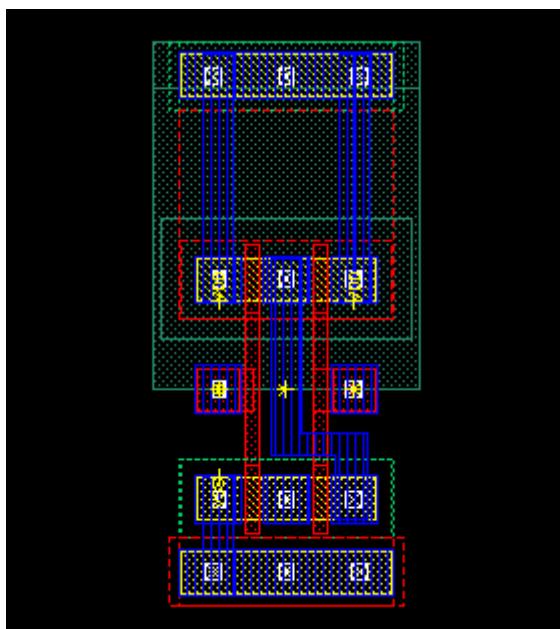


PTAP_TO_TR_SPACE	0	5.0
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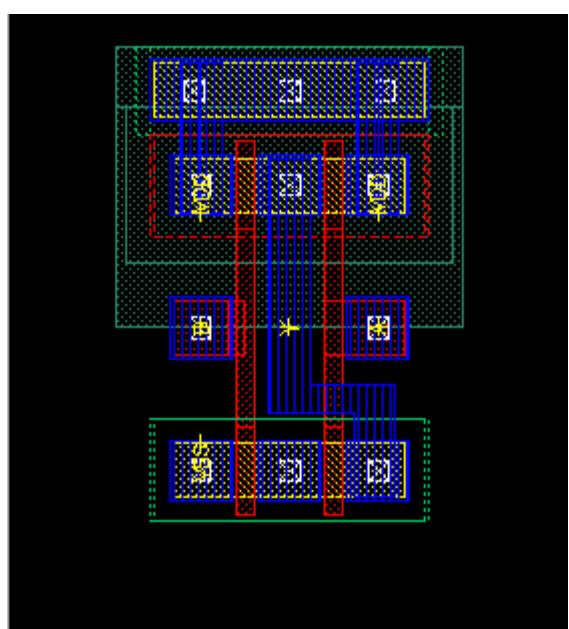


6.3 nand2

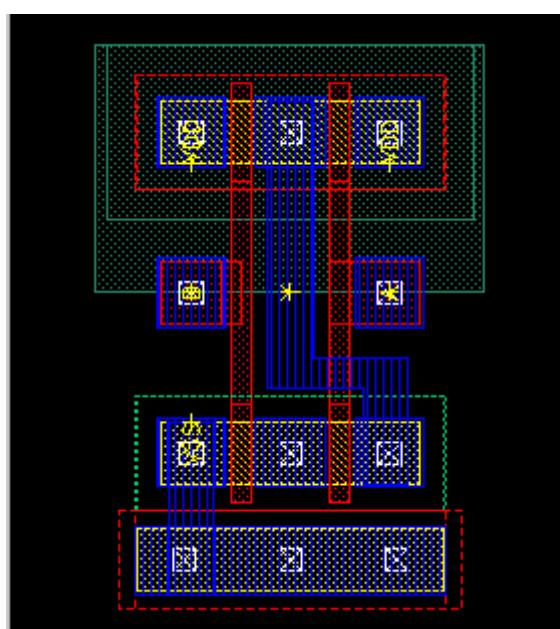
NTAP_TO_TR_SPACE	0	5
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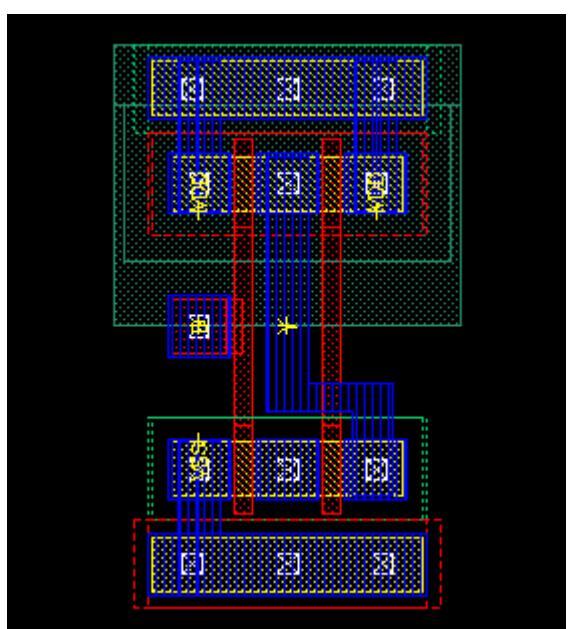
PTAP	<input checked="" type="checkbox"/>	<input type="checkbox"/>
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NTAP	<input checked="" type="checkbox"/>	<input type="checkbox"/>
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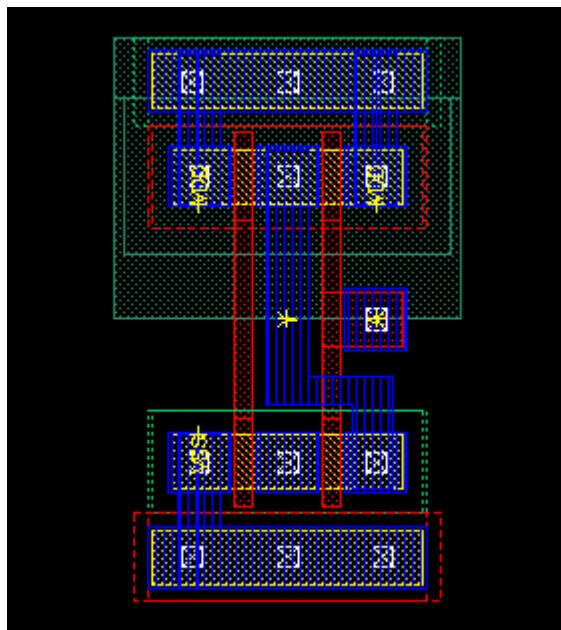


POLY1CONT A	<input checked="" type="checkbox"/>	<input type="checkbox"/>
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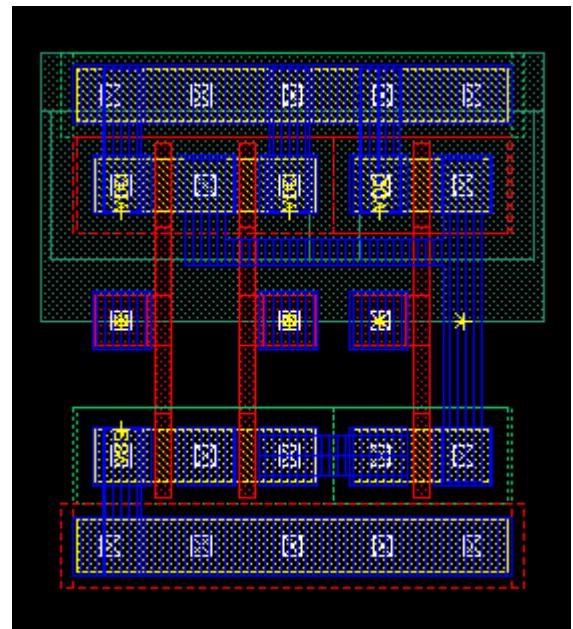
6.3 nand2

POLY1CONTB

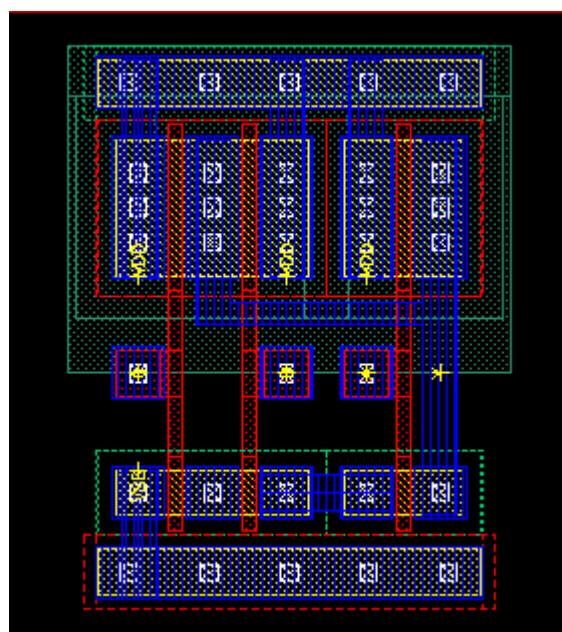


6.4 nand3

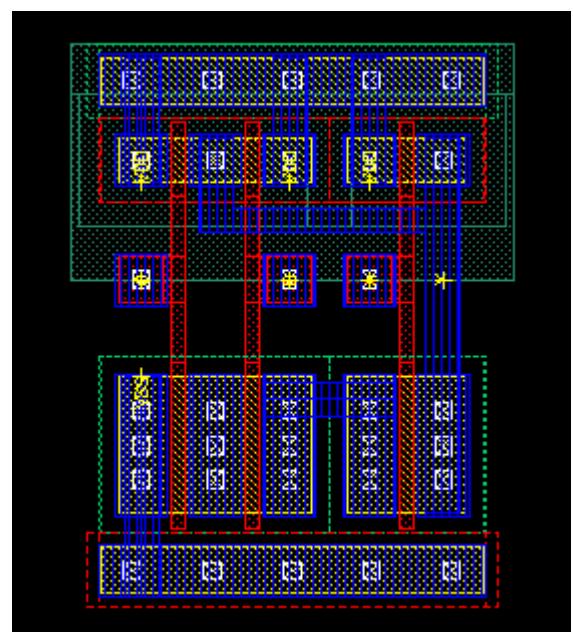
Parameter	Default	Change
P_WIDTH	1.6	<i>value</i>
N_WIDTH	1.6	<i>value</i>
LENGTH	0.5	<i>value</i>
POLY_TO_PTR_SPACE	2.6	<i>value</i>
POLY_TO_NTR_SPACE	2.6	<i>value</i>
PTAP_TO_TR_SPACE	0	<i>value</i>
NTAP_TO_TR_SPACE	0	<i>value</i>
PTAP	<input checked="" type="checkbox"/>	<input type="checkbox"/>
NTAP	<input checked="" type="checkbox"/>	<input type="checkbox"/>
POLY1CONT A	<input checked="" type="checkbox"/>	<input type="checkbox"/>
POLY1CONT B	<input checked="" type="checkbox"/>	<input type="checkbox"/>
POLY1CONT C	<input checked="" type="checkbox"/>	<input type="checkbox"/>



P_WIDTH	1.6	4.8
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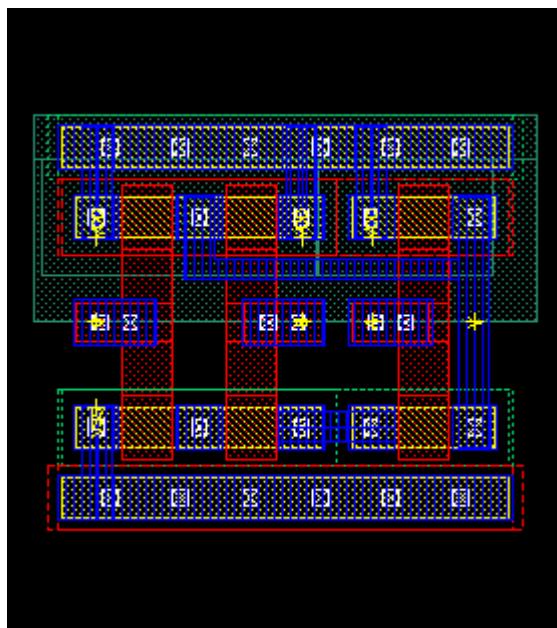


N_WIDTH	1.6	4.8
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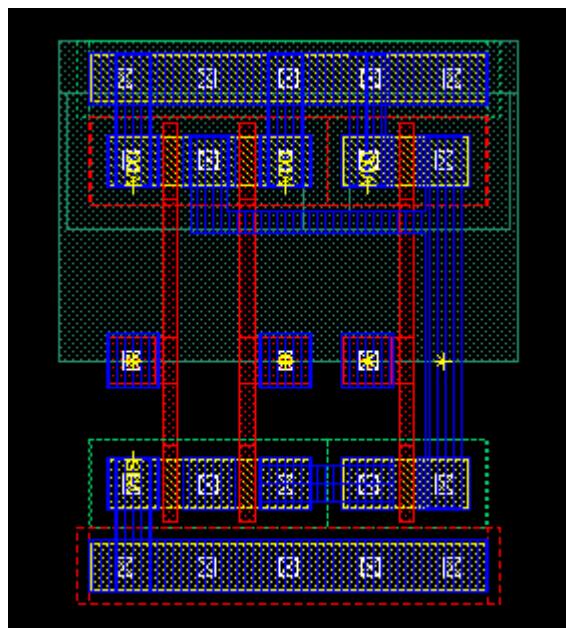


6.4 nand3

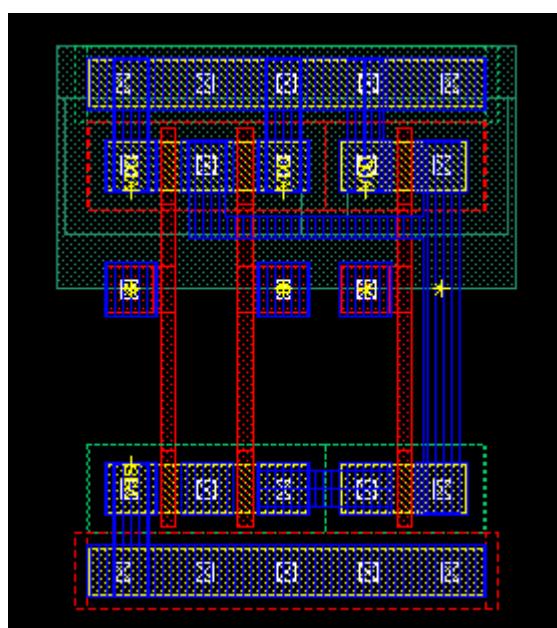
LENGTH	0.5	2
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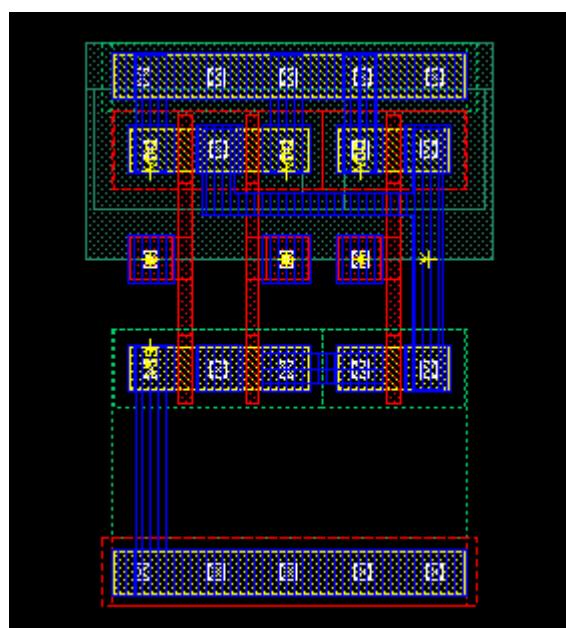
POLY_TO_PTR_SPACE	2.6	5.2
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POLY_TO_NTR_SPACE	2.6	5.2
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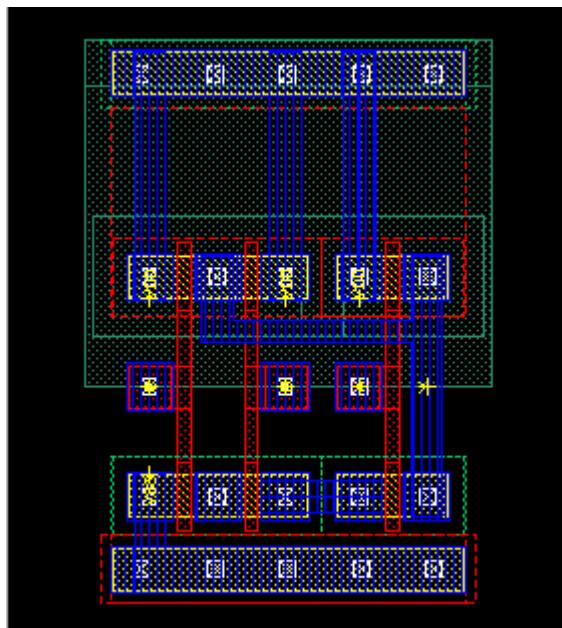


PTAP_TO_TR_SPACE	0	5.0
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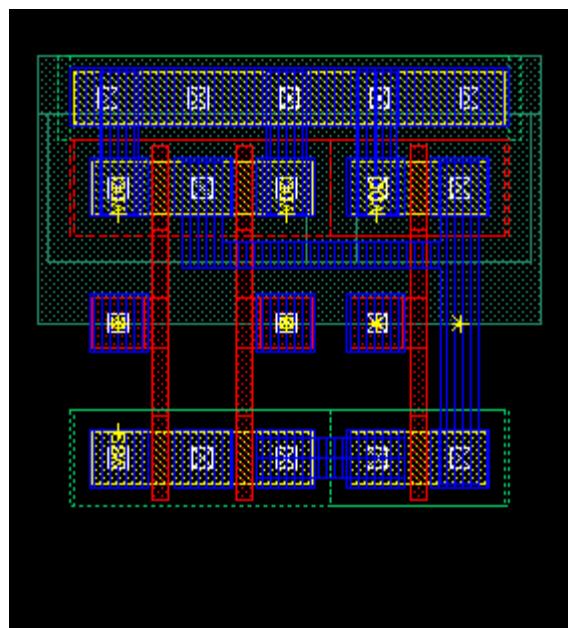


6.4 nand3

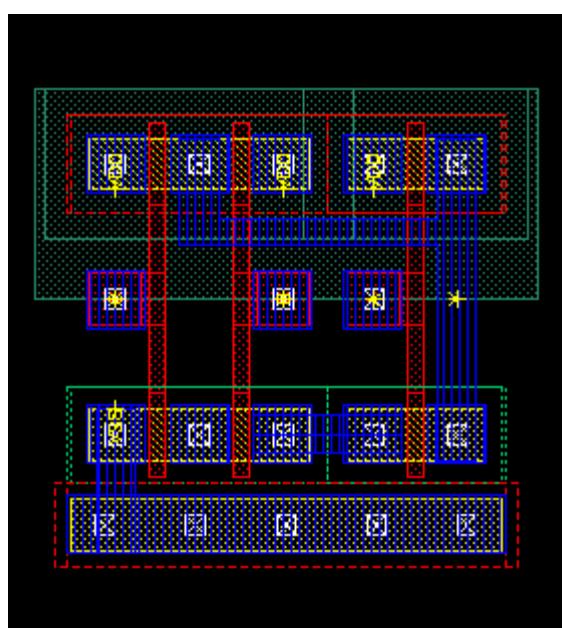
NTAP_TO_TR_SPACE 0 5



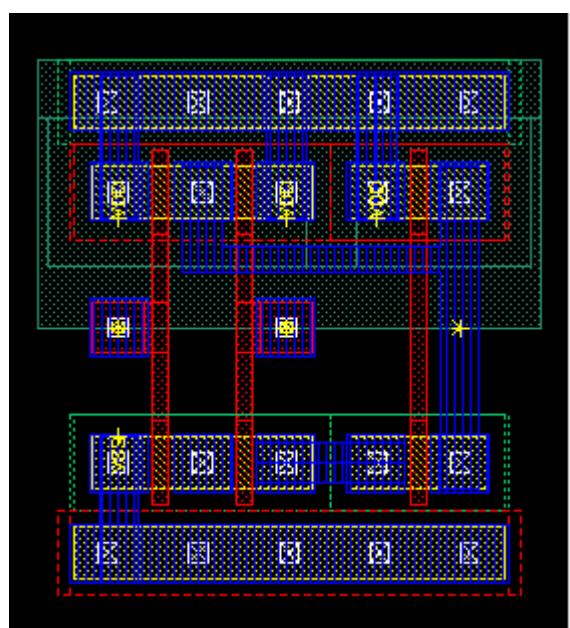
PTAP



NTAP

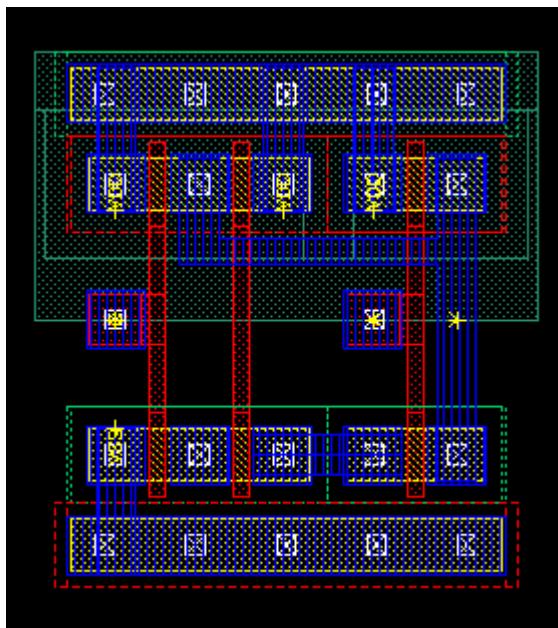


POLY1CONT A

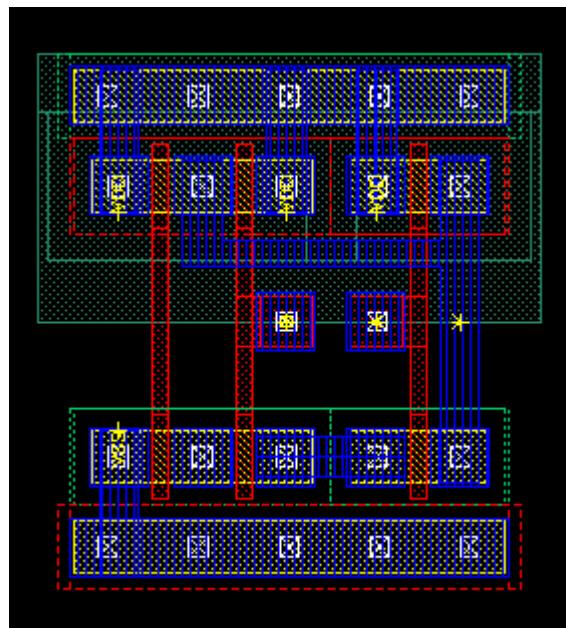


6.4 nand3

POLY1CONTB

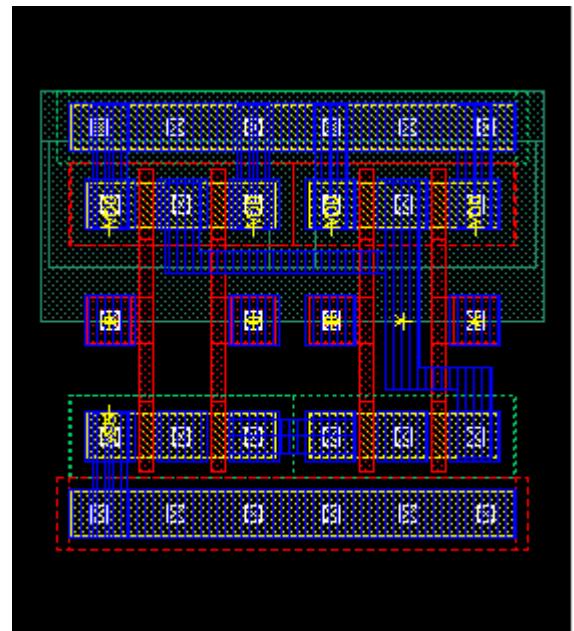


POLY1CONTC

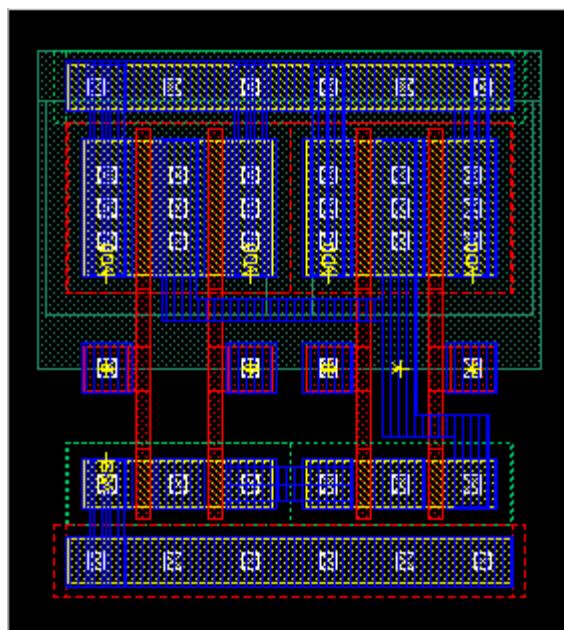


6.5 nand4

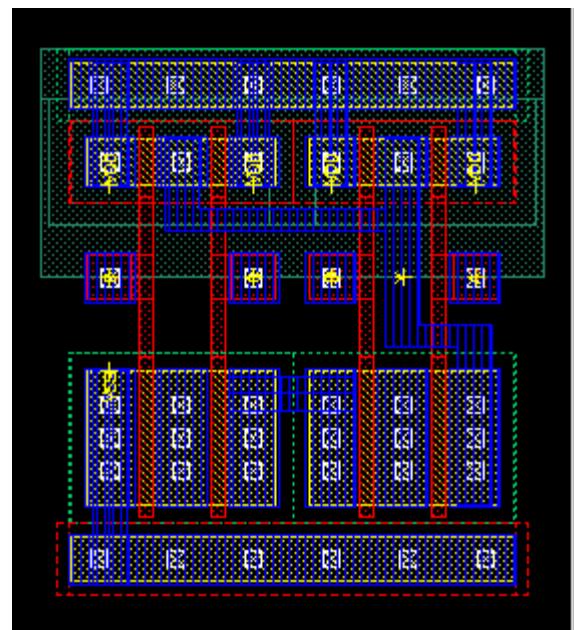
Parameter	Default	Change
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N_WIDTH	1.6	<i>value</i>
LENGTH	0.5	<i>value</i>
POLY_TO_PTR_SPACE	2.6	<i>value</i>
POLY_TO_NTR_SPACE	2.6	<i>value</i>
PTAP_TO_TR_SPACE	0	<i>value</i>
NTAP_TO_TR_SPACE	0	<i>value</i>
PTAP	<input checked="" type="checkbox"/>	<input type="checkbox"/>
NTAP	<input checked="" type="checkbox"/>	<input type="checkbox"/>
POLY1CONT A	<input checked="" type="checkbox"/>	<input type="checkbox"/>
POLY1CONT B	<input checked="" type="checkbox"/>	<input type="checkbox"/>
POLY1CONT C	<input checked="" type="checkbox"/>	<input type="checkbox"/>
POLY1CONT D	<input checked="" type="checkbox"/>	<input type="checkbox"/>



P_WIDTH	1.6	4.8
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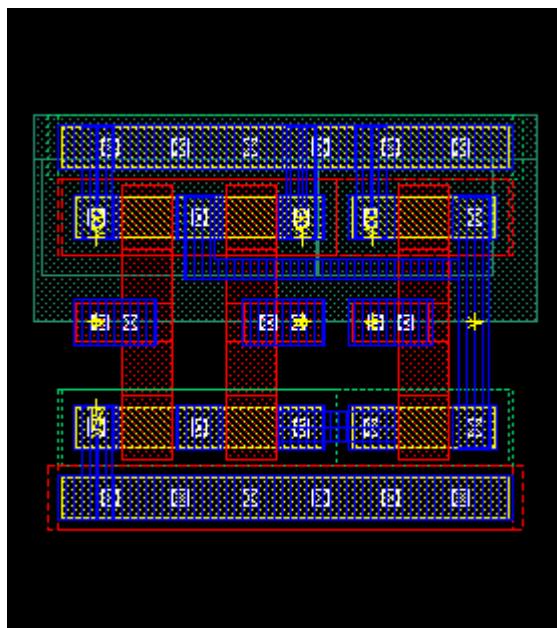


N_WIDTH	1.6	4.8
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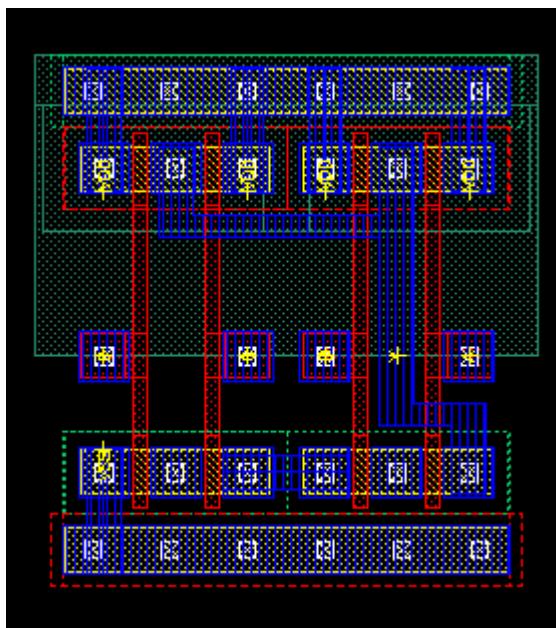


6.5 nand4

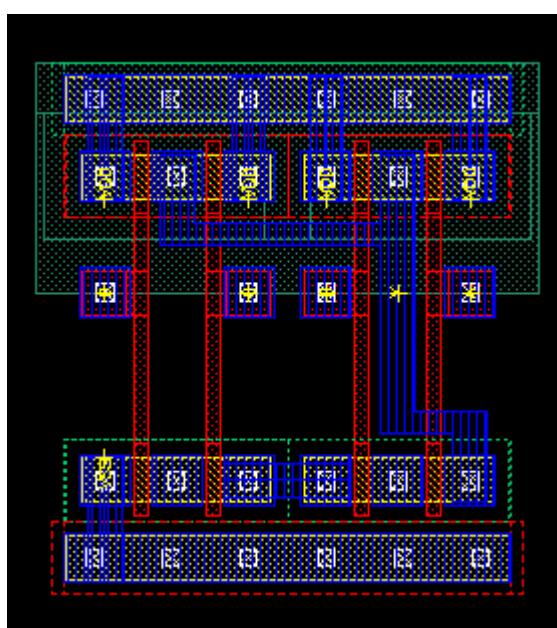
LENGTH	0.5	2
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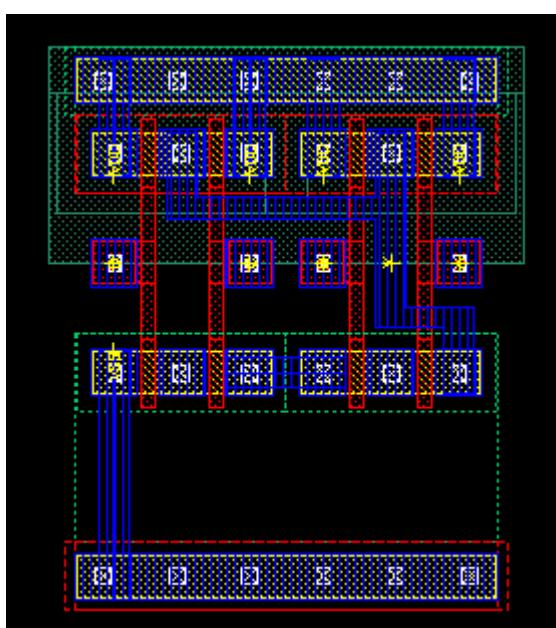
POLY_TO_PTR_SPACE	2.6	5.2
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POLY_TO_NTR_SPACE	2.6	5.2
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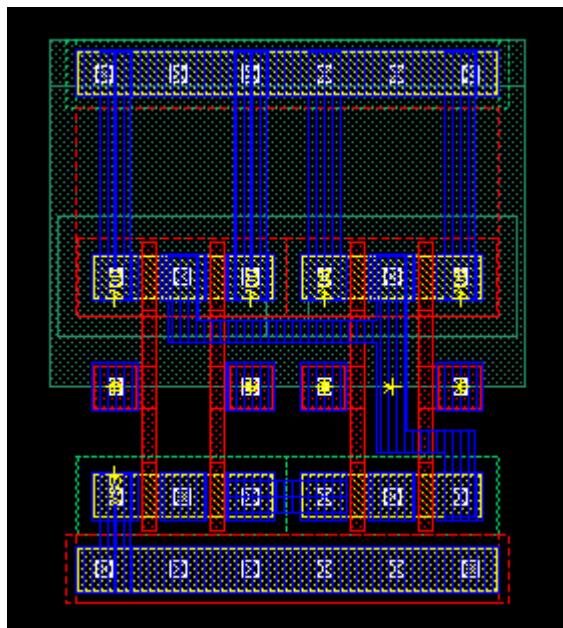


PTAP_TO_TR_SPACE	0	5.0
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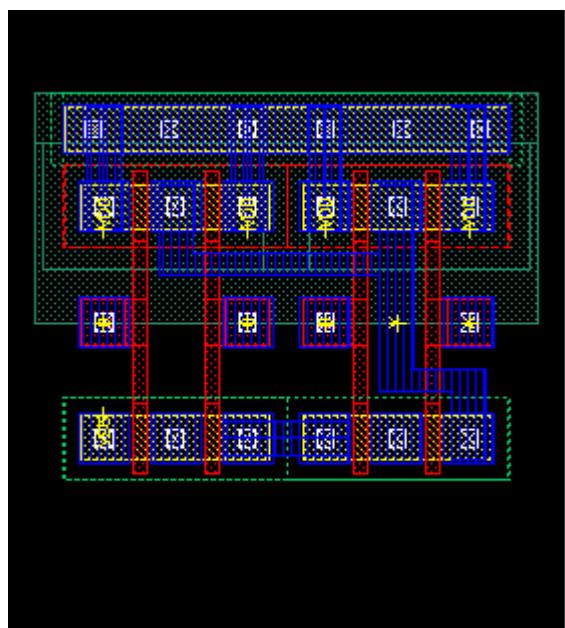


6.5 nand4

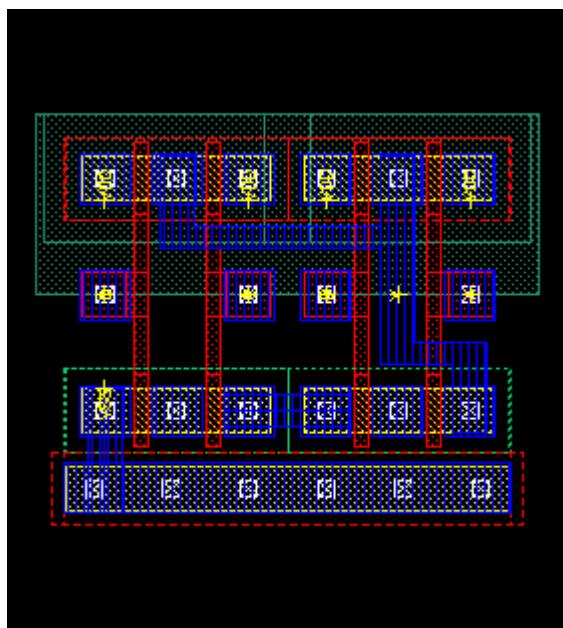
NTAP_TO_TR_SPACE 0 5



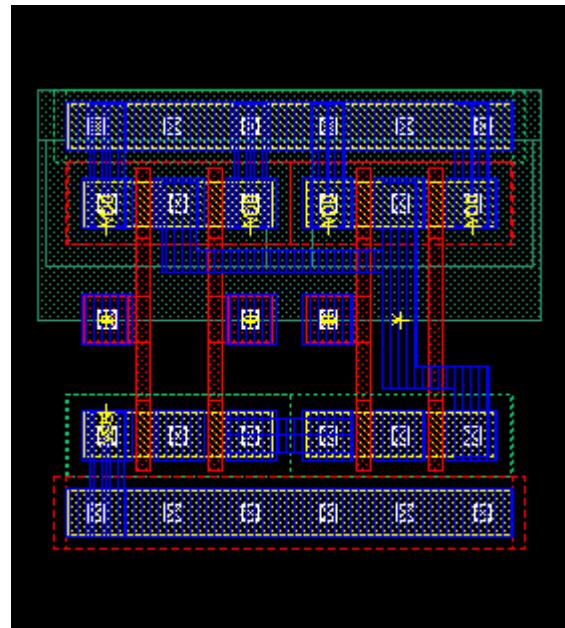
PTAP



NTAP

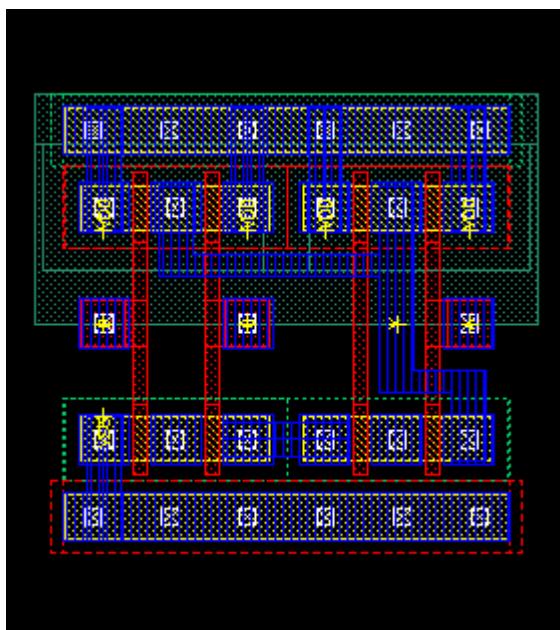


POLY1CONT A

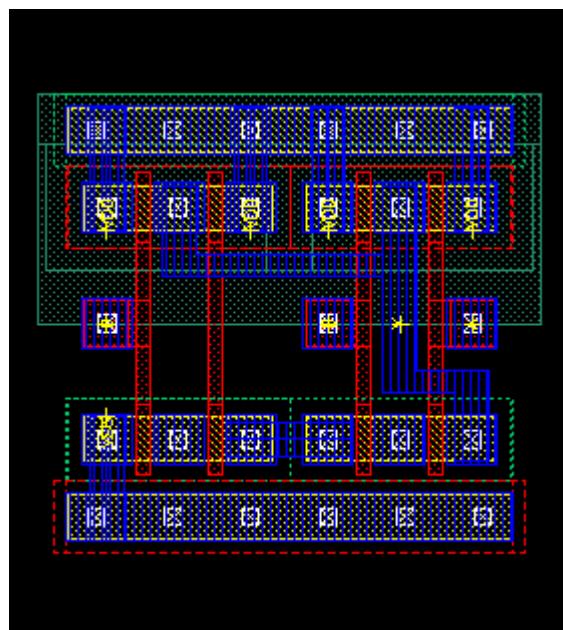


6.5 nand4

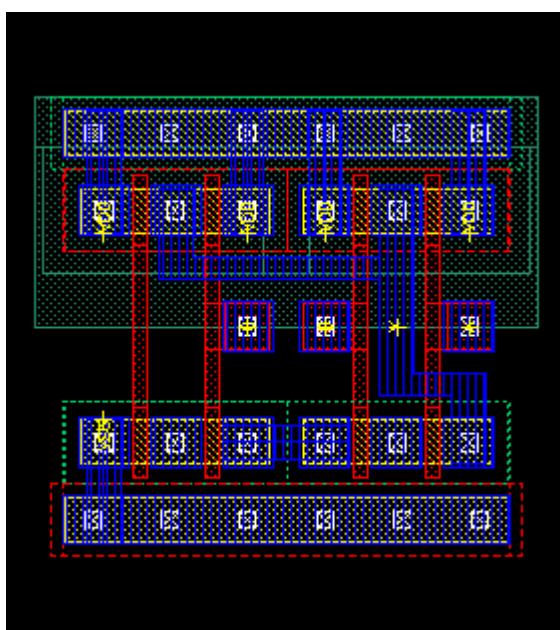
POLY1CONTB



POLY1CONTC

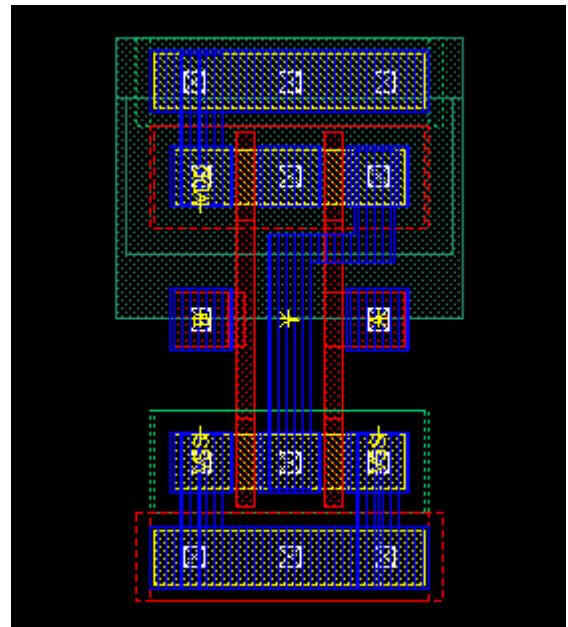


POLY1CONTD

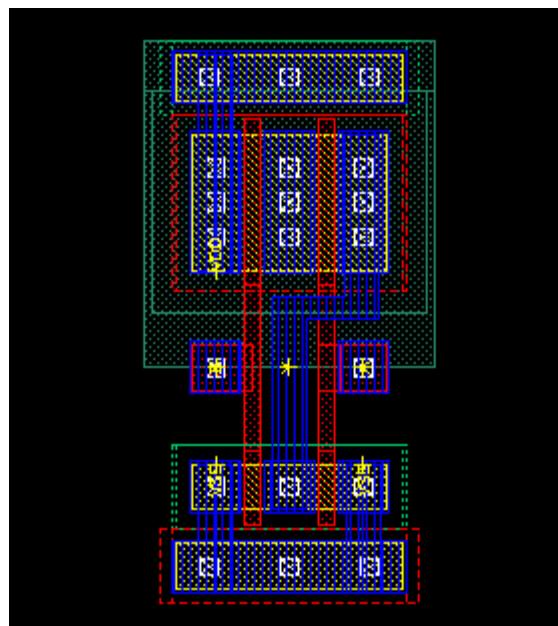


6.6 nor2

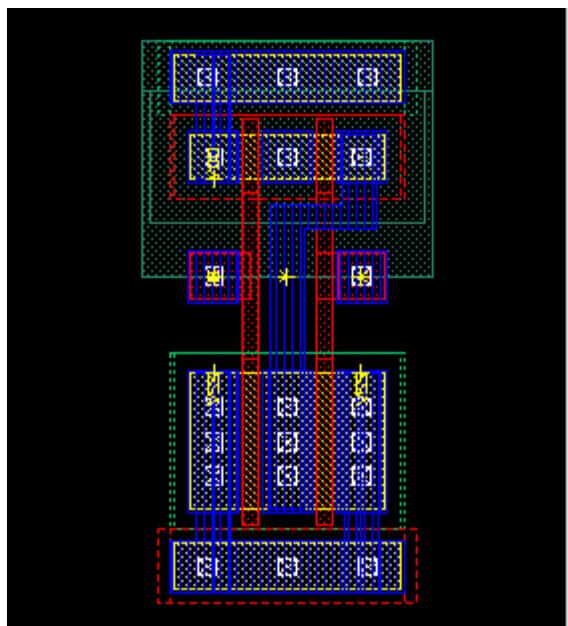
Parameter	Default	Change
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N_WIDTH	1.6	<i>value</i>
LENGTH	0.5	<i>value</i>
POLY_TO_PTR_SPACE	2.6	<i>value</i>
POLY_TO_NTR_SPACE	2.6	<i>value</i>
PTAP_TO_TR_SPACE	0	<i>value</i>
NTAP_TO_TR_SPACE	0	<i>value</i>
PTAP	<input checked="" type="checkbox"/>	<input type="checkbox"/>
NTAP	<input checked="" type="checkbox"/>	<input type="checkbox"/>
POLY1CONTA	<input checked="" type="checkbox"/>	<input type="checkbox"/>
POLY1CONTB	<input checked="" type="checkbox"/>	<input type="checkbox"/>



P_WIDTH	1.6	4.8
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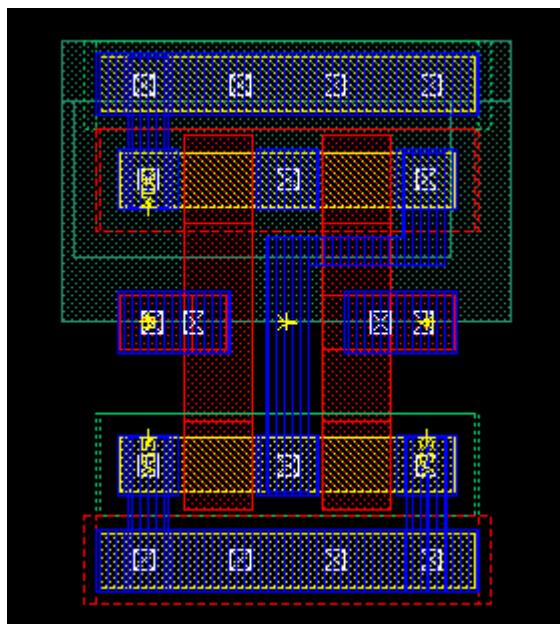


N_WIDTH	1.6	4.8
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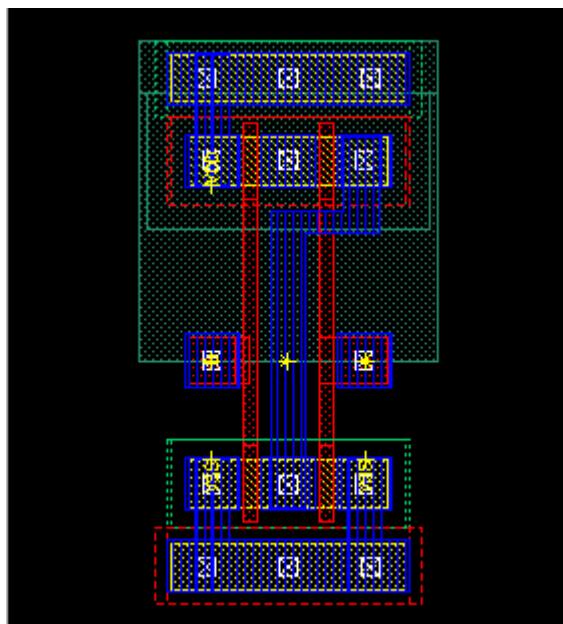


6.6 nor2

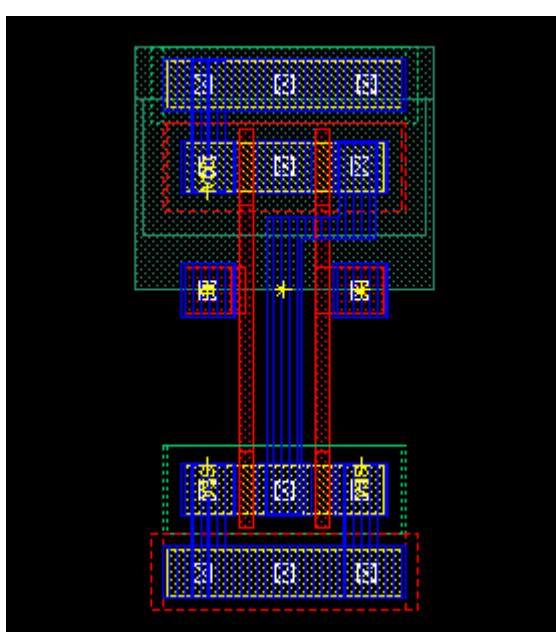
LENGTH	0.5	2
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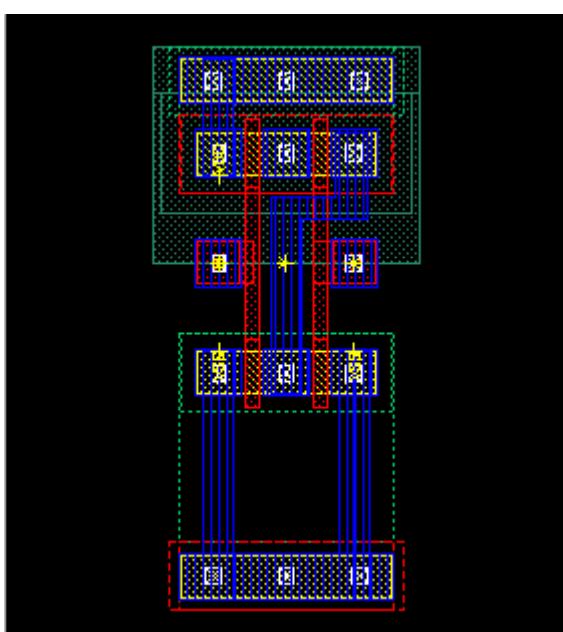
POLY_TO_PTR_SPACE	2.6	5.2
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POLY_TO_NTR_SPACE	2.6	5.2
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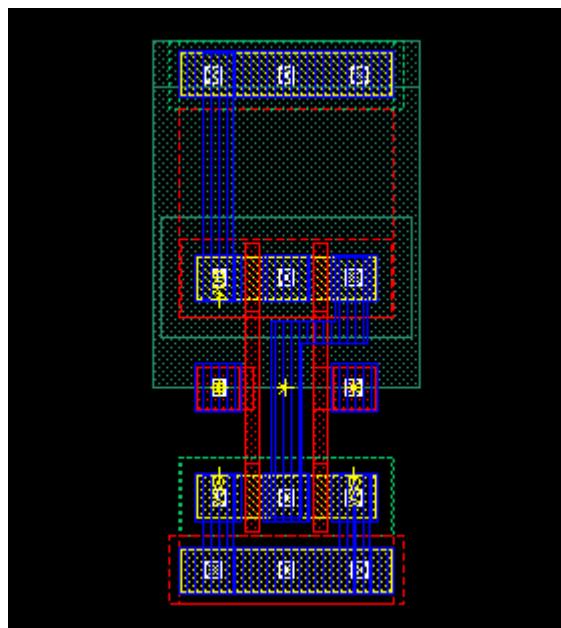


PTAP_TO_TR_SPACE	0	5.0
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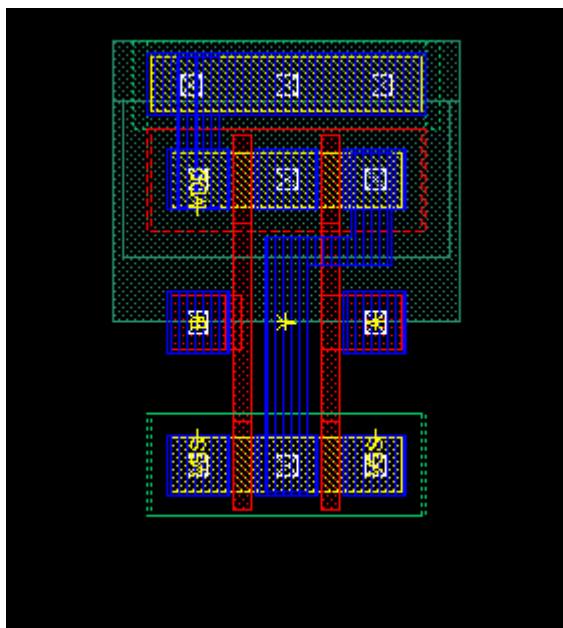


6.6 nor2

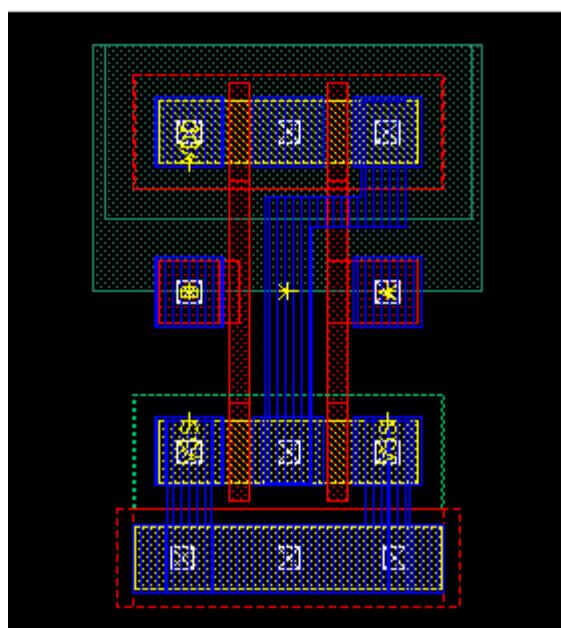
NTAP_TO_TR_SPACE 0 5



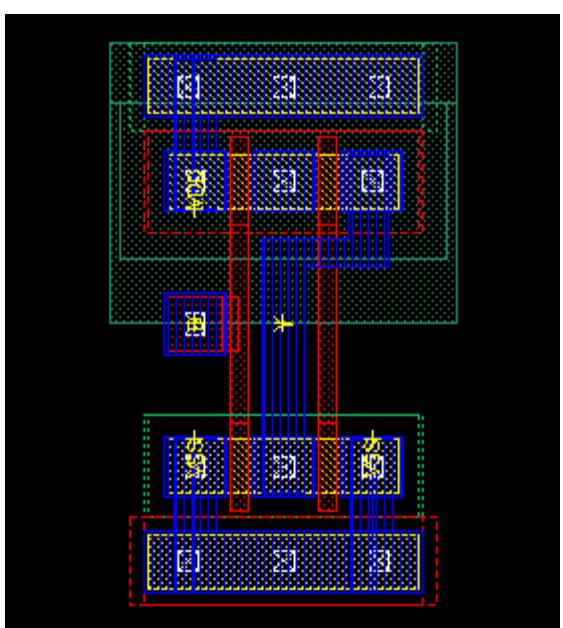
PTAP



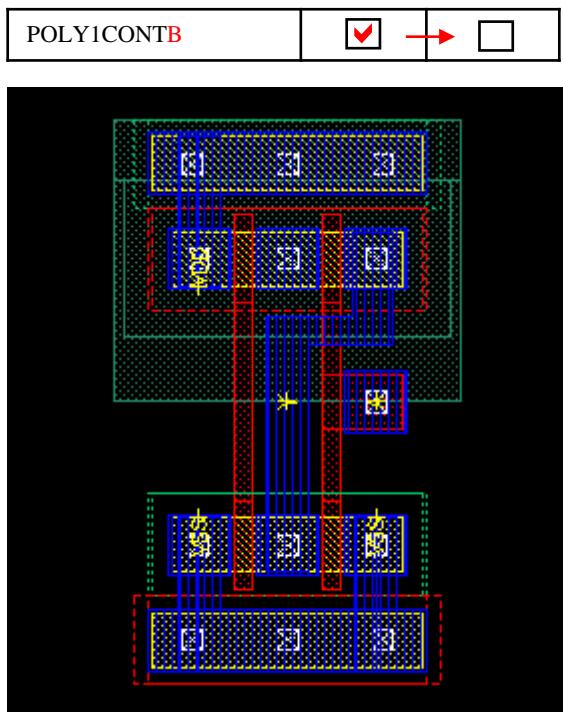
NTAP



POLY1CONT A

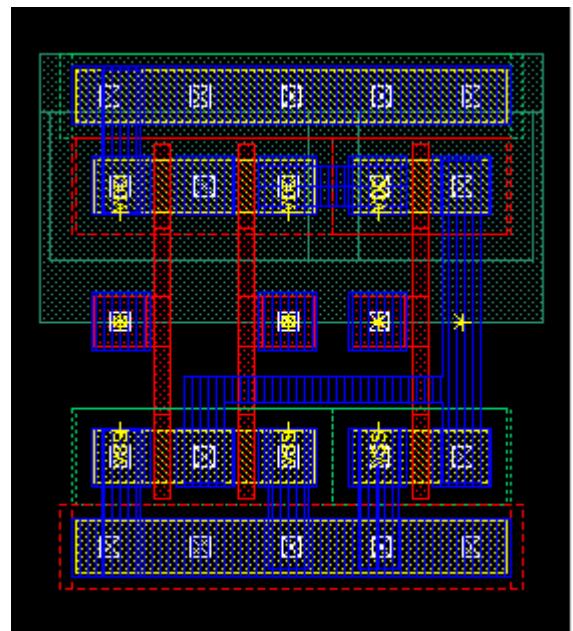


6.6 nor2

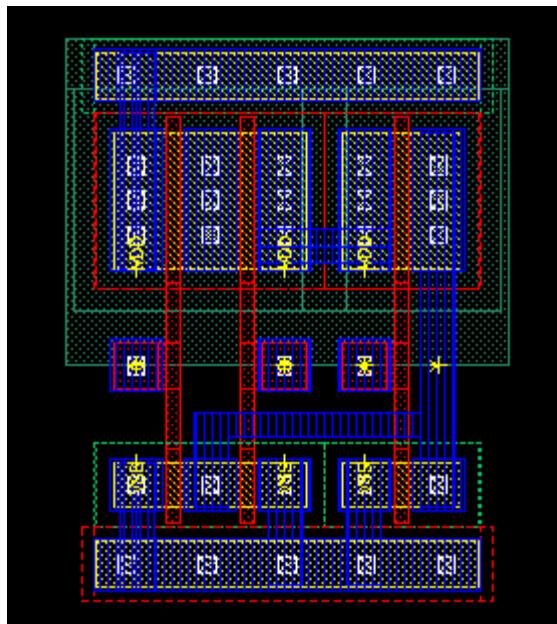


6.7 nor3

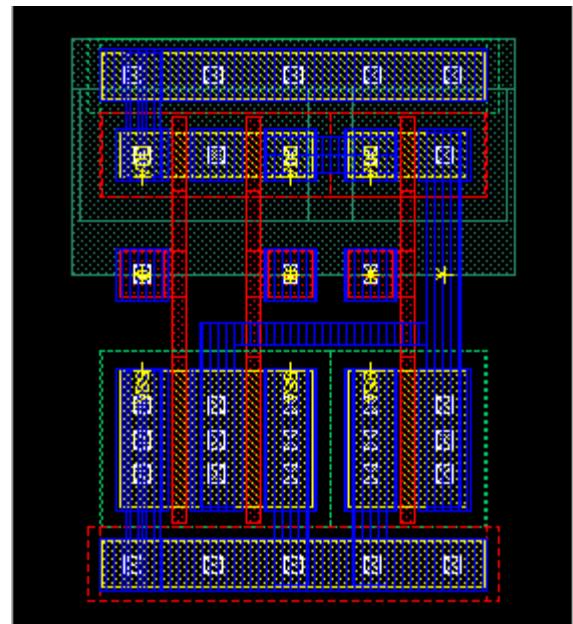
Parameter	Default	Change
P_WIDTH	1.6	<i>value</i>
N_WIDTH	1.6	<i>value</i>
LENGTH	0.5	<i>value</i>
POLY_TO_PTR_SPACE	2.6	<i>value</i>
POLY_TO_NTR_SPACE	2.6	<i>value</i>
PTAP_TO_TR_SPACE	0	<i>value</i>
NTAP_TO_TR_SPACE	0	<i>value</i>
PTAP	<input checked="" type="checkbox"/>	<input type="checkbox"/>
NTAP	<input checked="" type="checkbox"/>	<input type="checkbox"/>
POLY1CONT A	<input checked="" type="checkbox"/>	<input type="checkbox"/>
POLY1CONT B	<input checked="" type="checkbox"/>	<input type="checkbox"/>
POLY1CONT C	<input checked="" type="checkbox"/>	<input type="checkbox"/>



P_WIDTH	1.6	4.8
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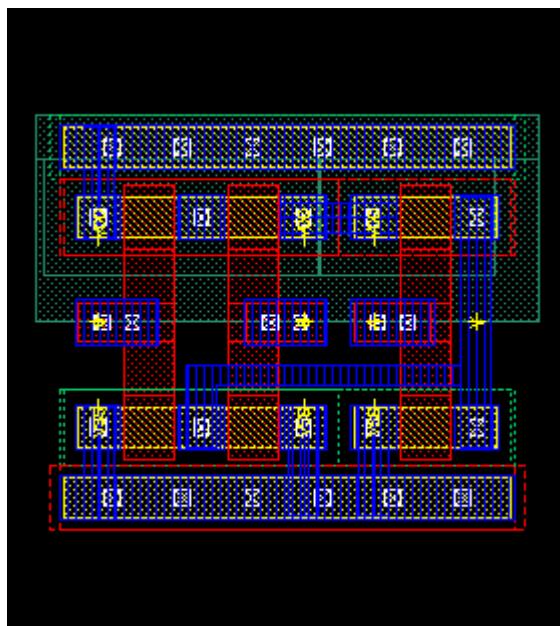


N_WIDTH	1.6	4.8
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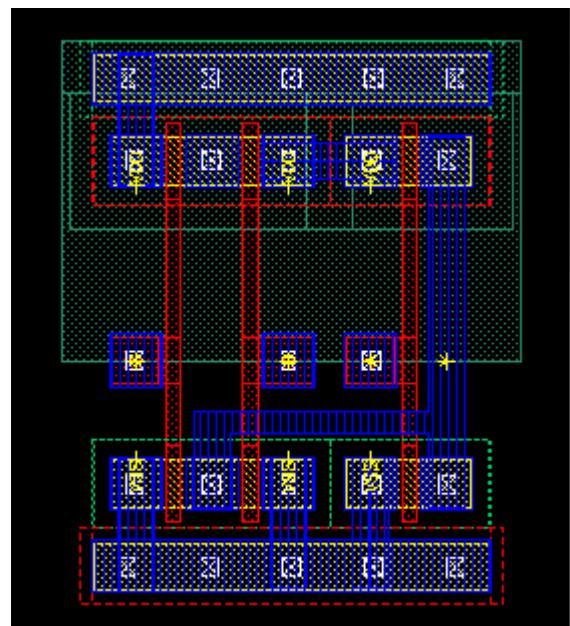


6.7 nor3

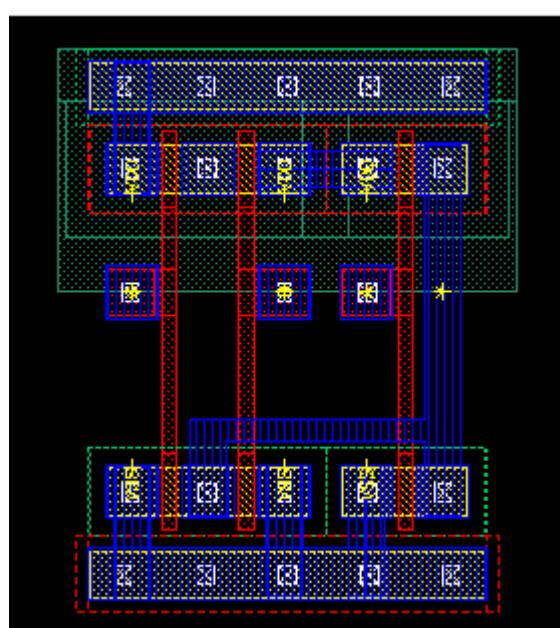
LENGTH	0.5	2
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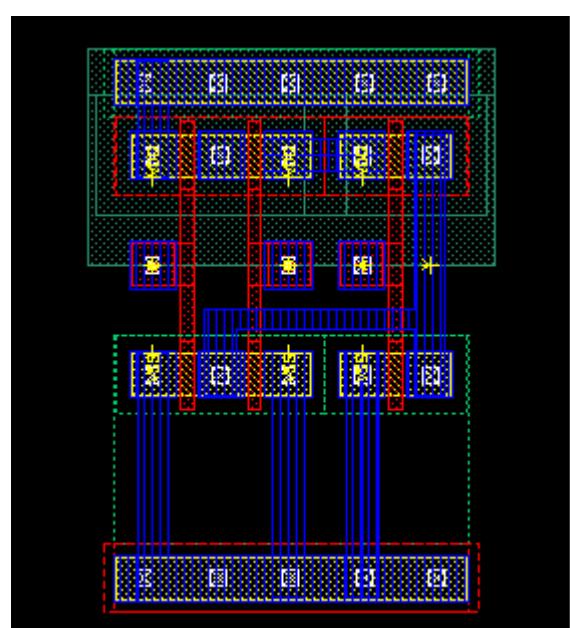
POLY_TO_PTR_SPACE	2.6	5.2
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POLY_TO_NTR_SPACE	2.6	5.2
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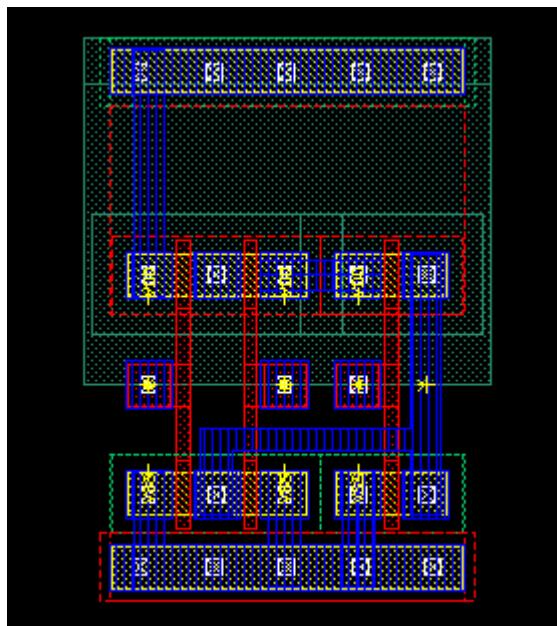


PTAP_TO_TR_SPACE	0	5.0
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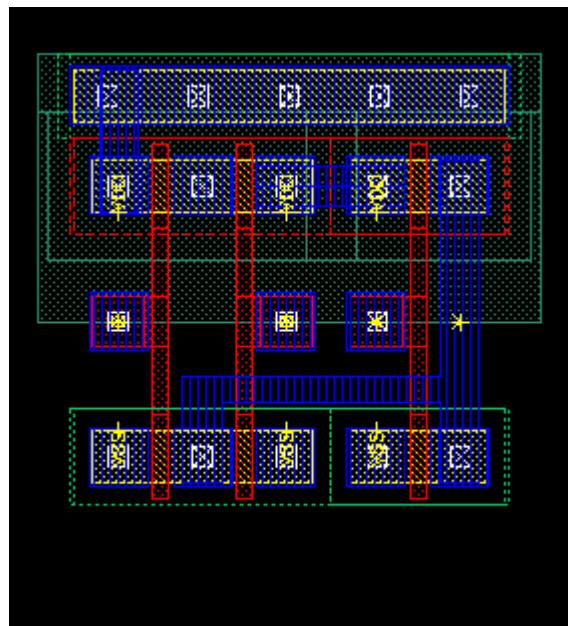


6.7 nor3

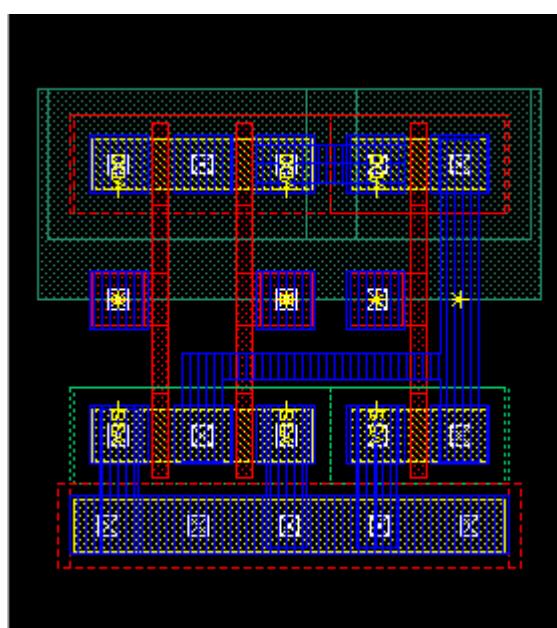
NTAP_TO_TR_SPACE	0	5
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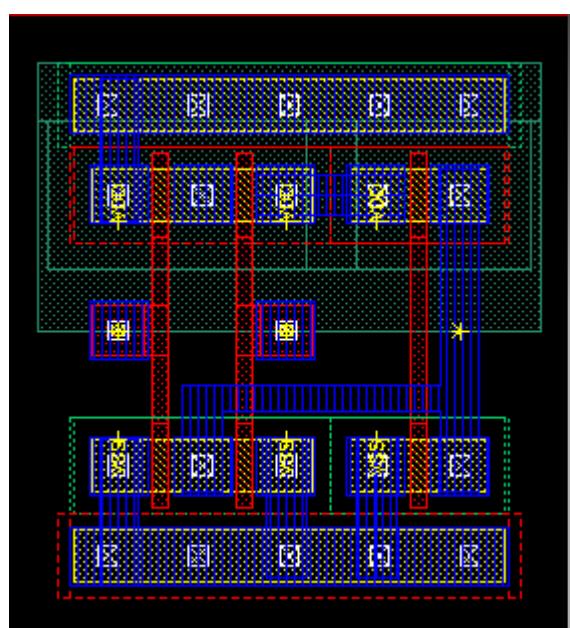
PTAP	<input checked="" type="checkbox"/>	<input type="checkbox"/>
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NTAP	<input checked="" type="checkbox"/>	<input type="checkbox"/>
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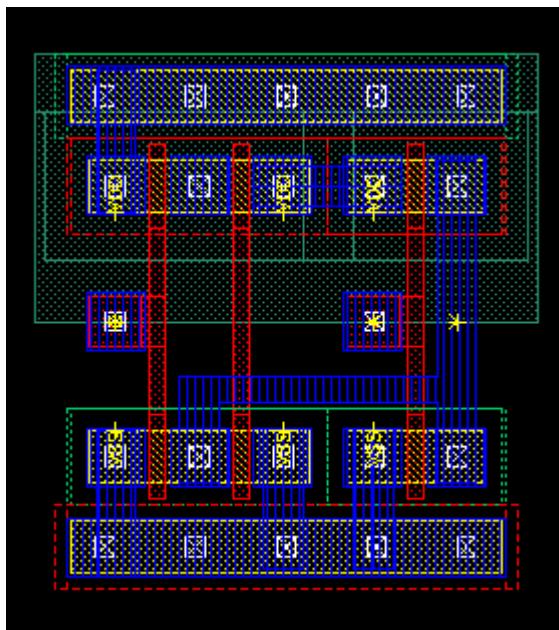


POLY1CONT	<input checked="" type="checkbox"/>	<input type="checkbox"/>
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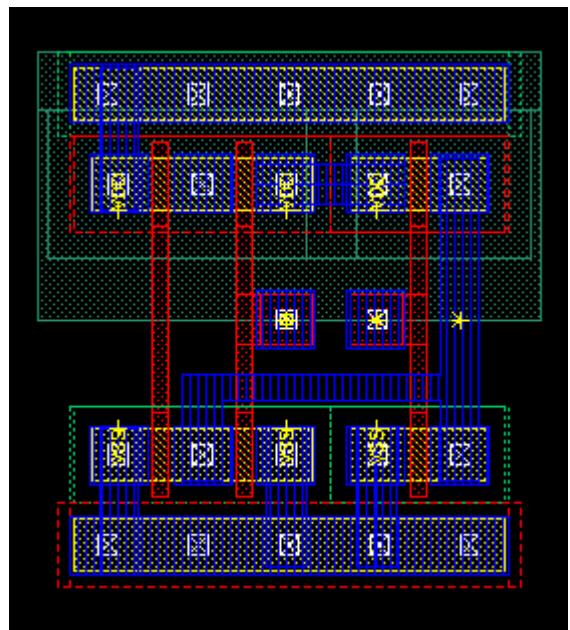


6.7 nor3

POLY1CONTB →

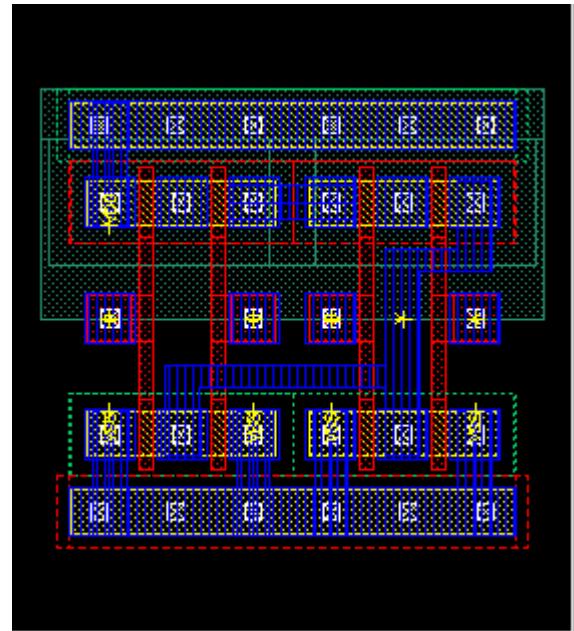


POLY1CONTC →

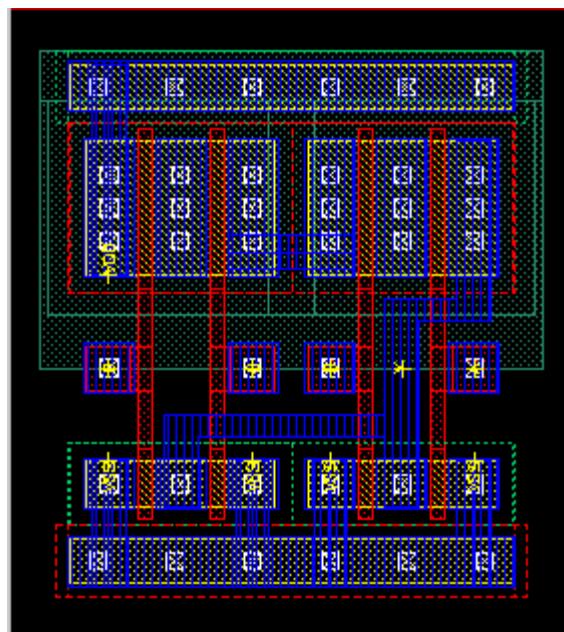


6.8 nor4

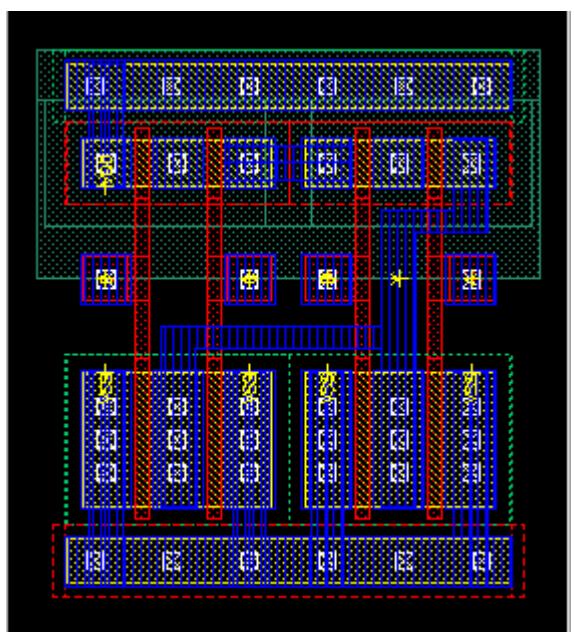
Parameter	Default	Change
P_WIDTH	1.6	<i>value</i>
N_WIDTH	1.6	<i>value</i>
LENGTH	0.5	<i>value</i>
POLY_TO_PTR_SPACE	2.6	<i>value</i>
POLY_TO_NTR_SPACE	2.6	<i>value</i>
PTAP_TO_TR_SPACE	0	<i>value</i>
NTAP_TO_TR_SPACE	0	<i>value</i>
PTAP	<input checked="" type="checkbox"/>	<input type="checkbox"/>
NTAP	<input checked="" type="checkbox"/>	<input type="checkbox"/>
POLY1CONT A	<input checked="" type="checkbox"/>	<input type="checkbox"/>
POLY1CONT B	<input checked="" type="checkbox"/>	<input type="checkbox"/>
POLY1CONT C	<input checked="" type="checkbox"/>	<input type="checkbox"/>
POLY1CONT D	<input checked="" type="checkbox"/>	<input type="checkbox"/>



P_WIDTH	1.6	4.8
---------	-----	-----

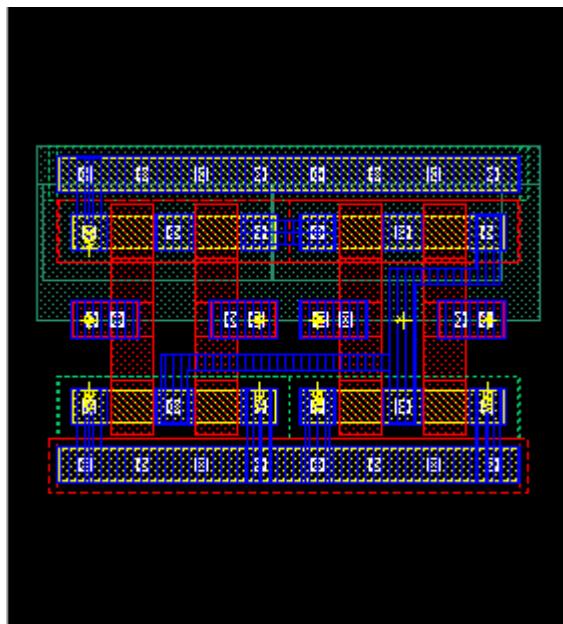


N_WIDTH	1.6	4.8
---------	-----	-----

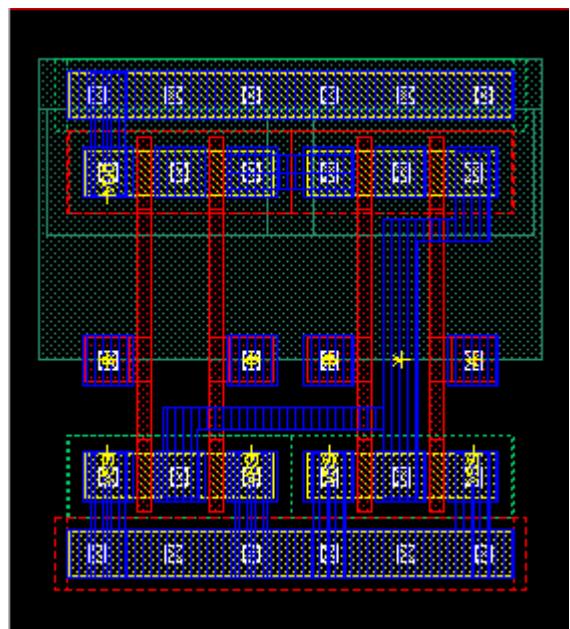


6.8 nor4

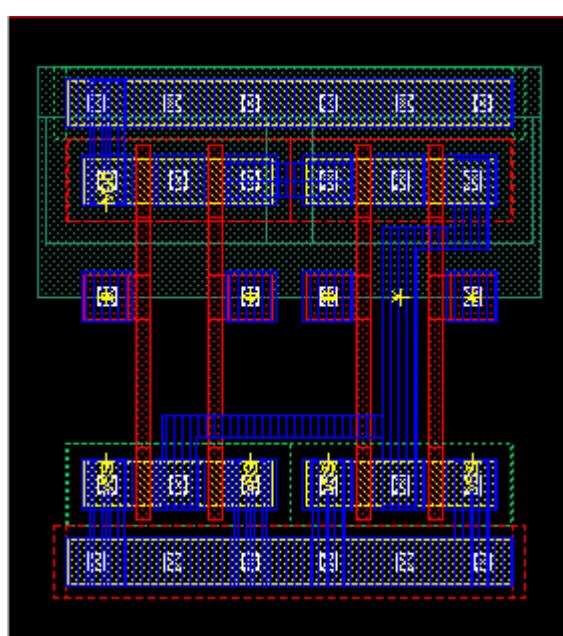
LENGTH	0.5	2
--------	-----	---



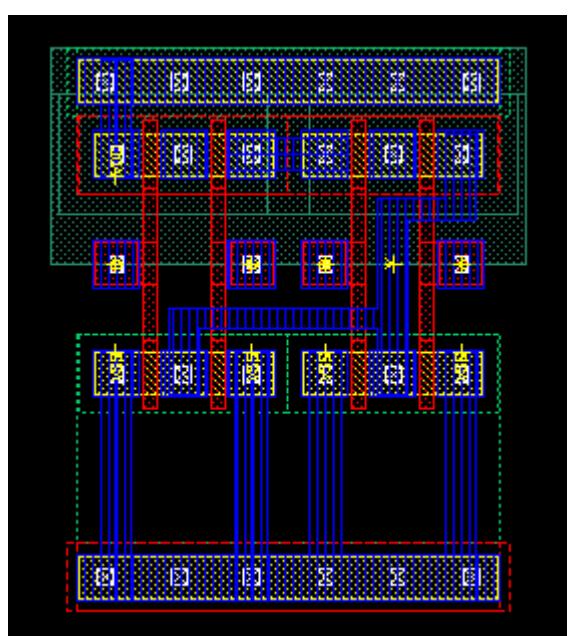
POLY_TO_PTR_SPACE	2.6	5.2
-------------------	-----	-----



POLY_TO_NTR_SPACE	2.6	5.2
-------------------	-----	-----

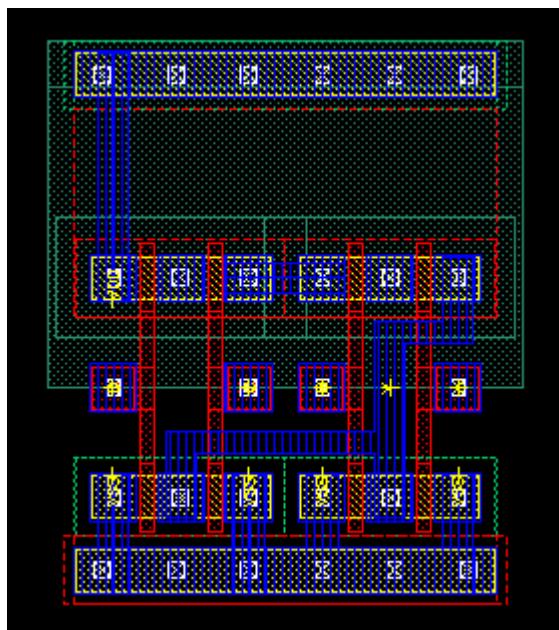


PTAP_TO_TR_SPACE	0	5.0
------------------	---	-----

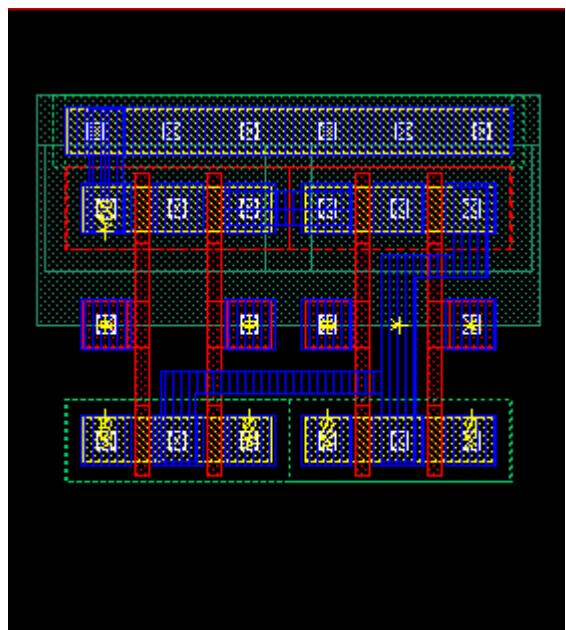


6.8 nor4

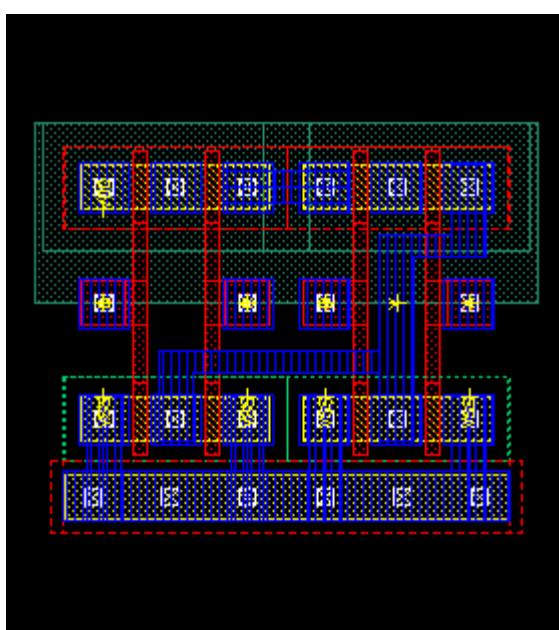
NTAP_TO_TR_SPACE 0 5



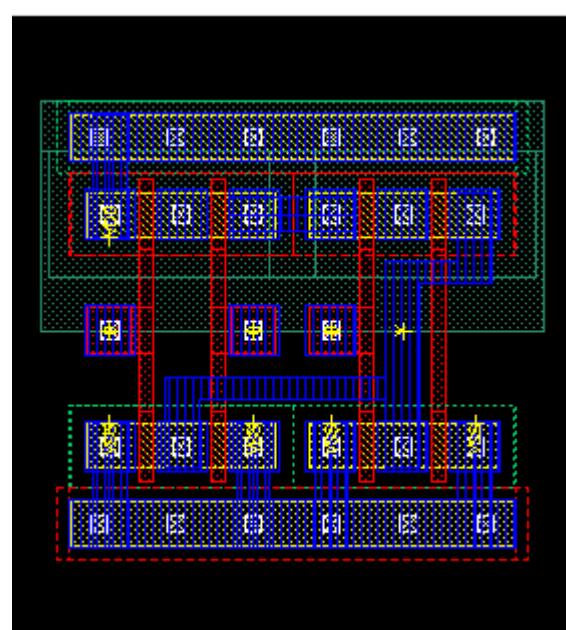
PTAP



NTAP

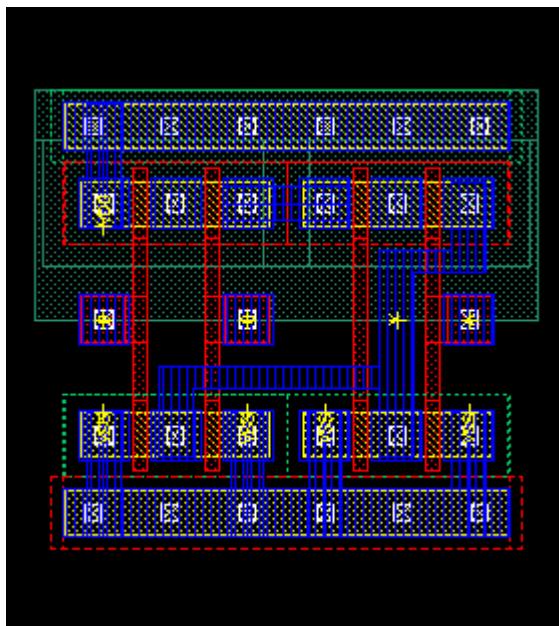


POLY1CONT A

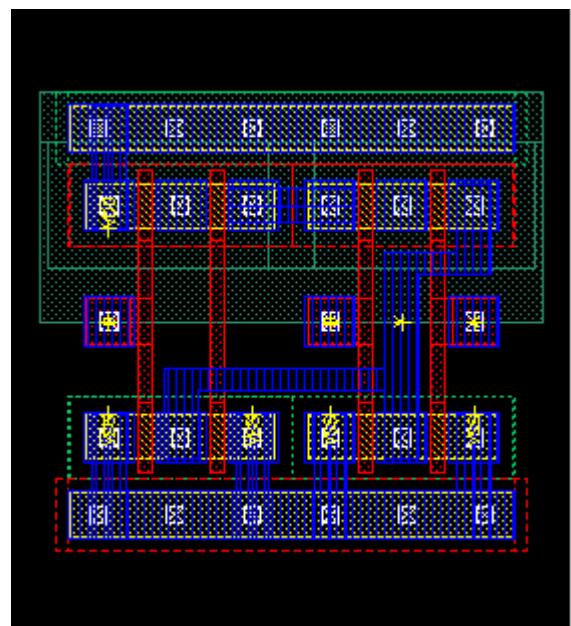


6.8 nor4

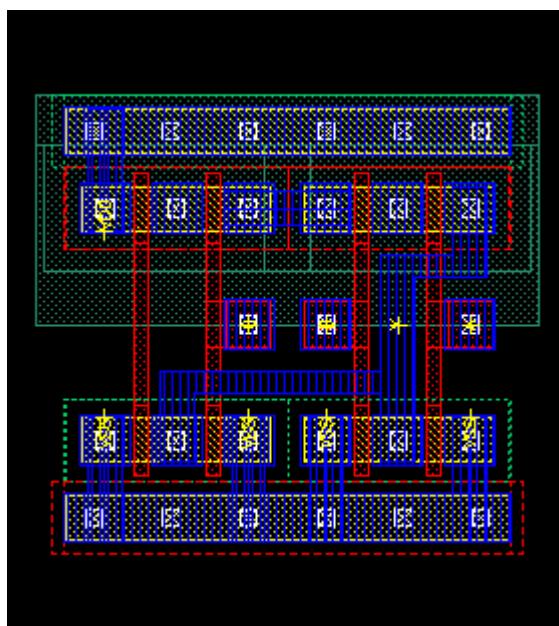
POLY1CONTB



POLY1CONTC

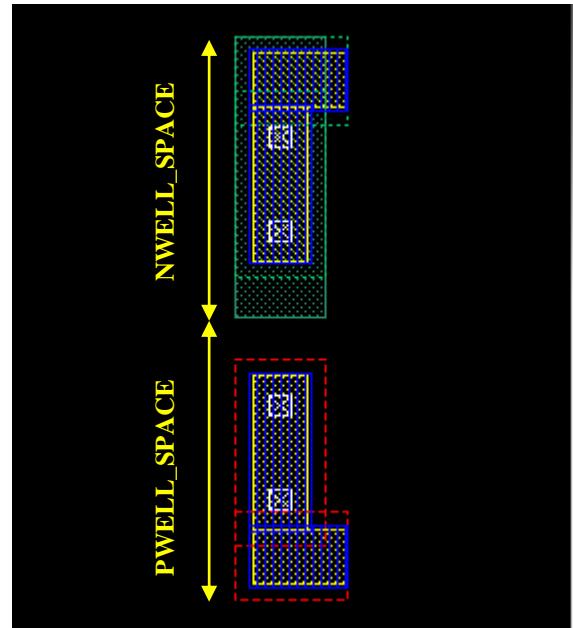


POLY1CONTD

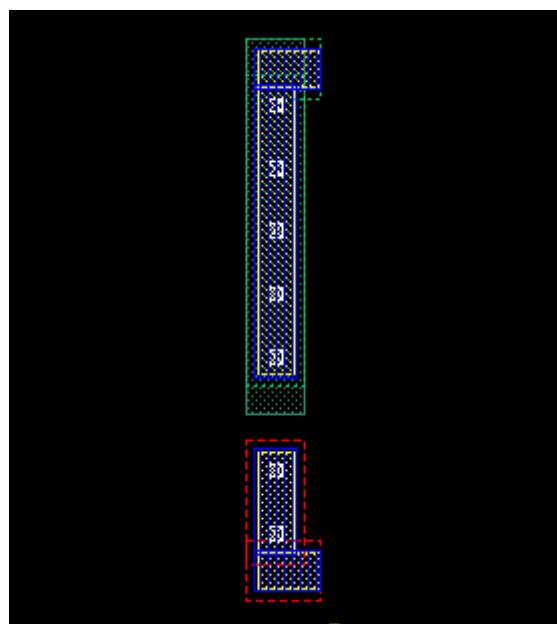


6.9 edge

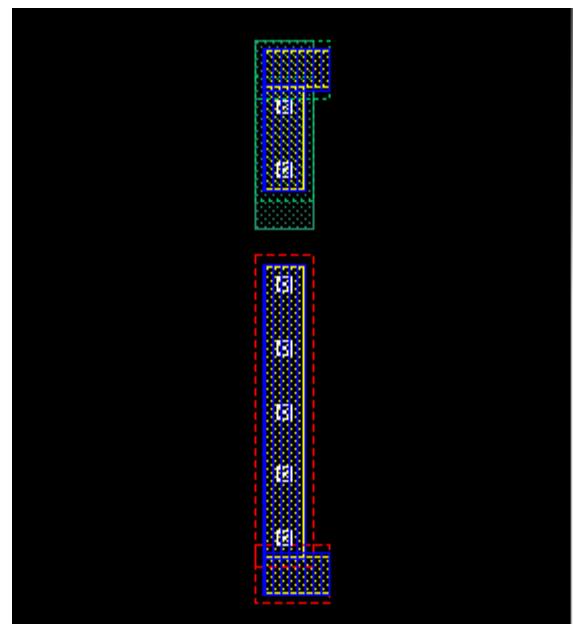
Parameter	Default	Change
NWELL_SPACE	8.3	<i>value</i>
PWELL_SPACE	8.3	<i>value</i>



NWELL_SPACE	8.3	16.6
-------------	-----	------

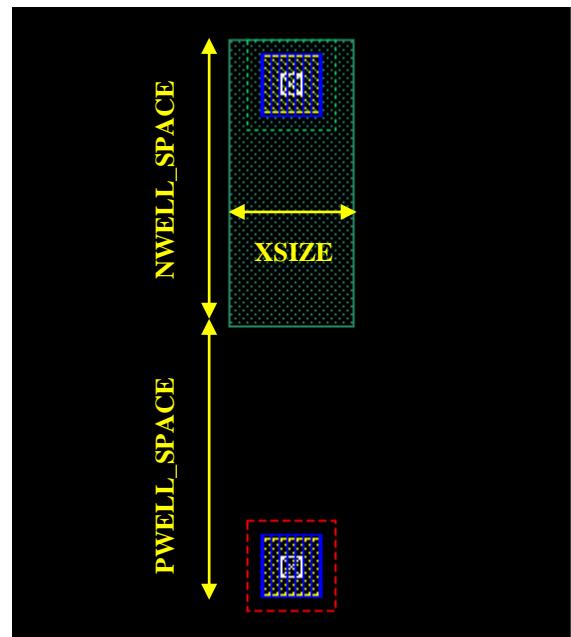


PWELL_SPACE	8.3	16.6
-------------	-----	------

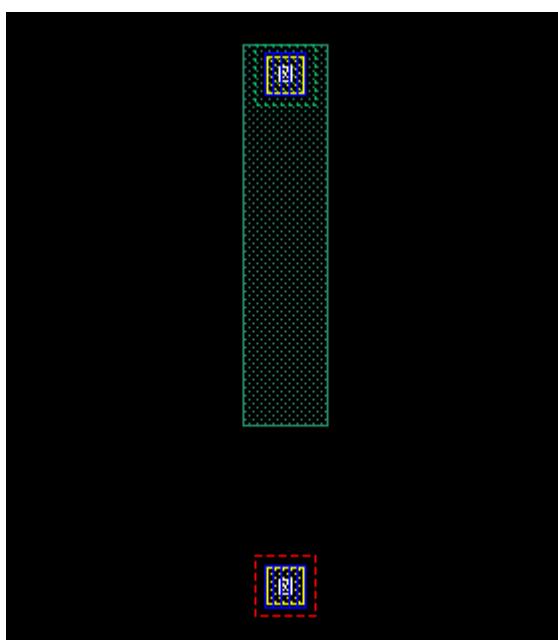


6.10 filler

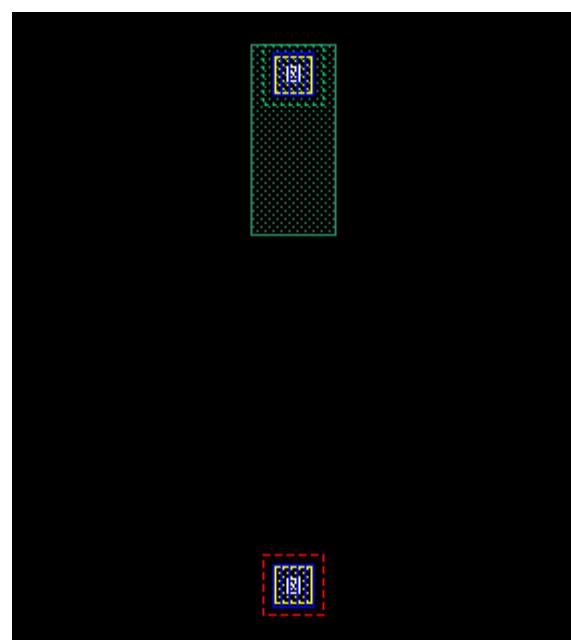
Parameter	Default	Change
NWELL_SPACE	8.3	<i>value</i>
PWELL_SPACE	8.3	<i>value</i>
XSIZE	1.8	<i>value</i>



NWELL_SPACE	8.3	16.6
-------------	-----	------

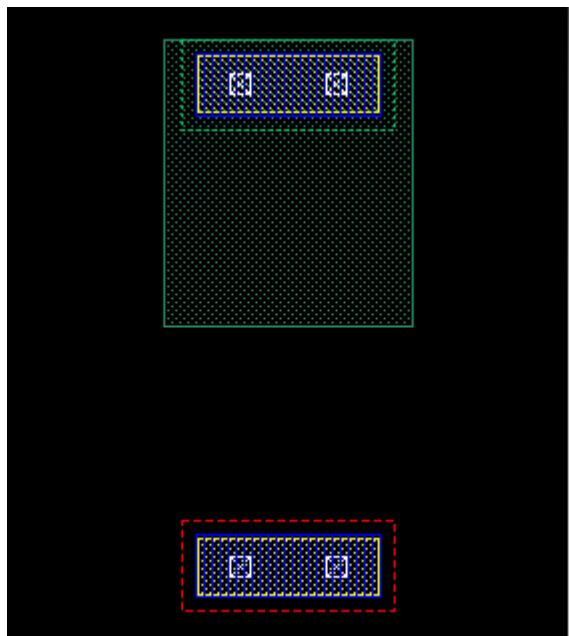


PWELL_SPACE	8.3	16.6
-------------	-----	------

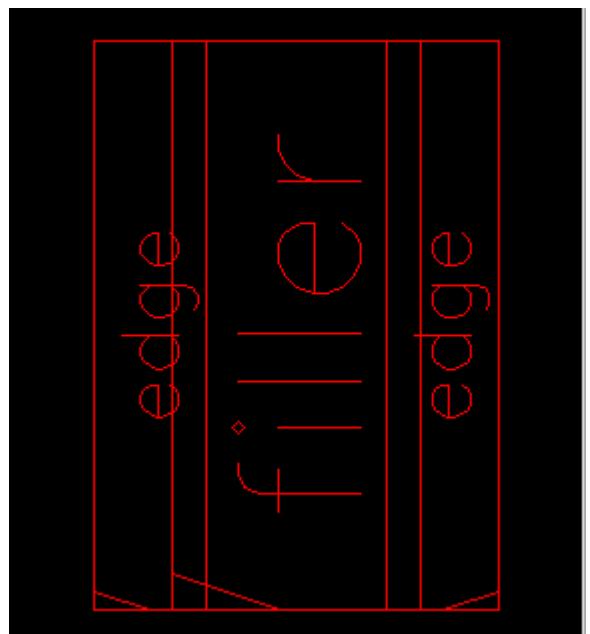
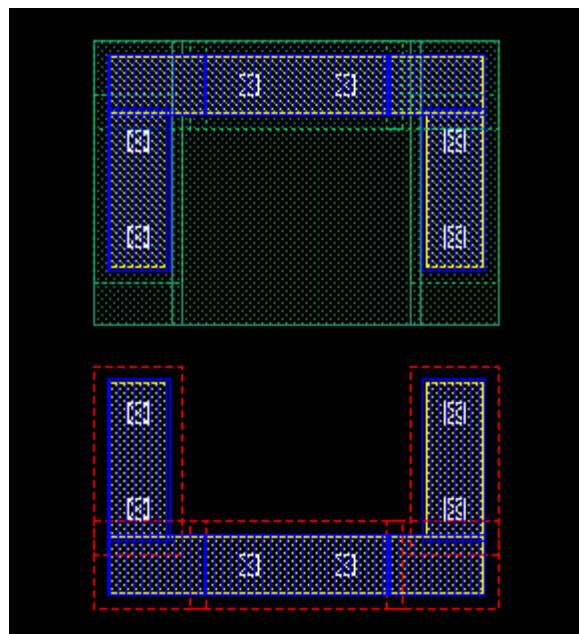


6.10 filler

XSIZE	1.8	5.4
-------	-----	-----



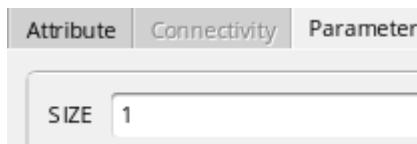
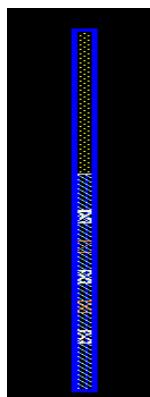
6.11 edge_filler



7. Sealring

7.1 Sealring information [[ETRI 0p5um Analog CMOS 2P3M 5V NSPL pcell](#)]

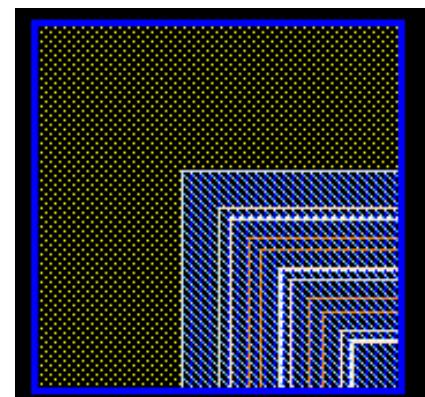
- For protect layout block from DIE cutting, you can use sealring cell in ETRI_0p5um_Analog_CMOS_5p0V_pcell library.
(SEALRING_UNIT, SEALRING_CONER)



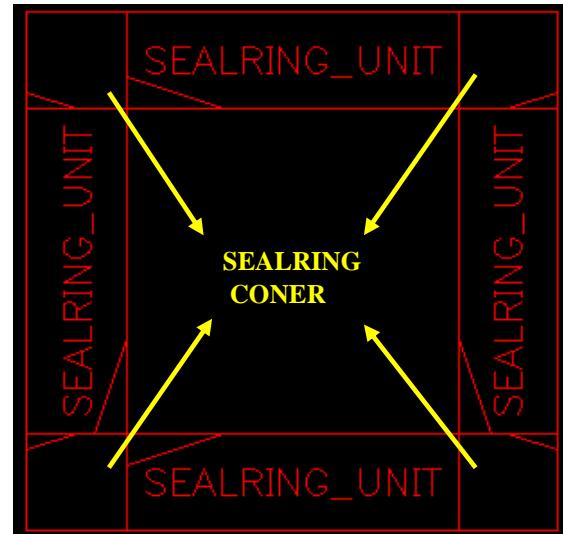
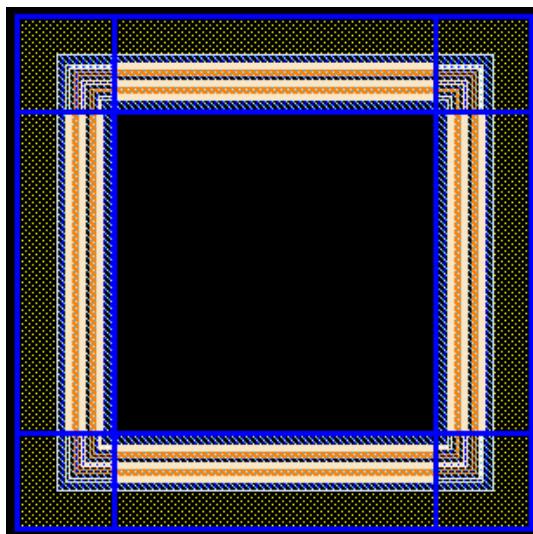
Can adjust size using SIZE parameter

SIZE Minimum value is 1

-SEALRING_UNIT



-SEALRING_CONER

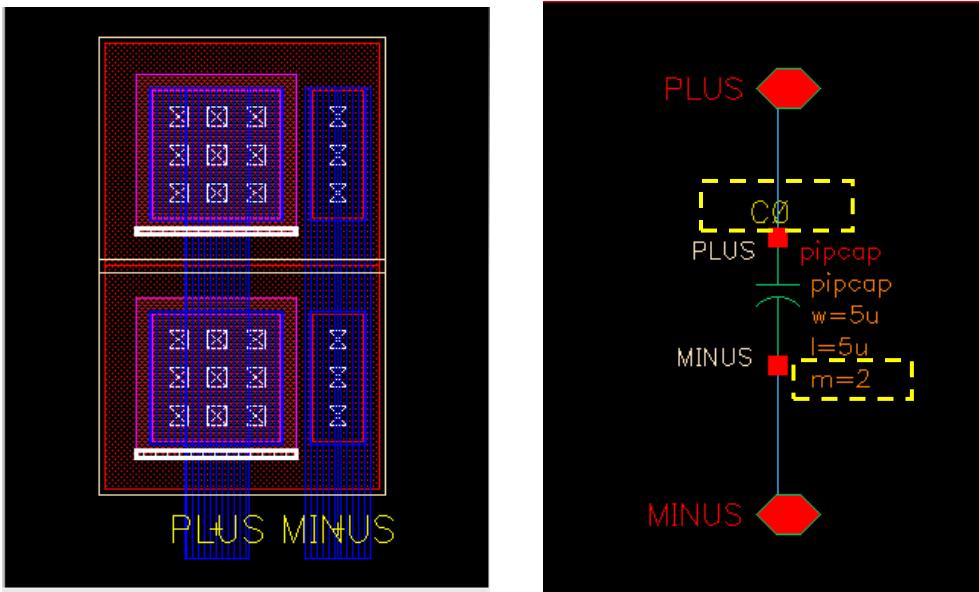


-Adjusted SEALRING_UNIT and SEALRING_CONER

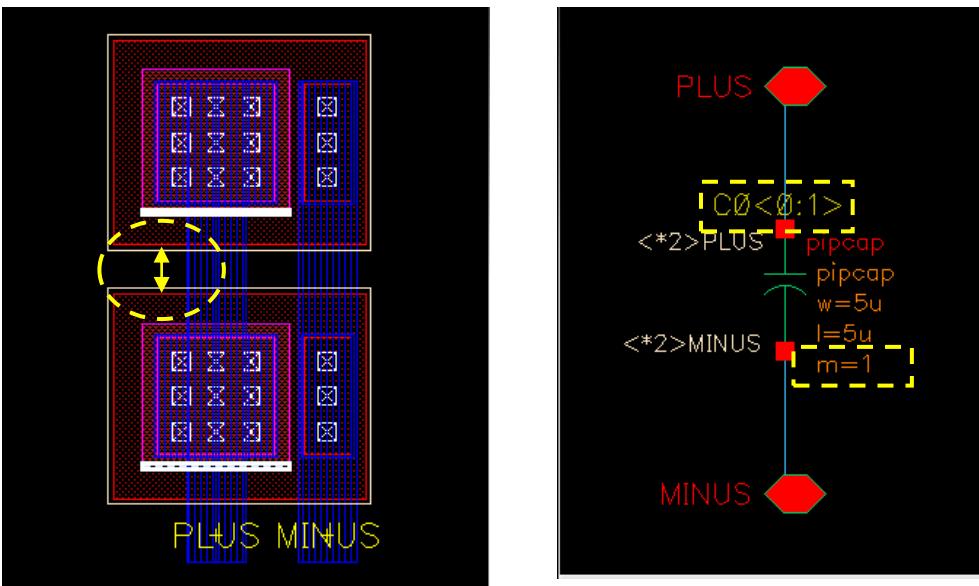
8. LVS Guide

8.1 PIPCAP Layout/Circuit Structure

- Case1 : Merged PIPCAP

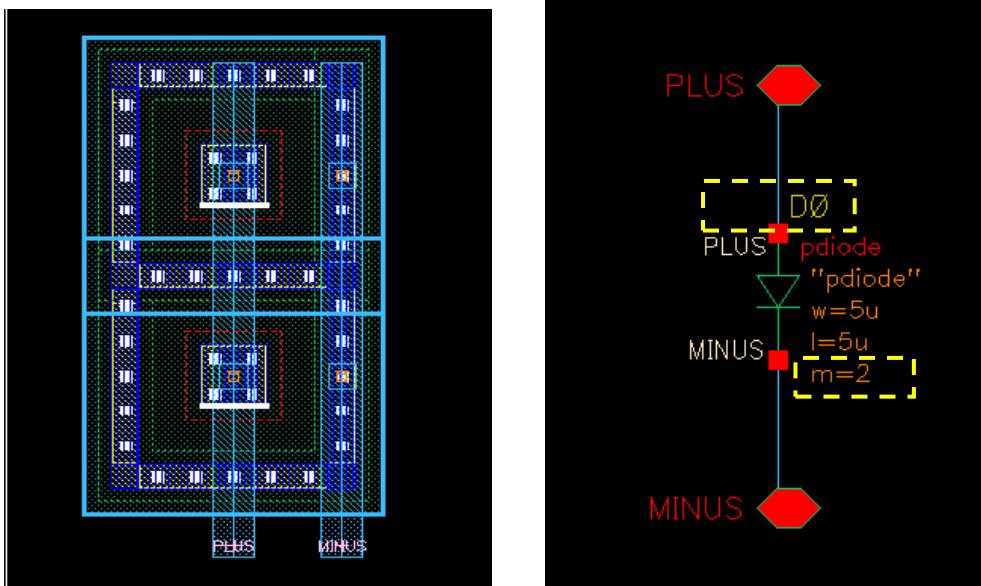


- Case2 : Separated PIPCAP

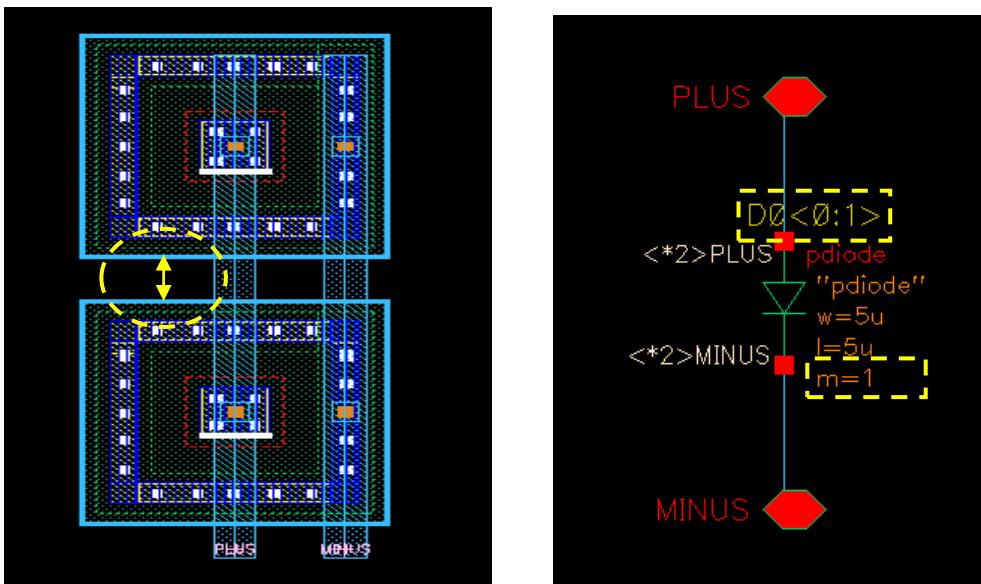


8.2 PDIODE Layout/Circuit Structure

- Case1 : Merged PDIODE

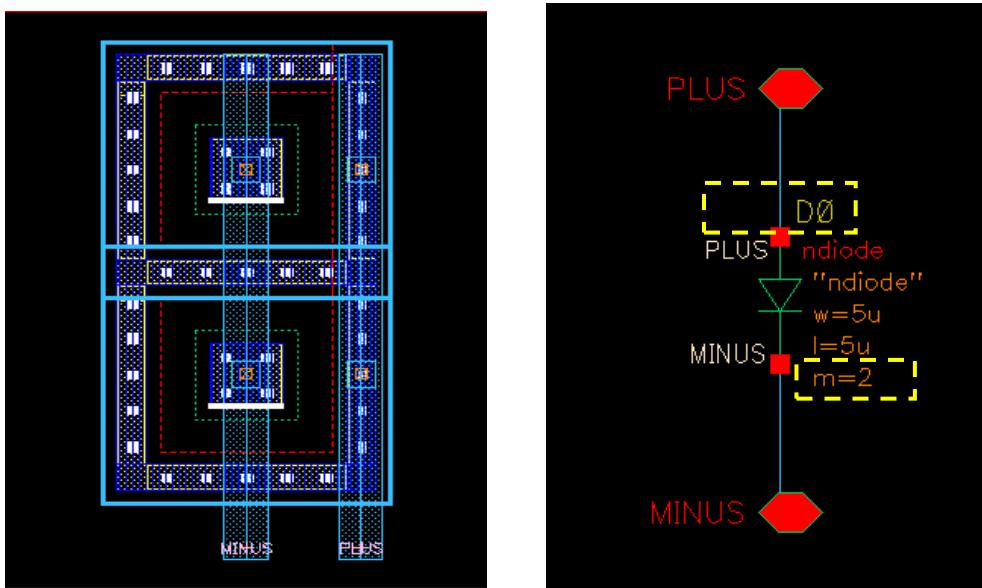


- Case2 : Separated PDIODE

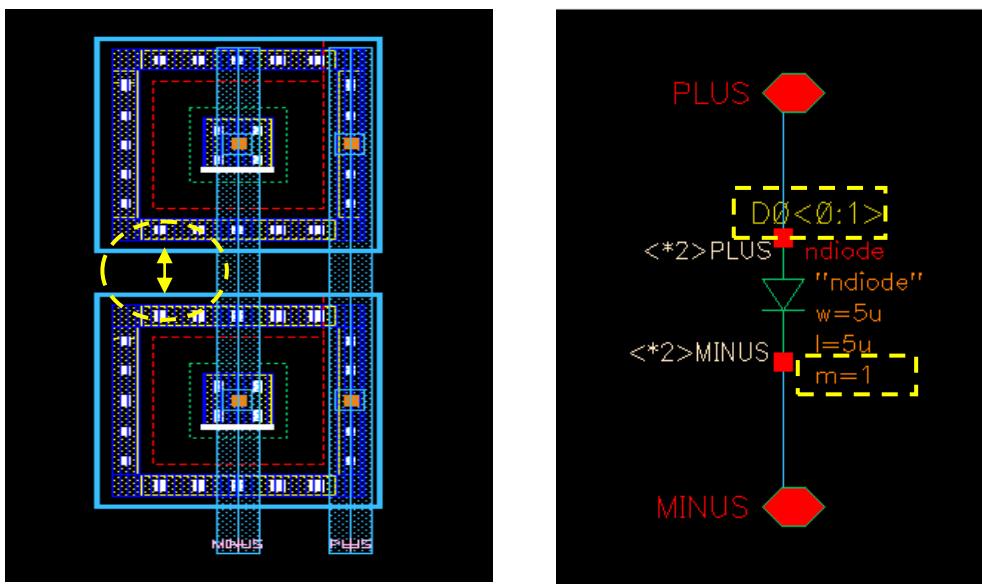


8.3 NDIODE Layout/Circuit Structure

- Case1 : Merged NDIODE



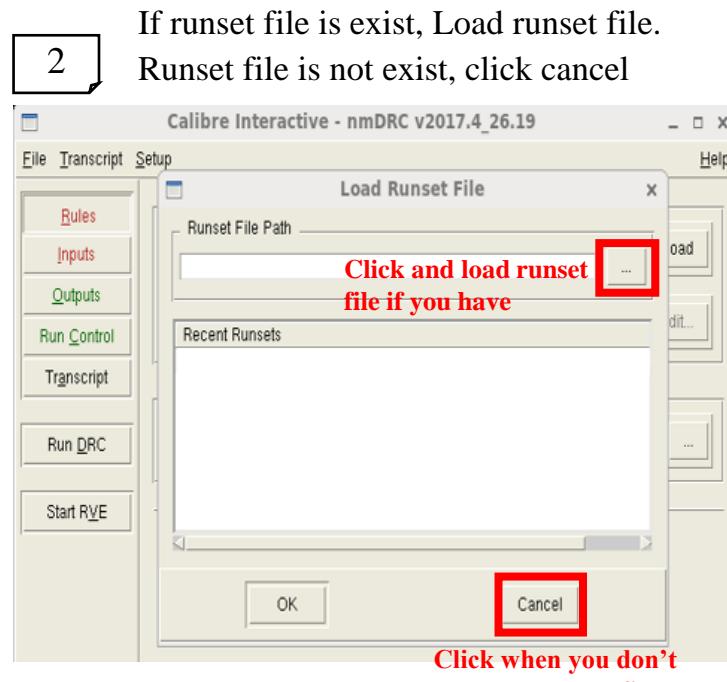
- Case2 : Separated NDIODE



9. Calibre DRC

9.1 Run for DRC at GUI

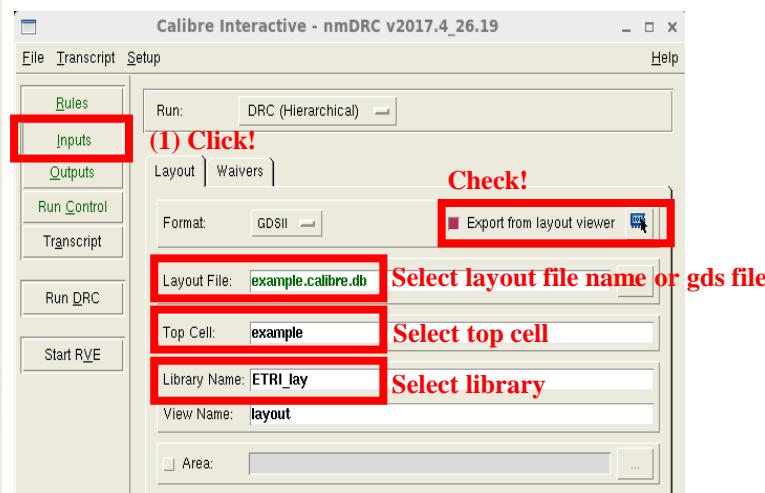
- For running DRC(Design Rule Check) at GUI after layout, need to several steps like below pictures



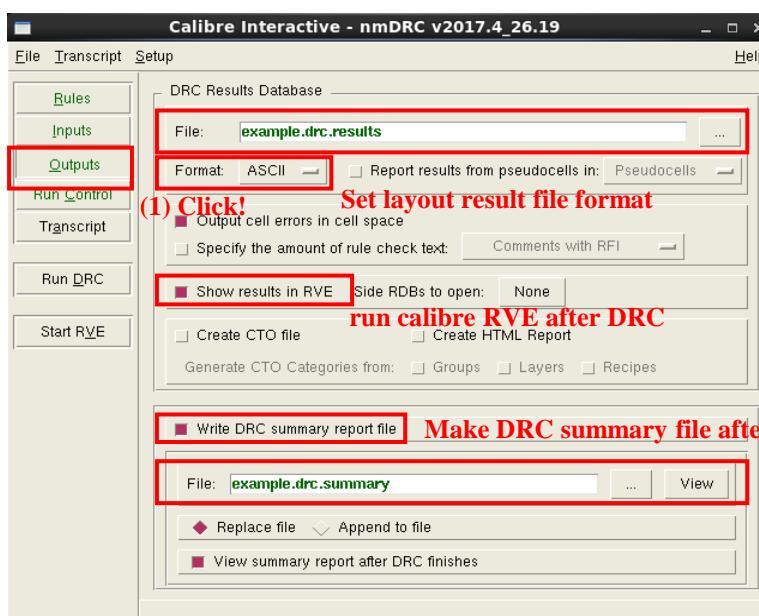
3 Load DRC rules file.



4 Set Input data. If you checked Export from layout viewer, insert layout file name to layout file. Not checked, Input your gds name want to run.

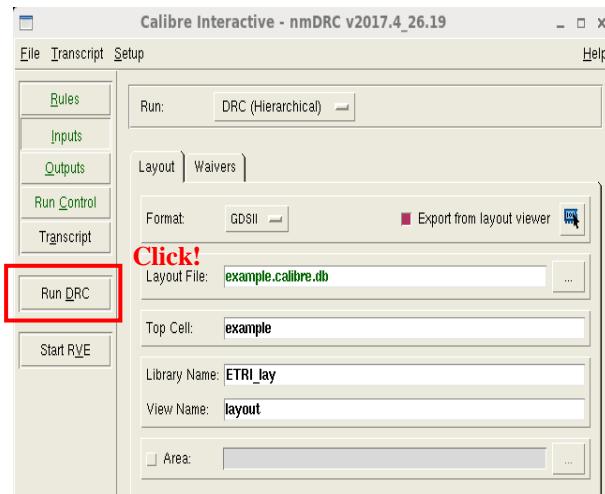


5 Set layout output data



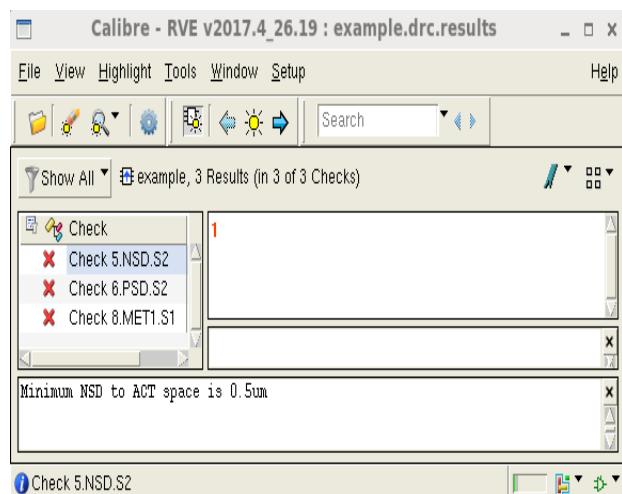
6

Run DRC



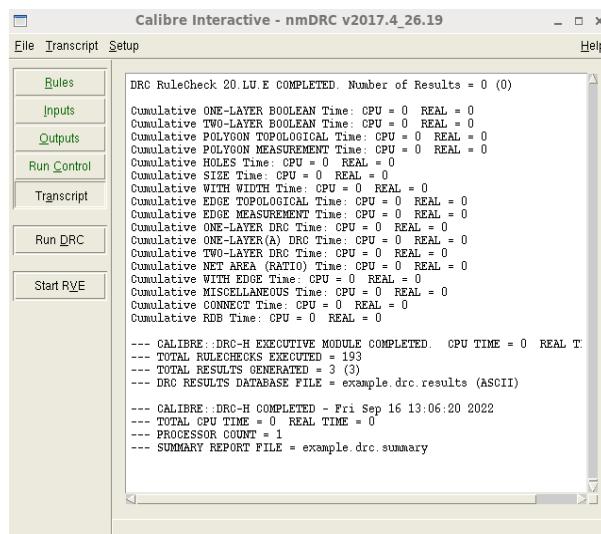
7

Get results (RVE)



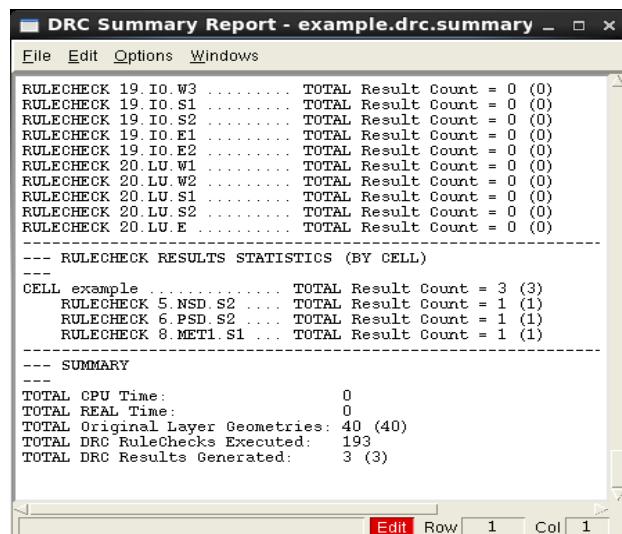
7

Get results (transcript)

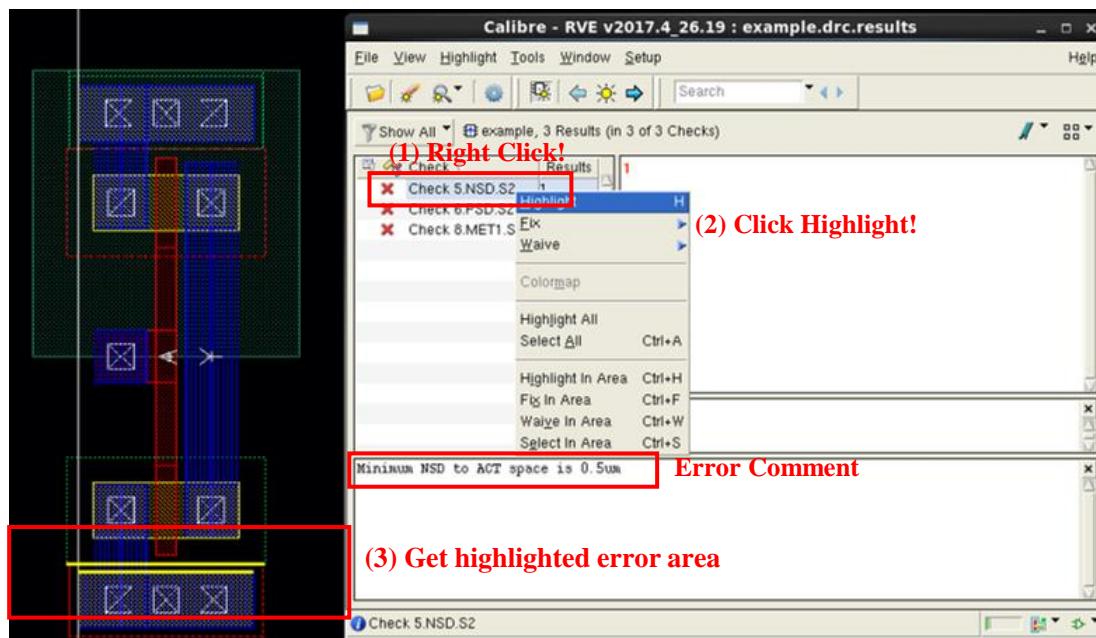


7

Get results (summary)



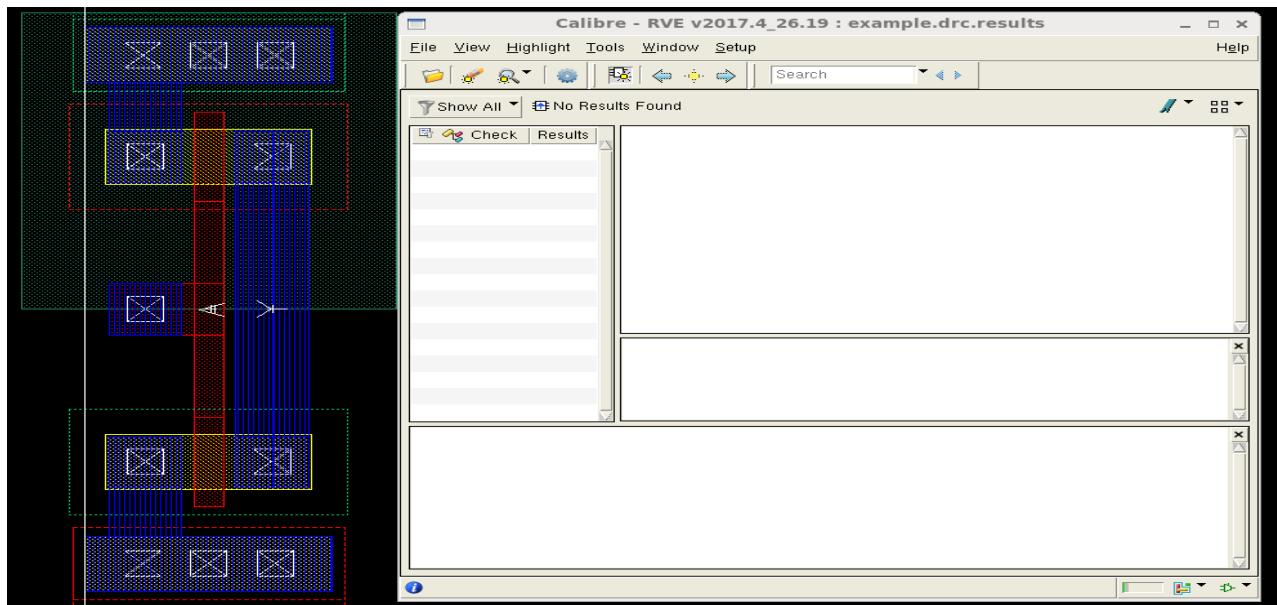
8 Run DRC



- After correct DRC errors, run again DRC.

9

Check Error Results



The screenshot shows the Calibre Interactive interface with the title 'Calibre Interactive - nmDRC v2017.4_26.19'. The menu bar includes File, Transcript, Setup, and Help. The left sidebar has buttons for Rules, Inputs, Outputs, Run Control, and Transcript. The main transcript window displays the following text:

```
Cumulative MISCELLANEOUS Time: CPU = 0 REAL = 0
Cumulative CONNECT Time: CPU = 0 REAL = 0
Cumulative RDB Time: CPU = 0 REAL = 0
--- CALIBRE :: DRC-H EXECUTIVE MODULE COMPLETED. CPU TIME = 0 REAL TIME = 0
--- TOTAL RULECHECKS EXECUTED = 193
--- TOTAL RESULTS GENERATED = 0 (0) Check error count
--- DRC RESULTS DATABASE FILE = example.drc.results (ASCII)
```

The screenshot shows the 'DRC Summary Report - example.drc.summary' window. The menu bar includes File, Edit, Options, and Windows. The report displays the following statistics:

```
--- RULECHECK RESULTS STATISTICS (BY CELL)
--- SUMMARY
--- TOTAL CPU Time: 0
--- TOTAL REAL Time: 0
--- TOTAL Original Layer Geometries: 39 (39)
--- TOTAL DRC RuleChecks Executed: 193
--- TOTAL DRC Results Generated: 0 (0) Check error count
```

At the bottom right, there are buttons for Edit, Row, Col, and a page number indicator (Page 1).

9.2 Script options

- In running DRC, you can use several options for convenience.
if you need, modify this comment in the drc_header.cal

option	value	comment
LAYOUT SYSTEM	GDSII OASIS	Select layout data format GDSII or OASIS
DRC MAXIMUM RESULTS	ALL [Maxresults]	Select maximum result of errors in running drc. Non-negative integer can be Maxresults. Default value is 1000
DRC SELECT CHECK	[rule name] [group name]	Only check selected rules You can add other rules or groups by writing name after values
DRC UNSELECT CHECK	[rule name] [group name]	Running drc except selected rules You can add other rules or groups by writing name after values
EXCLUDE CELL	[cell name]	Select cells not to be processed by drc verification. You can add other cells by writing name after values

- Before run drc, you have to modify script file(drc_header.cal) some parts below.

LAYOUT PATH “[gds_path]/[CELLNAME.gds]”

gds_path : the directory where layout gds file is exist

CELLNAME.gds : put in your gds file

LAYOUT PRIMARY “[CELLPRIMARY]”

Layout database topcell for running drc.

LAYOUT SYSTEM [GDSII or OASIS]

You can choose layout data type GDSII or OASIS

INCLUDE “[rule_path]/ETRI_0p5um_Analog_CMOS_2P3M_5V_DRC.cal”
path that rule file is exist.

- If you want to run drc in terminal, you can use command described below.

- Example drc_header.cal

```
LAYOUT PATH "temp.gds"      Layout gds file name for DRC
LAYOUT PRIMARY "temp"        Layout primary cell name
LAYOUT SYSTEM GDSII          Select layout system GDSII or OASIS
DRC RESULTS DATABASE "TOPCELL.db" ASCII Set DRC result file name
DRC MAXIMUM RESULTS ALL    Set DRC maximum error counts
DRC SUMMARY REPORT "TOPCELL.rep" Set DRC summary report name
//DRC SELECT CHECK rulename or groupname Choose rules or groups want to check
//DRC UNSELECT CHECK rulename or groupname Except rules or groups want to check
//Groups -> 1.NWL, 2.ACT, 3.PL1, 4.PL2, 5.NSD, 6.PSD, 7.CONT, 8.MET1, 9.VIA1, 10.MET2,
11.VIA2, 12.MET3, 13.PAD, 14.PLN2R, 15.CAP, 16.PNP, 17.NPN, 19.IO, 20.LU List of groups
//EXCLUDE CELL cellName1 cellName2 Set exclude cells in DRC
Remove "//" before using these options

INCLUDE "/PROJECT DIRECTORY/ETRI/DRC/ETRI_0p5um_Analog_CMOS_2P3M_5V_DRC.cal"
|                                         DRC rule path
```

- If you want to run drc in terminal, you can use command described below.

Command: calibre –drc –hier drc_header.cal

- If you want to see results at RVE in terminal, you can use command described below.

Command: calibre –rve –drc [DRC RESULTS DATABASE]

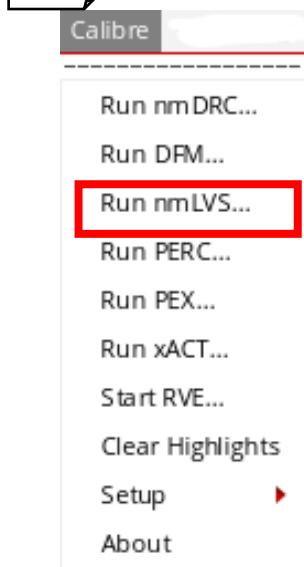
ex) calibre –rve –drc TOPCELL.db

10. Calibre LVS

10.1 Run for LVS at GUI

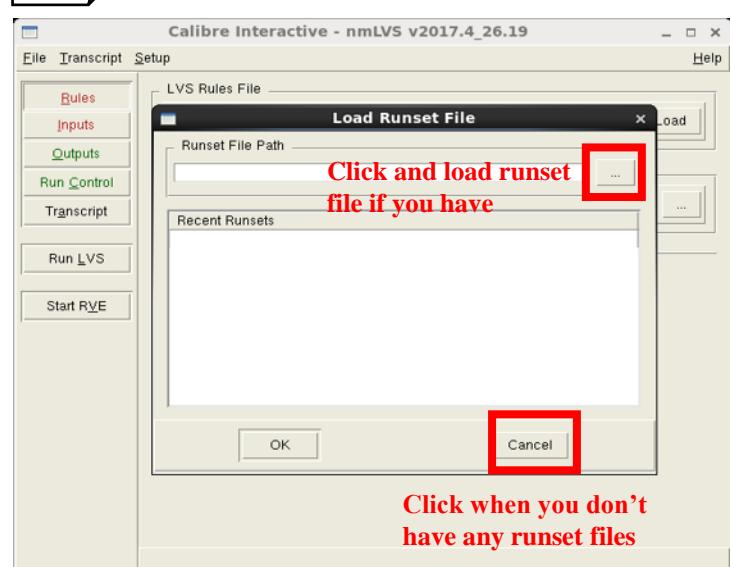
- For running LVS(Layout VS Schematic) at GUI after layout, need to several steps like below pictures

1 Click Run nmLVS in Calibre menu



Click

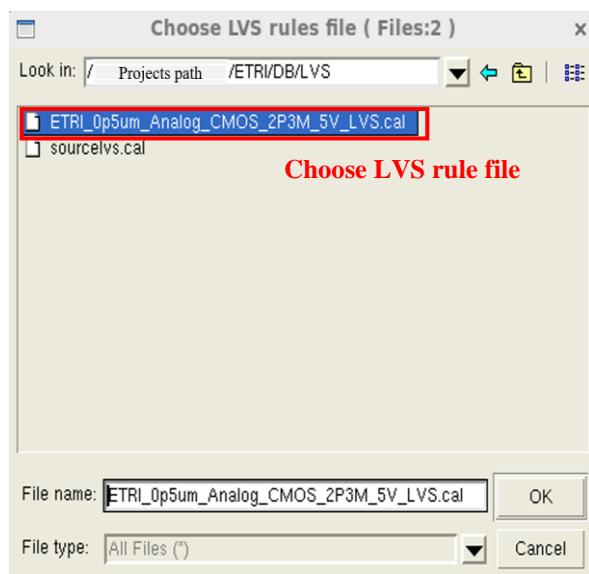
If runset file is exist, Load runset file.
Runset file is not exist, click cancel



3 Load LVS rules file (ETRI_0p5um_Analog_CMOS_2P3M_5V_LVS.cal)

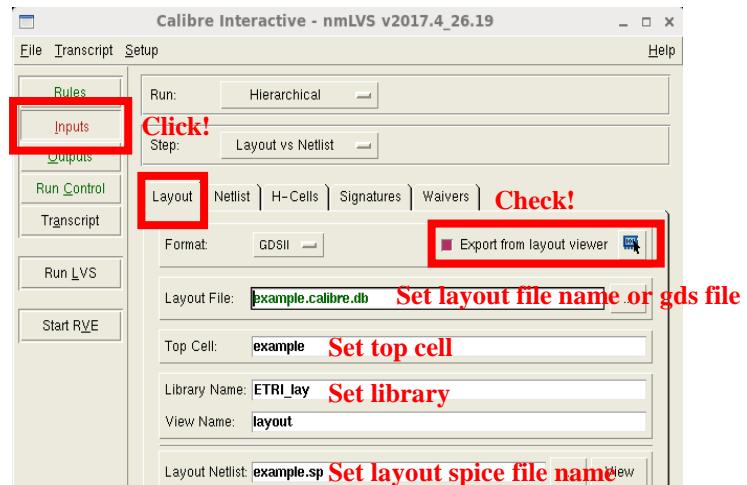


3 Load LVS rules file.



Set layout Input data. If you checked Export from layout viewer, insert layout file name to layout file. Not checked, Input your gds name want to run.

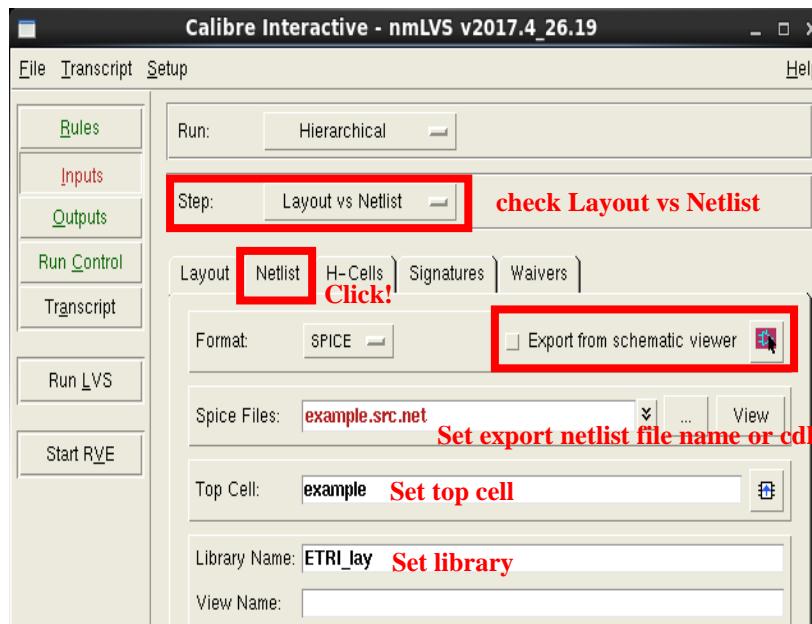
4



Set schematic Input data. If you checked Export from schematic viewer, insert layout file name to Spice files.

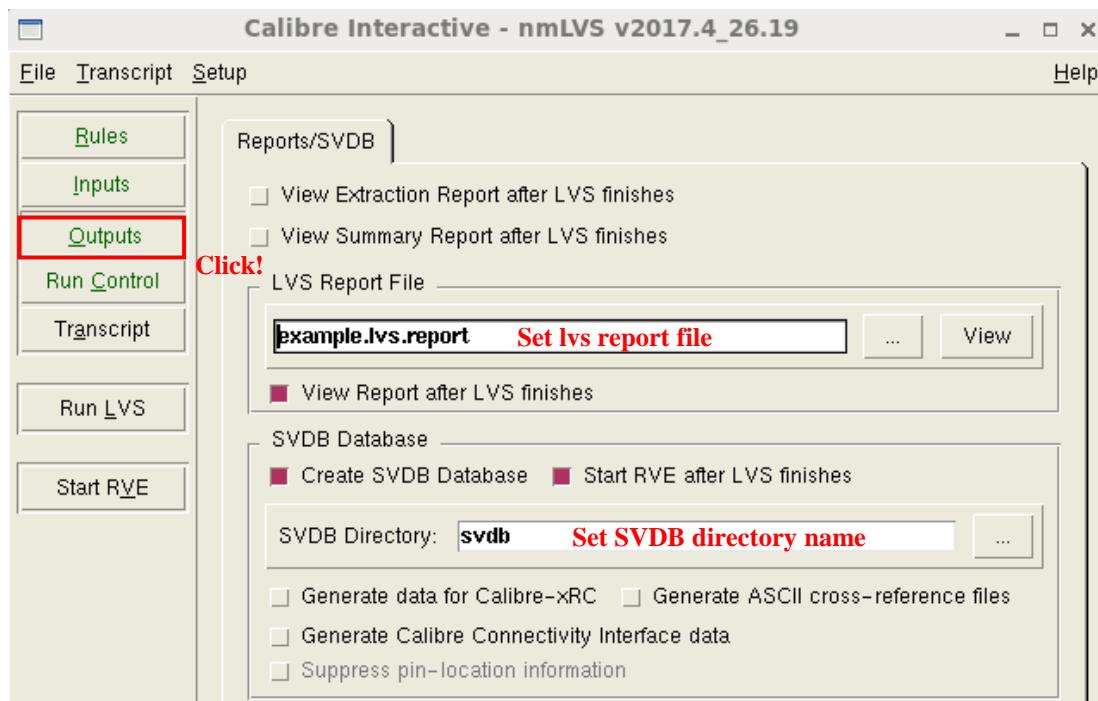
4

Not checked, Input your netlist name want to run.

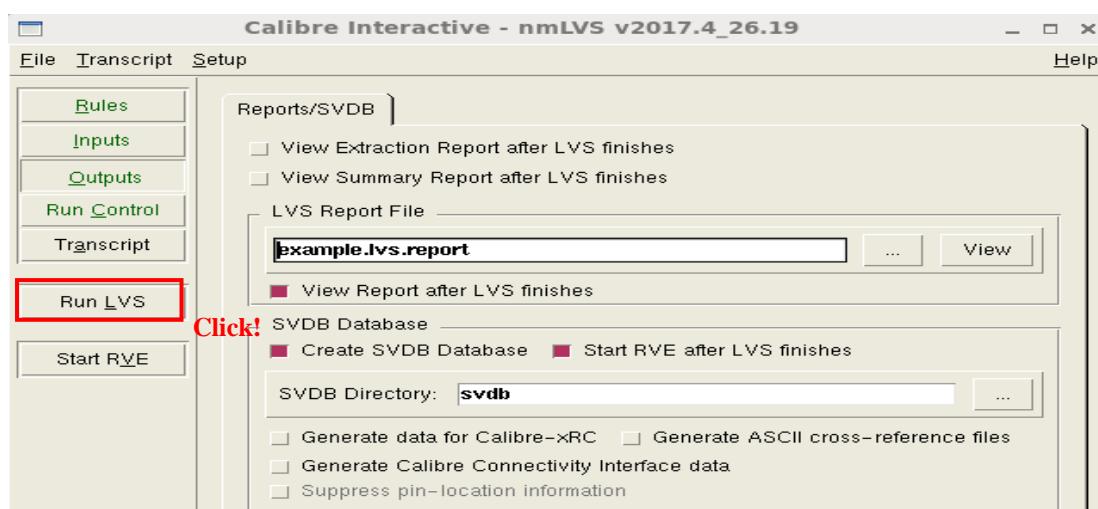


Check!

5 Set LVS outputs

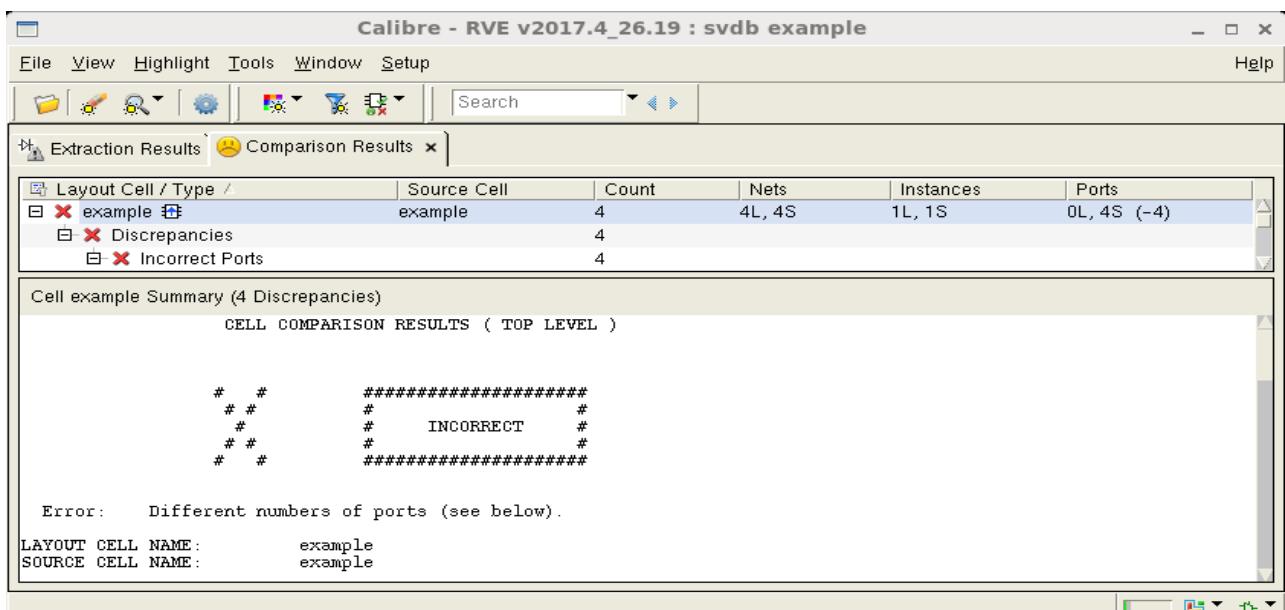


6 Run LVS



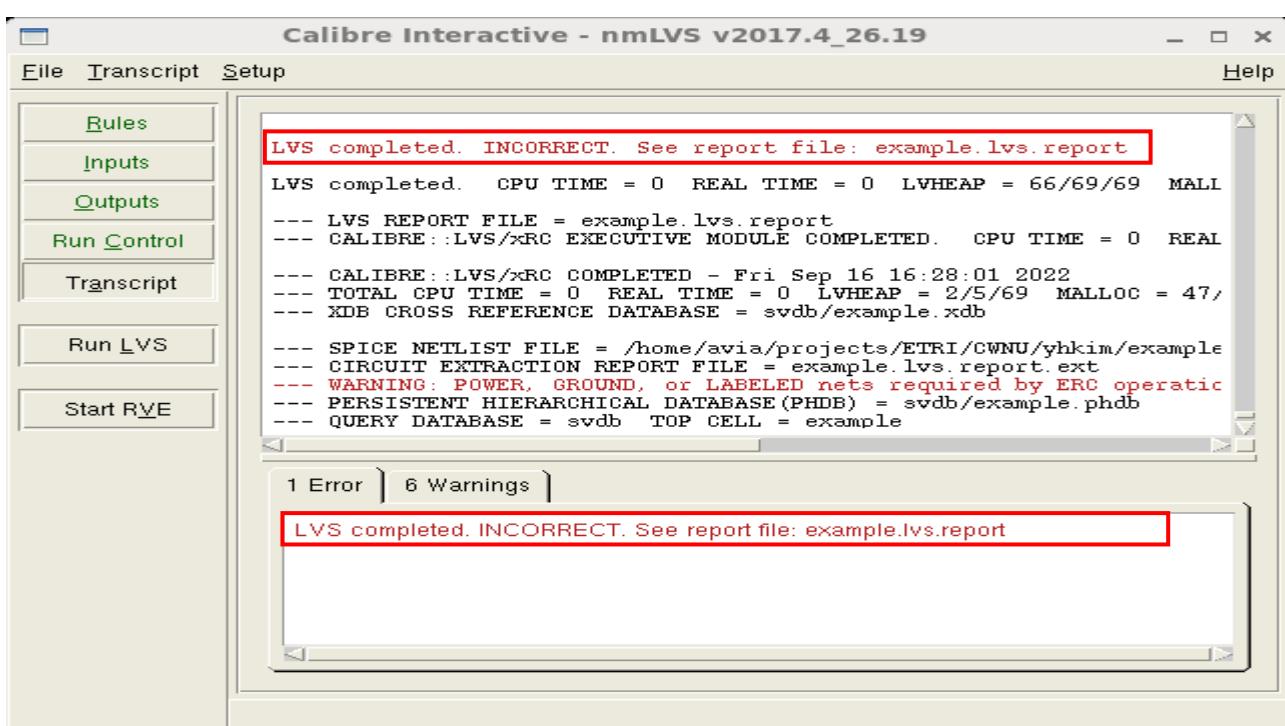
7

Get results(RVE)



7

Get results(Transcript)



7 Get results(report)

LVS Report File - example.lvs.report

File Edit Options Windows

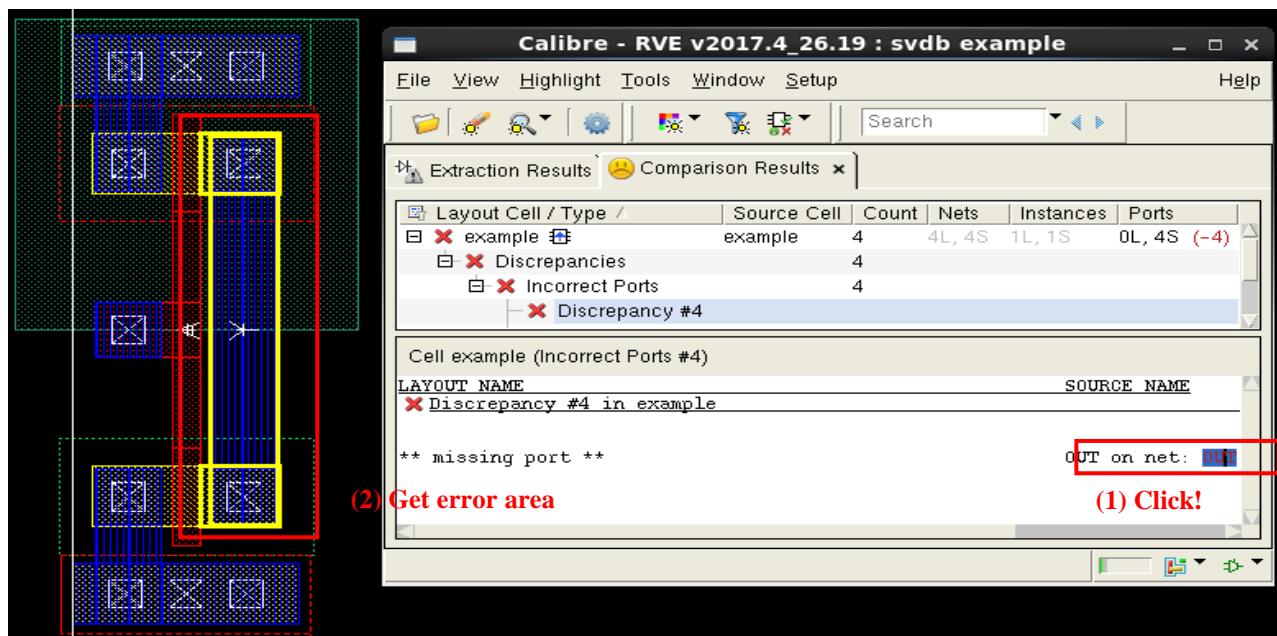
LEGEND:

ne = Naming Error (same layout name found in source circuit, but object was matched otherwise).

***** INCORRECT PORTS *****

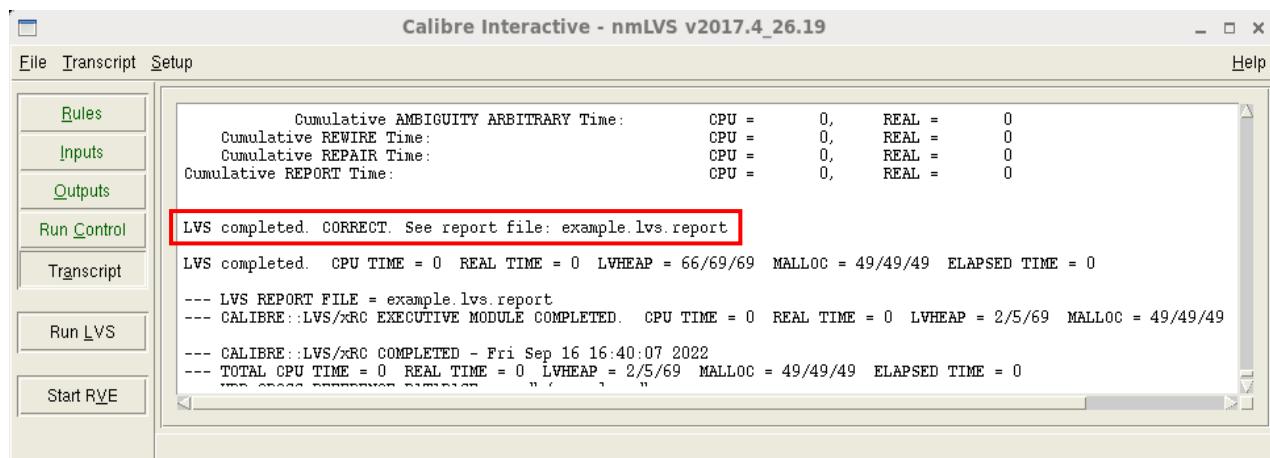
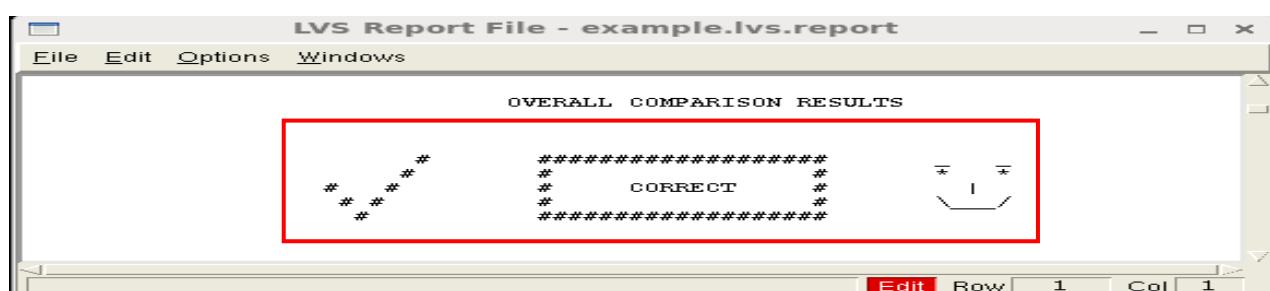
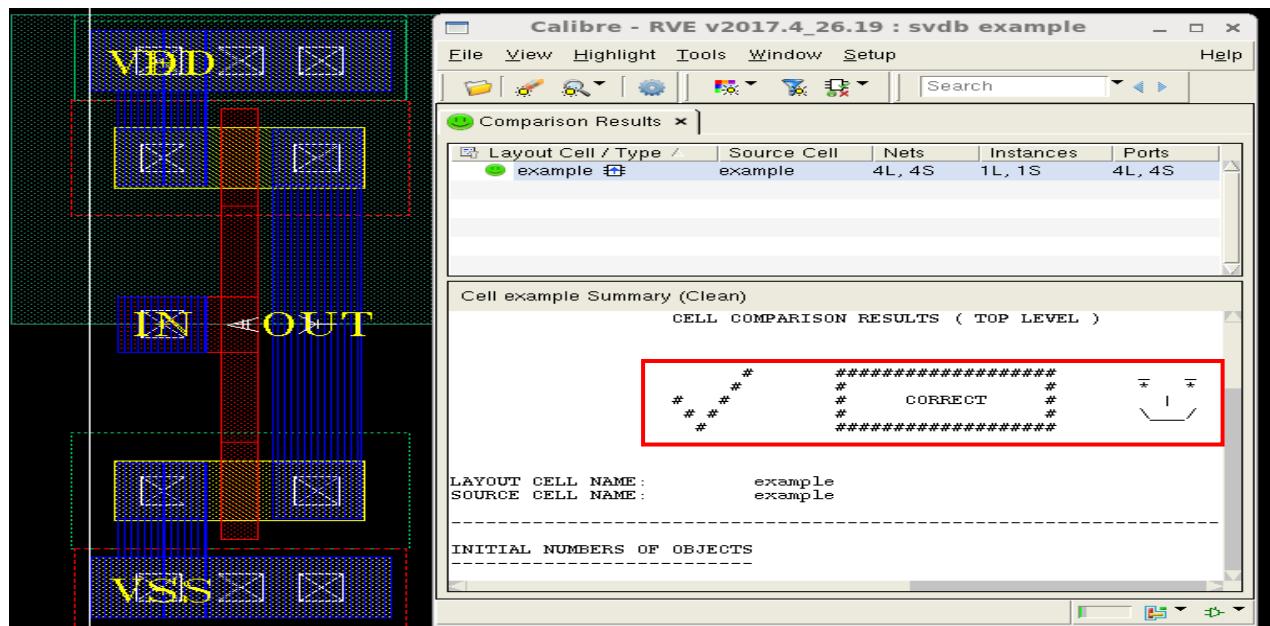
DISC#	AYOUT NAME	SOURCE NAME
1	** missing port **	VDD on net: VDD
2	** missing port **	VSS on net: VSS
3	** missing port **	IN on net: IN
4	** missing port **	OUT on net: OUT

8 Run lvs



- After correct LVS errors, run again LVS.

9 Check error results



10.2 Script options

- In running LVS, you can use several options for convenience.
if you need, modify this comment in the lvs_header.cal.
- Before run lvs, you have to modify script file(lvs_header.cal) some parts below.

LAYOUT PATH “[gds_path]/[CELLNAME.gds]”

gds_path : the directory where layout gds file is existed.

CELLNAME.gds : put in your gds file

LAYOUT PRIMARY “[CELLPRIMARY]”

Layout database topcell for running lvs.

LAYOUT SYSTEM [GDSII or OASIS]

You can choose layout data type GDSII or OASIS

SOURCE PATH “[cdl_path]/[CELLNAME.cdl]”

cdl_path : the directory where schematic cdl file is exist

CELLNAME.cdl : put in your cdl file

SOURCE PRIMARY “[CELLPRIMARY]”

Schematic database topcell for running lvs.

SOURCE SYSTEM SPICE

ERC RESULTS DATABASE “[ERC_DB]” ASCII

Set ERC DB name and format

ERC SUMMARY REPORT “[ERCSUMMARY]”

Set ERC summary report name

ERC MAXIMUM RESULTS 100

Set ERC maximum error counts

INCLUDE “[rule_path]/ETRI_0p5um_Analog_CMOS_2P3M_5V_LVS.cal”
path that rule file is exist.

- Example lvs_header.cal

```
LAYOUT PRIMARY "test" Layout primary cell name
LAYOUT PATH "test.gds" Layout gds file name for LVS
LAYOUT SYSTEM GDSII Select layout system GDSII or OASIS

SOURCE PRIMARY "test" Schematic primary cell name
SOURCE PATH "test.cdl" Schematic cdl file name for LVS
SOURCE SYSTEM SPICE Select source system SPICE

DRC RESULTS DATABASE "drc.db" ASCII // ASCII or GDSII Set DRC result file name
DRC SUMMARY REPORT "drc.sum" Set DRC summary report name

LVS REPORT "lvs.rep" List of groups
LVS REPORT MAXIMUM 1000 // ALL Set LVS maximum error counts
LVS REPORT OPTION A B C D S V Set LVS report option

ERC RESULTS DATABASE "erc.db" ASCII Set ERC result file name
ERC SUMMARY REPORT "erc.sum" Set ERC summary report name
ERC MAXIMUM RESULTS 100 Set ERC maximum error counts

INCLUDE "/ Project Directory /ETRI/LVS/ETRI_0p5um_Analog_CMOS_2P3M_5V_LVS.cal"
Include LVS rule path
```

- If you want to run lvs in terminal, you can use command described below.

Command: calibre –lvs –hier lvs_header.cal

- If you want to see results at RVE in terminal, you can use command described below.

Command: calibre –rve –lvs [SVDB directory]

ex) calibre –rve –lvs svdb

※ LVS virtual connection option is set Yes. If you don't want virtual connect,
Please set “VIRTUAL CONNECT COLON” to “NO” in LVS rule file.

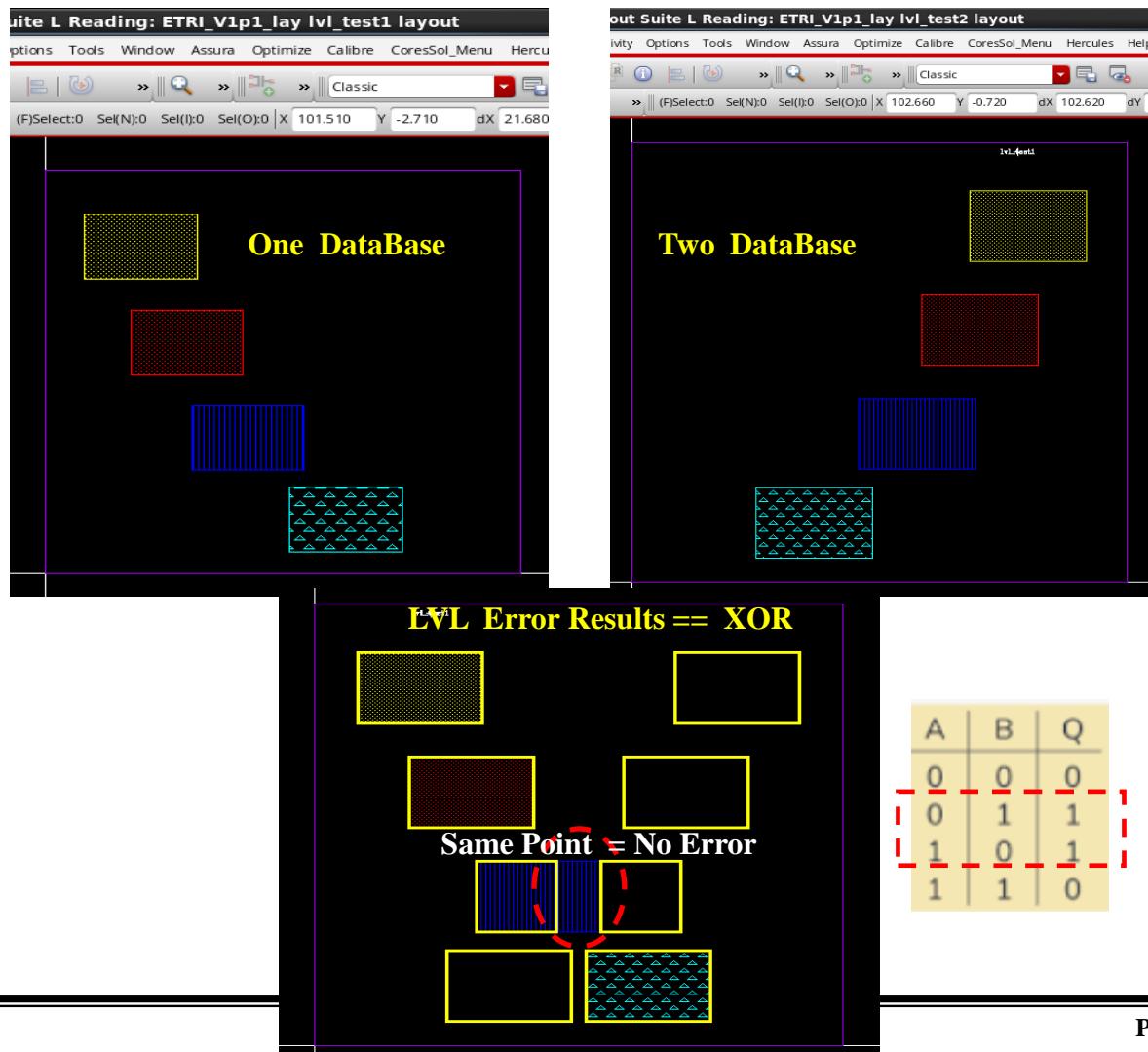
※ LVS REDUCE PARALLEL/SERIES CAPACITORS
option is set NO in LVS rule file.
please do not change this option for exact LVS verification.

FILE NAME: ETRI_0p5um_Analog_CMOS_2P3M_5V_LVS.cal

11. Calibre LVL

11.1 LVL (Layout Versus Layout) Verification

- Distributes of the two input data that are not equal to each other as errors.
- Calibre has the Capability to compare two separate Layout Database
- When comparing two layout database :
 - * Specify One of the Database Using
 - LAYOUT SYSTEM
 - LAYOUT PATH
 - LAYOUT PRIMARY
 - * Specify the other Database Using
 - LAYOUT SYSTEM2
 - LAYOUT PATH2
 - LAYOUT PRIMARY2



11.2 Script Option

- In running LVL, you can use several options for convenience.
if you need, modify this comment in the lvl_header.cal

option	value	comment
LAYOUT SYSTEM	GDSII OASIS	1 st Input : Select layout data format GDSII or OASIS
LAYOUT SYSTEM2	GDSII OASIS	2 nd Input : Select layout data format GDSII or OASIS
LAYOUT BUMP2	Number > 1 st DB	Increments 2 nd Layout Data Base Layer Number by Specified Value
DRC RESULTS DATABASE	<i>Filename[type]</i>	Specifies the filename and type of the results database
DRC SUMMARY REPORT	<i>Filename</i>	Specifies the DRC Summary report File

- Before run lvl, you have to modify script file(lvl_header.cal) some parts below.

LAYOUT PATH “[gds_path]/[CELLNAME.gds]“

gds_path : the directory where layout 1st gds file is exist

CELLNAME.gds : put in your gds file

LAYOUT PRIMARY “[CELLPRIMARY]“

Layout database 1st topcell for running drc.

LAYOUT PATH2 “[gds_path]/[CELLNAME.gds]“

gds_path : the directory where layout 2nd gds file is exist

CELLNAME.gds : put in your gds file

LAYOUT PRIMARY2 “[CELLPRIMARY]“

Layout database 2nd topcell for running drc

INCLUDE “[rule_path]/ETRI_0p5um_Analog_CMOS_2P3M_5V_LVL.cal “

path that rule file is exist.

- If you want to run lvl in terminal, you can use command described below.

11.2 Script Option

- Example lvl_header.cal

LAYOUT SYSTEM GDSII	1 st : Select layout system GDSII or OASIS
LAYOUT PATH "lvl_test1.gds"	1 st : Layout gds file name for LVL
LAYOUT PRIMARY "lvl_test1"	1 st : Layout primary cell name
LAYOUT SYSTEM2 GDSII	2 nd : Select layout system GDSII or OASIS
LAYOUT PATH2 "lvl_test2.gds"	2 nd : Layout gds file name for LVL
LAYOUT PRIMARY2 "lvl_test2"	2 nd : Layout primary cell name
LAYOUT BUMP2 2500	Set Number of 2 nd GDS Number
DRC RESULTS DATABASE "lvl.db" ASCII	Set LVL result file name
DRC SUMMARY REPORT "lvl.sum"	Set LVL summary report name
INCLUDE "./ETRI_0p5um_Analog_CMOS_2P3M_5V_LVL.cal"	LVL rule path

- If you want to run drc in terminal, you can use command described below.

Command: `calibre -drc -hier lvl_header.cal`

- If you want to see results at RVE in terminal, you can use command described below.

Command: `calibre -rve -drc [DRC RESULTS DATABASE]`

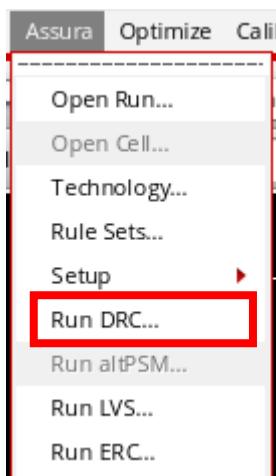
ex) `calibre -rve -drc TOPCELL.db`

12. Assura DRC

12.1 Run for DRC at GUI

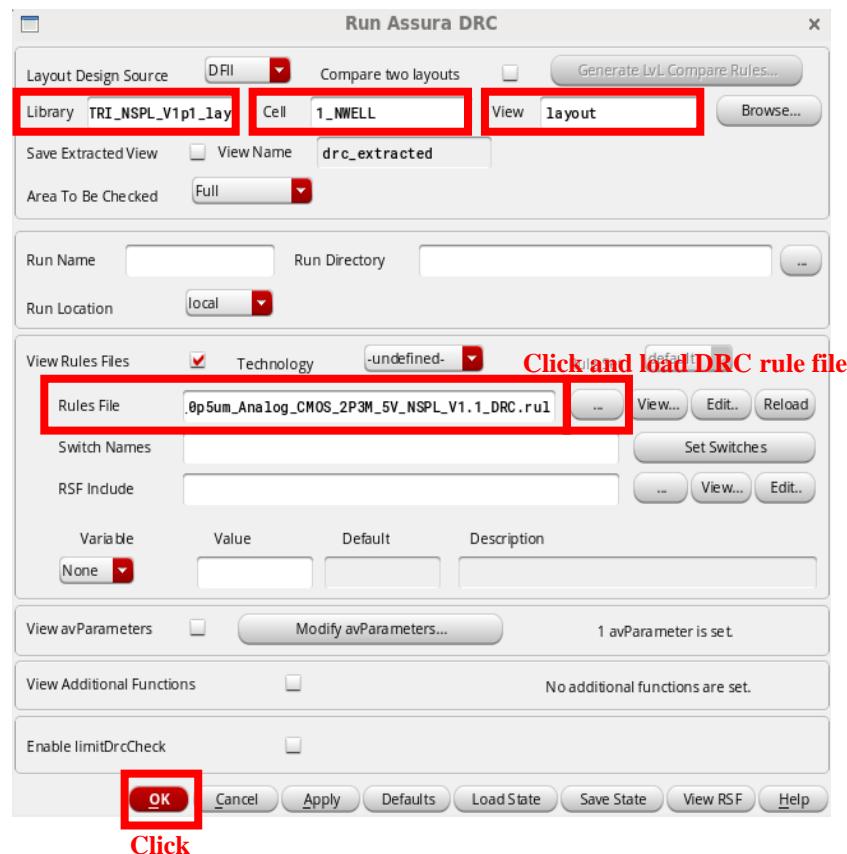
- For running DRC(Design Rule Check) at GUI after layout, need to several steps like below pictures

1 Click Run DRC in Assura menu.



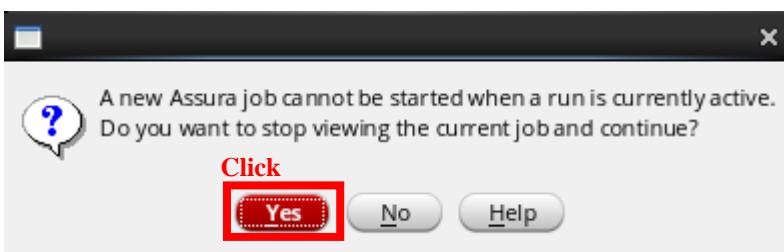
Click

In the Run Assura DRC window, type Library, Cell, View, Rules File and click OK at the bottom.



Click

3 When this phrase comes up, press yes.



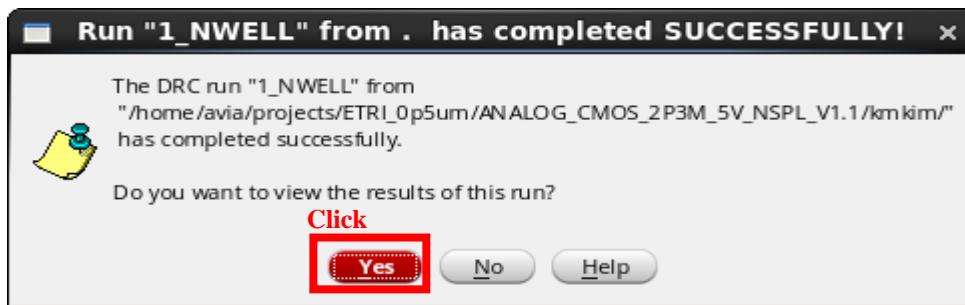
Click

Yes

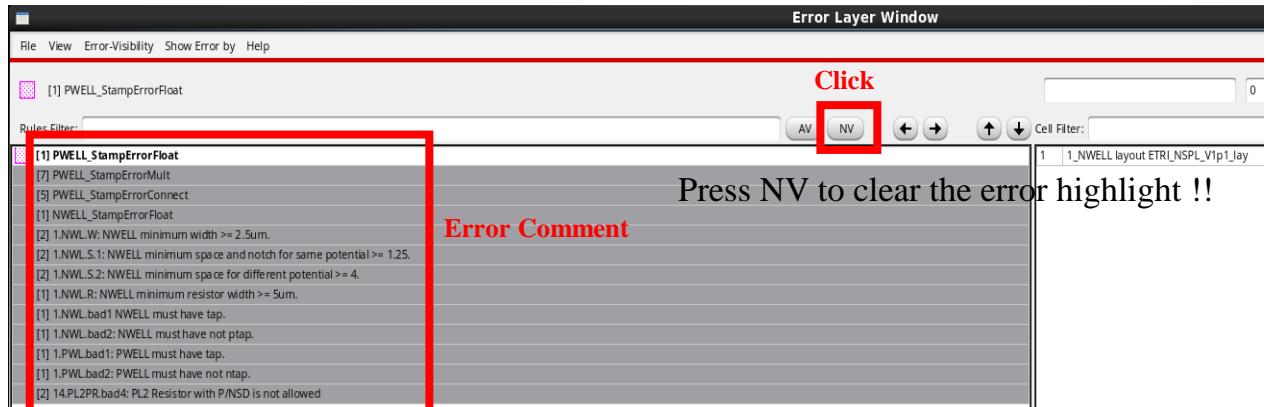
No

Help

- 4 When this phrase comes up, press yes.



- 5 When the error layer window appears, press NV to select nothing.

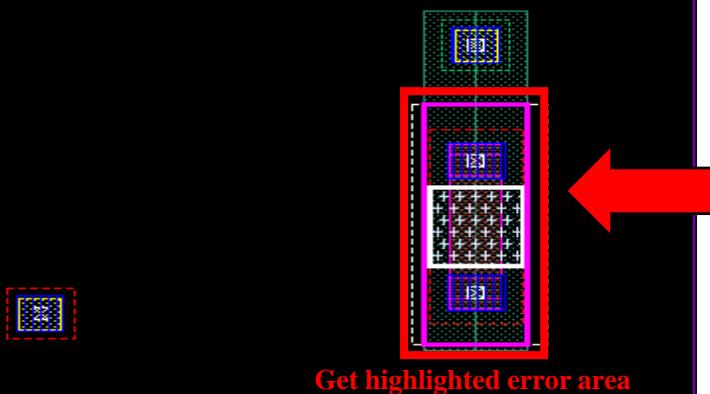


- 6 If you click on the error item and zoom in and out of the mouse on LAYOUT, you will see the error highlight.



- 6 If you click on the error item and zoom in and out of the mouse on Layout, you will see the error highlight.

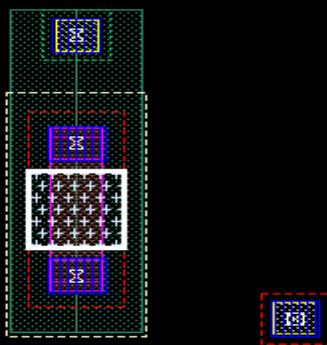
1_NWL_R_FAIL



ERROR highlights are seen in the FAIL pattern.

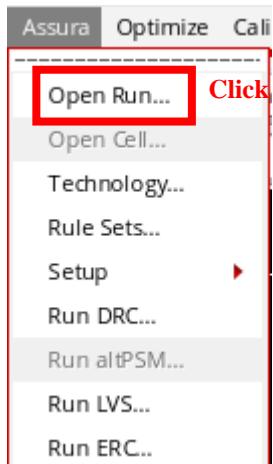
1_NWL_R_PASS

* Minimum NWELL resistor width is 5um



ERROR highlights are not identified in the PASS pattern.

- 7 If you press open run, the most recent DRC-verified cell data remains. However, it does not apply to the layout modifications. (If the layout is modified, it should be verified as run drc.)



- 8 When this phrase comes up, press yes.



- 9 If you proceed with number 8, you can see the error layer window.

Click

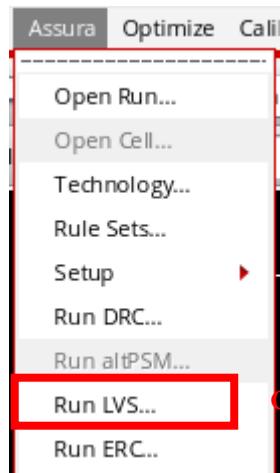


13. Assura LVS

13.1 Run for LVS at GUI

- For running LVS(Layout VS Schematic) at GUI after layout, need to several steps like below pictures

1 Click Run LVS in Assura menu.



2 When the Run Assura LVS window opens, fill in Library, Cell, View, Extract rules, Compare rules and click OK at the bottom.

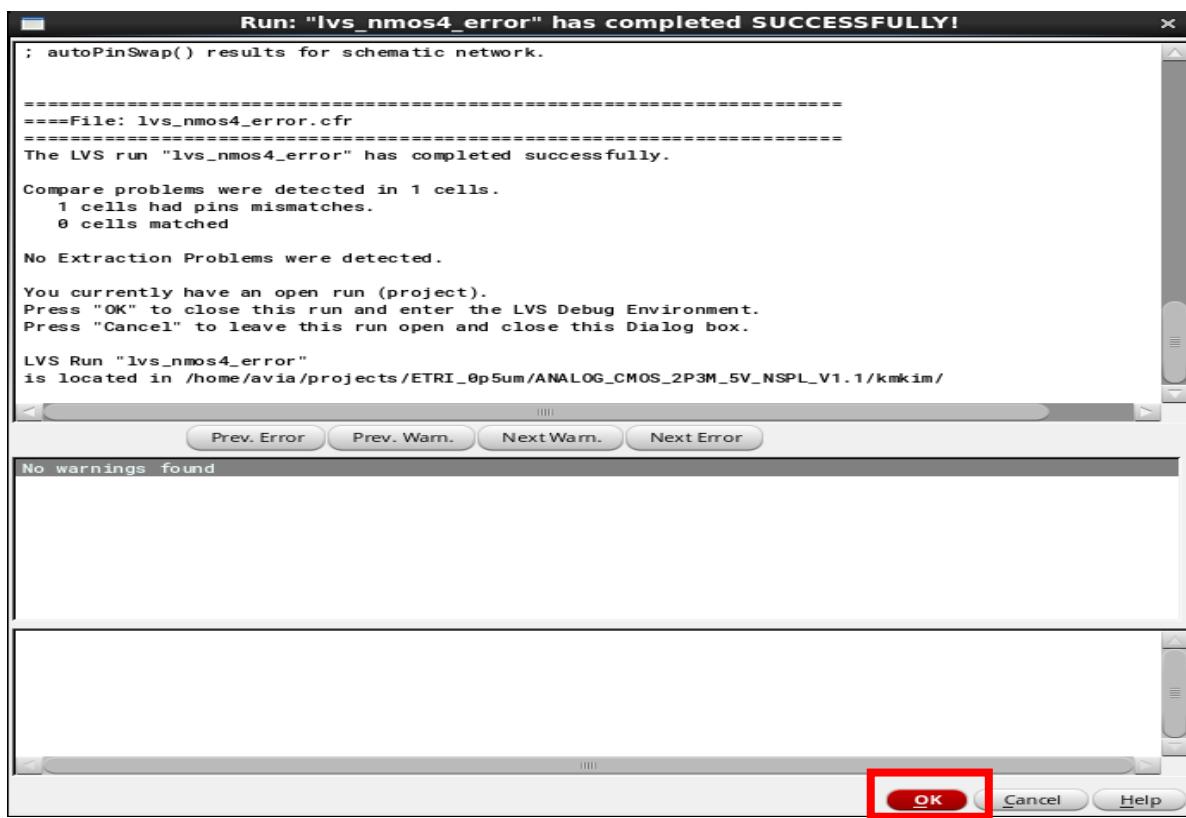


Click and load Extract rule file

Click and load Compare rule file

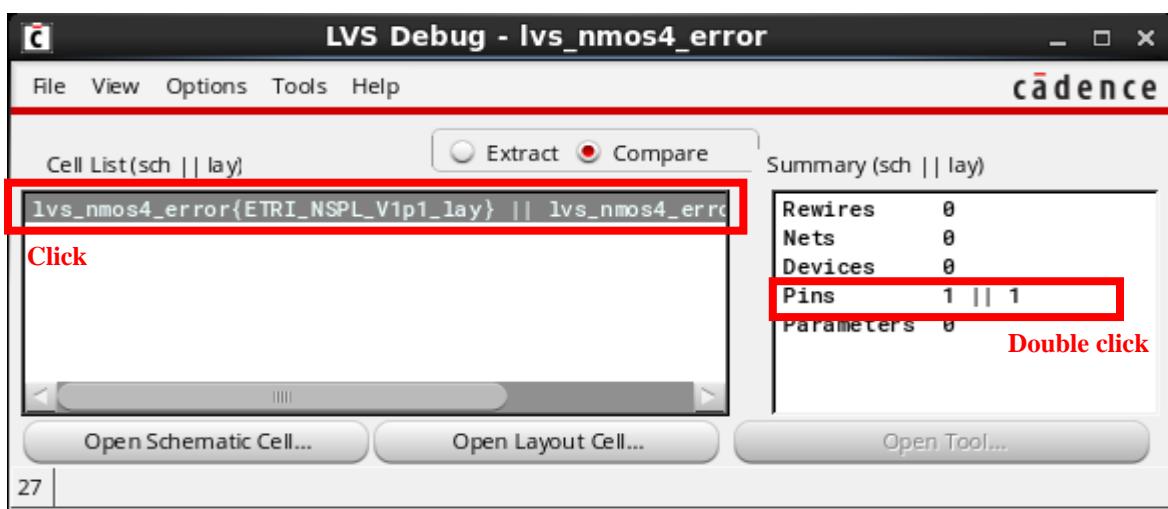
Click

- 3 When this phrase comes up, press yes.



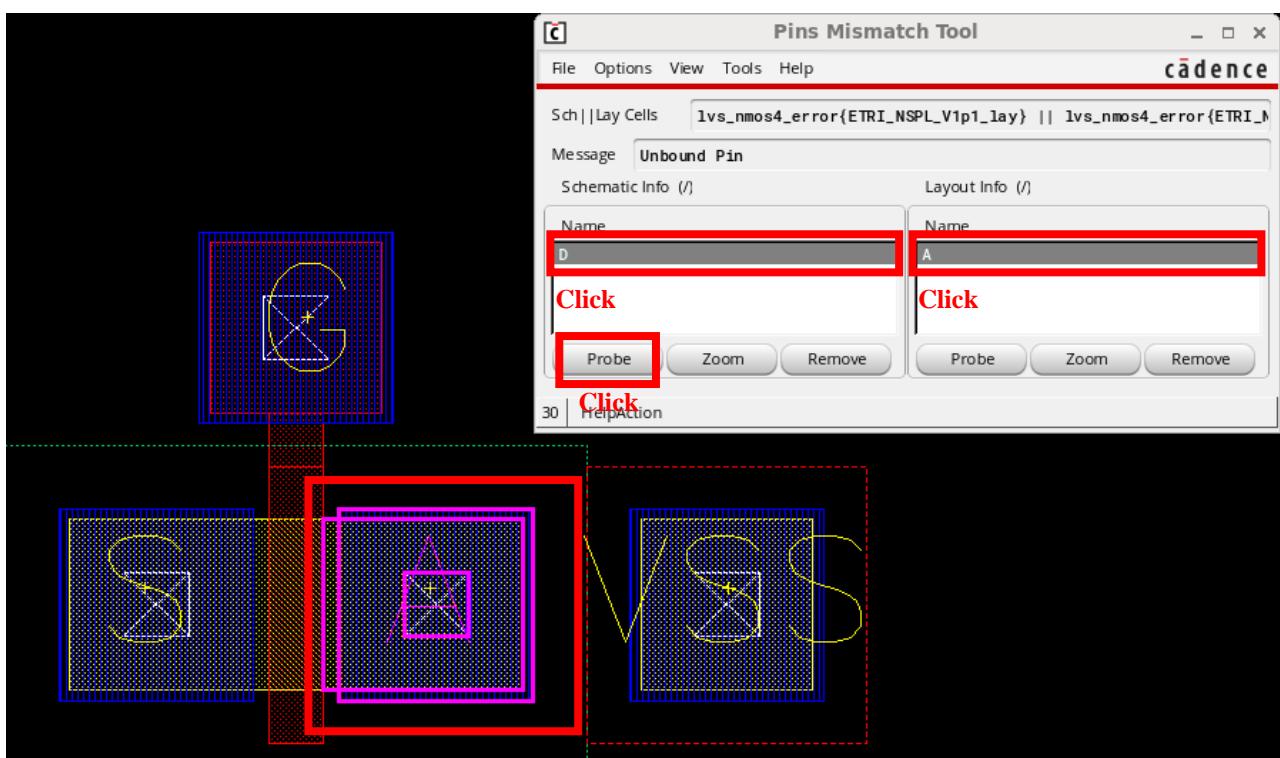
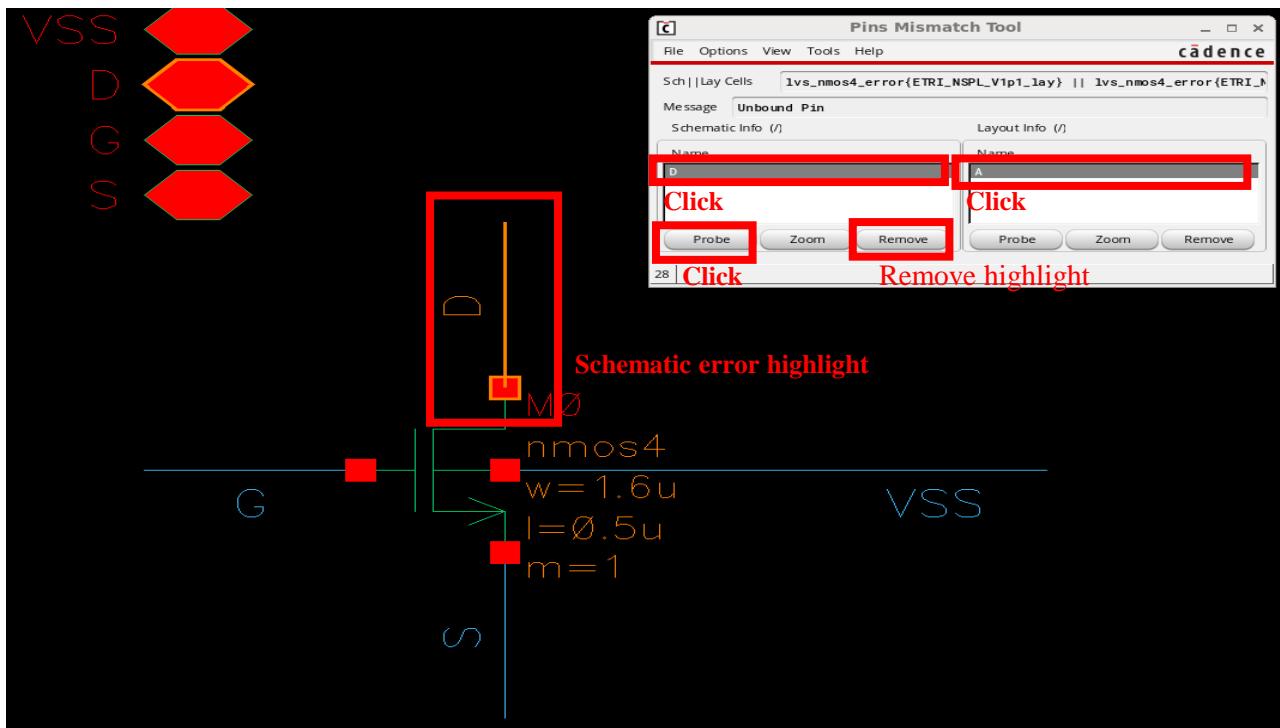
Click

- 4 Get error results



5

If you click the part where the layout and schematic do not match, the part that does not match will be highlighted.



6

If the Layout and Schematic match, the LVS pass window comes out.

