Design and Development of RF CMOS MEMS Switches for Configurable RF Circuits

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Dedication

To my parents,

Bin Zhang and Xiying Wang

To my wife,

Weihong Zhao

Without their patience, understanding, support, and most of all love, the completion of this work would not have been possible.

Acknowledgment

I would like to gratefully acknowledge all those people who have helped me to complete this dissertation. The journey to get a Ph.D was not easy, however, without all these wonderful people and their support, it would be impossible.

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Abstract

Design and Development of RF CMOS MEMS Switches for
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Radio Frequency Micro-Electro-Mechanical System (RF MEMS) switches have been used extensively in configurable circuits, antennas, and other RF applications. The work reported in this dissertation illustrates a novel RF MEMS capacitive switch design that is Complementary Metal-Oxide Semiconductor (CMOS) process-compatible, allowing possible integration of the CMOS circuit with the RF MEMS switch. This series capacitive MEMS switch solves the substrate loss and down-state capacitance degradation problems commonly plaguing MEMS switches. The switch structure is cantilever with fingers for capacitive coupling. The vertical bending characteristic of bimorph cantilever beams under different temperatures is utilized to turn the switch on and off. A set of electrical, mechanical, and thermal models is established, and cross-domain electro-thermo-mechanical simulations are performed to optimize the design parameters of the switch. This switch is designed and fabricated using a commercial CMOS AMI 0.6 μm process through Metal Oxide Semiconductor Implementation Service (MOSIS). Two maskless postprocessing Reactive Ion Etching (RIE) steps are used to release the cantilever structure. The measured results show the insertion loss and isolation are 1.67 dB and 33 dB respectively, at 5.4 GHz, and 0.36 dB, and 23 dB at 10 GHz. The actuation voltage is 25 V. This switch has a vast number of applications in the RF/microwave field, such as configurable voltage control oscillators, filters, and configurable matching networks.

To illustrate the applications of the switch, two broadband communication applications for the designed MEMS switch, broadband voltage controlled oscillator

(VCO) and broadband filter, were demonstrated. The RF MEMS switch model developed in this dissertation is used in VCO simulation to reduce the noise introduced by the traditional PMOS switch. The low-loss, low-noise nature of the MEMS switch improved VCO phase noise performance. The MEMS technology also can be used to improve the inductor quality factor by using finite element simulation; it is found that the quality factor (Q factor) of a micromachined inductor is improved to 11.5 compared to the previous Q factor of 7. In addition, we demonstrate the use of MEMS switches to enable large corner-frequency adjustments in high-frequency, lowpass filter designs. The frequency corner of the filter was demonstrated to be configurable over a very wide range, from 944 MHz to 3.06 GHz.

Overall, this work demonstrates how high-performance configurable microwave circuit design can benefit from the introduction of the novel MEMS switch.

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List of Acronyms

AFM	Atomic Force Microscopy
AMOS	Accumulation Metal-Oxide Semiconductor
BER	Bit Error Rate
BiCMOS	Bipolar and Complementary Metal-Oxide Semiconductor
CAD	Computer Aided Design
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
EDP	Ethylene-Diamine-Pyrocatechol
EM	Electromagnetic
ET	Electro-Thermal
FDNR	Frequency Dependent Negative Resistor
FEM	Finite-Element Modeling
FET	Field Effect Transistor
FOM	Figure of Merit
FSR	Frequency of Self Resonance
HFSS	Ansoft High Frequency Structure Simulator
IC	Integrated Circuit
ICP	Inductively Coupled Plasma
ISS	Impedance Standard Substrates
LNB	Low Noise Block Converters
LPF	Low Pass Filter
L-Band	1-2 GHz Microwave Band

MIM	Metal Insulator Metal
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor
MOSIS	Metal Oxide Semiconductor Implementation Service
OP-AMP	Operational Amplifier
PAN	Personal Area Network
PCB	Printed Circuit Board
Q factor	Quality Factor
RIE	Reactive Ion Etching
RF	Radio Frequency
RF-CMOS	Radio Frequency Complementary Metal-Oxide Semiconductor
RF-MEMS	Radio Frequency Micro-Electro-Mechanical System
SAW	Surface Acoustic Wave
S-Band	2-4 GHz Microwave Band
SCA	Switched Capacitor Array
SEM	Scanning Electron Microscopy
SOLT	Short, Open, Load and Thru
SPICE	Simulation Program with Integrated Circuit Emphasis
SSB	Single Sideband
TAI	Tunable Active Inductor
TCE	Thermal Coefficient of Expansion
VCO	Voltage Controlled Oscillator
WCDMA	Wireless Code Division Multiple Access
WLAN	Wireless Local Area Network

Chapter 1 — Introduction and Background

1.1 Introduction

A radio frequency micro-electro-mechanical (RF MEMS) switch is a semiconductor device that uses mechanical movement to achieve a short circuit or open circuit in radio frequency applications. RF MEMS switches offer low contact resistance, low power consumption, low off-state capacitance, broadband operation, and high linearity [1]. In this dissertation, a novel RF MEMS switch is proposed with applications for VCO and filters. This chapter introduces the background information about the Radio frequency micro-electrical-mechanical system (RF MEMS) switch and its broadband applications.

1.2 Radio Frequency Micro-Electro-Mechanical System Switch Background

1.2.1 MEMS Switch Overview

Switches are used in various RF systems and provide the capability of redirecting the signals, thus enhancing the system flexibility and expandability. The RF switch is an integral part of any RF system. The quality of the RF switch can make the difference between marginal and superior performance. Various parameters are to be considered in the design of RF switches, such as:

1. Transition time
2. Switching rate
3. Switching transients
4. RF power handling
5. Matching with circuits
6. Bandwidth
7. Insertion loss

8. Isolation
9. Series resistance
10. Actuation voltage
11. Lifetime
12. Resonant frequency
13. Interception and level of distortion
14. Phase and amplitude tracking and matching for multi-throw switches [2].

RF MEMS switches offer a substantially higher performance than p-i-n or field-effect transistor (FET) diode switches and have been used extensively in state-of-the-art MEMS phase shifters and switching networks up to 120 GHz [3]. The switches can be categorized by the following three characteristics:

1. RF circuit configuration
2. Mechanical structure
3. Form of contact. The common contact forms are the capacitive (metal–insulator–metal) and resistive (metal-to-metal). Each type of switch has certain advantages in performance or manufacturability. Figure 1-1 illustrates two commonly used MEMS switch configurations: cantilever and air bridge [4].

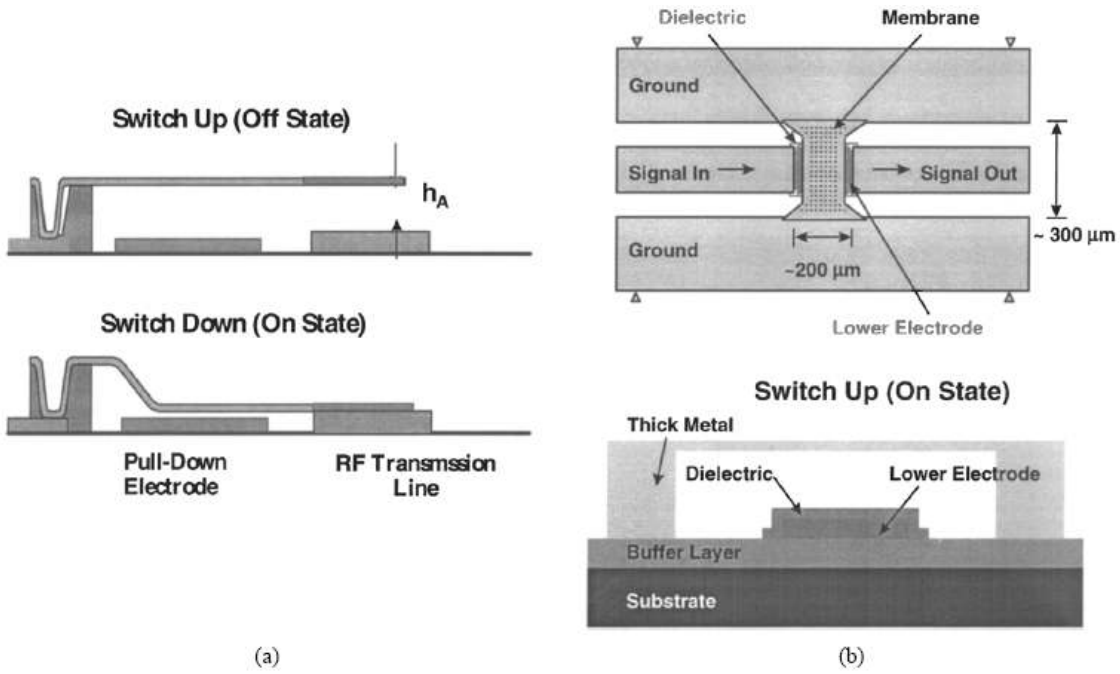


Figure 1-1: Diagrams of two common RF MEMS switch structures, (a) cantilever (b) air Bridge [4]

The cantilever uses a thin layer of metal and dielectric that is anchored at one end and free moving on the other. The air bridge type of switch uses a thin strip of metal and a dielectric that is fixed at both ends and is free moving in the middle. The actuation of the switch is when a bias voltage is applied between the contacts. The charge potential will pull the top contact down toward the bottom contact; when the applied voltage reaches a certain threshold value, the cantilever contacts the bottom one. This makes a DC signal path between the top layer and the bottom layer metals. If the actuation voltage is removed, the cantilever backs up due to the build-in stress of the structure.

The DC contact switch may operate unreliably or be subject to premature failure resulting from the adhesive force and the microwelding of the two contact metal layers [5]. The capacitive switch has the advantage of not having this problem; however, there are several problems with current capacitive switches [6]:

1. The substrate loss depreciates switch performance.
2. The small on/off ratio of the switch capacitance is limited by the small distance between the two electrodes.
3. The high-actuation voltage [5] (50~60 V) requirement is not compatible with the complementary metal oxide semiconductor (CMOS) process .
4. The down-state capacitance degradation problem, that is, the actual down-state capacitance, is much smaller than the designed value. This problem is usually caused by the nonplanar property of the metal bridge, the roughness of the contact area, and the existence of the etching holes in the metal bridge.

Recently, a capacitive switch built on a highly resistive substrate was reported by Yu, et al., [7]. It solves the substrate loss and the down-state capacitance degradation problems by using a dielectric layer on the ground pad. However, the higher resistive substrate is expensive, and the process is complex. To reduce the actuation voltage, Lee reported a switch design that used movable pads for switching operations [8]. A piezoelectrically actuated RF MEMS switch is reported in [9]. This switch achieved switching voltage of 2.5 V, which is compatible with standard CMOS circuits. However, the MEMS switch in [8] and [9] was custom built and required extra processing steps and lithographical masks, implying high cost and low repeatability. In another development of the MEMS switch using the piezoelectric bimorph actuator [10], low actuation voltage 3 V is achieved. However, it requires special steps and extra lithographic masks to deposit piezoelectric material Aluminum Nitride (AlN), which results in higher cost. Silva [11] demonstrated integration of a cantilever MEMS switch and Bipolar CMOS (BiCMOS) actuation circuit in the same package.

Because the actuation voltage is 30 V, a charge pump is implemented to generate the 30 V from the 3 V power supply. The die mounting, wire-bonding process for putting both chips in the same package is a complex process.

1.2.2 Applications in Broadband Communication

Broadband communication systems require high-performance local oscillators and filters to achieve the high data rate transceiver design. At the same time, the oscillators and the filters need to be tunable within a wide range of frequencies for two reasons: first to compensate the process and temperature variations, and second, to be flexible to support multiple communication standards. By using a low-loss, low-noise MEMS switch, the oscillator and filter performance can be improved dramatically compared to their counterpart, which uses the metal-oxide semiconductor field effect transistor (MOSFET) switch.

1.3 Contributions of the Dissertation

The work reported in this research demonstrates a novel switch design that addresses many of the problems described above. The proposed electro-thermally (ET) actuated switch reduces the substrate loss and down-state capacitance degradation problems. It does not require complex fabrication steps. The switch is fabricated using a commercial CMOS process through metal oxide semiconductor implementation service (MOSIS). It is built on a low-resistive substrate, and the capacitor is formed by the sidewall coupling of a set of interdigitally crossed fingers on a cantilever beam. A thermal actuation method is used to reduce the actuation voltage and to improve reliability. Two maskless reactive ion etching (RIE) steps are used to release the cantilever structure. The measurement results show that the insertion loss is 1.67 dB, and isolation is 33 dB at 5.4 GHz; the

insertion loss is 0.36 dB, and isolation is 23 dB at 10 GHz. The MEMS switches are small, with high linearity, and can be integrated with CMOS circuits. However, as the first implementation of the switch requires actuation voltage of 25 V, it is not compatible with CMOS circuit voltage requirement of 5 V. With better optimization, the activation voltage can be reduced.

Application of the switch to a multiband VCO is illustrated. Two Colpitts voltage controlled oscillator (VCOs) were designed, simulated, and compared: one with a MOSFET switch and one with a MEMS switch. The simulation results show that the VCO phase noise improvement is 20 dB at 1.9 GHz with 100 K offset.

The second application of the switch is an integrated 6th-order, elliptical lowpass filter. The filter is configurable to L-band or S-band operation. The design is implemented using frequency dependent negative resistor (FDNR) structures with configurable capacitor blocks utilizing MEMS switches. The frequency corner of the filter was demonstrated to be configurable over a very wide range – from 944 MHz to 3.06 GHz.

1.4 Organization of the Dissertation

The organization for the rest of this dissertation is as follows. The design and modeling of the novel ET actuation RF MEMS switch are given in Chapter 1 , the switch design flow, design parameter tuning, and the actuation method are described in detail. Different MEMS computer aided design (CAD) software is used in simulation and design of the MEMS switch. The equivalent circuit model is derived based on 3-D electromagnetic (EM) simulation results. In Chapter 3 , the CMOS compatible fabrication process of an ET switch is presented, and the released structure is shown and described.

Chapter 4 presents the measurements and characterization of the ET switch. Experimental characterization of the ET switch includes the test of its electrical, mechanical, and thermal characteristics. In Chapter 5 the application of the broadband voltage controlled oscillator that was developed by using the ET switch is described, the different VCO topologies are compared for the multiband application, and the final design and experiment results are presented. In Chapter 6 another microwave application of the ET switch, broadband filter, is described. An integrated 6th-order, elliptical lowpass filter that can be configured to L-band or S-band operation is presented. The design is implemented using FDNR structures with configurable capacitor blocks utilizing MEMS switches. Chapter 7 concludes the dissertation and possible direction of future works.

Chapter 2 — Novel Electro-Thermal Actuated RF MEMS Switch Design and Modeling

This chapter covers the novel ET MEMS capacitive switch design and modeling. The switch design flow, parameter tuning, and actuation method are described in detail. Different MEMS design software is used in designing and modeling the switch. A comprehensive introduction of a novel computer-aided MEMS switch design flow is given. An electrical equivalent model of the switch is derived from the 3-D EM simulation.

2.1 MEMS Switch Design

2.1.1 Theory of Switch Operation

Currently, the capacitive coupled switches are usually implemented using two vertically aligned electrode plates [5]. By actuating the top electrode plate to move downward and reduce the gap between the two plates, the switch is turned on. The popular actuation methods are electrostatic, thermal, or EM. However, it is difficult to implement two vertically separated metal plates with sufficient distance between them using a commercial CMOS process. The process normally has 2–6 layers of metal and 1–3 layers of SiO_2 on top of the silicon substrate. The thickness of the dialectic layer between the metal layers is normally less than 1 micrometer. That gives very small capacitance while two plates are close to each other. Another problem for vertically implemented capacitive switches is the difficulty of etching between two metal layers to release the top metal plate.

Because of these limitations, a horizontally coupled capacitive MEMS switch is proposed as an alternative. The design uses fingers on the side of the cantilever beam to implement a capacitive series RF MEMS switch. The capacitance value is configurable based on the number of fingers on the structure. The schematic and 3 D view of the design switch is shown in Figure 2-1 and Figure 2-2, The switch is thermally activated through the heating of a trace of the polysilicon. The meaning of RLC components in Figure 2-1 are explained in the section 2.2 .

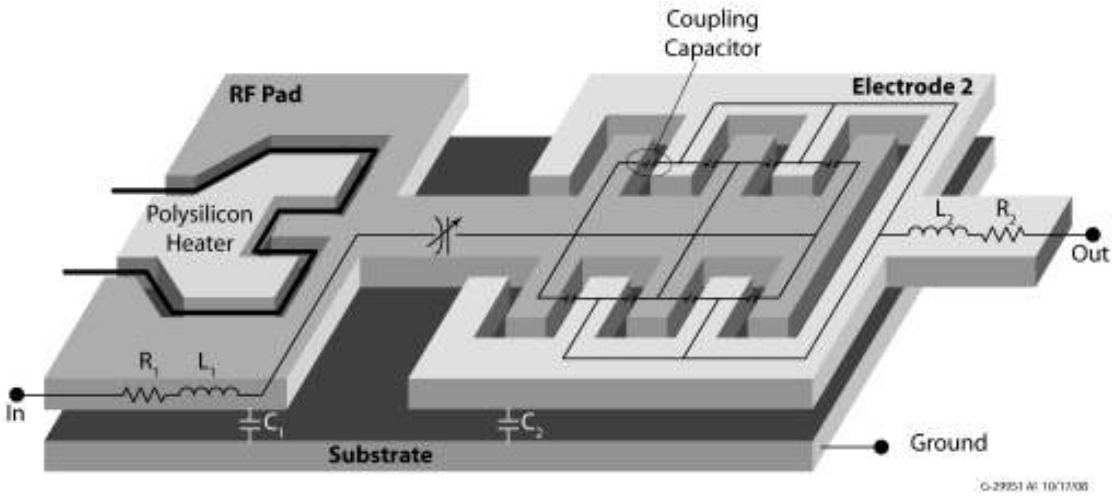


Figure 2-1: Thermally actuated RF-MEMS switch diagram

The capacitance is also determined by the composition of the finger structure. The process used in this work has a total of three layers of metal with SiO_2 between them. The total height of the structure is approximately 4.2 μm. The ON-OFF condition of the switch has to be simulated both in the electrical and thermal domains. A finite element modeling (FEM) based MEMS design software, Coventorware, is used to simulate the coupled electro-thermo-mechanical behavior. Based on the CoventorWare simulation results and measurement results of prototypes with different combinations of metal layers, the structure with all three layers of metal is selected for better capacitive coupling.

Figure 2-2 shows the 3-D view of the RF MEMS switch. Port0 and Por1 are RF pads. The Port 0 is also used as DC bias pads. In order to provide proper DC isolation, there is a small DC blocking gap at the top-level metal between the support beam and the heater.

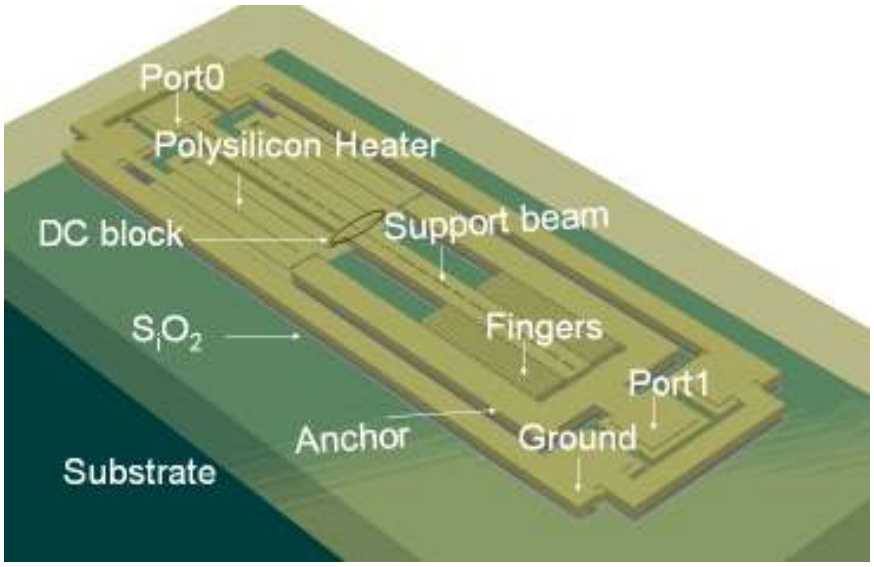


Figure 2-2: RF switch 3-D view with substrate (40-finger design is shown)

There are several parameters to be optimized to achieve the desired capacitance ratio and actuation voltage: the length of the supporting beam, the polysilicon heater resistance, the number of the fingers, and the gap between the fingers that determines the coupling capacitance. The maximum capacitance is also limited by the process and the composition of the finger structure. The length of the beam is determined from the thermal simulation. One end of the cantilever is fixed as an anchor. Figure 2-3 shows the stacked up information for the switch from the silicon substrate up. The polysilicon located between the substrate and the metal layer 1 is used as a heater. The different metal layers are connected by many tungsten vias for electrical conductivity.

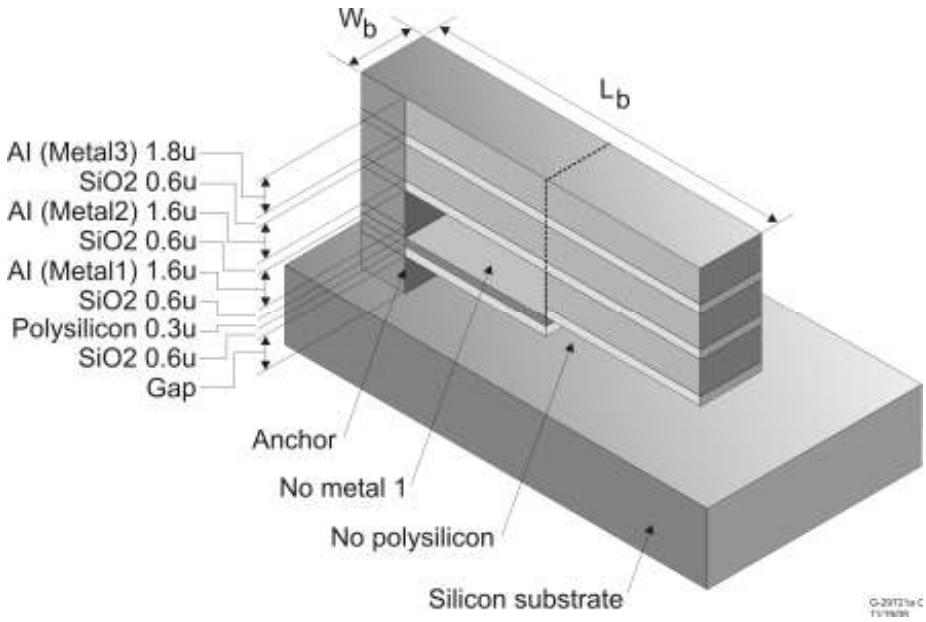


Figure 2-3: Side view of the RF MEMS switch (stator and rotor fingers are not shown for clarity)

Switch topologies include the cantilever and membrane switches, and the contact types including DC and capacitive contact. The movement type can be vertical or lateral. The actuation method includes electrostatic, electromagnetic, magnetic, piezoelectric, and thermal. Out of all these choices, the following design parameters were chosen, as shown in Table 2-1.

Table 2-1: MEMS switch design parameter

Topology	Cantilever
Contact Type	Capacitive
Movement	Vertical
Actuation	Thermal/Electrostatic
CMOS Process Compatible	Yes

The design choices are made based on the application. Cantilever topology was chosen because it requires lower actuation voltage than membrane implementation. The

lateral movement switch can be low-voltage actuated; however, it is more complicated in process and occupies a larger area than the vertical switch. Thus, a vertical movement switch is chosen over a lateral one. Because the DC contact type requires high force and has the issues of stiction, corrosion, and microscopic bonding, the capacitive switch is chosen. Because the thermal actuation is very reliable and uses relatively low voltage, the thermal actuation method is chosen to achieve a reliable, low-voltage switch operation. Electrostatic actuation is used to reduce the power consumption. Because of the need for integration with electronic circuitry, a complicated MEMS process cannot be applied. As shown in Figure 2-4, the ON position of the switch is when the cantilever is in its flat position and two set of fingers are interdigitally coupled. The OFF position, as shown in Figure 2-5, is when the cantilever beam is buckled up and two sets of fingers are not on the same plane. This design has the property of high ON/OFF capacitance ratio, required by the MEMS switch.

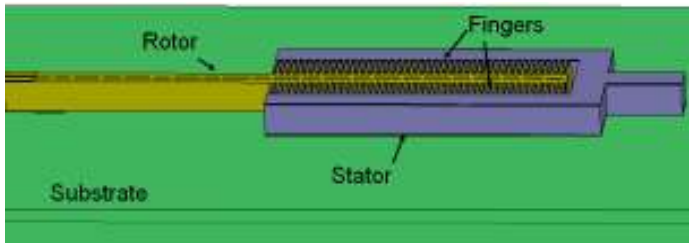


Figure 2-4: MEMS switch ON position

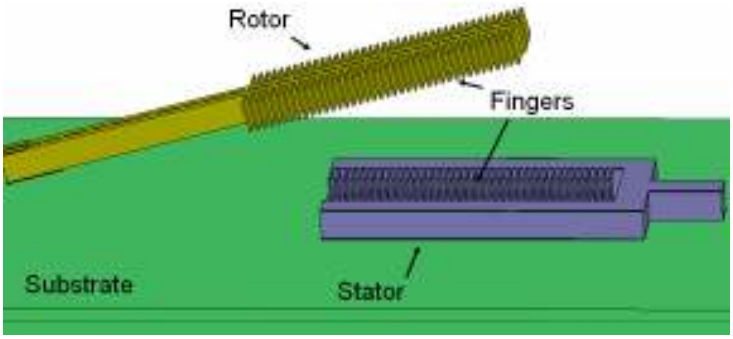
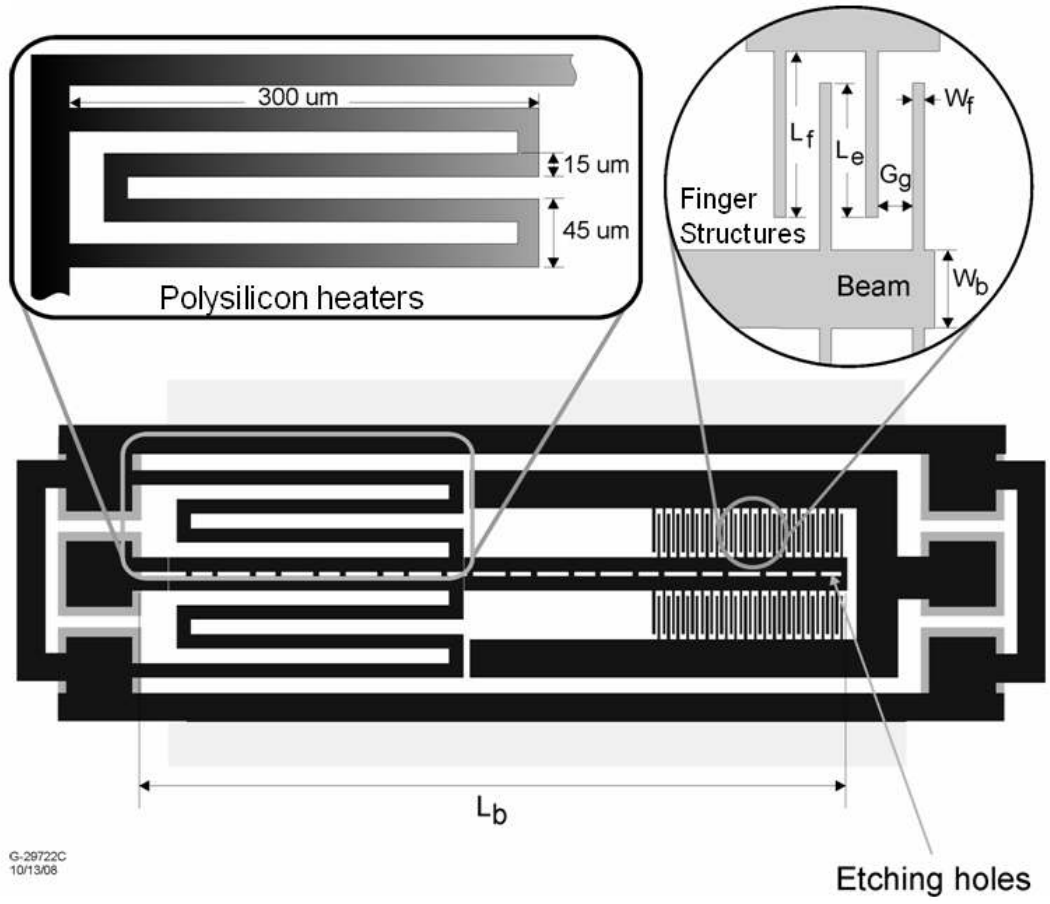


Figure 2-5: MEMS switch OFF position

Figure 2-6 shows the top-view geometry of the capacitive series switch and the polysilicon heater. The parameters are chosen based on EM and thermal simulation; the ON-state capacitance values are determined by the engaged length of the fingers L_e, the gap between the fingers G_g, and the number of fingers f_n. The finger gap was chosen based on postprocessing capability as well.



W_b : Width of the supporting beam

L_b : Length of the supporting beam

L_f : Length of the finger

L_e : Engage length of the finger

G_g : Gap between the fingers

W_f : Width of the finger

f_n : Number of the finger

h_a : Height of the finger

Figure 2-6: Schematic view of the designed fingers

The design variables are listed in Table 2-2. The polysilicon heaters are located near the anchor point of the beam for better control of the beam temperature. In CMOS circuits, normally the switch fingers are disengaged, corresponding to the switch-off condition. When the polysilicon heater is heated, the temperature rise of the beam causes the bimorph beam to bend downward so that the intercoupled fingers are engaged, serving as a switch-on position. The parameter of the beam is chosen based on EM and thermal simulation as listed in Table 2-2.

Table 2-2: Design specifications of switches

Design	f_n	L_b **(µm)**	L_f **(µm)**	L_e **(µm)**	G_g **(µm)**	W_f **(µm)**
1	80	738	45	40	1.5	3
2	80	500	45	40	1.9	3
3	40	250	45	40	2.1	3

For all designs, all three layers of metal are used at the stacked finger part and metal 2,3 are used at the beam as shown in Figure 2-3. The width of the beam W_b is set to 35 µm. To facilitate etching, 10 µm x 5 µm etching holes are designed on the supporting beam as shown in Figure 2-6. The etching holes are located in the center of the beam to avoid structure stability issue.

2.1.2 ET Actuator Design

This section presents a thermal actuator design and steady-state analysis of the thermal actuator. ET actuators yield a higher output force (O(1mN)) at a significantly lower drive voltage (5–10 V) than electrostatic actuators of comparable size, which have

output forces of O(1 μN) at a drive voltage of 100 V [12]. ET actuators are also easy to fabricate because of their unitized construction and material compatibility with the manufacturing processes of CMOS microelectronics.

2.1.2.1 Thermal Actuator Design

The heating elements are implemented using polysilicon strips. The sheet resistance of the poly is 22.9 Ω/sq μm from AMI C5 process datasheet. The resistance of the polysilicon strips is designed to be 1 kΩ to reduce the impedance impact of the polysilicon heater. The polysilicon heaters are located under the main cantilever beam, and they are released together with the cantilever structure. The heat is transferred from the polysilicon heater to the cantilever structure through the SiO_2 layer. The device is anchored to the Si substrate. The substrate is thermally grounded by contact with a large thermal mass at the ambient temperature. The thermal equilibrium point is achieved when the heat generated by DC current and the loss to the substrate and air are equal. The polysilicon resistor on the bottom of the beam is driven by a static DC voltage U_{dc}. The electrothermally generated power is

$$P(t) = \frac{U_{dc}^2}{R} \tag{2.1}$$

where R is the electrical resistance of the heater resistor. The static power results in a static temperature distribution with a uniform heat generation over the resistor, assuming the heat flows toward the anchor point, which is the ideal heat sink. As shown in Figure 2-7, for the heat generated from the resistor centered at location x_0, the average temperature elevation ΔT_{av} integrated over the beam depends on x_0/l and is given by [13].

$$\Delta T_{av} = P_{stat} \frac{l[x_0/l - (x_0/l)^2]}{2bh\lambda} \tag{2.2}$$

where b, h, and l are the width, thickness, and length of the beam, respectively, and λ is the heat conductivity of the beam material. With $\lambda = 235$ W/mK for aluminum, w = 35 µm, h = 4.2 µm, l = 300 µm, position $x_0/l = 0.95$, the temperature elevation can be calculated as $\Delta T_{av}/P_{stat} = 206k/W$ [14].

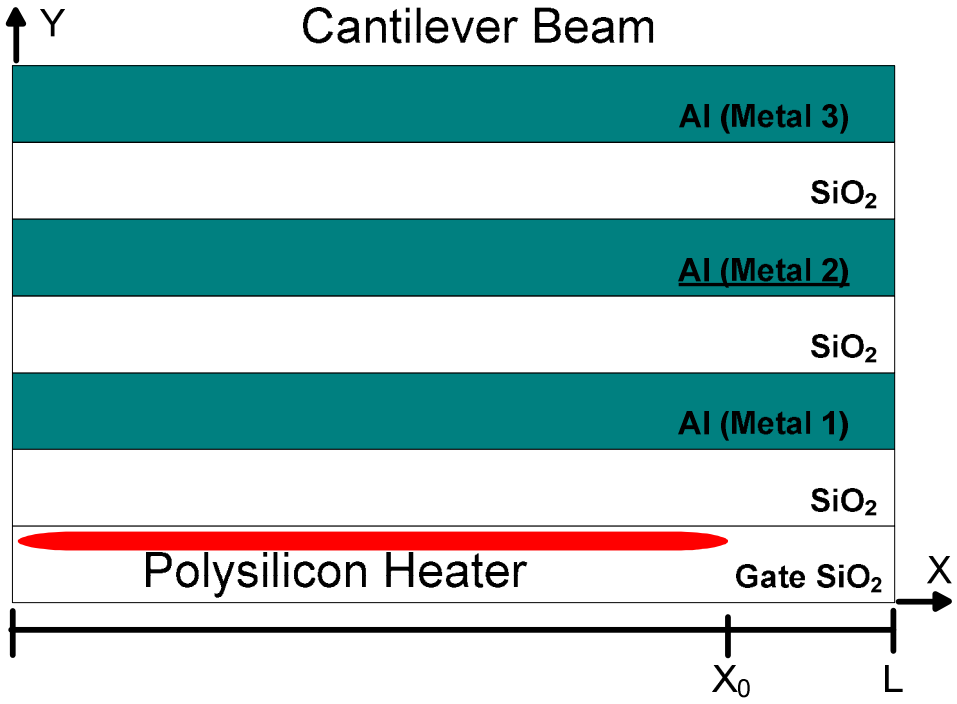


Figure 2-7: Cross section of a thermally actuated composite cantilever beam

In the composite beam structure, the dioxide and nitride layers of the CMOS process are modeled as a single SiO_2 layer with single thermal and mechanical properties as shown in Figure 2-7. The metal 3 layer is used as the etching mask for the postprocessing steps. The average temperature elevation of the beam induces an expansion of the beam due to the different temperature coefficients of the Al and SiO_2. The beam bends toward the substrate when the temperature rises.

For these thermally actuated switches, proper isolation between the DC heater supply and AC signal is required. Different options were explored. Option 1 is shown in Figure 2-8 (a); this structure is connected to the G-S-G type of probe and the DC is provided through two separate DC pads. The advantage of this option is that there is no crossing between DC path and AC path, so the isolation is good. The disadvantage is that the heaters are not connected to the DUT, the heat transfer is through air radiation and substrate coupling, and the efficiency is low. Also, the measurement is difficult due to multiple DC source requirements. Another option is to use the same probe pad for both DC and AC signals, as shown in Figure 2-8 (b). The advantage of this option is good thermal coupling between heater and the DUT because the heater is located under the beam of the DUT. The measurement of this option is also easier than option 1 as only one bias-tee at the DC/AC pad to isolate the DC power from AC signal is required. However, proper layout arrangement is required to isolate the protective metal 3 on top of the polysilicon heater, there are a small cut (2μm) made to the metal 3 showing in the drawing for this purpose.

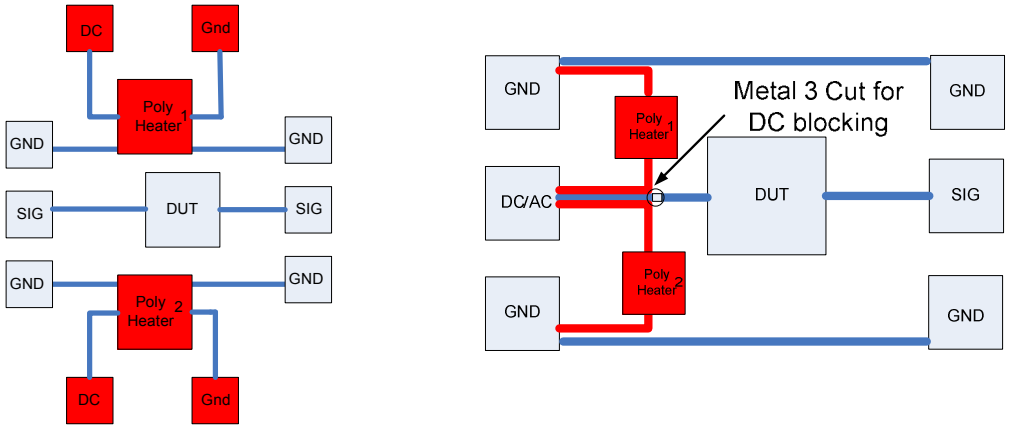


Figure 2-8: Heater design options for thermally actuated switch (a) heater uses separated DC pad, (b) heater uses shared signal pad

In order to find the optimal layout for the polysilicon heater, three layout options for the polysilicon heater are shown in Figure 2-9. Option (a) uses a separate DC bias pad, and the heater is designed to be embedded underneath the finger structure intended to have better heat transfer to the finger structure. However, after RIE release step, the finger structure is released and separated from the heaters, this option is not thermally efficient. Option (b) is improved over option (a) as the polysilicon heater is covered by the beam and released with the beam. However, the resistance of the polysilicon is low because of the parallel path of the heater. Finally, option (c) is selected for its configurable resistance and better heat transfer to the beam. It also shares the pad for AC/DC signals.

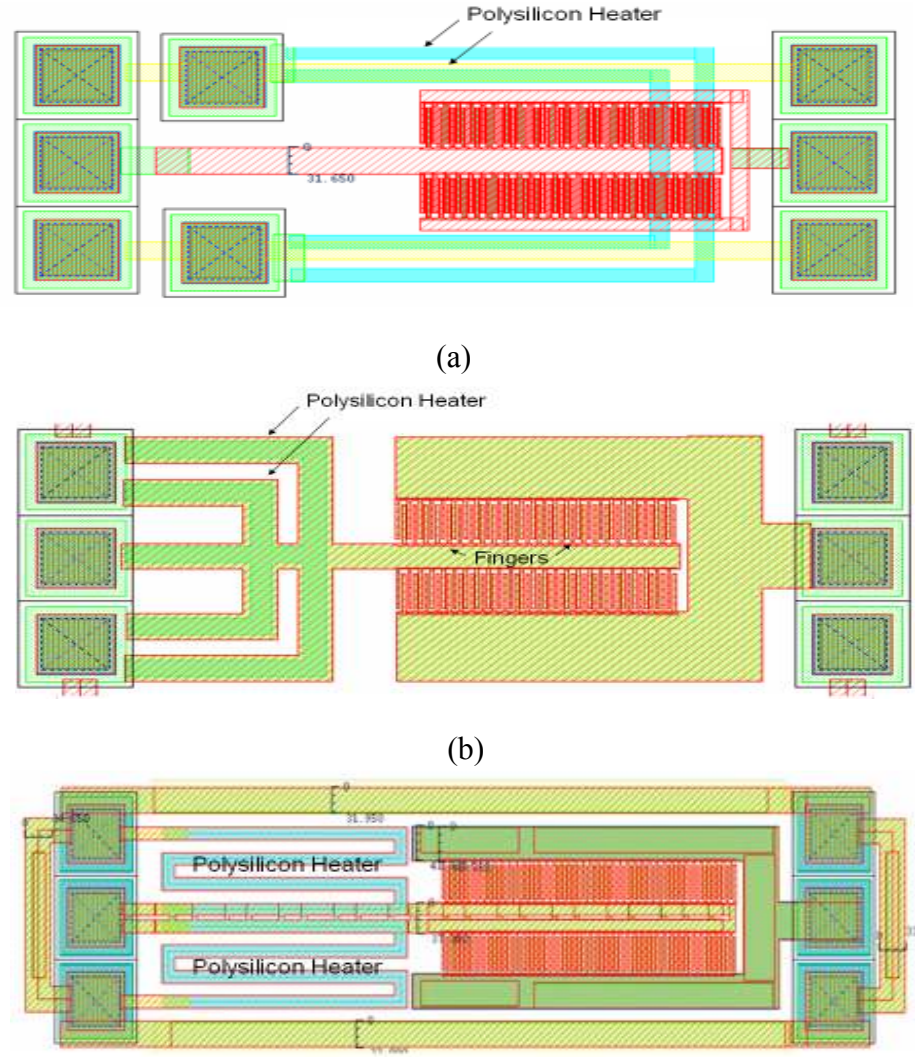


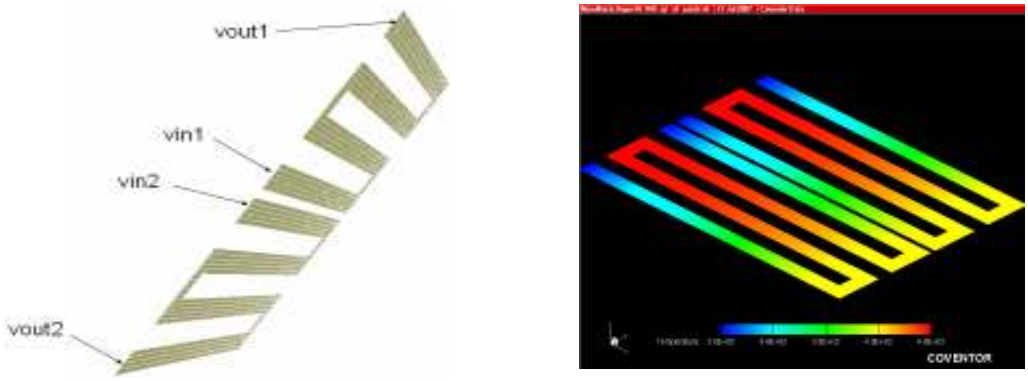
Figure 2-9: Heater design layout options for thermally actuated switch (a) heater uses separated DC pad, (b) heater uses shared signal pad, (c) final heater design

In order to find the optimal design of the heater, different heater materials and different geometries were explored. Table 2-3 shows the design options of the heater, and the shape of the heater is shown in Figure 2-9 (c). The resistance value is from the AMI C5 process technology specifications. A 3-D model is constructed and meshed by using

Manhattan brick configuration, and thermal simulation was carried out using CoventorWare to determine the temperature of the device. Figure 2-10 shows one of the simulation setups with two polysilicon heaters and the temperature simulation result.

Table 2-3: The heater design options

Parameters	**Poly**	**Poly**	**Poly**	**Poly2**	**N-Well**	**N-Well + Poly**	**N-Well + Poly**
Sheet resistance Ω/square	22.9	22.9	22.9	1000	804	814	814
Length (μm)	3056	300	1338	300	300	300	300
Width (μm)	70	15	15	15	15	15	15
# of heater parallel	1	1	1	1	1	1	3
Resistance (Ω)	1000	458	2043	20000	16080	16280	5427
Input voltage (V)	35	25	35	35	15	25	35
Current (mA)	35.01	54.59	17.13	1.75	0.93	1.54	6.45
Power (mW)	1225.31	1364.63	599.70	61.25	13.99	38.39	225.74



(a) (b)

Figure 2-10: Polysilicon heater design layout and simulation results of the thermally actuated switch (a) the meshed 3D model of the polysilicon heater (b) simulation of heater temperature versus input voltage, Vin1= Vin2 = 25V, Vout1 = Vout2 = 0

From the mechanical simulation in section 2.1.3 , the required temperature rise for a switch to turn on is around 100 K, based on the calculation of equation 2.2 in which the required power to raise the temperature of the device to 100 K is about 500 mW. The final parameter of the heater is designed and listed in Table 2-4.

Table 2-4: Selected polysilicon heater parameter

Sheet resistance(Ω/square)	22.9
Resistance required (Ω)	1000
Power required (mW)	1000
Voltage supply (V)	35
Current (mA)	35
Width (μm)	70
Length (μm)	3056
Single arm length (μm)	365
Number of arms	7
Turn length (μm)	80
Number of turns	6
Total length (μm)	3035

The thermal conductivity, Young Modulus, and density of the materials used in the composite beam are listed in Table 2-5.

Table 2-5. Material properties for the finite element simulation [15]

Material	**Young Modulus** E[GPa]	**Density** $\rho[g/cm^3]$	**Thermal Conductivity** $\lambda[W/mK]$
Polysilicon	168	2.3	2.8
Silicon Oxide	74	2.2	1.4
Silicon Nitride	320	2.8	3
Aluminum	72	2.7	236

The tip displacement of the cantilever beam due to the thermal actuation is simulated using the thermal-mechanical finite element analysis tool CoventorWare. Figure 2-11 shows a polysilicon strip is used as the heater; apply the thermal drive voltage Va will result in increased temperature, which in turn generates mechanical actuation in the perpendicular direction to the substrate. For the designed beam, the generated heat from the thermal drive voltage and current Va and Ia causes the beam to buckle toward the substrate. The beam tip displacement ΔZ is simulated with different voltage Va. There is also a horizontal displacement ΔX which occurs due to the thermal expansion of the beam. ΔX is very small compared to ΔZ. The Vb is the electrostatic drive voltage that can be applied between the beam and the substrate for electrostatic hold after the beam is in its flat position. In the current device, the Vb is not applied.

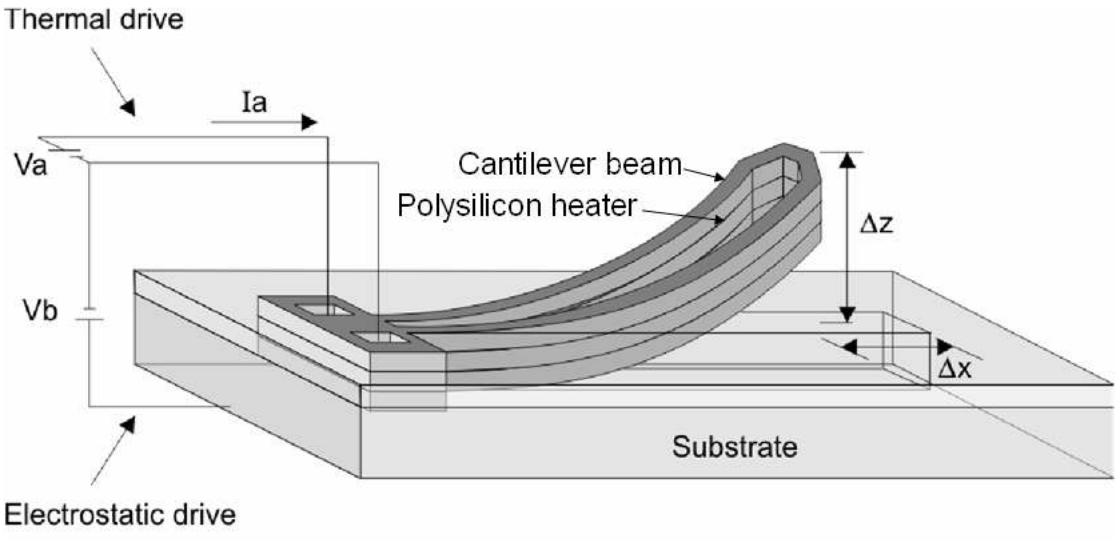


Figure 2-11: Thermal actuated bimorph beam with polysilicon heater

The model simulated was the 80-finger switch structure, and the mesher setting was shown in Figure 2-12. The Coventor simulation result of Va versus temperature change and max ΔZ displacement is shown in Figure 2-13.

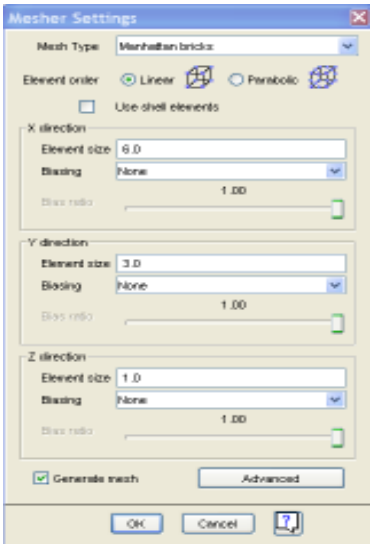


Figure 2-12: Thermal actuated bimorph beam with polysilicon heater

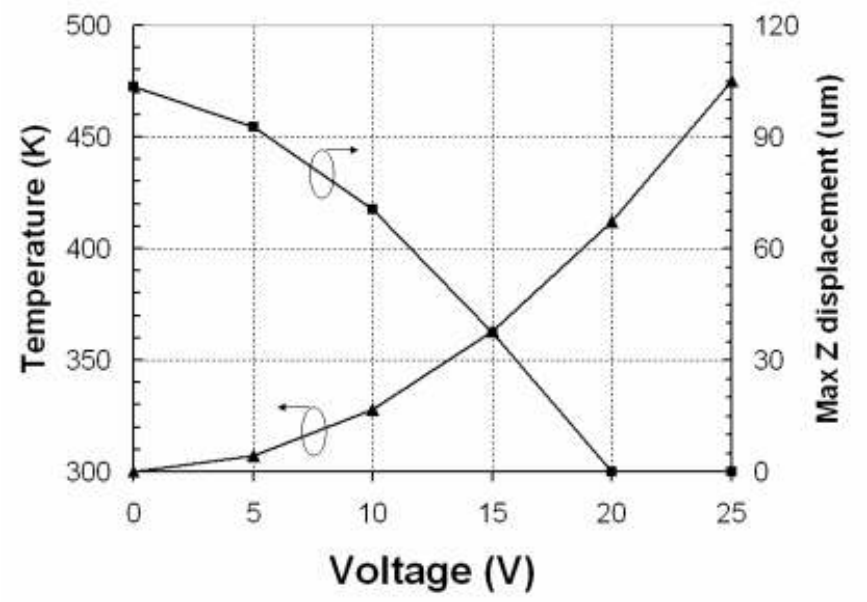


Figure 2-13: Thermal actuated bimorph beam with polysilicon heater

Figure 2-14 shows the simulated structure temperature with heated polysilicon structure and the thermal contour of the structure when input voltage is 25 V, with an ambient temperature of 300 K. The layout of the fabricated device is imported directly to the FEM tool CoventorWare for this simulation. A 3-D model is constructed and meshed by using manhatten brick configuration as shown in Figure 2-12, and thermal simulation was carried out using CoventorWare to determine the temperature of the device.

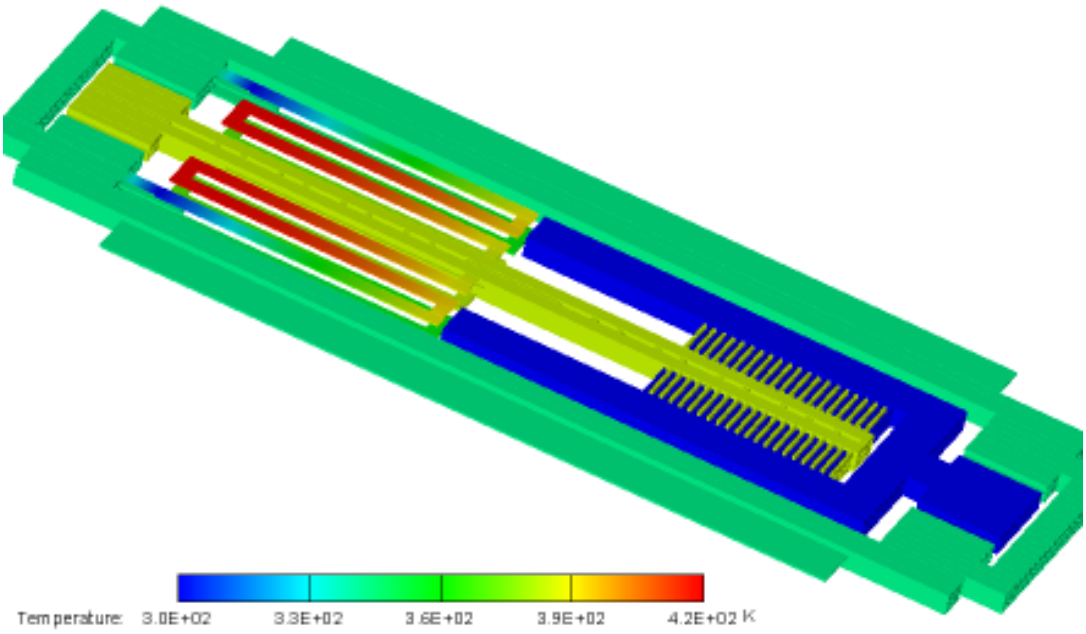


Figure 2-14: RF MEMS switch temperature distribution

2.1.2.2 Electrothermal Analysis

Electrothermal analysis assumes certain electrical driving conditions and uses the thermal model to derive the temperature distributions of the structure. The heat loss includes surface heat transfer via radiation, convection, and conduction, which are also affected by the thermal boundary conditions at the device anchors. When an electrical current is applied to the heating polysilicon, the temperature of the beam can be represented as a function of the input current. All the heat is dissipated by heat conduction and heat convection until the system is in equilibrium[16]. Heat conduction or thermal conduction is the spontaneous transfer of thermal energy through matter, from a region of higher temperature to a region of lower temperature, and hence it acts to even out temperature differences. Convective heat transfer is a mechanism of heat transfer occurring because of bulk motion of fluid.

The energy loss of the beam is mainly through heat transfer to the substrate, through radiation, and through the transfer to the ambient gas atmosphere. To reduce the energy loss of the heated beam to the substrate, reduce the electrical power input to the beam; all dimensions of the system need to be reduced. Minimize the surface area of the beam to achieve low driving power. Table 2-6 is the material property of polysilicon used in the simulation and calculation. The specific heat is the amount of heat per unit mass required to raise the temperature by 1 degree Celsius.

Table 2-6: Polysilicon properties [17]

Property	**Value**
Young modulus	169 Gpa
Thermal conductivity	30 W/m-K
Poisson ratio	0.22
Specific heat	754 J/kg-K

Figure 2-15 shows the heat transfer flow of the thermally actuated switch. Minimizing heat loss to the environment is the key to reduce the actuation energy. As stated in [18], the most significant heat loss is through the anchor point to the Si substrate. Heat flow into three parts is shown in Figure 2-15.

1. Heat conduction to the anchor q_1;
2. Free convection of upper surface of metal layer q_2;
3. Heat conduction to SiO_2 layer and free convection of lower surface of SiO_2 layer q_3. Because the mean free path of the gas molecule at room pressure is less

than 0.1 μm, assume the heat flow of the lower surface of SiO_2 layer to be free-convection.

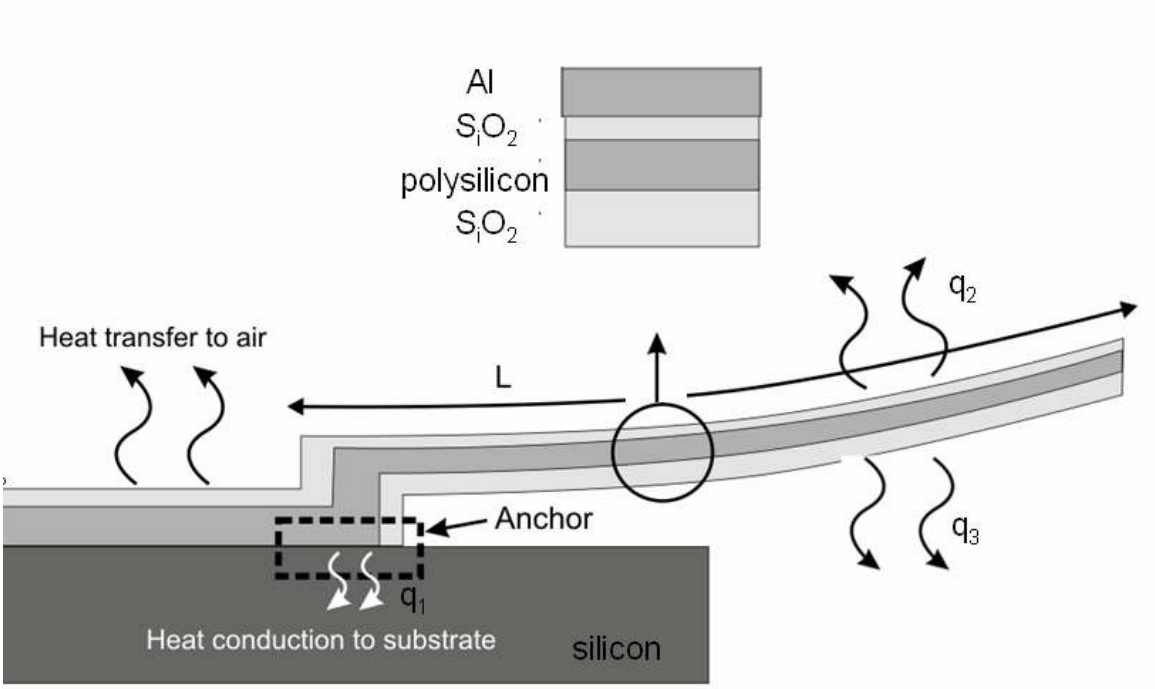


Figure 2-15: Heat flow diagram from the cross section of the thermal actuator

The power consumption P can be calculated using following equations [16]

$$P = (q_1 + q_2 + q_3) \tag{2.3}$$

$$q_1 = \frac{T_w - T_0}{\frac{n}{K_1 t_1} + \frac{t_2}{K_2 A_1} + \frac{H}{K_3 A_1}} \tag{2.4}$$

$$q_2 = h_1 A_2 (T_w - T_0) \tag{2.5}$$

$$q_3 = \sqrt{h_2 p K_2 A_2}\,(T_w - T_0)\frac{\sinh mL + \left(\frac{h_2}{mK_2}\right)\cosh mL}{\cosh mL + \left(\frac{h_2}{mK_2}\right)\sinh mL} \tag{2.6}$$

where T_0 is the room temperature, T_w is surface temperature of the Al beam, K is the thermal conductivity, h is the convection heat-transfer coefficient, A is the interface area,

H is the height of the anchor, p is the perimeter of the cantilever, L is the length of the cantilever, and $m = \sqrt{h_2 p / K_2 A_2}$. The constant n is determined by the ratio of b_0 to b, where b_0 is the width of the anchor, and b is the width of the cantilever. The power consumption as the function of the temperature change is shown in Figure 2-16. The parameters used for the calculations are listed in Table 2-7.

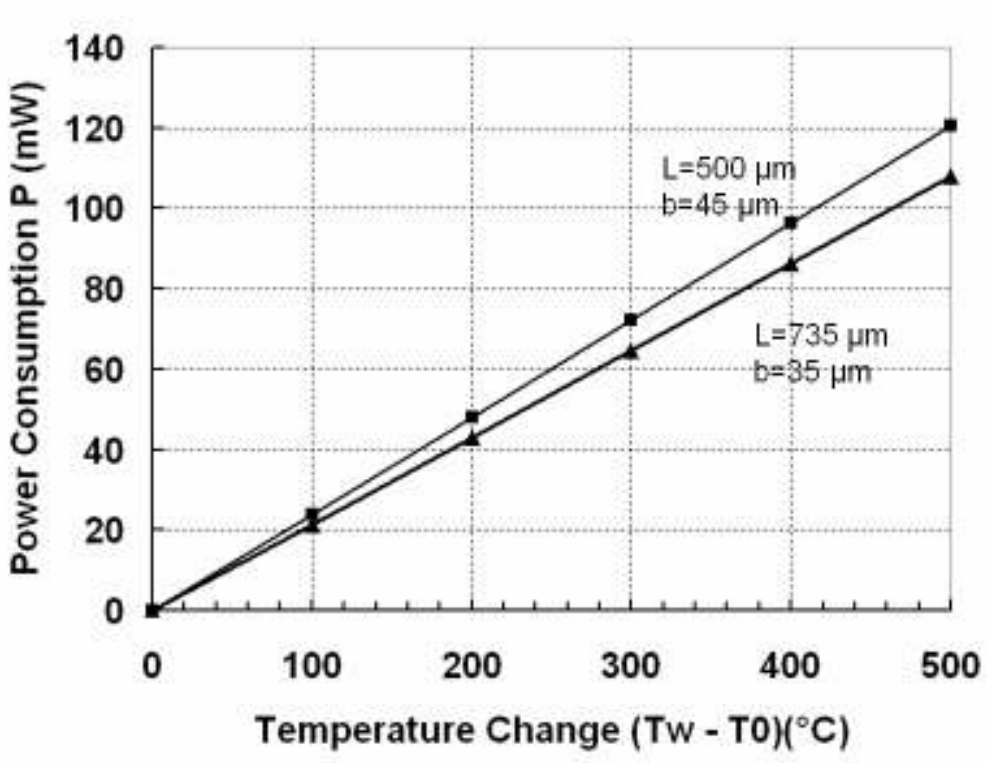


Figure 2-16: Power consumption as the function of the temperature change for bimorph beam

Table 2-7: Parameters used in the heat flow calculations

Thermal conductivity for SiO_2	K_2	2.66 $w/m°C$
Thermal conductivity for Al	K1, K_3	202 $w/m°C$
Heat transfer coefficient for upper surface of Al	$h_1 = 1.32(\frac{T_w - T_0}{L})^{\frac{1}{4}}$	$w/m°C$
Heat transfer coefficient for lower surface of SiO_2	$h_2 = 0.59(\frac{T_w - T_0}{L})^{\frac{1}{4}}$	$w/m°C$
Height of the anchor	H	64μm
Thickness of Al layer	t_1	1.8 μm
Thickness of SiO_2 layer	t_2	0.6 μm
Length of the cantilever	L	735 μm
Constant	n	1
Width of the cantilever	b	35 μm
Perimeter of the cantilever	p=2(L+b)	1540 μm
Interface area of the anchor	$A_1 = b_0^2$	100 x 100 μm^2
Interface area of the beam	A_2 = L x b	25725 μm^2

When the switch is thermally actuated with the temperature rise, the beam will bend down because of the different thermal coefficient of the composite material.

Figure 2-17 shows the heat flux distribution of the simplified model at the input of 10 V. The fingers are removed for faster simulation time.

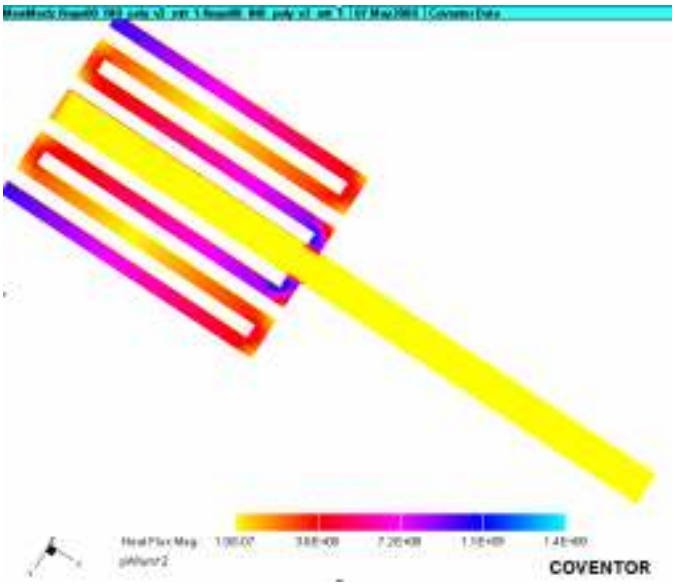


Figure 2-17: Heat flux when input is 10 V

In order to determine the threshold voltage applied to the thermal heater, thermal simulation has been carried out to find the relationship between the input power and the temperature rise of the structure.

Figure 2-18 shows the current of the polysilicon heater when the input voltage is changing from 10 V to 100 V. The polysilicon heater resistance is designed as 1 kΩ.

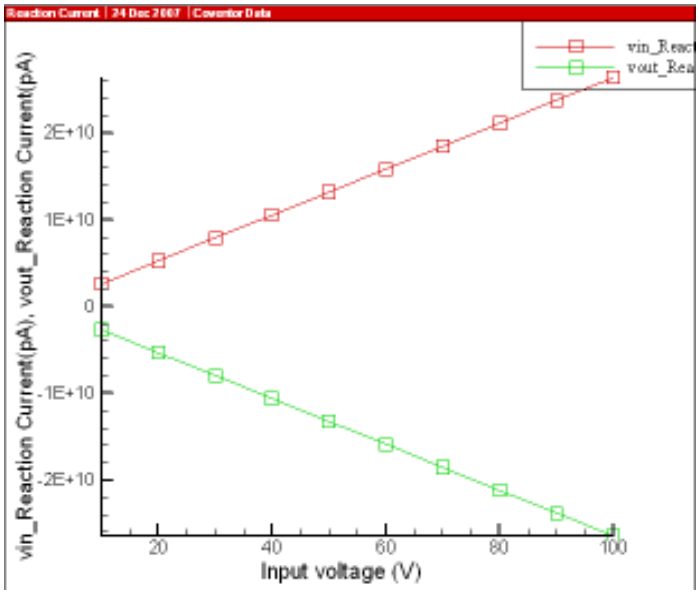


Figure 2-18: Current vs. voltage with polysilicon heater simulation

Figure 2-19 shows the Coventor simulation result of temperature change versus the input power change. At 0.5 W, the temperature of the structure reaches 100° C.

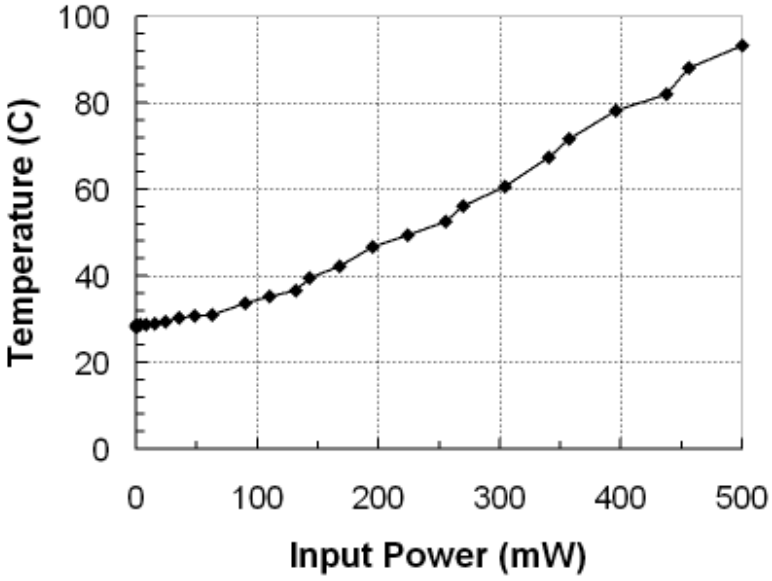


Figure 2-19: Temperature change with variation of the input power

2.1.3 Mechanical Design Considerations

This section describes the analysis of initial displacement of the switch and the analysis of displacement of the switch responding to the actuator temperature change.

Thermal-elastic analysis uses the results from electrothermal analysis and predicts the mechanical deformation of the structure based on the elastic and thermal characteristics of the materials. The switch is composed of metal layers and silicon dioxide layers. As the silicon dioxide film is grown or deposited at an elevated temperature and the coefficient of the thermal expansion of the film is different from that of silicon, internal strain or stress develops when the SiO_2/Al composite beam is cooled down to room temperature. The strain/stress is often referred to as a thermal strain/stress or a residual strain/stress. [19] Initially the bimorph switch with one end fixed will curve up after

release of the beam. With temperature increase, the upper aluminum layer will expand more than the lower SiO_2 layer due to its larger thermal expansion coefficient.

Figure 2-20 shows the diagram of one of the thermally actuated beams with polysilicon resistor as the heater. The beam width is 35 μm, the length is 735 μm, and the thickness of the composite beam is 4.2 μm. The silicon substrate is about 300 μm thick. The thermal expansion difference between SiO2 and Al is listed in Table 2-8.

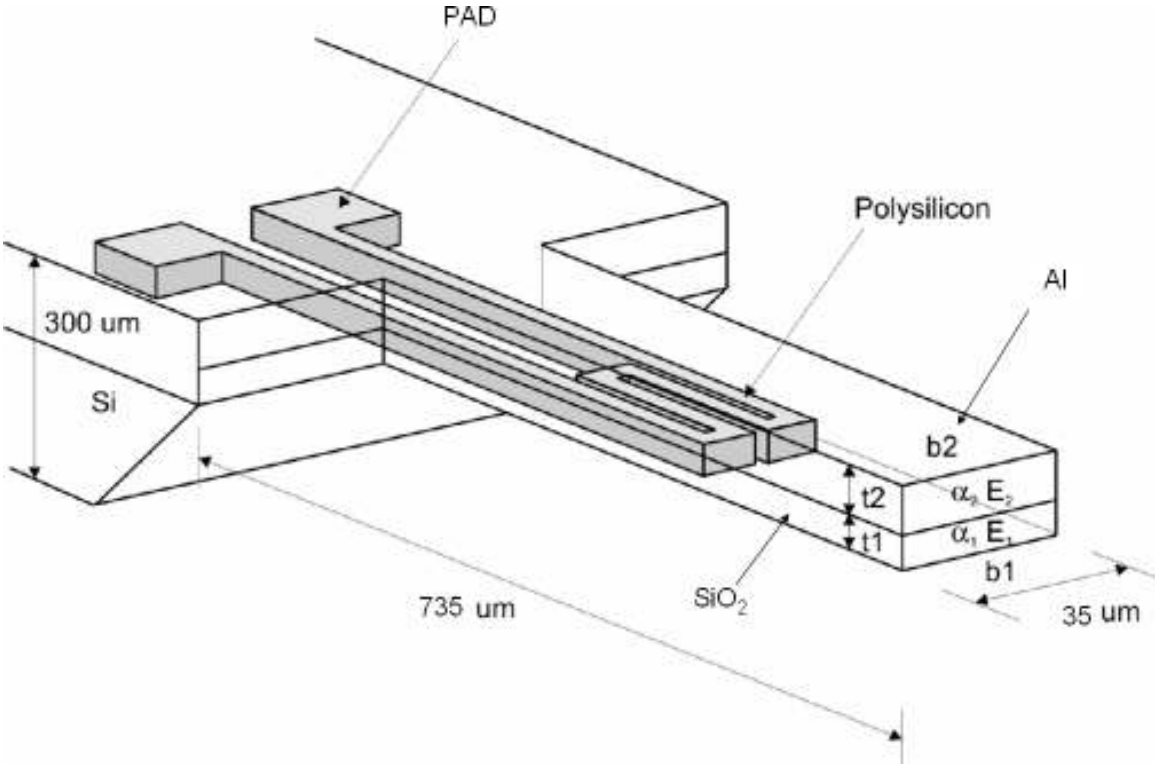


Figure 2-20: Diagram of the thermally actuated beam showing composite material

Table 2-8: Conversion factor for different combination of materials [20]

Material	γ [10^{-6}/k]	$\Delta\alpha$ ($l = 500\mu m$ $t = 0.5\mu m$)
Si-Al	3.95	1
SiO_2-Al	4.84	-7

For a bimorph beam, the deflection d at the free end of the cantilever with the temperature change ΔT_{av} is calculated with the following formula:

$$d = \gamma.\Delta T_{av} \tag{2.7}$$

γ is the conversion factor assuming the heat distribution within the cantilever is uniform [20].

$$\gamma = \frac{l^2}{2r\Delta T} \tag{2.8}$$

where r is the radius of the bending beam, and l is the length of the beam. Assuming l << r, r can be expressed by the following equation [20], schematic shown in Figure 2-20.

$$r = \frac{2}{3}\frac{\frac{7}{4}(t_1+t_2)^2 - 2t_1t_2 + \frac{E_1b_1t_1^3}{E_2b_2t_2} + \frac{E_2b_2t_2^3}{E_1b_1t_1}}{\Delta\alpha\Delta T(t_1+t_2)} \tag{2.9}$$

where

E_i is the Young modulus,

α_i is the thermal coefficient of expansion,

$\Delta\alpha = \alpha_1 - \alpha_2$,

t_i is the thickness of the layer, and

b_i is the width of the layer.

The width of the structure does not affect the characteristics of the beam if different layer have the same width. The larger conversion factor γ can be obtained when $\Delta\alpha$ and l are large and t is small.

The calculation is carried out in Figure 2-21 and the result is shown in Figure 2-22. The maximum displacement of a 735 μm long beam at the temperature rise of 100 K is 133 μm, which matches the simulation result shown in Figure 2-24, and the measurement result as shown in Figure 2-26.

```
% Thermal Elastic Analysis, mathematica 5.0.

% t1 is the thickness of the SiO2 layer, unit is m
% t2 is the thickness of the AL layer, unit is m.


In[52]:= t2 := 1.8 * 10 ^ (-6)
         t1 := 0.6 * 10 ^ (-6)
         E1 := 0.74
         E2 := 0.69
         b1 := 40 * 10 ^ (-6)
         b2 := 40 * 10 ^ (-6)
         alfa1 := 0.4
         alfa2 := 23
         deltaalfa := alfa2 - alfa1
         deltaT := 100
         l := 750 * 10 ^ (-6)
         r =
          (2 / 3)
           ((7 / 4) * (t1 + t2) ^ 2 - 2 t1 * t2 + ((E1 * b1 * t1 ^ 3) / (E2 * b2 * t2)) +
              (E2 * b2 * t2 ^ 3) / (E1 * b1 * t1)) / (deltaalfa * deltaT * (t1 + t2))

Out[53]= 2.10324 × 10^-9

In[54]:= garma = l ^ 2 / (2 * r * deltaT)

Out[54]= 1.33722

In[55]:= d = garma * deltaT

Out[55]= 133.722
```

Figure 2-21: Calculation of initial deflection of the beam

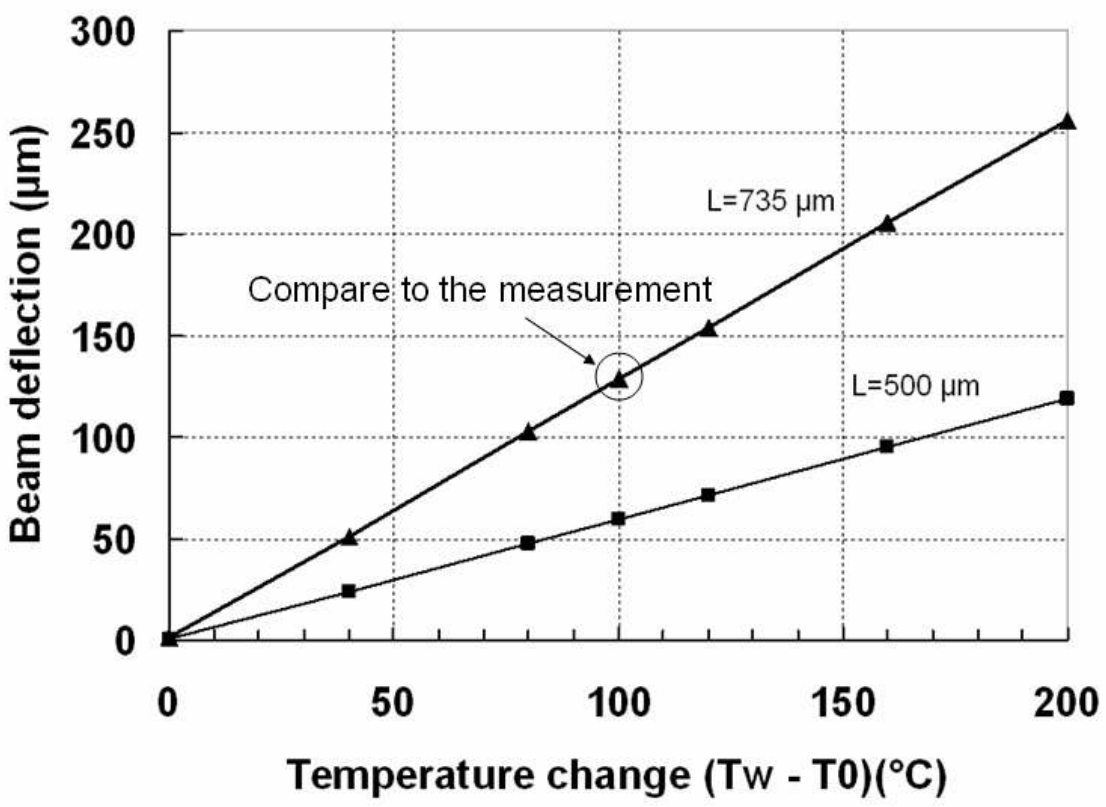


Figure 2-22: Beam deflection as a function of temperature change for bimorph beam

For a multilayer composite beam, the resultant beam length, the position of the neutral plane, and the curvation of the beam consisting of n layers can be found in [19].

$$L = L'(1 - \alpha_{eff}\Delta T) \tag{2.10}$$

where

$$\alpha_{eff} = \frac{E_1 t_1 \alpha_1 + E_2 t_2 \alpha_2 + ... + E_n t_n \alpha_n}{E_1 t_1 + E_2 t_2 + ... + E_n t_n} \tag{2.11}$$

where E_i, t_i and α_i are Young modulus, the thickness, and the coefficient of thermal expansion of the i'th layer, respectively. The position of the neutral plane is

$$Z_0 = \frac{E_1 t_1 (0 + Z_1) + E_2 t_2 (Z_1 + Z_2) + ... + E_n t_n (Z_{n-1} + Z_n)}{2(E_1 t_1 + E_2 t_2 + ... + E_n t_n)} \tag{2.12}$$

where $Z_i = \sum_{j=1}^{i} t_j (i = 1, 2, 3...., n)$ that is, the position of the bottom of the i'th layer.

Beams with various lengths and compositions are designed and laid out on chip. The initial beam tip displacements after postprocessing are measured from the SEM photo as shown in Figure 2-25 and Figure 2-26. The Coventor simulation results match the measurement of different beam structures as shown in Figure 2-23, Figure 2-24, and Figure 2-27. Coventor software is used to calculate the residual stress (internal stress) using the TCE model with zero stress temperature. The TCE model states that there is a zero stress temperature, which is the deposition temperature when the material is at no stress. As the material cools down to room temperature, the thermal contraction causes stresses. The initial displacement simulation specifies that the temperature of the part is 300 K. The solver returns the displacement and stress value. The material TCE and zero stress temperatures are found from AMI C5 process specification and listed in Table 2-9.

Table 2-9: TCE and zero_stress_temperature of materials

Parameters	**Aluminum**	**SiO_2**
TCE (1/k)	2.31 e-5	5e-7
Zero_stress_Temperature (K)	473	673

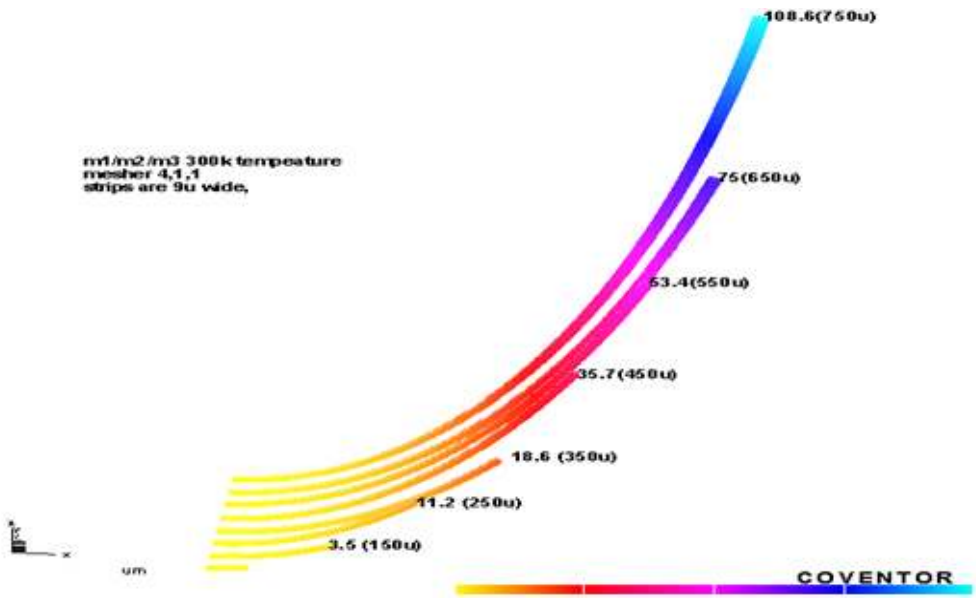


Figure 2-23: The initial displacement simulation result of various length beams with 300 K ambient temperature

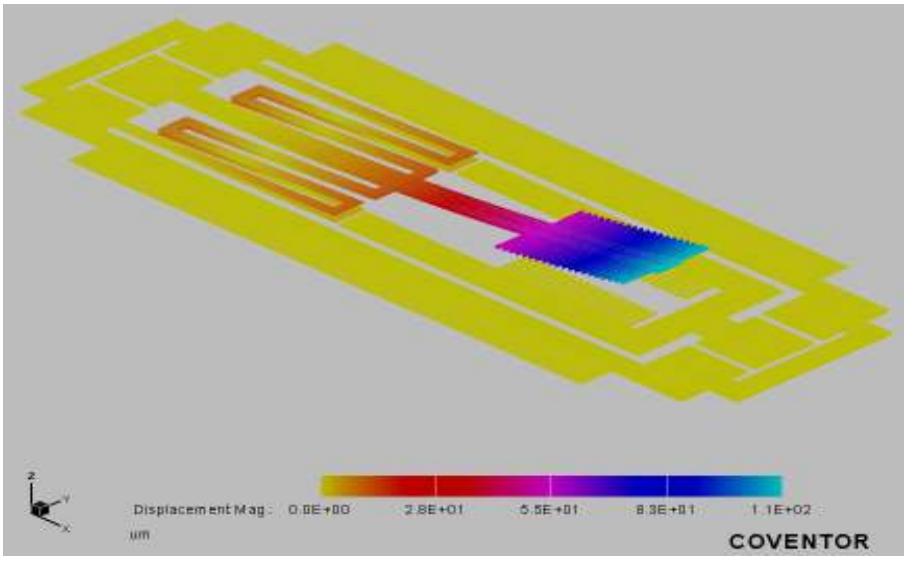


Figure 2-24: Coventor simulation of the initial displacement of a 80-finger RF MEMS switch with 300 K ambient temperature

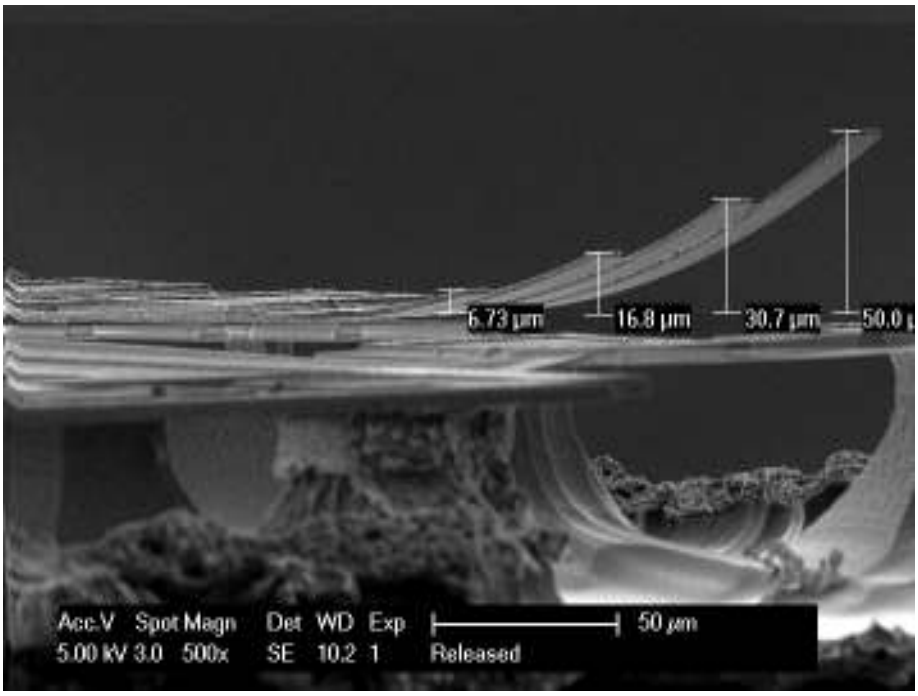


Figure 2-25:SEM photo and measurement of the M1/M2 metal strip

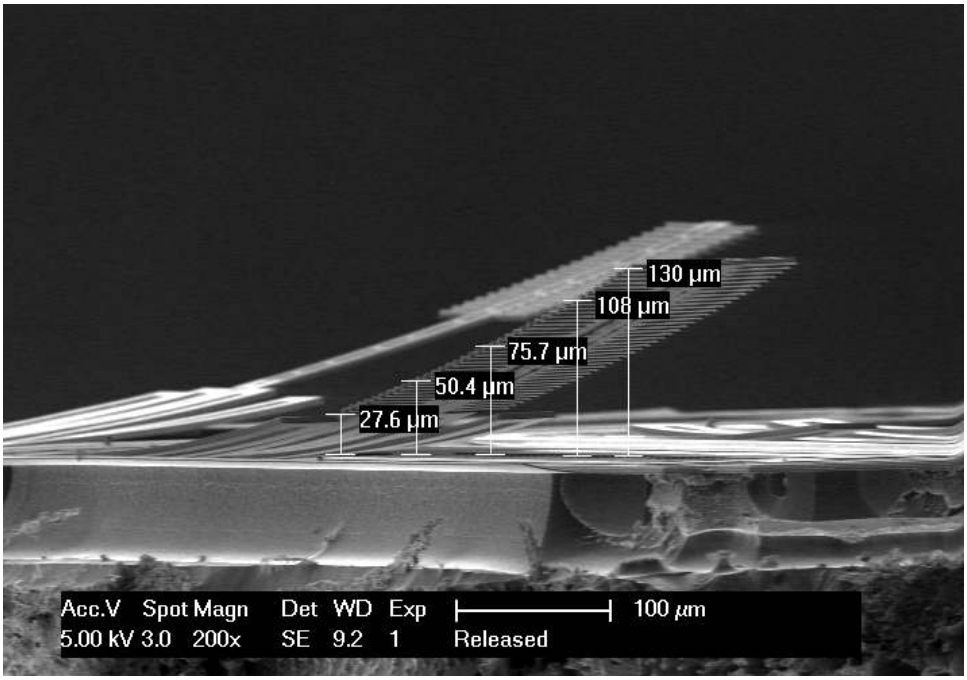


Figure 2-26: SEM photo and displacement measurement of the released 80-finger switch

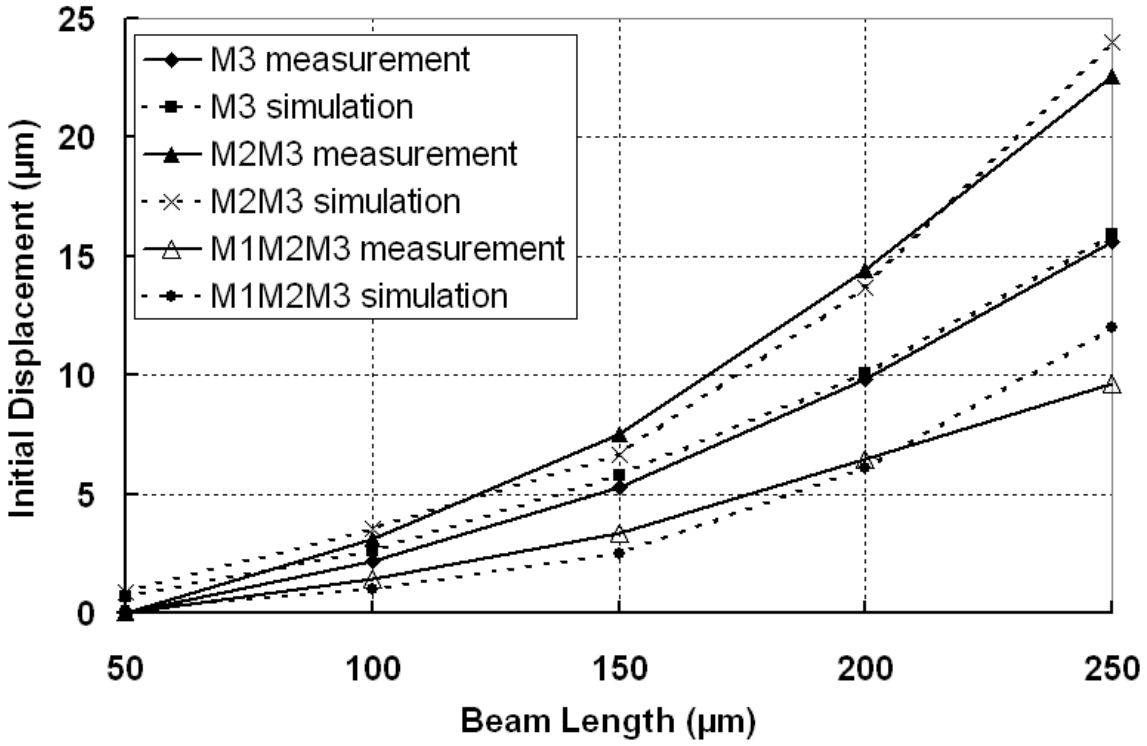


Figure 2-27: Simulation and measurement of the initial displacement with different beam composition and beam length

The theory, simulation, and experiment results of the initial displacement of a 735 µm beam are listed in Table 2-10.

Table 2-10: Initial displacement result comparison

	Calculated	**Coventer Simulation**	**Measurement**
Initial Displacement (µm)	133	115	130

The simulation was done using CoventorWare; the simplified beam structure without fingers was used for the simulation. The ambient temperature was 300 K, and the mesh model setting was shown in Figure 2-12. The result shows that the required temperature for the beam to be flat is around 400 K. The initial displacement is 103 µm. Both matched

the measurement results. Figure 2-28 shows the simulation model used with meshed element. The boundary condition for the simulation is shown in Figure 2-29.

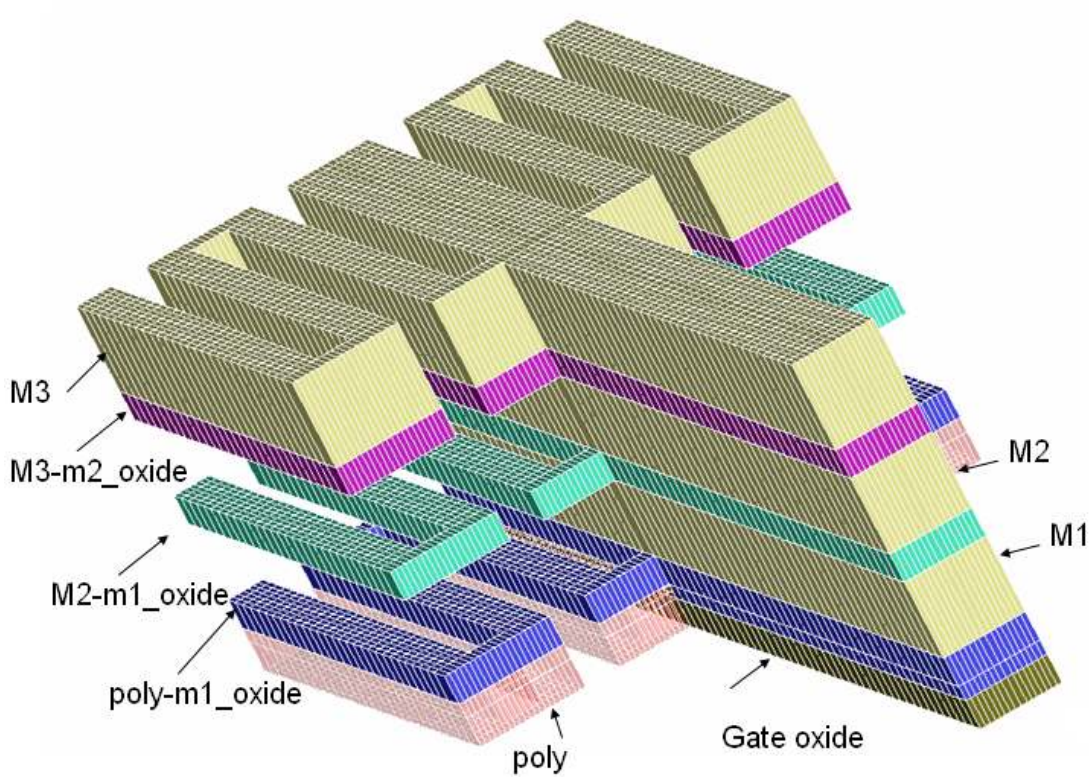


Figure 2-28: Coventor device model for tip displacement simulation after mesh (simplified, without fingers)

SurfaceBCs

SurfaceBCs	FixType	Patch1	and1	Patch2	and2	Patch3	LoadValue		Variable	Transient
Set1	fixAll	anchor	or	vin2	or	vin1	Scalar	0.0	Fixed	Fixed
Set2	fixAll	vout1	or	vout2	and	none	Scalar	0.0	Fixed	Fixed
Set3	Temperature	vin2	or	vin1	and	none	Scalar	300	Fixed	Fixed
Set4	Temperature	vout1	or	vout2	and	none	Scalar	300	Fixed	Fixed
Set5	Potential	vin1	or	vin2	and	none	Scalar	1	MechBC1	Fixed
Set6	Potential	vout1	or	vout2	and	none	Scalar	0.0	Fixed	Fixed

Figure 2-29: Coventor displacement boundary condition settings

Figure 2-30 shows the simulation result of beam tip displacement versus temperature for the 735 μm beam.

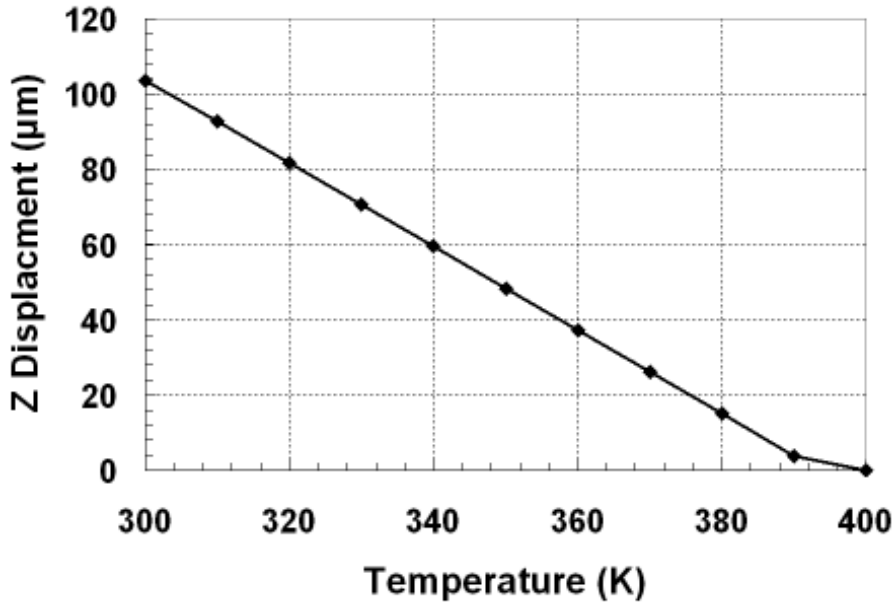


Figure 2-30: Coventor simulation result of maximum cantilever beam tip Z displacement versus temperature

2.2 Modeling of the RF MEMS Switch

2.2.1 Circuit Model of the MEMS Capacitive Switch

Modeling is an important part of the design process since it leads the direction for the design and predicts performance before fabricating the switch. Goldsmith used a simple variable capacitor suspended over a spring model [21], which did not acknowledge the serial resistance of the dielectrics, the transmission line, and the inductance due to the EM coupling. Buccella proposed a modeling method for the MEMS switch using the FEM and ALE methods. [22] However, the model is based on CPW and bridge type switch; it does not apply to the switch structure in this work.

In this section, an efficient electromagnetic model of the MEMS switch is created. The proposed model accounts for all the losses in the switch. The model is based on a finite element method. S-parameters of the switch are extracted from EM simulation using Ansoft High Frequency Structure Simulator (HFSS) [23], and a lumped circuit model is constructed. The lumped circuit model is verified by comparing it with the measurement. Figure 2-31 illustrates the equivalent RLC circuit of the MEMS switch overlapped on the physical structure. Figure 2-32 presents the first-order equivalent circuit model obtained for the capacitive MEMS switch.

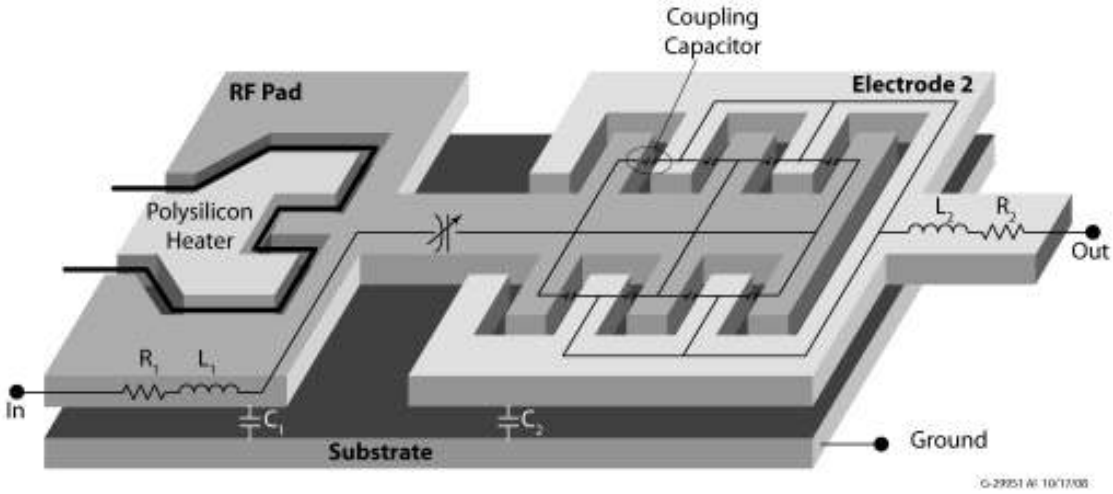


Figure 2-31: Switch diagram with RLC equivalent circuit

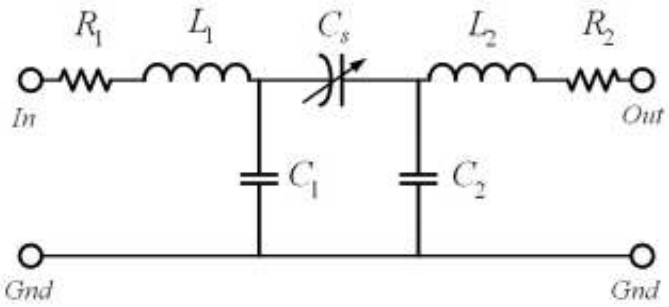


Figure 2-32: Equivalent-circuit model of the RF MEMS switch

As shown in Figure 2-32, the switch in this work is modeled as an RLC circuit. R_1 and R_2 represent the resistance of the support beam structure that carries the fingers [24]. The resistances can be calculated using the size of the structure and the sheet resistance of the material from the design library as shown in Figure 2-35. C_1 represents the capacitance between the rotor and the substrate, and C_2 represents capacitance between the stator and the substrate. L_1, and L_2 are the transmission line inductance. *Cs* is the capacitor between the fingers. Of all the components, C_2 is fixed for this design and can be represented using a mathematical equation. It is difficult to use a theoretical equation to present C_1 and *Cs* when the switch is in its OFF position; thus C_1, *Cs* and the

inductance L_1, L_2 are extracted from HFSS simulation results. C_1 and C_2 are obtained via single port HFSS simulation. Ansoft Q3D is used for beam-to-substrate capacitance value verification. Figure 2-34 shows the three HFSS models for the parasitic extraction simulation.

In this work, the full-wave electromagnetic simulation of the switch is done by a finite element method using Ansoft HFSS. The substrate model is high-resistive silicon with a dielectric constant of 11.9. The thickness of the substrate is 300 μm; silicon oxide is on top of the substrate and has the dielectric constant of 4.0. Y-parameters are extracted from the full wave analysis in the range of 1 GHz to 20 GHz. Both the On and Off states of the switch are simulated, and the capacitance is extracted from the Y11 parameter.

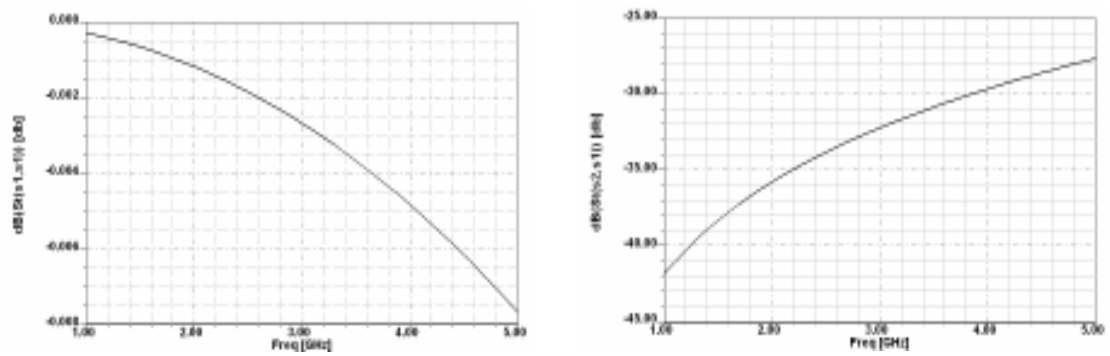
$$C = imag(Y_{11})/(2*\pi*freq) \tag{2.13}$$

where imag is the imaginary part of the result, freq is the frequency of interest, and Y1 (P1, P1) is the Y parameter measured from Port 1.

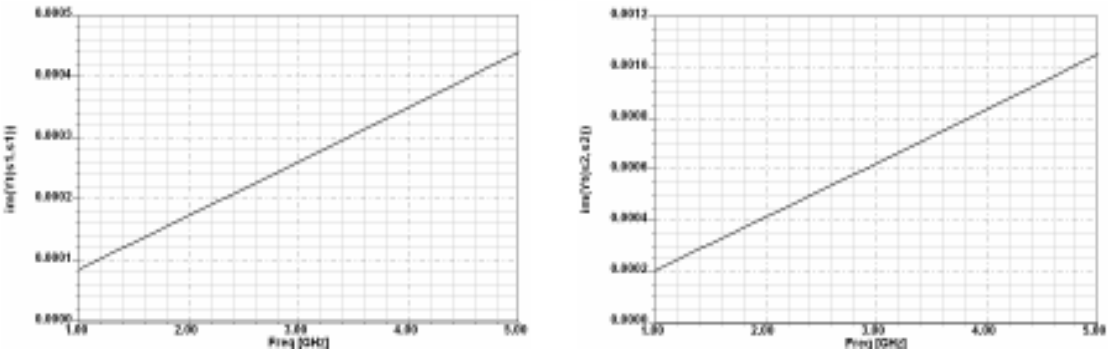
From the single port HFSS simulation (rotor and stator only), the inductance of the structure can be extracted from the Y parameters.

$$L_{nn} = -1/(2*\pi*freq*imag(Y_{nn})) \tag{2.14}$$

Figure 2-33 shows the HFSS simulation results of an 80-finger RF MEMS switch. The RLC model is extracted from these results.

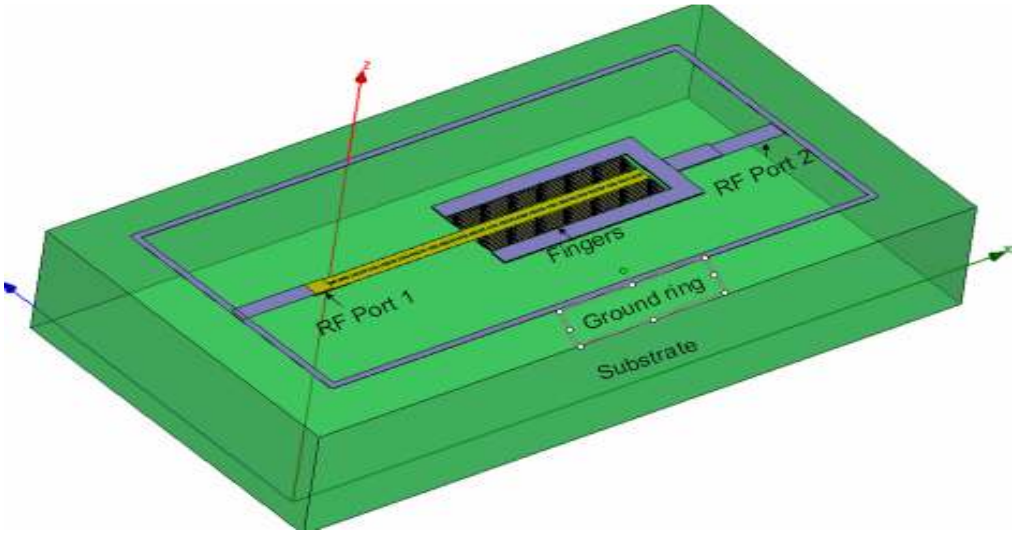


(a) S11 (b) S22

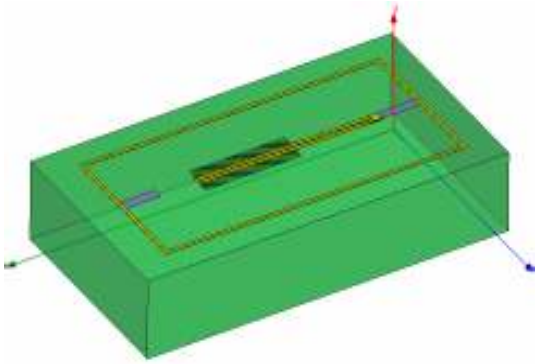


(c) Image (Y(11)) (d) Image (Y(22))

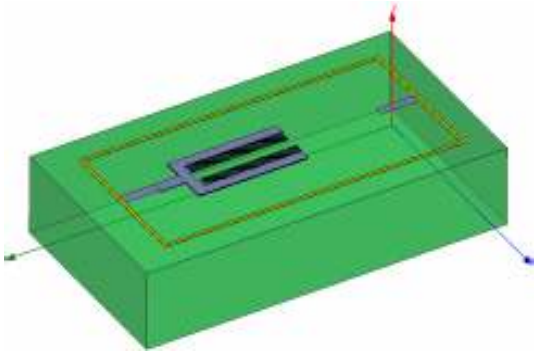
Figure 2-33: The HFSS simulation result of 80-finger RF MEMS switch ON



(a)



(b)



(c)

Figure 2-34: HFSS simulation model of RF MEMS switch for equivalent circuit model extraction (a) with both rotor and stator (b) rotor only (c) stator only

Table 2-11 gives the simulation result of the switch. Port 1 is the rotor and port 2 is the stator.

Table 2-11: Equivalent circuit model parameters of the 80-finger rf mems switch at 2 GHz

	L_1 (nH)	R_1 (Ω)	C_1 (pF)	Cs (pF)	C_2 (pF)	R_2 (Ω)	L_2 (nH)
Switch ON	0.42	0.63	0.016	0.5	0.019	0.25	0.27
Switch OFF	0.42	0.63	0.004	0.07	0.019	0.25	0.27

As shown in Figure 2-35, the resistances of the rotor and stator are calculated using the sheet resistance of the Al material from MOSIS AMI C5 process datasheet. The sheet resistance of the Al is 0.09 Ω/square, and the geometry of the rotor and stator beam is marked on the beam. Note that rotor is made of three layers of metal, so the calculated value is divided by 3 and listed in Table 2-11.

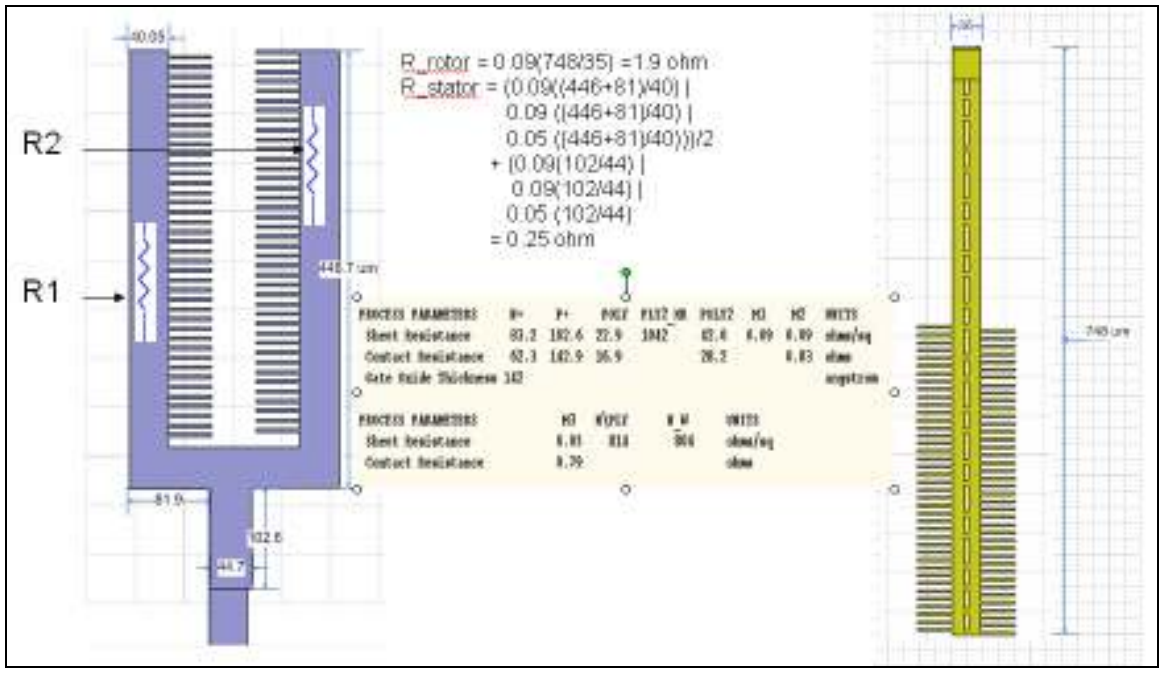


Figure 2-35: The calculation of R for RF MEMS switch

2.2.2 Switch Capacitance and Resonance Frequency Characterization

To characterize the capacitance of the designed switch, one simple 12 finger switch was used to simulate the switch EM response for different switch angles. Table 2-12 shows the design parameter for the EM modeling.

Table 2-12: Switch design specification

Finger gap	2 μm
Fingers	12
Finger engage length	20 μm
Finger length	25.5 μm (substrate), 24.5 μm (finger on beam)
Finger thickness	4.2 μm
Beam length	150 μm
First finger location	17 μm
Convergence	S= 0.02
Frequency sweep	0.1–20 GHz

The air gap capacitance is calculated as Cgap = Cm-air + Cd_air. The capacitances in up and down states are given by:

$$C_{on} = 2\varepsilon_D f_n L_e h_a / G_g \tag{2.15}$$

$$C_{off} = \sum_{i=1}^{f_n} \frac{2\varepsilon_D L_e w_{f_i}}{L_b \sin(\theta_i)} \tag{2.16}$$

where ε_D is the permittivity of dielectric material, where ε_D is the permittivity of dielectric material, and θ is the bending angle between the supporting beam and the substrate at the Off position. The fridge capacitors at the end of the fingers are not considered in these equations.

Figure 2-36 and Figure 2-37 show the isolation and return loss of the switch and capacitance value change corresponding to the switch beam tilt angle change.

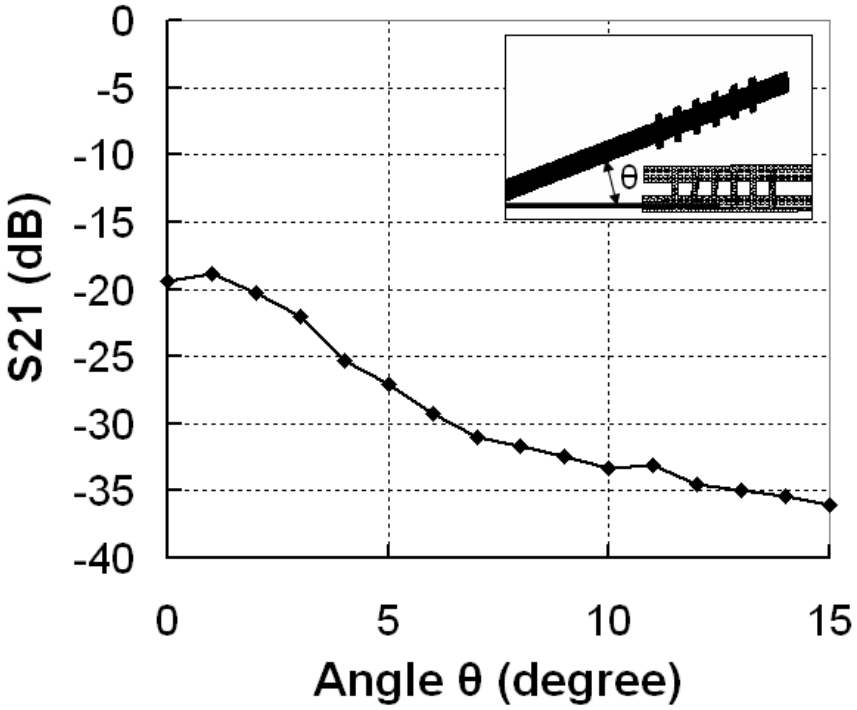


Figure 2-36: Isolation S21 with different tilt angle at 5.4 GHz 12-finger switch

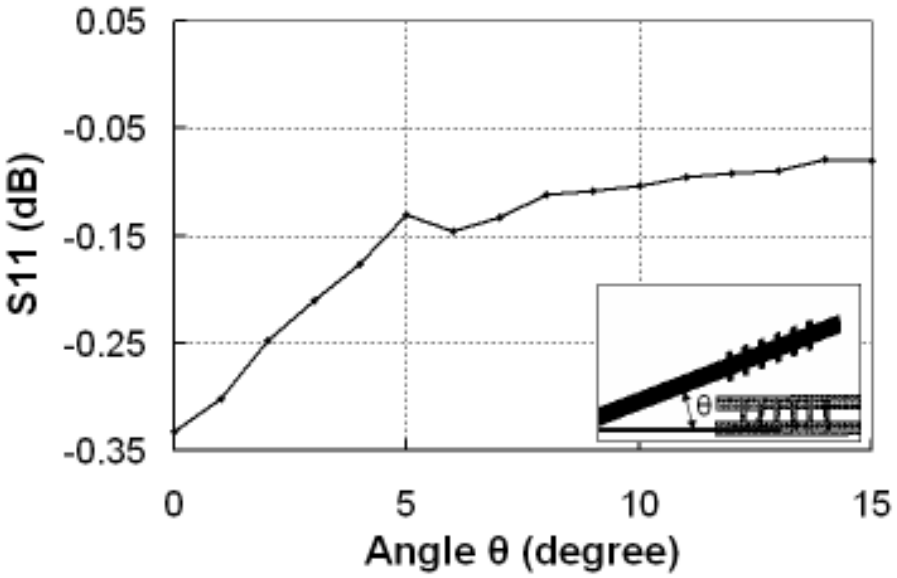


Figure 2-37: S11 versus angle at 5.4 GHz 12-finger switch

Figure 2-38 shows the capacitance change with the variation of the bending angle of the supporting beam of the switch. The initial bending angle is determined by the built-in stress of the bimorph beam. Thermal actuation voltage results in temperature change, which causes the beam to bend further down toward the substrate. The angle of zero corresponds to the flat position of the rotor.

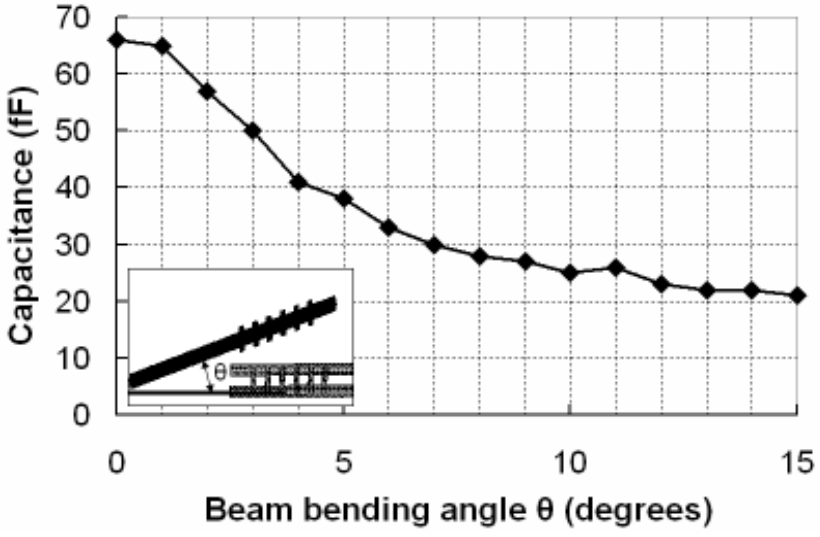


Figure 2-38: Simulation of the capacitance of the RF-MEMS switch with support beam angle change (12-finger device is shown at frequency of 2.4 GHz)

Figure 2-39 shows the electrical field distribution when the switch is in its ON position. The maximum electrical field is between the coupled fingers as expected. When the switch is moving from the ON to OFF position, the electrical field concentration moves to the substrate [24].

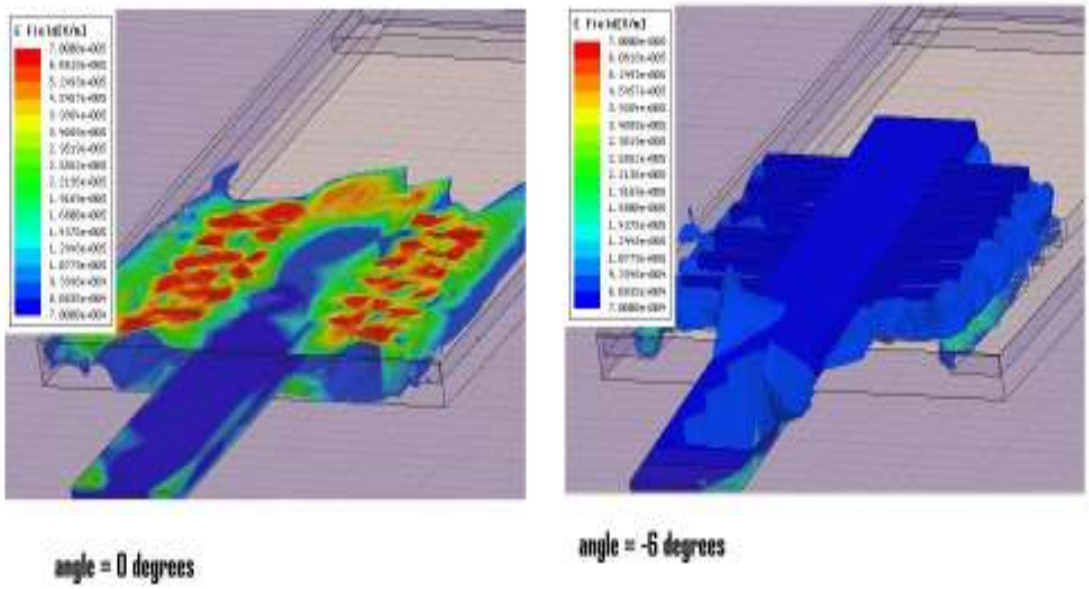


Figure 2-39: Field distribution of the RF MEMS switch at the on/off position

Figure 2-40 shows the RF MEMS switch measured self-resonant frequency is 8.78 GHz. The self-resonance frequency is determined by L_1 , L_2 , C_1 , and C_2 .The Y parameter was converted from the measured full 2-port S parameters of the 80-finger device. The self-resonance frequency can be optimized by altering the size of the stator and rotor.

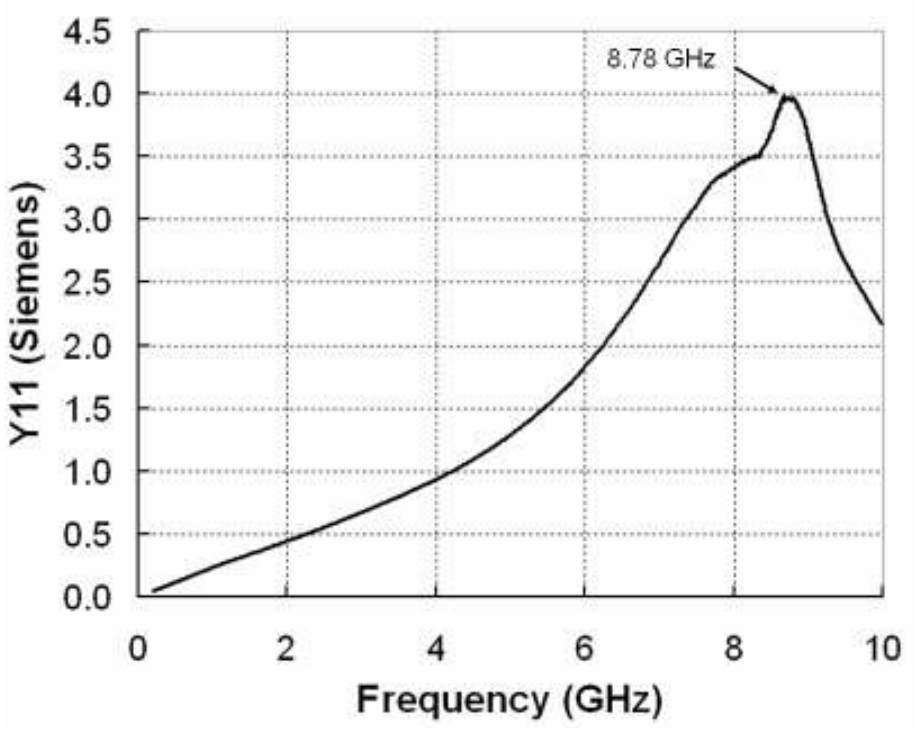


Figure 2-40: Self-resonance frequency of the 80-finger RF MEMS switch after release [24]

2.3 Novel MEMS CAD Design Flow

Because of the complexity of the MEMS design, CAD tools have to be used to perform various analyses in multiple physical domains. This section gives a review of the MEMS CAD tools used and a novel design flow for RF MEMS design.

2.3.1 Mechanical and Thermal Analysis Tool

In this work, CoventorWare [25] is used for the thermal actuation voltage analysis and mechanical displacement analysis. The input of the tool is the fabrication process data and material property of each layer. The design layout is imported directly from the Cadence layout tool. Then the definition of the fabrication flow is defined and used to generate a two- and three-dimensional solid model, followed by meshing the structure, analysis, and detailed simulation of the meshed model. Optionally a reduced order system level model can be derived.

Normally, the first step is to create a two-dimensional layout of a MEMS design using Coventor Designers' layout editor, which is a full-featured, two-dimensional mask-drawing tool capable of all-angle generators. Layout creates a .cat format file and supports the format used by other layout software such as GDS II, CIF, IGES, and DXF. In the second step the fabrication steps for a MEMS device are defined and emulated. The process editor supplies the information needed to create a three-dimensional MEMS model from the two-dimensional mask information provided by the layout editor. The depth information is defined by the various material layers in a sequence of deposit and etching steps with control of bulk and thin-film geometries. Materials for each process layer for the MEMS device are chosen from a material property database. The material properties include elasticity, stress, density, viscosity, conductivity, dielectric, piezoelectric, and thermal characteristics. The fabrication process parameters are defined by material thickness, deposition type (stacked, conformal, or planar), sidewall profiles of angular slope, mask parameter offset, and mask polarity.

Once the layout and fabrication process flow have been generated, the Coventor Solid Model tool is used to build a three-dimensional model using the two-dimensional layout geometry from the mask files and the deposit/etch and thickness information from the fabrication process file.

The next step performs the finite element model creation and meshing of the device. The meshing tool creates a three-dimensional mesh based on the model created by the solid model tool and the process file created by the process editor. The user can choose among various mesh elements such as tetrahedral, bricks, and hexahedral according to the device geometry. The result is stored in a file containing all model input and output

parameters such as the geometry and material properties, conductors and dielectric types, and the mesh information used by the various simulation solvers.

The analyzer tool is the core of the CoventorWare, consists of various solvers such as MemCap, MemMech, CoSolveEM, and SimMan. The tools used in this work are MemCap, MemMech, and CoSolveEM. MemCap is the electrostatic solver that computes a charge matrix based on voltage conditions or a voltage matrix based on charge conditions for the MEMS design under investigation. Secondary effects such as fringe capacitances and the influences of a lossy media on the electric behavior can be simulated as well.

- MemMech is the mechanical solver that analyzes structural, displacement, modal, harmonic, stress, and contact steady-state thermomechanical structure. MemMech can be used for computation of the thermal field and the electrical potential resulting from an imposed voltage and current flow through a resistive material. The joule heating effect results can be used to compute displacement and stresses due to thermal expansion.
- CoSolveEM is a coupled electromechanical solver that combines the electrostatic and mechanical solutions. It also can perform pull-in voltage and hysteresis analysis efficiently in one sweep.
- MemThrerm is an electrothermal solver that computes the potential drop through a resistor resulting from a voltage and/or current flow and the resulting temperature distribution from joule heating.
- MemTrans is the transient analysis solver that computes transient thermal and mechanical deformation and stresses.

Two different solvers offer thermal analysis capabilities:

- MemMech, the mechanics solver, can be set for steady state or transient thermal or steady-state thermomechanical analysis. It also supports analysis of film convection effects.
- MemETherm, the thermo-electromechanical solver, is a special solver that computes the thermal field and the electrical potential resulting from an imposed voltage and/or current flow through a resistive material.

Another CAD software, ANSYS, is used for electrostatic pull-in voltage analysis. ANSYS is capable of structural, vibration (modal, harmonic, and transient), thermal, acoustic, fluidic, electromagnetic, and piezoelectric analyses (or combinations of these). While not specifically written for the simulation of MEMS, many of these analyses apply equally well in the microdomain, and as such, ANSYS has been widely used throughout the MEMS community.

ANSYS is used to simulate micromechanical behavior in this work. It allows CIF files to be imported, thus enabling MEMS designs to be input from other software packages.

ANSYS simulations are generally performed in three stages. The first is carried out in the preprocessor and defines the model parameters (that is, its geometry, material properties, degrees of freedom, boundary conditions, and applied loads). Next is the solution phase, which defines the analysis type, the method of solving, and actually performs the necessary calculations. The final phase involves reviewing the results in the post-processor [26]. The work is detailed in Appendix A.

2.3.2 Electromagnetic Analysis Tool

In this work, the Ansoft HFSS™ is used for inductor quality factor analysis and switch on/off RF characteristic analysis. HFSS is 3-D full-wave electromagnetic field simulation software for S-parameter, full-wave SPICE™ extraction and 3-D electromagnetic field simulation of high-frequency and high-speed components. [23]

In this work, the equivalent circuit model is verified by using the Ansoft Q3D Extractor®. The Ansoft Q3D is a 3-D parasitic extraction software tool for engineers designing multilayer boards, complex IC packages, and 3-D on-chip passive components. The Q3D Extractor performs the 3-D and 2-D electromagnetic-field simulation required for the extraction of RLCG parameters from an interconnect structure and automatically generates an equivalent SPICE subcircuit model. These models can then be used to perform signal integrity analysis to study EM phenomena. [27]

2.3.3 The Design Methodology of the RF MEMS Switch

The design methodology of the MEMS switch design is shown in Figure 2-41. There are two parts of the switch design: electrical domain and mechanical domain. There are different tools for each domain analysis, and the results are fed back to each domain for cross-domain optimization. First, the switch parameters are estimated from theoretical analysis; then the cadence layout tool virtuoso is used for the implementation. The GDSII netlist is taken by MEMS cad tool CoventorWare along with the AMI C5 process data, and the 3-D model is created and meshed. Then HFSS is used for the EM simulation, and CoventorWare is used for coupled electro-thermal-mechanical simulation. The simulation result of displacement is fed to HFSS for switch-off condition simulation. The HFSS outputs S-parameters in touchstone format. The S-parameters of the switch are used by

cadence circuit simulator SpectreRF for RF circuit simulation, for example, VCO and filter circuits. The transient simulation and phase noise analysis were performed using the cadence SpectreRF simulator.

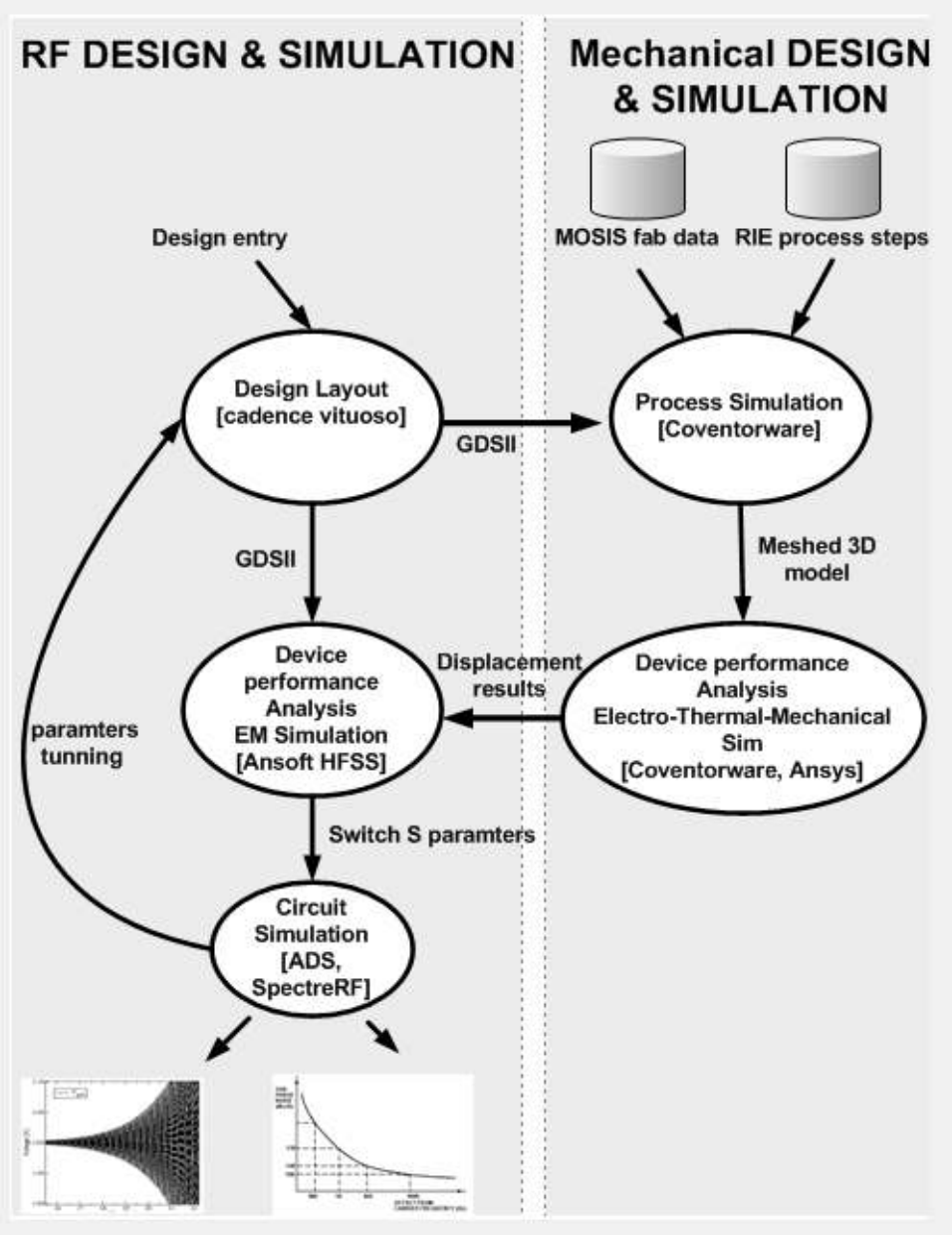


Figure 2-41: RF MEMS switch thermal and mechanical CAD design flow

2.4 Summary of Switch Design and Modeling

This chapter described the design and modeling of the novel ET switch. First, the electrothermal actuation analyses were given and the optimization of the thermal actuator geometry was carried out. Second, the mechanical deformation of the cantilever beam was analyzed with different temperature input. Thirdly, the design and simulation methodology of RF MEMS switch using industrial CAD software were given. And last, a complete electrical model of the ET switch was derived using FEM simulation results.

Chapter 3 — CMOS Compatible Fabrication Process of ET-Switch

This chapter introduces the fabrication technology and postprocessing techniques used in developing the ET-Switch. CMOS technology is the most widely used technology in the current integrated circuit industry because of its low power, high performance, and high level of integration capabilities. Industry-standard CMOS fabrication steps are used for the chip fabrication, and CMOS-compatible postprocessing techniques are used for releasing the MEMS structure. The following sections give the details of each step.

3.1 CMOS-MEMS Technology

Even though MEMS technology is promising for many integrated electronics applications, many MEMS processes are not compatible with standard IC processes. The non-CMOS-compatible MEMS processes often require complex fabrication sequences and special micromachining techniques. All of those special requirements lead to high cost and low yield.

CMOS-MEMS technology enables the integration of the MEMS functionality with analog and digital electronics all in a single chip. Unlike other MEMS manufacturing technologies, CMOS MEMS employs standard CMOS processes to fabricate microstructures within the metal-dielectric layers that are deposited during the standard CMOS processing flow. CMOS compatibility provides high yields and low cost due to the batch fabrication. There are three types of process methods: pre-CMOS, post-CMOS, and intermediate-CMOS, depending on whether the additional fabrication steps precede, follow, or are performed in between the regular CMOS steps [28].

CMOS process-compatible implies that the postprocess temperature cannot exceed 400° C. Because the CMOS circuit normally uses power supply around 5 V, low voltage

actuation is part of CMOS-compatible consideration. There are different ways to achieve low voltage actuation, such as increasing the area of actuation, decreasing the gap between the switch and the bottom electrode, and using the low spring constant structure. Increasing the actuation area is not practical, and reducing the gap between the switch and the bottom electrode will degrade the return loss. Fedder and Xie defined a CMOS-compatible process to implement the MEMS beam structure [29] [30]. The uniqueness of this process is that no etching mask is required. The actuation voltage is 11 V for that particular design. Thermal actuation is another choice because of its high reliability, Brand proposed a thermal actuated method that is also maskless and used polysilicon stripes for heating purposes [15]. A wet etching EDP method is used in that work. Another CMOS-compatible process is proposed in [31], where surface layer copper is used for the etching mask and wet etching Cu is used for electroplating of the sacrificial layer. Guillou [32] proposed a RIE method similar to that of G. Fedder. CHF_3/O_2 and SF_6/O_2 are used for SiO_2 and Si etching. Ericssion [33] proposed a micromachining method that is also CMOS postprocess compatible.

3.2 Common CMOS Micromachining Processes

This section lists some of the common micromachining processes for defining MEMS structure. Oxidation, sputter deposition, and evaporation are mostly used.

- **Oxidation:** High-quality silicon dioxide is obtained by oxidizing silicon in either dry oxygen or in steam at elevated temperature. Thermal oxidation of silicon generates compressive stress in the silicon dioxide film. As a result, thermally grown oxide films thicker than one micrometer can cause bowing of the

underlying substrate. Moreover, freestanding membranes and suspended cantilevers made of thermally grown silicon oxide tend to wrap or curl.

- **Sputter deposition:** A target object made of a material to be deposited is physically bombarded by a flux of inert ions in a vacuum chamber. There are three classes of sputter tools: DC glow discharge, planar RF, and cylindrical magnetron (s-gun).
- **Evaporation:** This involves the local heating of a target material to a sufficiently high temperature in order to generate a vapor that condenses on a substrate. Poor step coverage, leaving corners and sidewalls exposed and thin films deposited by evaporation exhibiting high tensile stresses increase with a higher material melting point. For example, evaporated tungsten or nickel films can have stress in excess of 500 μpa that is sufficient to cause curling or even peeling. Raising the deposition temperature of the substrate reduces stress.

The common etchant and etching methods for Silicon and SiO_2 are described below:

- Etching of silicon
  - Fluorine, chlorine, and bromine processes are standard for silicon etching, resulting in reaction products SiF_4, $SiCl_4$, and $SiBr_4$, respectively. Fluorine processes are safer to use, but they are seldom fully anisotropic. Chlorine and bromine processes inherently result in vertical sidewalls. However, these two gases are highly toxic, and the equipment for Cl_2 and HBr etching must be equipped with a loadlock. Loadlocks complicate system operation but simultaneously improve repeatability since the reaction chamber is not exposed to room air and humidity.
  - SF_6- and CF_4-based processes typically have 10% to 40% oxygen added. Oxygen has several roles: it reacts with SFn and CFn fragments and keeps fluorine concentration high by preventing fluorine recombination with the fragments. Oxygen etches resist and contributes to sidewall film formation by oxidation and their effect on resist consumption.
  - CHF_3 is used as oxide etching gas when selectivity against silicon is required. It provides fluorine and carbon for etching (SiF_4, CO_2 etch products) and CF_2 radicals, which are polymer precursors. Polymerization takes place on silicon surfaces and on oxide surface. $(CF_2)n$ polymerization does not take place due to oxygen supply. Ion bombardment-induced reactions on oxide result in CO_2 formation.
- Etching of silicon dioxide

  Silicon dioxide etching is driven by ion bombardment. Therefore, isotropic plasma etching of oxide is difficult, but high enough radical concentration will

result in reasonable isotropic etch rates. Any fluorine-containing gas can be used as an etchant for oxide, for example, CF_4 or SF_6. However, both gases etch silicon, and they are suitable for nonselective etching only.

A disadvantage of wet etching is the undercutting caused by the isotropy of the etching process. The purpose of dry etching is to create an anisotropic etch – meaning that the etching is unidirectional. An anisotropic etch is critical for high-fidelity pattern transfer. RIE etching is one method of dry etching. Figure 3-1 shows a diagram of a common RIE setup. An RIE consists of two electrodes (1 and 4) that create an electric field (3) meant to accelerate ions (2) toward the surface of the samples (5).

The area labeled (2) represents plasma that contains both positively and negatively charged ions in equal quantities. These ions are generated from the gas that is pumped into the chamber. In the Figure 3-1, CF_4 has been pumped into the chamber, making plasma with many Fluorine (F-) Ions.

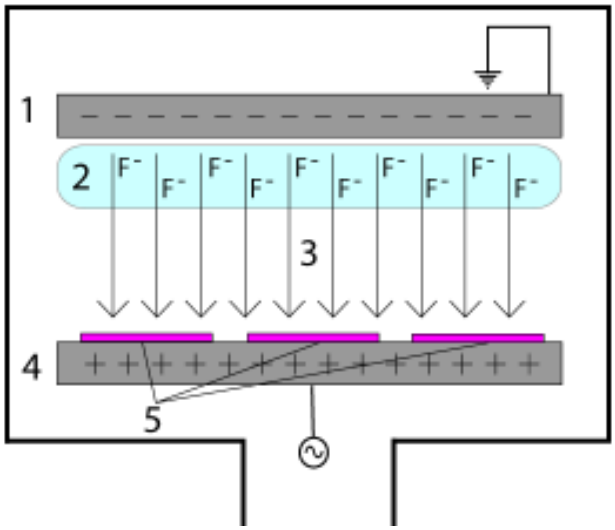


Figure 3-1: RIE theory diagram

The fluorine ions are accelerated in the electric field, causing them to collide with the surface of the sample. A hard mask is used to protect certain areas from etching, exposing only the areas desired to be etched.

Figure 3-2 shows a photoresist mask on silicon dioxide. The etching ions are accelerated into the etching region where they combine with silicon dioxide and are then dispersed. Because the electric field accelerates ions toward the surface, the etching caused by these ions is much more dominant than the etching of radicals. Ions travel in various directions, so the etching is anisotropic.

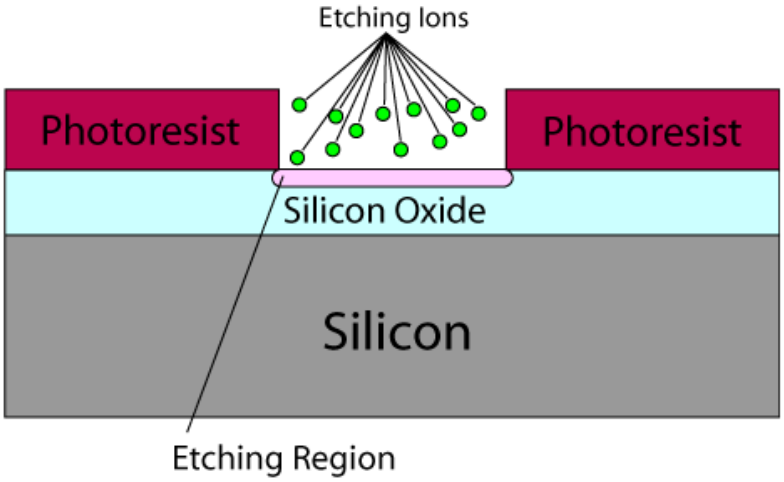


Figure 3-2: RIE etching diagram

The etch chemistries used to etch various substrates are listed in Table 3-1.

Table 3-1: Etch chemistries of different etch processes

Material Being Etched	**Etching Chemistry**
Deep S_i trench	$HBr/NF_3/O_2/SF_6$
Shallow S_i trench	$HB_r/Cl_2/O_2$
Poly S_i	$HB_r/Cl_2/O_2$, HB_r/O_2,BCl_3/Cl_2, SF_6

Al	BCl_3/Cl_2,S_iCl_4/Cl_2, HB_r/Cl_2
S_iO_2	CF_4/CHF_3/Ar, C_2F_6, C_3F_8,C_4F_8/CO_2 C_5F_8, CH_2F_2
Si_3N_4	CHF_3/O_2, CH_2F_2, CH_2CHF_2

3.3 Fabrication of the RF MEMS Switch

The RF MEMS switches are fabricated using AMI C5 (0.6 μm) technology. The process is a three-metal, two-poly process. The cantilever microstructure is realized using anisotropic and isotropic dry etches. The top-level metal is used as an etch-resistant mask to define the microstructures. The process conditions are listed in Table 3-2.

Table 3-2: The AMI process data

	Thickness (μm)	**Process**	**Temperature (Degree C)**
Passivasion	1	Plasma	400
M2 Al	1.15	Deposit	200
M1-M2 Oxide	0.65	Plasma	400
M1 Al.	0.6	Deposit	200
Poly-M1 Oxide	0.85	CVD Oxide	800
Poly2	0.4	Deposit	n/a
Ploy1-Poly2 Oxide	0.4	CVD Oxide	800
Poly1	0.4	Deposit	n/a
Field Oxide	0.6	Thermally Grown	1000

Note: From AMI data sheet.

The CMOS process is a 22-step process, modeled closely to the AMI C5 process. The chip is fabricated through MOSIS AMI C5 process and postprocessed with CMOS-compatible RIE micromachining steps. Figure 3-3 shows the coventor process definition for the whole fabrication and postprocessing steps [34].

Number	Step Name	Action	Layer Name	Material Name	Thickness	Mask Name
0	Substrate	Substrate	Substrate	SILICON	300	DIE
1	Planar Fill	Planar Fill	GateOxide	OXIDE	0.04	
2	Straight Cut	Straight Cut				G_OX
3	Planar Fill	Planar Fill	Poly1	POLYSILICON	0.4	
4	Straight Cut	Straight Cut				Poly1
5	Conformal Shell	Conformal Shell	Interpoly	OXIDE	0.07	
6	Straight Cut	Straight Cut				InterPolyOxide
7	Conformal Shell	Conformal Shell	Poly2	POLYSILICON	0.4	
8	Straight Cut	Straight Cut				Poly2
9	Conformal Shell	Conformal Shell	M1_P2_OX	OXIDE	0.9	
10	Straight Cut	Straight Cut				M1_p1_oxide
11	Conformal Shell	Conformal Shell	M1	ALUMINUM	0.6	
12	Straight Cut	Straight Cut				METAL1
13	Conformal Shell	Conformal Shell	M1_M2_OX	OXIDE	0.65	
14	Straight Cut	Straight Cut				M1_M2_OX
15	Conformal Shell	Conformal Shell	M2	ALUMINUM	0.65	
16	Straight Cut	Straight Cut				METAL2
17	Conformal Shell	Conformal Shell	M2_M3_OX	OXIDE	0.65	
18	Straight Cut	Straight Cut				M2_M3_OX
19	Conformal Shell	Conformal Shell	M3	ALUMINUM	0.67	
20	Release HF Etch	Delete		PSG		
21	Reactive Ion Etch (RIE)	Straight Cut				METAL3
22	Release Dry Etch	Delete		SILICON		

Figure 3-3: Process defined in Coventor process editor

3.4 CMOS-Compatible Postprocess Steps

The postprocess is based on surface micromachining; the process is CMOS-compatible because it only requires low temperature postprocesses. However, the dielectric buckles and bends due to its large intrinsic stress. Both cantilever and membrane can be defined using this process. Shunt or series switches are both possible.

- The key to the process is the use of the CMOS metallization as an etch-resistant mask to define the microstructures.

- Conventional CMOS processing is followed by a sequence of maskless dry-etching steps.
- Laminated structures are etched out of the CMOS silicon oxide, silicon nitride, and aluminum layers.
- A minimum beam width and gap of 1.9 μm and maximum beam thickness of 4.2 μm are fabricated in a 0.5 μm three-metal CMOS process available through MOSIS.
- Cantilever structures slightly curl up with a radius of curvature of about 4.2 mm because of the built-in stress during fabrication and different thermal expansion coefficients of different layers.

A CMOS MEMS process similar to that of Carnegie Mellon University is developed. [29] The top-level metal is used as an etch-resistant mask to define the microstructures.

1. An anisotropic RIE with CHF_3 and O_2 removes silicon oxide not covered by top-level metal.
2. CHF3/O_2 (SiO_2) exposes the S_i.
3. An isotropic RIE process using SF_6 is used to remove the bulk silicon to release the cantilever beam structure.
4. The heater is implemented using a polysilicon layer.

The postprocessed structure exhibits bending because of the different thermal expansion coefficient of the beam structure composed of CMOS metal and dielectric layers. This bending is actually an advantage in this particular application. The bend-up position is considered the switch-off position, while the press-down position is

considered the switch-on position. Metal layers 1, 2, and 3 are used to construct the device with a thickness of 4.2 μm.

For all postprocessing steps, the chips are mounted to silicon carrier wafers using diffusion pump oil to provide thermal heat sink for the chips. The silicon carrier wafers are kept cool during each etching step through Helium back-side cooling within the etching chambers. The first step is to remove the SiO_2 over-glass from the surfaces and from between the fingers. The Panasonic E640 Inductively Coupled Plasma (ICP) etching chamber is used for this part of the process. The top layer metal is used as the etching mask. The details of each step are summarized in Table 3-3 [14].

Table 3-3: Postprocess steps of RF MEMS switch

	Oxide Etch Step 1	**Oxide Etch Step 2**	**Silicon Etching**
Gas Flow [Sccm]	CHF3 40	CHF3 40	SF6: 100; Ar: 40
Pressure	0.3 Pa	0.5 Pa	23 mT
Power [W]	ICP: 900 Substrate: 100	ICP: 900 Substrate 200	RF: 9 ICP: 825
Etch Time [Sec]	1920	300	540

The first-step process conditions are as follows: Bias power to the substrate is 100 W to minimize pad etching while maintaining a moderate etching rate of SiO_2; time: 32 minutes; pressure: 0.3 Pa; ICP power: 900 W; Gas: CHF3; flow rate: 40 sccm. After this etch is completed, there is still some SiO_2 remaining between the fingers. A higher bias power of 200 W is used to assist with the deeper etching between the fingers. A pressure of 0.5 Pa was also used to maximize the etch rate for these conditions. The time

is 11.5 minutes, and the other process parameters are unchanged. The depth of total removed SiO_2 is 4.2 µm. Figure 3-4 and Figure 3-5 shows the SEM photo of the structures after the first release step.

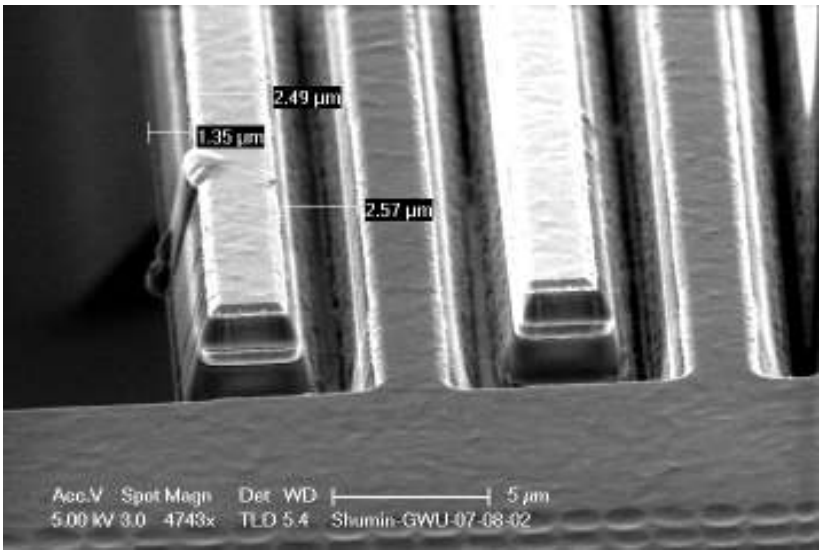


Figure 3-4: SEM of fingers after oxide etching and before release etch

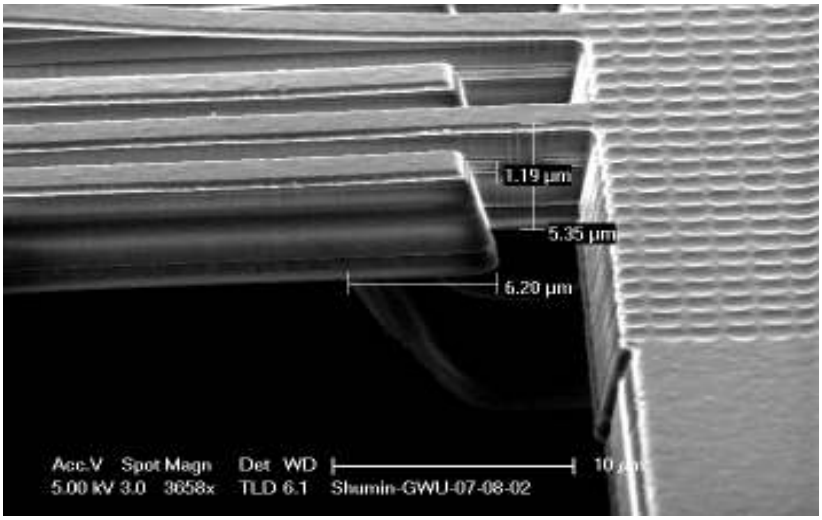


Figure 3-5: Finger SEM after oxide etching before release etching

The second step is to etch the silicon under the structure and release the cantilevers. It is performed using a Plasma-therm 770 SLR ICP etching system. The substrate temperature is 10º C; time: 9 minutes; pressure: 23 mT; ICP power: 825 W; sample bias

power: 9 W; gas: SF6/Ar; flow rates: 100 sccm/40 sccm. Figure 3-6 is the SEM photo of the released device. About 65 μm of silicon was removed at the end of this process step, and the structure was fully released. After the release, the switch is at its OFF state.

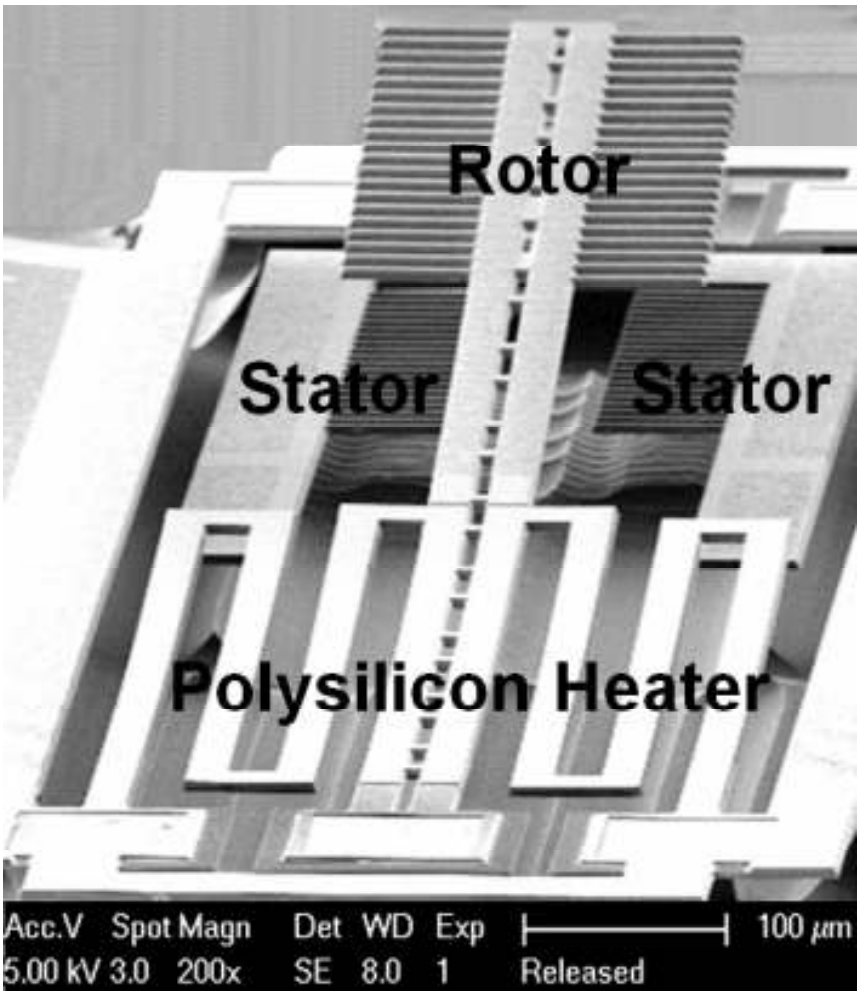


Figure 3-6. SEM photo of the ET-Switch after RIE release

The postprocessing of this device is done at The University of California, Santa Barbara Nanofabrication Facility. The URL is http://www.nanotech.ucsb.edu/.

3.5 Summary

This chapter provided the details of the fabrication technology and the postprocessing sequence in developing the ET-Switch in this research. The CMOS-MEMS concept and

general practices were explained, and a two-step maskless RIE process was deployed to release the design structures.

Chapter 4 — Measurements and Characterization of ET-Switch

Experimental characterization of the ET-Switch includes the test of the electrical, mechanical, and thermal characteristics. The following sections describe the procedure of characterizing the ET-Switch and results. The switch is characterized in the following areas: initial displacement, on/off capacitance and capacitance ratio, insertion loss and isolation, power consumption for switch on/off operation, and the on/off thermal actuation threshold voltage.

4.1 Initial Displacement Testing of the MEMS Switch

The initial displacement of the released structure is measured using the SEM system from FEI company [35].

After RIE postprocessing step of the cantilever beam, the beam is deflected upwards due to internal built-in stress. In the CMOS technology used, metal 3 is the topmost metal layer, followed by metal 2 and metal 1, which is the bottom layer of metal. All structures are 9 μm wide. Figure 4-1 shows the measured result of the deformed bimorph release beam structure, which has metal 1 and metal 2 combinations.

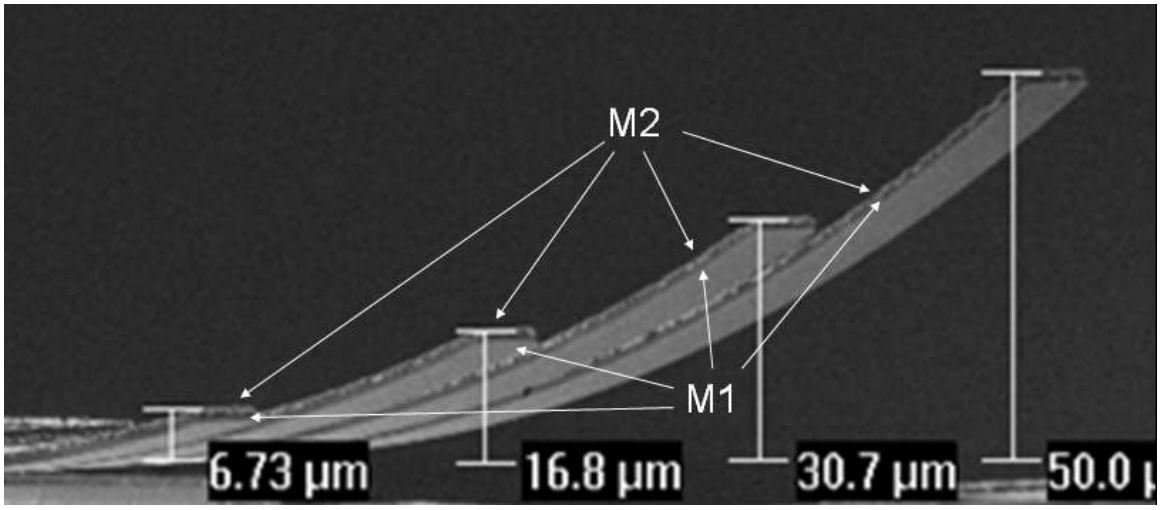


Figure 4-1: SEM photo of metal 1, 2 beams initial deformation measurements [36]

Figure 4-2 shows the measurement result of the released switch. The length of the beam is 738 μm, and the displacement is 130 μm at the tip. The measurement was done in nanofabrication lab of University of California, Santa Barbara.

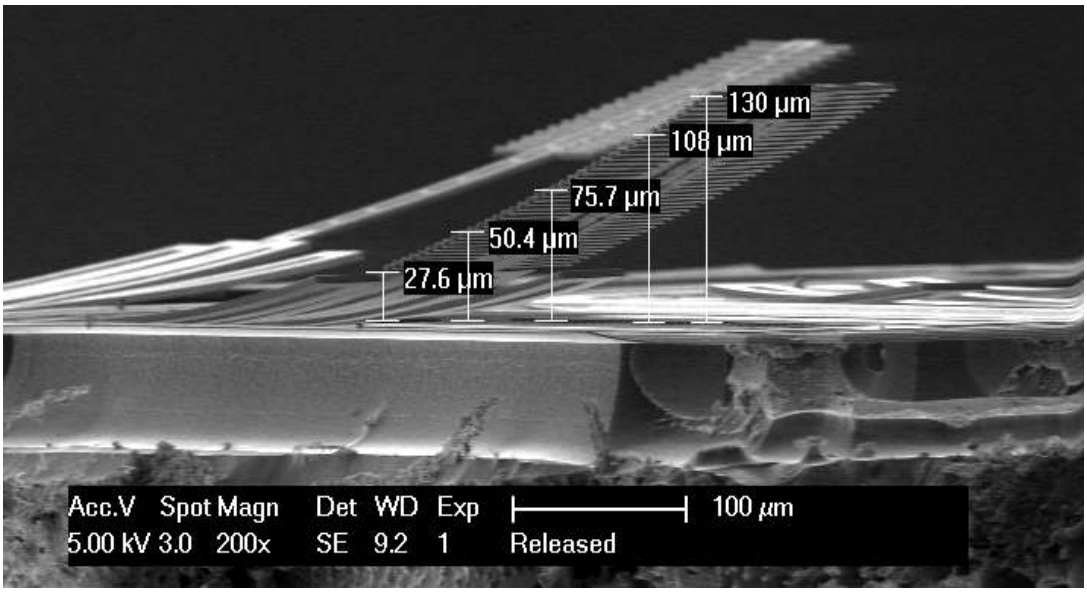


Figure 4-2: Measured 80-finger switch initial displacement

Figure 4-3 shows the initial beam displacement measurement and simulation result; the material composition of the supporting beam determines the displacement of the structure. The radius of the curved beam is the same; thus, the longer the beam, the bigger the initial displacement.

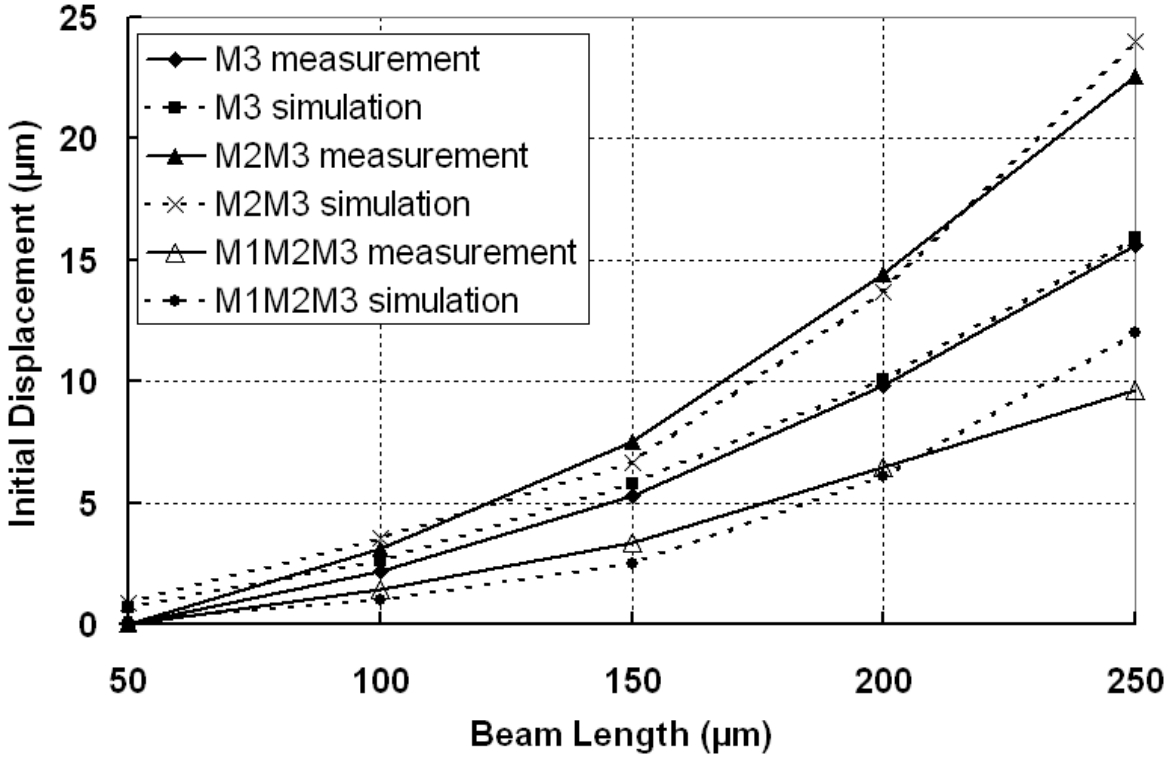


Figure 4-3: Initial maximum displacement with different beam length

4.2 Insertion Loss and Isolation Measurements

The design is targeted for high frequency application, so the calibration and de-embed technique is introduced first; then the measurement procedure and results of the isolation and insertion loss are given.

4.2.1 VNA Calibration

The HP 8722ES network analyzer calibration process is the test set using directional couplers or bridges to pick off the forward and reverse waves traveling to and from each port. It downconverts these signals to four IF sections and amplifies and digitizes the signals for further digital processing and display. VNA calibration is the process of measuring devices with known or partly known characteristics and using these measurements to establish the measurement reference plane.

VNA calibration options [37]:

- A “response” calibration is simply a vector magnitude and phase normalization of a transmission or reflection measurement used only at low frequencies. A “thru” sample of Impedance Standard Substrates (ISSs) is used for response-type calibration. This type of calibration is only used when accuracy requirement is low. This kind of calibration removes frequency response error.
- Full calibration uses open, thru, short, and load samples. It delivers highest accuracy for dual-port devices. It removes the following errors: directivity, source match, load match, reflection tracking, transmission tracking, and crosstalk.

4.2.2 De-Embedded Technique

The pad capacitance is removed from the measurement results. A dummy pad is fabricated on the same chip for pad de-embedding and the procedures are:

1. Calibrate VNA, coaxial cable, and probes using the ISS and full two-port calibration method.
2. Measure the two-port S-parameters of the dummy pad as [S2x2] dummy and [S2x2] DUT, respectively.
3. Convert S-parameters to Y-parameters using HPADS.
4. Devices can be de-embedded from the probing pads using Y[2x2] device = Y[2x2] DUT – Y[2x2] dummy.
5. The algorithm discussed along is programmed using the network analyzer.

Short, open, load, and thru (SOLT) structures provided on the Cascade Impedance Standard Substrate (ISS) are shown in Figure 4-4. Calibration using the SOLT standards which are entered as calibration coefficients into the HP8712 network analyzer to provide

an accurate error model of the parasitic loads caused by the probes and the connected cables.

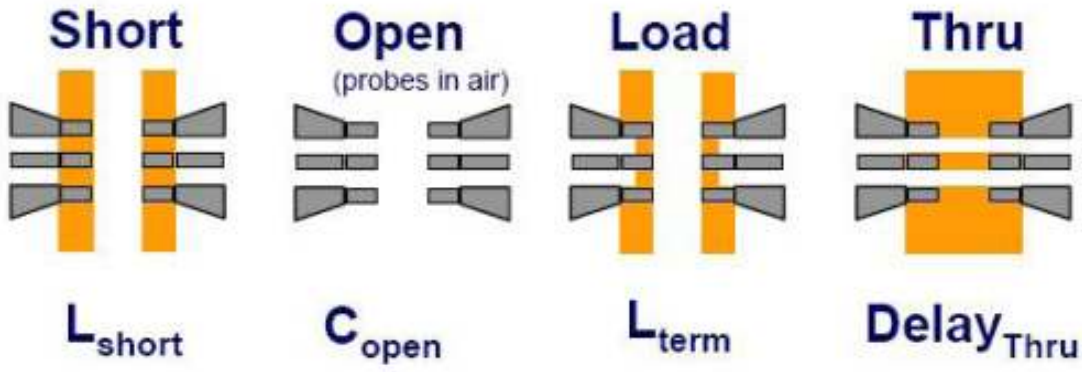
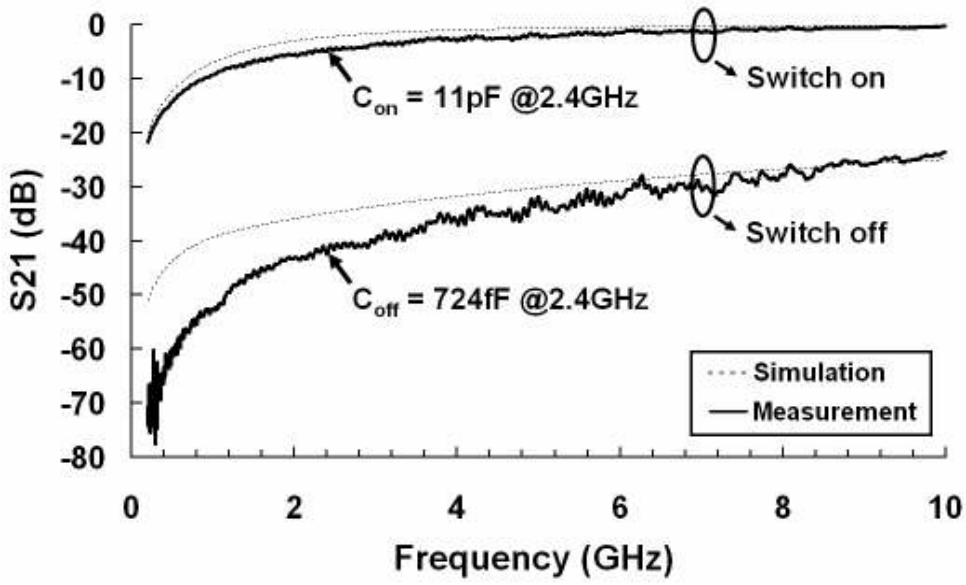


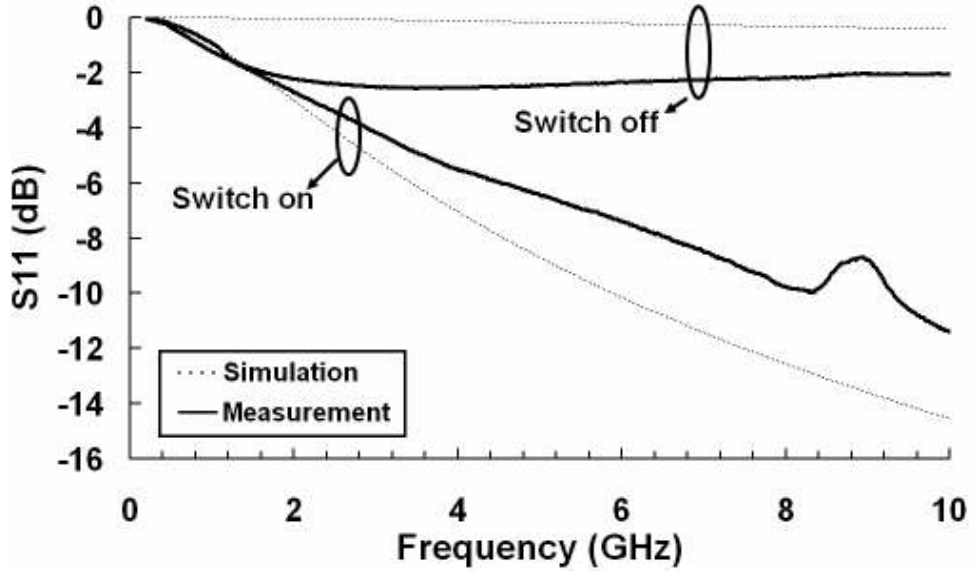
Figure 4-4: Short, Open, Load and Thru calibration structures provided on the impedance standard substrate

The full wave electromagnetic simulation of the switch is done by a finite element method using the Ansoft HFSS. The substrate is highly resistive silicon with a dielectric constant of 11.9 and a thickness of 300 μm. Silicon oxide is on top of the substrate and has the dielectric constant of 4.0. Figure 4-5 gives the EM simulation and measurement result of the 80-finger RF MEMS switch. The RF characteristics are measured using a Cascade RF-1 microprobing station and an HP 8722ES network analyzer. A full SOLT calibration is done before the measurement. The test fixture is de-embedded from the measurement.

Figure 4-5 shows the switch insertion loss at the ON state and isolation at the OFF state of an 80-finger switch. For the ON condition, the insertion loss is 1.6 dB, and isolation is 33 dB at 5.4 GHz. The measurement results matched HFSS simulation results well.



(a) Insertion loss



(b) Return loss

Figure 4-5: Insertion loss and isolation of the switch when switch is on and off

4.3 Temperature and Thermal Actuation Measurement

This section describes the measurement of the effect of the temperature change as a function of the input voltage on the embedded heater. This measurement is done using the Compix® PC2100 thermal imaging system, which consists of an infrared camera and

the WinTES camera control and analysis software. The camera has thermal resolution of 0.1 C/step and minimal detection feature size of 50 μm. This resolution is sufficient for this application. A series of thermal images were taken at different applied voltages as shown in Figure 4-6.

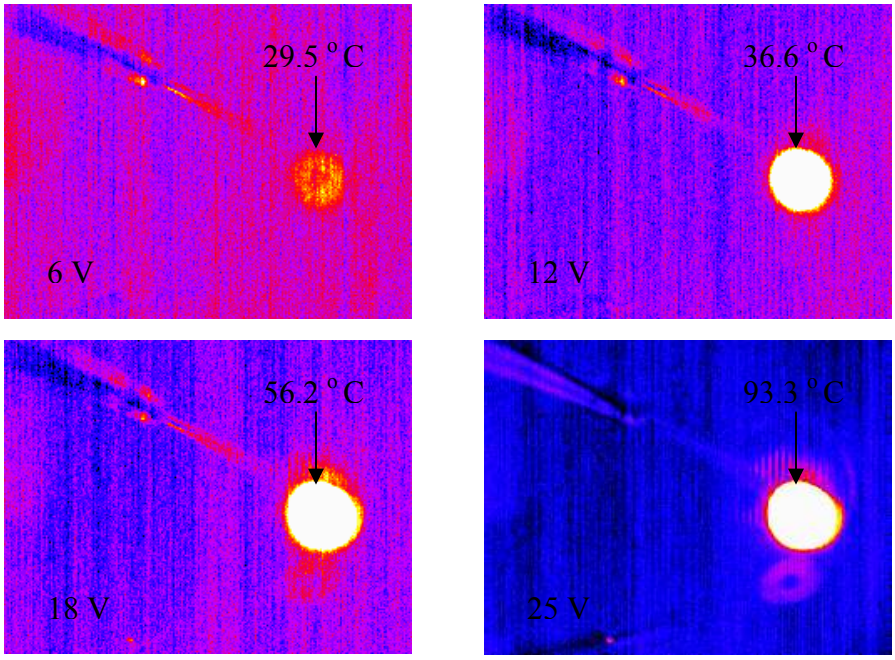


Figure 4-6: Series of thermal camera image indicating the applied voltage and temperature of the RF MEMS switch actuator

The measurement of the device's temperature versus applied voltage to the polysilicon heater is shown in Figure 4-7. The ambient temperature was 30 °C. The device was attached to a thermal isolation sheet on the Cascade probing station. The DC power was applied via two DC probes. At input voltage of 25 V, the device temperature reached 93°C. The quadratic relationship between the applied voltage and the temperature was extrapolated based on Figure 4-7 and is shown in the same figure, where X is the voltage and Y is the temperature.

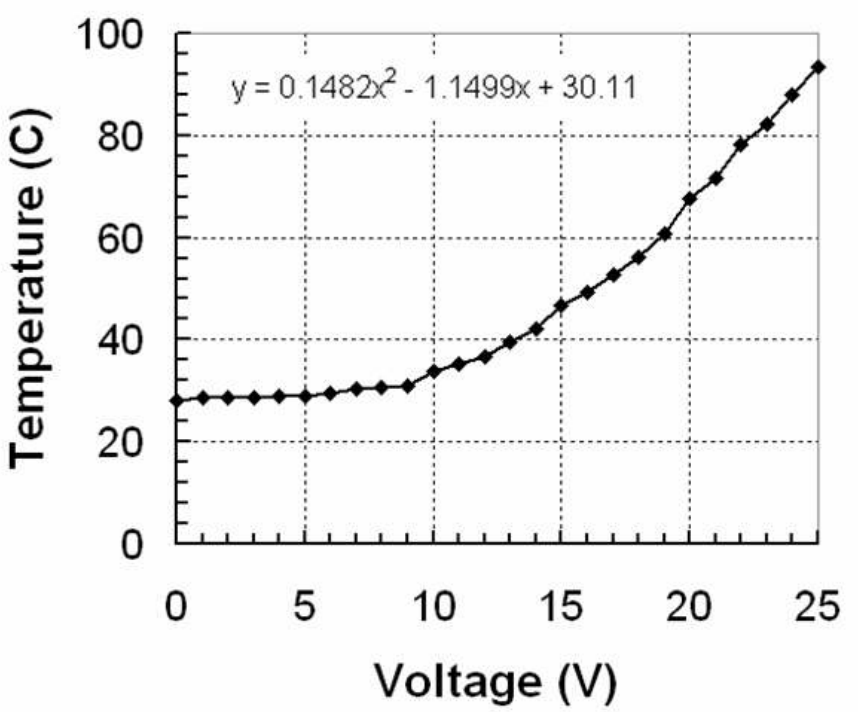


Figure 4-7: Measurements of device temperature versus applied voltage to polysilicon heater

Figure 4-8 shows the measured displacement result of the beam versus input voltage. The switch turn-on voltage is 25 V. The displacement was measured from the surface reference point. At 25 V, the cantilever beam is completely flat [14].

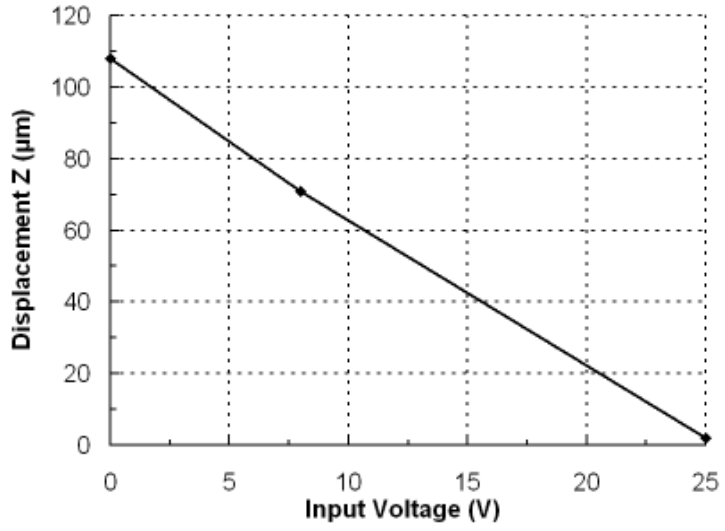


Figure 4-8: Measured displacement versus input voltage with thermal isolation to the chuck

Figure 4-9 shows a lab set up for measuring the temperature of the structure. A thermal camera is set on top of the device, which is powered via DC probes on a Cascade probing station. The measurement is done using a Nikon microscope.

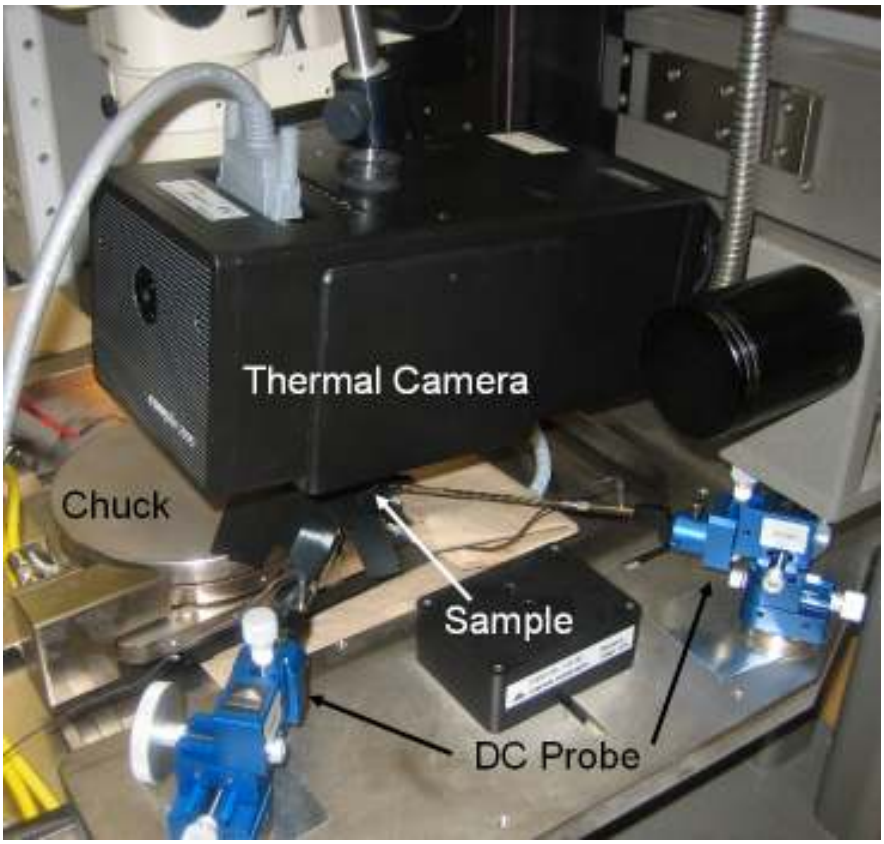


Figure 4-9: Test setup for thermal measurement of the RF MEMS switch

4.4 Conclusion

In this chapter, a novel, vertical, thermal-actuated, CMOS-compatible MEMS switch for ISM/WLAN band applications was fabricated and characterized. Thermal actuation threshold voltage was measured as 25 V. The measured results show the insertion loss and isolation are 1.67 dB and 33 dB, respectively, at 5.4 GHz, and 0.36 dB and 23 dB at 10 GHz. Measurement results demonstrated good RF characteristics at 5.4 GHz band.

Chapter 5 — Simulation of ET-Switch in Realizing Broadband Voltage Controlled Oscillator

This chapter covers the simulation of the multiband voltage controlled oscillator (VCO) using the MEMS switch model developed in the previous chapters. In this work, we used differential Colpitts VCO architecture, and compared several VCO topologies for multiband application. A MOSFET switched inductor VCO chip is fabricated and the measurement results are presented at the end.

5.1 Introduction

Recent advances in the wireless communication market have led to the coexistence of several networks such as cellular network, personal area network (PAN), wireless local area network (WLAN), etc, along with several different air interfaces (802.11a, 802.11g, Bluetooth, wireless code division multiple access (WCDMA), etc.) [1]. All the wireless devices need to be compatible with the different communication standards in order to enable "global roaming." The technology of the wireless devices also needs to allow for a smooth migration to future generations of communication standards with higher data rates. Hence, a compact and power-efficient implementation of such multistandard terminals calls for the need of an intelligent RF front-end that can achieve maximum hardware sharing for various standards. The simple way to implement a multistandard receiver is to use multiple RF front-ends for different standards. This makes each front-end design easier; however, this approach requires multiple low noise block converters (LNBs), mixers, and VCOs. The second approach of designing a multistandard receiver is to design single receiver architecture for all and add multistandard features to the single wireless receiver architecture. Such architecture

would require reconfigurable frequency agility on the individual RF blocks. One of the most critical RF blocks that needs to exhibit frequency agility is the VCO, which needs to have a very wide tuning range in order to be used for several standards. The use of reconfigurable VCO in multistandard receiver architecture is as shown in Figure 5-1. The baseband is the digital signal processing element for the communication systems. The reconfigurable VCO and LPF are configurable by baseband module.

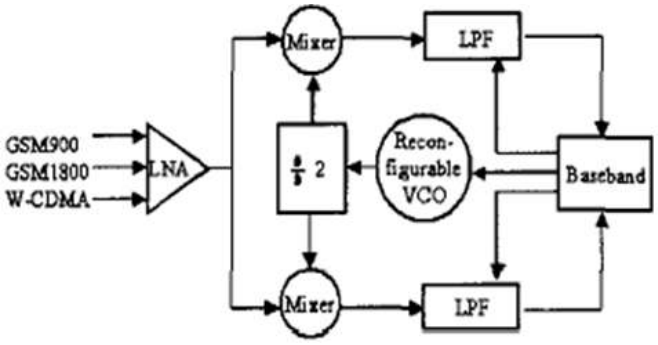


Figure 5-1: Multiband VCO in the RF receiver

5.2 Voltage Control Oscillator Background

Oscillators are used at various places in an RF transceiver system. Figure 5-2 illustrates the block diagram of a zero-IF receiver. The local oscillator in the tuning system provides the in-phase and quadrature mixers with a signal equal in frequency to the average received RF carrier frequency. The mixers convert the wanted signal directly to baseband.

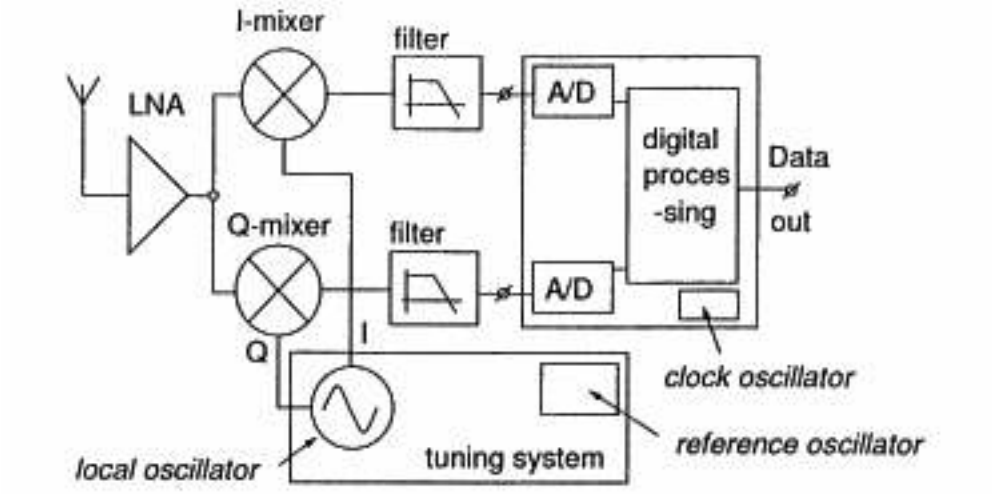


Figure 5-2: Simplified block diagram of a zero-IF receiver

5.2.1 VCO Topologies

Oscillator classification may be based on one of the properties of an oscillator; for example, if it is a distributed type or a lumped type. By distinguishing the oscillators with or without inductor, the oscillators can be categorized as LC and RC. The presence of both inductor and capacitor make it possible to preserve energy in an oscillation period; thus, the quality factor of the LC oscillator is better than the RC oscillators. Q is close to unity for RC oscillators because there is no energy preserved per oscillation period. RC oscillators usually have poorer spectral purity than LC oscillators. A break-up diagram, Figure 5-3, shows the possible classification of the oscillators. [38] Crystal oscillators have excellent spectral purity and very good long-term stability; however, the thickness of the crystal imposes a limit on the maximum frequency that can be achieved. A surface acoustic wave (SAW) resonator allows higher oscillator operation frequencies when compared to crystals. Ring oscillators are known for their ease of integration. The principle of a relaxation oscillator is based on the charging and discharging of a capacitor. A current charges a capacitor until a positive voltage threshold is reached and the

direction of the current is reversed. Once the negative threshold voltage is reached, the current direction is again reversed.

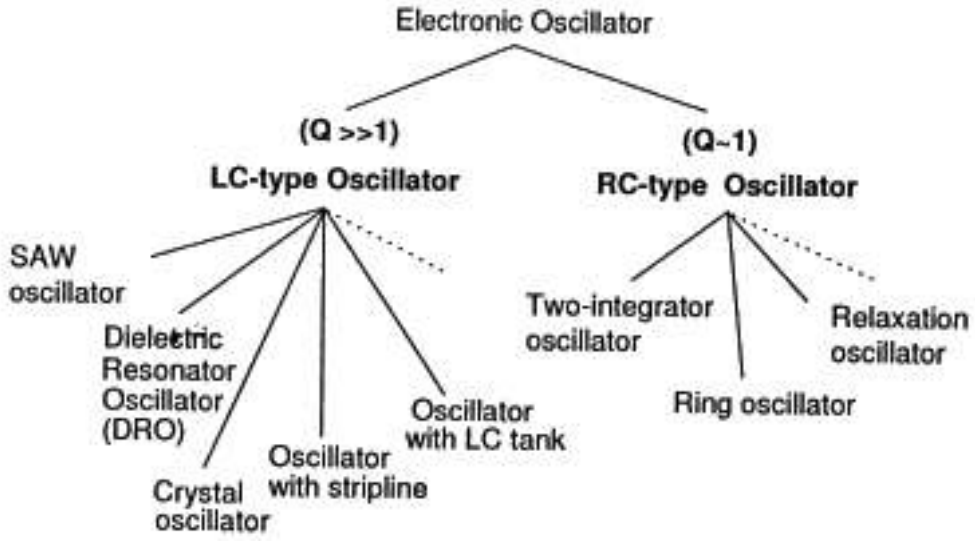


Figure 5-3: Oscillator classification

5.2.2 VCO Design Specifications

The basic function of an oscillator is to generate a periodic signal with certain properties. The output of an ideal harmonic oscillator (Figure 5-4 a) with angular frequency ω_{osc} [rad/s] and peak amplitude $V_{carrier}$ [V] can be written as

$$V_{out}(t) = V_{carrier} \cos(\omega_{osc} t) \tag{5.1}$$

A tunable ideal oscillator (Figure 5-4 b) can be represented by

$$V_{out}(t) = V_{carrier} \cos(2\pi\ (K_{vco}\ V_{tune} + F_{center})t) \tag{5.2}$$

The initial phase of (1) is assumed to be zero. Tuning voltage V_{tune} controls the frequency, and tuning constant K_{vco} [Hz/V] determines the tuning slope. F_{center} is the oscillation frequency with zero tuning voltage.

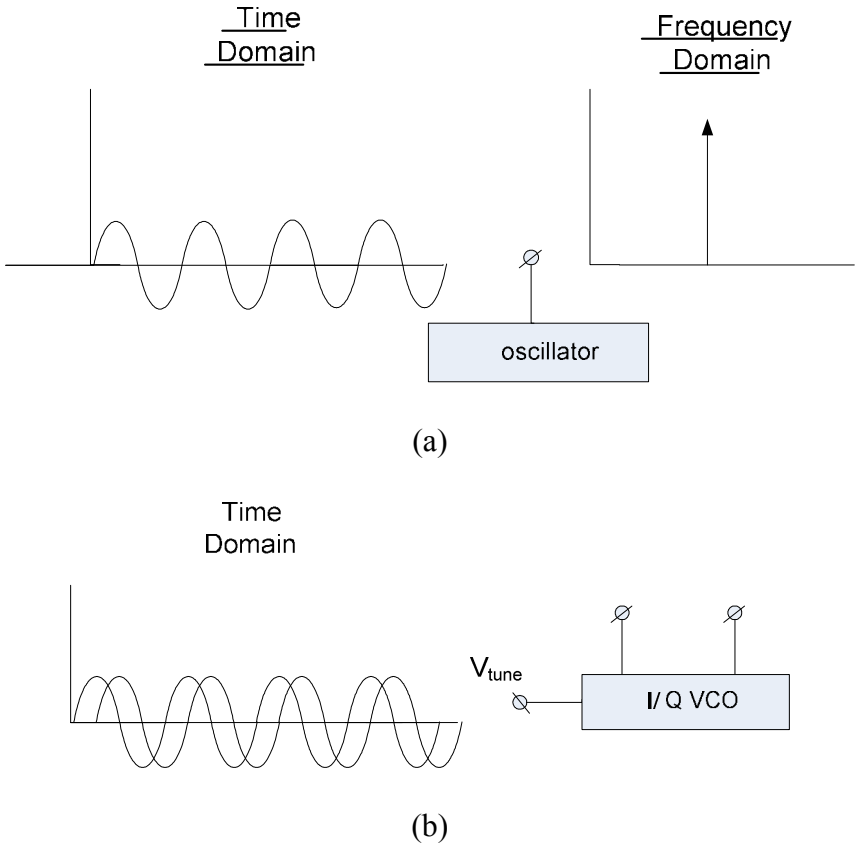


Figure 5-4: Single phase oscillator (a) and a tunable I/Q VCO (b)

Oscillator frequency usually changes due to the processing variation in the manufacture process; therefore, some additional tuning range will always be required. Noise from the oscillator circuitry and from the external environment corrupts the spectral purity of an oscillator signal. This means that the carrier power is now distributed in a finite bandwidth around ω_{osc} and its harmonics. Figure 5-5 shows the fundamental frequency and two harmonics of a square wave. The application determines whether the harmonics of an oscillator output signal are unwanted or wanted. The most important difference between the ideal and nonideal oscillator are phase noise sidebands, as shown in Figure 5-5. Although most power is present at ω_{osc}, some power is also present at small offset frequency from ω_{osc}. These phase noise sidebands decrease with increasing offset frequency from ω_{osc} or its harmonics. White noise becomes dominant at a certain offset

frequency. In the time domain, phase noise is referred to as jitter and is shown in the inset of Figure 5-5. In general, amplitude noise also is present in nonideal oscillators; however, the amplitude noise can be removed by a limiter at the expense of generation of harmonics.

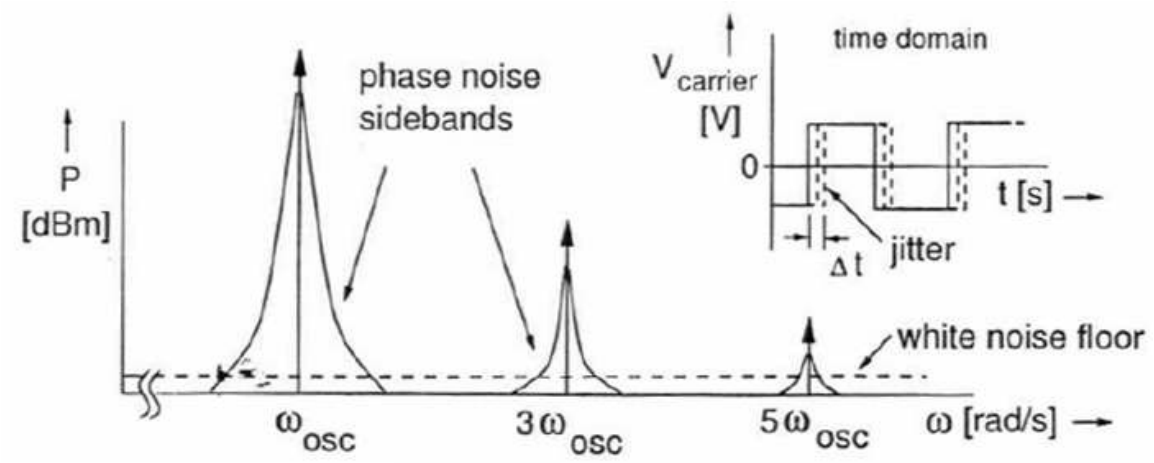


Figure 5-5: Spectrum (Fundamental and Two Harmonics) of a square wave with phase noise sidebands (The inset shows the effect of the sidebands in the time domain: jitter.)

5.2.2.1 Phase Noise

A practical oscillator suffers from frequency instabilities. These frequency instabilities are called phase noise. VCO phase noise has a negative impact on system performance. In the timing domain, phase noise degrades the bit error rate (BER) of the receiver and increases jitter on the data stream (transmitter must have jitter below a specified level) on the transmitter. Short-term instability of an oscillator (frequency changes less than seconds) is characterized by the single-sideband (SSB) phase noise to carrier ratio L at offset frequency $f_{m,}$ which is defined in dBs as:

$$L(fm) = 10\log(\frac{\text{phase noise density at } f_m \text{ in 1Hz}}{P_{carrier}}) \qquad (5.3)$$

Its units are commonly given in dBc/Hz, indicating that the phase noise is measured relative to the carrier and in a 1 Hz bandwidth.

$L(f_m)$ can be measured directly using a spectrum analyzer. The spectrum analyzer measures the power spectrum of the oscillator, which includes both the phase noise and amplitude variations. However, the phase noise component is dominant in many practical oscillators because the amplitude component is reduced by limiting mechanisms.

5.2.2.2 Tuning Range

The frequency and tuning ranges are important specifications for oscillator design. Table 5-1 shows the frequency tuning requirements of several telecom standards. The tuning range is considered small compared to the center frequency in these standards; a satellite receiver that requires a tuning range of at least 950 MHz to 2150 MHz is considered a wide range systems.

Table 5-1: Tuning range of several standards

Standard	**Mobile Receiver [MHz]**	**Mobile Transmitter [MHz]**
DECT	1880-1920	Same
Bluetooth	2400-2483	Same
GSM	890-915	925-960
UMTS TDD	1900-1920 2010-2025	Same
UMTS FDD	2110-2170	1920-1980

The tuning range specification has to be met under worst case conditions. Therefore, frequency deviations due to temperature changes, process spread, and power supply

variations should be added to the tuning range. For an RC oscillator, the process spread can easily be 20% to 40%. In an LC oscillator the (planer) inductor tolerance is usually very good (for example, 1%) because of the accurate lithography of the IC process. However, the varactor and fixed capacitances can vary up to 20% in value, and the center frequency can therefore change by more than 10% [39].

A VCO has a tuning constant, Kvco, which is specified in Hz/V. This constant is sometimes also referred as VCO gain. For example, if the tuning range is 2.4 GHz to 2.483 GHz (Bluetooth standard) and the available tuning voltage range is 2.7 V, the tuning constant is about 30.7 MHz/V. The tuning constant actually varies due to the nonlinearity of the circuit components. At the end of the tuning range, where the parasitics dominate, Kvco decreases for typical VCO.

5.2.2.3 Power Consumption

An oscillator is normally part of a larger system with a restricted power budget. Low power design is very important, especially for portable systems. Lower power consumption also translates into a cheaper package solution and a higher degree of integration. The power budget of an oscillator is specified in miliwatts or by the available current given a supply voltage. The maximum supply voltage can be dictated by the application or the technology (for example, the breakdown voltage in CMOS). Additional current is needed to realize output buffers, which form the interface between the oscillator and the cascaded blocks such as mixers and dividers.

5.2.2.4 Figure of Merit

“How good is the VCO design?” This question is difficult to answer precisely because there are many ways to improve the phase noise (such as increasing the DC

current or improving inductor Q) that have nothing to do with the circuit design. In order to get around this problem, researchers in the field have developed a VCO "Figure of Merit" (FOM), which normalizes VCO performance to make comparison easier. This FOM is given by

$$FOM = L(f_m) + 20\log(\frac{f_0}{f_m}) - 10\log(\frac{P_{diss}}{1mW}) \quad (5.4)$$

where f_0 is the center frequency, f_m is the offset frequency, and P_{diss} is the DC power consumption. Thus, the higher the FOM, the better the VCO design.

5.2.3 Current Design Trend for VCO

Current wireless communication systems are developing toward broadband, putting stringent phase noise requirements on local oscillators. This implies that the current VCO design needs to incorporate passive resonators. These resonators can be narrowband SAW filters, transmission lines, or LC tanks. In addition to low phase-noise, wide tuning range and low power consumption are also important requirements.

Even though the MEMS resonator has much higher Q than the on-chip LC tanks, the maximum frequency of the MEMS resonators is limited to less than 1 GHz due to process. For VCO running about 30 GHz, a transmission line type of resonator is a good choice. However, a transmission line is not a realistic choice for VCOs running under 10 GHz due to the required length of the transmission line.

That leaves the LC tanks for the VCOs whose center frequency is below 10 GHz. Recent developments also demonstrate examples of using on-chip transformers for the feedback loop. Although a transformer is still difficult to build on-chip, it is clearly showing some good characteristics, such as uncoupled loop-back ratio with tuning range.

5.3 The State of the Art of Multiband VCO Design

5.3.1 Wide Tuning Range VCOs

Various techniques to achieve wide tuning ranges, such as switching between VCOs for separate bands, utilizing intermodal multiple frequency relations [5], and using switched resonators for band selection [6] [7] have been proposed. However, these result in large integrated circuits (ICs) and generation of only discrete frequencies. Broadband distributed oscillators provide a possible solution, but at the cost of a large die area and high power consumption. More recently, active-inductor-based VCOs have been proposed, but very few measured CMOS tunable active-inductor (TAI)-based VCOs exist [8] [9].

Most wide-range VCOs are implemented with wide-range varactors. VCOs using a bank of capacitors or varactors have been proposed in [40-43]; however, the capacitor bank switch is considered ideal, which oversimplifies the problem. The actual switch noise degrades VCO phase noise performance. As researchers analyzed and compared the noise level from different parts of the VCO circuit, it was concluded that the tail current source was the major noise contributor. Je-Kwang [44] proposed a tail current control method along with the capacitor bank control to improve the phase noise performance. On the other hand, Araki, Hyunchol, and Guermand [45-47] utilized a variable frequency divider to generate required local oscillator frequencies for the wide tuning range application; however, this frequency divider introduces extra noise to the system. Although difficult, it is still possible to achieve very wide tuning range VCOs using CMOS varactors. Fong [48] used accumulation mode varactors to achieve a tuning range of 58%. However, the high sensitivity of the AMOS varactors becomes an issue that affects system performance. On the configurable inductor side, Mukhopadyay [49]

proposed an active device-compensated inductor VCO structure, but the noise level of the active device degrades the VCO phase noise as well. Overall, a wide tuning range can be achieved using the CMOS process, but the active device noise seriously affects VCO performance.

5.3.2 Multiband VCOs

The software-defined radio application requires a flexible RF front-end, which includes wide tuning range VCO and multiband filter. The wideband VCO is usually used to generate frequencies ranging from 900 MHz to 2.5 GHz. Wide tuning range VCO has been proposed in [40, 41]; however, the authors of [40] only pointed in the direction of using MEMS devices for better performance. The design was not implemented using MEMS technology, and only existing MEMS inductor data was used in the simulation. Manetakis [41] used a capacitor bank to coarse tune the frequency; however, the capacitor bank lowers the overall Q of the tank, also resulting in a smaller inductor for the given frequency band, thus worsening the sensitivity of parasitic. Araki and Hyunchrol [45, 46] utilized a variable frequency divider to generate required local oscillator frequencies for the wide tuning range application, and this frequency divider introduced extra noise to the system.

The simplest method to implement multiband VCO is to combine multiple VCOs that have different center frequencies [40]. Obviously, having multiple VCOs on-chip increases the chip size, and the switching element adds noise to the system. Recently, the MEMS technology has been explored in tunable LC network [50], demonstrating an LC resonator with a DC surface micromachined switch that has a tuning range from 3.5 GHz to 7 GHz, while in [51] a P-I-N diode is used to control parallel LC tank values, thus

achieving variable matching network at the output of the power amplifier. Jong-Man [52] demonstrates a power amplifier design with a configurable LC matching network in the input and output stages. The configuration of the LC bank is controlled through a shunt MEMS switch. The MEMS switch design process is independent of the circuit design, and they are bonded together by a chemical bonding agent. This process is incompatible with the CMOS process and increases the cost of this solution.

Due to the absence of a good varactor compatible with CMOS technology, the integrated LC oscillator suffers from a very limited tuning range. The lot-to-lot process variations manifest as spreads of up to 20% in capacitance. Kral explained that the inductance of the on-chip inductor depends on the number of turns and that the geometry of metal traces is little affected by fluctuations in lithography [39]. The author proposed the use of a CMOS switch for capacitor tuning and inductor tuning. The switch is implemented using an active device. In order to reduce the switch energy loss, a MEMS switch is proposed for this purpose, and a MEMS inductor is also proposed to improve the tank Q.

The methodology used in this work is as follows:

- Use a spiral inductor with substrate etching to improve the Q factor.
- Use of a switched inductor bank instead of a capacitor bank.
- Tuning range control select, if a switch is used, the tuning range is divided into sections determined by the variable inductor within each section. Variable capacitor controls the tuning characteristics.

5.3.3 Switched Resonator, Variable Inductor

This section summarizes the area of switched resonator using variable inductor for VCO design. Y. Seong-Mo, et al. demonstrated a switched inductor-based LC VCO [53]. In [39, 54-56], the authors proposed the use of CMOS switch for capacitor tuning and inductor tuning, and the switch is implemented using active devices. However, the losses that result from the active switch are significant. It was shown that the inductor quality factor degrades 30% due to the losses in the switch, and less than a 10% decrease of the self-resonance frequency is due to the switch parasitic capacitance [57]. TAI based on variable feedback resistor and harmonic VCO is demonstrated by [58, 59]. The major advantage of TAI is a smaller area and more tunability; however; at the cost of noise and nonlinearity due to the use of resistance for the feedback control, the Q of the inductor is degraded. To reduce the switch losses, the first variable inductor using a MEMS switch is described in [60]. It is thermally and electrostatically actuated. The driven voltage is 20 V, which is too high to be integrated with the CMOS circuit. There has been research on realizing variable inductors using micromaching technology [60, 61].

Lubecke et al. developed 3-D self-assembly MEMS variable inductor utilizing the thermal deformation of a large MEMS structure on the substrate. Because of the structure limitation, the variance of the inductance is about 13%. Zhou et al. developed a planar variable inductor using MEMS relays [60], in which the mutual inductance of each tap causes large nonlinearity for inductor value. [62] proposed using a multicontact MEMS switch and CPW to realize variable inductors in RF frequency, but the structure applies to frequency around 20 GHz to 50 GHz. A variable inductor structure is needed for GSM 1.8 GHz band and WLAN 5.5 GHz applications. Low power consumption and high

linearity are desired for these applications. MEMS switches are also considered in [50]; 75% tuning range was achieved. For multiband VCOs, the inductor can be realized using a solenoid inductor that has multiple taps to fulfill the variable inductor requirements. The inductor Q would be degraded due to the taping, and the solenoid inductor also has the potential of achieving higher Q than its spiral counterpart. The solenoid inductor is linear and with a fairly small footprint; if the plastic deformation and magnetic assembly (PDMA) method is used; an even smaller footprint (90 degree vertical inductor) can be realized. There are also tunable magnetic RF inductors proposed by [63], in which the tuning of the inductor value is achieved by changing the current and thus changing the permeability of the ferromagnetic (FM) core. This method requires a special process that allows the insertion of the EM core into the solenoid inductor.

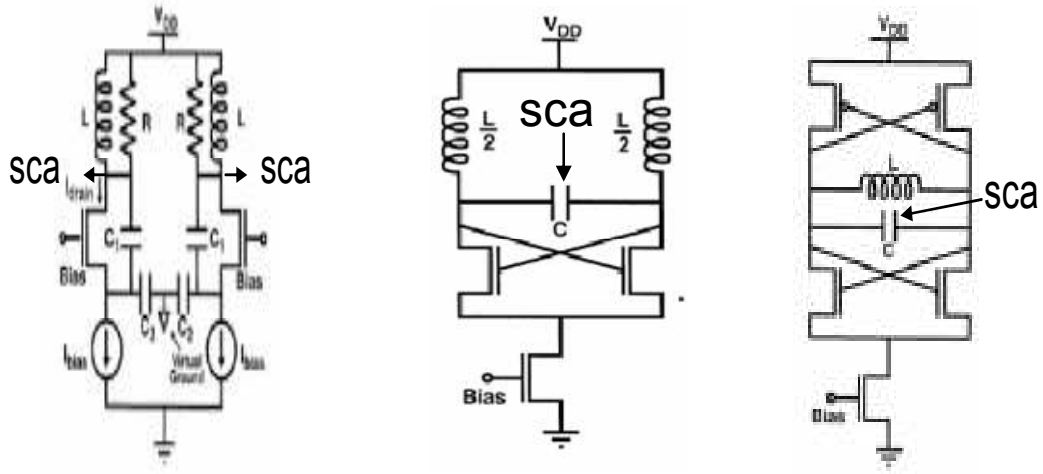
To realize the multiband VCO, either band-switched capacitor can be used or a variable inductor can be utilized. The popular bank switch capacitor requires many capacitors on-chip, which means a large area. Also, the switch noise of the bank selector degrades the VCO phase noise.

On the other hand, a variable inductor can be realized using electrical switches. However, the transistor-based electrical switch suffers from high ON-state resistance, non-zero OFF-state current, and high noise insertion. The emergence of the MEMS switch shows excellent characteristics for the purpose of switching RF components.

5.4 Colpitts Voltage Controlled Oscillator Design

Three popular VCO topologies: cross-coupled, complementary cross-coupled, and differential Colpitts are investigated in terms of their performance for wideband wireless communication applications. Figure 5-6 shows the different VCO topologies. Three

VCOs, implemented in a standard 0.5 μm CMOS technology, are compared from the prospective of phase noise sensitivity to various noise sources, tuning range limitations, and power dissipation. Switched capacitor arrays (SCAs) are used for frequency tuning along with varactor.



(a) (b) (c)

Figure 5-6: Circuit schematic of (a) differential Colpitts (VCO_CO), (b) NMOS cross-coupled (VCO_C), (c) complementary cross-coupled (VCO_CC)

The SCA is used for wide tuning range. The block diagram of the SCA with varactor is shown in Figure 5-7, where two capacitors are switched by MOSFET switch.

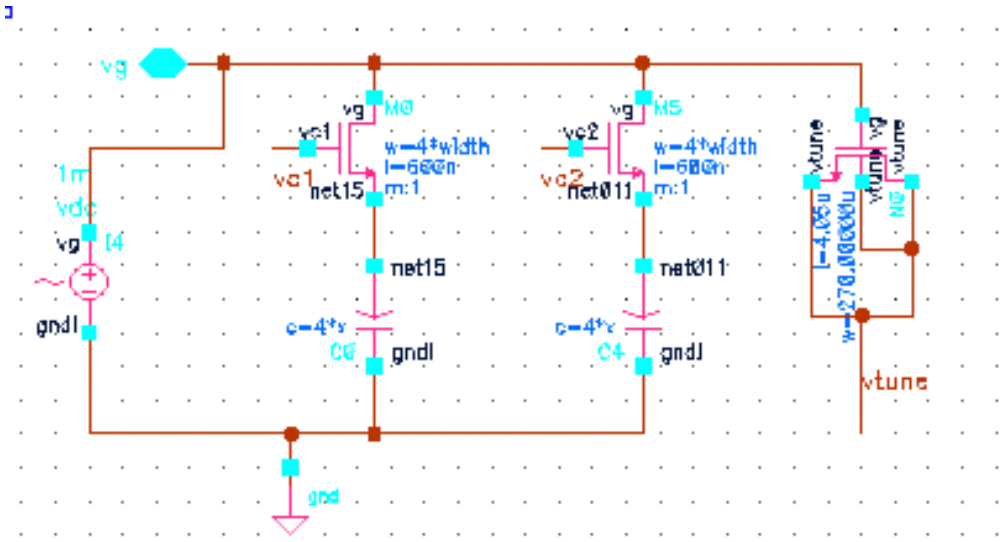


Figure 5-7: Switched capacitor array (SCA) with varactor

To sustain continuous oscillation, energy needs to be injected back to the resonator or "tank" periodically to compensate for losses. The Colpitts VCO uses a capacitive divider to couple the tank voltage back to the source of the MOSFET sustaining amplifier by turning the amplifier on periodically. Because this happens at the peak of the tank voltage, the current noise is injected at the peak of the swing, resulting only in amplitude degradation, not phase degradation. Thus, the Colpitts oscillators have inherent advantages for phase noise performance. The differential Colpitts oscillator topology was introduced to meet the need of suppressing common mode noise. The basic theory of operation of the differential Colpitts is the same as that for the single-ended topology.

The cross-coupled and complementary cross-coupled VCOs are designed in current limited mode, with the negative gm provided by the cross-coupled NMOS and PMOS pairs. Figure 5-8 shows the input impedance of PMOS and NMOS pair in VCO_CC.

In all cases the differential topology is useful in suppressing even order harmonics, which are detrimental to the operation of direct conversion (zero-IF) and low-IF receivers.

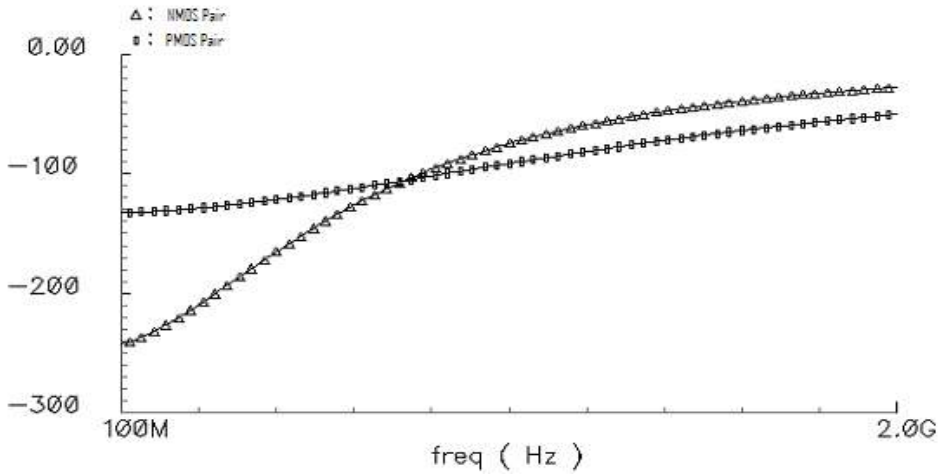
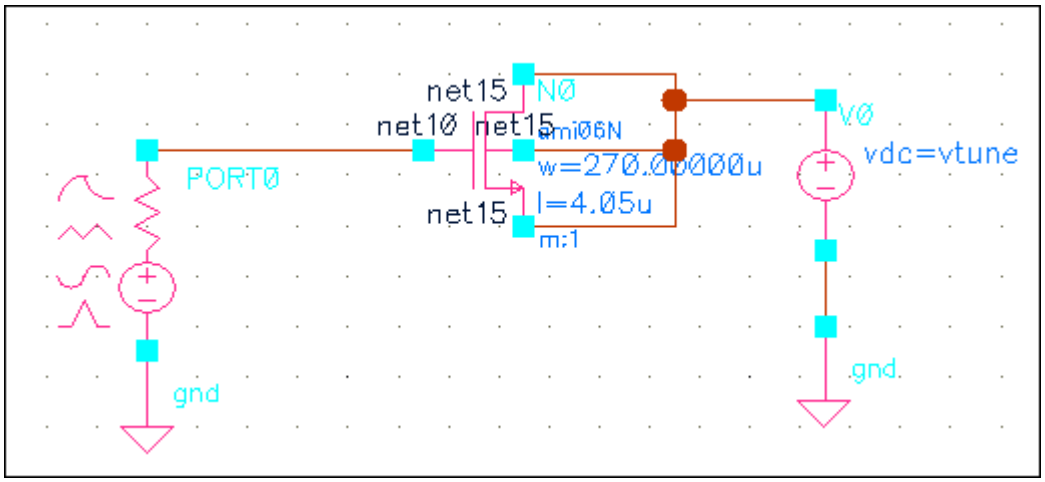


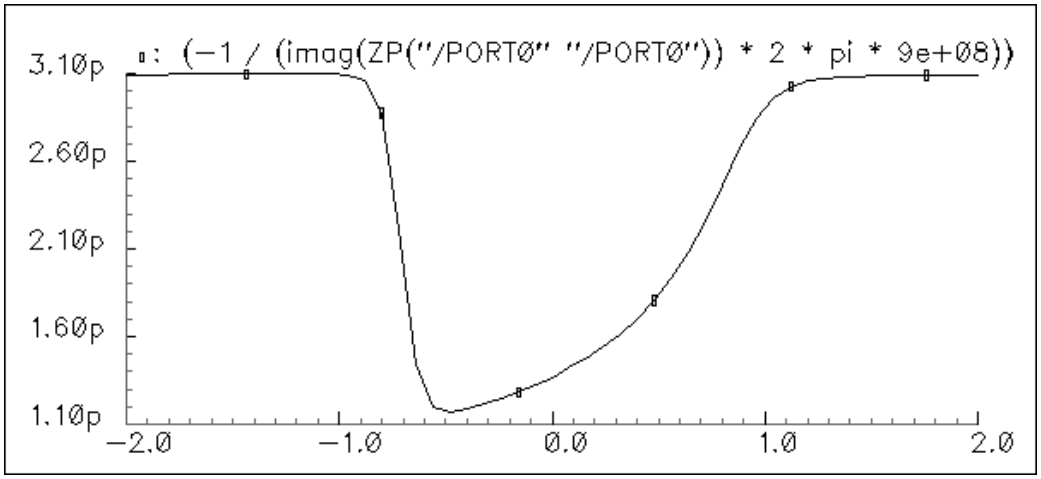
Figure 5-8: The input impedance of PMOS and NMOS pair for VCO_CC

5.4.1 CMOS Varactor Design and Characterization

Varactors are used for fine tuning the VCO frequency. Reversed-biased diodes are a common varactor in CMOS processes. However, reverse-biased diodes have a poor quality factor (Q) that degrades the VCO phase noise performance over the whole tuning range. The MOS transistor with drain, source, and bulk connected together can be used as a configurable capacitor; the capacitance value depends on the voltage between the bulk and the gate. In this work, an NMOS device is used in its depletion and accumulation region. Figure 5-9 shows the designed CMOS varactor characteristics and the test setup.



(a)



(b)

Figure 5-9: Varactor test setup (a) and tuning curve (b)

Table 5-2 shows that the complementary VCO can achieve the widest tuning range using the same varactor bank. The VCO_C, VCO_CC, and VCO_CO circuits are shown in Figure 5-6.

Table 5-2: Tuning range comparison

Topology	**Fmin (GHz)**	**Fmax (GHz)**	**Range**
VCO_C	1.33	2	41%
VCO_CC	1.06	1.22	14%
VCO_CO	0.9	1.38	42%

5.4.2 Noise Contribution of Switched Capacitor Array and Tail Bias Current Source

Center frequency is set to 1.4 GHz for all three circuits. The noise contributions of the SCA switches on the total phase noise are shown in Table 5-3. The results are obtained through Cadence SpectreRF simulations. Table 5-3 shows that VCO_CO has the lowest

phase noise level. The VCO_C, VCO_CC, and VCO_CO circuits are shown in Figure 5-6.

Table 5-3: Phase noise contribution comparison

Topology	**SCA Switch (%)**	**Tail (%)**	**PN @100 K (dBc)[1]**	**PN @100 K (dBc)[2]**
VCO_C	3.3	0.63	-107	-114
VCO_CC	0.1	92	-88	-101
VCO_CO	0	24	-110	-120

1. *SCA switches all ON*
2. *SCA switches all OFF*

5.4.3 Figure of Merit (FOM)

The normalized figure of merit, FOM, suggested by [64] is used.

$$FOM = 10\log\left(\left(\frac{F_{center}}{\Delta f}\right)^2 \frac{1}{L(\Delta f)\cdot V_{dd} I}\right) \tag{5.5}$$

where f_{center} is the oscillation frequency, Δf is the frequency offset, $L(\Delta f)$ is single sideband phase-noise at the frequency offset, V_{dd} is the bias voltage, and I is the tail bias current. Table 5-4 listed the comparison of FOMs for the three VCOs under consideration. The VCO_C, VCO_CC, and VCO_CO circuits are shown in Figure 5-6.

Table 5-4: Figure of merit comparison

Topology	Frequency (GHz)	Phase Noise (dBc/Hz)	Current Supply (mA)	FoM
VCO_C	1.33	-107	12	172
VCO_CC	1.06	-88	58	144
VCO_CO	0.9	-110	14	171

The phase noise is measured at 100 kHz offset. The power supply is 5 V for all three VCOs. This FOM does not, however, include an important performance metric of VCO, the tuning range. The following proposes a new FOM, which includes the tuning range. Tr is the tuning range in percentage. The comparison of the new FOM is listed in Table 5-5. The VCO_C, VCO_CC, and VCO_CO circuits are shown in Figure 5-6.

$$FOM_{new} = 10\log\left(\left(\frac{F_{center}}{\Delta f}\right)^2 \frac{100*Tr}{L(\Delta f)\cdot V_{dd} I}\right) \tag{5.6}$$

Table 5-5: New figure of merit comparison

Topology	New FoM	FoM
VCO_C	208	172
VCO_CC	175	144
VCO_CO	207	171

5.4.4 Inductor Design and Analysis

Self-inductance and resistance of the spiral is magnetically coupled with the conductive target. Self-inductance L is defined as a coefficient of proportionality in the equation

$$\Phi = L \bullet I \tag{5.7}$$

where Φ is the flux of the magnetic field through a contour, and I is the current in that contour. A time derivative of this equation results in

$$\frac{d\Phi}{dt} = L \bullet \frac{dI}{dt} \tag{5.8}$$

Using Faraday's law of induction

$$E = -\frac{d\Phi}{dt} \tag{5.9}$$

Obtain another expression containing inductance:

$$E = -L\frac{dI}{dt} \tag{5.10}$$

The minus sign here is the manifestation of Lenz's rule, stating that induced current always opposes its cause. Because the current induced in the aluminum target is opposed to the driving current, the total magnetic field flux through the spiral is smaller when the target is in close proximity to it. Therefore, self-inductance is smaller when the target is close to the spiral. Image current has been generated in the target. This current meets some resistance, and the overall effect is the increased resistance seen in the primary circuit. As spacing between the spiral and the target increases, this effect diminishes. [65]

The design goals of the inductor are the following:

1. High Q
2. Small size
3. High self-resonance frequency

The major loss of the inductor is due to the ohmic loss of the metal trace and the eddy current in the substrate induced by magnetic field. Much research has been done to model and reduce these two losses. Other factors affecting the quality factor of the inductors are as the follows:

1. Sheet resistance of the metal layer can be used only for calculating the dc resistance of the spiral.
2. Due to the skin effect, eddy current, and "current crowding," the resistance of the spiral increases at high frequency.
3. Copper metal and thick top-level metal improve the maximum inductor Q.
4. Multiple levels of metal are strapped together to create a spiral with a lower DC resistance.
5. Pattern ground shield (PGS) reduces the substrate loss.
6. CMOS substrate losses are still the limits factor.

For the metal loss, the current state of art is as the following:

1. Use wider metal trace.
2. Use high permittivity metal like gold.
3. Combine different layers of metal to reduce the resistance.

For the substrate loss, the current solutions are the following:

1. Remove the underneath substrate using the micromachine technique.

2. Use metal shielding to reduce the eddy current.
3. Use an implant to form N-P-N diodes in the substrate to block the eddy current.
4. Use higher resistive substrate material like sapphire or glass.
5. Differentially drive the inductor.
6. Use differential shielding.
7. Lift up the inductor using the thick oxide layer between the metal and the substrate.
8. Use the self-assembly technique to realize vertical inductor.

There are other methods proposed such as the iron-coil solenoid inductor design that really help to improve the Q of a large inductor, can be used in the field of a large current, DC-DC converter, etc.

Solenoid inductor is one possible solution to reduce the size, even though the high resistance of the vias affects the overall Q. Another solution is a stacked topology [57]. This requires several layers of metal to be used, and it has a larger interlevel capacitance, thus reducing the frequency of self resonance (FSR).

The modeling of the inductor is mostly from the Greenhouse theory [66], the sum of the self-inductance, and mutual inductance. In addition, the eddy current loss and skin effect have been included. 3-D EM simulator (Ansoft HFSS) has been used to carry out the simulation for complex structures. The models developed so far can be used toward design of maximum Q inductors. Optimal design parameters can be picked from simulation of the models.

Many design guidelines have been formed to improve the Q of the inductor. The rules include optimizing the layout shape, picking the right number of turns, selecting the spacing between metal traces, etc. The rule also recommends not using the innermost space of the spiral inductor because of the eddy current loss.

Although the optimization of layout or techniques to reduce the substrate loss did gain some ground for Q-factor improvement, the improvement is limited. The recorded Q for several nH inductors is still below 10. For a discrete passive device, Q is usually over 50, which is required by most communication systems. On the other hand, the micromachined (MEMS-enabled) inductor design shows quite impressive results; Q over 60 has been reported around the GHz range for several nH inductors. This definitely has much potential for future deployment.

Even though the MEMS-enabled inductor shows promise, it requires process modification or additional postprocess steps. These steps are costly and difficult to characterize. The problem is to utilize a simple process to do the job and characterize the process.

Calculation of inductor value using Modified Wheeler Formula [67] is as follows

$$L_{mw} = K_1 \mu_0 \frac{n^2 d_{avg}}{1 + K_2 \rho} \tag{5.11}$$

where n is the number of turns, μ0 = 4Pi x 10e-7.

k_1 and k_2 are listed in Table 5-6 for different inductor topologies.

Table 5-6: Coefficients for modified wheeler expression

Layout	K_1	K_2
Square	2.34	2.75
Hexagonal	2.33	3.82
Octagonal	2.25	3.55

This section gives the general equation and equivalent circuit for the inductors. Figure 5-10 is the simplified RLC model of the on-chip inductor.

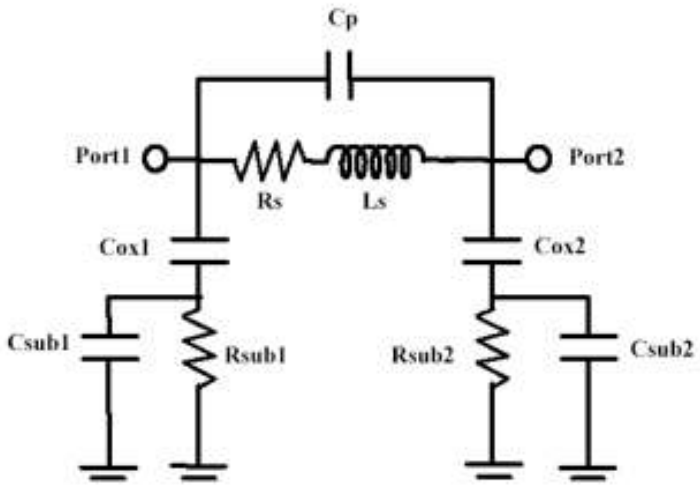


Figure 5-10: On-chip inductor equivalent circuit

The C_{sub1} and R_{sub1} are the substrate resistance and capacitance. The R_s and L_s are the equivalent resistance and inductance of the inductors, and C_p is the cross-coupled cap between turns. C_{ox2} is the capacitance between layers of metal.

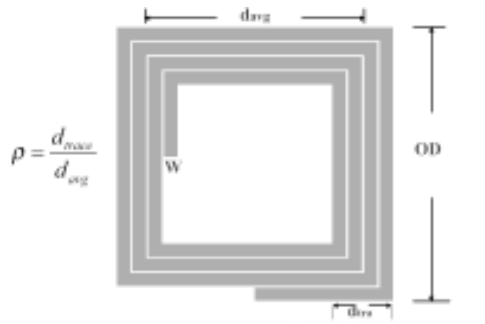


Figure 5-11: Example drawing of an inductor for inductance calculation

The following is an empirical formula. The parameters are shown in Figure 5-11.

$$L_{mw} = \frac{2\mu n^2 d_{avg}}{\pi}\left[\ln\left(\frac{2.067}{\rho}\right) + 0.178\rho + 0.125\rho^2\right] \tag{5.12}$$

where:

n is the number of turns

μ is the permeability of free space

d_{avg} is the average diameter

ρ is the percentage of the inductor area filled by metal traces

The result of inductance calculation is

Method	**Inductance (nH)**
Modified Weeler	1.97
EM Simulation	2
Current sheet Expression	1.96

As we know, the substrate coupled eddy current causes the quality factor of the on-chip inductor to degrade. The section below explores a potential technique that removes the partial substrate underneath the inductor in which the FEM simulation shows promising results.

The FEM tool, Ansoft, is used to model the planar inductor on the EPI substrate; the 2.5 turn spiral is used as an example. The parameters are 300 μm substrate, 9.8 μm oxide, and 0.7 μm passivation layer. Two-port analysis and different materials are used, and depth of the substrate removal is simulated. The simulation setup is shown in Figure 5-12 and Figure 5-13.

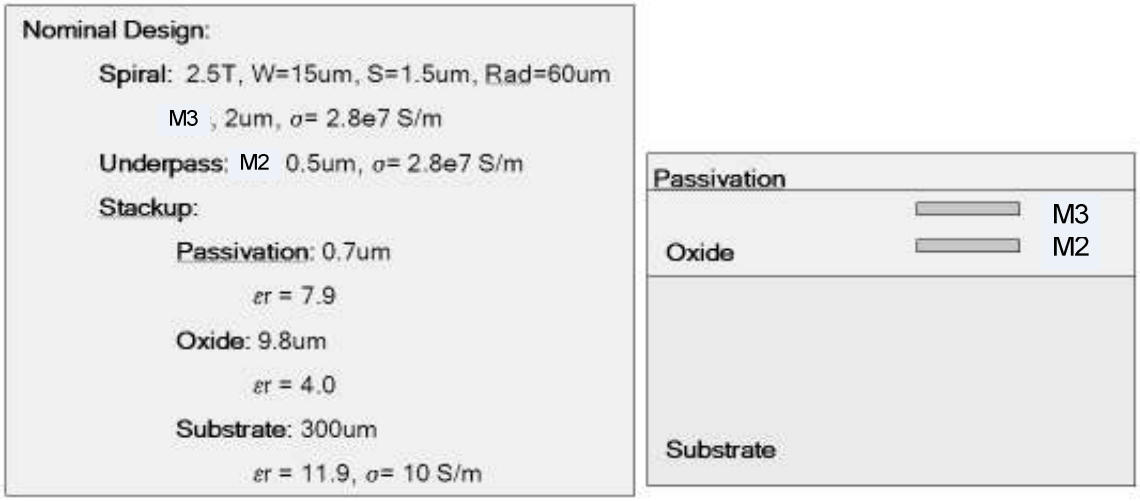


Figure 5-12: HFSS setup for inductor analysis

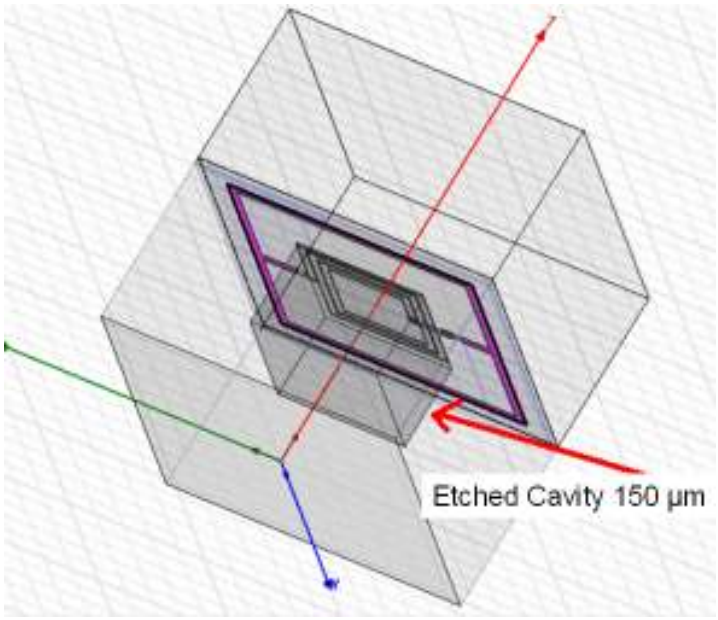


Figure 5-13: Spiral inductor with etched substrate [68]

From Figure 5-14, the self-resonance frequency is 16 GHz, and the inductance at 5 GHz is ~2 nH.

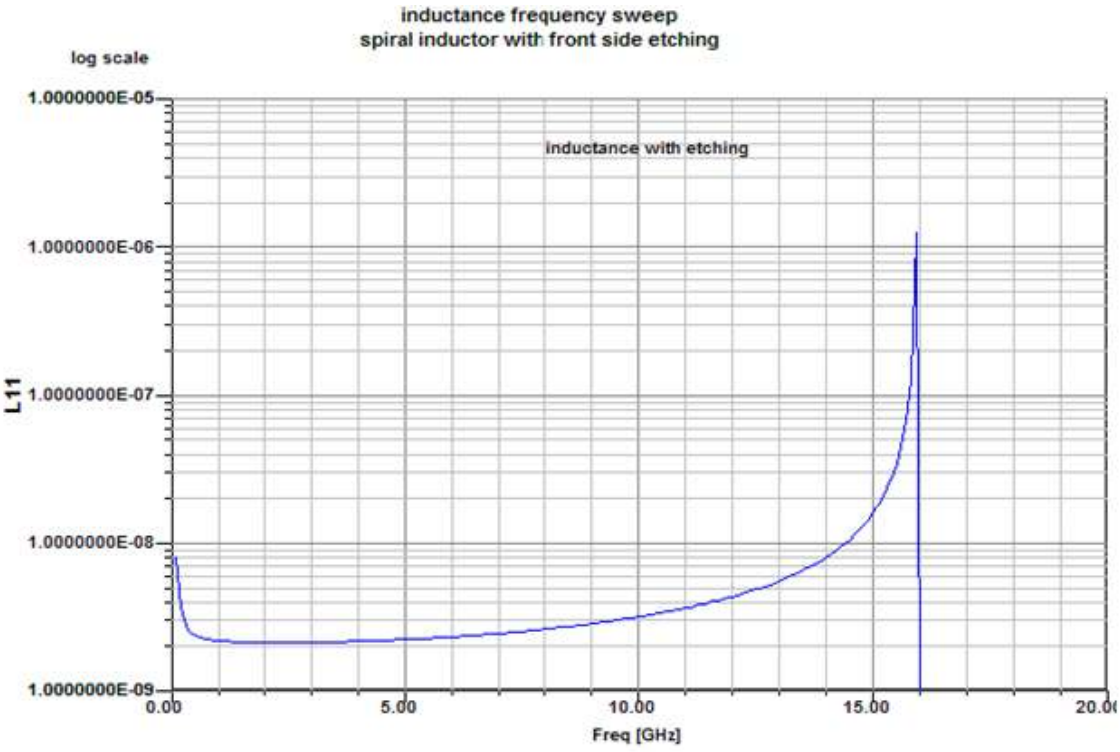


Figure 5-14: Spiral inductor with the etched substrate

Table 5-7 summarizes the simulation result of using different materials and removal of part of the substrate under the inductor. Table 5-8 listed the material properties used.

Table 5-7: Summary of inductors with different material

	Metal Type	**Sub Etch** (μm)	**L** (nH)	**Q**	**Fsr** (GHz)
Inductor 1	Aluminum	0	2	7.7 (2G)	13
Inductor 2	Aluminum	100	2	11 (5G)	15
Inductor 3	Aluminum	250	2	11.5 (5G)	15.6
Inductor 4	Gold	0	2	16 (2G)	13
Inductor 5	Copper	0	2	17.5 (2G)	13
Inductor 6	Copper	250	2	23.8 (4G)	16
Inductor 7	Silver	100	2	24 (4G)	16

Table 5-8: Material properties

	Relative Permittivity	**Relative Permeability**	**Bulk Conductivity (Simens/m)**
Al	1	1	2.8 e7
Gold	1	0.99996	4.1 e7
Copper	1	0.999991	5.8 e7
Silver	1	0.99998	6.1 e7

5.5 VCO Design Simulation

One of the most important tasks in integrated VCO design involves ensuring that the oscillation criteria are met over the desired frequency range. This task is not trivial and requires more than the usual transient and small signal analyses.

For example, a common practice in IC design is to run a long transient analysis, "ping" the supply or one of the critical nodes in the circuit with a sharp spike, and observe whether the circuit oscillates at the desired frequency. Although such an approach may be used to give some indication of whether the circuit is stable, it gives no indication of the margin with which the circuit meets or misses the stability criteria, and it certainly does not guarantee that the circuit will, in fact, oscillate when fabricated. An additional problem is that transient simulations in SPICE do not model electronic noise, which may become significant in some situations.

For VCO, the $g_m > \frac{1}{R_p}$ is the requirement, where $g_m = \sqrt{2\frac{W}{L}\mu_n C_{ox} I_{Dsat}}$, μ_n is the mobility and C_{ox} is the oxide thickness, the designer should perform a minimum of three analyses in verifying the proper functionality of an oscillator. First, one must generate magnitude and phase plots vs. frequency of the small-signal loop gain, looking for the magnitude to be larger than 2 at the phase zero-crossing to ensure startup. Second, one should generate and examine the Nyquist plot of the small-signal loop gain to ensure that the Nyquist instability criterion is met, that is, the plot encircles the (1, 0) point. Finally, the designer should run a transient analysis to verify that the circuit oscillates at the predicted frequency and characterize the swing of oscillation.

When Colpitts topology is selected for wideband application, the equivalent SPICE model of MEMS switch ON/OFF state derived in 2.2.1 is incorporated into VCO circuit simulation.

Figure 5-15 shows the topology of a differential Colpitts VCO that uses the MEMS switch to configure the LC tank elements. The tail current source is provided by an

NMOS current mirror. The switches can be MEMS switch or CMOS switch for comparison.

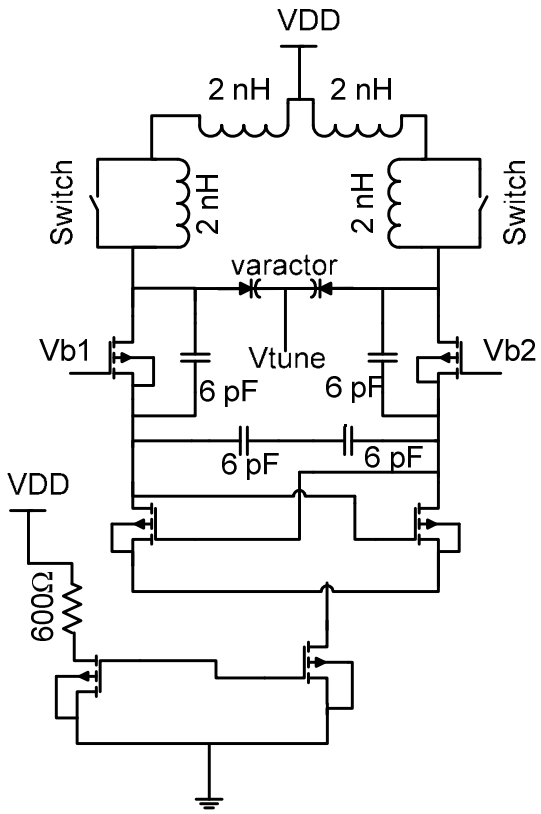


Figure 5-15: Schematic of Colpitts VCO using switched inductor; the switch can be MEMS switch or CMOS switch

Figure 5-16 shows the simulated center frequency change when the switch is ON/OFF. The amplitude difference is due to the serial resistance of the inductors. The center frequencies are 712 MHz and 1.35 GHz when the switch is in its ON/OFF position.

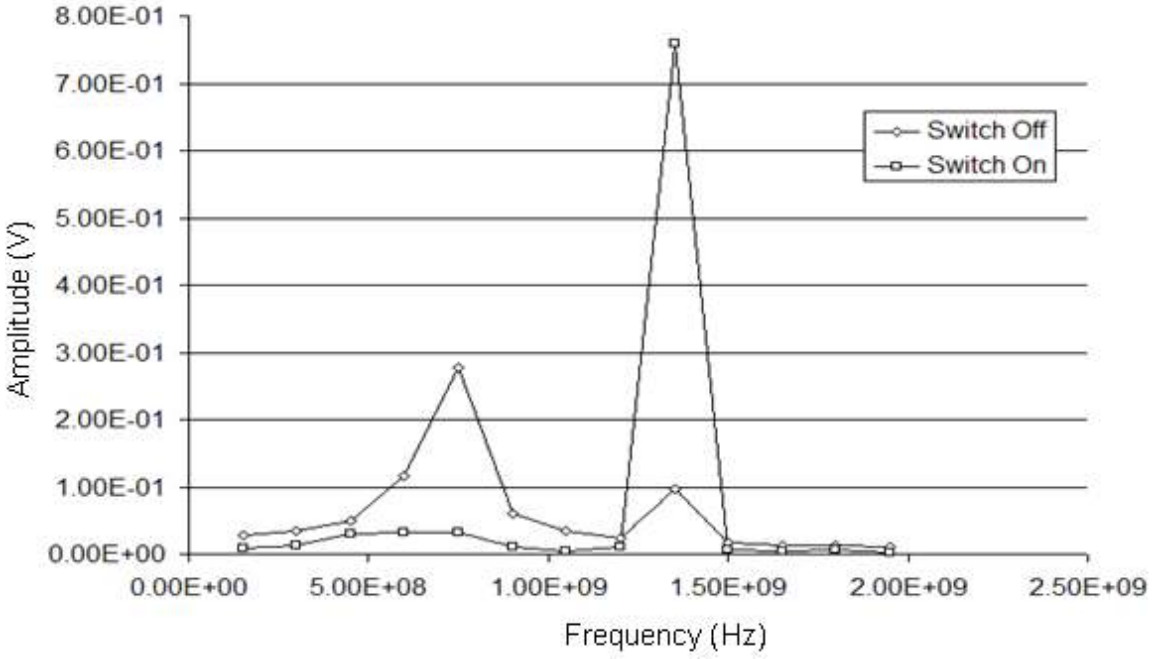


Figure 5-16: Simulation result of VCO frequency when switch ON/OFF with MEMS switch

With the edge-coupled capacitive MEMS switch SPICE model, the differential Colpitts VCO circuit has been simulated using Cadence SpectreRF. Figure 5-17 shows the phase noise comparison of the VCO with the MEMS switch and the CMOS switch. The VCO phase noise of 1.9 GHz at 100 K offset is about 20 dB better when the MEMS switch is used. The phase noise simulation is carried out at frequency offset from 100 Hz to 100 MHz.

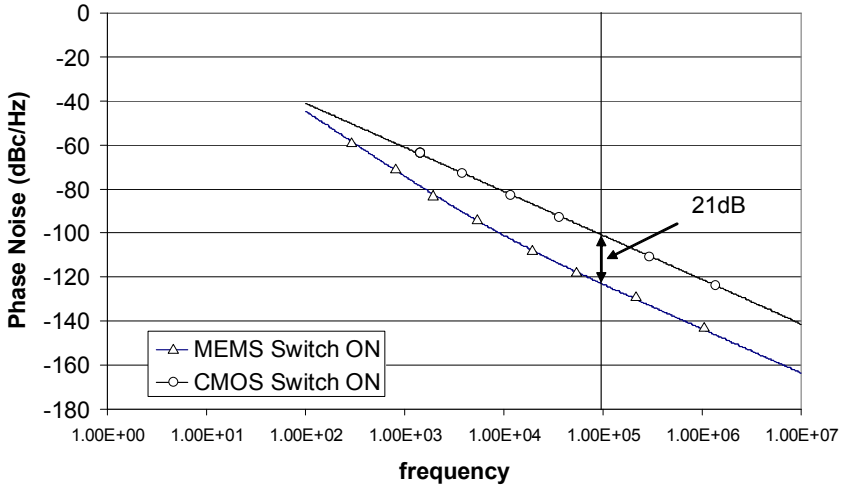


Figure 5-17: VCO phase noise comparison of CMOS switch versus MEMS switch

Figure 5-18 shows the MOSFET switched inductor, single ended Colpitt VCO that has been simulated to quantify the noise contribution of the MOSFET switches.

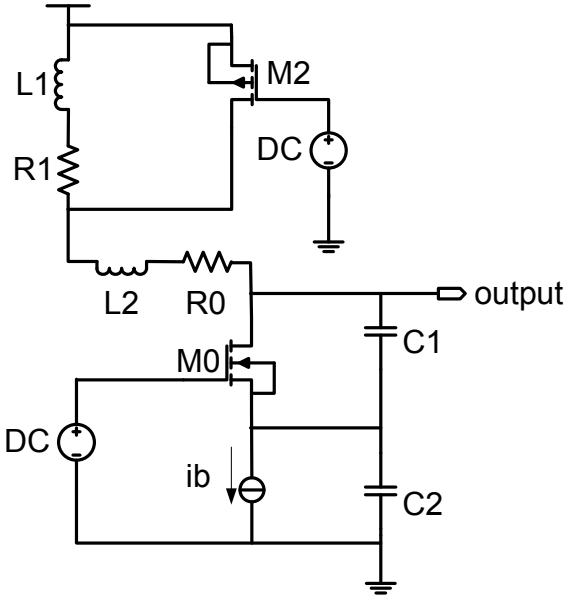


Figure 5-18: Schematic of switched inductor VCO using MOSFET switch

Table 5-9 shows the noise contributors in percentage when the PMOS switch is ON. This is the simulation result from Cadence SpectreRF. The results show that the MOSFET switches are the dominant source of noise. The major contributors of noise are the M_0 and M_2 active switches. M_2 contributes 37% of the total phase noise.

Table 5-9: Noise contributor when switch is ON

Device	Param	Noise Contribution	% Of Total
/M0	id	2.06971e-16	45.38
/M2	id	1.69175e-16	37.09
/R0	rn	4.60415e-17	10.09
/M2	fn	3.1904e-17	6.99
/R1	rn	1.69721e-18	0.37
/M0	fn	3.21744e-19	0.07
/L3	fn	0	0.00
/L3	rn	0	0.00
/L4	fn	0	0.00
/L4	rn	0	0.00

When the switch is OFF, the noise contribution of M_2 is only 0.62%, which is negligible compared to the M_0 and R_1, R_0 noise. Table 5-9 and Table 5-10 show that the MOSFET switch imposes a big noise impact on the VCO performance.

Table 5-10: Noise summary when switch is OFF

Device	Param	Noise Contribution	% Of Total
/M0	id	4.59877e-17	58.80
/R1	rn	1.8316e-17	23.42
/R0	rn	1.33187e-17	17.03
/M2	id	4.87383e-19	0.62
/M0	fn	9.40474e-20	0.12
/M2	fn	6.07033e-23	0.00
/L3	fn	0	0.00

5.6 Fabrication and Testing of Prototype VCO

Due to the contamination concern of postprocessing facility, we could not have the MEMS switch integrated with the VCO circuit. In order to prove the concept of switched inductor VCO, A MOSFET switched inductor VCO chip was fabricated using the MOSIS AMIC5 process. The layout of the VCO is shown in Figure 5-19. A single inductor VCO is fabricated for comparison purpose.

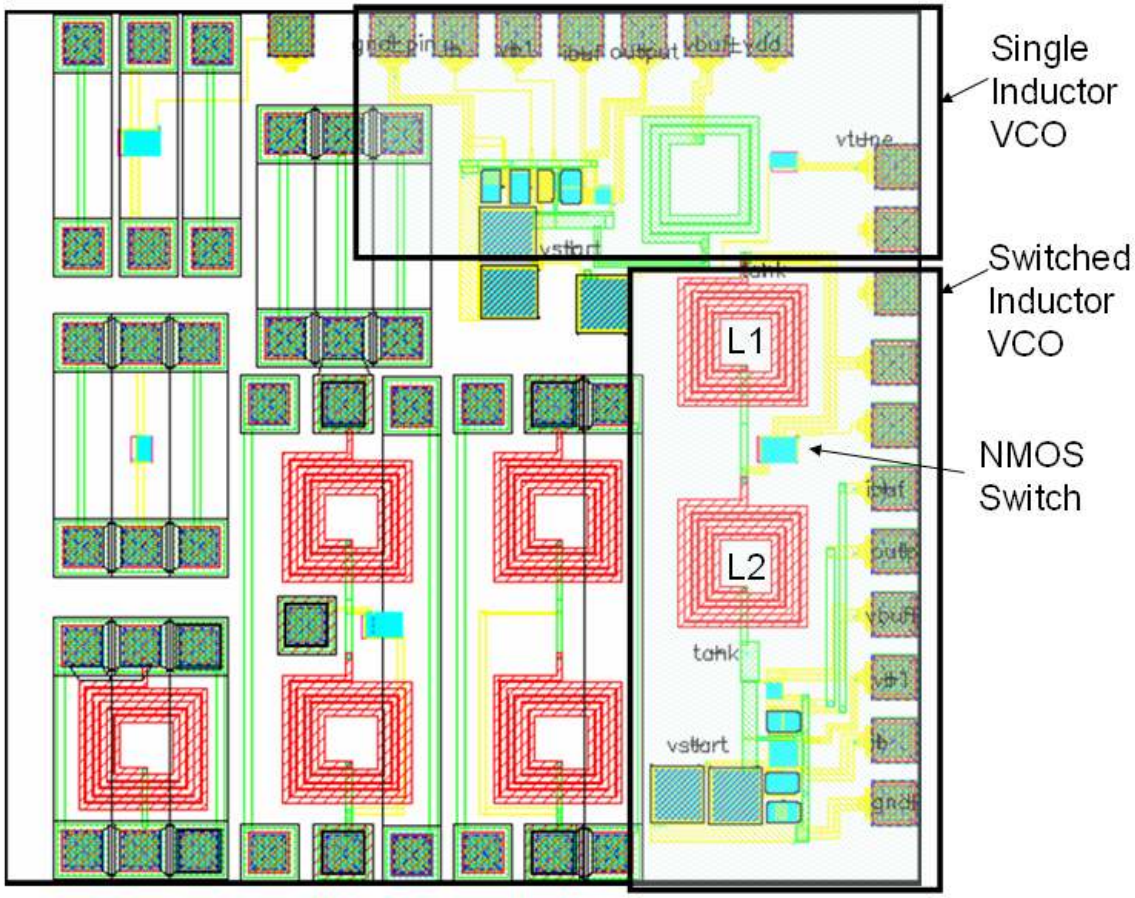


Figure 5-19: Layout of fabricated MOSFET switch inductor VCO

Test boards were designed and fabricated using Sun Stone PCB design services. The test chip are mounted on the PCB boards and tested in the lab. Figure 5-20 shows the schematic of the VCO test board.

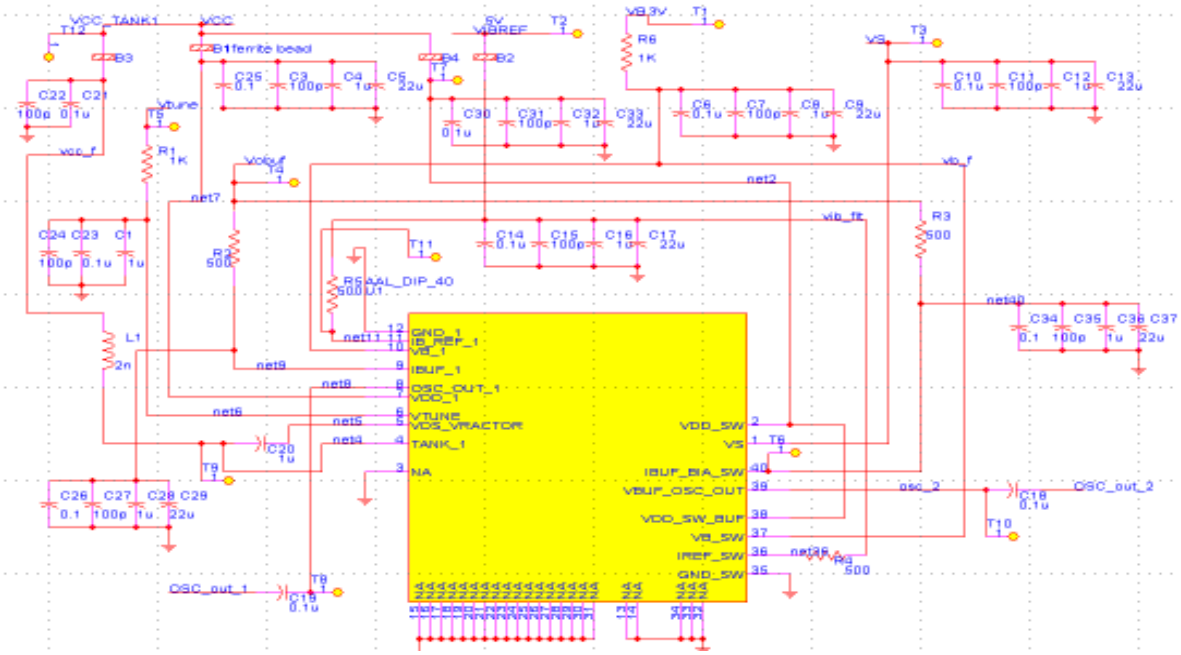


Figure 5-20: VCO test board schematic

Figure 5-21 shows the PCB layout of the VCO test board. Two similar VCOs are designed in the MOSIS T66AAL chip. The schematic is shown as Figure 5-18. One VCO has MOSFET switched inductors and one has a fixed inductor and tuning varactor. A few filtering capacitors are put on board to filter out high frequency noise.

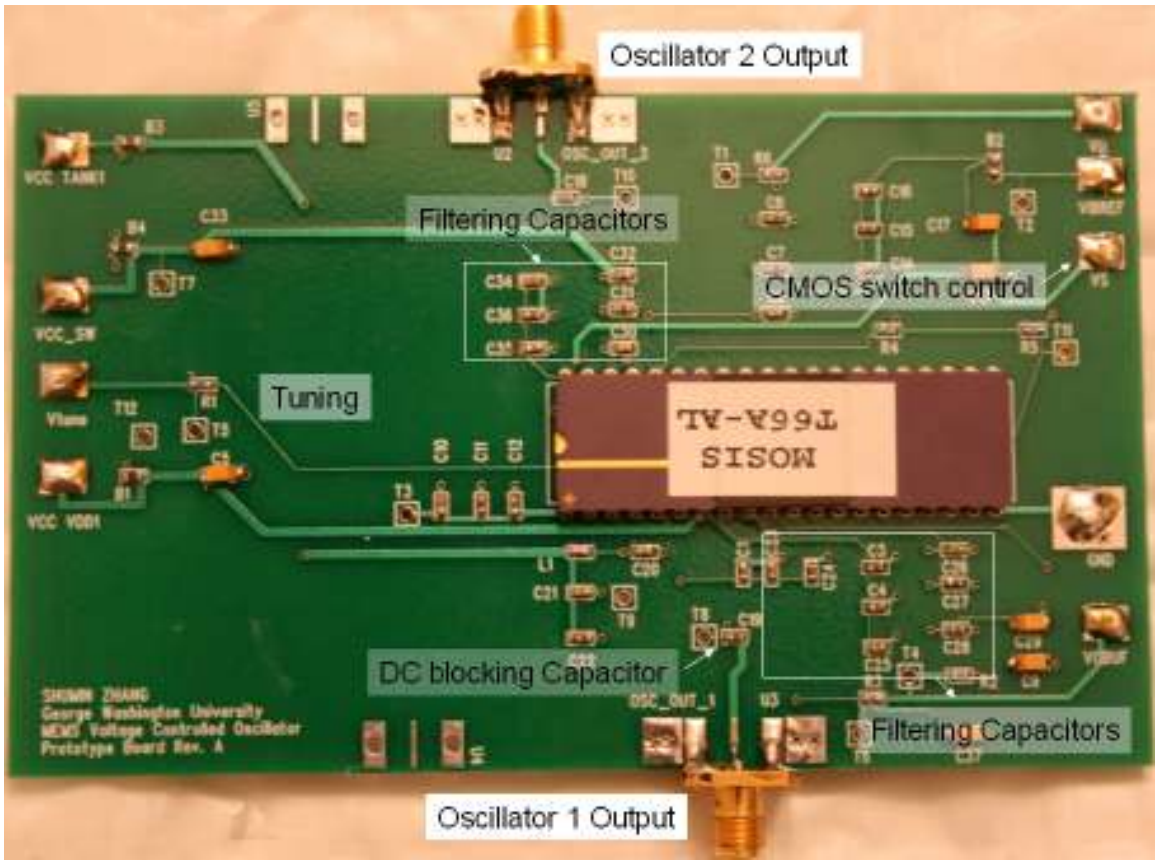
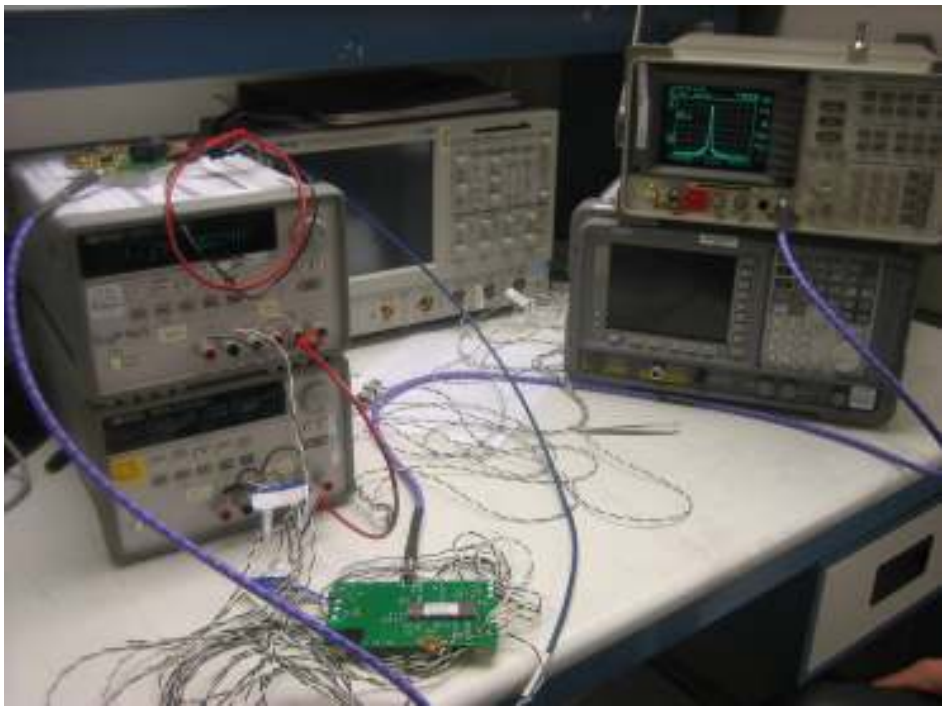
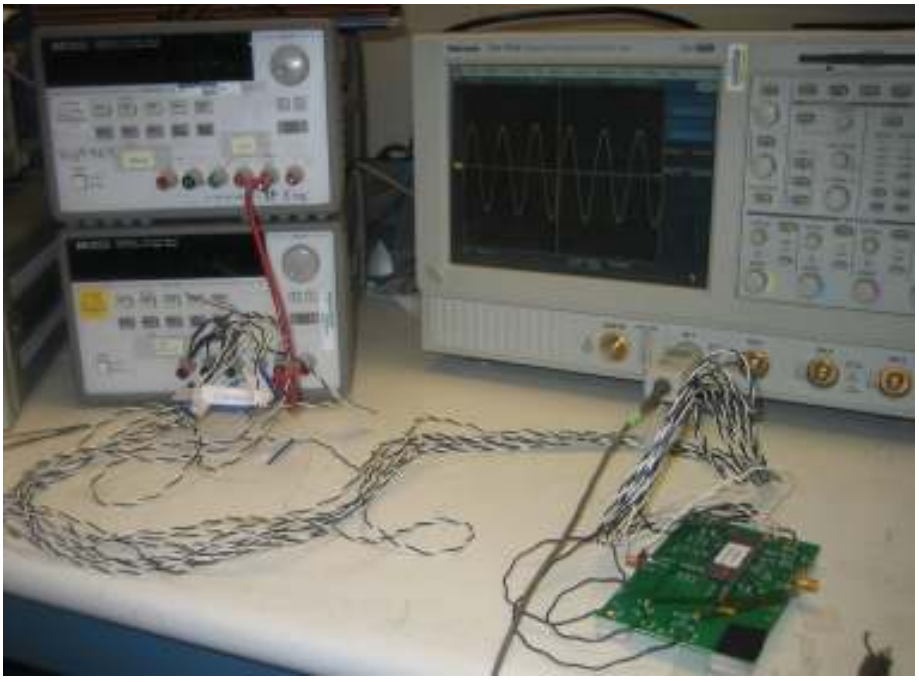


Figure 5-21: VCO test board with VCO 1 and VCO 2 (CMOS switch controlled variable inductor)

Oscillator frequency and output voltage swing were measured with an HP 8591 E spectrum analyzer. Supply and bias voltages were generated with two HP 6626A DC power supply. Figure 5-22 shows the lab testing of the prototype VCOs. And testing results are shown in Figure 5-23, through Figure 5-26.



(a)



(b)

Figure 5-22: VCO board test setup, (a) spectrum test, (b) transient test

The nominal oscillator bias conditions are bias Vb = 3 V, and supply Vdd = 5 V, tail current Itail = 30 mA. The nominal oscillation frequency is 625 MHz with -14 dBm output.

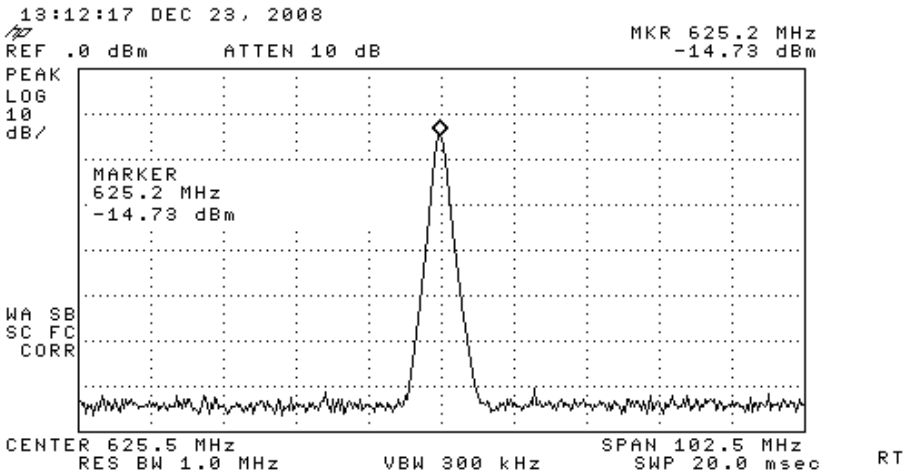


Figure 5-23: Testing frequency result of the prototype VCO 1

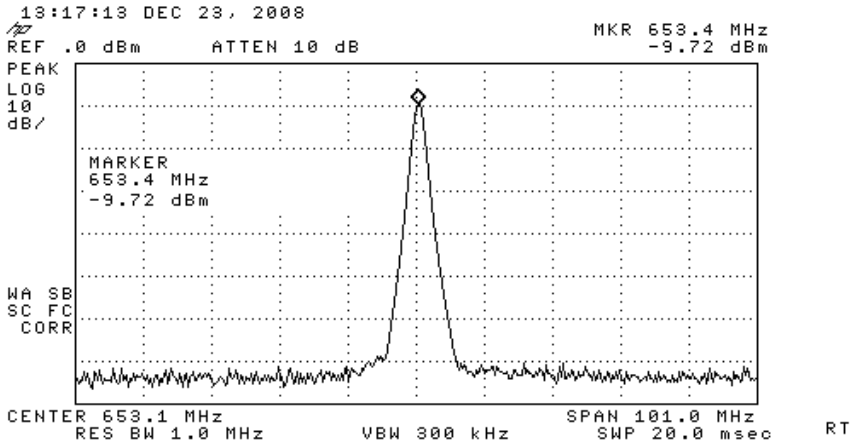


Figure 5-24: Testing frequency result of the prototype VCO 2 with switch On (Vs = 0)

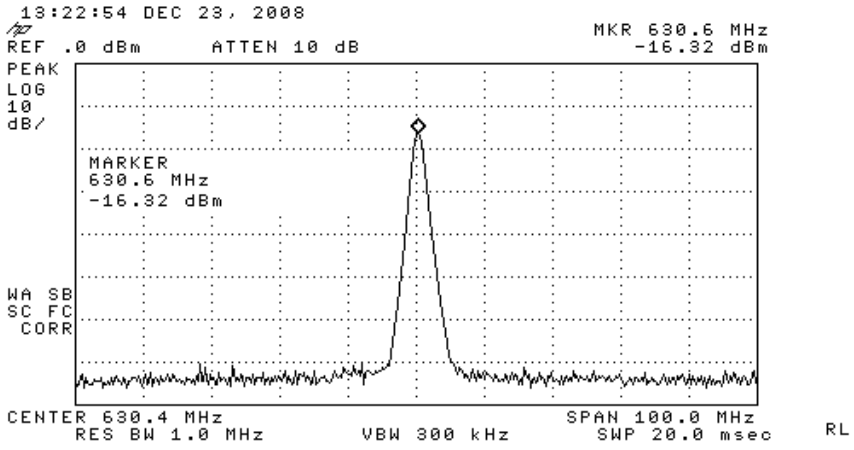


Figure 5-25: Testing frequency result of the prototype VCO 2 with switch Off (Vs = 5 V)

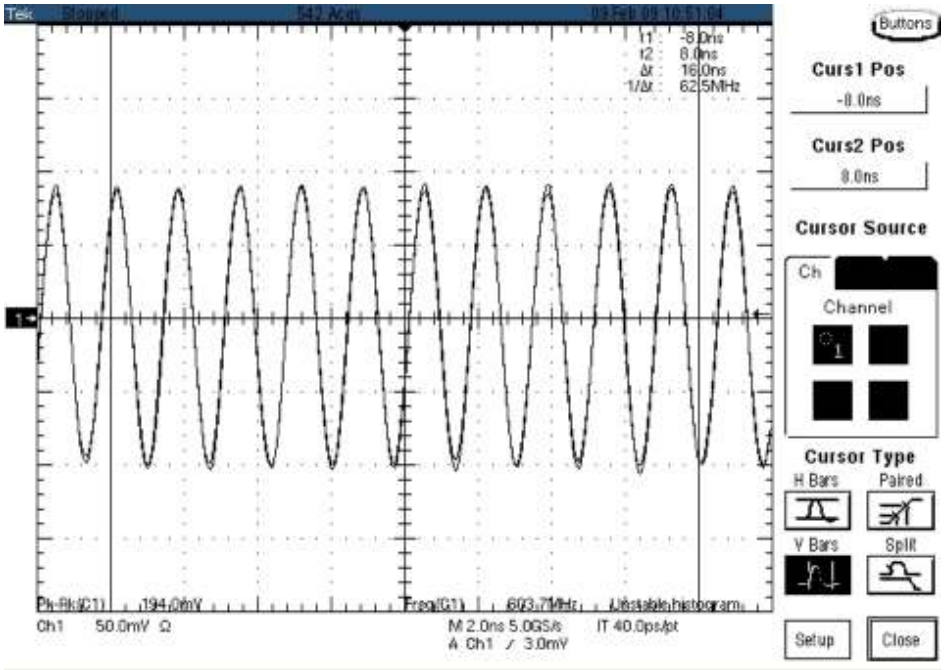


Figure 5-26: Testing transient result of the prototype VCO 1

Table 5-11 listed the measurement results of designed VCOs. The measured center frequency 625 MHz is lower than designed value 1.3 GHz. The reason is the large package (DIP 40) from the MOSIS with large bonding wire inductance. The bonding wire length from the die to the pad is about 15 mm. From the bonding wire inductance table at http://www.mosis.com/Technical/Packaging/pkg-intro.html#plastic, the bonding

wire inductance is about 18 nH, which is dominant. This design is limited by the packaging option through MOSIS.

Table 5-11: VCO characteristics with MOSFET switched inductor

Parameter	**VCO 1** **(w/o switched resonator)**	**VCO 2** **(with switched inductor, Switch on)**	**VCO 2** **(with switched inductor, Switch off)**
Core Current	30 mA	30 mA	30 mA
Inductance	1.67 nH	2.3 nH	4.6 nH
Supply Voltage	5 V	6 V	6 V
Center Frequency	625 MHz	653 MHz	630 MHz
Power	-14.73 dBm	-9.72 dBm	-16.32 dBm

From the testing, one issue was found: the tuning varactor was connected to a capacitor resulting in a DC bias problem of the varactor. For this reason the phase noise of the designed VCO cannot be characterized.

5.7 Summary of Broadband VCO Design

With the edge-coupled capacitive MEMS switch SPICE model, the differential Colpitt VCO circuits were simulated using Cadence SpectreRF. Phase noise and oscillator tuning range results were shown. Phase noise simulation was carried out at frequency offset from 100 Hz to 100 MHz. Cadence SpectreRF was used for the simulation. The VCO phase noise of 1.9 GHz at 100 K offset was about 20 dB better when the MEMS switch was used. Two VCOs (with MOSFET switch) were fabricated and tested on board.

Chapter 6 — Simulation of ET-Switch in Realizing Broadband Filter Application

This chapter describes how to use the designed RF MEMS switch in broadband analog filter application. The design presented in the section is an integrated 6th-order, elliptical lowpass filter that can be configured to L-band or S-band operation. The design is implemented using Frequency-Dependent Negative Resistor (FDNR) structures with configurable capacitor blocks utilizing MEMS switches. The operation of the filter is simulated using the Cadence SpectreRF simulator.

6.1 Introduction

High performance analog filters are typically used in electronic applications such as RF receivers, high-speed base-band data links, and digital video recording. These filters facilitate noise reduction and noise whitening, interference suppression, anti-aliasing, and conditioning for audio and IF (intermediate frequency) signals. Significant research has been conducted to design robust high-frequency integrated filters using active-RC, switched-capacitor, and Gm-C techniques [69].

The reason not to use direct passive filter implementation is that such structures are sensitive to process variations and poor quality factor of on-chip inductors. The quality factor of an inductor is limited by the resistive losses in metal traces and by induced eddy currents in both the metal strips and the substrate. Active-RC filters use less area, and these filters are commonly used in low frequency applications such as low frequency communication networks, signal processing circuits, and instrumentation systems. However, active-RC filters are limited to low-frequency filter implementations due to the high gain-bandwidth product requirements placed on the operational amplifiers (op-amps). Switched-capacitor filters can achieve higher frequency operation, larger

dynamic range, and better linearity, but the performance of these filters is limited by switching noise and clock feed through in high frequency applications [70, 71]. Wideband op-amps are required for switched-capacitor type filters because the sampling frequency has to be much higher than the filter bandwidth. A few architectures using transconductor capacitor (Gm-C) lowpass filters in the GHz range have been presented in literature [72, 73], demonstrating advantages of simplicity and electronic tuning at high frequencies. However, the stop-band rejection and tuning range of these filters are limited by the gain, bandwidth, and linearity of the amplifiers. For example, a biquad Gm-C lowpass filter in the GHz range would require amplifiers with bandwidths exceeding tens of GHz.

Another class of active filter design is based on FDNR structures. These filters have less dependency on the gain-bandwidth product of the operational amplifiers than previous designs to achieve similar performance, making them more amenable to high-frequency designs [70]. Furthermore, FDNR filters retain the passband insensitivity and sharp roll-off response characteristics of LC-ladder filters [74]. However, like all other integrated filter structures, FDNR filters in integrated form require tuning and/or configurability to compensate for the poor tolerances of integrated passive structures. This section demonstrates how MEMS switches enable large corner-frequency adjustments in high-frequency, lowpass filter designs.

The design presented in this section is an integrated 6th-order, elliptical lowpass filter that can be configured to L-band or S-band operation. The design is implemented using FDNR structures with configurable capacitor blocks utilizing MEMS switches. Section 6.2 gives the background for RF filter design. Section 6.3 describes the design and

analysis of the FDNR lowpass filter. Section 6.4 presents the simulation result of filter, and Section 6.5 gives conclusions.

6.2 Filter Design Background

Analog electronic filters are used in almost every electronics device, such as television, radio, and wireless handset. When the signal is digitized, an analog filter is usually required before the analog-digital converter to prevent aliasing. Figure 6-1 shows a wireless communication receiver. An RF band-select filter passes the appropriate band and applies it to the front-end, which includes a low-noise amplifier, mixer(s), and analog-to-digital (A/D) converter. The filter is necessary to reject undesirable components, which may fold into the band of interest during the sampling operation of the A/D converter and may be orders of magnitude larger than the desired signal.

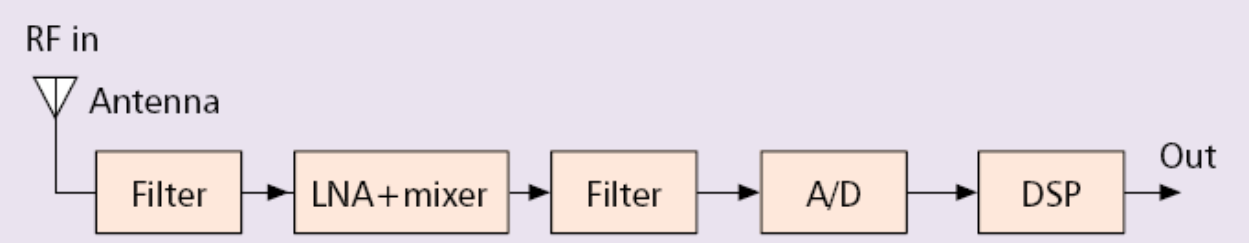


Figure 6-1: Receiver block diagram [69]

The range of signal frequencies that are allowed to pass through a filter with little or no change to the signal level is called the passband. The passband cutoff frequency (or cutoff point) is the passband edge where there is a 3 dB reduction in signal amplitude (the half-power point). The range of signal frequencies that are reduced in amplitude by an amount specified in the design and effectively prevented from passing, is called the stopband. In between the passband and the stopband is a range of frequencies called the skirt response, where the reduction in signal amplitude (also known as the attenuation) changes rapidly. As shown in Figure 6-2, there are four possible frequency domain

responses: lowpass, highpass, bandpass, and bandstop. [75] The filter order is equal to the number of poles in the frequency response of the filter. It is also equivalent to the number of reactive components in the ladder of the LC network.

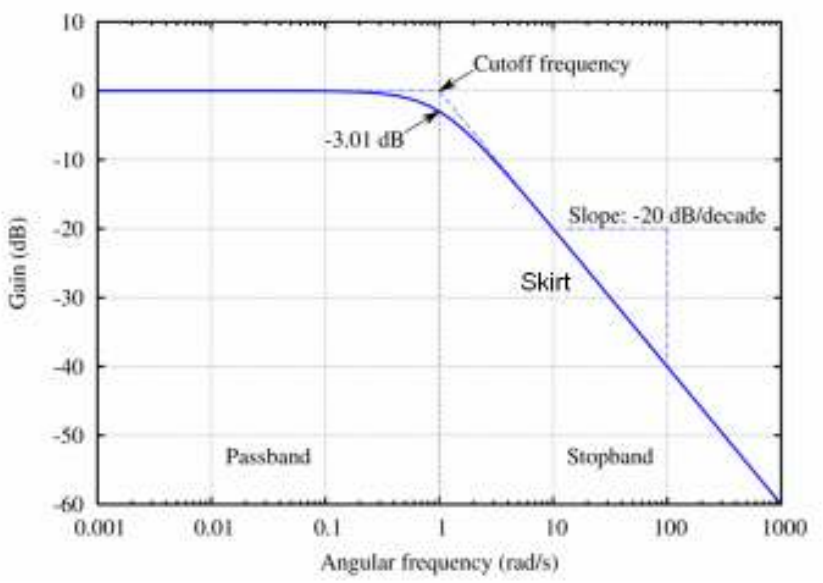


Figure 6-2: Frequency response of a lowpass filter

Analog filter can be passive or active. Passive filters use only resistors, capacitors, and inductors. Passive designs tend to be used where there is a requirement to pass significant direct current (above about 1 mA) through lowpass or bandstop filters. They are also used more in specialized applications, such as high-frequency filters or where a large dynamic range is needed. (Dynamic range is the difference between the background noise floor and the maximum signal level.)

In the design of integrated analog filters, the lack of good inductors is a big disadvantage. This drawback can be overcome by using an active analog filter. Active analog filters use operational amplifiers (op-amps) as the “active” element. Op-amps are combined with resistors and capacitors to produce a filter with the appropriate frequency response without the need for inductors. Active filters have the advantage of being

smaller than the passive types. However, active analog filters have several disadvantages: op-amps add noise and harmonic distortion to the signal, while the signal amplitude is limited by the op-amp's output slew rate and the power supply voltage.

Switched-capacitor filters provide a good alternative approach to the design of integrated active analog filters. Switched-capacitor filters belong to the category of analog sampled-data filters. Switched-capacitor filters are composed of arrays of capacitors, analog switches, and operational amplifier integrators. Compared to the conventional active-RC filters, they offer a unique advantage. Under certain conditions, the pole positions of the filter function are determined by capacitor ratios. Since capacitor ratios can be precisely controlled and are stable with temperature, very accurate filter transfer functions can be implemented [76]. However, the switched-capacitor filters require the input signal bandwidth much less than the switch frequency. This restricts the use of the switched-capacitor type filter in RF applications.

6.3 FDNR Lowpass Filter Design and Analysis

6.3.1 FDNR Structure

A frequency dependent negative resistance (FDNR) is an active circuit that behaves like an unusual capacitor. The schematic symbol for an FDNR looks like a capacitor with four plates and is also known as a D-element. The circuit of an FDNR is given in Figure 6-3.[75] FDNR circuits can be used to make an active filter based on a passive ladder filter design. In applications where an elliptical lowpass filter is required and an active filter is possible, FDNR filters can be used as an alternative to a biquad filter. FDNR filters require fewer op-amps than biquad filters of the same order, so they consume less power assuming the same type of op-amp is used. For the FDNR circuit to

work properly, the source impedance of the FNDR should be low and the load impedance must be high impedance.

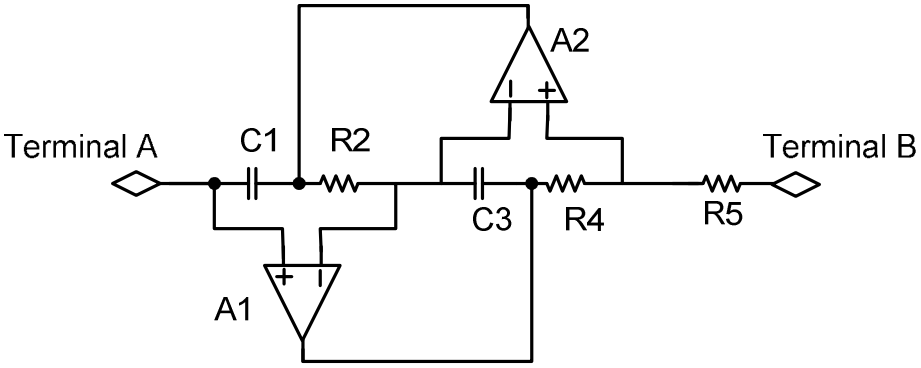


Figure 6-3: FDNR structure used to implement a D-element

The equation for the negative resistance D-element is as follows: [75]

$$D = \frac{R_2 R_4 C_1 C_3}{R_5} \tag{6.1}$$

FDNR-based filter design replaces the inductors and capacitors of a passive ladder filter with resistors and FDNRs. This gives the same low sensitivity to the component tolerances as the original ladder structure. If there are two signal paths in a system that must be closely matched in terms of amplitude and phase, an FDNR filter is the better choice. In decibel terms, a signal applied to an RC network has a rate of fall of 6dB/octave (a first-order filter). The same signal applied to an RD network has a rate of fall of 12 dB/octave. This double rate of decrease is the reason for the four plates in the D-element symbol rather than two in the capacitor symbol. [75]

To use FDNR structure in the filter design, a transformation of the passive components is required. FDNR elements are used to replace the capacitors in passive lowpass filters. Resistors are used to replace the inductors, and capacitors are used to

replace resistors. The transformation of the passive elements is shown in Figure 6-4. An example lowpass LC ladder filter is transformed to FDNR filter and shown in Figure 6-5.

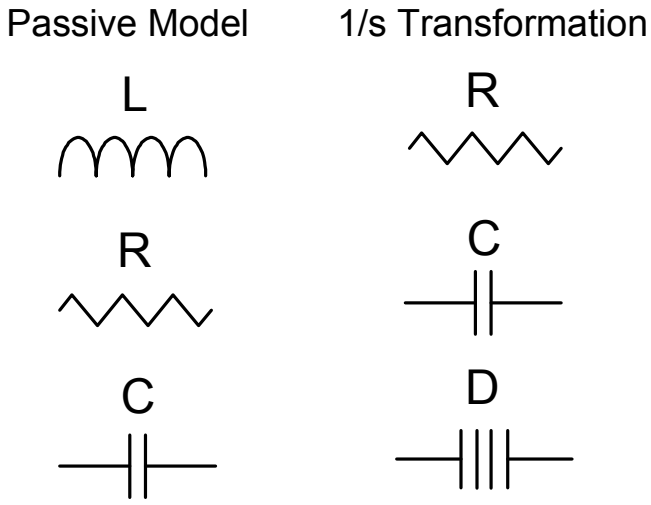


Figure 6-4: 1/S Transformation of passive elements

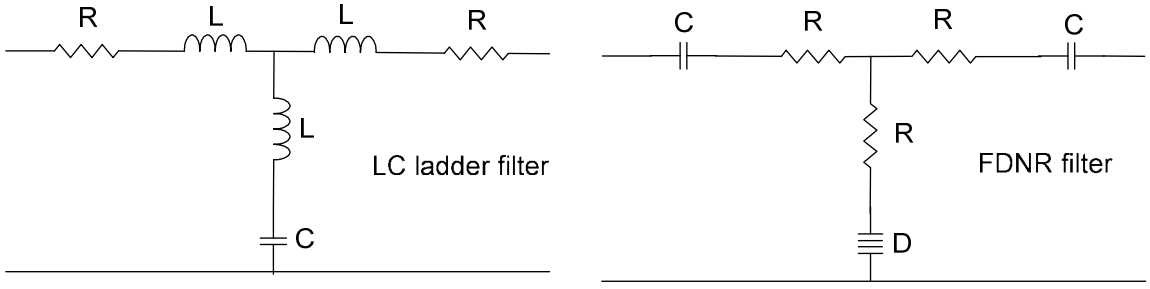


Figure 6-5: 1/S Transformation of passive LC ladder filter

6.3.2 Lowpass Filter Design

The lowpass filter implementation is based on a 6th-order elliptical LC ladder filter. Elliptical filters have a finite ripple in both the passband and the stopband response. Similar to Chebyshev filters, they exhibit a very sharp attenuation slope outside the passband. Elliptical filters are the most efficient filter type in terms of the component count necessary to implement the filter function [76]. For integration, it is desirable to obtain a filter design that does not rely on the use of area-consuming, low-Q integrated

inductors. Many filter designs using active circuits have been documented in literature; however, most of them are limited to low-frequency operation by the performance requirements placed on the active circuitry [69].

The basic building block of active filter design is the biquadratic filter function, often referred as the biquad. It is a second-order transfer function as expressed in the following equation [76].

$$H(s) = \frac{a_2 s^2 + a_1 s + a_0}{s^2 + b_1 s + b_0} = \frac{a_2 (s + z_1)(s + z_2)}{(s + p_1)(s + p_2)} \tag{6.2}$$

where s is the complex frequency variable, and z_i and p_i are the respective zeros and poles of the transfer function. The biquad transfer function can be implemented with a single operational amplifier and can serve as a building block for complex filter functions.

The architecture chosen for this design uses FDNR structures implemented by using generalized impedance converters. The operational amplifiers used in these structures have been found to yield nearly ideal frequency response results in L-band and S-band filters as long as a gain-bandwidth product greater than 15 GHz can be achieved. Such op-amps were realized by two-stage amplifiers in SiGe bipolar technology. The f_T of the NPN transistors used in this design is approximately 65 GHz at 1 V VCE. The resulting open-loop gain of each op-amp is 40 dB as shown in Figure 6-9.

In order to enable use of FDNR structures, the impedances of all components in the LC ladder are multiplied by 1/s. While the overall transfer function of the filter remains unchanged, this technique has the effect of transforming inductors into resistors, resistors into capacitors, and capacitors into D-elements with $1/s^2$ dependence. The resulting 6th-order elliptical filter structure is shown in Figure 6-6.

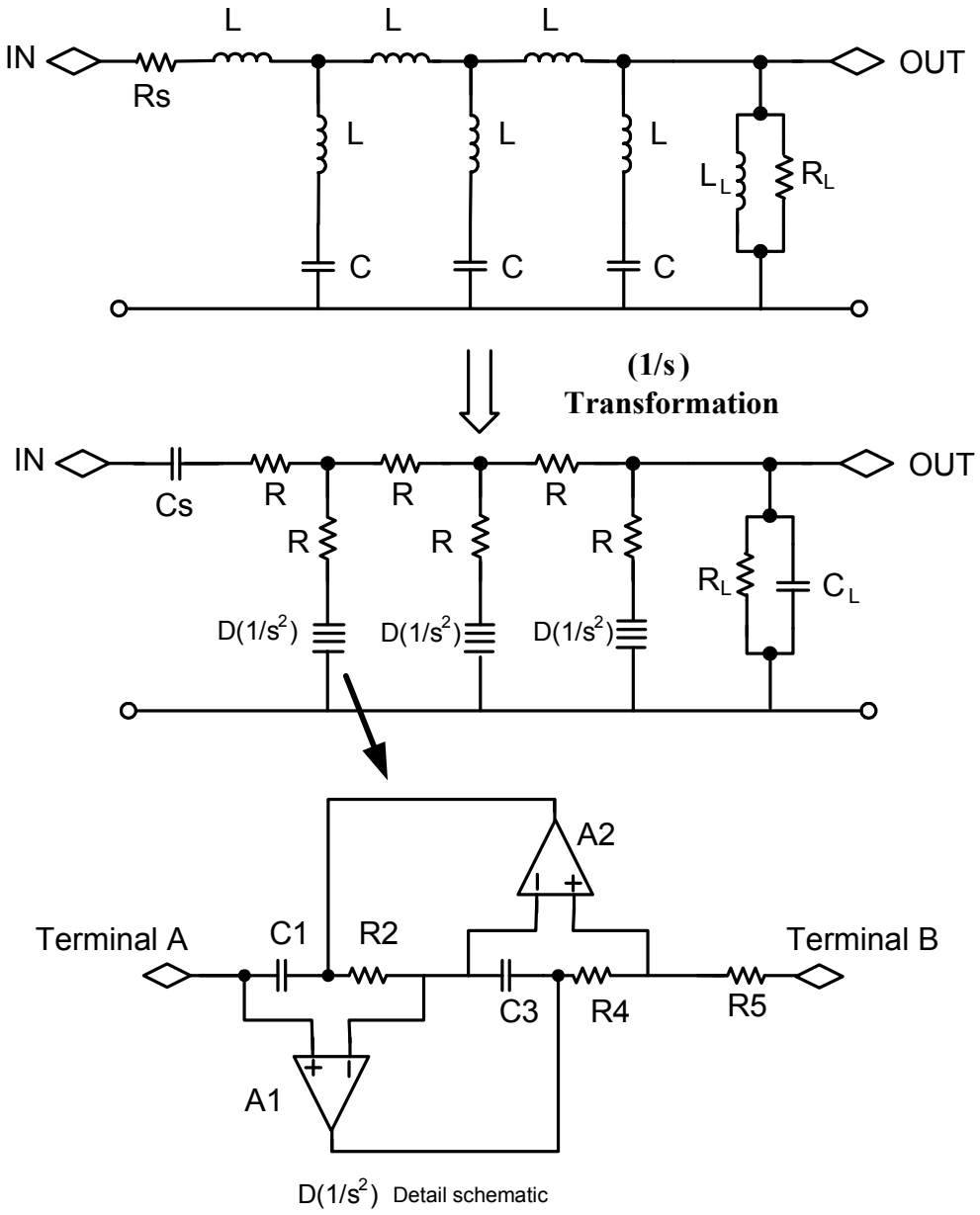


Figure 6-6: Sixth-order elliptical filter structure obtained via 1/s multiplication of the component impedances in an LC Ladder

The D-elements can be implemented using FDNR structures as shown in Figure 6-6. The input impedance of these structures is given by Equation (6.3). The corner frequency of the lowpass filter structure discussed above can be configured by adjusting the values

of capacitors C_S, C_L, C1, and C3 in the circuit shown in Figure 6-6. The design is scaled such that all these capacitors have the same value. Thus, the configurable capacitor blocks can all be made identical for optimal matching. [75]

$$Z_{in,FDNR} = \frac{1}{s^2} \cdot \frac{R_5}{R_2 R_4 C_1 C_3} \tag{6.3}$$

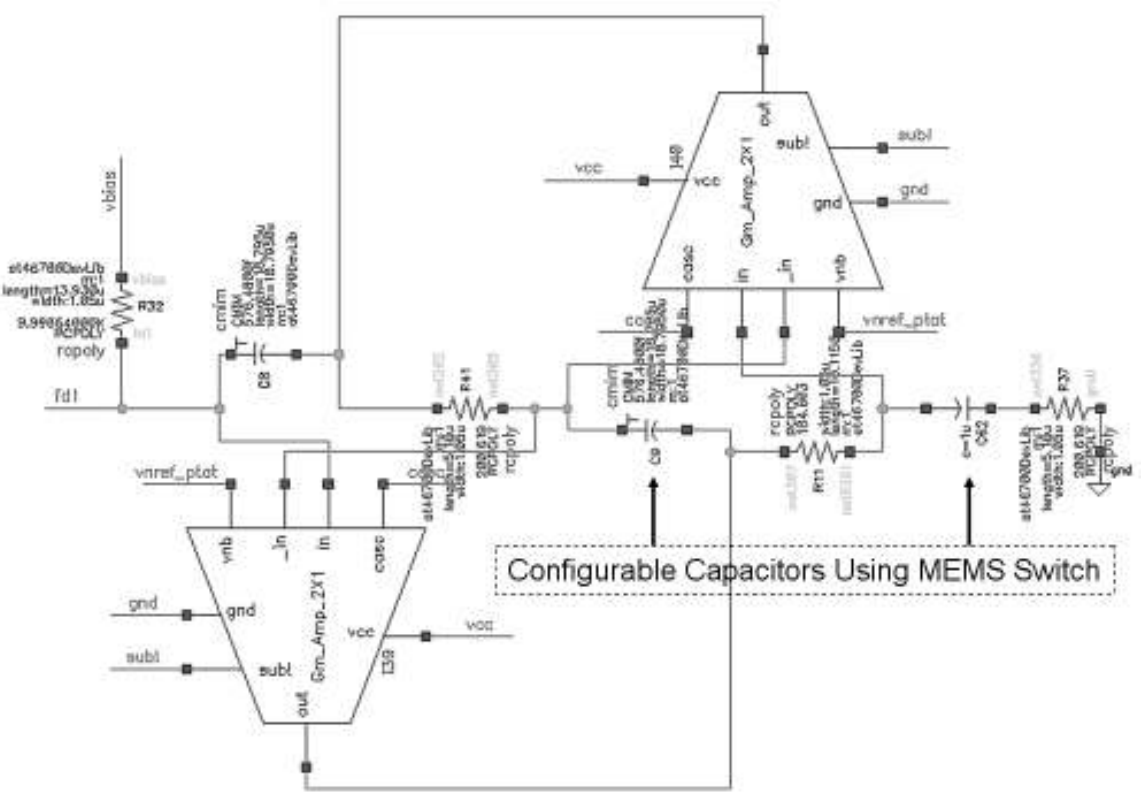


Figure 6-7: Schematics of an FDNR structure implementation

6.3.3 Op-amp Design

For high-frequency filter design we prefer to use a simple op-amp circuit structure to avoid internal transconductor nodes forming higher-order poles and high-ohmic nodes. The op-amp is one of the critical blocks of lowpass filter (LPF) design. The schematic of the op-amp, indicated as Gm_Amp_2X1 in Figure 6-8 and used as a building block in the FDNR structure, is shown in Figure 6-3.

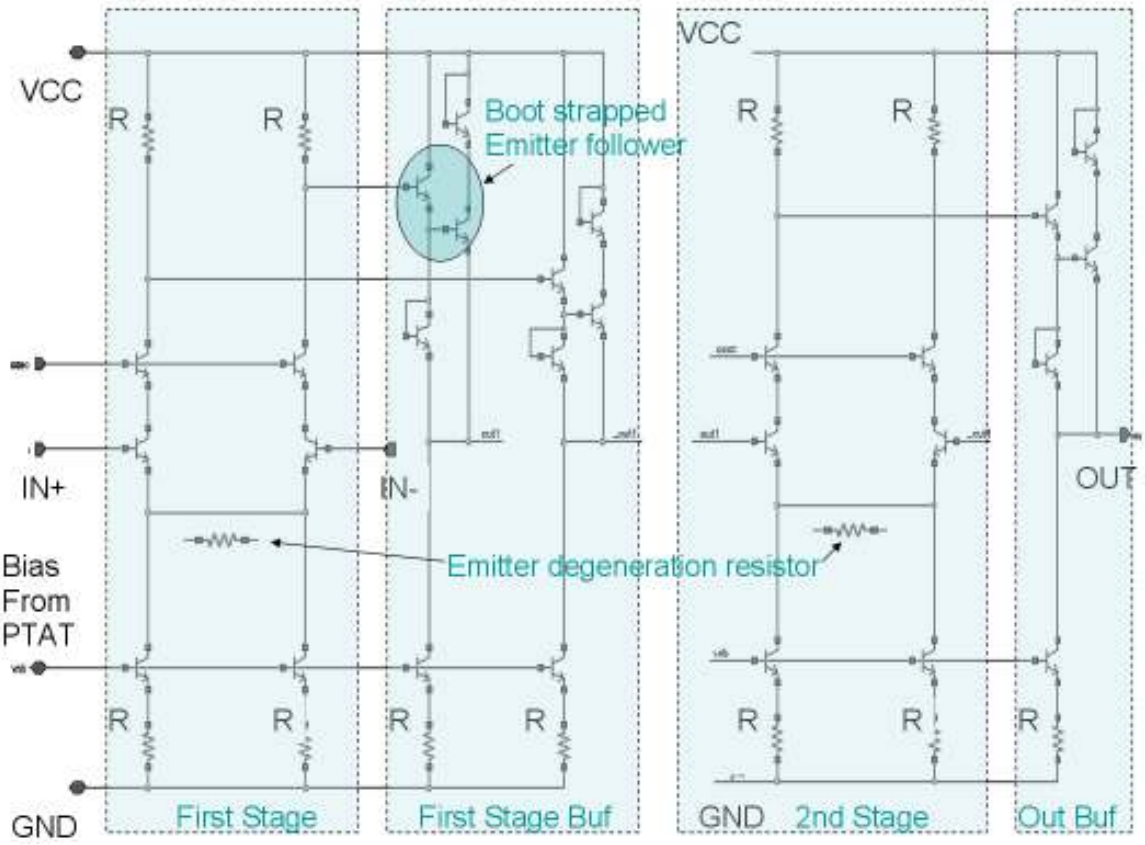


Figure 6-8: Schematics of the two-stage Op-Amp (Gm_Amp_2X1)

The op-amp is a two-stage differential amplifier with resistive loads, followed by an emitter-follower buffer. The cascaded architecture provides high output impedance and better input-output isolation. A boot-strapped emitter-follower structure is used to obtain wider bandwidth operation as well as sufficient output drive strength. A PTAT tail current source is used to bias the amplifier so that temperature variations can be reduced. As can be seen from Figure 6-8, emitter degeneration is reduced (emitter degeneration resistors are set to zero) so as to provide enough transconductance over process variation. However, this compromises linearity requirements of the filter. The small-signal gain response of the designed op-amp is shown in Figure 6-9.

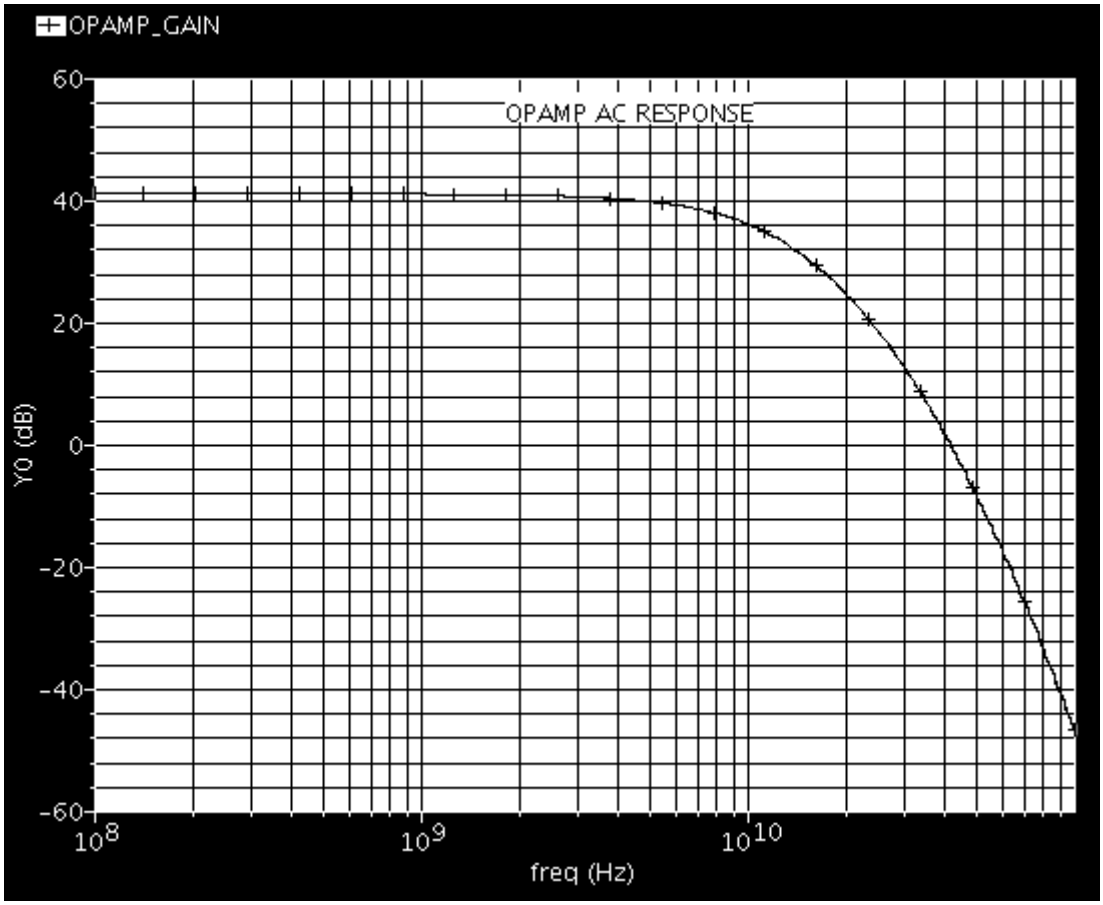


Figure 6-9: Small-signal response of the two-stage Op-Amp

The bias current for the amplifier circuit mentioned in the above section is designed using the reference current, which is obtained by forcing a difference between the base-emitter voltages of two transistors across an integrated resistor. It can be shown that the secondary effects arising from the temperature dependence of resistor are negligible in the normal range of temperature. The schematic of the PTAT reference generator circuit using translinear cross-quad structure is shown in Figure 6-10. Based on common current mirror circuit, the equations governing the characteristics of circuit are given by:

$$I_{out} = \frac{V_t}{R} \cdot \ln\left(\frac{A_5 A_7}{A_6 A_4}\right) \tag{6.4}$$

where A_4, A_5, A_6,, A_7 are the area of Q_4, Q_5, Q_6, Q_7 transistors, R is the resistance of R_{10}, and V_t is the threshold voltage of all transistors, which is approximately 26 mV at 300 K.

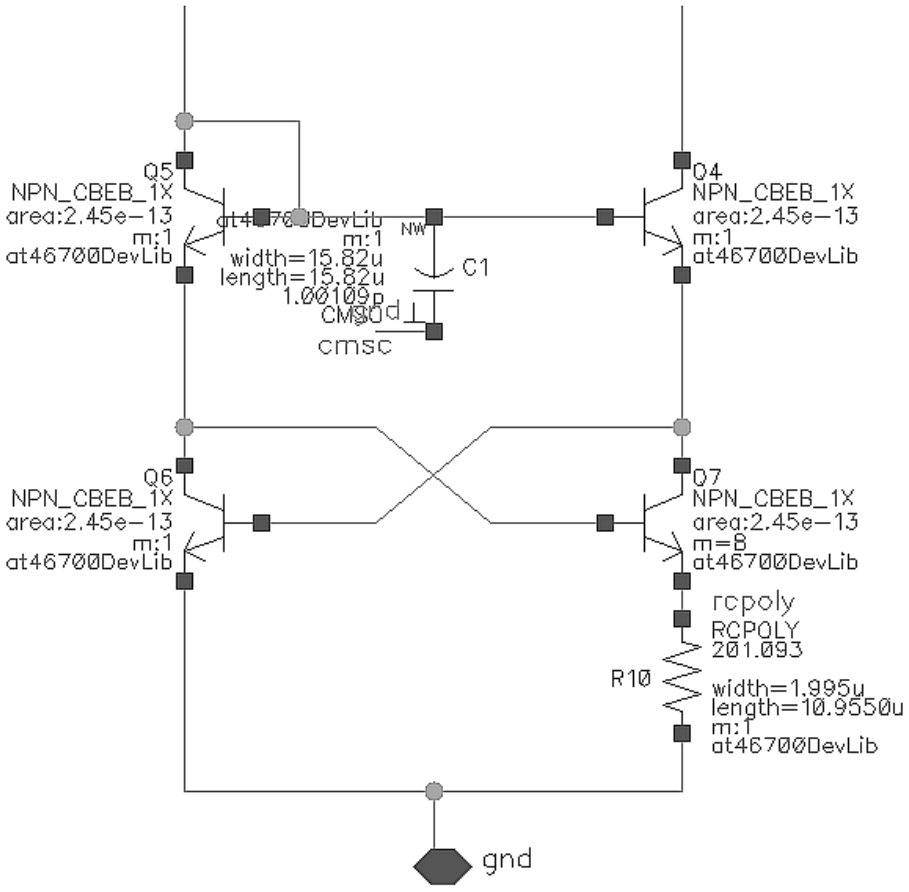


Figure 6-10: PTAT reference using translinear cross-quad

6.3.4 Configuring the Lowpass Filter

The corner frequency of the lowpass filter structure discussed above can be configured by adjusting the values of capacitors C_S, C_L, C_1, and C_3 in the circuit shown in Figure 6-6. The design is scaled such that all these capacitors have the same value. Thus, the configurable capacitor blocks can all be made identical for optimal impedance matching.

The configurable capacitor structures are enabled by MEMS switches. The structure of the configurable capacitor Ca and Cb is shown in Figure 6-11. The letter "T" in the figure indicates the top plate of the metal-insulator-metal (MIM) capacitors. The MEMS switch model is generated from Section 2.2 and described in Figure 2-32 [77].

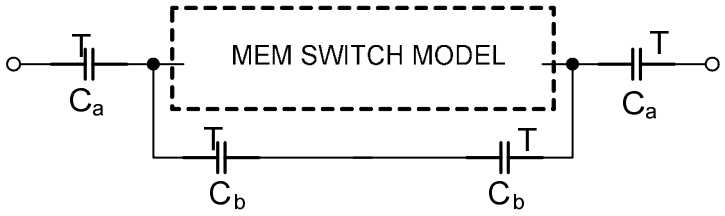


Figure 6-11: C1 and C3 configurable capacitor block showing a model of the MEMS switch

The main challenge in utilizing MEMS switches in RF applications is their poor and variable quality factor (Q). The frequency dependence and value of the MEMS-switch Q are different in the ON and OFF states. As shown in Figure 6-11, the configurable capacitor block was designed to address this limitation. Rather than connecting the switch directly to sensitive nodes in the filter, it is placed in parallel with high-Q MIM capacitors and coupled to the filter through two more MIM capacitors. This structure transforms the relatively high series resistance to a much lower resistance seen at the terminals of the capacitor block. The filter corner frequency is set by choosing the desired values for the MIM capacitors C1 and C2. From HFSS simulation of the switch, the MEMS switch appears approximately as a capacitor of 31 fF and 18.4 pF in the OFF and ON states, respectively. The capacitance of the overall block is determined largely by the values of two or four series MIM capacitors as long as Ca and Cb have values in the range 300 fF to 1.8 pF.

6.4 Filter Simulation Results

The GDSII netlist of the switch is taken by HFSS along with the AMI C5 process data, and the 3-D model is created and meshed. Then HFSS is used for the EM simulation. The simulation result of displacement is fed to HFSS for switch On/Off condition simulation. The HFSS outputs S-parameters in touchstone format.

The 6th-order elliptical filter performance was simulated in Cadence by using s-parameter definitions of the MEMS switch in the ON and OFF states, generated using Ansoft's HFSS 3-D E-M simulator. The s-parameter files were imported into Cadence to enable cosimulation with the bipolar and passive devices in the design.

The capacitor block was characterized by analyzing the equivalent capacitance and quality factor in the ON and OFF states of the switch. To obtain the desired cutoff frequencies of approximately 1 GHz and 3 GHz for the overall filter, the values of Ca and C_b in the capacitor block were set to 1.5 pF and 1.0 pF, respectively. Simulations of capacitance and quality factor versus frequency demonstrated two main limitations of this MEMS-based implementation of the configurable capacitor block. In the ON state, the finite, variable capacitance of the MEMS switch causes variation with frequency of the overall equivalent capacitance. In the OFF state, the MEMS switch has no appreciable effect on the equivalent capacitance, but it begins to significantly degrade the quality factor of the overall capacitor block.

The simulations in this work demonstrated that the overall filter frequency response is not significantly degraded by the limited performance of the capacitor block. For comparison, the filter response was plotted for three different configurations in each switch position: with both the switches and op-amps as real circuits, with both switches

and op-amps as ideal circuits, and with real op-amps and ideal switches. For purposes of this work, ideal switches were modeled as ideal capacitors of 1 fF and 1 nF in the OFF and ON states, respectively, while the ideal op-amps were modeled to have an open-loop gain of 1000 V/V and infinite bandwidth. By comparing the three results in each switch state, the effect of using real MEMS switches and real op-amps with finite gain-bandwidth products becomes apparent. The filter response with the switch in the OFF state is shown in Figure 6-12, and the response with the switch in the ON state is shown in Figure 6-13. The filter circuits are shown in Figure 6-6 [77].

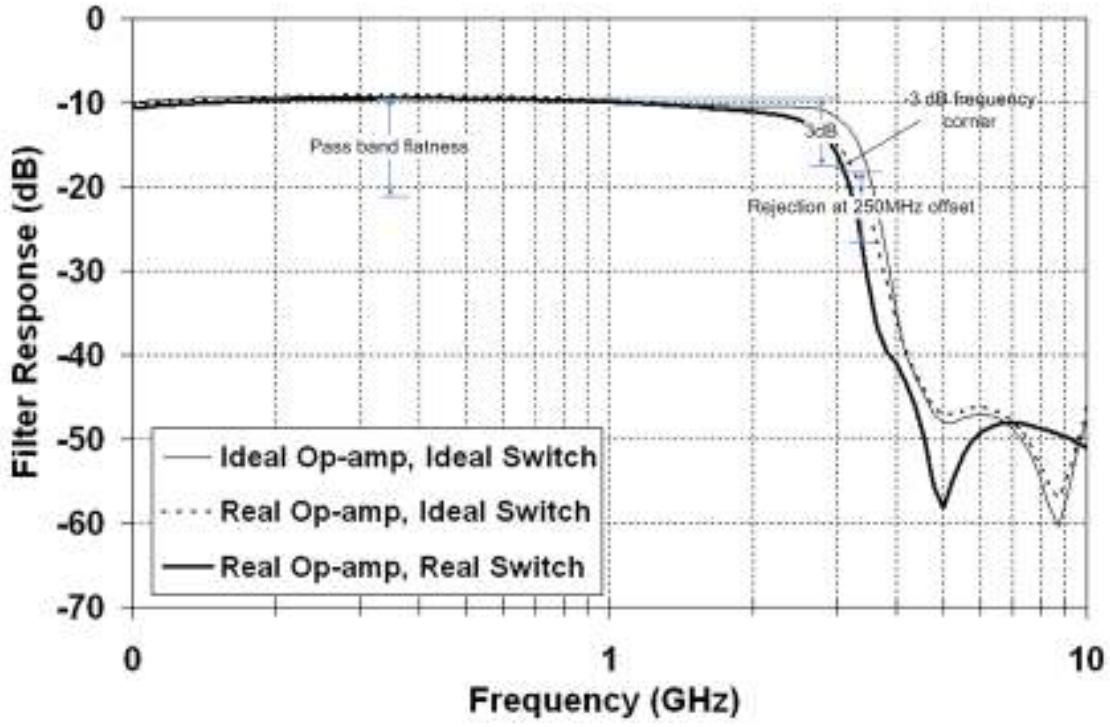


Figure 6-12: Filter response with the switch in the OFF position (S-band Configuration) showing measurements of 3 dB frequency corner

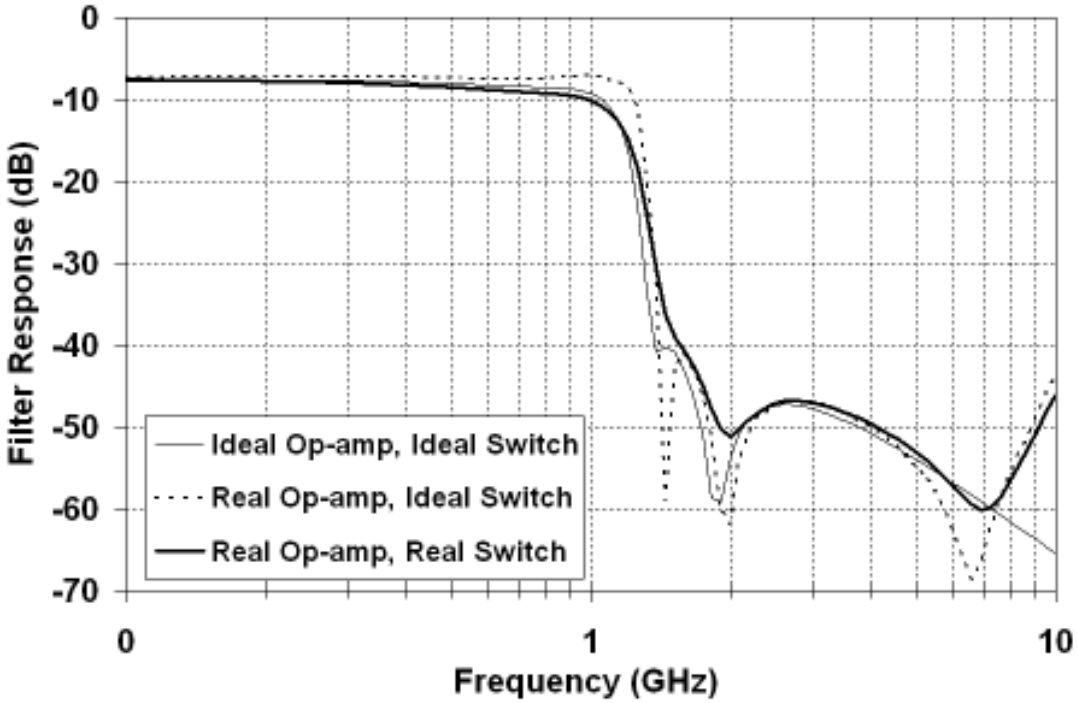


Figure 6-13: Filter response with the switch in the ON position (L-band configuration)

Finally, this work analyzed some performance metrics of the designed 6th-order elliptical lowpass filter based on the simulation results. These results correspond to the real circuit implementation of the entire filter and all associated bias circuitry. The performance results are measured from the simulation curves and summarized in Table 6-1.

Table 6-1: Filter design performance metrics

	L-band	S-band
-3 dB frequency corner	0.94 GHz	3.06 GHz
Rejection at 250 MHz offset from 3 dB corner	10.8 dB	2.6 dB
Rejection at 500 MHz offset from 3 dB corner	29.0 dB	9.6 dB
Rejection at 1 GHz offset from -3 dB corner	40.2 dB	26.2 dB
Pass-band flatness (100 MHz – 0.8·f-3 dB)	1.6 dB	1.3 dB

Table 6-1: Filter design performance metrics

	L-band	S-band
Mid-passband insertion loss (at 0.5·f-3 dB)	-8.4 dB	-10.3 dB
Quiescent power dissipation	0.457 W	0.457 W

6.5 Filter Design Conclusion

This section presented a new, MEMS-based approach to designing configurable integrated high-frequency, low-pass filters. The frequency corner of the filter was demonstrated to be configurable over a very wide range – from 944 MHz to 3.06 GHz. Additional research is required to characterize the noise and linearity performance of this filter architecture.

Chapter 7 — Conclusion and Future Work

7.1 Conclusion

A novel, vertical, thermal-actuated CMOS-compatible MEMS switch for ISM/WLAN band applications is designed, fabricated, and characterized. This series capacitive MEMS switch solves the substrate loss and downstate capacitance degradation problems commonly plaguing MEMS switches. The switch uses finger structure for capacitive coupling. The vertical bending characteristics of bimorph cantilever beams under different temperatures are utilized to turn the switch on and off. A set of electrical, mechanical, and thermal models is established, and cross-domain, electro-thermo-mechanical simulations are performed to optimize the design parameters of the switch. The fabrication of the switch is completely CMOS-process compatible. The design is fabricated using the AMI 0.6 μm CMOS process and a maskless reactive-ion etching (RIE) process. The measured results show the insertion loss and isolation are 1.67 dB and 33 dB, respectively, at 5.4 GHz, and 0.36 dB and 23 dB at 10 GHz. Thermal actuation threshold voltage is analyzed, simulated, and measured. The actuation voltage is 25 V. This switch has a vast number of applications in the RF/microwave field, such as configurable voltage control oscillators, filters, and configurable matching networks.

Then the MEMS switch model is simulated with a differential Colpitts VCO, and frequency band selection was achieved by switch inductors in and out of the circuit. The MEMS switch is characterized using 3-D EM simulator in this work, and the equivalent SPICE model has been extracted and used in the circuit simulation. The simulation result shows significant improvement for the VCO phase noise over the MOSFET switched VCO.

A new, MEMS-based approach to designing configurable integrated high-frequency lowpass filters has been developed. The frequency corner of the filter was demonstrated to be configurable over a very wide range – from 944 MHz to 3.06 GHz. Nevertheless, this approach has several drawbacks. First, it is important to note that the transition band rejection degrades significantly in the higher S-band configuration. Overall, the filter performance is slightly degraded by the variable capacitance and low Q of the MEMS switch. Since the filter architecture is passive in nature, with the active elements employed outside of the direct signal path, the filter suffers from significant passband insertion loss. Further, the op-amp gain-bandwidth requirements in the FDNR structures, though relatively low compared to other architectures, require significant power dissipation to work.

7.2 Future Work

Even though significant progress was made to develop a high-quality CMOS-compatible RF MEMS switch, a few problems still need to be further addressed. One area of improvement lies in power consumption. To reduce the power consumption of the switch, the electrostatic hold method can be combined with the thermal actuation method currently used. The proposed new method is described as the following: initially, thermal actuation voltage is applied to make the rotor move toward the substrate, after the rotor reaches its flat position; switch is in its on state. Then the electrostatic voltage can be used to hold the rotor in place. By using this combined thermal and electrostatic actuation method, the DC bias current after the switch is turned on can be lowered significantly, and the power consumption of the switch is reduced. Other drawbacks of the designed switch are high activation voltage and the slow switching time of thermal actuated switch,

which is about several hundred microseconds [78]. The improvement of the switching speed and actuation voltage can be achieved by combining the electrostatic and thermal actuation as well. The switch can also be implemented as a DC contact switch giving the specific application. The operation of the switch is quite general, so it can be used in other physical domains such as fluid control, optical switching, and gyros. The designed switch uses sidewall to form coupling capacitance; the value of the coupling capacitance depends on the sidewall area. With better technology and more layers of metal, the larger number of metal layers can increase the size of sidewall coupling area thus reducing the insertion loss of the switch at its ON state. Furthermore, it is possible to deposit metal on the sidewall to improve the capacitance coupling. All these methods can increase the switch On/Off capacitive ratio. For the heater design, different types of heaters can be developed, such as the N-Well heater and the metal heater. The heater optimization can lead to lower actuation voltage and more reliable operation. Because this switch is targeted to be used for RF applications, the temperature rise implies higher thermal noise, and this aspect needs to be characterized and optimized. The lifetime of the switch needs to be characterized as well.

In this work, the MEMS switch is not integrated with the multiband VCO on the same chip; one of the future works is to integrate them on the same CMOS chip. The op-amp power consumption presented in the filter design has not been optimized, and the power reduction is part of the future work. Furthermore, additional research is required to characterize the noise and linearity performance of the MEMS configurable filter architecture.

This work has explored the application of voltage controlled oscillator and filter; however, there are many other types of applications that can be integrated with the MEMS switch, for example, configurable matching network and configurable power amplifier.

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APPENDIX A

In this section, an equivalent electrostatic actuated switch model is established, the pull-in static voltage is analyzed, and threshold for electrostatic actuation is determined. ANSYS software is used for pull-in voltage simulation. Figure 0-1 shows the design flow using ANSYS tool for the electrostatic pull-in analysis.

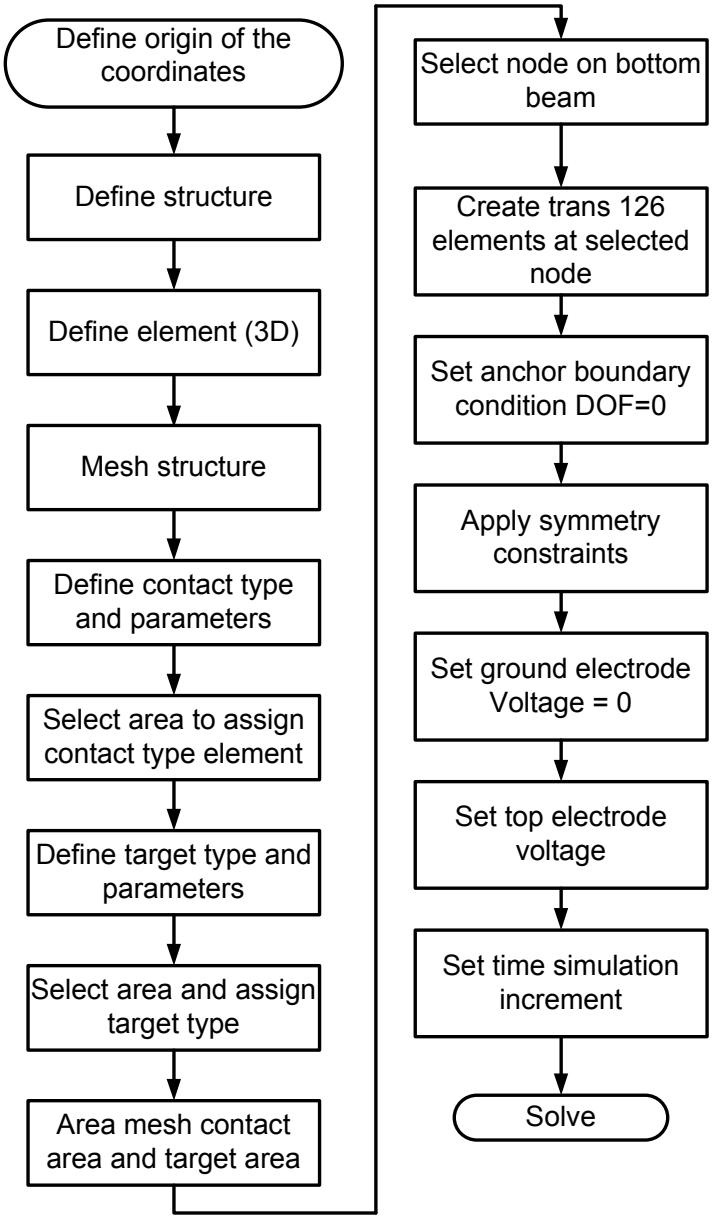

Figure 0-1: ANSYS design and analysis flow

For the device pull-down voltage estimation, the following equation is used.

$$V_p = \sqrt{(8kg_0^3)/(27\varepsilon_0 W_w)} \tag{0.1}$$

where k is the effective spring constant of a membrane, W is the center conductor width, w is the membrane width, ε_0 is the permittivity of free space, and g_0 is the nominal gap height. [79]

One MEMS switch has been modeled using ANSYS. The pull-in voltage is simulated to meet the low voltage requirement. Figure 0-2 shows the beam. A voltage difference between the supporting beam and the drive electrode creates electrostatic forces in the supporting beam.

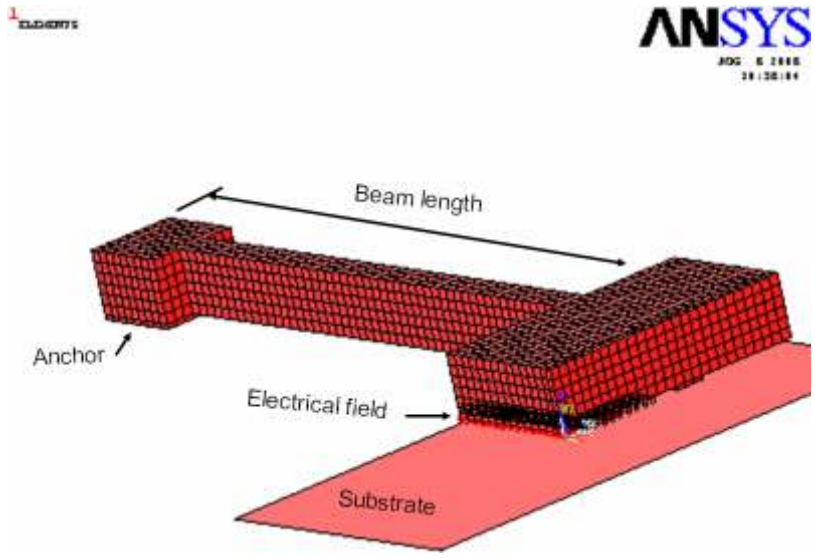

Figure 0-2: MEMS beam model for pull-in voltage simulation

A distributed array of TRANS126 elements are used to model the air between the beams and the drive electrode. TRANS126 is a fully coupled two-nodded, one-dimensional, electromechanical element that relates the electrostatic and structural responses. It has UX (or UY or UZ) and volt DOFs.

TRANS126 elements can be used in the "lumped" sense to represent the overall behavior of a device or in a "distributed" sense to represent an electrode. In this simulation, distributed arrays of TRANS126 elements were used.

Model

1. The resonator beam, supporting beams, dimples, and anchors were modeled using SOLID45 elements.
2. Surface-to-surface contact elements were used to recognize contact between the dimple and the ground plane.

Boundary Conditions

1. The bottoms of the anchors were restrained in all directions (UX, UY, and UZ).
2. A voltage difference was placed across the TRANS126 elements. The top nodes of the TRANS126 elements were set to zero voltage (ground), and the input voltage was applied to the bottom nodes. Figure 0-3 shows the pull-in voltage simulation result. At 50 V, the switch is pulled to its ON position.

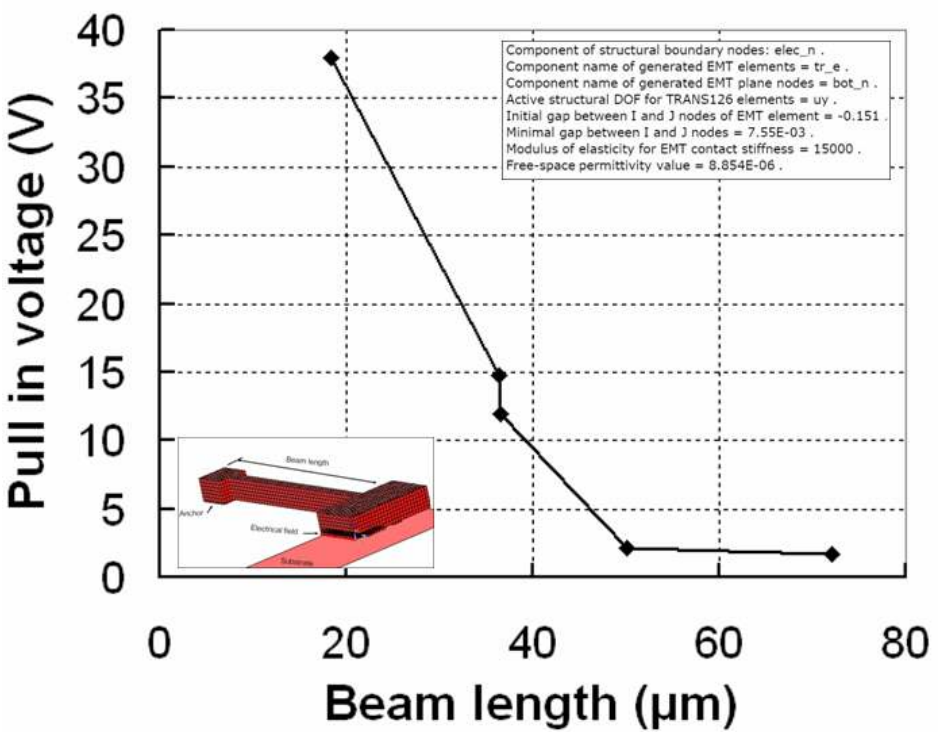

Figure 0-3: Pull-in voltage vs. supporting beam length (insert shows the supporting beam structure and environment parameters)

Beam parameters are listed in Table 0-1.

Table 0-1: Parameters of pull-in voltage simulation

Parameter	Value (μm)	Explanation
lr	17.8	Resonator beam length
wr	10	Resonator beam width
ls	50.4	Supporting beam length
ws	1	Supporting beam width
ht	2.05	Resonator beam thickness
we	4.5	Drive electrode width
ln	4.0	Node location (distance from end of resonator to center of supporting beam)

Table 0-1: Parameters of pull-in voltage simulation

Parameter	Value (μm)	Explanation
di	0.151	Adjusted initial gap height
dh	0.123	Dimple height

Figure 0-4 shows the pull-in simulation result of the supporting beam length of 36.4 μm. At a voltage of 14.8 V, the beam dimple presses the substrate.

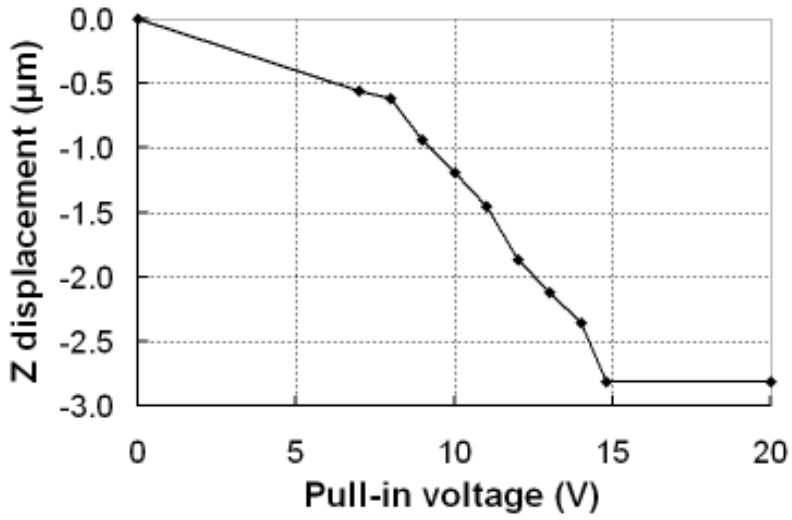

Figure 0-4: Pull-in voltage simulation when support beam length is 36.4 μm, and pull-in voltage is 14.8 V

In summary, this work opens a door to a broad research area which can go in many directions. I hope this research can lead the way to make MEMS part of the CMOS RF circuit design.