

# 0.5um Analog CMOS 2P3M 5V Design Tutorial

**Version 1.0**

Electronics and Telecommunications  
Research Institute

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# 1. Overview

# 1. Overview

## 1.1 Overview

The purpose of this paper is 0.5um Analog CMOS 2P3M 5V Design tutorial.

## 1.2 Tools and Software Version

- Virtuoso 6.1.7 version
- Calibre 2019.4\_36.18

## 1.3 File Configuration

File : ETRI\_0p5um\_Analog\_CMOS\_2P3M\_5V\_NSPL\_V1p0.tar.gz

- ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_V1p0	
- ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_V1p0.tf	: tech file
- display.drf	: display file
- DRC	
- ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_V1.0_DRC.cal	: DRC rule file
- drc_header.cal	: with script file
- LVL	
- ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_V1.0_LVL.cal	: LVL rule file
- lvl_header.cal	: with script file
- LVS	
- ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_V1.0_LVS.cal	: LVS rule file
- lvs_header.cal	: with script file
- PEX	
- ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_V1.0_PEX.cal	: PEX rule file
- pex_header.cal	: with script file
- ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_V1p0_pcell	: Pcell library
- ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_V1p0_sch	: sch library
- ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_V1p0_std_lay	: std lay library
- ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_V1p0_std_sch	: std sch library

## 1.4 Documents

- 0.5um Analog CMOS 2P3M 5V Design Rule V1.0	: Design rule
- 0.5um Analog CMOS 2P3M 5V Design Guide V1.0	: Design Guide
- 0.5um Analog CMOS 2P3M 5V Design Guide V1.0	: Design Tutorial

## 1.5 Document history

Rev	Date	From	Description
1.0	2023.09.15	ETRI	<p><b>Added Items</b></p> <ul style="list-style-type: none"><li>1. Overview</li><li>2. PDK Library 설정</li><li>3. 회로 설계 및 검증</li><li>4. Layout</li><li>5. DRC</li><li>6. LVS</li><li>7. PEX</li></ul>
Title			<b>ETRI 0.5µm Analog CMOS 2P3M 5V Design Tutorial</b>
Division			<b>ETRI</b>

## 2. PKD Library 설정

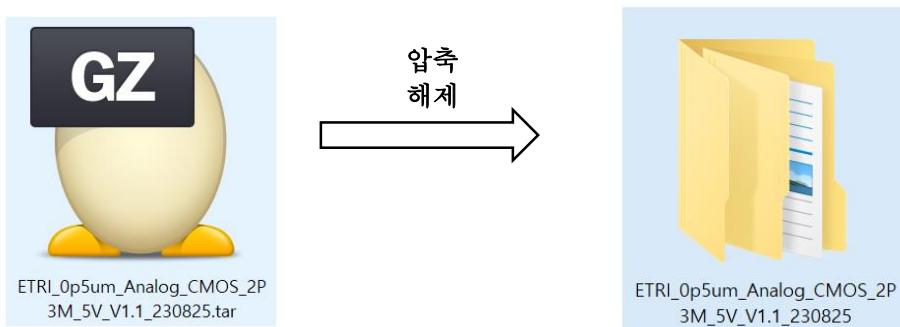
## 2. PDK Library 설정

- 목적 : 회로 설계 및 검증에 앞서 제공받은 PDK를 설정

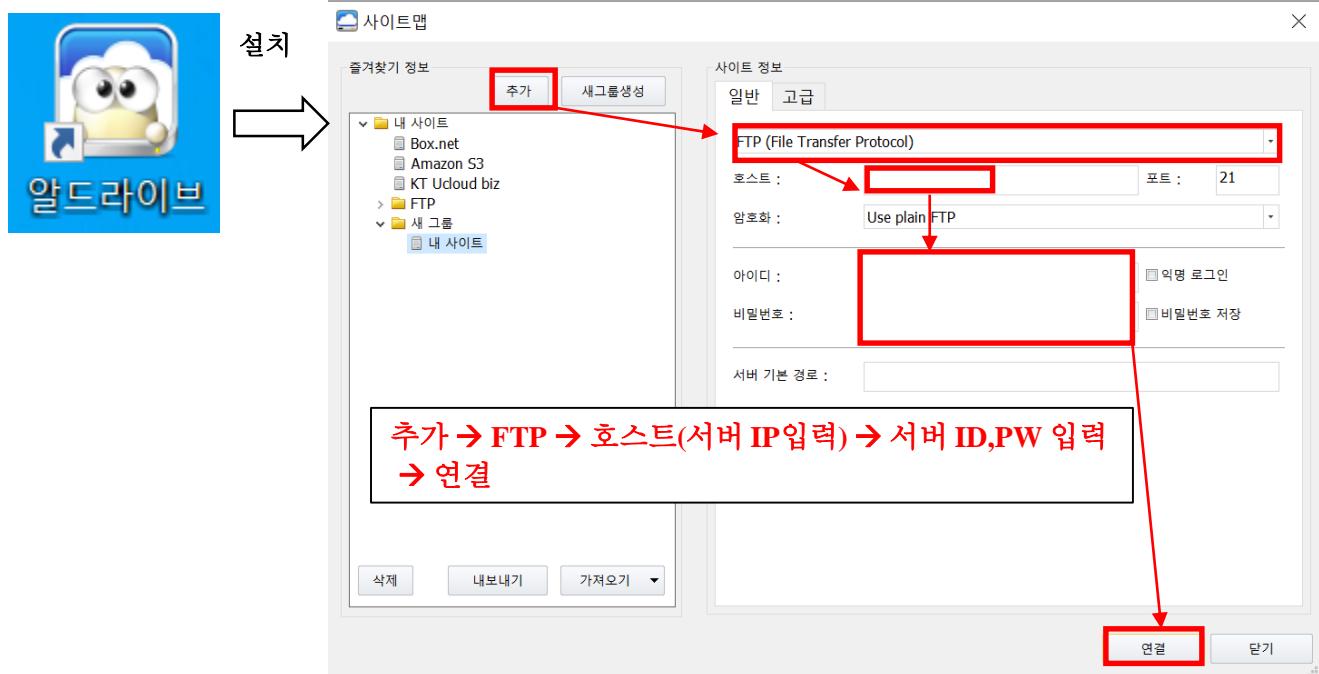
### 1) PDK Library 전송 (서버 기반의 워크스테이션 접속일 경우)

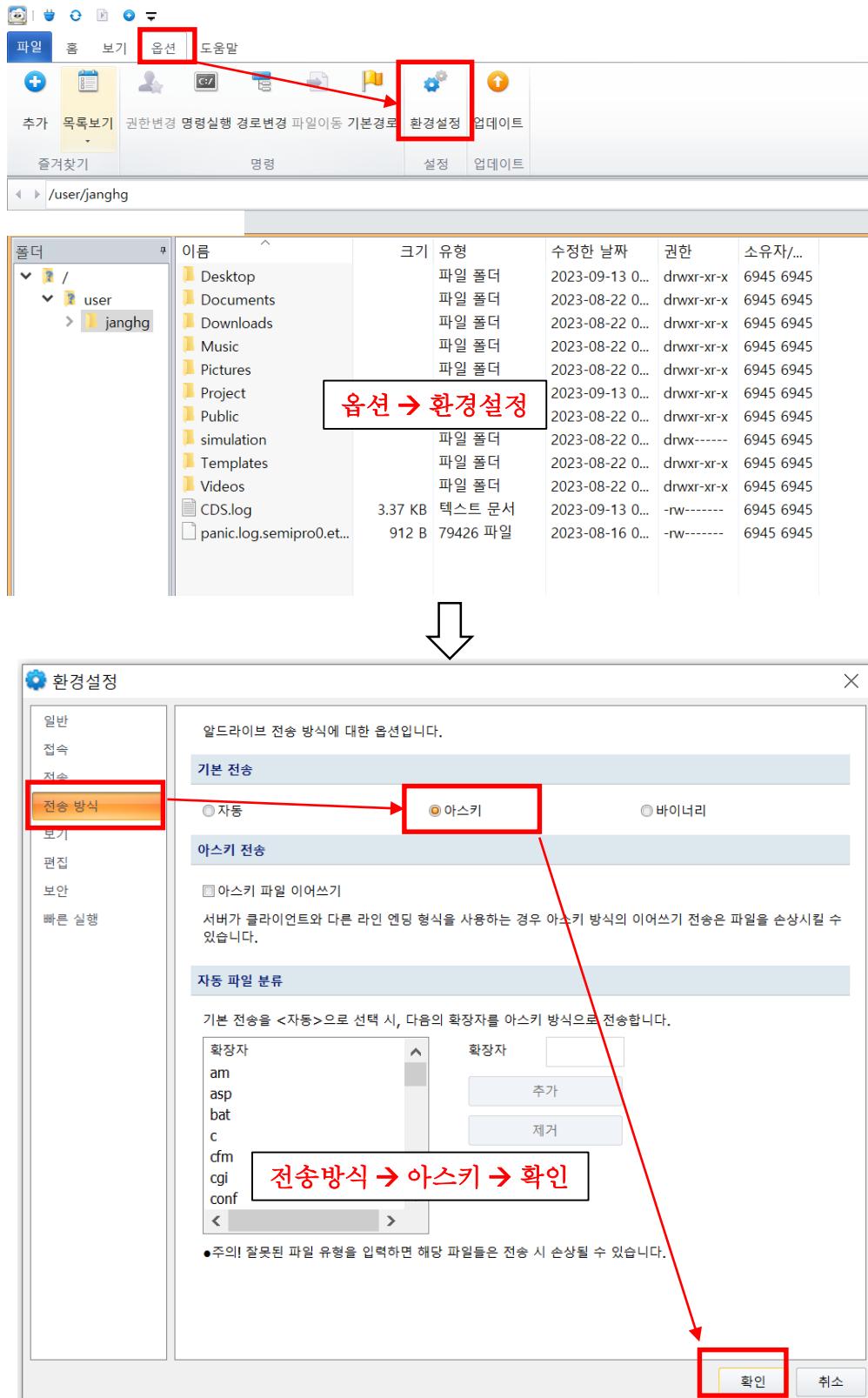
- 제공된 PDK를 FTP(File Transfer Protocol)을 이용하여 워크스테이션에 전송

#### ① 제공된 PDK 파일 압축 해제

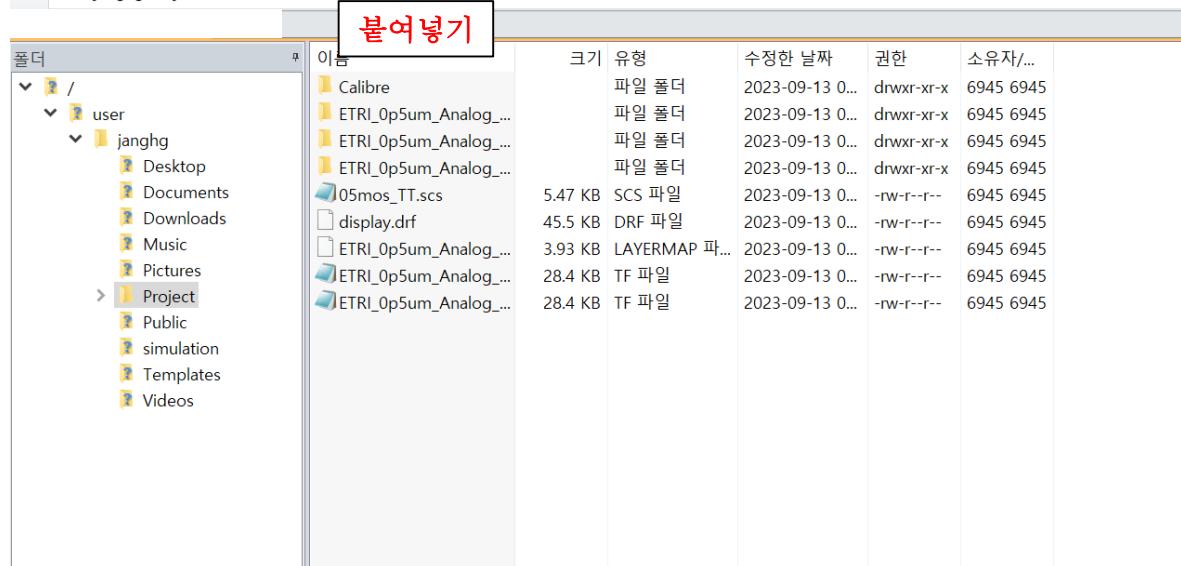
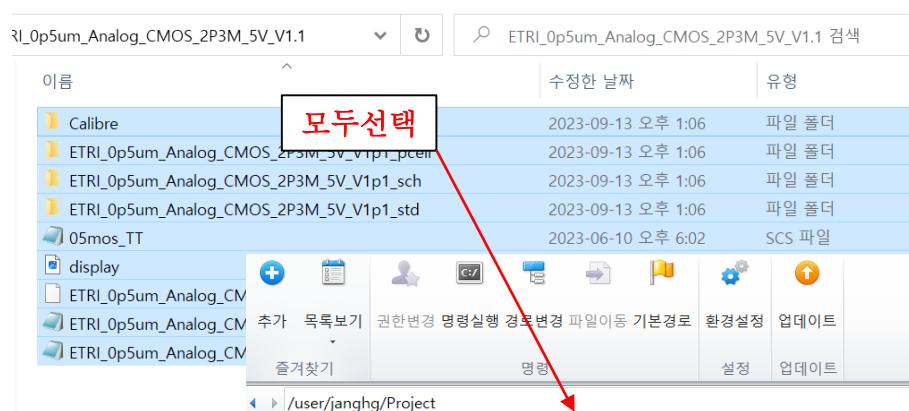
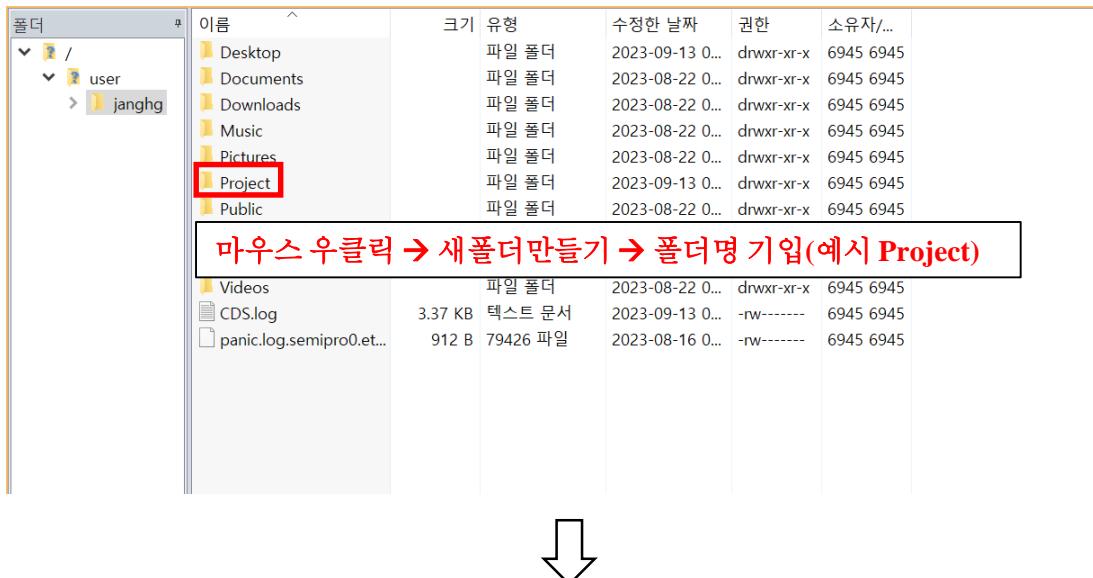


#### ② FTP 프로그램 설치 및 설정 (예시로 알드라이브 사용)

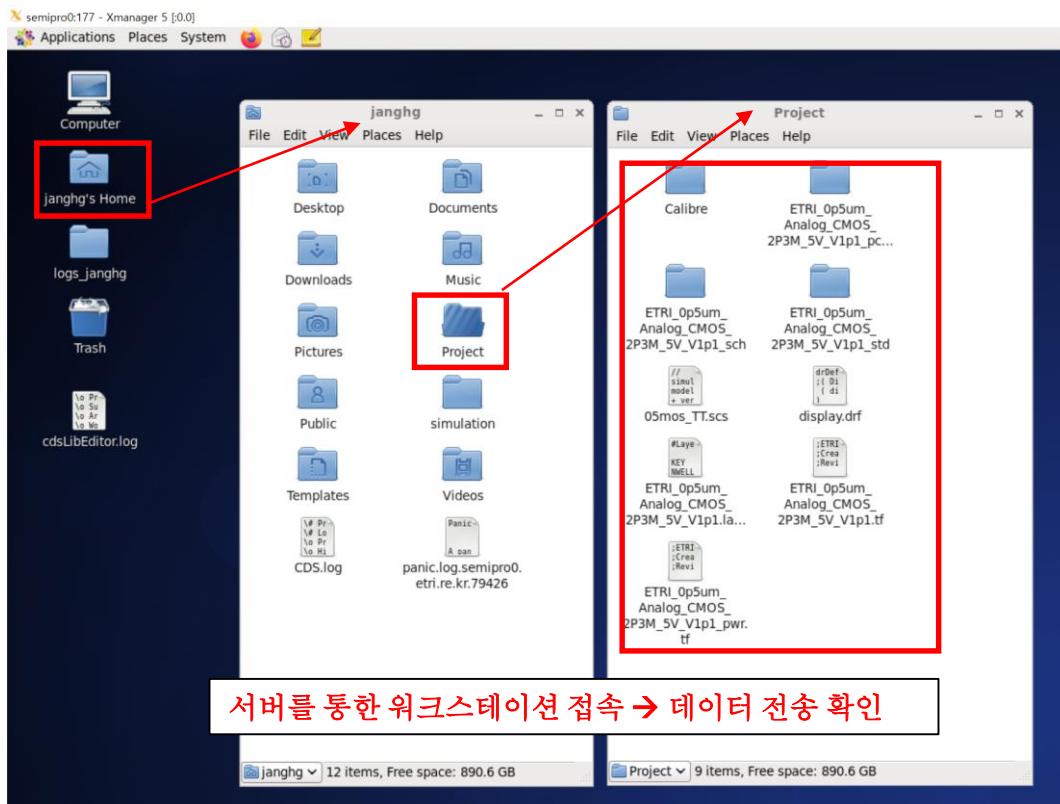




### ③ 폴더 설정 및 파일 전송



#### ④ 전송된 파일 확인

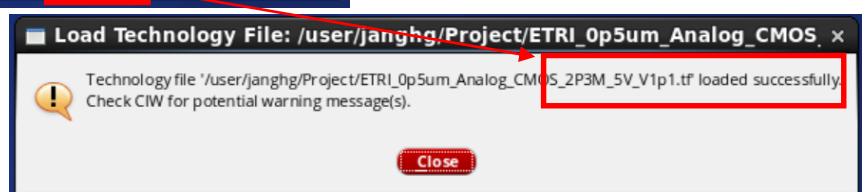
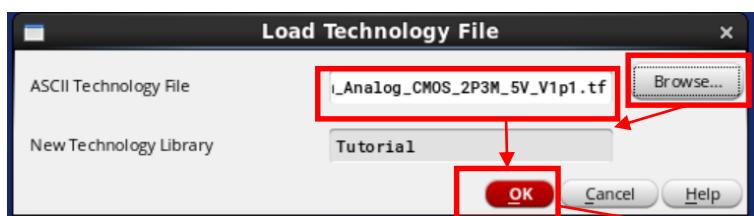
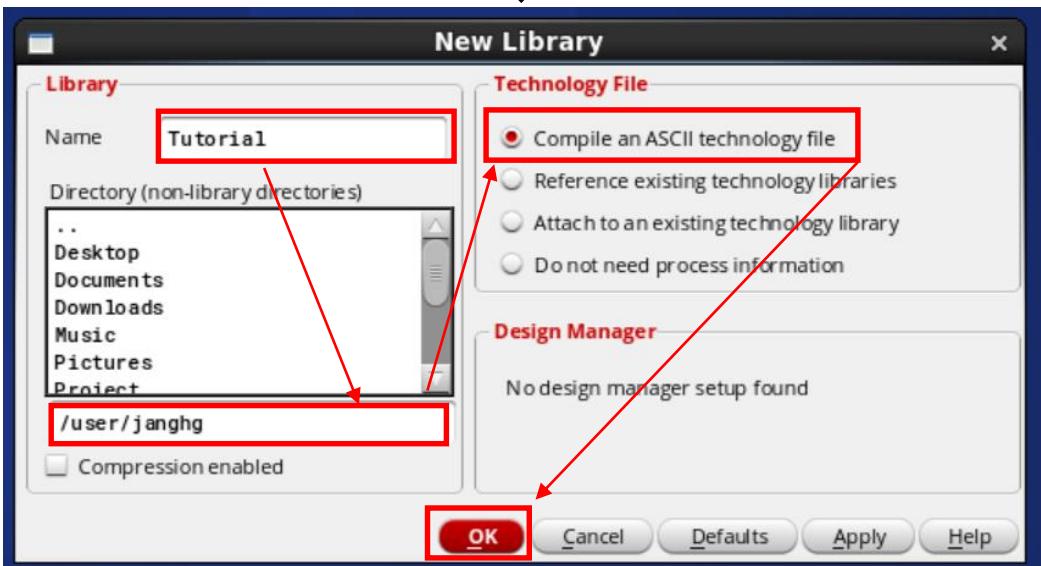
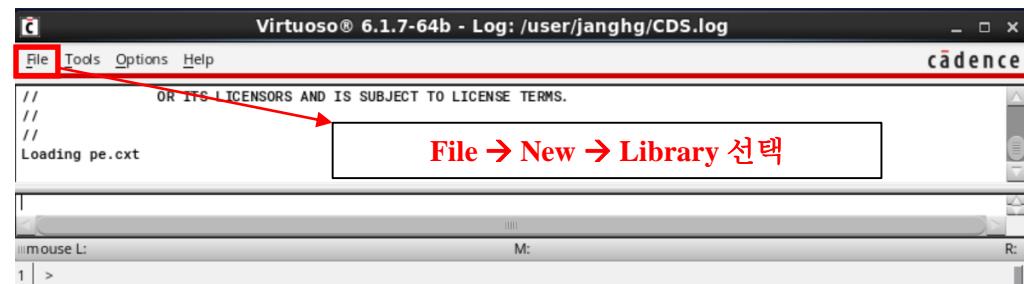


## 2) Library 생성 및 추가

### ① Cadence 실행

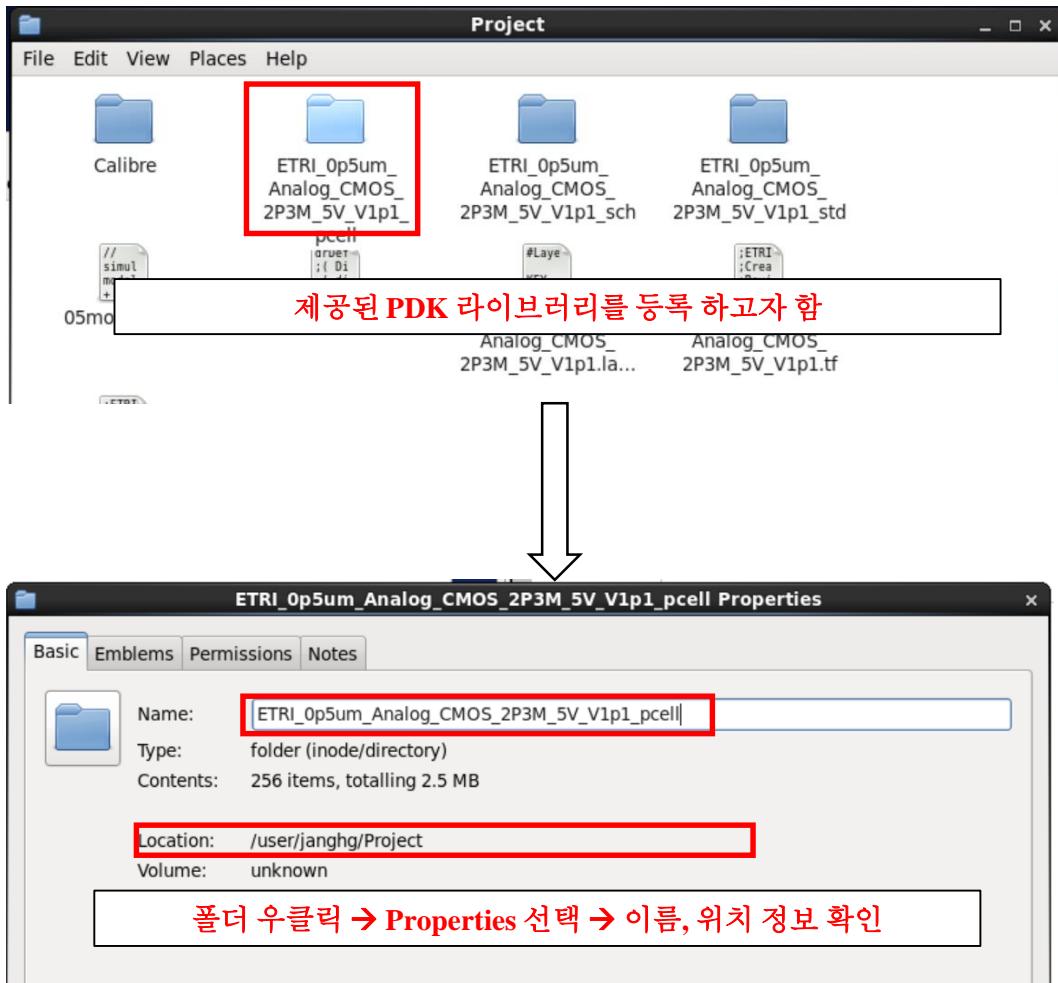


## ② 라이브러리 생성



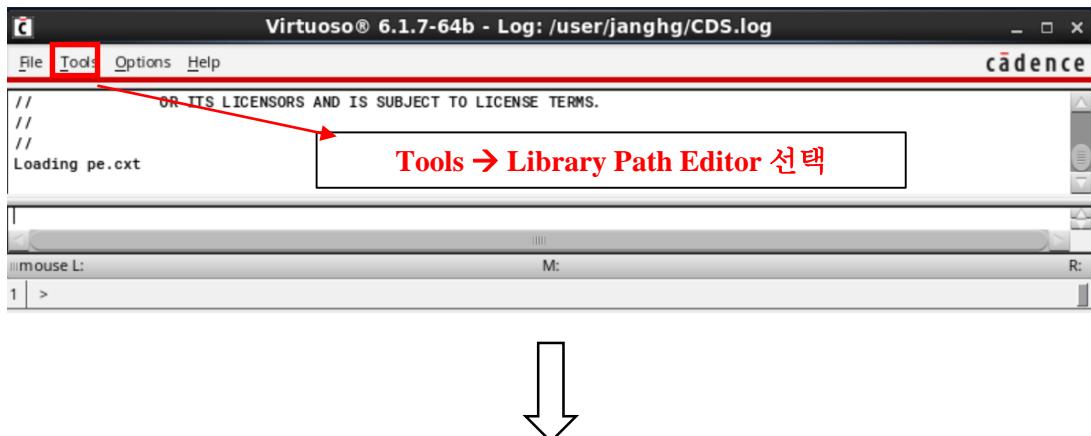
Browse 선택 → Project 폴더에 있는 xxx.tf 파일 선택 → OK  
→ 문제없을 시 성공 메시지 확인 가능

### ③ 제공된 PDK 라이브러리 추가



- 이름 : ETRI\_0p5um\_Analog\_CMOS\_2p3M\_5V\_V1p1\_pcell
- 위치 : /user/jangh/Project

→ 라이브러리 추가에 따른 경로 설정에 필요함  
→ 라이브러리 경로 설정시 위치/이름 삽입 필요! (뒷장 계속)



**Library Path Editor: /user/janghg/Desktop/cds.lib [NameSpace CDBA] (Not Locked)**

Library	Path
1 cdsDefTechLib	/.../tools/dfl/etc/cdsDefTechLib
2 basic	/.../etc/cdllib/basic
3 US_8ths	/.../etc/cdllib/sheets/US_8ths
4 rfLib	/.../samples/artist/rfLib
5 rfExamples	/.../samples/artist/rfExamples
6 abdlib	/.../samples/artist/abdlib
7 Tutorial	/user/janghg/Tutorial
10 ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_V1p0_sch	/user/janghg/Project/ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_V1p0_sch
11 ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_V1p0_std_lay	/user/janghg/Project/ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_V1p0_std_lay
12 ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_V1p0_std_sch	/user/janghg/Project/ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_V1p0_std_sch
13 ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_V1p0_pcell	/user/janghg/Project/ETRI_0p5um_Analog_CMOS_2P3M_5V_NSPL_V1p0_pcell
14	

제공된 라이브러리 (위치 / 폴더명)으로 경로 설정

폴더명 위치/폴더명

Library cdsDefTechLib is defined in include file "dfl/cds.lib".

- 만일, 라이브러리 추가 오류 발생시 빨간색 글씨로 바뀜
- 파란색일 경우 정상적인 등록

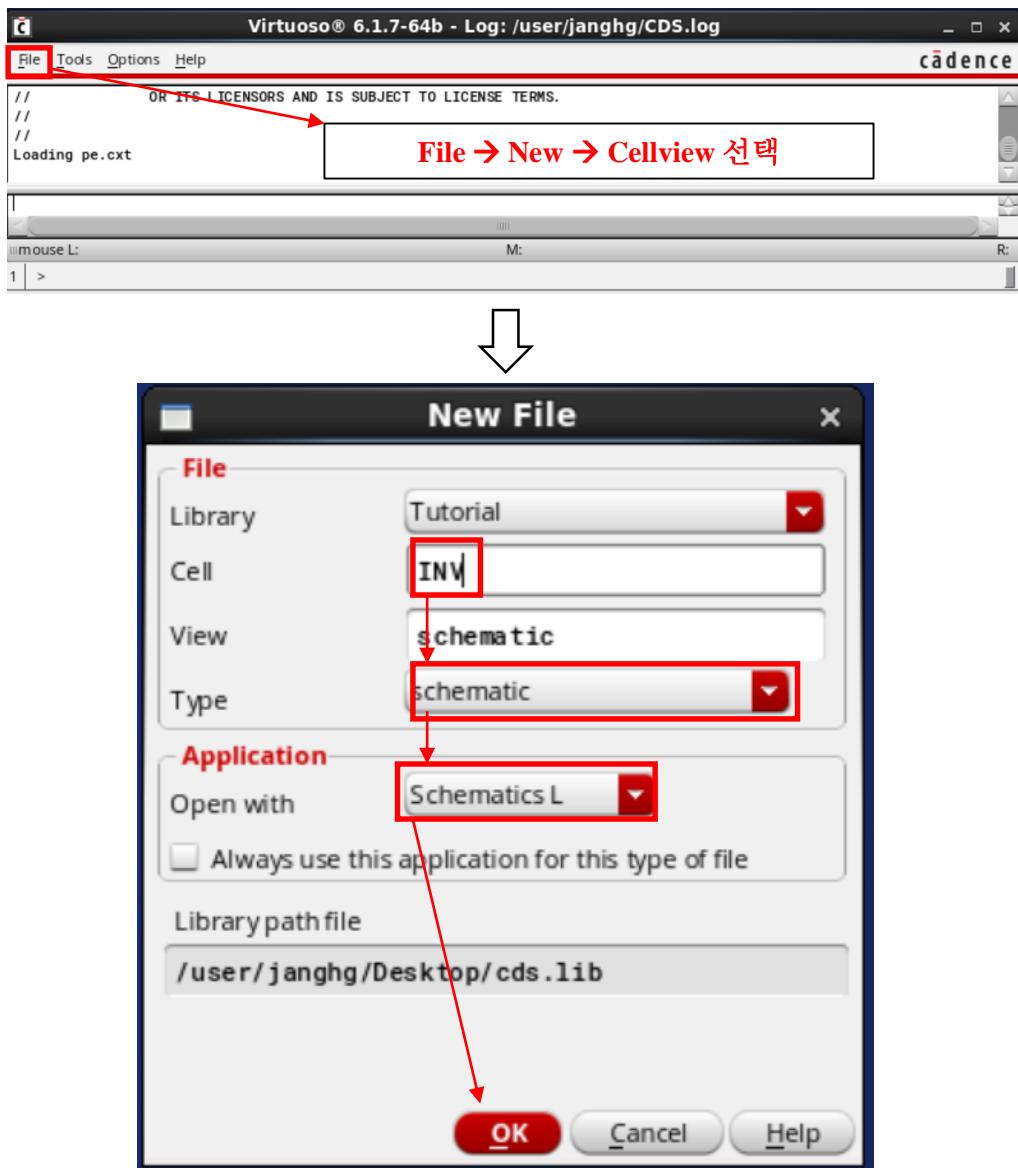
### 3. 회로 설계 및 검증

### 3. 회로 설계 및 검증

- 목적 : 회로 설계 및 시뮬레이션을 통한 회로 검증
- 예: 인버터 회로 설계 및 검증

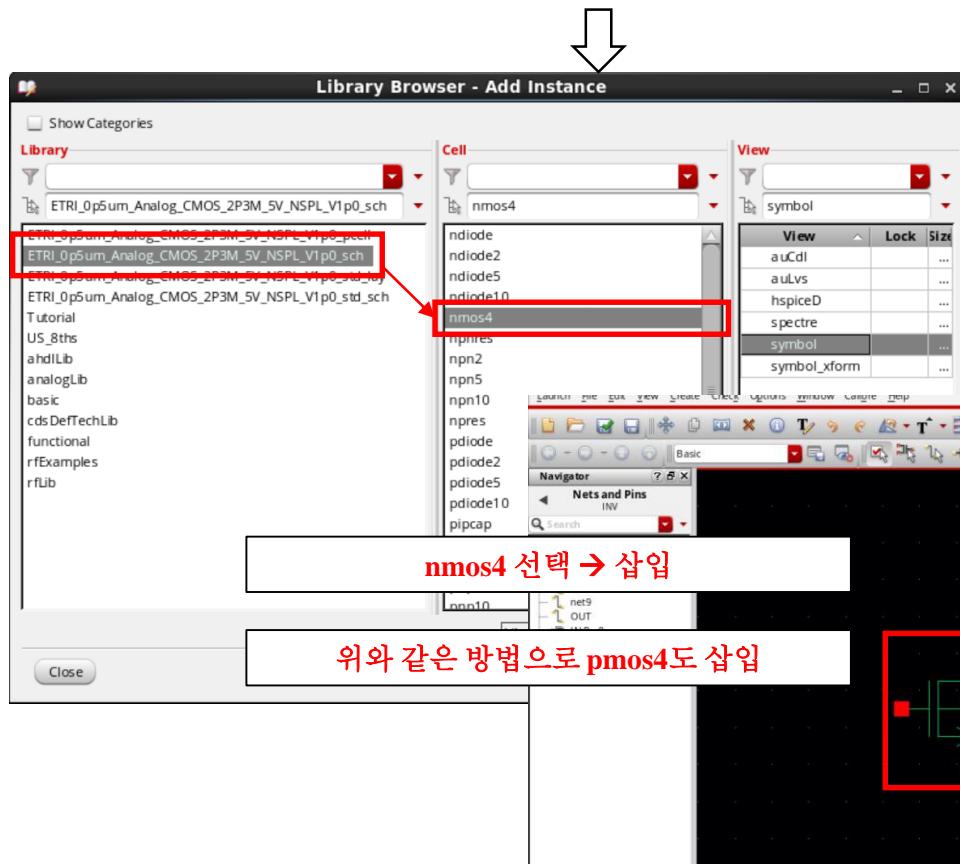
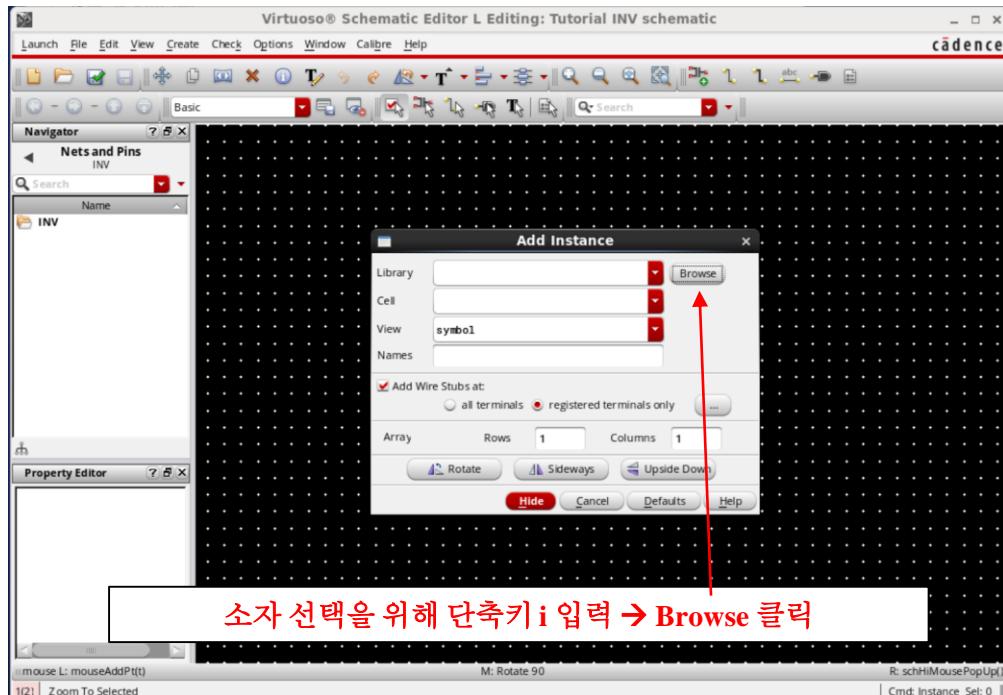
#### 1) 인버터 설계

##### ① Schematic 설계 프로그램 실행

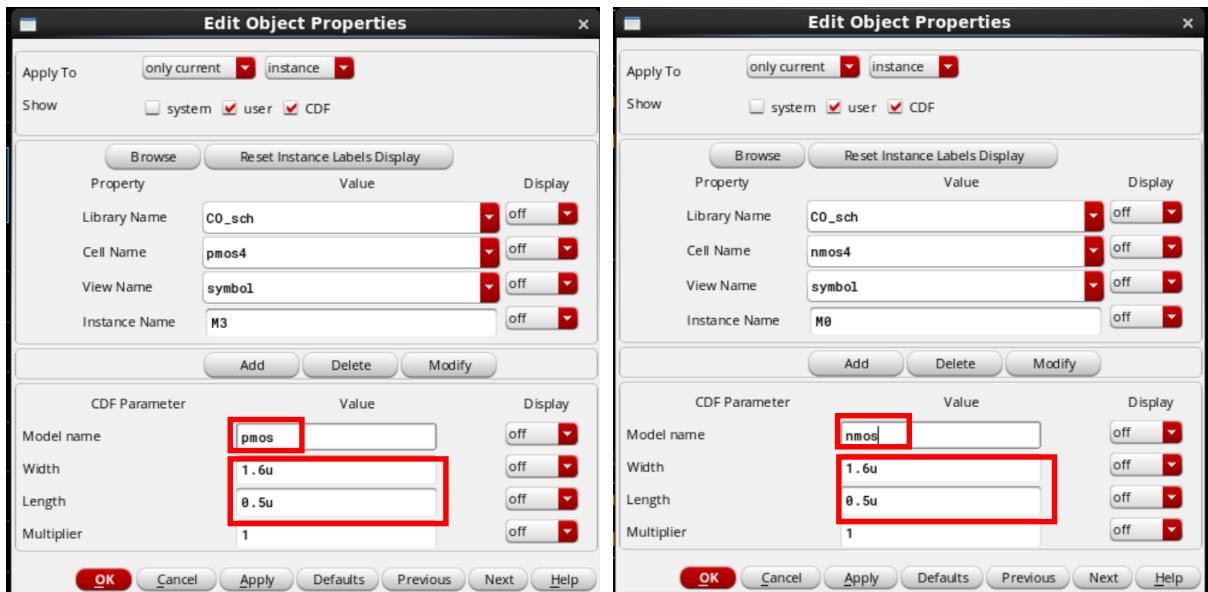


Cell 명 → Type 설정 → 실행 가능한 시뮬레이터 선정 → OK 클릭

## ② 소자 설정

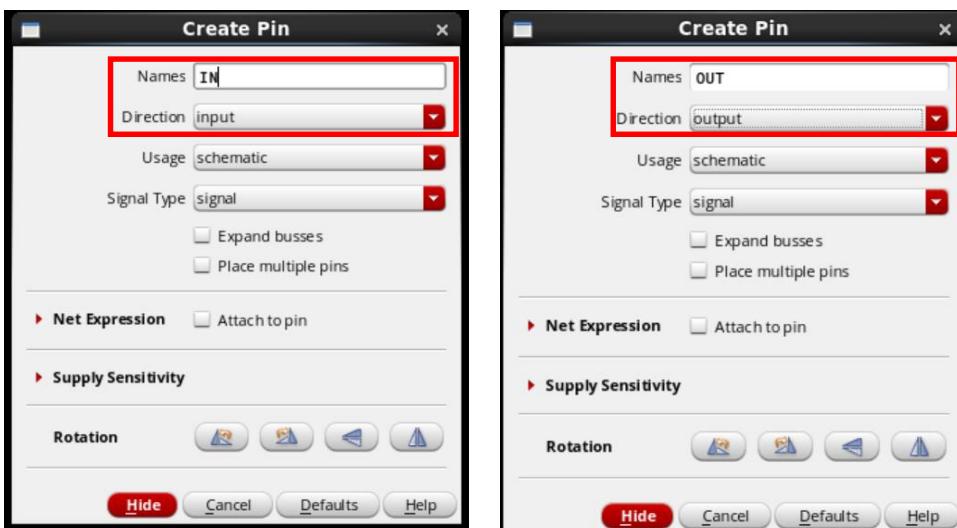


소자별 parameter 입력을 위해 소자 클릭 후 단축키 Q



- Model name은 시뮬레이션을 위해 모델파라미터 이름 입력 (pmos, nmos)
- Width, Length 값 기입

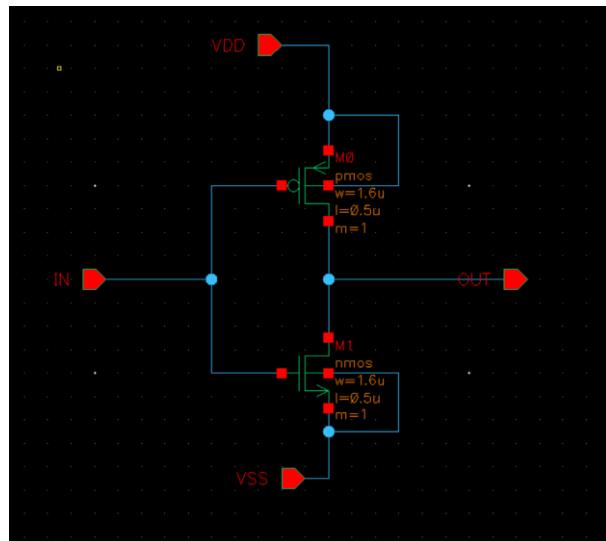
### ③ Pin 설정



포트 설정(단축키 P), 편명과 방향(Input, Output) 설정

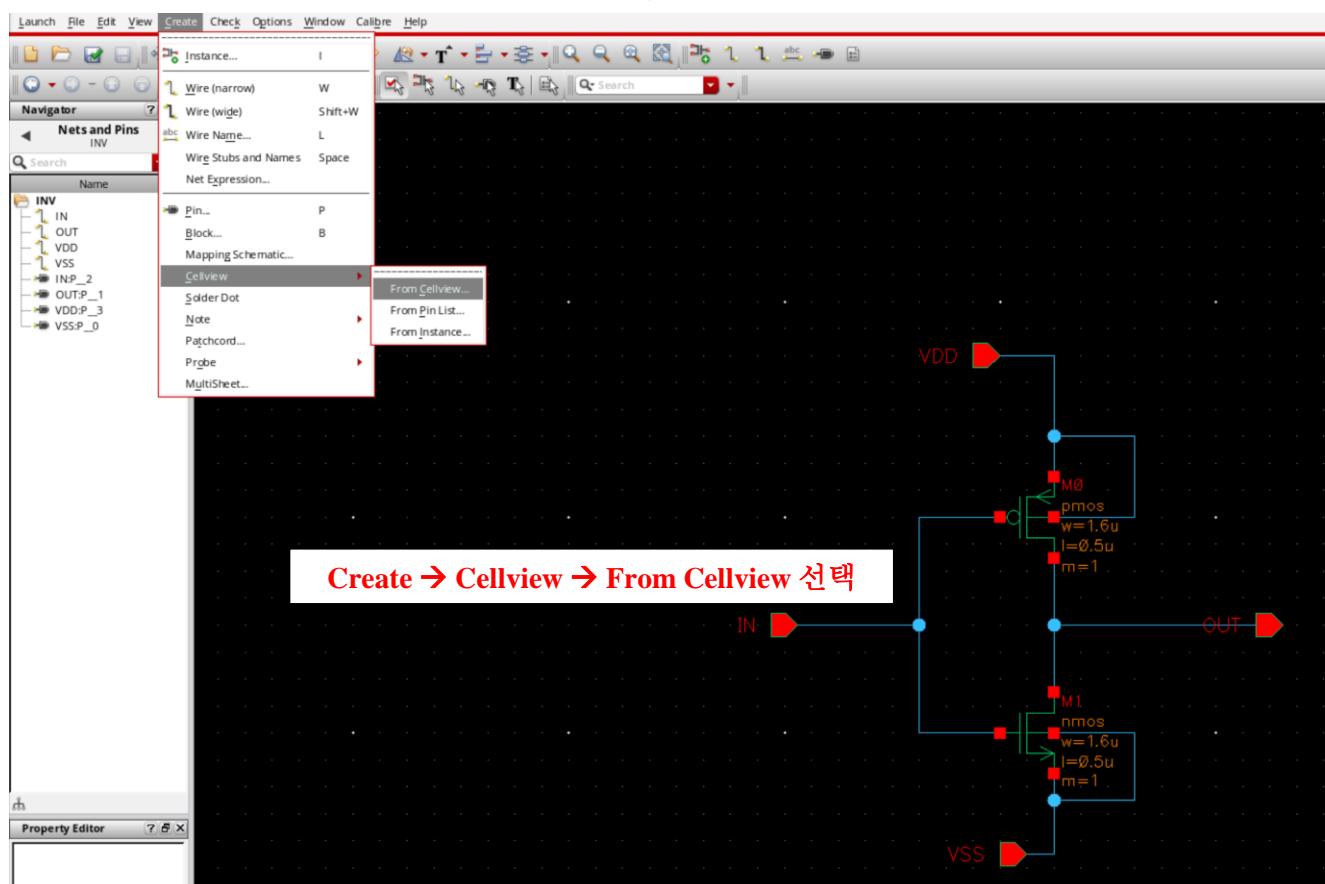
IN, OUT, VDD, VSS 포트 삽입

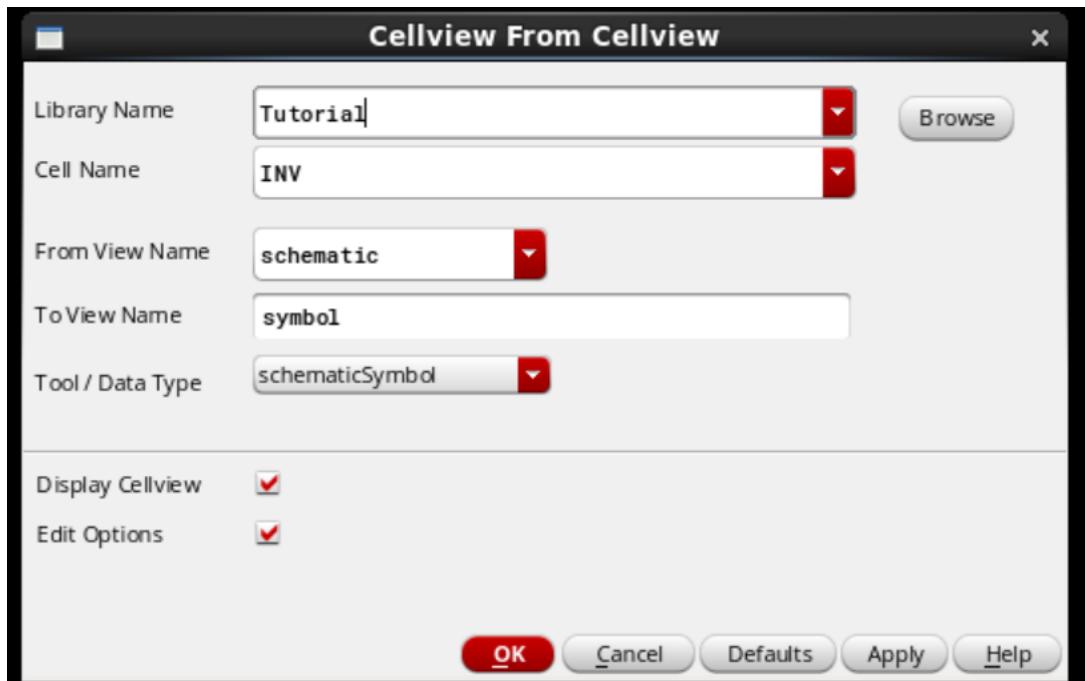
## ④ 와이어 연결



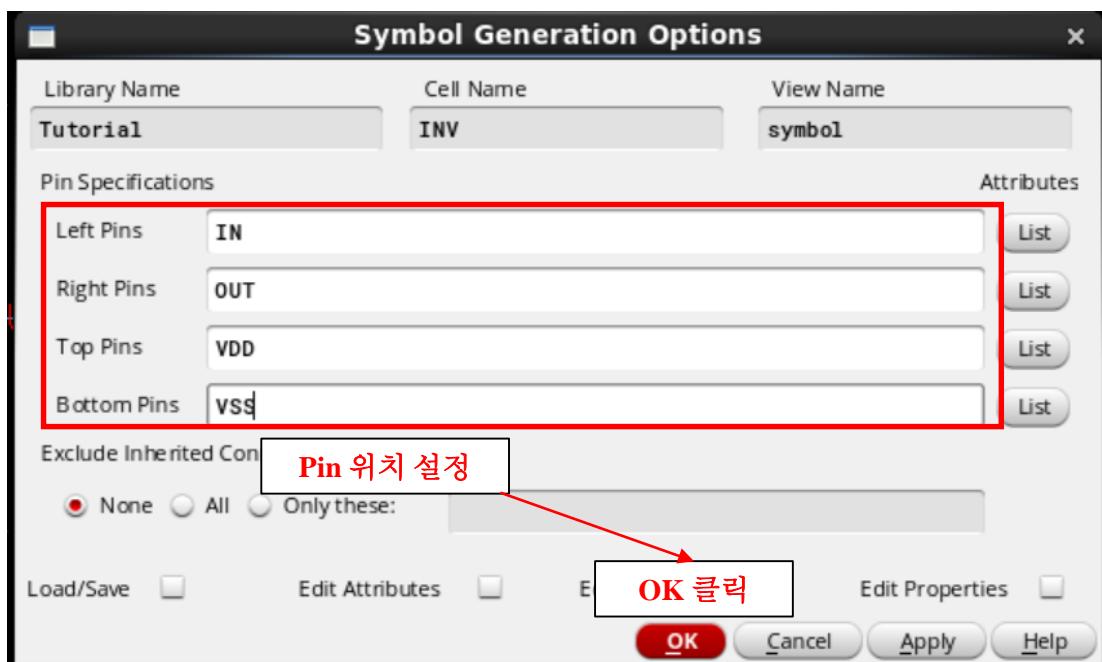
와이어 연결(단축키 w)

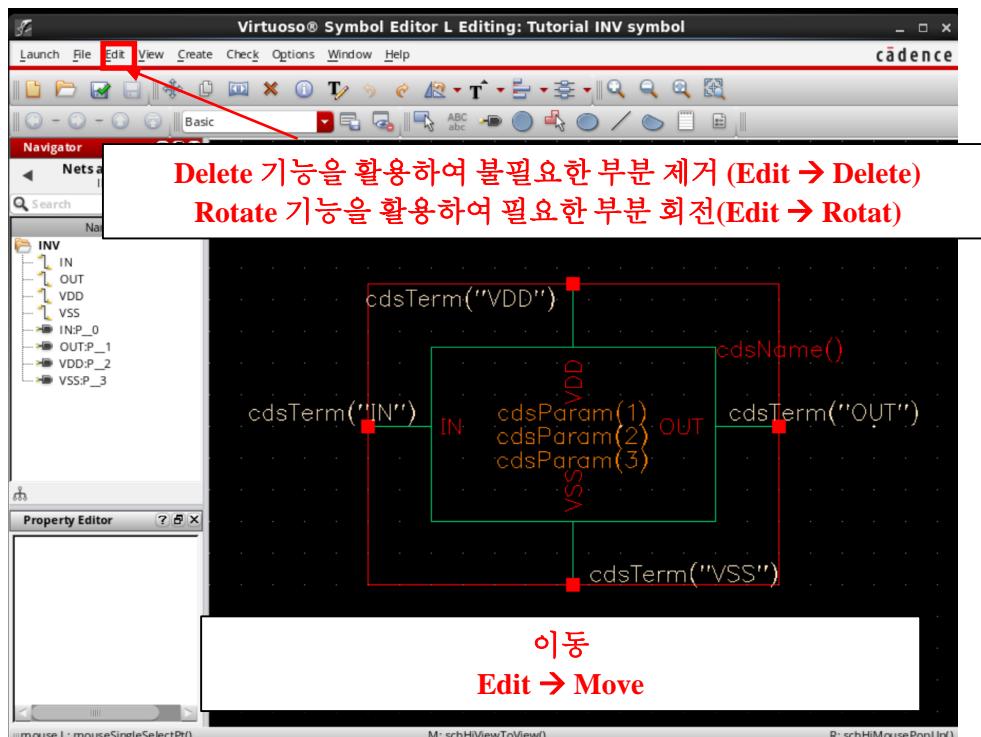
## ⑤ 심볼형성



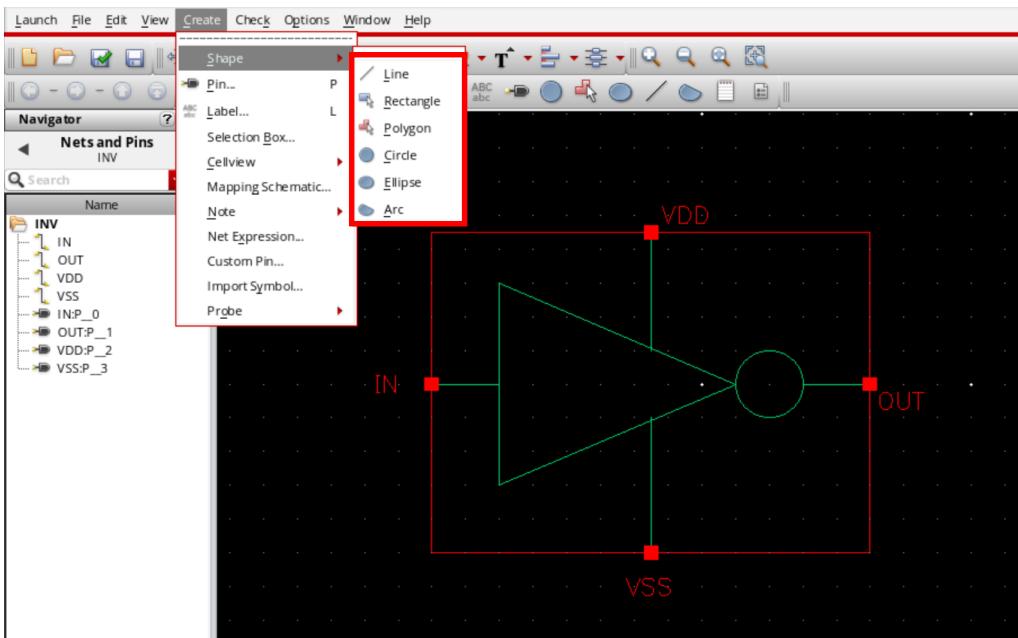


OK 선택





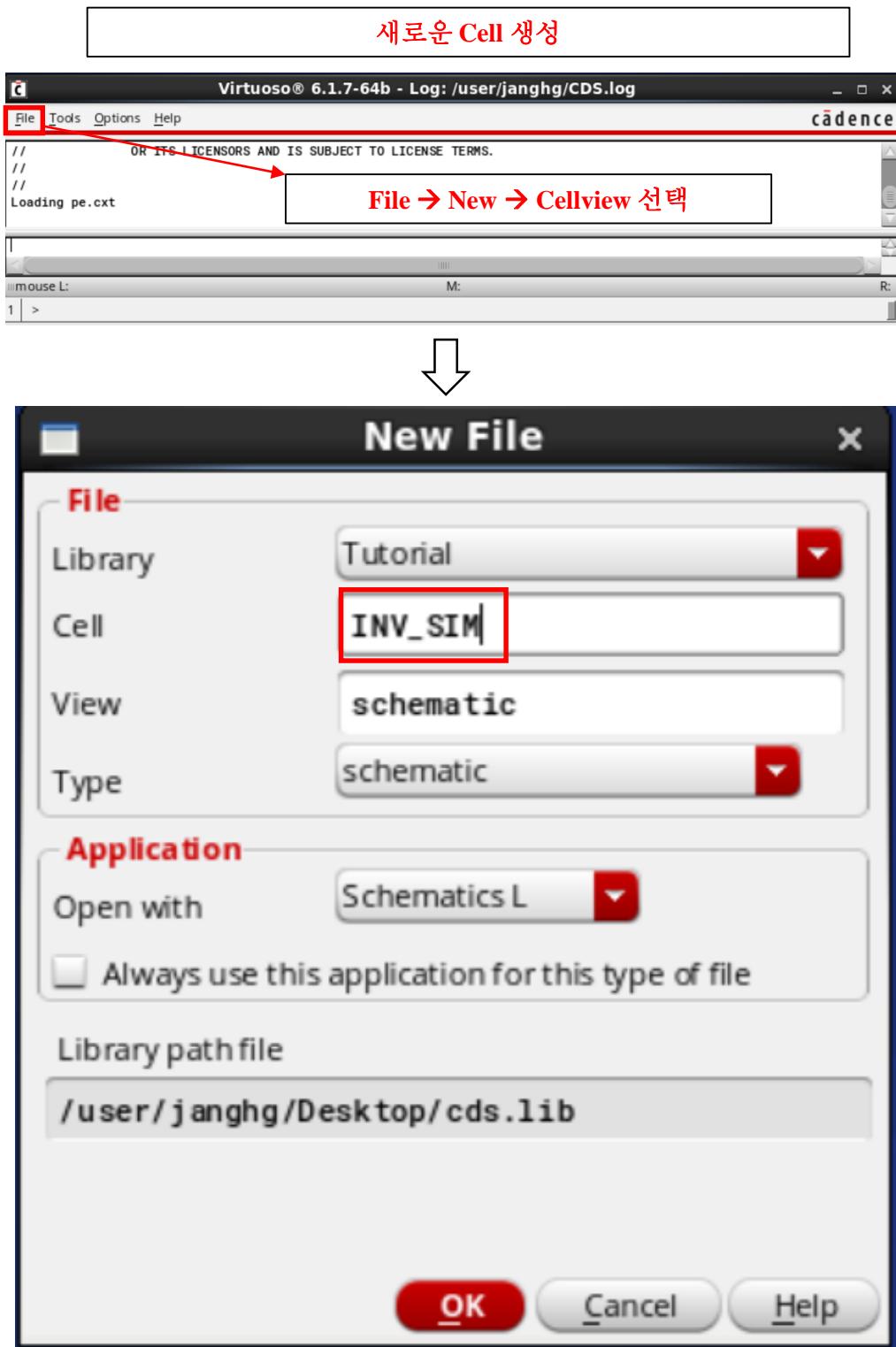
이동  
Edit → Move



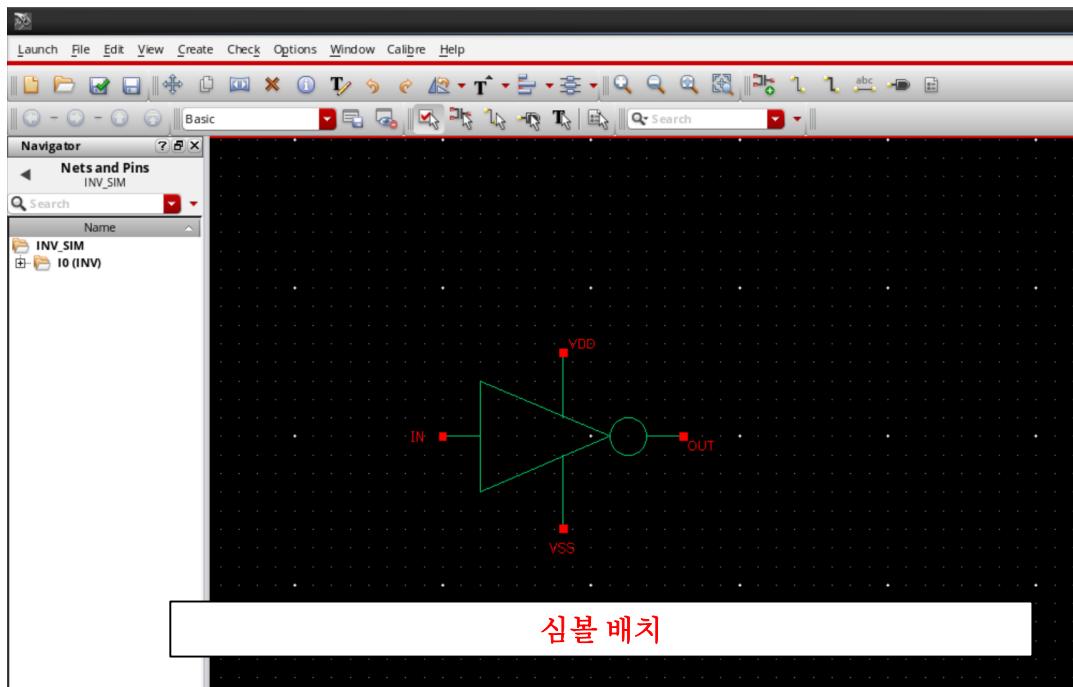
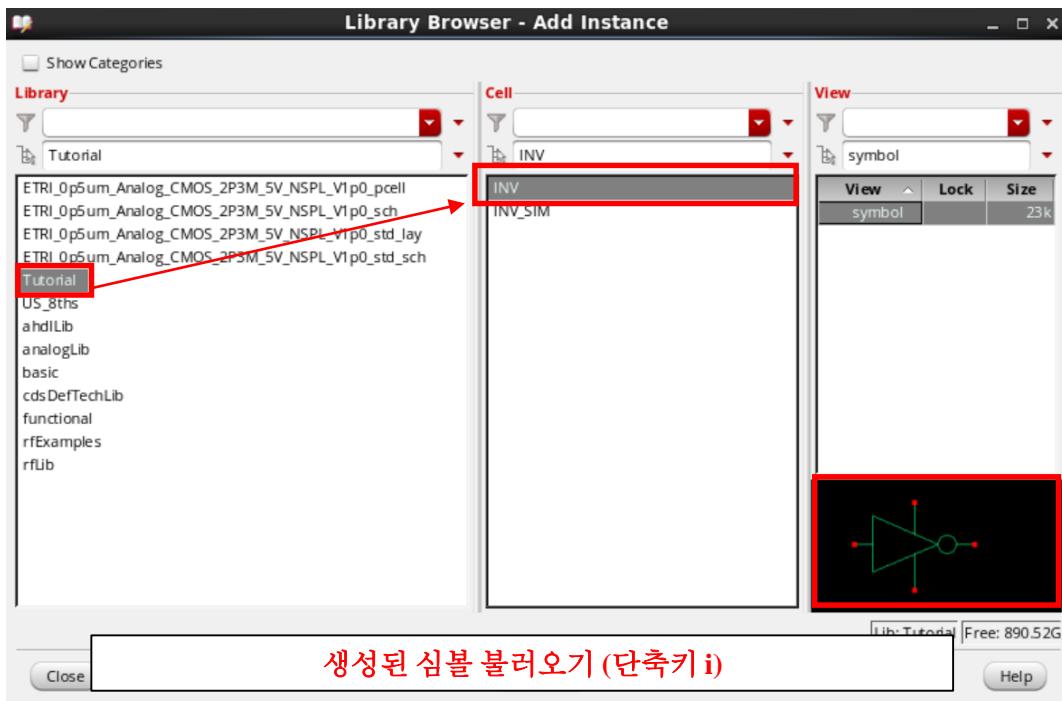
저장

## 2) 시뮬레이션을 위한 회로 설계

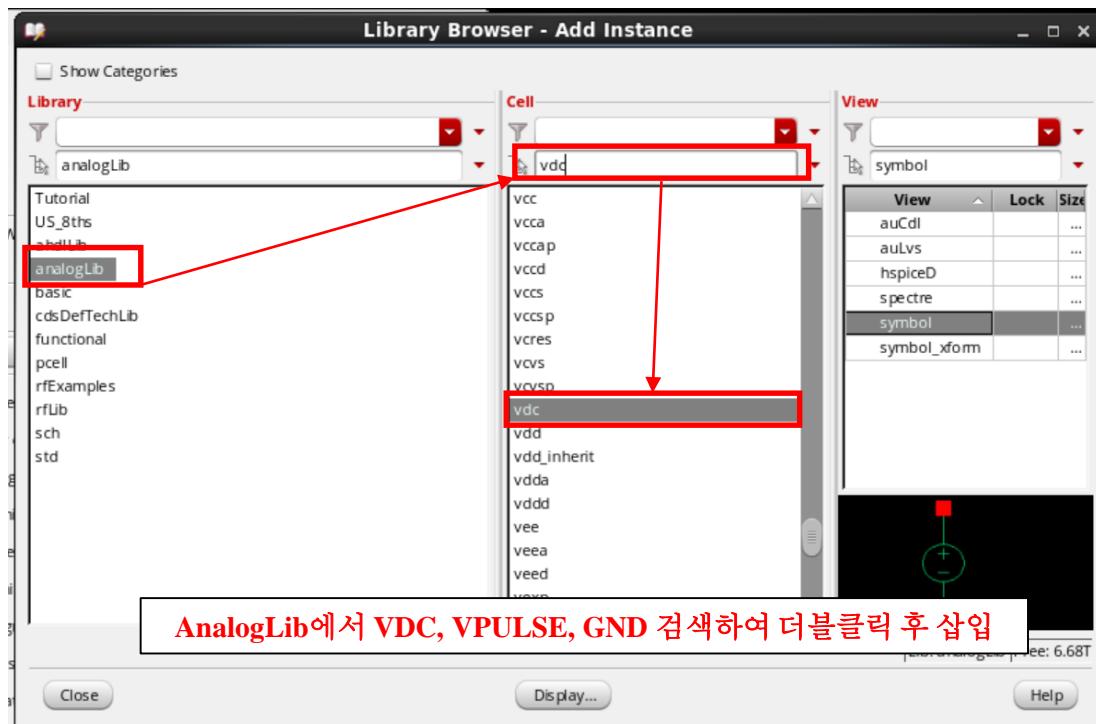
### ① Schematic 설계 프로그램 실행



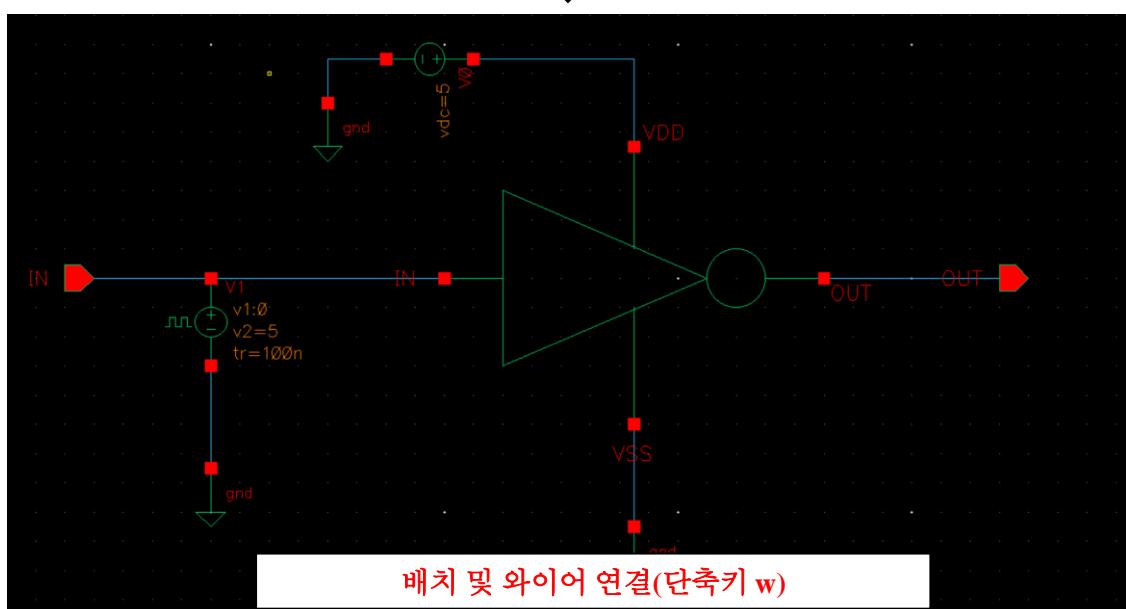
## ② 인버터 심볼 불러오기



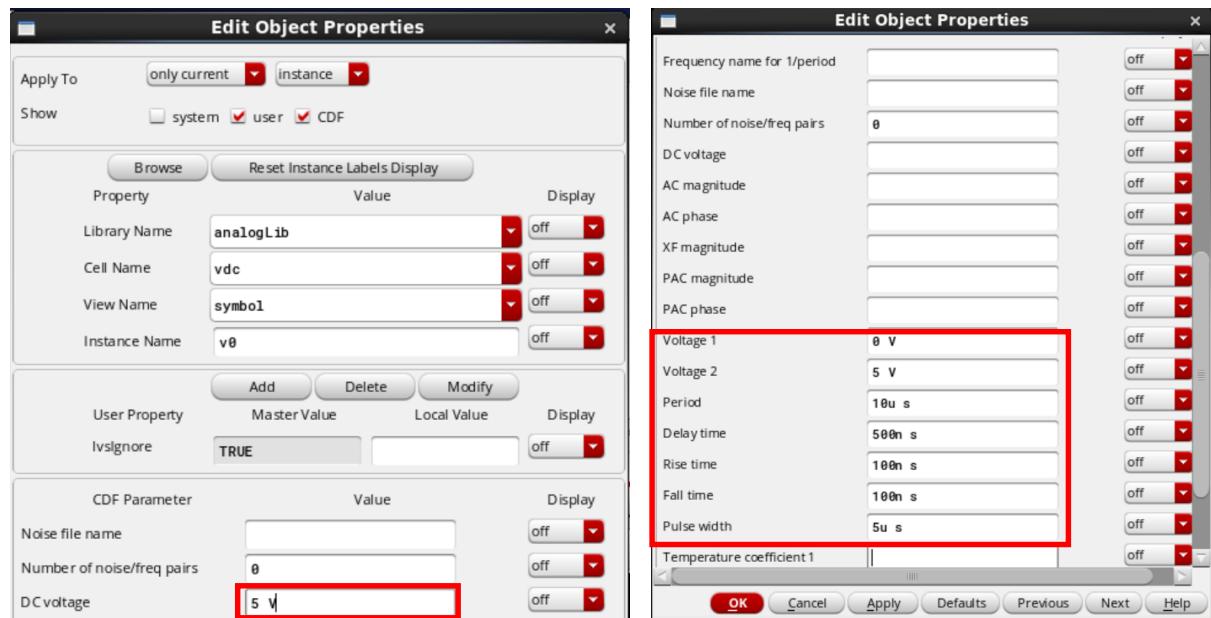
### ③ 소자 배치 및 와이어 연결



IN, OUT 포트 생성 (단축키 P)



## ④ 인가값 설정



시뮬레이션을 위해 VDC 및 VPULSE 값 입력

## ⑤ 저장 및 검증



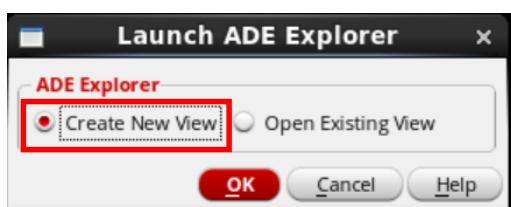
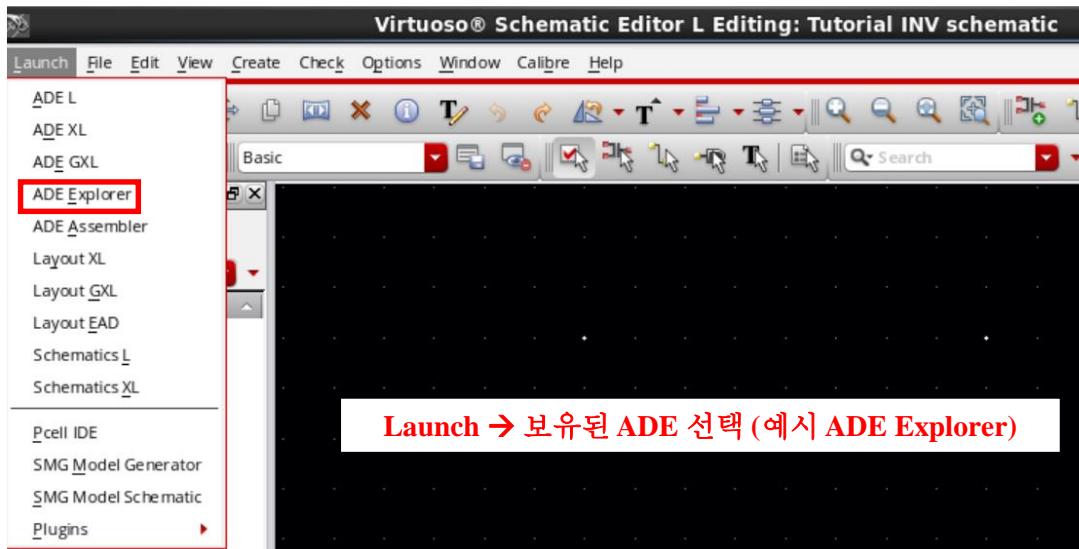
Check & save 버튼 클릭



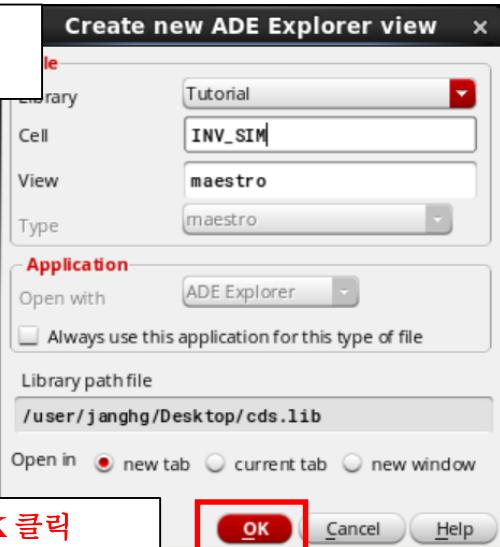
에러 및 경고 메시지 확인, 에러 0까지 수정 및 검증

### 3) 인버터 시뮬레이션

#### ① Schematic 시뮬레이션 프로그램 실행

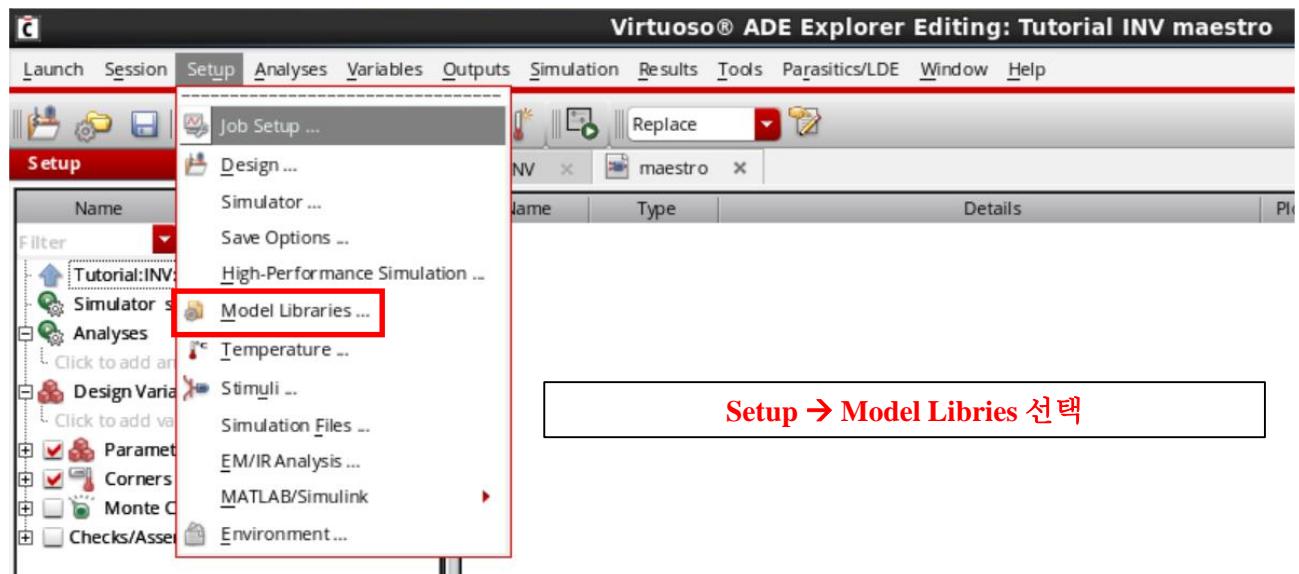


Create New View 선택  
(시뮬레이션 완료 저장 후에는 Open Existing View 선택)

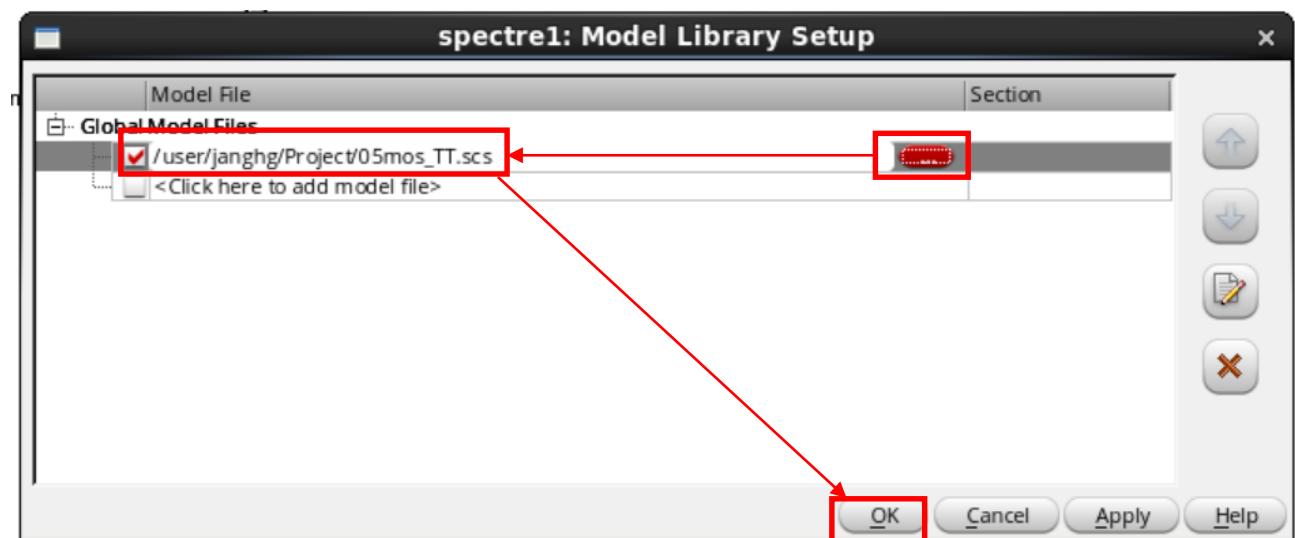
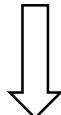


오픈 방식 설정 후 OK 클릭

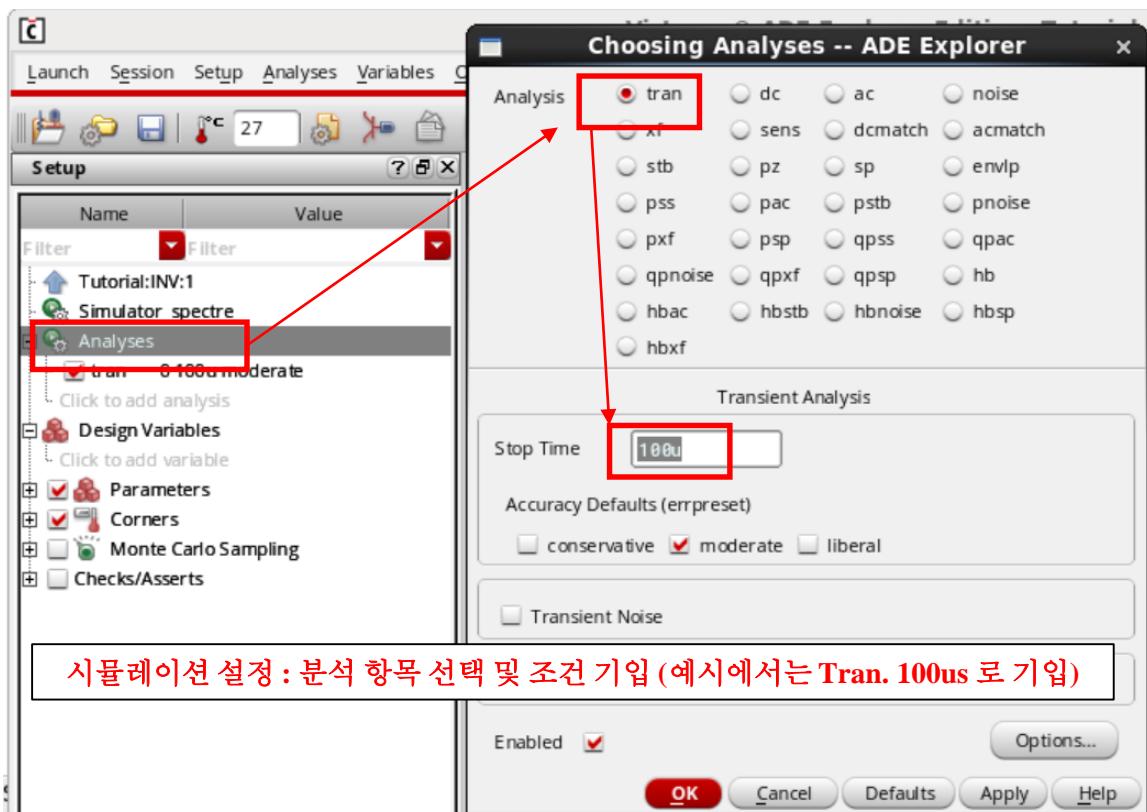
## ② 회로 검증 시뮬레이션 환경 설정



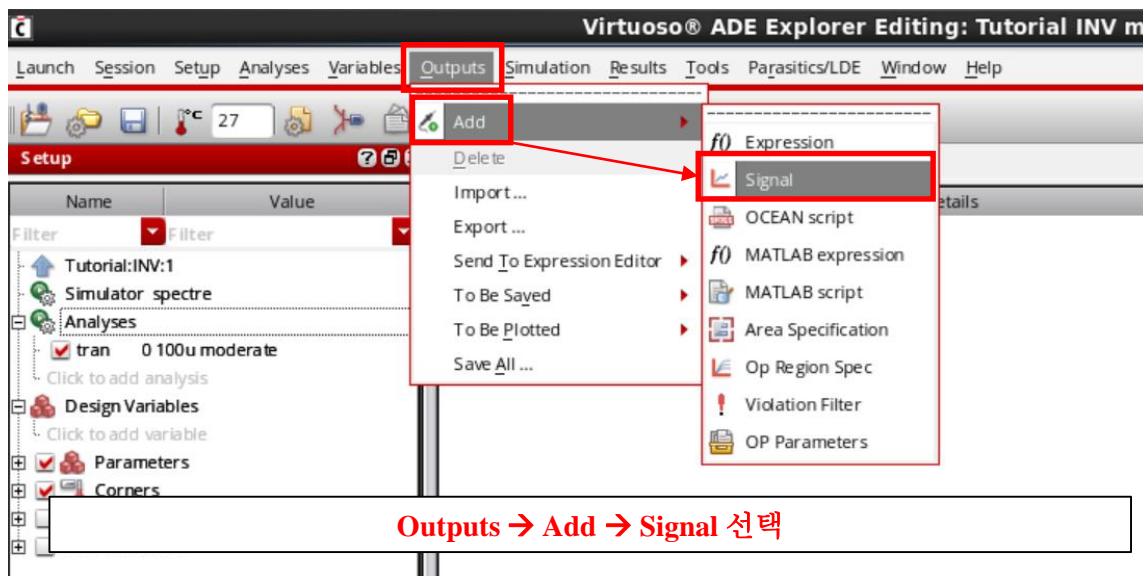
Setup → Model Libraries 선택

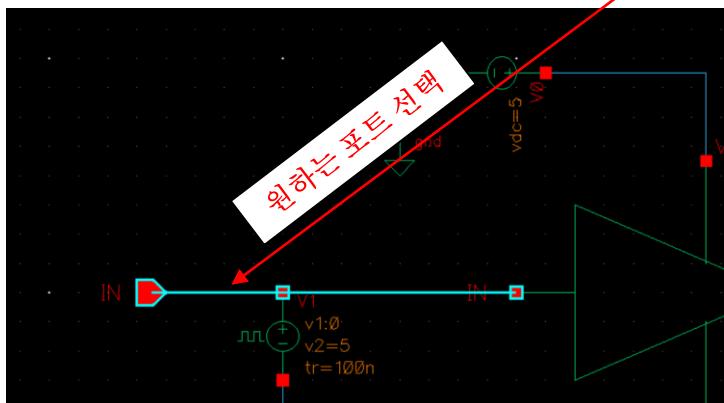
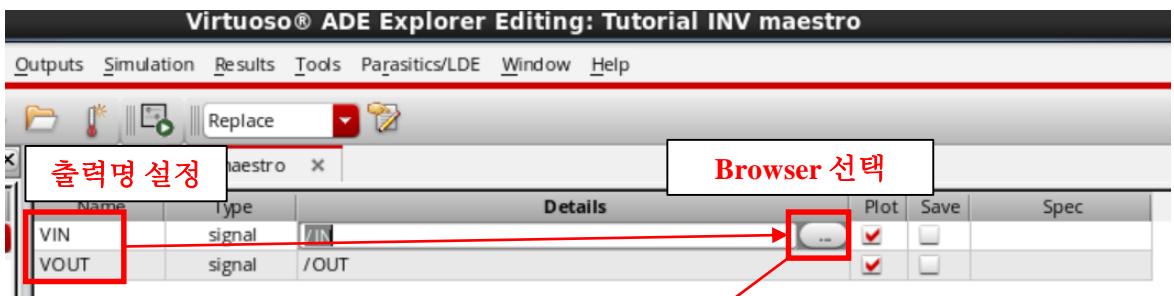


Browse → 제공된 모델파라미터 파일 xxx.scs 선택 → OK



### ③ 시뮬레이션 포트 설정

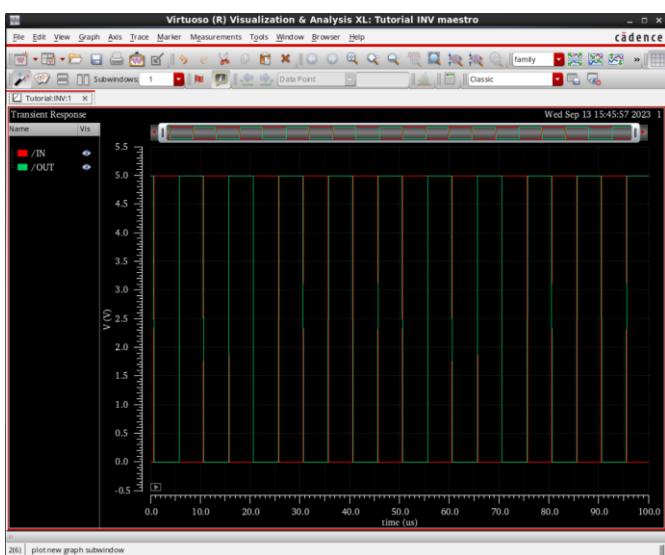
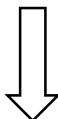




#### ④ 시뮬레이션 실행



저장 및 시뮬레이션 실행



시뮬레이션 결과 출력

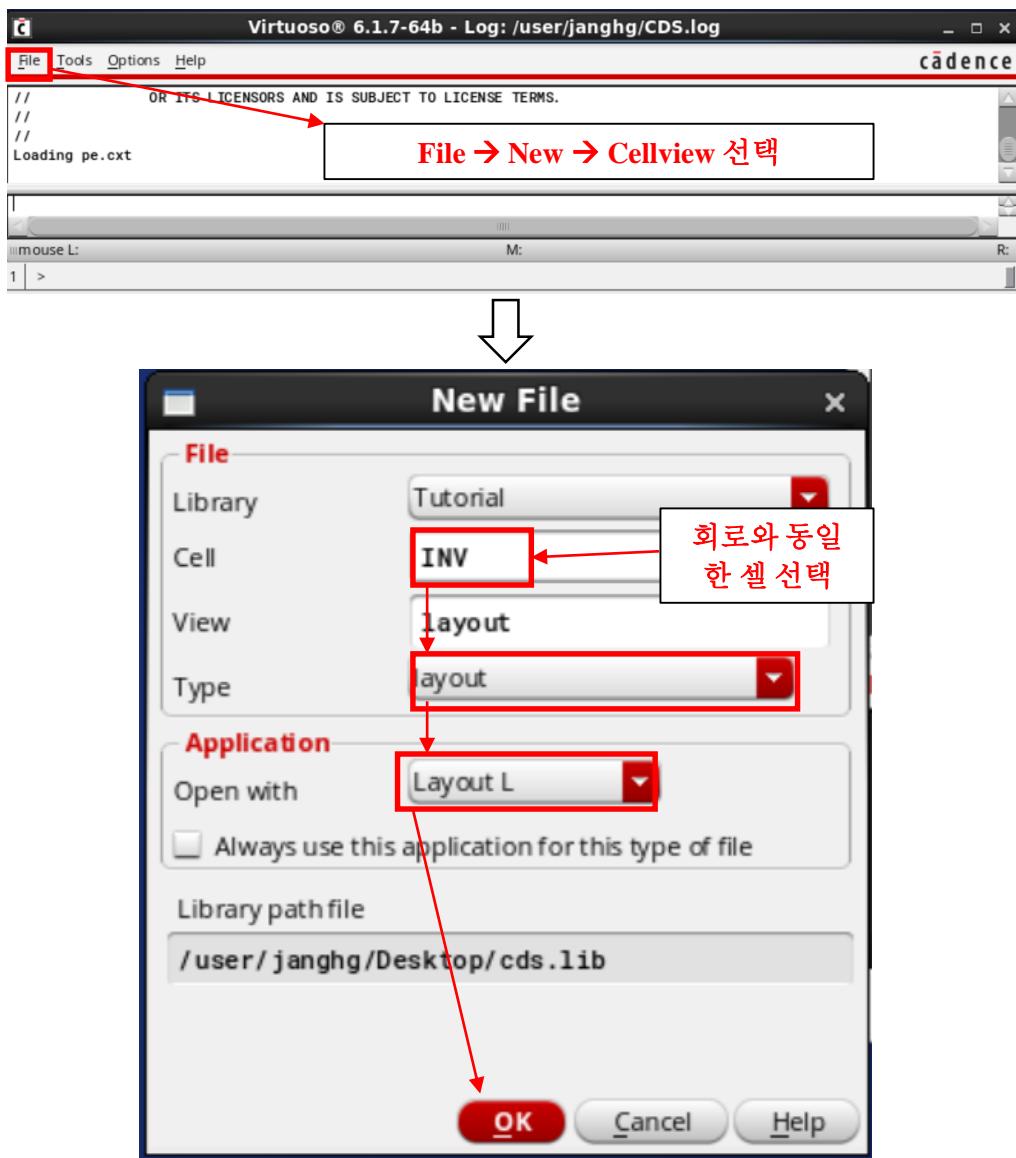
## 4. Layout

## 4. Layout

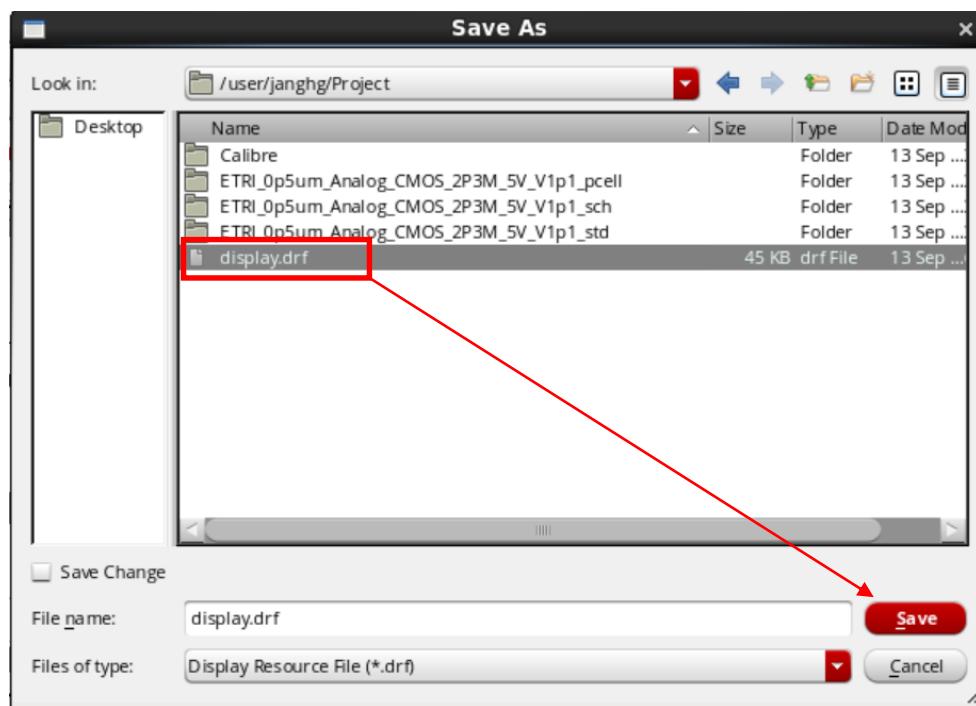
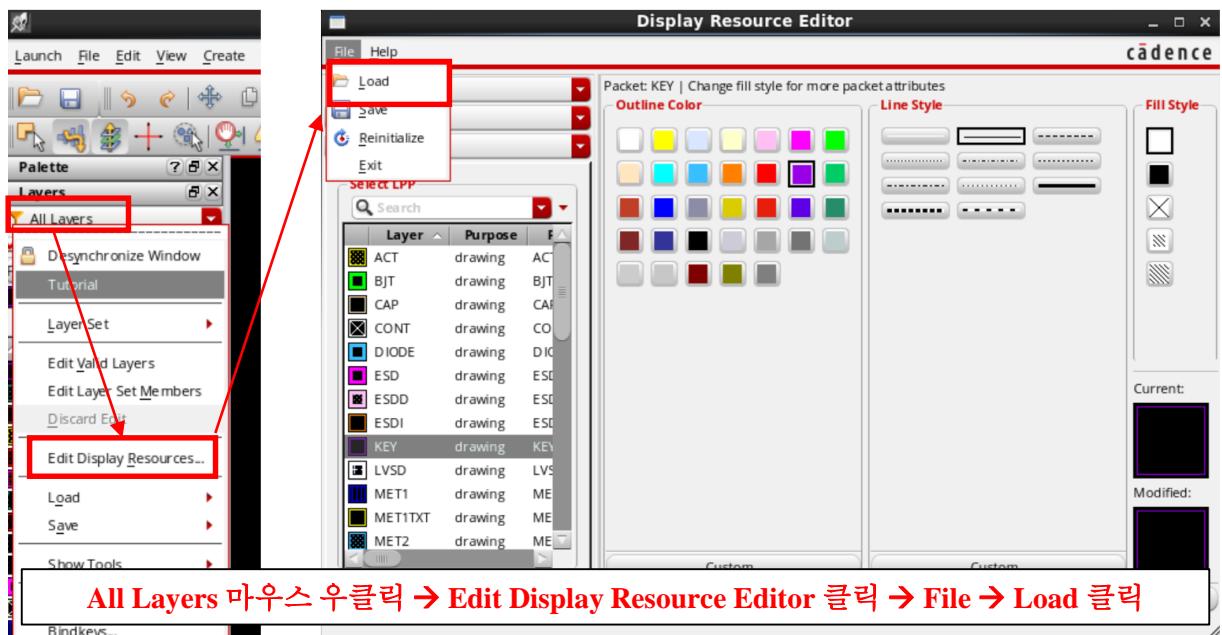
- 목적 : 반도체 회로 제작을 위한 레이아웃 설계
- 예: 설계된 인버터 회로로 적용

### 1) 인버터 회로의 레이아웃 설계

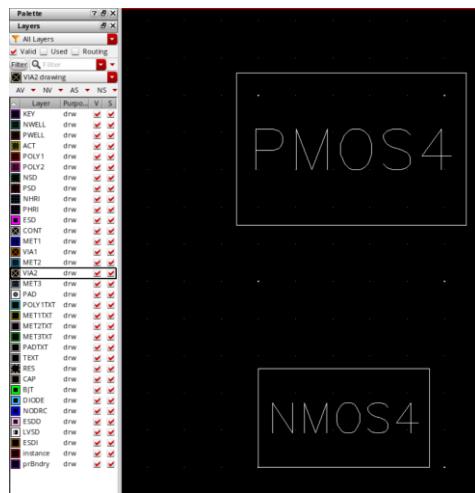
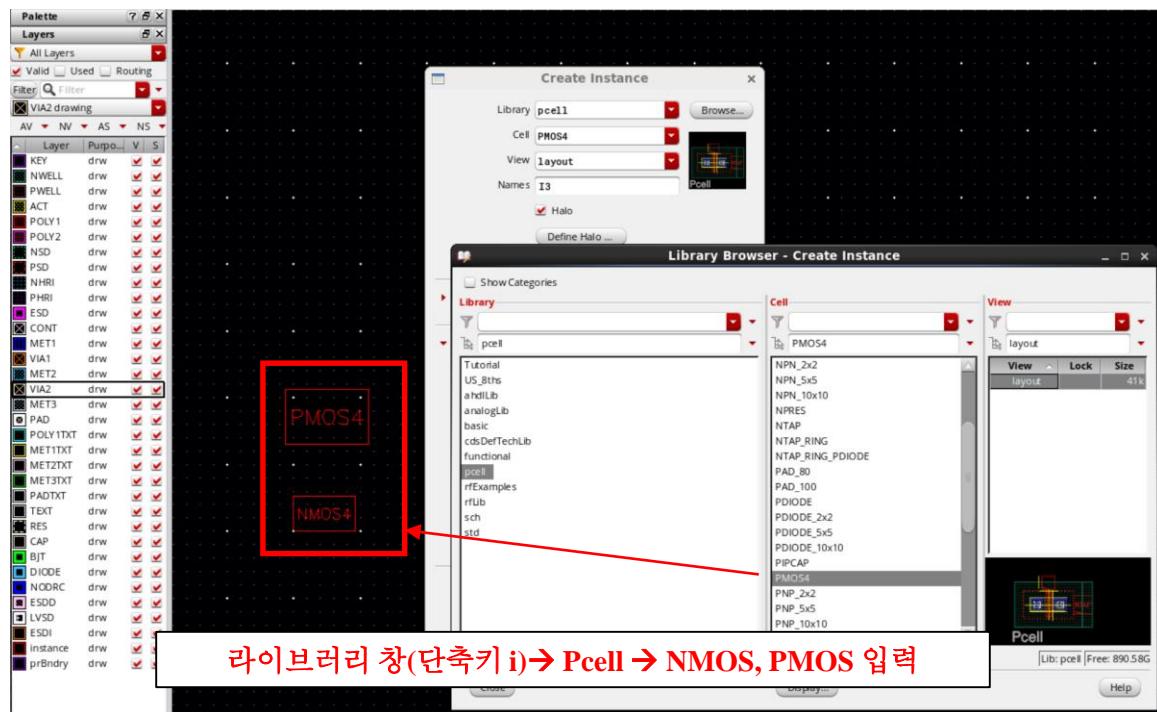
#### ① 레이아웃 디자인 설계 프로그램 실행



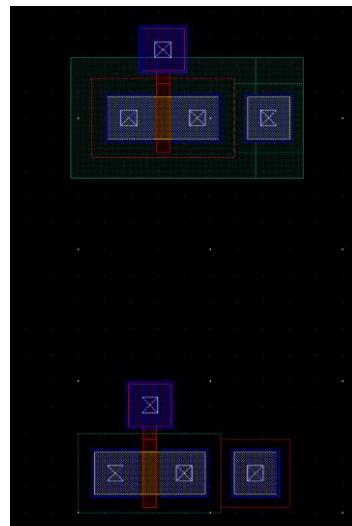
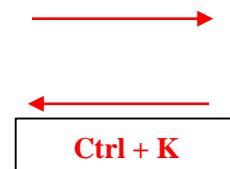
## ② Display resource 파일 불러오기



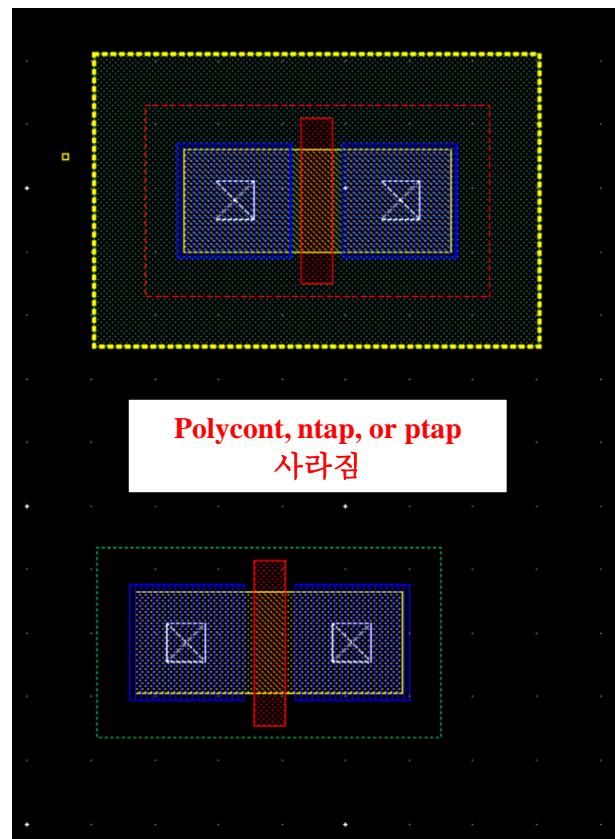
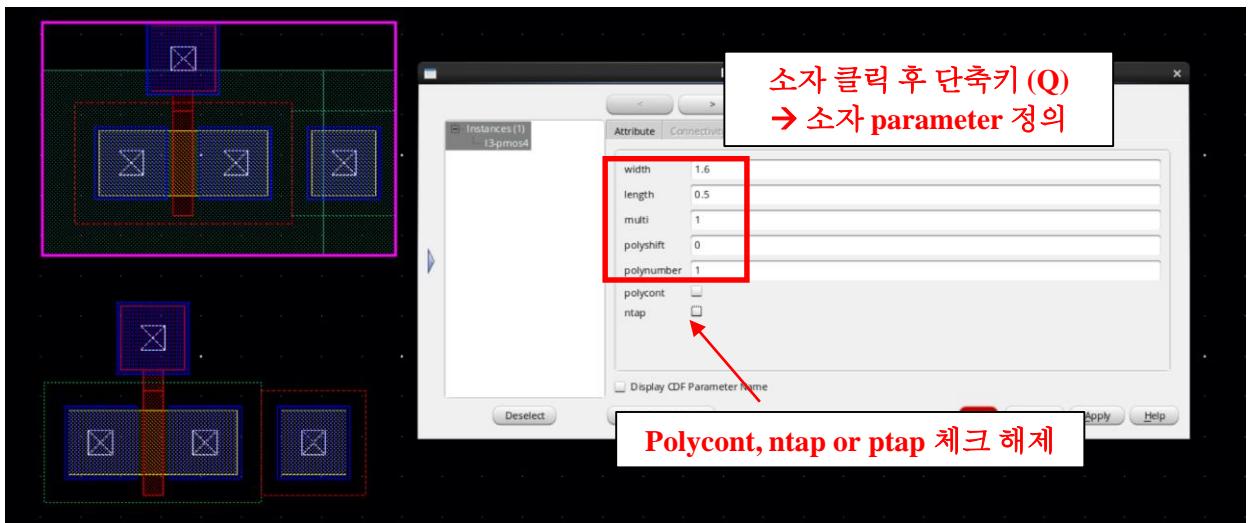
### ③ Pcell 불러오기



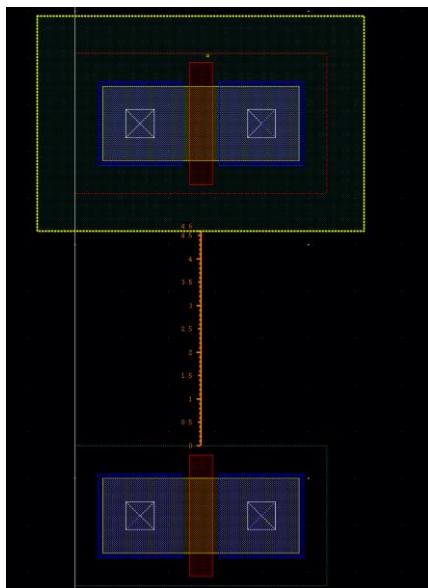
**Shift + K**



#### ④ Pcell 파라미터 설정

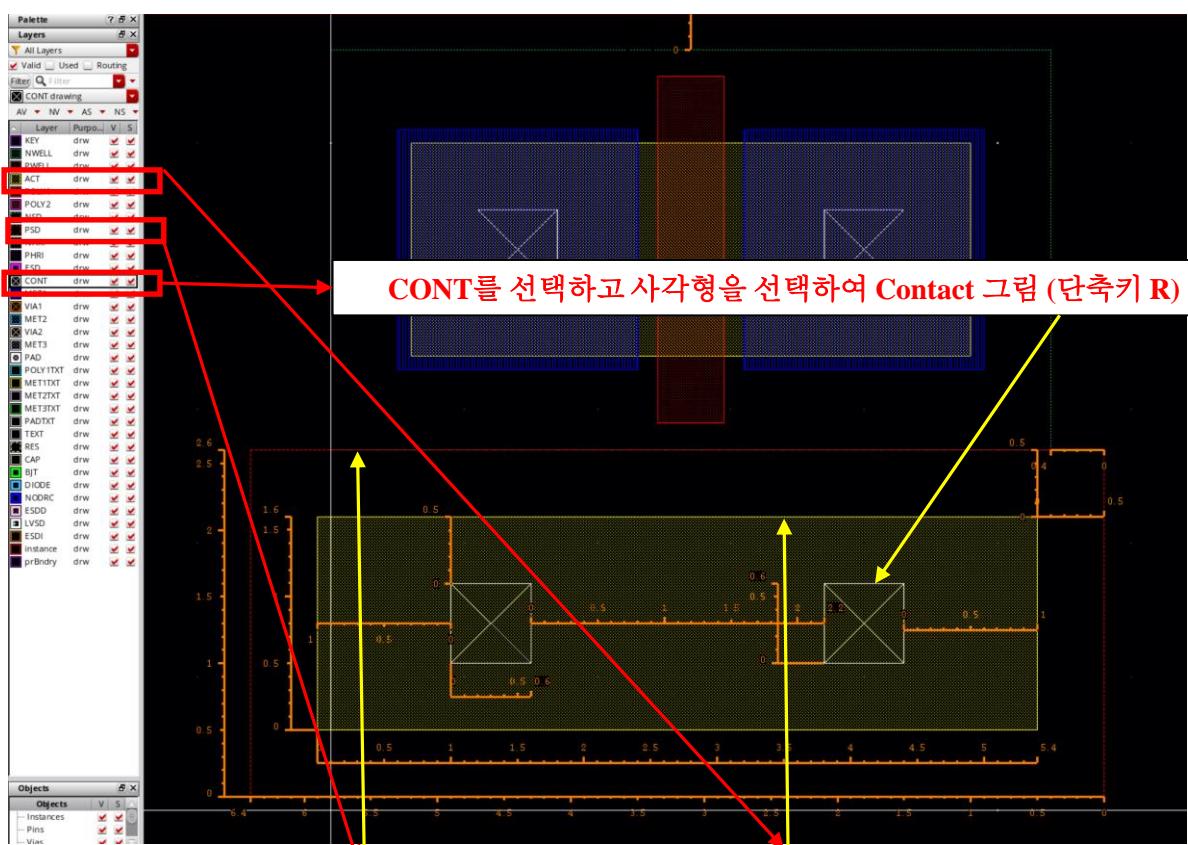


## ⑤ Layout 진행



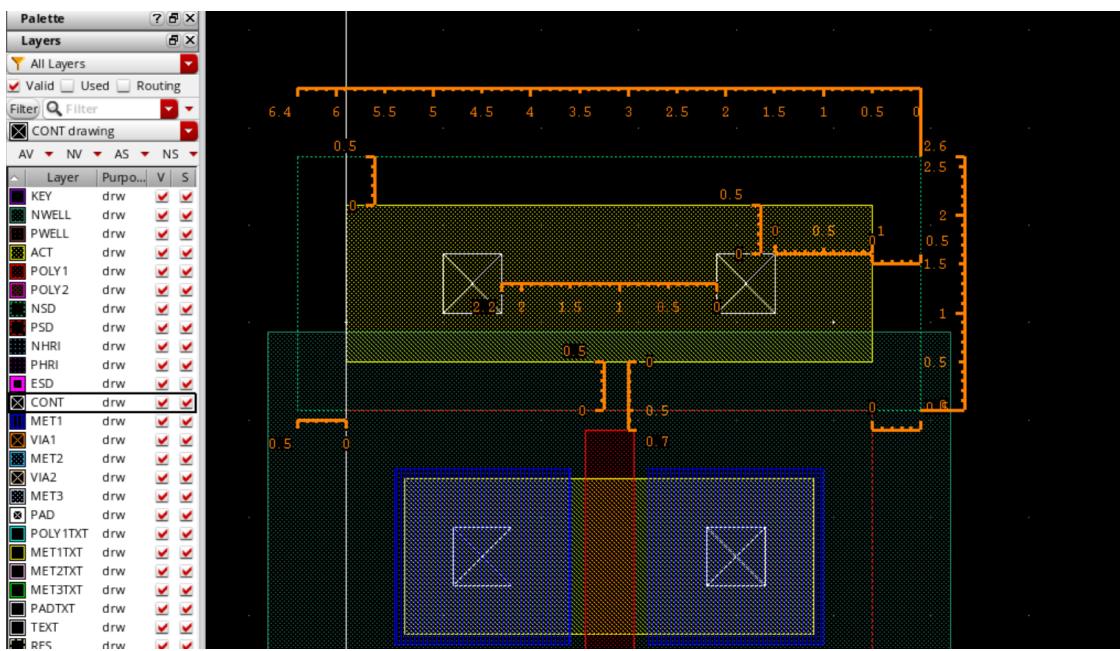
Ruler를 이용하여 사이즈를 확인함( 단축키 K)  
모든 Ruler를 사라지게 하는 단축키 → Shift + K

PMOS, NMOS 적절한 위치 배치

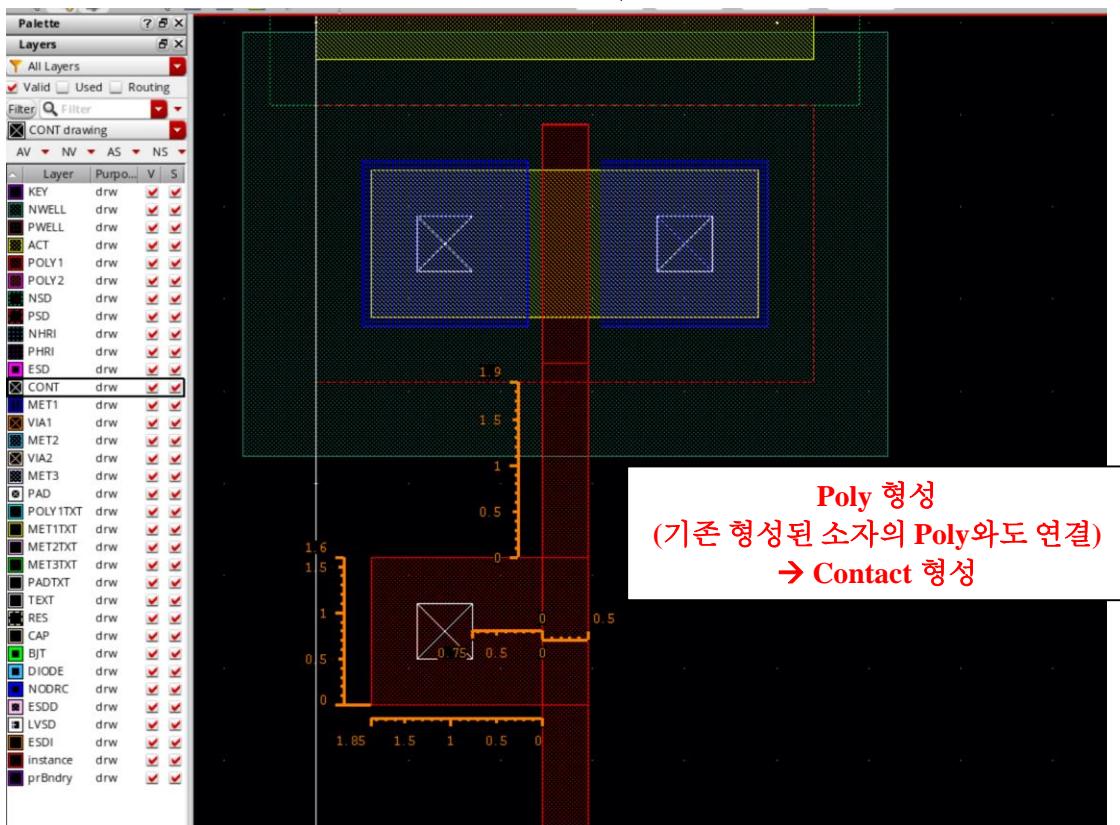


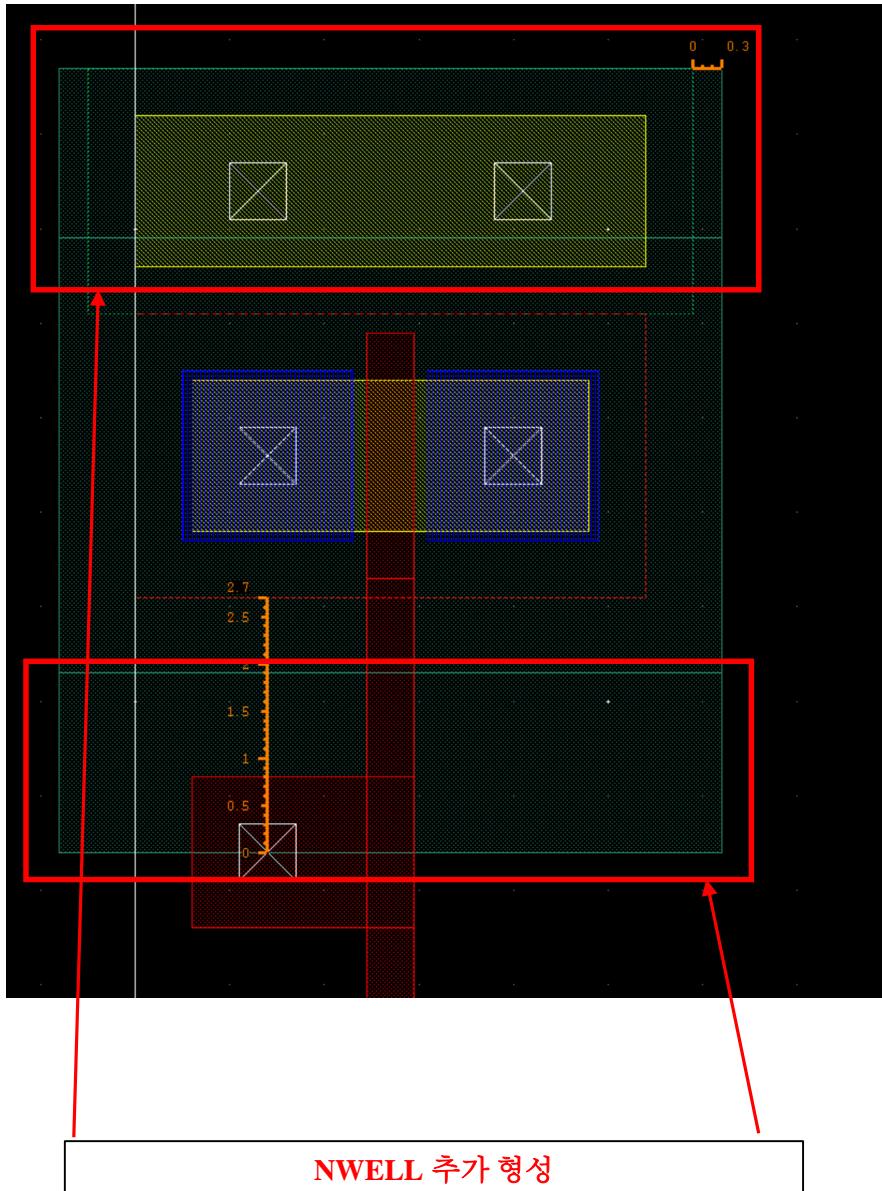
PSD 선택 → 단축키 R → PSD 그림

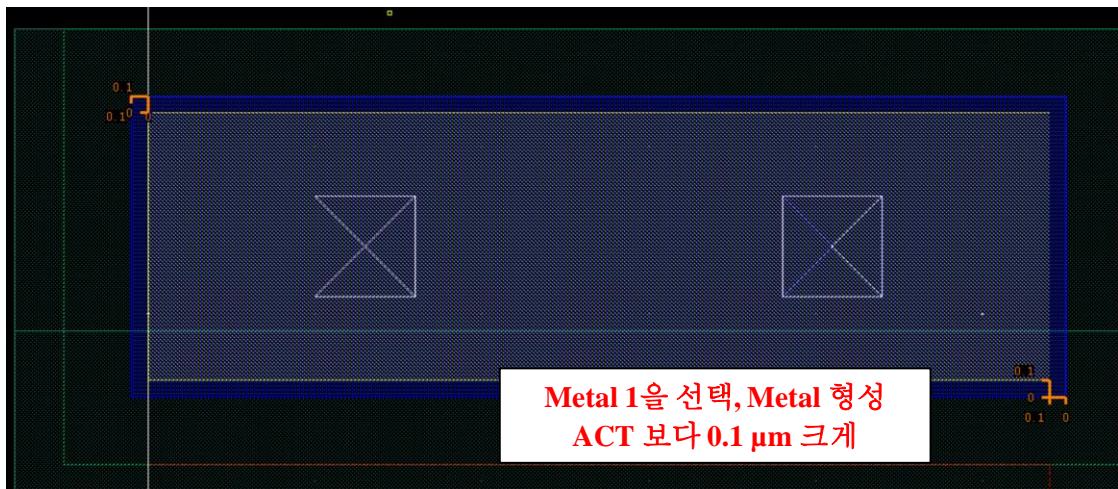
ACT 선택 → 단축키 R → ACT 그림



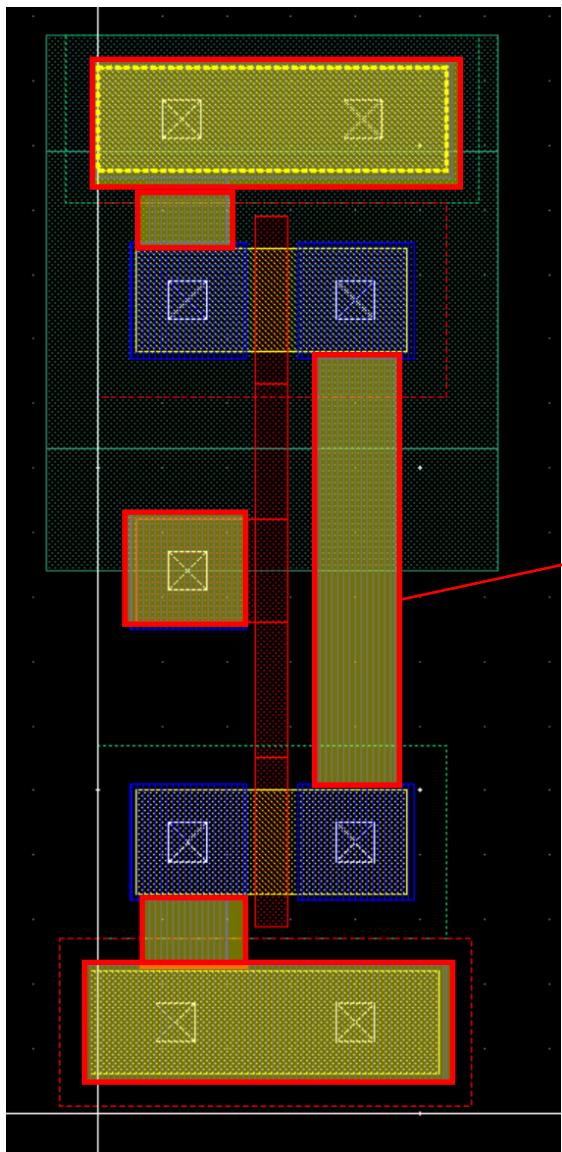
VDD : NSD → ACT → CONT 순서로 설계







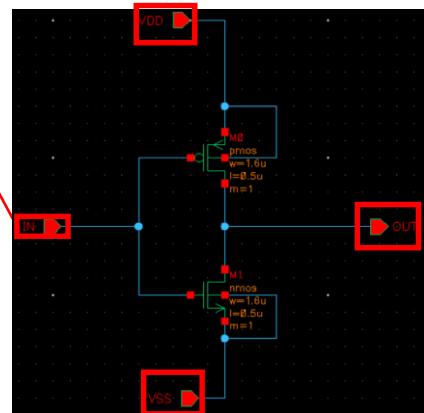
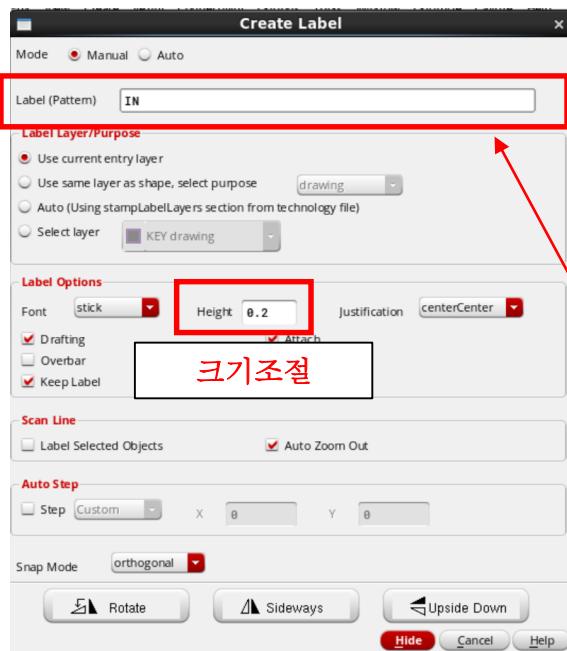
Metal 1을 선택, Metal 형성  
ACT 보다 0.1  $\mu\text{m}$  크게



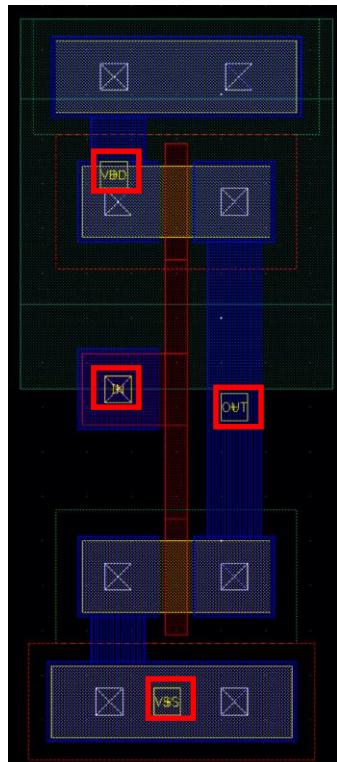
위와같은 방법으로 Metal 1을  
이용하여 좌측과 같이 소자간  
연결

## ⑥ Label 할당

MET3	drw	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
PAD	drw	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
POLY1TXT	drw	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<b>MET1TXT</b>	<b>drw</b>	<b><input checked="" type="checkbox"/></b>	<b><input checked="" type="checkbox"/></b>
MET2TXT	drw	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
MET3TXT	drw	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>

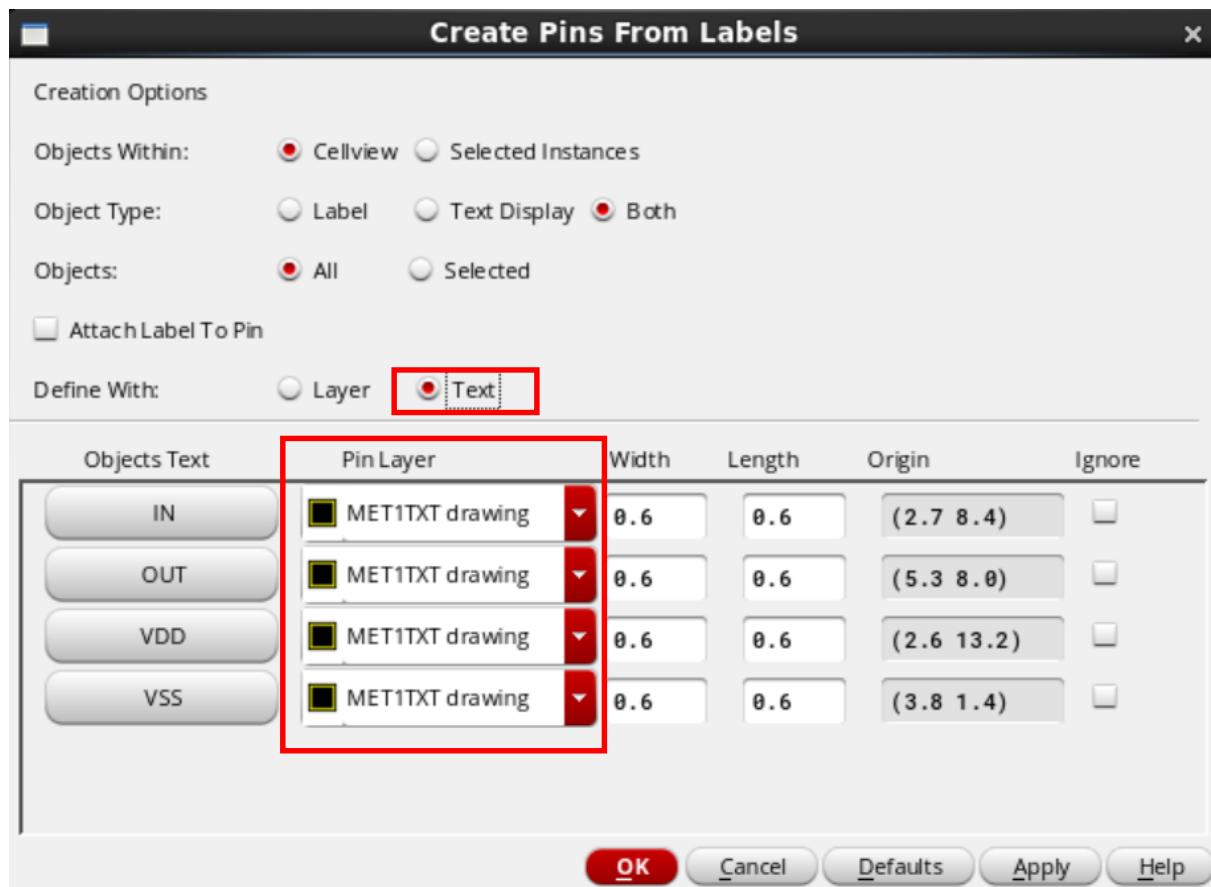


Label 설정 : MET1TXT Layer 선택 → Create → Label (단축키 L)  
→ Label명은 회로도와 동일하게 할당



Metal1 안쪽으로 각각의  
Label 배치

## ⑦ Label로 부터 Pin 할당



File → Save

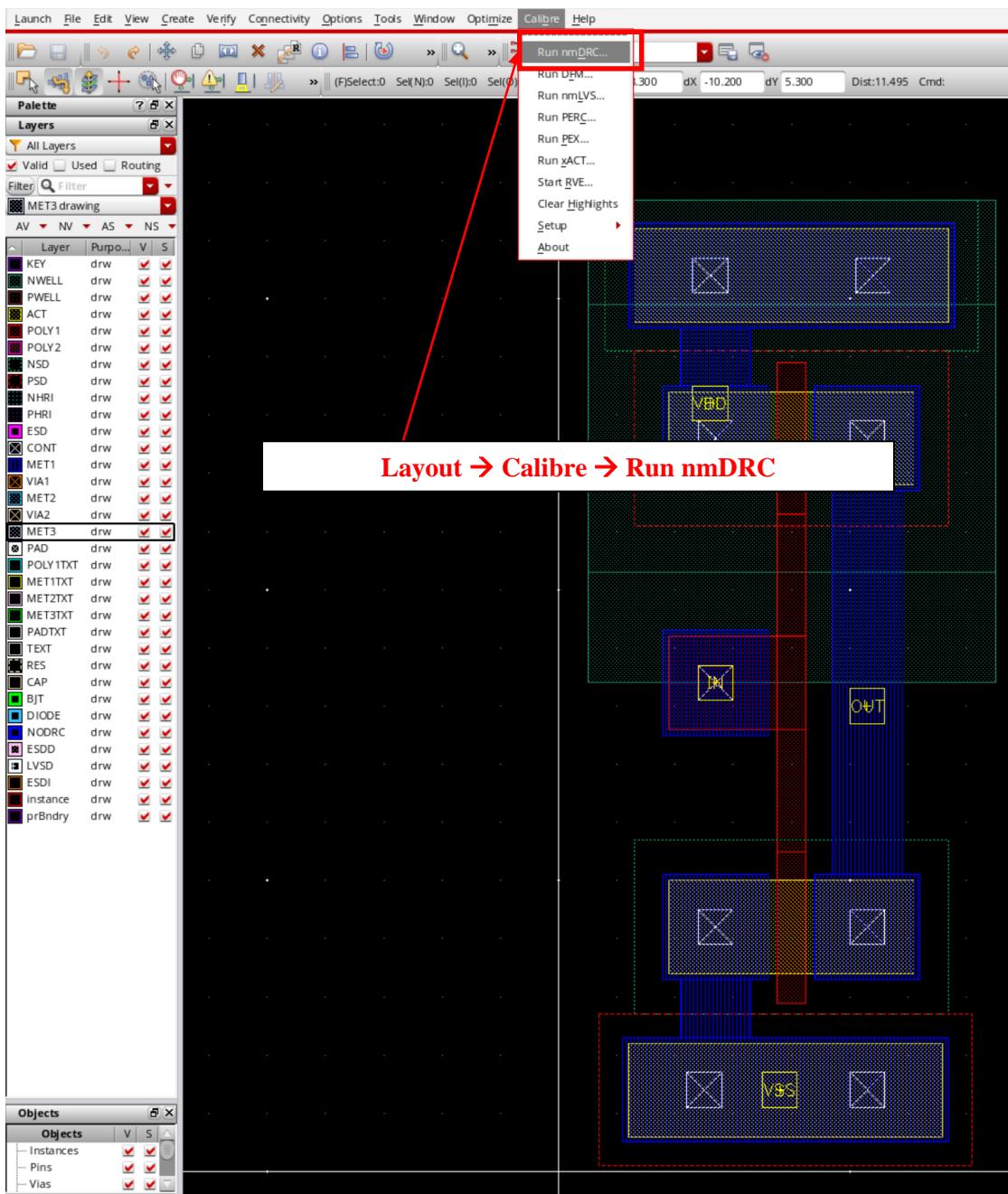
## **5. DRC (Design Rule Check)**

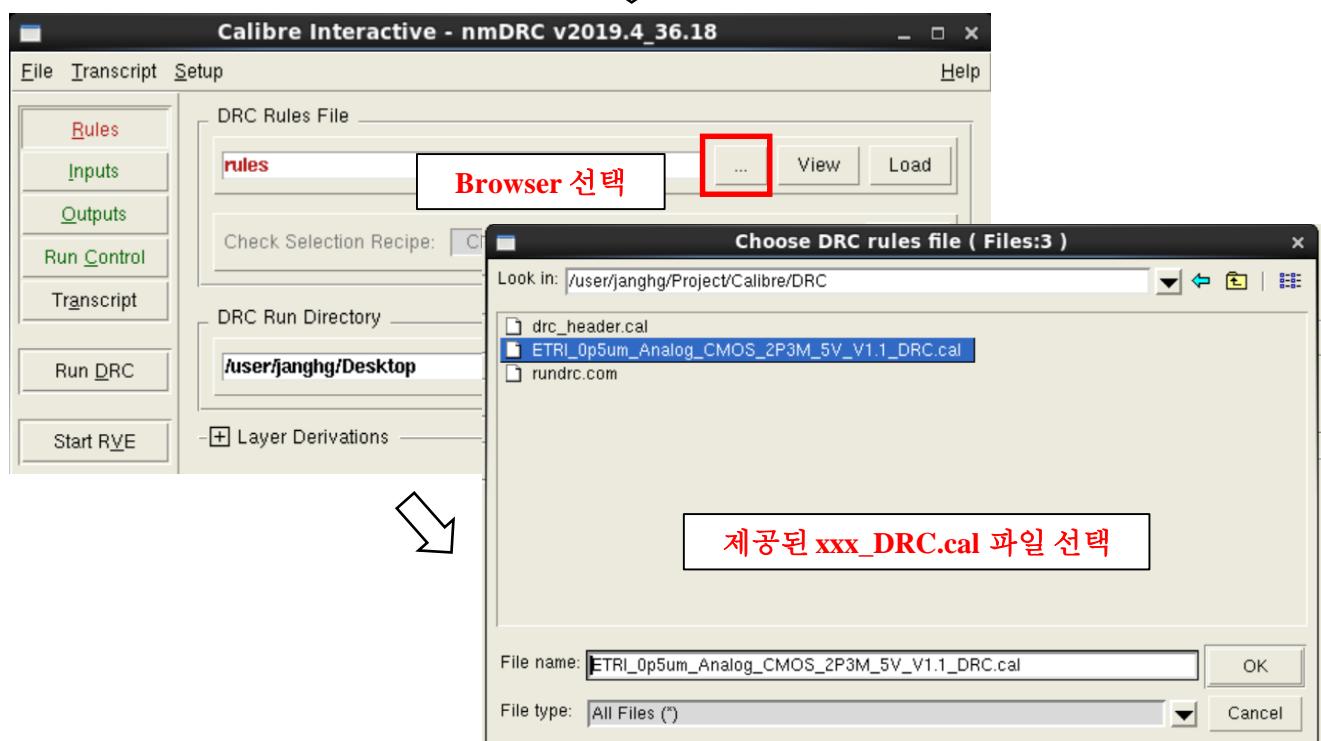
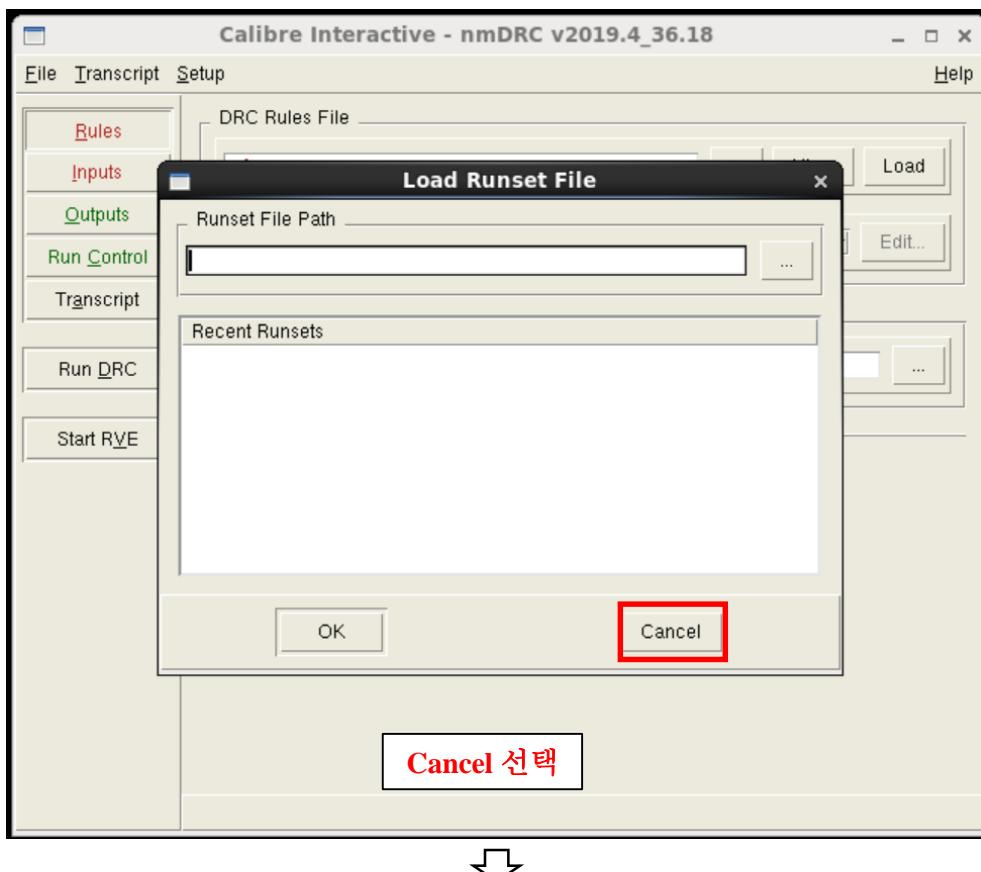
## 5. DRC

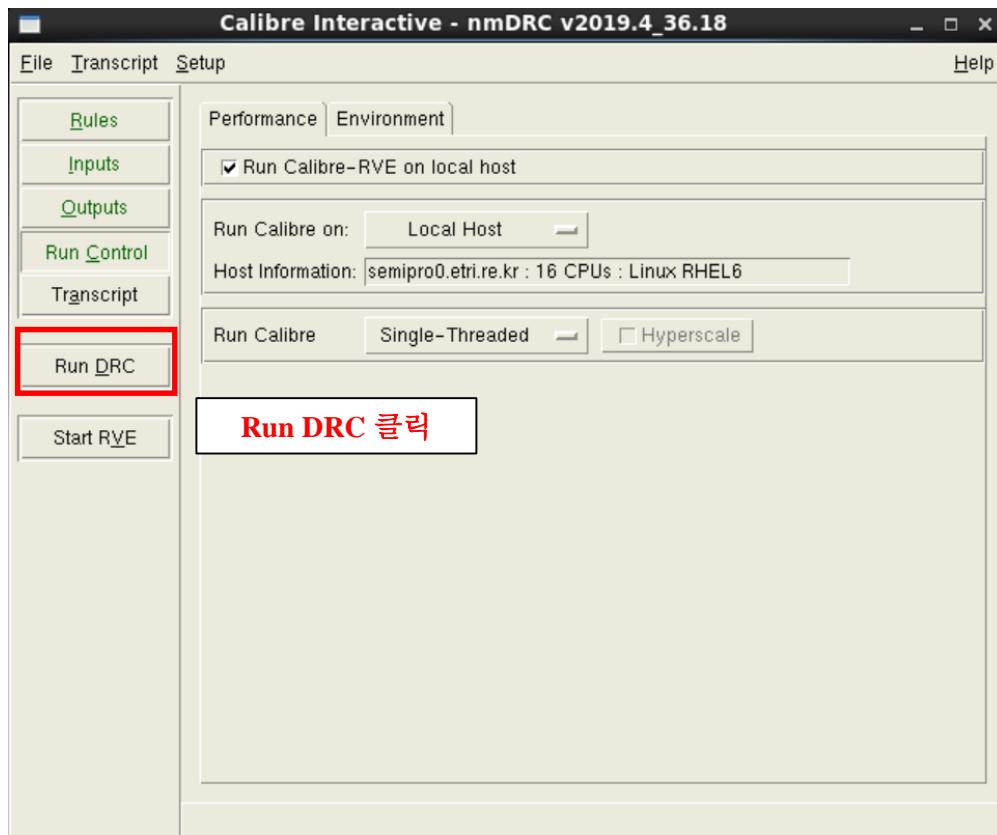
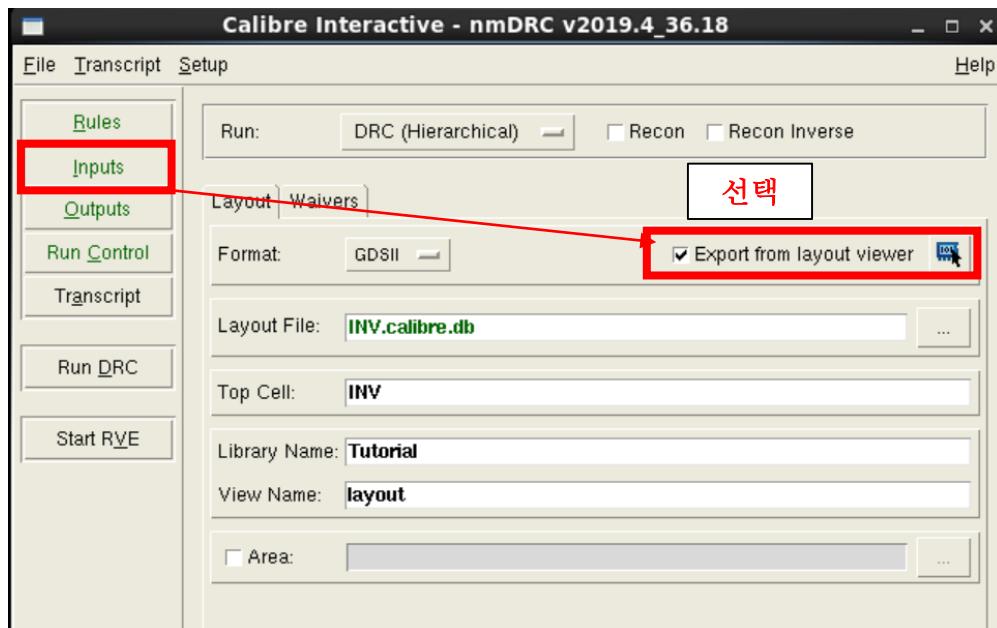
- 목적 : 설계된 레이아웃 디자인의 디자인룰에 적합한지 검토

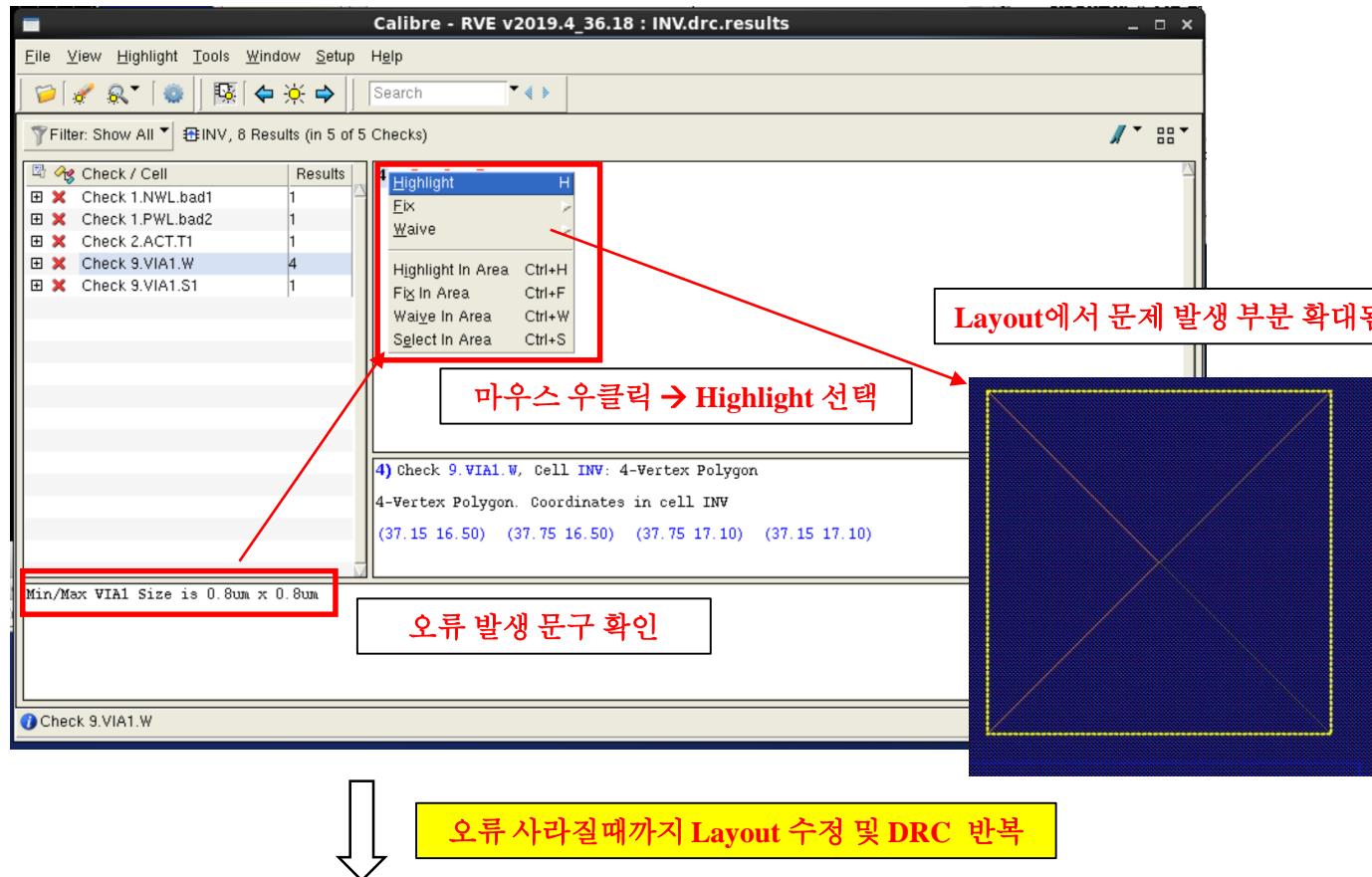
### 1) DRC 검토

#### ① DRC 검증 방법

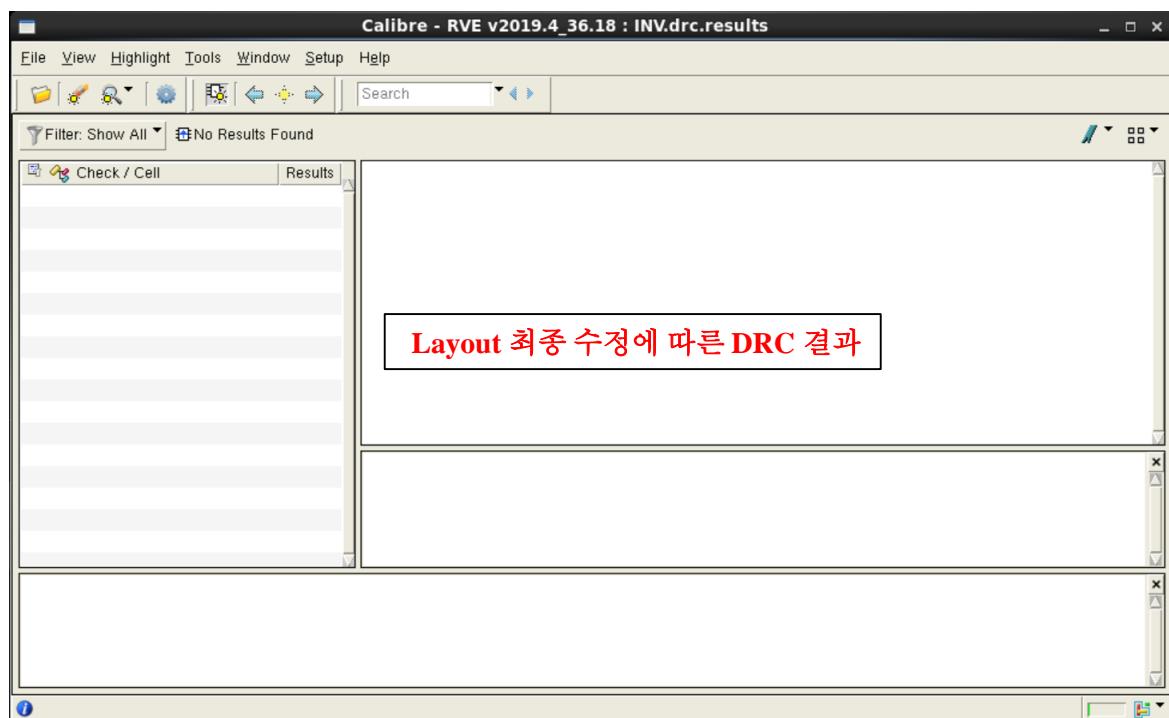








오류 사라질때까지 Layout 수정 및 DRC 반복



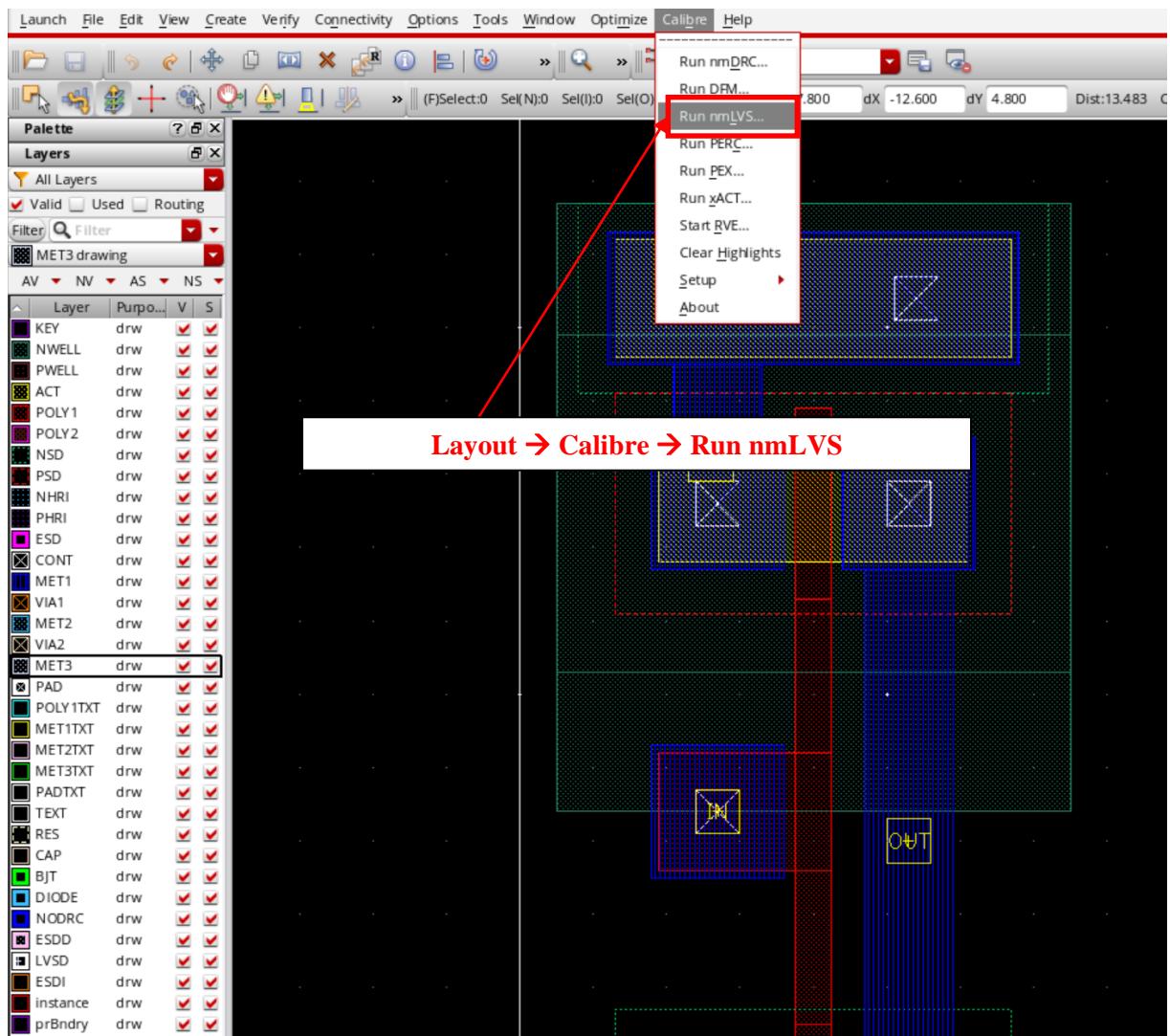
## 6. LVS (Layout Versus Schematic)

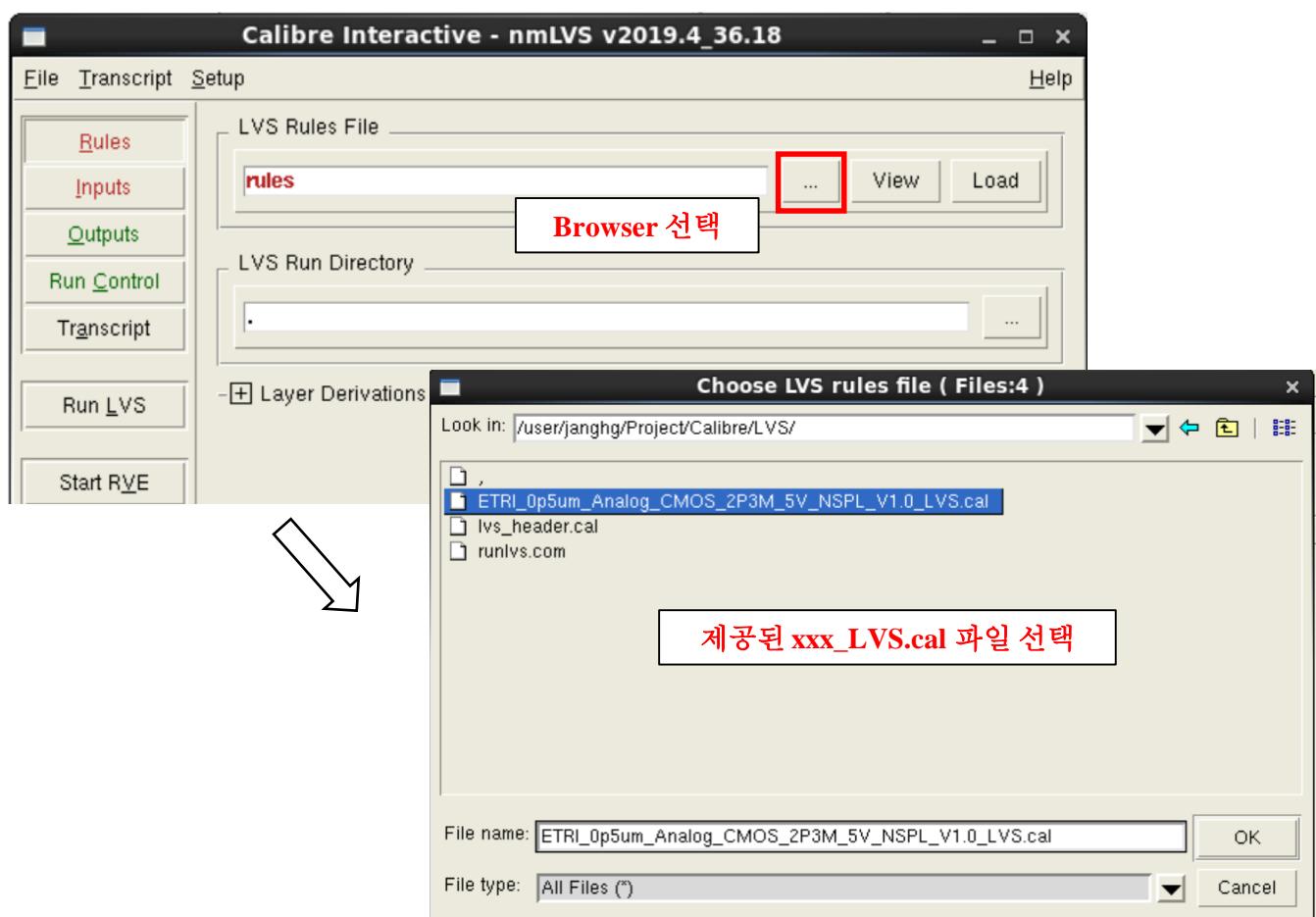
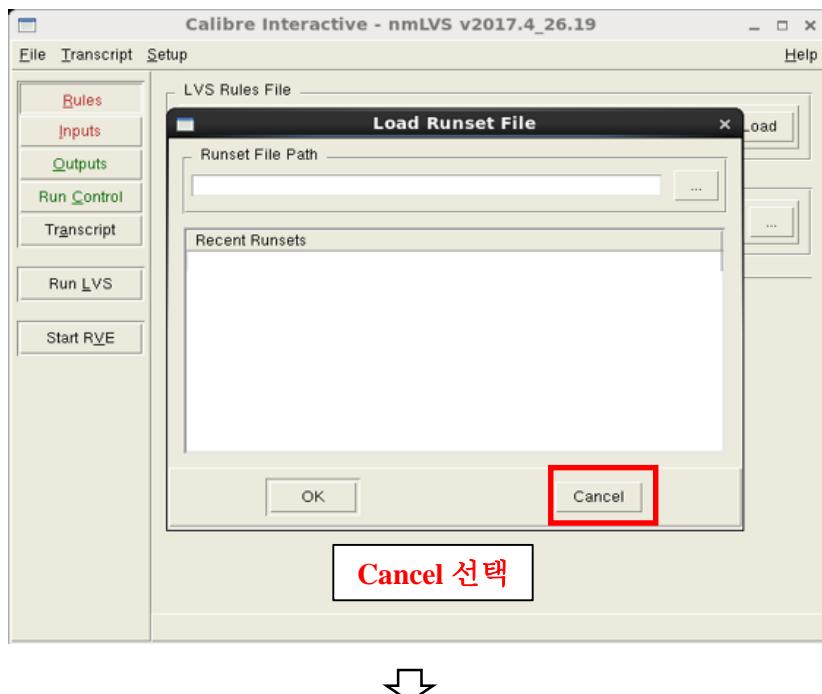
## 6. LVS

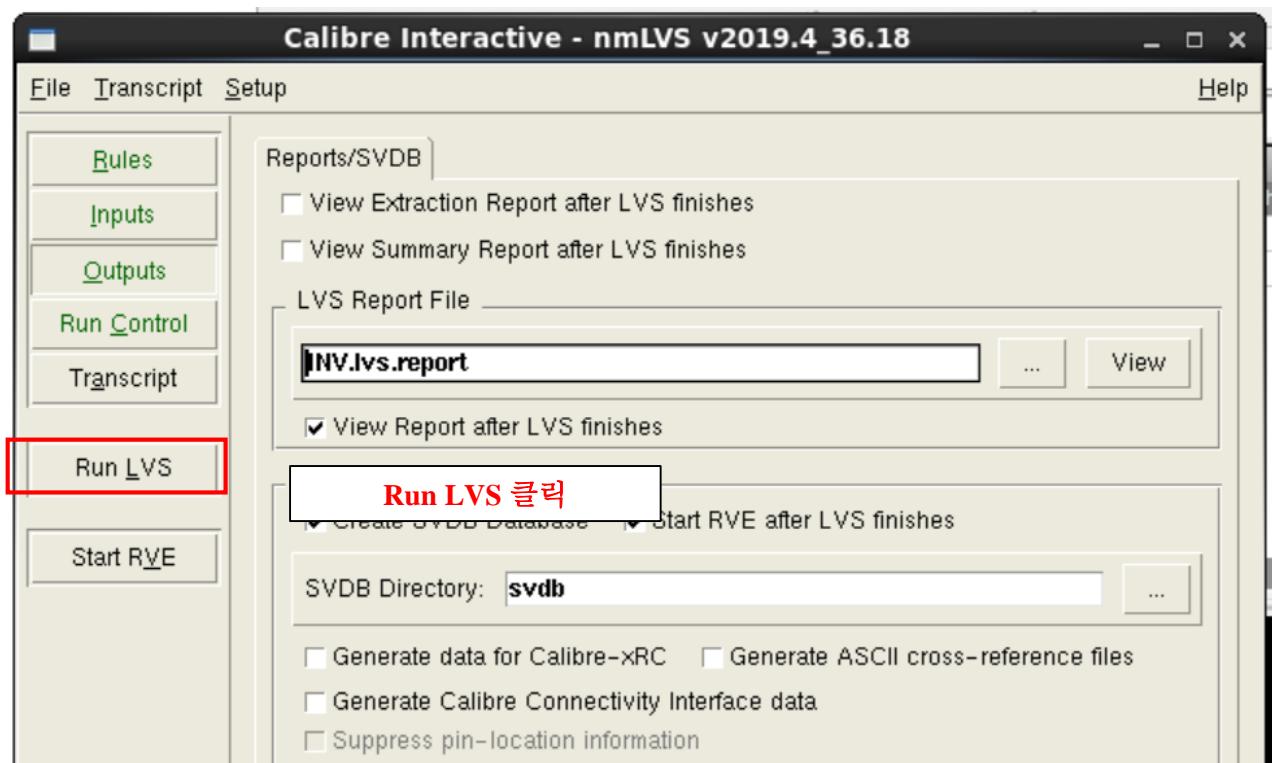
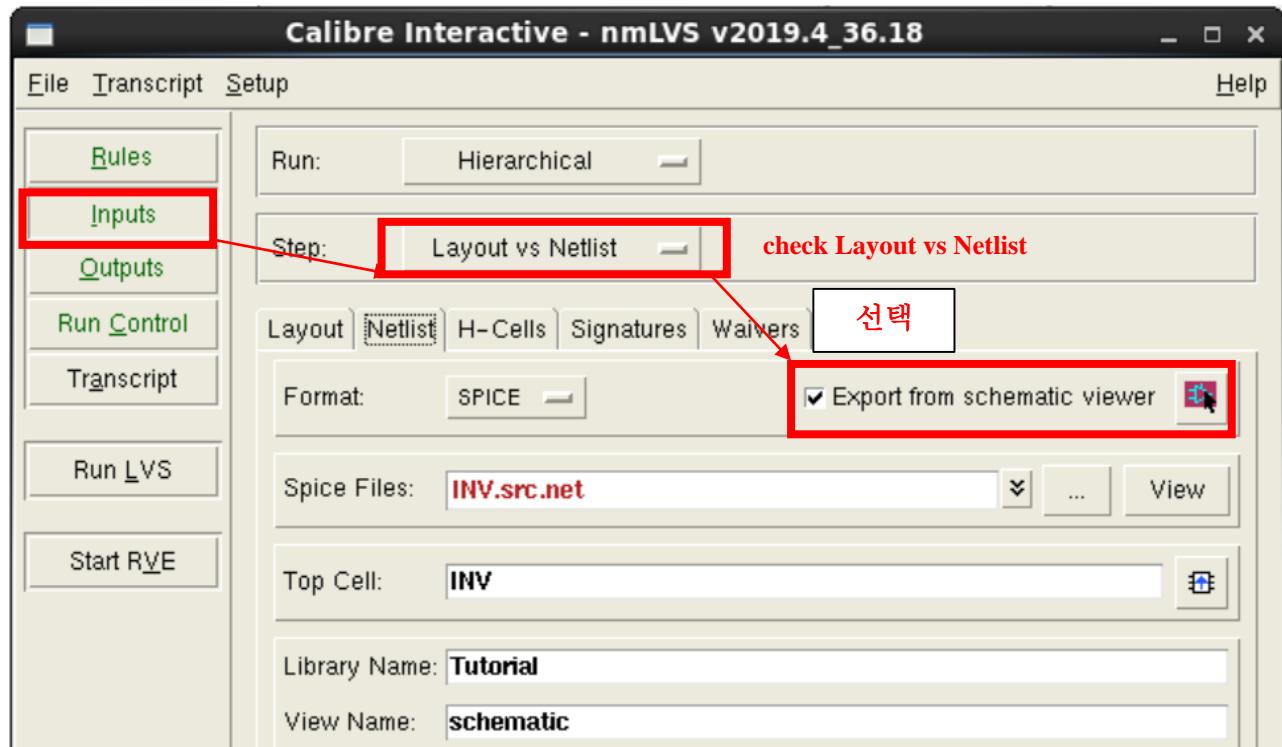
- 목적 : 설계한 Layout과 Schematic 비교

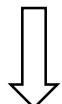
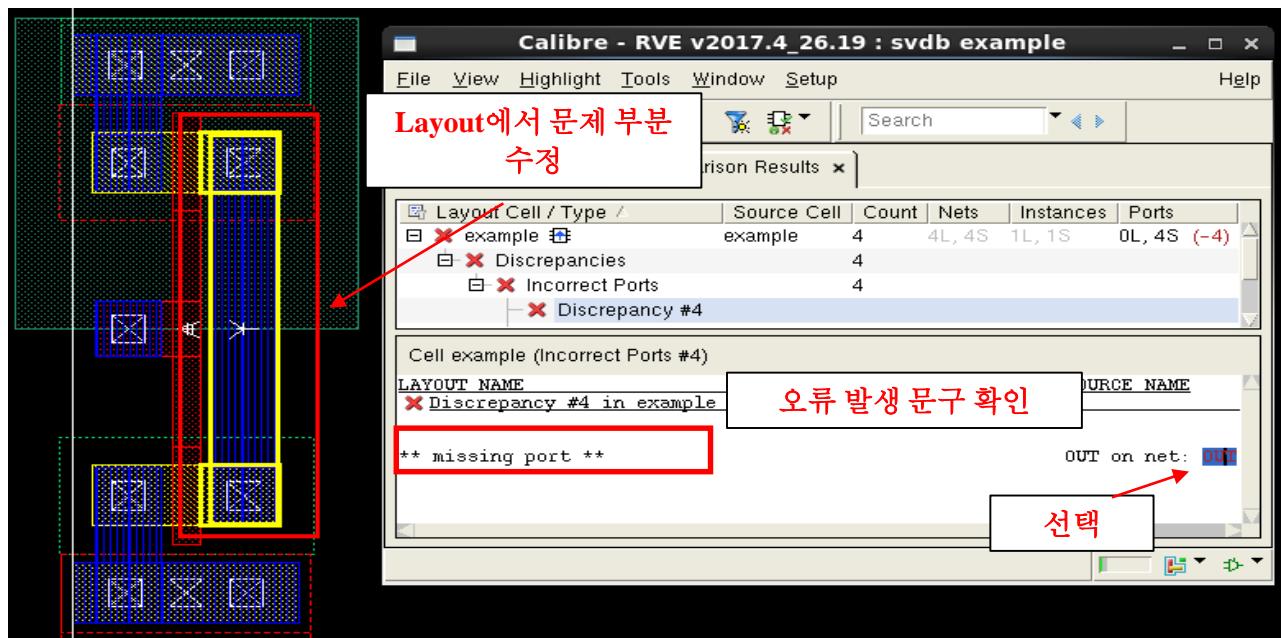
### 1) LVS 검토

#### ① LVS 검증 방법

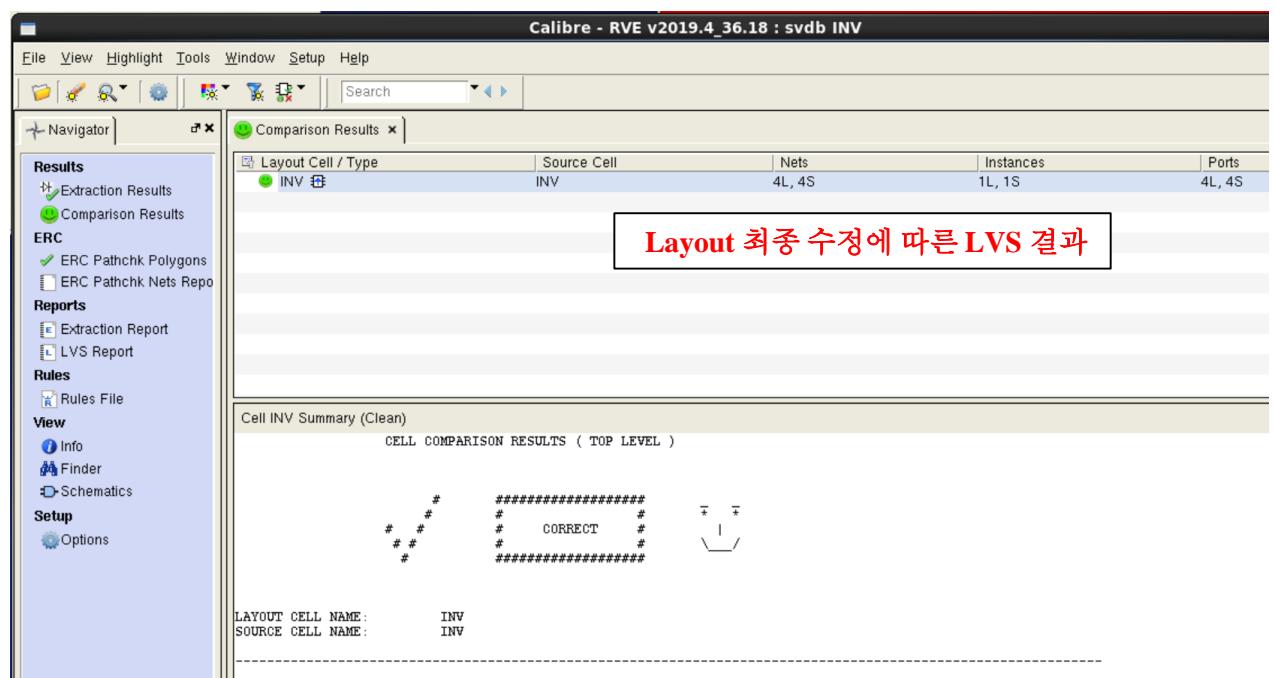








오류 사라질때까지 Layout 수정 및 LVS 반복



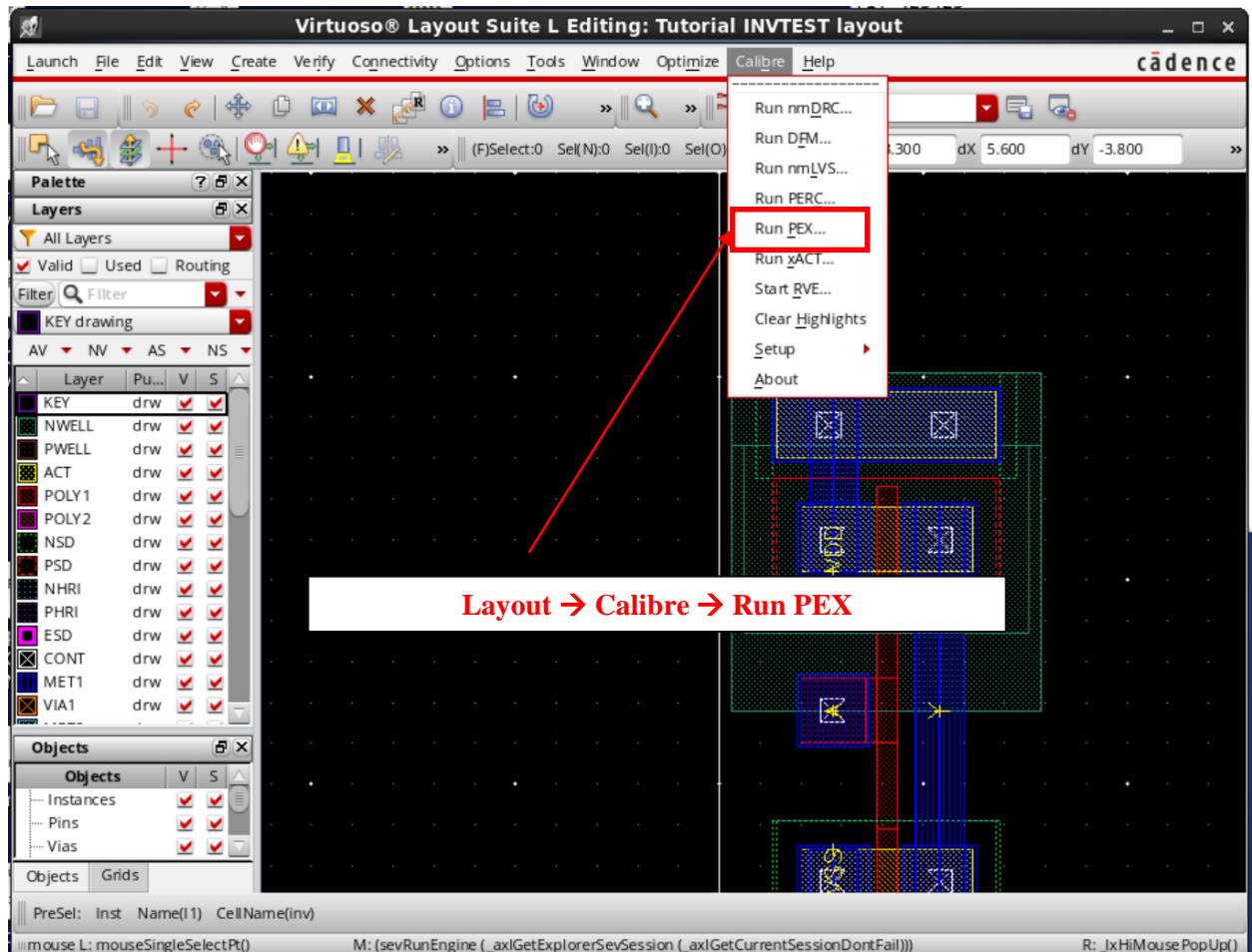
## 7. PEX (Parasitic EXtraction)

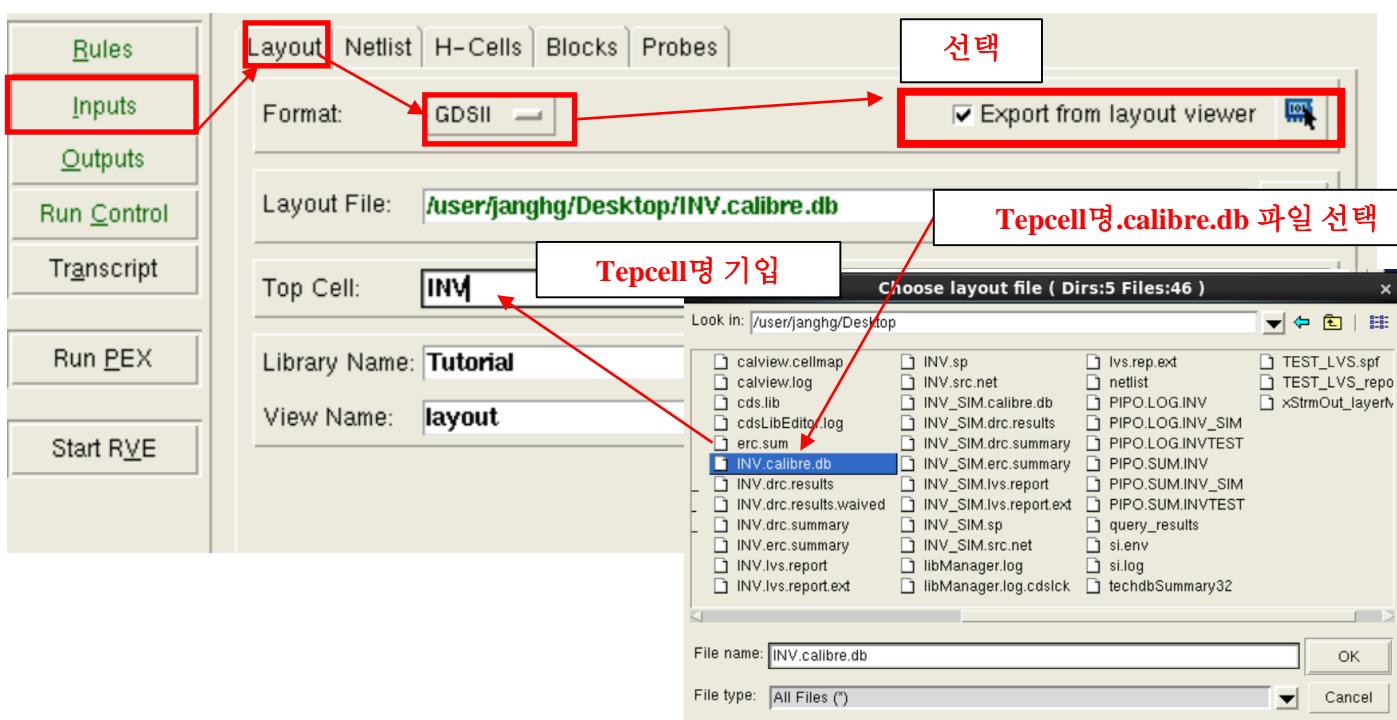
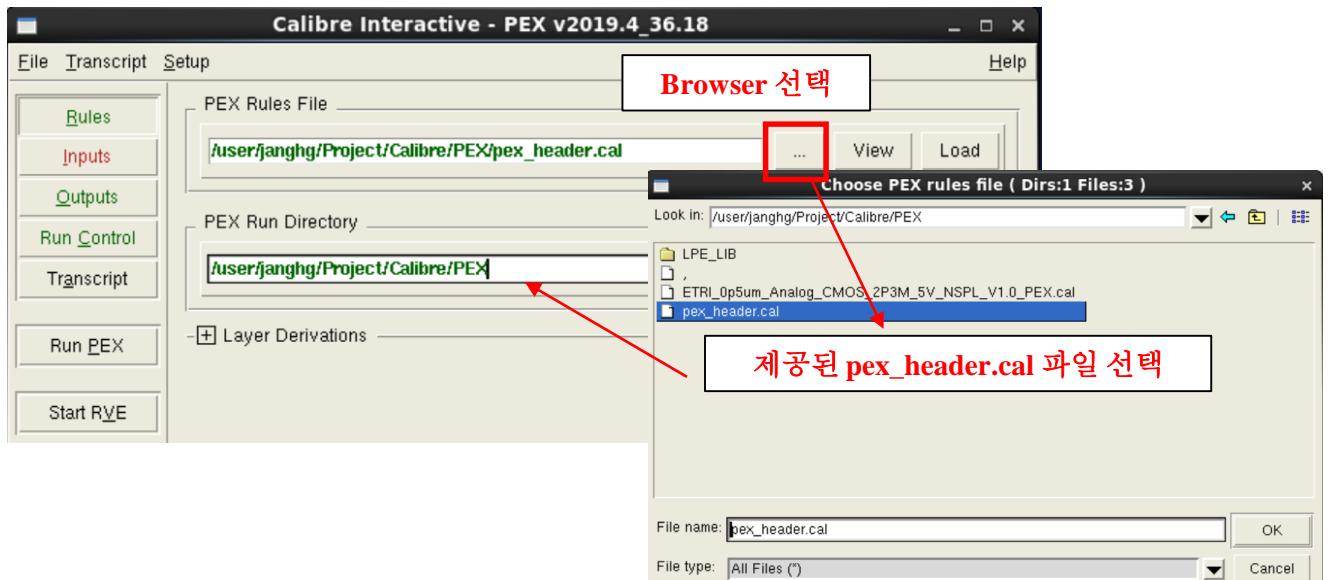
## 7. PEX

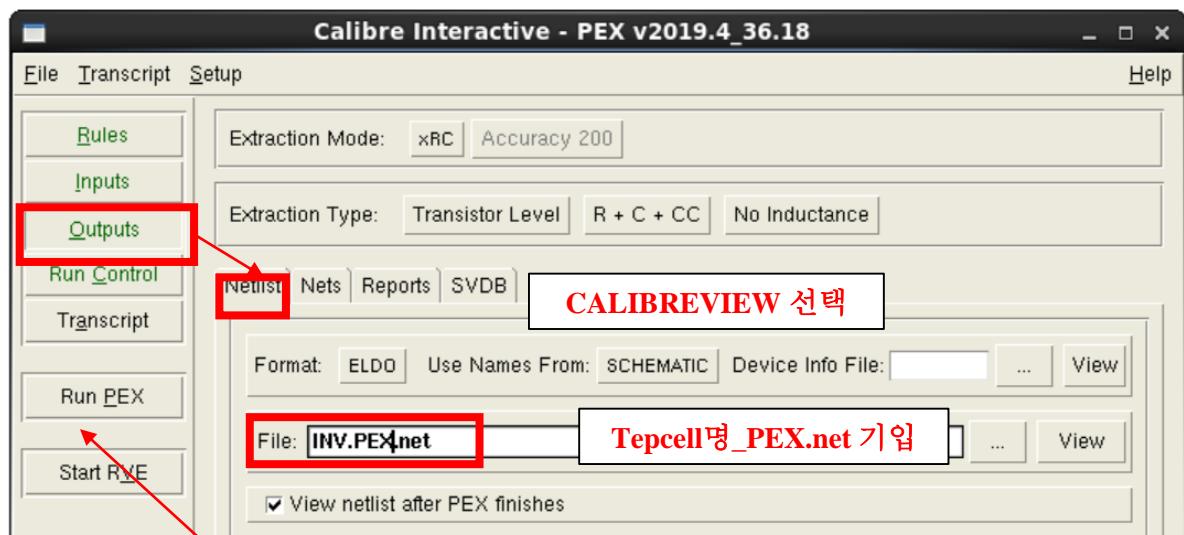
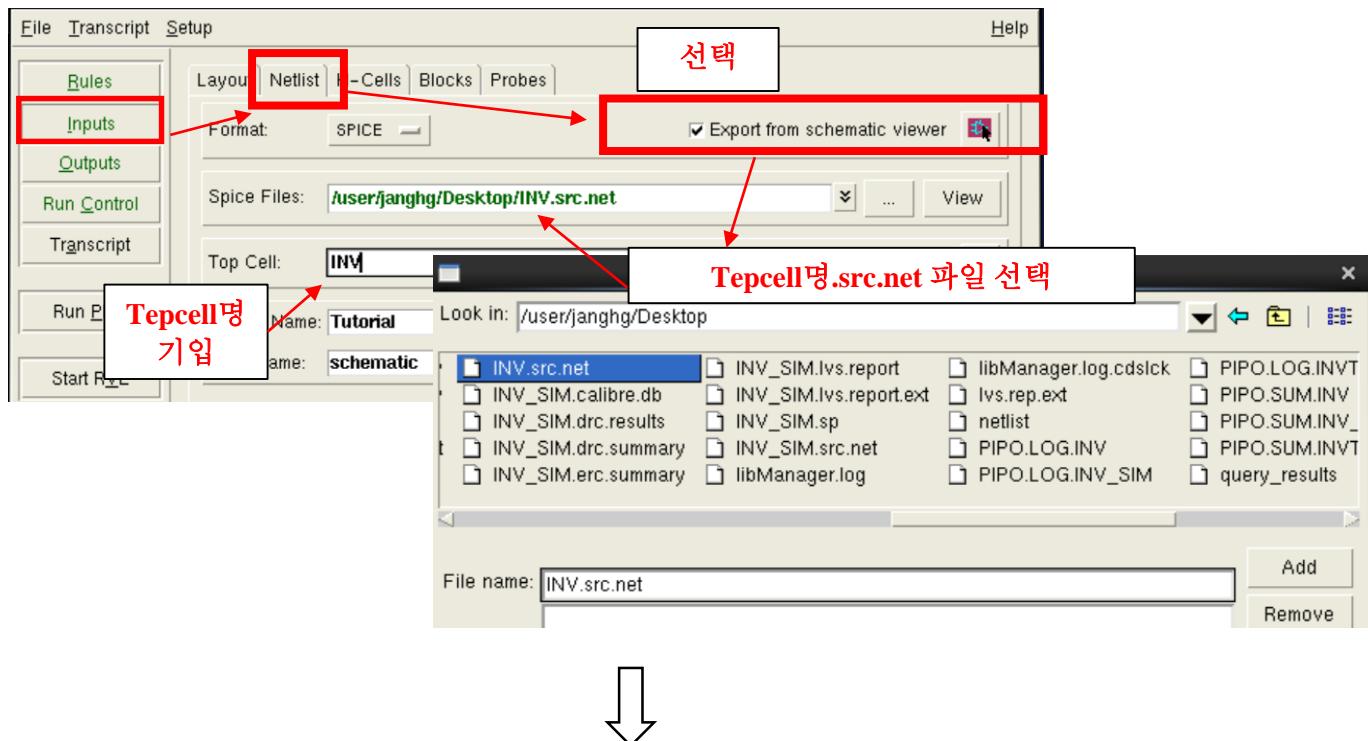
- 목적 : Parasitic 성분 추출

### 1) PEX 검토

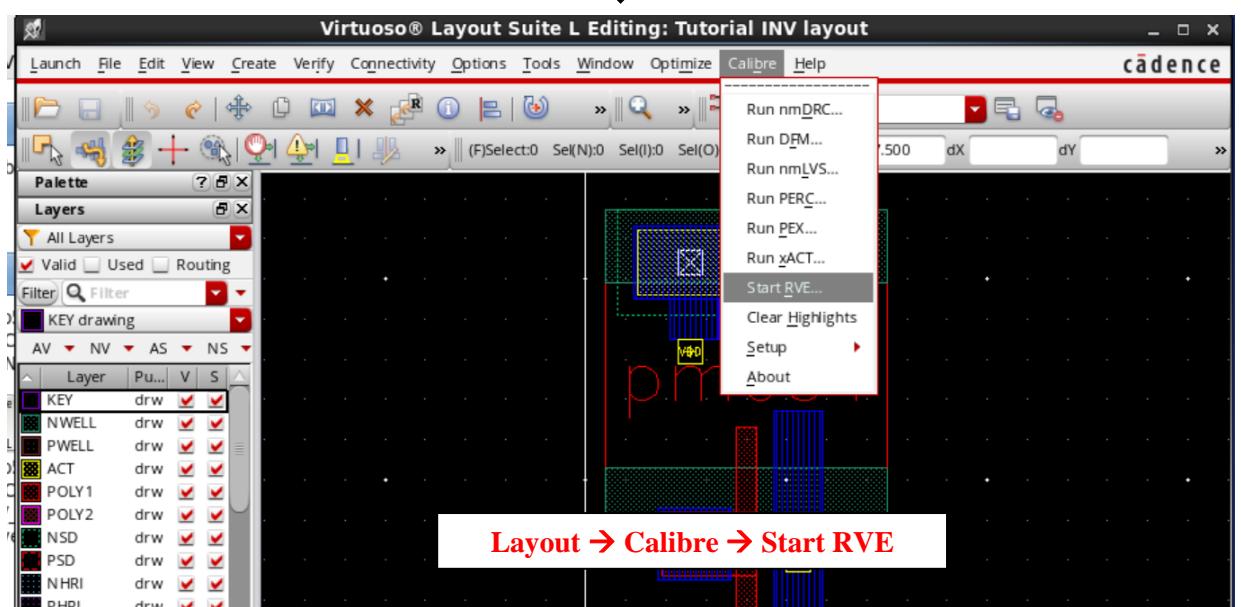
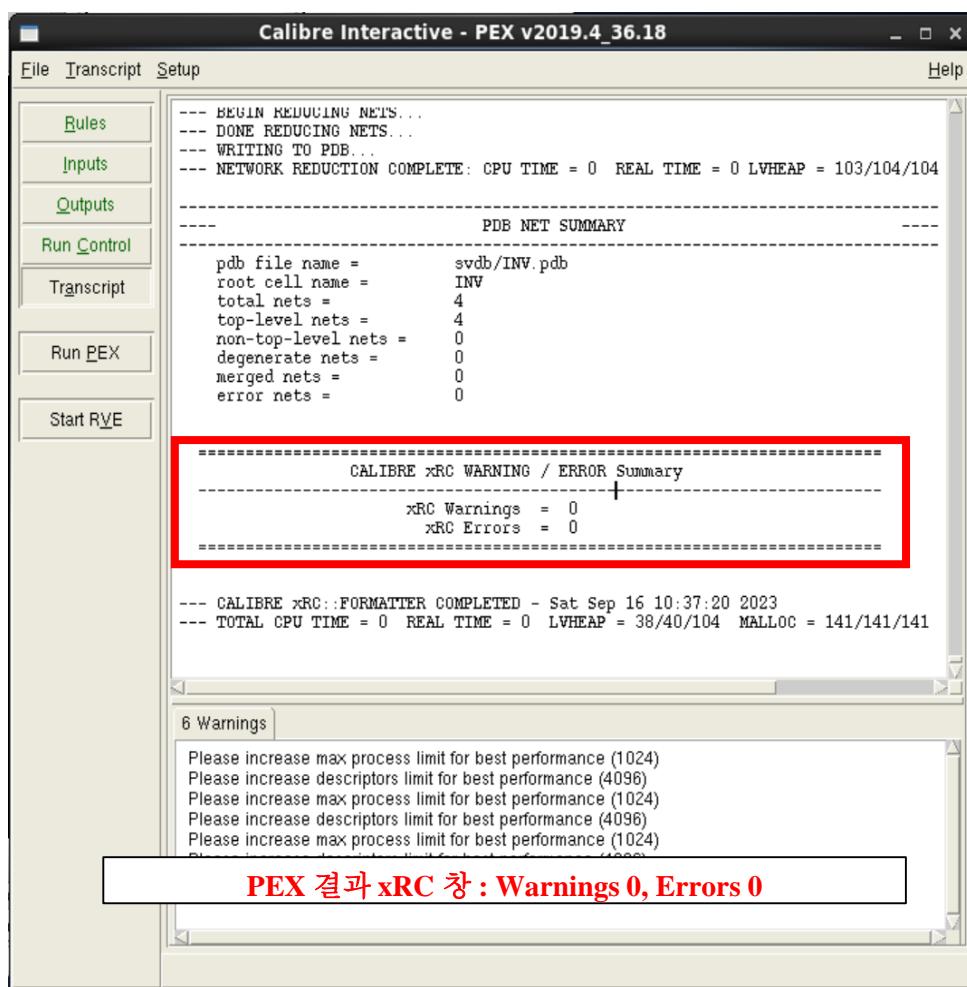
#### ① PEX 진행 방법

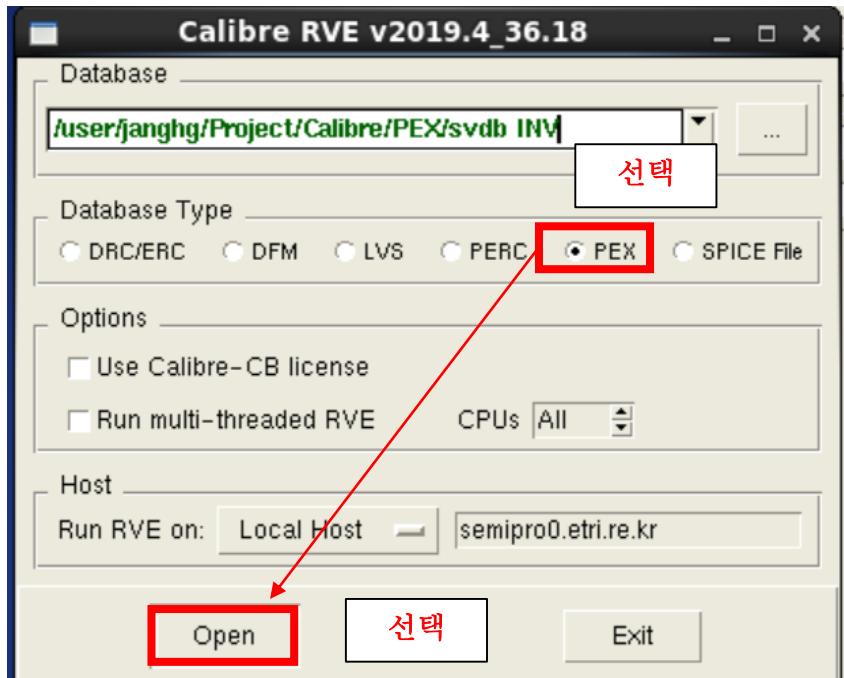






**RunPEX!!!**





No.	Layout Net	R Count	C Total (F)	C+CC Total (F)
1	IN	15	1.62089E-15	1.62089E-15
2	VSS	8	4.45309E-14	4.45309E-14
3	VDD	7	4.44690E-14	4.44690E-14
4	OUT	8	2.42288E-14	2.42288E-14

결과 출력