Universal Flow Configuration Variables

These are flow configuration variables that are used commonly enough that we decided to expose them to all steps and all flows.

Configuration objects, be they JSON, Tcl or directly passed to the Python API, can freely override these values.

> **Note**
>
> `?` indicates an optional variable, i.e., a value that may hold a value of `None`. OpenLane steps are expected to understand that these values are optional and behave accordingly.

Variable Name	Type	Description	
`DESIGN_DIR`	Path	The directory of the design. Should be set via command-line arguments or :meth:`Config.load` flags and not actual configuration files. If using a configuration file, `DESIGN_DIR` will be the directory where that file exists.	`None`
`PDK_ROOT`	Path	The home path of all PDKs. Should be set via command-line arguments or :meth:`Config.load` flags and not actual configuration files.	`None`
`DESIGN_NAME`	str	The name of the top level module of the design. Must be a valid C identifier, i.e., matches the regular expression `[_a-zA-Z][_a-zA-Z0-9]+`.	`None`
`PDK`	str	Specifies the process design kit (PDK). Must be a valid C identifier, i.e., matches the regular expression `[_a-zA-Z][_a-zA-Z0-9]+`.	`sky130A`
`CLOCK_PERIOD`	Decimal	The clock the desigr	

Variable Name	Type	Description	
`CLOCK_PORT`	(str | List[str])?	The name(s) of the design's clock port(s).	None
`CLOCK_NET`	(str | List[str])?	The name of the net input to root clock buffer. If unset, it is presumed to be equal to CLOCK_PORT.	None
`VDD_NETS`	List[str]?	Specifies the power nets/pins to be used when creating the power grid for the design.	None
`GND_NETS`	List[str]?	Specifies the ground nets/pins to be used when creating the power grid for the design.	None
`DIE_AREA`	Tuple[Decimal, Decimal, Decimal, Decimal]?	Specific die area to be used in floorplanning. Specified as a 4-corner rectangle "x0 y0 x1 y1".	None
`EXTRA_EXCLUDED_CELLS`	List[str]?	Wildcards matching additional cells to exclude from both synthesis and PnR.	None
`MACROS`	Dict[str, Macro]?	A dictionary of Macro definition objects. See `openlane.config.Macro` for more info.	None
`EXTRA_LEFS`	List[Path]?	Specifies miscellane files to be indiscriminately	None

Variable Name	Type	Description	
		whenever LEFs are loaded.	
`EXTRA_VERILOG_MODELS`	List[Path]?	Specifies miscellaneous Verilog models to be loaded indiscriminately during synthesis.	`None`
`EXTRA_SPICE_MODELS`	List[Path]?	Specifies miscellaneous SPICE models to be loaded indiscriminately whenever SPICE models are loaded.	`None`
`EXTRA_LIBS`	List[Path]?	Specifies LIB files of pre-hardened macros used in the current design, used during timing analyses (and during parasitics-based STA as a fallback). These are loaded indiscriminately for all timing corners.	`None`
`EXTRA_GDS_FILES`	List[Path]?	Specifies GDS files of pre-hardened macros used in the current design, used during tape-out.	`None`
`FALLBACK_SDC_FILE`	Path	A fallback SDC file for when a step-specific SDC file is not defined.	`/home/docs/che`