Standard Cells in ASIC Design | Standard Cells in VLSI

May 18, 2020 by Team VLSI

Standard cells are well defined and pre-characterized cells used in ASIC (Application Specific Integrated Circuit) Design flow as basic building blocks. All these cells are equal in height and can easily fit into the standard cell row. Standards cells are highly reusable and save lots of ASIC design time.

Standard Cell Layout

All the Standard cells are in equal in

characteristics of a standard cell have been explained with the help of the following figure.

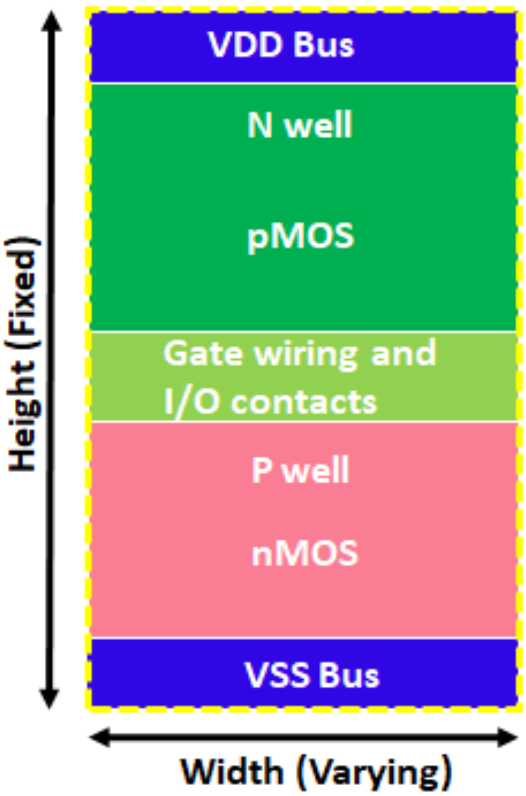

Figure-1: Standard Cell layout style

At the top of the standard cell, there is VDD rail and bottom there is a VSS rail. Both the Power rails are drawn in the Metal-1 layer. In between the VDD rail and VSS rail there are three main regions, a nwell region, a gap of nwell and pwell and pwell region. nwell region is near to the VDD rail and pwell region is near the VSS rail. pMOS transistors are build inside the nwell, so all the pMOS transistors are in the top half of the cell and similarly, all nMOS are in the bottom half of the

Layout of a schematic can be drawn in various ways. For example layout of a NAND gate can be drawn in following two different styles.

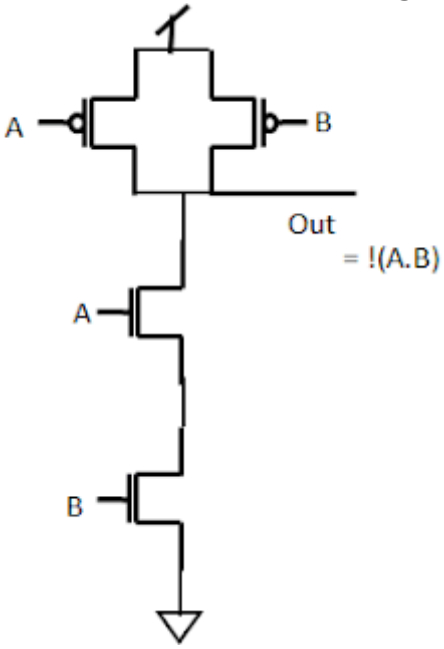

Figure-2: Schematic of a NAND gate

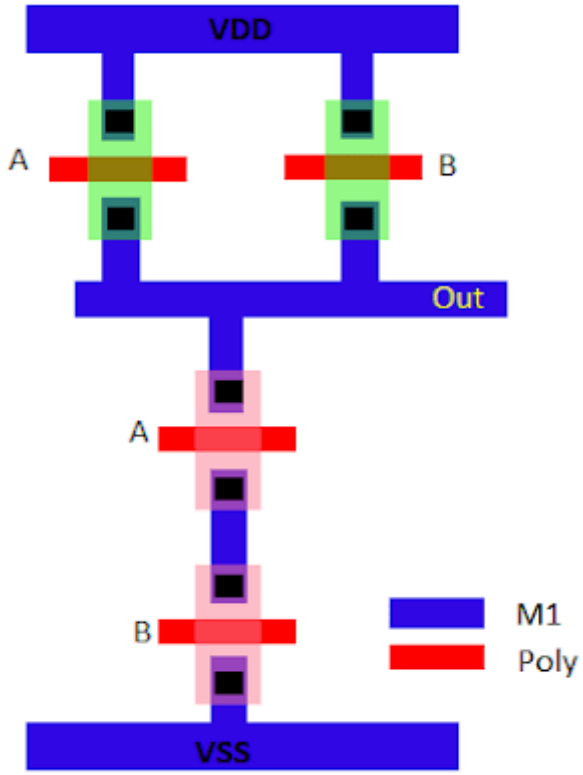

Figure-3: Layout of a NAND gate

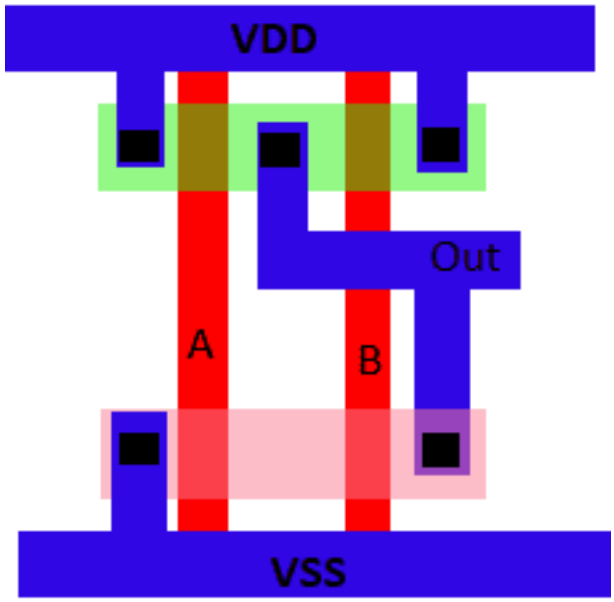

Figure-4: Layout of a NAND gate

Figure-2 is showing the schematic of a NAND gate and figure-3 and figure-4 showing two different layouts of the schematic shown in the figure. In figure 3 both the nMOS are in not the same level, they are stacked but in the layout of figure 4 all nMOS are in one level and all pMOS are at one level. And in figure-3 gates are drawn horizontal and not common in nMOS and pMOS. But in figure-4, all the poly gates are drawn vertical and common to nMOS and pMOS both.

There are many reasons f0r preferring a layout style like in figure-4. Some of them are:

1. Save Design Area: Both the nwell and pwell are in the same level for all the standard cell, so they can easily abut and make a common well which saves lots of areas.

Place and Route) to place them. They also have power rails in the same location for all the standard cells, so power rails can also be abutted easily.

3. Easy to route: All the pins of standard cells are in the intersection of horizontal and vertical tracks, So it becomes easy to route them by the APR tool

Tracks in standard cells:

Track can be defined as a line on which metal layers are drawn. A track means one M1 Pitch. Height of Standard cell is generally measured in term of no. of tracks inside it. like a 6T standard cell means that the height of the standard cell is 6 Track of M1. An example of 13T standard cell is given below in figure-5.

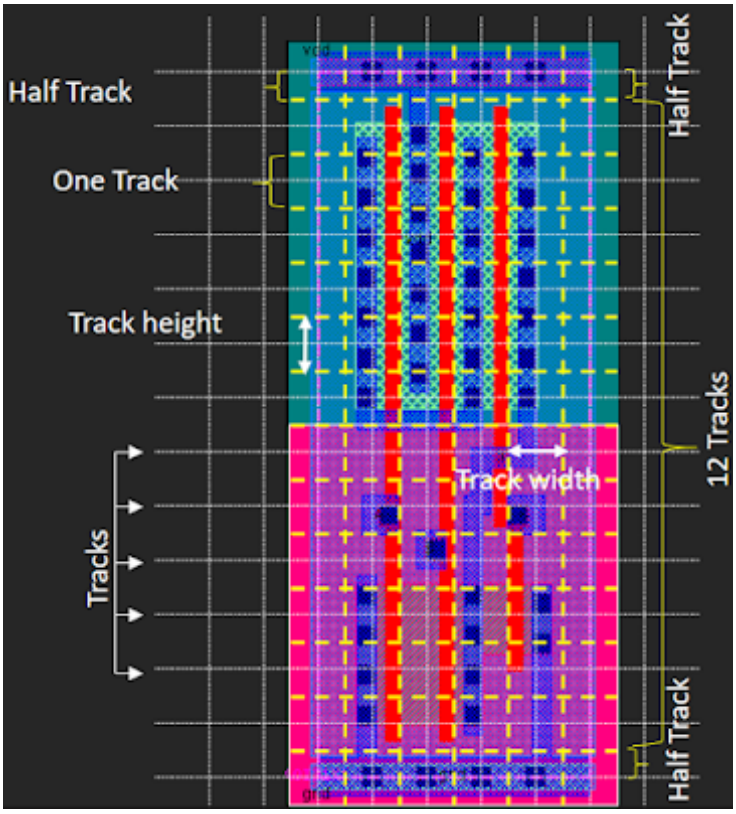

Figure-5: A 13T height standard cell

In the above example, the height of one track is

Various heights standard cell library:

Generally, there are various sets of standard cell library having different track size of standard cells. Depending on the use of ASIC, track height a standard library has selected. There are generally three sets of standard cell library characterized as small transistor standard cell, large transistors standard cell and medium transistor standard cell. An example for 6T, 12T and 9T size standard cells are shown below.

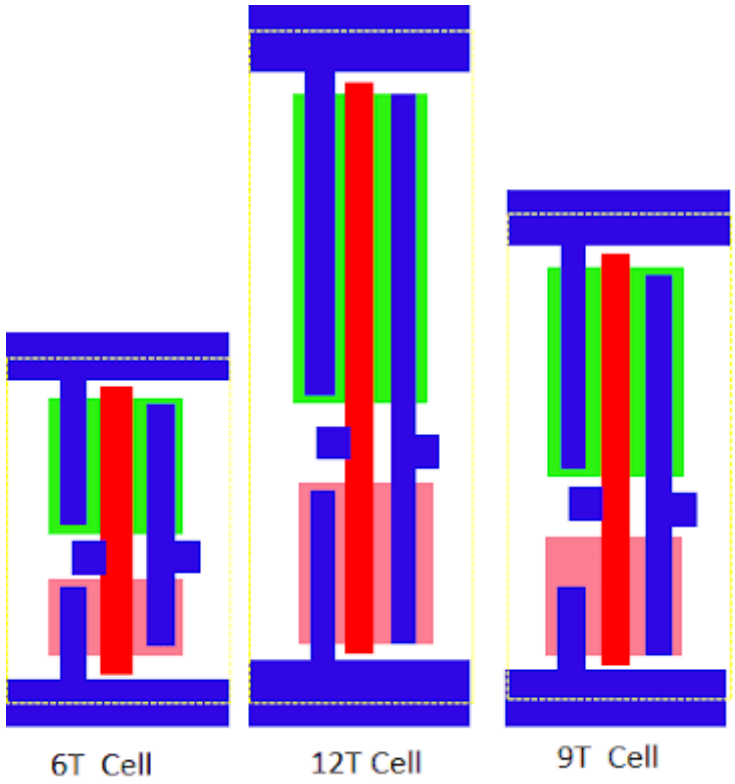

Figure-6: Various height's of standard cell

Small transistor standard cells are used for high-

area but having very good performance. Medium transistors standard cells have a balance between large transistors and small transistors. So there is a tradeoff between area/power vs performance. A comparison has been shown below in figure-7.

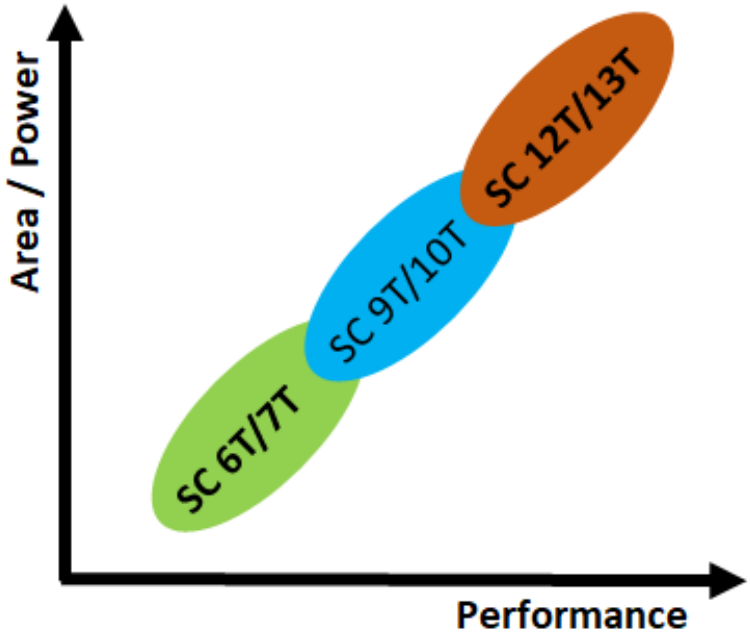

Figure-7: Tradeoff between performance and area for various heights standard cell

Various applications of these cells are as bellow.

- Small transistor cells (6T Cells)
  - Minimum area and low power
  - Mobile applications
  - Ultra-low-power applications
  - Embedded microcontroller

- Large transistors cells (12T Cells)
  - Large area

- Medium transistors cells (9T Cells)
    - Balance area and performance
    - General Computing
    - GPU
    - General-purpose circuit

Thank you!

standard cell, Standard cell layout, Standard Cell Library

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2 thoughts on “Standard Cells in ASIC Design | Standard Cells in VLSI”

vamosabv

November 1, 2021 at 5:46 am

Thanks a lot for publishing this post!

Pankaj

May 26, 2022 at 1:02 pm

How to choose VDD/VSS rail width for any track configuration.

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