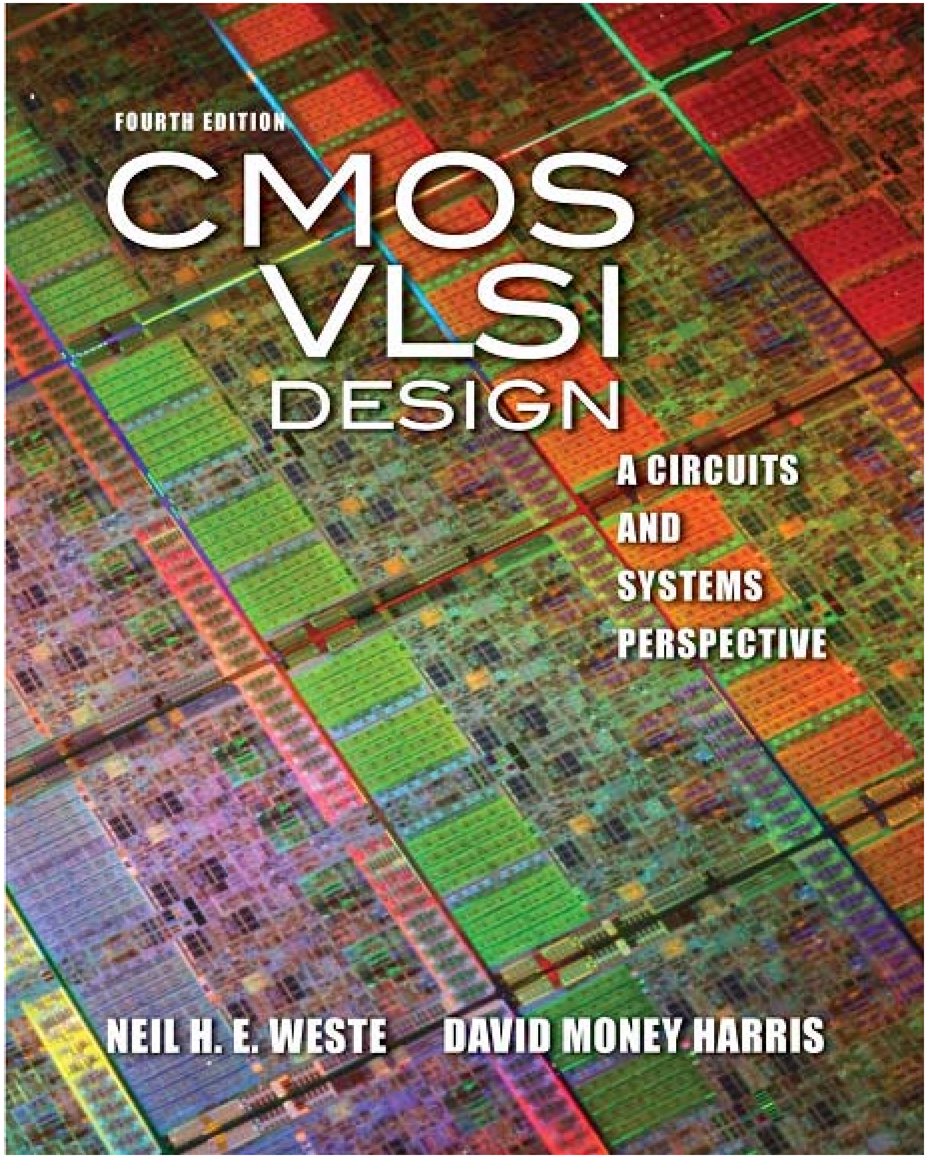


Lecture 22: I/O

Outline

- Basic I/O Pads
- I/O Channels
  - Transmission Lines
  - Noise and Interference
- High-Speed I/O
  - Transmitters
  - Receivers
- Clock Recovery
  - Source-Synchronous
  - Mesochronous

Input / Output

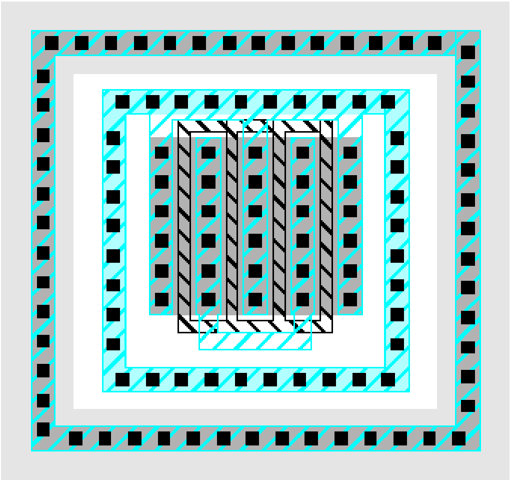
- Input/Output System functions
  - Communicate between chip and external world
  - Drive large capacitance off chip
  - Operate at compatible voltage levels
  - Provide adequate bandwidth
  - Limit slew rates to control di/dt noise
  - Protect chip against electrostatic discharge
  - Use small number of pins (low cost)

I/O Pad Design

- Pad types
  - V_{DD} / GND
  - Output
  - Input
  - Bidirectional
  - Analog

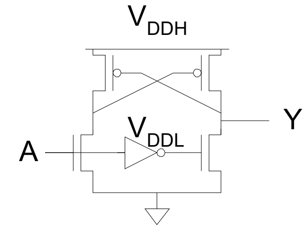
Output Pads

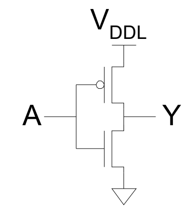
- Drive large off-chip loads (2 – 50 pF)
  - With suitable rise/fall times
  - Requires chain of successively larger buffers
- Guard rings to protect against latchup
  - Noise below GND injects charge into substrate
  - Large nMOS output transistor
  - p+ inner guard ring
  - n+ outer guard ring
    - In n-well



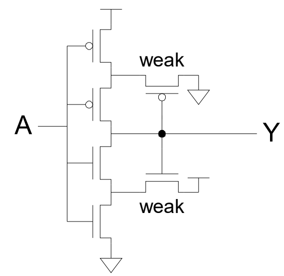
Input Pads

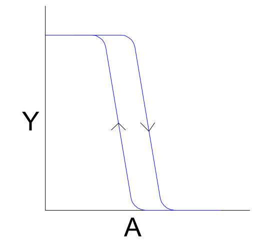
- Level conversion
  - Higher or lower off-chip V
  - May need thick oxide gates





- Noise filtering
  - Schmitt trigger
  - Hysteresis changes V_{IH}, V_{IL}

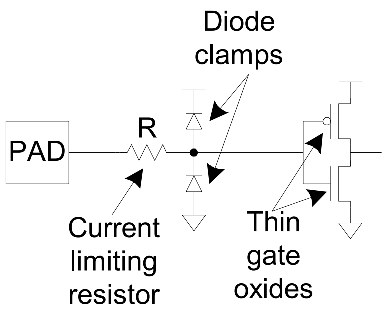




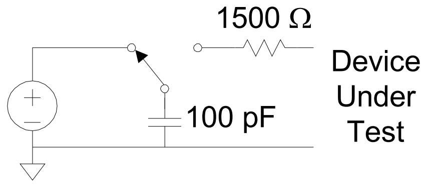
- Protection against electrostatic discharge

ESD Protection

- Static electricity builds up on your body
  - Shock delivered to a chip can fry thin gates
  - Must dissipate this energy in protection circuits before it reaches the gates
- ESD protection circuits
  - Current limiting resistor
  - Diode clamps

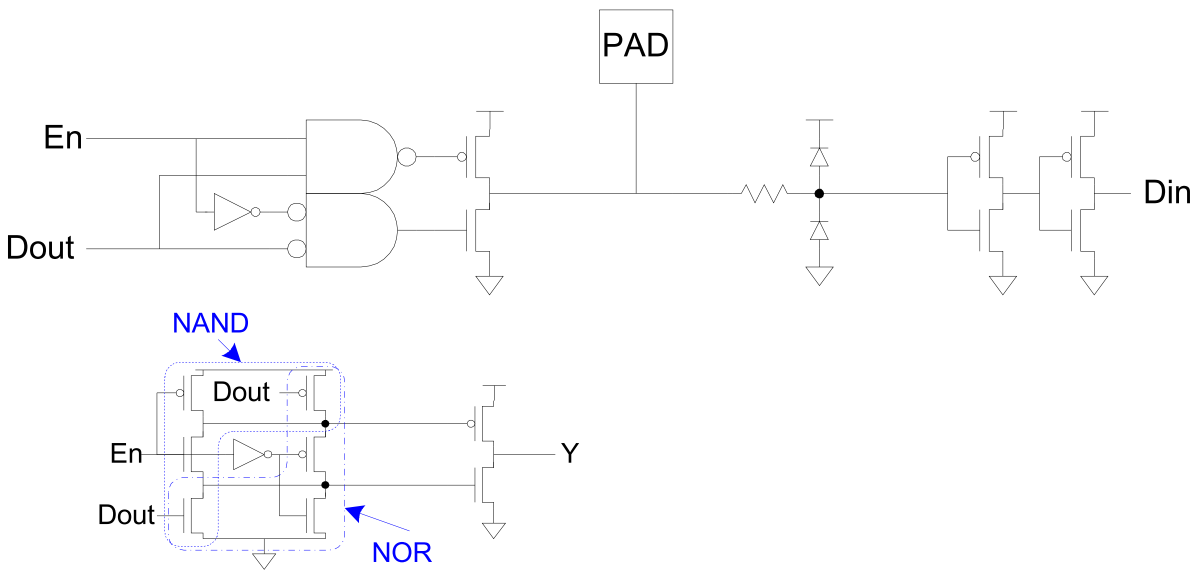


- ESD testing
  - Human body model
  - Views human as charged capacitor



Bidirectional Pads

- Combine input and output pad
- Need tristate driver on output
  - Use enable signal to set direction
  - Optimized tristate avoids huge series transistors

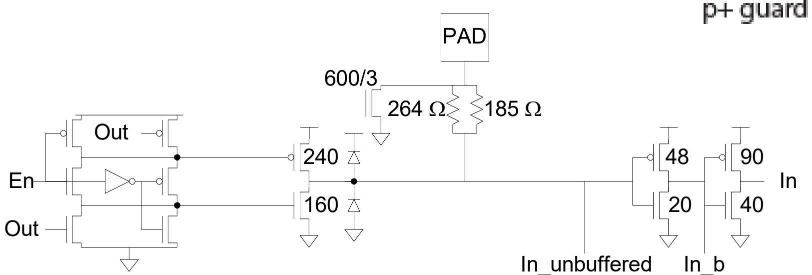


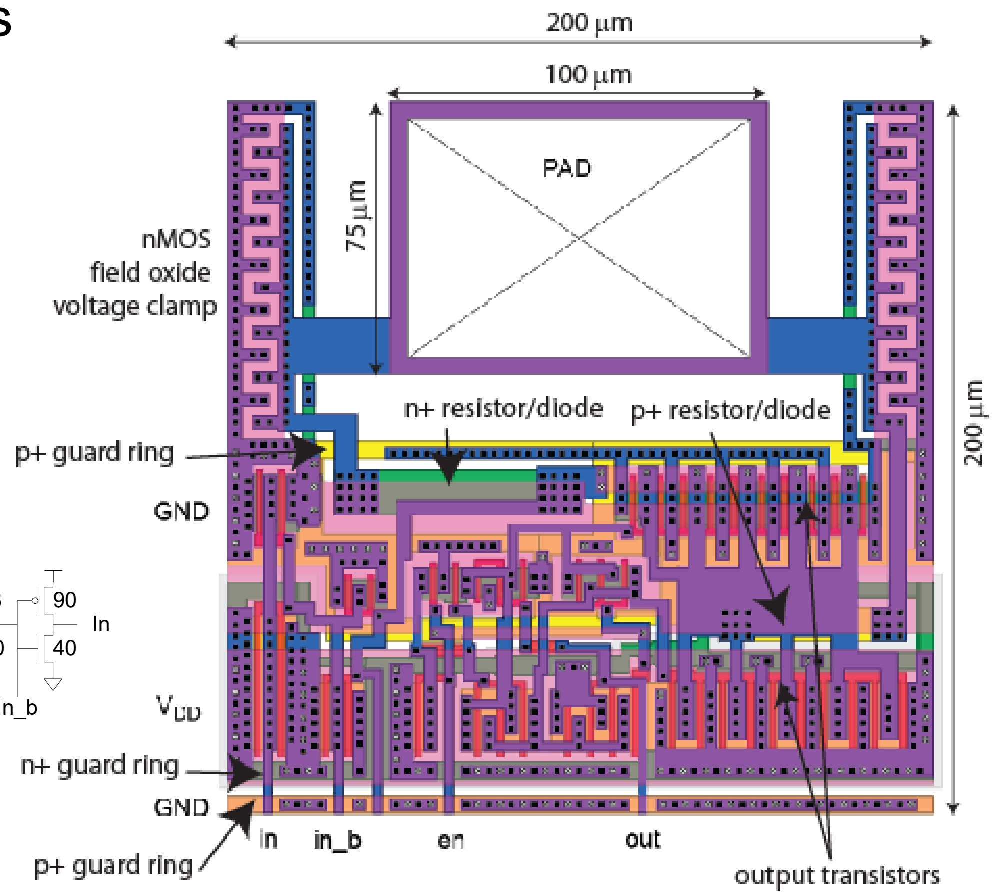
Analog Pads

- Pass analog voltages directly in or out of chip
  - No buffering
  - Protection circuits must not distort voltages

MOSIS I/O Pad

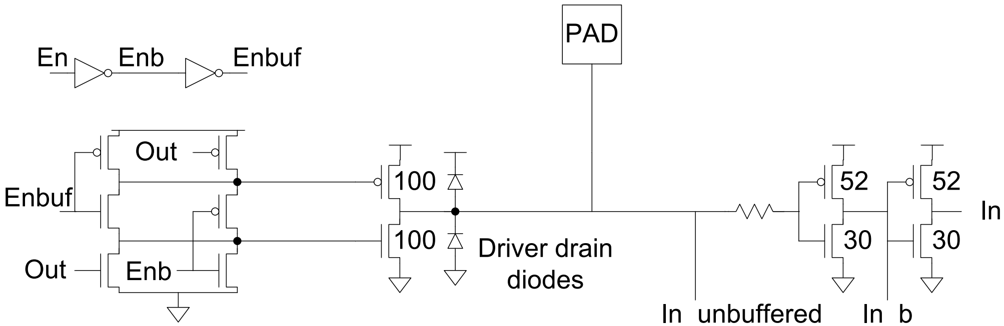
- 1.6 μm two-metal proces
  - Protection resistors
  - Protection diodes
  - Guard rings
  - Field oxide clamps

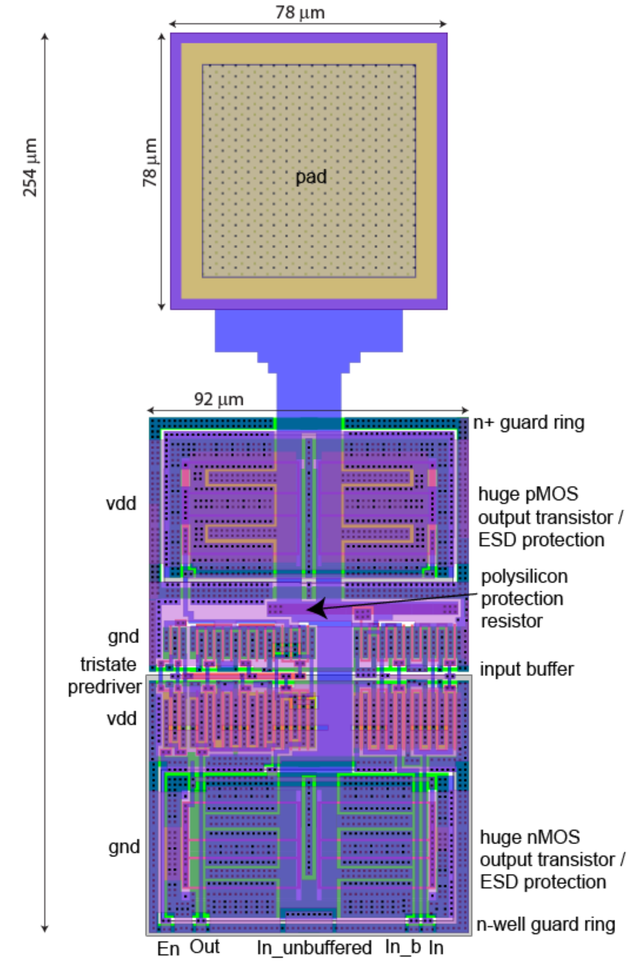




UofU I/O Pad

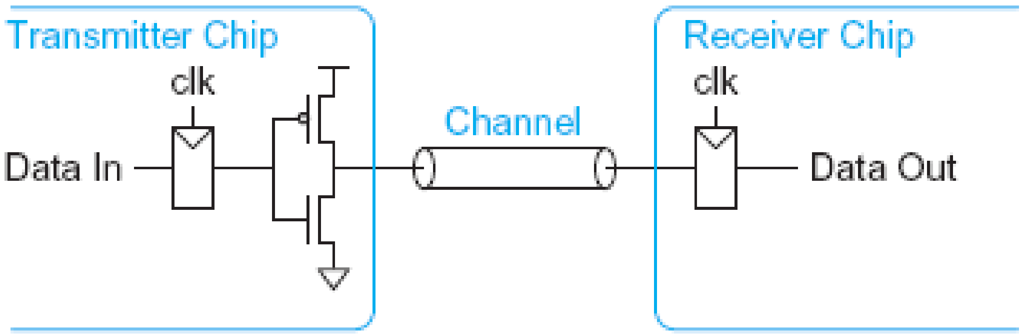
- 0.6 μm three-metal process
  - Similar I/O drivers
  - Big driver transistors provide ESD protection
  - Guard rings around driver





I/O Channels

- I/O Channel: connection between chips
  - Low frequency: ideal equipotential net
  - High frequency: transmission line
- Transmission lines model
  - Finite velocity of signal along wire
  - Characteristic impedance of wire



When is a wire a T-Line?

- When propagation delay along the wire is comparable to the edge rate of the signal propagating
- Depends on
  - Length
  - Speed of light in the medium
  - Edge rate

Example

- When must a 10 cm trace on a PCB be treated as a transmission line
  - FR4 epoxy has k = 4.35 ($\varepsilon = k\varepsilon_0$)
  - Assume rise/fall times are ¼ of cycle time
- Signal propagation velocity

$$v = \frac{c}{\sqrt{4.35}} = \frac{3\times10^{8}\ \frac{\text{m}}{\text{s}}}{2.086} = 14.4\,\frac{\text{cm}}{\text{ns}}$$

- Wire flight time

$$t = \frac{10\ \text{cm}}{14.4\ \frac{\text{cm}}{\text{ns}}} = 0.7\ \text{ns}$$

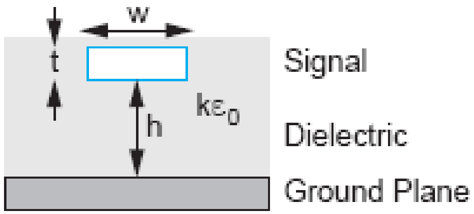
- Thus the wire should be treated as a transmission line when signals have a period < 2.8 ns (> 350 MHz)

Characteristic Impedance

- Z_0: ratio of voltage to current of a signal along the line
- Depends on the geometry of the line

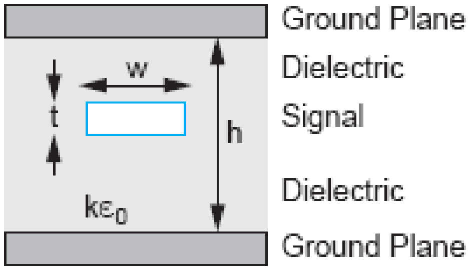
Microstrip: Outer layer of PCB

$$Z_0 = \frac{60}{\sqrt{0.457k + 0.67}} \ln \frac{4h}{0.67(0.8w + t)}$$



Stripline: Inner layer of PCB

$$Z_0 = \frac{60}{\sqrt{k}} \ln \frac{4h}{0.67\pi(0.8w + t)}$$



Example

- A 4-layer PCB contains power and ground planes on the inner layers and signals on the outer layers. The board uses 1 oz copper (1.4 mils thick) and the FR4 dielectric is 8.7 mils thick. How wide should the traces be to achieve 50 Ω characteristic impedance?
- This is a microstrip design. Solve for w with
  - $t = 1.4$ mils
  - $h = 8.7$ mils
  - $k = 4.35$
  - $Z_0 = 50\ \Omega$

$$Z_0 = \frac{60}{\sqrt{0.457k + 0.67}} \ln \frac{4h}{0.67\left(0.8w + t\right)}$$

- $w = 15$ mils

Reflections

- When a wave hits the end of a transmission line, part of the energy will reflect if the load impedance does not match the characteristic impedance.

- Reflection coefficient: $\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0}$

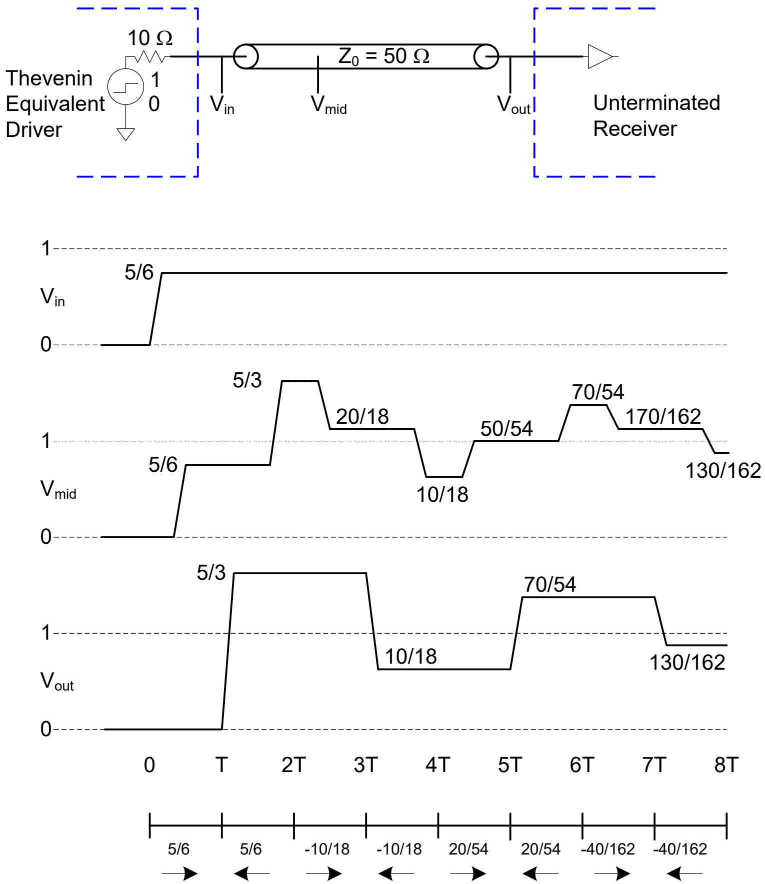
- A wave with an amplitude of $V_{reflected} = \Gamma V_{incident}$ returns along the line.

Example: Reflections

- A strong driver with a Thevenin equivalent resistance of 10 Ω drives an unterminated transmission line with Z_0 = 50 Ω and flight time T. Plot the voltage at the 1/3 point and end of the line.
- Reflection coefficients:

$$\Gamma_S = \frac{10-50}{10+50} = -\frac{2}{3}; \; \Gamma_L = \frac{\infty - 50}{\infty + 50} = 1$$

- Initial wave: 50/(10+50) = 5/6
- Observe ringing at load



Intersymbol Interference

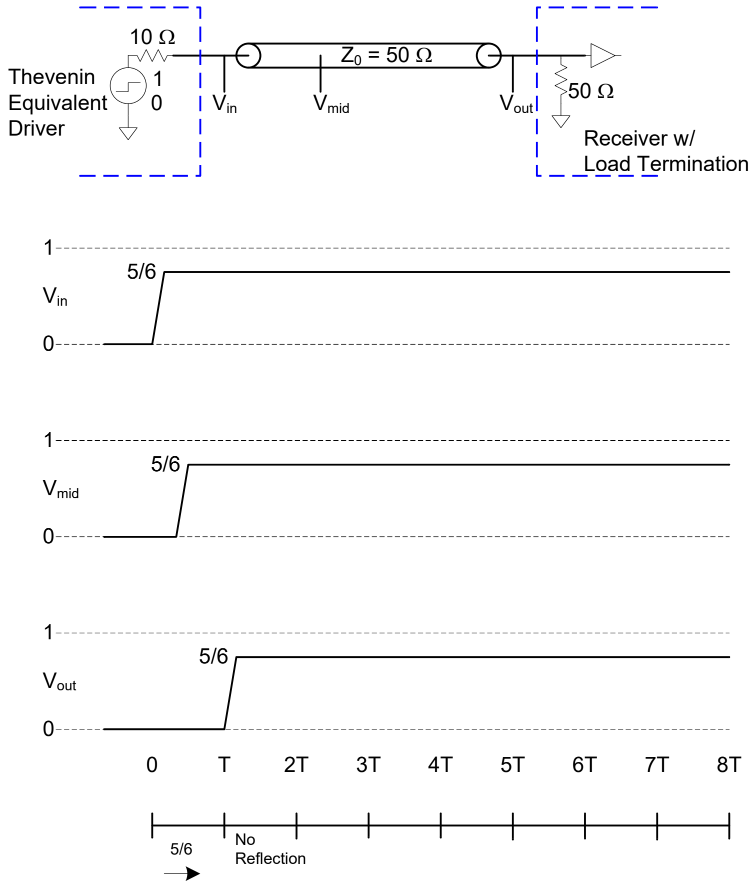
- Must wait until reflections damp out before sending next bit
- Otherwise, *intersymbol interference* will occur
- With an unterminated transmission line, minimum bit time is equal to several round trips along the line

Example: Load Termination

- Redo the previous example if the load is terminated with a 50 Ω resistor.
- Reflection coefficients:

$$\Gamma_S = \frac{10-50}{10+50} = -\frac{2}{3};\ \Gamma_L = \frac{50-50}{50+50} = 0$$

- Initial wave: 50/(10+50) = 5/6
- No ringing
- Power dissipation in load resistor

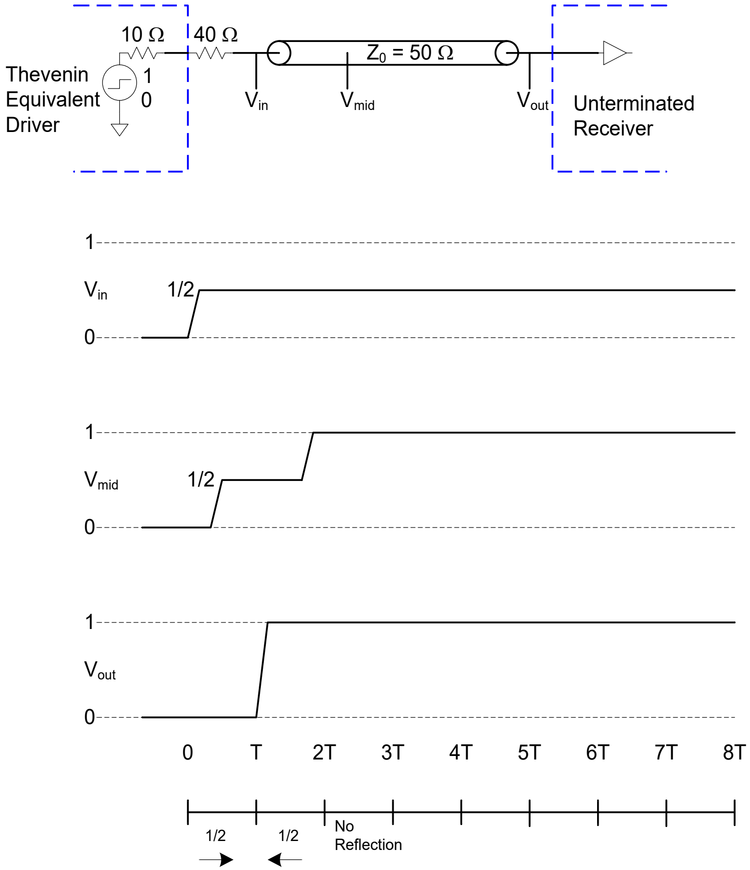


Example: Source Termination

- Redo the previous example if the source is terminated with an extra 40 Ω resistor.
- Reflection coefficients:

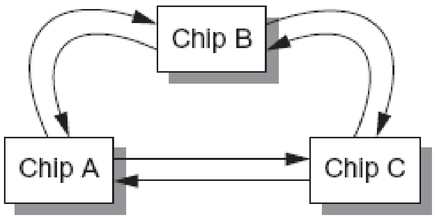
$$\Gamma_S = \frac{50-50}{50+50} = 0; \ \Gamma_L = \frac{\infty-50}{\infty+50} = 1$$

- Initial wave: 50/(50+50) = 1/2
- No ringing
- No power dissipation in load
- Taps along T-line momentarily see invalid levels

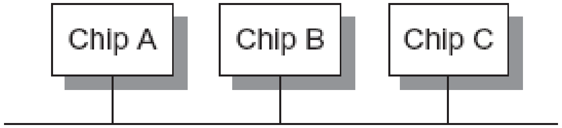


Termination Summary

- For point-to-point links, source terminate to save power



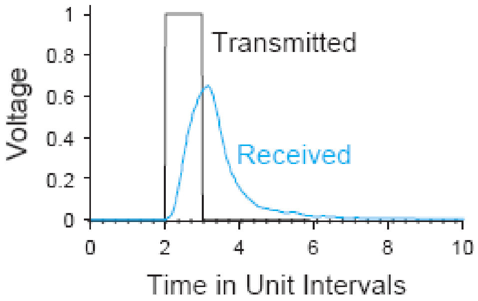
- For multidrop busses, load terminate to ensure valid logic levels

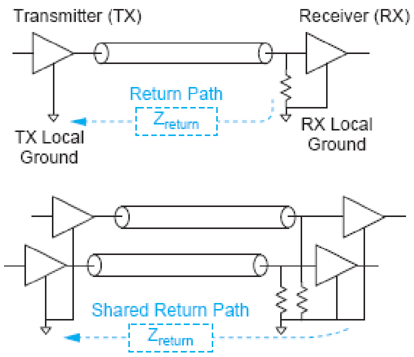


- For busses with multiple receivers and drivers, terminate at both ends of the line to prevent reflections from either end

Noise and Interference

- Other sources of intersymbol interference:
  - Dispersion
    - Caused by nonzero line resistance
  - Crosstalk
    - Capacitive or inductive coupling between channels
  - Ground Bounce
    - Nonzero return path impedance
  - Simultaneous Switching Noise





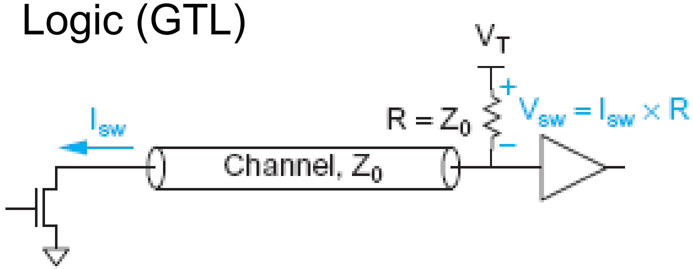
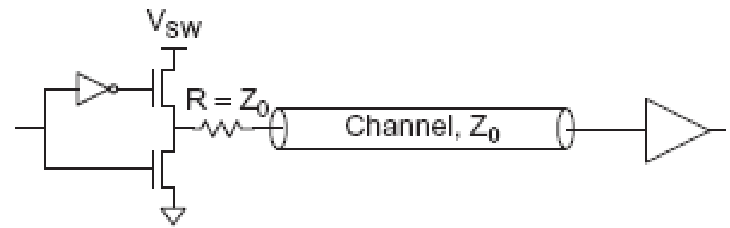
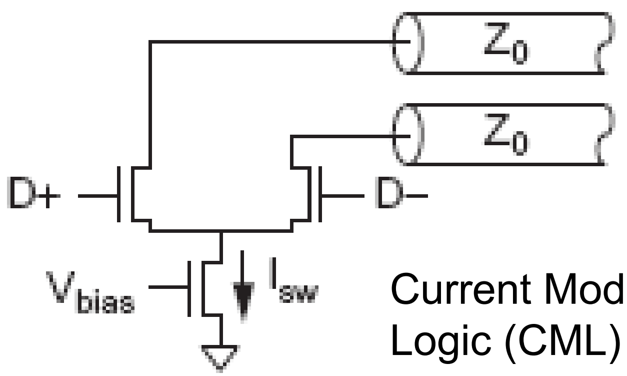
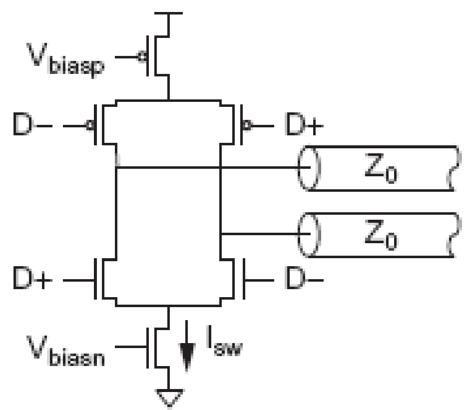
High-Speed I/O

- Transmit data faster than the flight time along the line
- Transmitters must generate very short pulses
- Receivers must be accurately synchronized to detect the pulses

High Speed Transmitters

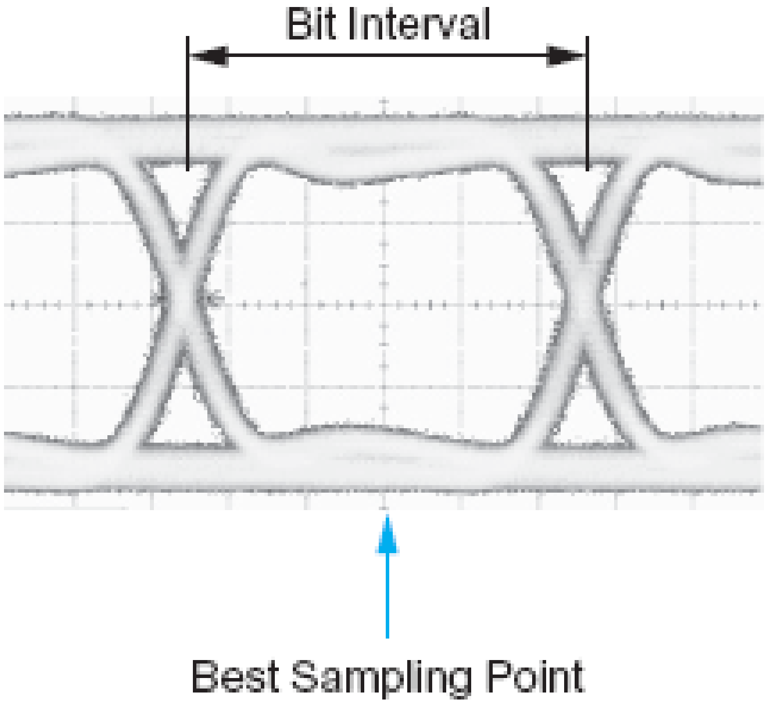
- How to handle termination?
  - High impedance current-mode driver + load term?
  - Or low-impedance driver + source termination
- Single-ended vs. differential
  - Single-ended uses half the wires
  - Differential is Immune to common mode noise
- Pull-only vs. Push-Pull
  - Pull-only has half the transistors
  - Push-pull uses less power for the same swing

High-Speed Transmitters

	Pull-Only	Push-Pull
Single-Ended	Gunning Transceiver Logic (GTL)  	
Differential	 Current Mode Logic (CML)	 Low-Voltage Differential Signalling (LVDS)

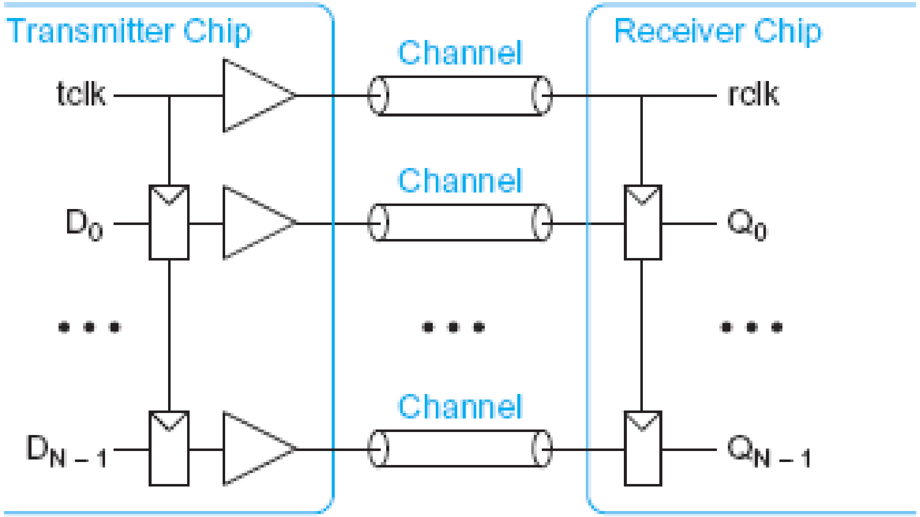
High-Speed Receivers

- Sample data in the middle of the bit interval
- How do we know when?



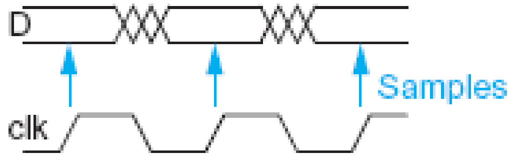
Source-Synchronous Clocking

- Send clock with the data
- Flight times roughly match each other
  - Transmit on falling edge of tclk
  - Receive on rising edge of rclk

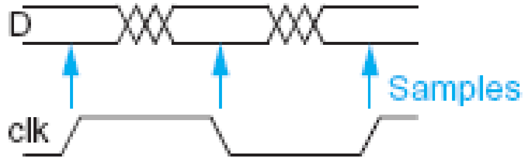


Single vs. Double Data Rate

- In ordinary single data rate (SDR) system, clock switches twice as often as the data

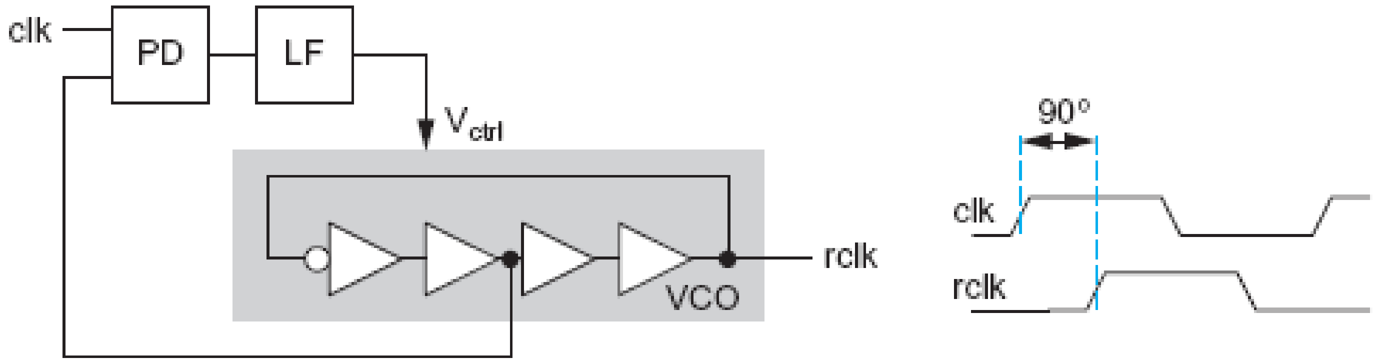


- If the system can handle this speed clock, the data is running at half the available bandwidth
- In double-data-rate (DDR) transmit and receive on both edges of the clock



Phase Alignment

- If the DDR clock is aligned to the transmitted clock, it must be shifted by 90º before sampling
- Use PLL



Mesochronous Clocking

- As speeds increase, it is difficult to keep clock and data aligned
  - Mismatches in trace lengths
  - Mismatches in propagation speeds
  - Different in clock vs. data drivers
- Mesochronous: clock and data have same frequency but unknown phase
  - Use PLL/DLL to realign clock to each data channel

Phase Calibration Loop

- Special phase detector compares clock & data phase