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Impact of Complex-Logic Cell Layout on the Single-Event Transient Sensitivity

Y. Q. Aguiar, F. Wrobel, J-L. Autran, P. Leroux, F. Saigné, A. D. Touboul and V. Pouget

***Abstract*—The design methodology based on standard cells is widely used in a broad range of VLSI applications. Further, several optimization algorithms can be employed to address different constraints such as power consumption or reliability. This work evaluates the implications of the usage of complex-logic cells from a 45 nm Standard-Cell library to the Single-Event Transient sensitivity under heavy ions. Results show that even though a reduction in the layout area is obtained when adopting complex-logic gates, a slight reduction in the total sensitive area of the circuit is observed. Moreover, the effectiveness of logical masking can be suppressed, leading to a higher SET cross-section for high particle LET.**

***Index Terms*— Complex-logic gate, Heavy ions, Logical Masking, Monte Carlo simulation, Single-Event Transient**

I. Introduction

THE constant scaling process of transistors has provided great achievements in terms of computational power. The design abstraction provided in a cell-based methodology for the design of Application-Specific Integrated Circuits (ASICs) enabled the development of highly integrated and complex devices, so-called Very-Large-Scale Integration (VLSI) systems. In this methodology, a Standard-Cell library containing thousands of pre-designed and characterized logic gates is used in the logic synthesis of the circuit design [1]. However, as devices are reaching the nanometer scale, reliability issues are exacerbated such as increased soft error rates and pronounced Short-Channel Effects (SCEs) [2, 3]. For instance, dedicated effort towards the reduction of the increased static power dissipation due to excessive leakage currents induced by SCEs is vastly investigated [4, 5]. Additionally, the effectiveness of soft error mitigation techniques is reduced due to multi-node charge collection and multiple bit upsets [6-9]. Apart from the dedicated leakage current mitigation schemes, the reduction of the number of transistors can be an effective way to improve the reliability and power consumption of VLSI designs at advanced technology nodes. By reducing the transistor count for a given circuit, the number of connections is also reduced leading to relaxed cell routing and improved reliability regarding physical manufacture failures [10]. Although the advantages of reducing the transistor count in a VLSI design is well-known, the impact to radiation sensitivity has not been widely analyzed yet. Denser layouts and the reduced number of transistors can be achieved by using complex-logic CMOS gates [10, 11]. Most of the works in the literature have focused only on the study of radiation effects in basic logic cells such as NAND, NOR and INV gates. Given the significance of charge sharing due to the multi-node collection at deeply scaled technologies, it is imperative to study the Single-Event Transient (SET) sensitivity of complex-logic gates at digital circuits. Therefore, this work aims to evaluate the impact of using complex gates from a Standard Cell library to the radiation reliability of VLSI designs. A Monte Carlo predictive tool named MC-Oracle is used for the particle interaction simulations considering the critical volumes extracted from the layout designs. At circuit level, a SET analyzer based on electrical simulations is used to evaluate the design SET cross-section.

This paper is organized as follows: Section II presents the complex-logic CMOS gate designs and the state-of-the-art concerning SET analysis of standard cells; the sensitivity analysis methodology is described in Section III; the results and discussions are provided in Section IV; and, Section V summarizes and concludes this paper.

II. Complex-Logic CMOS Gates

Different from the full custom layout design approach, Standard-Cell based methodology can improve the design implementation time with a fair reduction in performance and area [1]. However, during the logic synthesis, a given Boolean function can be implemented in many different combinations of logic cells, resulting in a different number of transistors and layout designs which directly impact the radiation robustness of the circuit. Accordingly, a Standard-Cell library contains multiple implementations of the same logic function, differing in area, performance and reliability [10]. The variety provided by the cell library can be used to accomplish different optimization constraints, for instance, targeting radiation robustness.

The usage of complex logic gates commonly available at cell libraries, such as the And-Or-Inverter (AOI) and Or-And-

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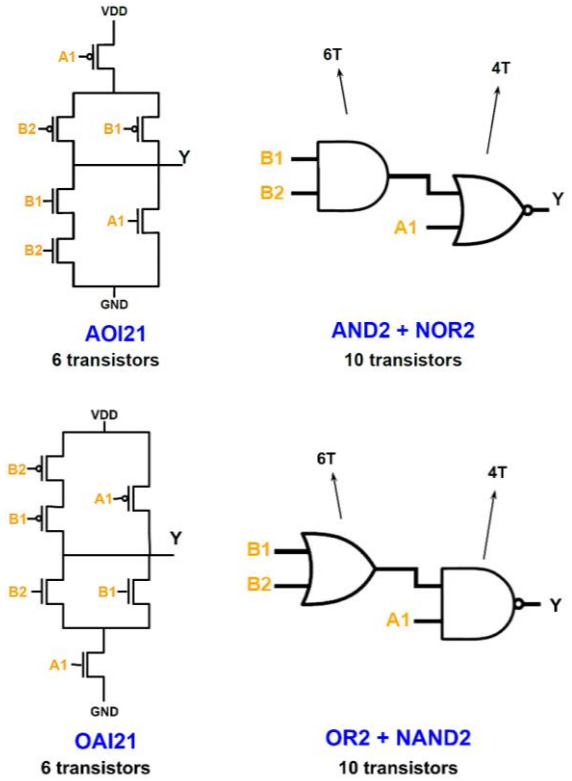

Fig. 1. CMOS transistor structure of the complex-logic gate AOI21 and OAI21 and its correspondent implementation with the gates: AND2, NOR2, OR2 and NAND2.

Inverter (OAI) cells, reduces the number of transistors and provides denser layouts reducing power consumption and area [10]. For example, the Boolean logic function given in Eq. 1 can be implemented by using basic logic standard cells as NAND, NOR and INV or by using the complex-gate AOI directly.

$$Y = \neg(A1 \wedge (B1 \vee B2)) \quad (1)$$

As shown in Fig. 1, the AOI21 implementation of Eq.1 contains 40% of reduction in the transistor count compared with the implementation using an AND2 gate coupled with a NOR2 gate. The same result can be obtained for the OAI21 gate. Clearly, the power consumption for the complex-logic gates are also reduced, but the sensitivity to radiation is not straightforward to be predicted in advance. In [11], an optimizing synthesis methodology is proposed to reduce the transistor count of circuits. The proposed methodology is called Gate Clustering and consists in the agglutination of basic logic gates into static CMOS complex gates (SCCG) [11]. As expected, the authors confirm that the reduced number of transistor improves the power consumption and layout area. Further, the circuit performance is also improved due to the reduction of the circuit wirelength which is the main source of delay at advanced technology nodes [12, 13]. Due to complex SET dependencies, as the node capacitance, charge sharing, pulse quenching and particle energy, the radiation sensitivity of these implementations must be analyzed at layout level. For instance, the charge sharing induced by the multi-node charge collection in deeply scaled CMOS transistors can improve the radiation robustness by reducing the SET cross-section and the transient pulse width due to the Pulse Quenching Effect [14]. However, it can also worsen the design reliability by inducing multiple SET and limiting the effectiveness of hardware techniques based on redundancy or even invalidating hardening schemes such as conventional Error Correcting Codes (ECCs) for memory elements [8].

In the literature, most of the studies generally concentrate to analyze basic CMOS logic combinatorial functions such as NAND, NOR or INV. A comparative analysis of NAND and NOR gates in bulk FinFET devices can be found in [15]. Different drive strength and supply voltages were used to investigate the SET sensitivity of these circuits. As expected, the increase of the drive strength or the supply voltage can shorten the SET pulse width, but with a penalty in the power consumption [15]. Radiation analysis of majority voter circuits designs based on NAND and NOR gates at 7nm bulk FinFET technology is provided in [16] for atmospheric constraints. Due to the high regularity of the cell layouts and the symmetric sizing of PFET/NFET devices provided by the technology, a similar drain area and restoring drive currents are obtained, leading to similar radiation robustness [16].

In [17], experimental results for NAND, NOR and INV logic gates in 90nm are provided for protons and heavy ion irradiation. Also, distinct SET robustness was observed for each gate due to the different drain sensitive areas and topology of the circuits [17]. However, the SET characterization in cell-based designs requires not only the analysis of these basic logic structures as shown in [18]. In terms of combinational cell SER, D. Alexandescu et al. provided an analysis of the SET contribution of 45nm CMOS standard cells to the overall SER of a multiplier circuit [18].

III. Methodology

This work aims to investigate the SET sensitivity of denser layouts provided by complex-logic cells in a Standard-Cell library. For this reason, the circuit implementations of Fig. 1 are considered by using 45-nm standard cells [19] and submitted to a Monte Carlo predictive tool. The complex logic gates AOI21 and OAI21 are compared with the radiation performance of its correspondent implementation based only on basic logic gates such as AND, OR, NAND and NOR. The simplified cell layout design of the gates is provided in Fig. 2, which only the metal1, active diffusion and poly layers are shown for clarity. Considering the gate sizing, it is adopted the minimum cell strength available in the library for all analyzed logic cells. Therefore, the suffix X1 is suppressed in the text. The cell height is defined to 1.57µm [19] and for the implementation of the AND+NOR and OR+NAND circuits, the standard cells were placed within the minimum distance.

The proposed predictive simulation chain is divided into two steps: first, the particle interaction simulation; second, the electrical simulation to account for the circuit response effects. A simplified diagram in Fig. 3 illustrates the SET prediction methodology adopted in this work. For the first step, the MC-Oracle, a predictive tool based on Monte Carlo simulations, is adopted to calculate the transient currents generated from the particle interaction within the devices [20, 21]. Besides the radiation environment specification, the tool requires the layout information contained in the GDS (Graphical Design System)

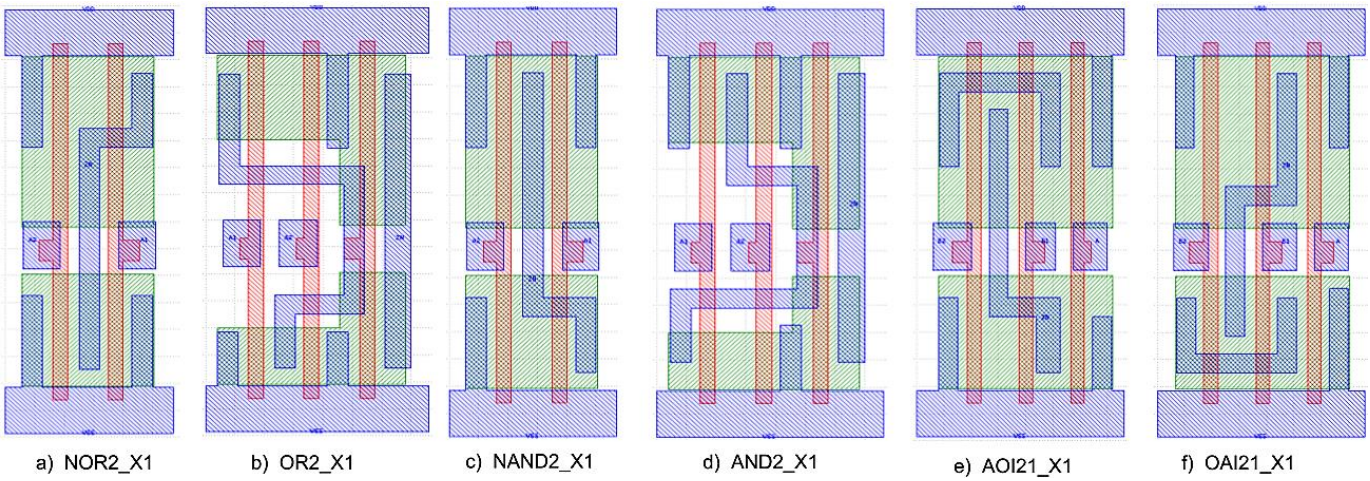

Fig. 2. Simplified cell layout design of logic gates from the 45-nm bulk CMOS [19] containing metal1, active diffusion and poly layers.

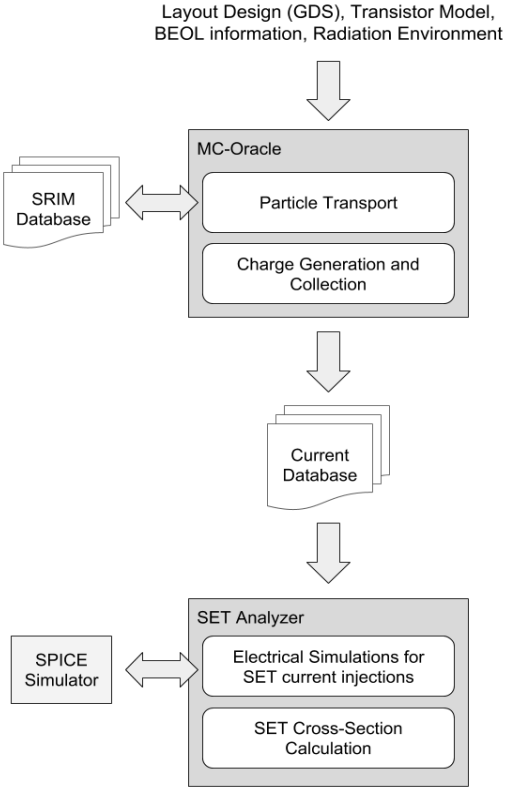

Fig. 3. Simplified diagram of the SET prediction methodology considering heavy ions.

format file, so the geometric structures of the sensitive volumes composed of the drain junctions can be extracted directly from the circuit design. Considering heavy ions simulations, several thousands of impinging particles are simulated for a given Linear Energy Transfer (LET). The LET is a measure of the average ionization energy deposited by a particle per unit distance traveled in the device. For each particle, the energy deposition, charge generation and collection are calculated for each collecting drain electrode of the circuit. The parameters that describe the radiation-induced transient current are stored in a database to be used by the SET Analyzer.

In the second step, the SET Analyzer performs the injection of the transient currents from the SET database generated by MC-Oracle through SPICE simulations considering the post-layout parasitic extraction netlist of the design implementations. The SET current injections consider the multiple node collection and the influence of the input signal of the circuit, i.e. different input signals provide different collection area patterns due to the different sensitive nodes [22]. Thus, the charge sharing effect is taken into consideration in this approach. The proposed simulation chain is able to consider the radiation response from the particle interaction physics to the electrical circuit effect in order to accurately predict the radiation sensitivity of digital circuits. For all the electrical simulations, an inverter was coupled to the output of the analyzed circuit, in which the SET pulse was measured, i.e. all circuits were driving a fan-out 1 (FO1). The calculation of the SET cross-section σ_{SET} follows the Eq. 2 and it is only considered for transient pulses that have reached half the value of the nominal supply voltage.

$$\sigma_{SET} = \frac{N_{SET}}{\Phi} \quad (2)$$

N_{SET} corresponds to the number of SET observed in the output of the circuit and Φ is the simulated fluence of particles. The heavy ions simulated by MC-Oracle were chosen for a range from 0.84 to 78.23 MeV.cm^2/mg.

IV. Results and Discussion

A. *The complex-gate AOI21*

To understand the individual behavior of the p-type and n-type devices in this study, the simulations were divided into two groups: the P-hit simulations, for which all the PMOS devices are turned off, i.e. input vector set to (1, 1, 1); and the N-hit simulations, for which all the NMOS devices are turned off, i.e. input vector set to (0, 0, 0). For instance, in the P-hit simulations, exclusively all the P-type transistors are sensitive to SET, i.e. all observed transient pulse is generated from a particle hit over the drain region of a PMOS transistor. The information of the P-hit and N-hit sensitive area can be found in Table 1 along with the value of the layout area and total sensitive collection area of each logic gate. The collection area refers to the area of the drain p-n junctions extracted from the layout circuit design and imported to the MC-Oracle tool.

Table 1
Total area for each cell layout design, total sensitive region and P-hit and N-hit sensitive area (μm²)

	Layout Area	Total Collection Area	P-hit Collection Area	N-hit Collection Area
NOR2	0.895	0.212	0.154	0.058
AND2	1.193	0.205	0.110	0.095
AOI21	1.193	0.359	0.243	0.116
AND + NOR	2.088	0.418	0.265	0.153

Notice that the complex-gate AOI21 provides a reduction of approximately 42% in the total layout area, as it was expected. However, it provides solely 14% reduction of the total sensitive area in which is responsible for the charge collection during a particle interaction into the silicon. The AND+NOR implementation has the largest collection drain area while the AND gate presents the smallest one.

The SET cross-section curves considering only P-hit interactions is shown in Fig. 4. It clearly shows that the implementation containing the basic logic cells AND+NOR provides a lower SET cross-section than the AOI21 for the entire LET range. Both circuits present the same threshold LET whereas there is a SET cross-section difference of approximately a factor of 2. The charge sharing effect and more importantly the logical masking [23] between the AND gate and NOR gate are responsible for this reduced number of observed SET in the output of the AND+NOR implementation. Any SET induced at the AND gate will be filtered by the logic of the NOR gate as observed in the truth table shown in Fig. 5. The output of the NOR gate will remain at logic zero as long as the secondary input remains at logic one. As it will be shown further in the results, this masking effect is not observed for the N-hit configuration. By analyzing the P-hit sensitive area of the two implementations presented in Table 1, both the AND+NOR and AOI21 gate present approximately the same sensitive area, a difference of only 2%. However, by analyzing the structure of the combinational logic and the electrical simulation results, the SETs observed for the AND gate are logically masked by the NOR gate, thus reducing the overall drain sensitive area to the PMOS devices issued in the NOR gate. The Fig. 6 presents the comparison between the SET cross-section of the AND+NOR implementation and the standalone NOR gate. It can be observed that the logical masking is effective by reducing the sensitivity of the circuit close to the sensitivity of the standalone NOR gate.

Considering only the N-hit interactions, the SET cross-sections are approximately the same for high LET ions as illustrated in the Fig. 7. Table 1 indicates that both circuits present very similar N-hit sensitive area. Further, there is no contribution of logical masking effect for the input signals considered. As previously shown in Table 1, the NOR gate output is determined whenever one of its input is at logic one. Then, as originally both inputs are set to logic zero, whenever a generated SET at the AND gate propagates to the NOR gate, it will be able to propagate to its output in case of not being electrically attenuated.

For ion LET lower than 5 MeV.cm²/mg, the difference in the sensitive area between the analyzed circuits becomes more evident. For instance, the complex-logic AOI21 gate has approximately 24% of reduced N-hit sensitive area and it reaches about 57.3% and 83.7% reduction on the SET cross-section for LET= 2.52 MeV.cm²/mg and LET = 1.69 MeV.cm²/mg, respectively. Moreover, the different circuit

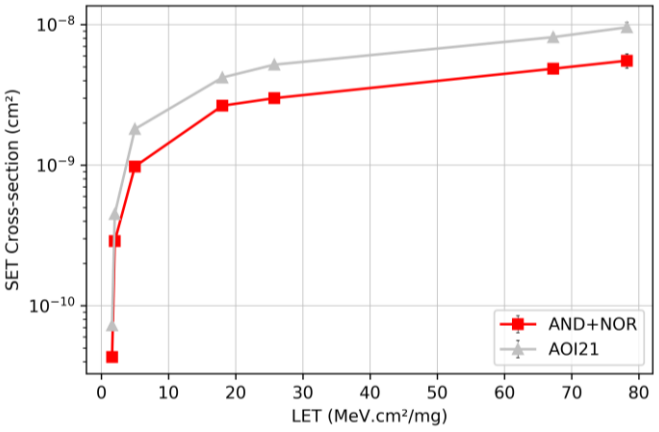

Fig. 4. SET cross-section curve of P-hit interactions for the complex-logic AOI21 gate and AND+NOR implementation.

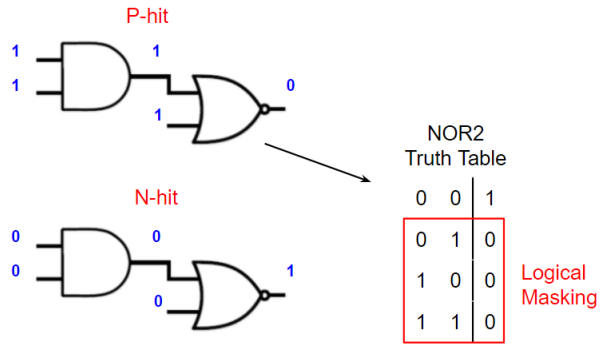

Fig. 5. Logical Masking Effect for the P-hit configuration in the combinational logic circuit AND+NOR. There is no logical masking when both inputs are set to logic zero.

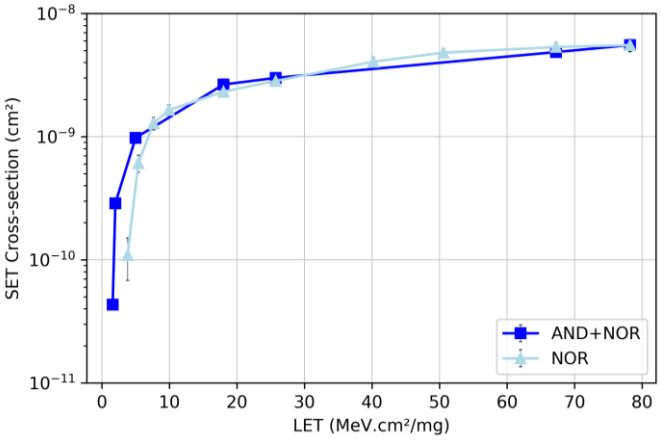

Fig. 6. Comparison of SET cross-section curve of the AND+NOR implementation and the standalone NOR gate.

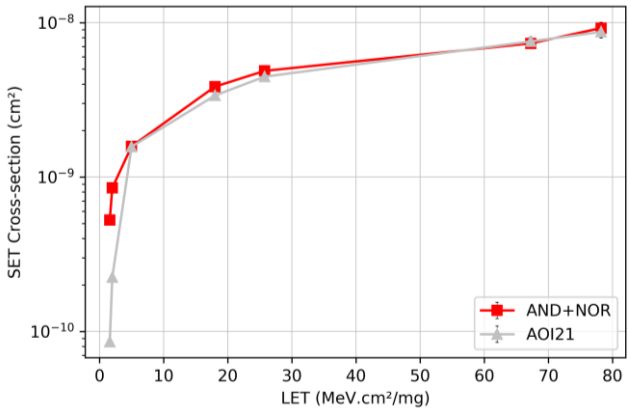

Fig. 7. SET cross-section curve of N-hit interactions for the complex-logic AOI21 agate and AND+NOR implementation.

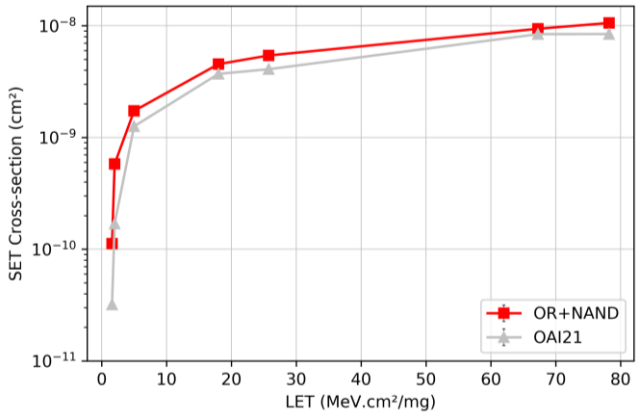

Fig. 8. SET cross-section curve of P-hit interactions for the complex-logic OAI21 gate and OR+NAND implementation.

topologies provide different transistor networks with different restoring current [15, 16]. The pull-up transistor network of AOI21 gate presents two parallel PMOS transistors. Accordingly, a higher restoring current is observed in the complex-logic gate improving the radiation performance at low LET by electrically attenuating the SET pulse.

B. The complex-gate OAI21

Similarly, the results for the complex-gate OAI21 is divided into P-hit simulations and N-hit simulations regarding the input signal of the circuits. Table 2 contains the layout area, total drain collection area and the P-hit/N-hit sensitive collection areas. Due to the regularity of the Standard-Cell designs, the OAI21 provides the same reduction in layout area provided by the AOI21 implementation, approximately 43% over the OR+NAND total layout area. Despite the considerable layout area reduction, only a reduction of 17.2% in the total collection area is obtained with the complex-logic layout. The OR+NAND circuit presents the largest layout area and collection drain area while the NAND gate has the smallest areas.

The SET cross-section curves for P-hit interactions is shown in Fig. 8 for the complex-gate OAI21 and OR+NAND circuits. Both implementations presented very similar cross-section results due to the absence of the logical masking effect for the OR+NAND under the P-hit configuration. Besides the similar SET cross-section for high LET and same threshold LET, the OR+NAND circuit shows a higher cross-section at LET = 1.6 MeV.cm^2/mg, approximately a factor of 2. This increased differences in cross-section at low LET can be explained by the

Table 2
Total area for each cell layout design, total sensitive region and P-hit and N-hit sensitive area (μm^2)

	Layout Area	Total Collection Area	P-hit Collection Area	N-hit Collection Area
NAND2	0.895	0.190	0.088	0.102
OR2	1.193	0.216	0.143	0.073
OAI21	1.193	0.336	0.176	0.160
OR + NAND	2.088	0.406	0.232	0.175

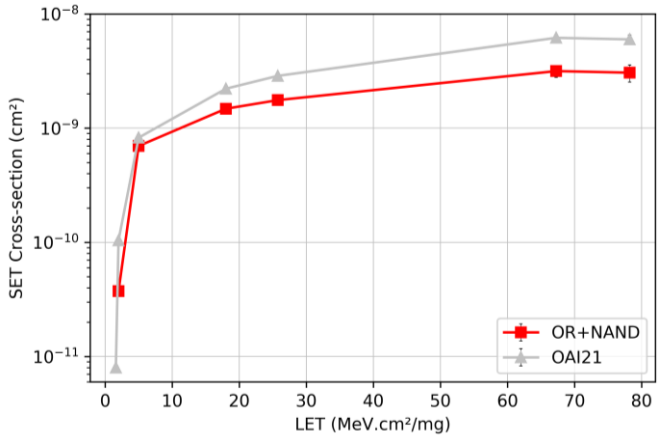

Fig. 9. SET cross-section curve of N-hit interactions for the complex-logic OAI21 agate and OR+NAND implementation.

restoring current effect. Due to the two parallel NMOS transistors in the pull-down network of the complex-gate, a higher restoring current counteracts against the radiation disturbance by shortening the transient pulses and reducing the SET cross-section compared to the estimated for the OR+NAND circuit.

Considering the N-hit simulations, the SET cross-section curves can be observed in Fig. 9. The complex-gate OAI21 presents the highest cross-section for the complete LET range with the greatest difference under high LET. In agreement to the observed for the complex-gate AOI21, the logical masking effect is also omitted from the complex-gate OAI21 which increases the SET cross-section compared to the OR+NAND structure. Even though the latter circuit structure contains a larger N-hit collection area, as shown in Table 2, due to the logical masking the effective collection area of the circuit reduces to the N-hit sensitive area of the NAND gate. Fig. 10 contains the gate-level schematic of OR+NAND circuit and the truth table for the NAND gate. The logical masking occurs at the NAND gate for N-hit configuration as long as one of its input signal is at logic zero. To confirm this observation, the cross-section for the OR+NAND and NAND gate are shown in Fig. 11 considering only the N-hit interactions. Clearly, the logical masking effect is able to reduce the sensitivity of the circuit to the sensitivity of the NAND gate when the N-hit configuration is analyzed.

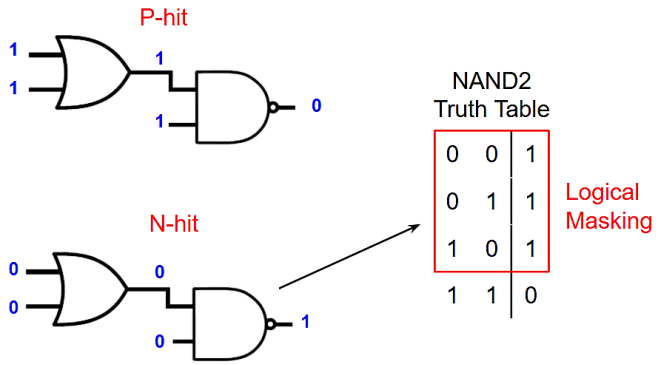

Fig. 10. Logical Masking Effect for the N-hit configuration in the combinational logic circuit OR+NAND. There is no logical masking when both inputs are set to logic one.

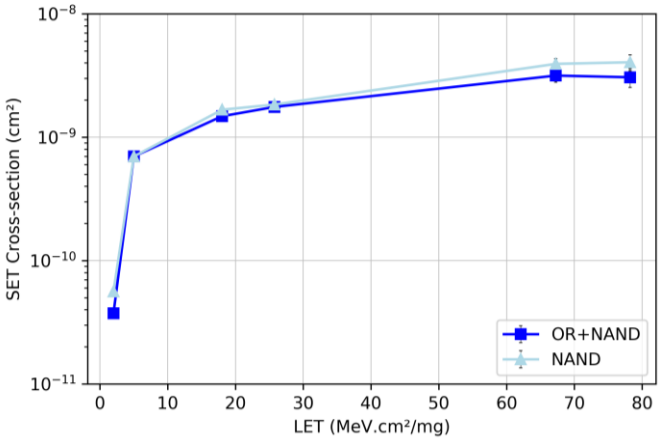

Fig. 11. Comparison of SET cross-section curve of the OR+NAND implementation and the standalone NAND gate.

C. *LET dependence and the Power Law shape*

Fig. 12 displays a comparison of the SET cross-section curves of the four circuits considering the P-hit and N-hit interaction under heavy ions of LET = 78.23 MeV.cm^2/mg, separately. The results show that the complex-logic gates present slight difference in the SET cross-section regarding the strike device which can be attributed to its symmetric topology of the pull-up and pull-down transistor networks. Unlikely, the AND+NOR and OR+NAND implementations present a difference of approximately 43% and 72%, respectively. For both complex-logic gates, the highest SET cross-sections were observed for P-hit interactions due to the reduced n-type collection volumes and the lower restoring current from the NMOS devices when compared to the PMOS devices. Due to different collection volumes and restoring currents of the standalone AND, OR, NAND and NOR gates, the AND+NOR and OR+NAND structures showed different trends regarding the P-hit and N-hit interactions. The AND+NOR presents the highest SET cross-section for the N-hit interactions while the OR+NAND is for P-hit interactions.

The comparisons with LET = 1.69 MeV.cm^2/mg is depicted in Fig. 13. For lower LET, the AOI21 gate shows an even smaller difference between the two hit interactions. In contrary to the higher LET result, now the N-hit SET cross-section is slightly greater than the P-hit one. Moreover, the low LET ion induced a pronounced difference between the results for the AND+NOR implementation. About 91.7% greater than the P-hit SET cross-section, the circuit shows a higher sensitivity to the N-hit configuration despite the reduced N-hit drain sensitive area as shown in Table 1. On the other hand, the complex-logic OAI21 gate and the OR+NAND circuit demonstrate to be resilient to this particle LET considering the N-hit interactions.

As verified in this study and in the literature, the sensitivity of the circuit design is highly dependent of its input signal state [14-17]. For a given VLSI circuit, the designer is able to estimate the switching activity probability, i.e. the likelihood that an input signal will have the logic state one. Accordingly, the SET sensitivity can be estimated based on the propagation of the switching activity probability of the primary input signals to the individual gates. For simplicity, in this work, the overall SET sensitivity of the circuits will be evaluated by the mean value of the SET cross-section for the P-hit interactions (i.e. all input signals at state one) and for the N-hit interactions (i.e. all input signals at state zero). In Fig. 12, the third column bar represents the mean SET cross-section for ion LET = 78.23 MeV.cm^2/mg. The complex-logic gates show a higher mean cross-section compared to their alternative implementations. However, for a low LET, as shown in Fig. 13, the lowest mean cross-sections are obtained for the complex-logic gates. Accordingly, for applications requirements underlying low LET radiation environment, the complex-logic gates can be the best implementation option.

The radiation-induced cross-section can be represented in logarithmic scales as proposed in [24]. As shown in Fig. 14 and Fig. 15, the cross-section curve follows a power law function of the particle LET. It occurs due to the collection efficiency that depends continuously on the distance between the collection zone and the location of the deposited charge. This behavior was verified and it is in agreement with experimental data of

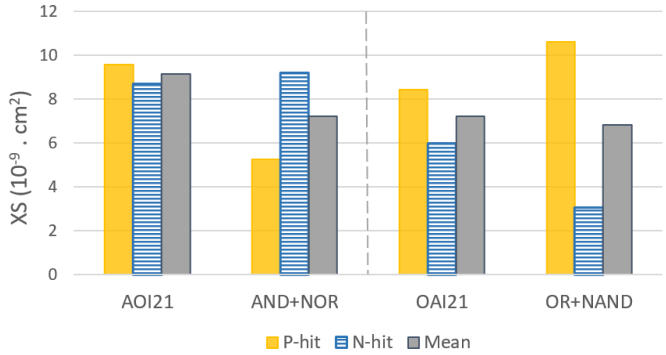

Fig. 12. Comparison of the SET cross-section considering P-hit and N-hit simulations under LET = 78.23MeV.cm^2/mg.

testing campaigns in [24]. In Fig. 14 the SET cross-section

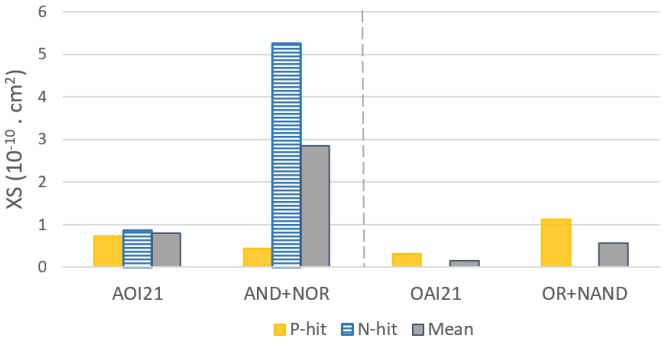

Fig. 13. Comparison of the SET cross-section considering P-hit and N-hit simulations under LET = 1.69MeV.cm^2/mg.

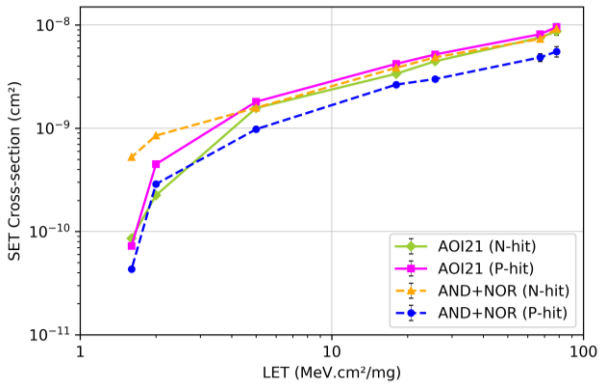

Fig. 14. Log-log representation of SET cross-section curves for AOI21 and AND+NOR considering N-hit interactions and P-hit interactions.

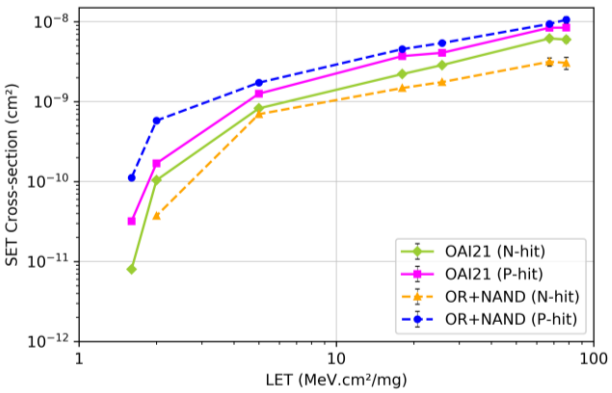

Fig. 15. Log-log representation of SET cross-section curves for OAI21 and OR+NAND considering N-hit interactions and P-hit interactions.

curves for the AOI21 and AND+NOR circuits are represented in logarithmic scales. Clearly, it is possible to observe the power law shape of the cross-section in function of the particle LET. However, considering the LET under 2 MeV.cm^2/mg for the AOI21 and 5 MeV.cm^2/mg for the AND+NOR, the cross-section curves show an abrupt decrease and fall out of the power law shape. It implies that multiple collection zones dominate the failure mechanism in different ways and the cross-section no longer follows the power law dependence [22, 24]. The same points are found for the OAI21 and OR+NAND circuits in Fig. 15. In contrast to the curves in Fig. 14, the cross-section curves in Fig. 15 are far more distant when comparing the N-hit interactions and P-hit interactions, mainly for the OR+NAND circuit. For the complete range of LET, both SET cross-section curves for the OAI21 remained in between the cross-section curves of the OR+NAND circuit.

V. Conclusions

The cell-based design methodology is widely used for a wide range of VLSI applications. Due to the plurality of pre-designed and characterized standard cells, different optimization algorithms can be implemented to address several constraints such as power consumption, performance and reliability. This work proposed to analyze the implications of adopting complex-logic cells to the Single-Event Transient sensitivity under heavy ions. The complex-logic cell layout provides a denser design with reduction in the power consumption and area. Further, due to the structure of its transistor networks, the complex-logic gates showed a quite similar sensitivity for the P-hit and N-hit interactions, in contrast with its counterpart implementation. However, the reduction of the layout design area does not reduce significantly the overall drain sensitive area of the circuit, leading to a similar or worse robustness than an implementation using basic logic cells. Additionally, the complex-logic gates limit the effectiveness of logical masking inherent in combinational logic circuits. For low LET, the usage of complex-logic gates can induce improved SET robustness, but more research should be conducted to carefully analyze its applicability. The SET analysis of standard cells can be used to improve the reliability of ASICs when applied along the logic synthesis. To overcome the overhead simulation time of the predictive MC simulations when considering circuits containing thousands of standard cells, this analysis can be used locally to evaluate single gates in the critical logic paths that greatly impact the functionality of the circuit.

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