Fake Currency Detector

Digital Systems (ES 203) Project

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ABSTRACT

With technological advancements increasing day by day, the misuse of this technology has also escalated, leading to a nuisance to the public and citizens. One such example of crimes is printing and using the fake currency. This is a loss not only for the individual who is duped but also for the country's economy as a whole. To curb this crime, we have designed a fake currency note detector, implemented on the **Field Programmable Gate Array (FPGA)**.

BACKGROUND

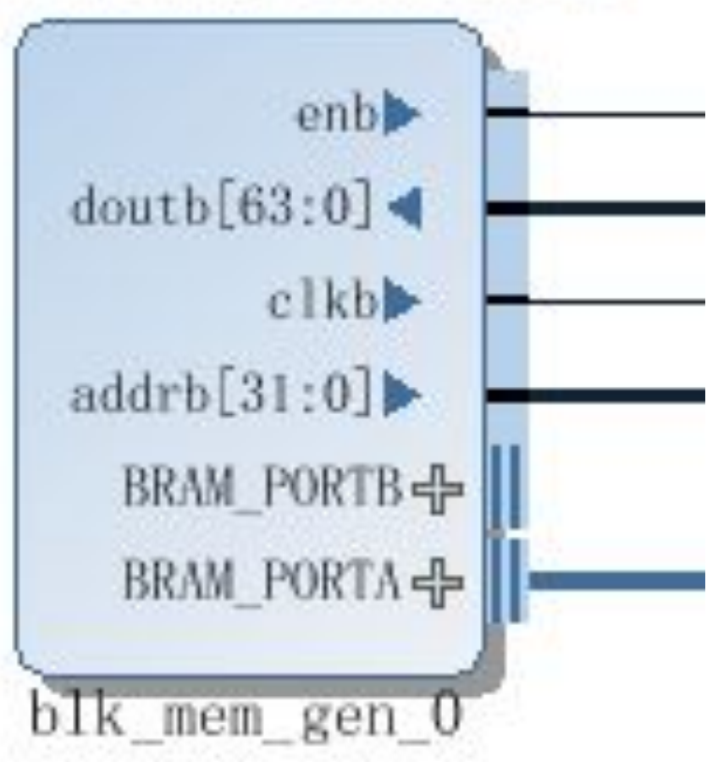
Every currency note has certain common features such as the security thread consisting of black strips and the triangular IM (Identification mark) on an Rs. 100 note.

These characteristics of the original note help to differentiate them from a fake one. Hence, we use a method to detect the absence of one or all of these features by firstly converting the note into the BW scale.

1) Storing Real Currency Note image into the FPGA:

- To feed the image of the real currency into Verilog, we need to convert it to binary (**.coe file**).
- The converted image from **MATLAB** is such that it has as many rows as the total number of pixels and the write depth is 1 (Binary number). So our **256 x 144p** currency note image will have **36864 rows**.
- Then a **Block Memory Module** is generated in the project which has as many addresses as the number of rows. So, in our case, it will have 36864 address bits.

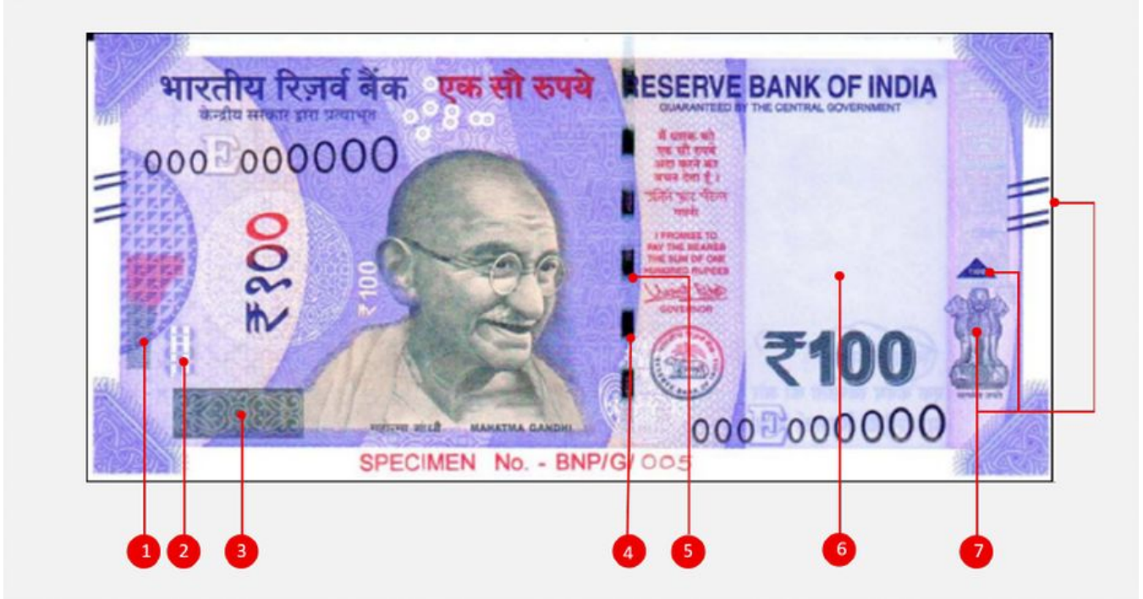
This Memory module, like other modules, can be instantiated and used in the main module.



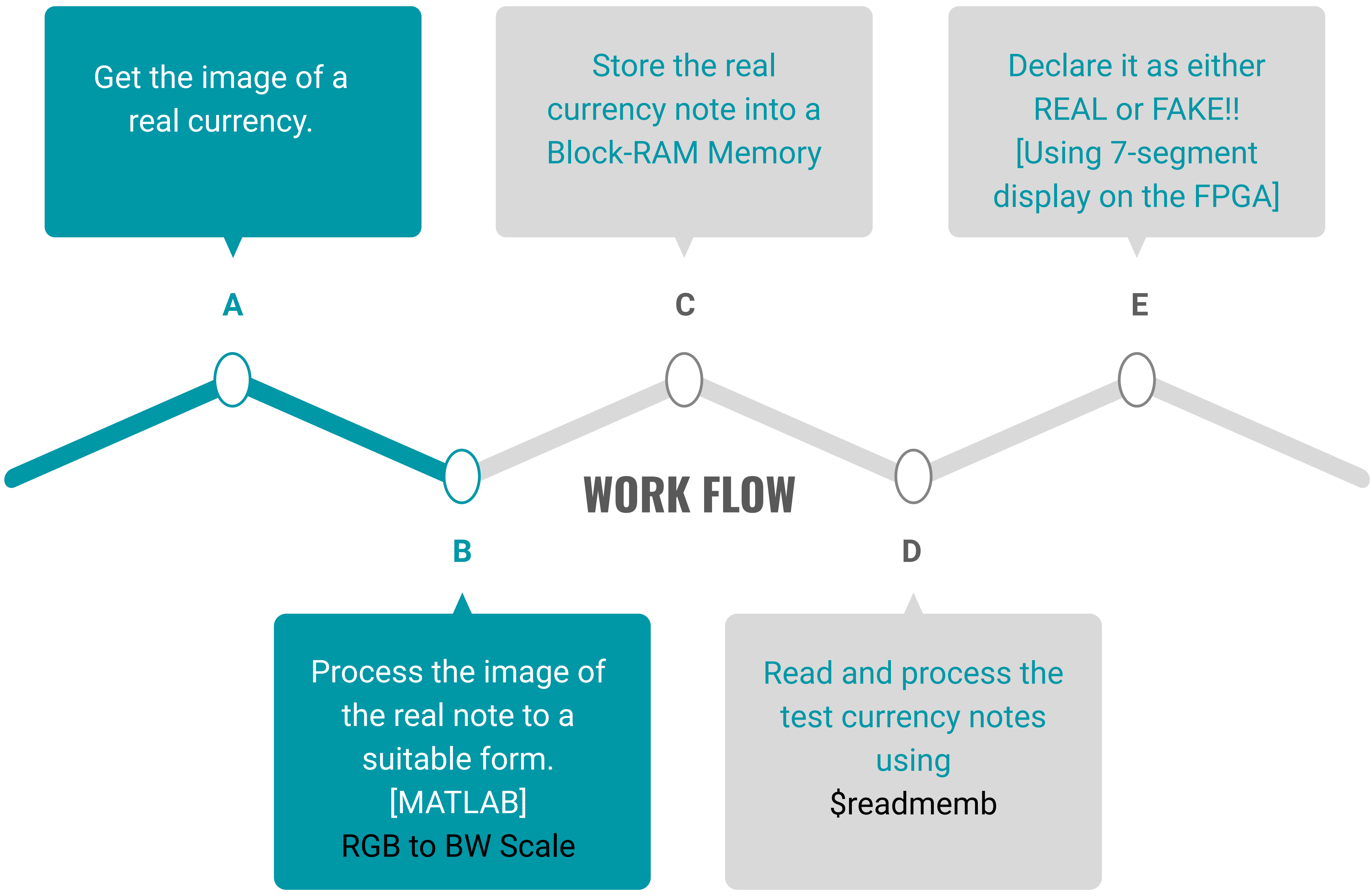
2) Scanning and Reading the Test Case Currency notes:

- Uploaded the ***'.txt'*** file of the pre-processed note (using MATLAB) in the simulation sources of the Vivado project.
- Read the text file values into a **2-D array** of one-bit numbers using the "***$readmemb***" function in Verilog.

3) Security Features that we have compared:



- The triangular identification mark in the 100 rupee note.[7]
- The vertical Security Thread.[4]



WORK FLOW

A: Get the image of a real currency.

B: Process the image of the real note to a suitable form. [MATLAB] RGB to BW Scale

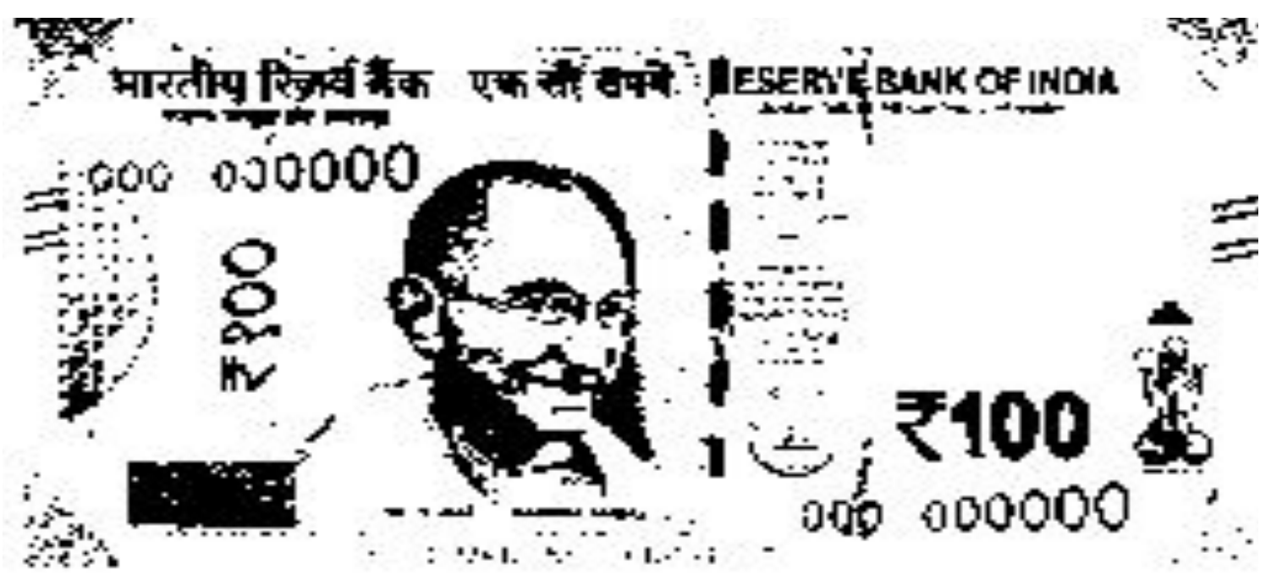
C: Store the real currency note into a Block-RAM Memory

D: Read and process the test currency notes using $readmemb

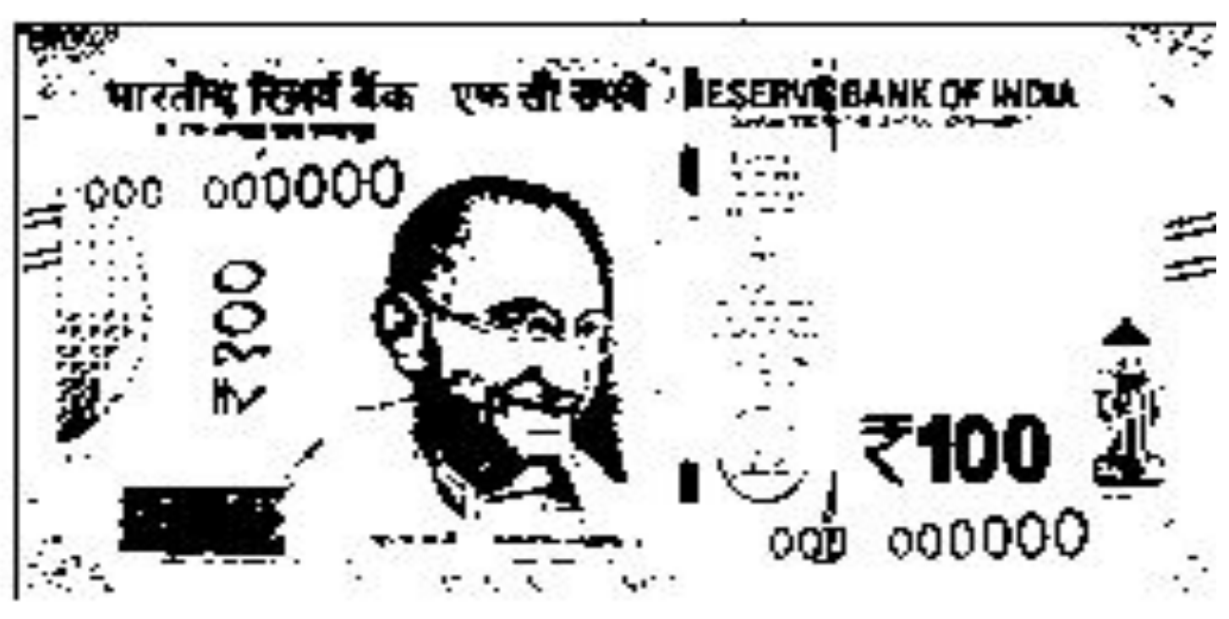
E: Declare it as either REAL or FAKE!! [Using 7-segment display on the FPGA]

Real Currency Note

RGB TO BW

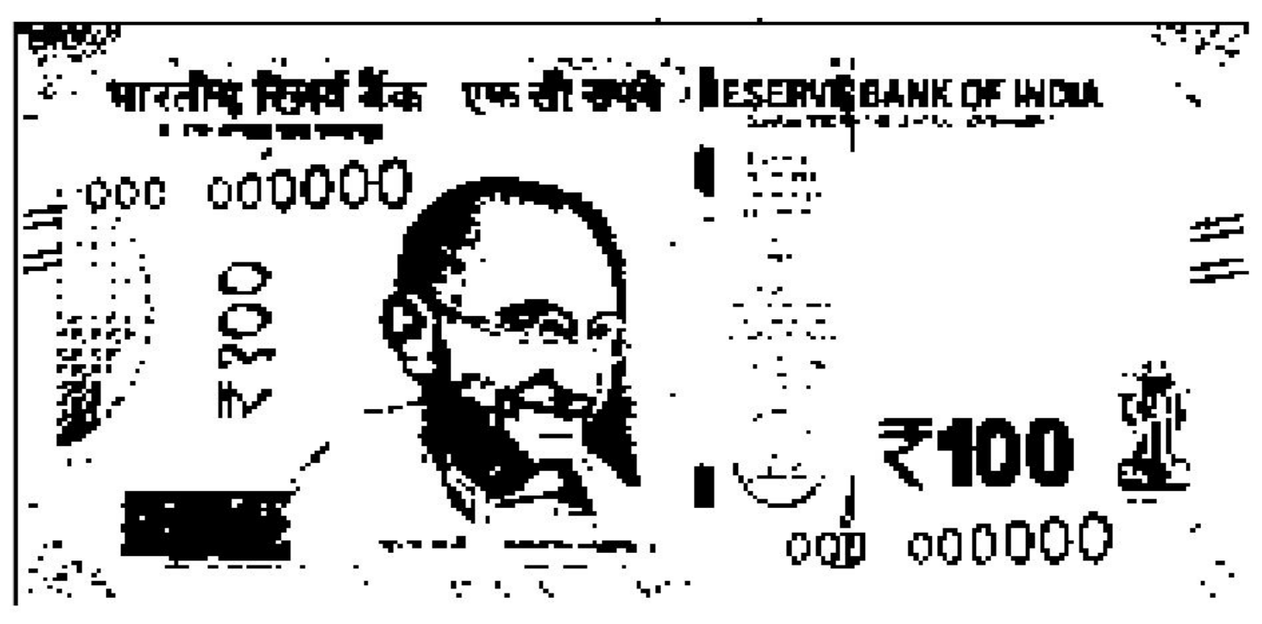


Real Currency Note

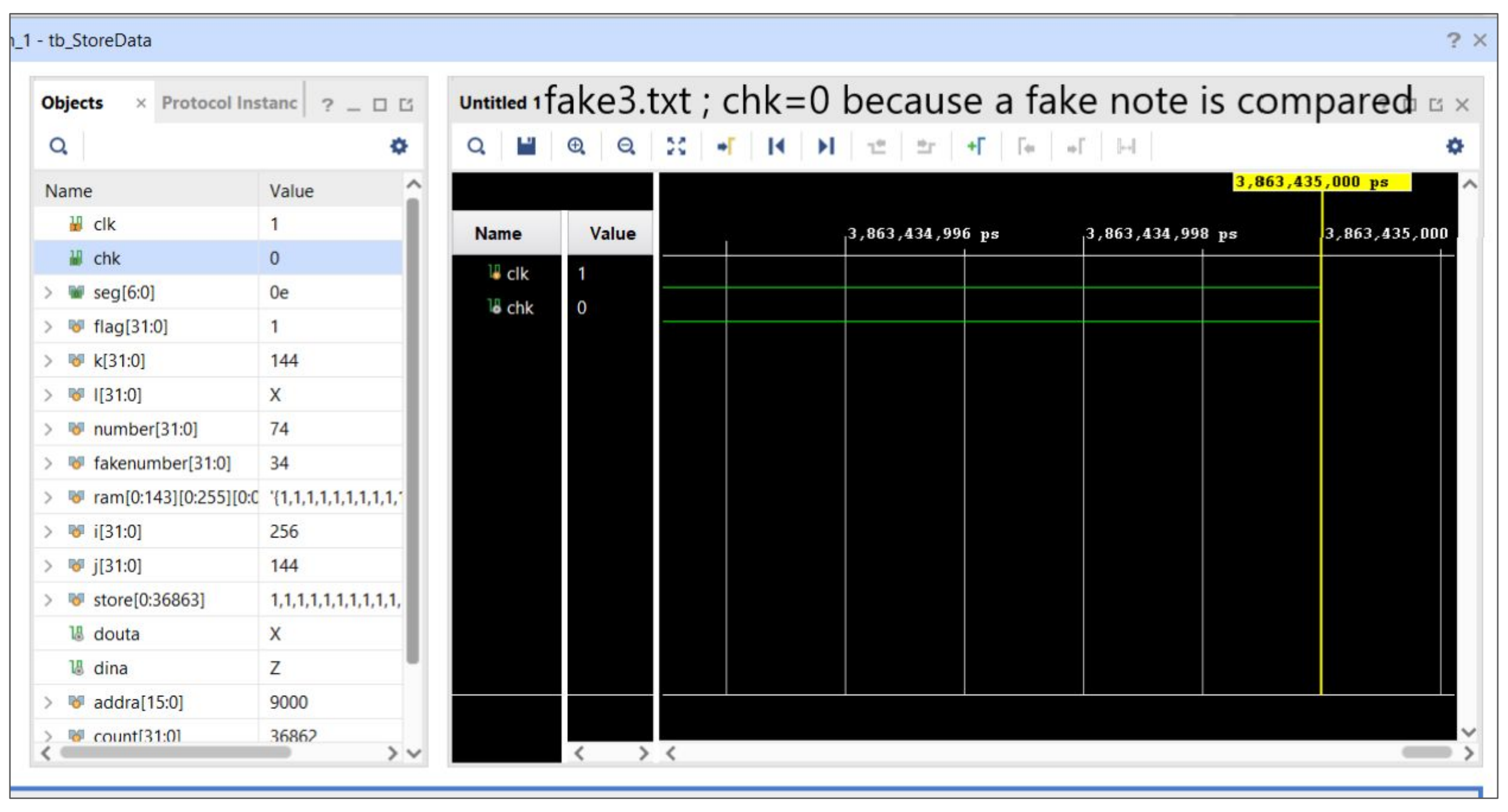


Fake Test Note - (a)
Absence of complete Security Thread

READING INTO VIVADO



Fake Test Note - (b)
Absence of the Identification Mark (Triangle) & complete Security Thread



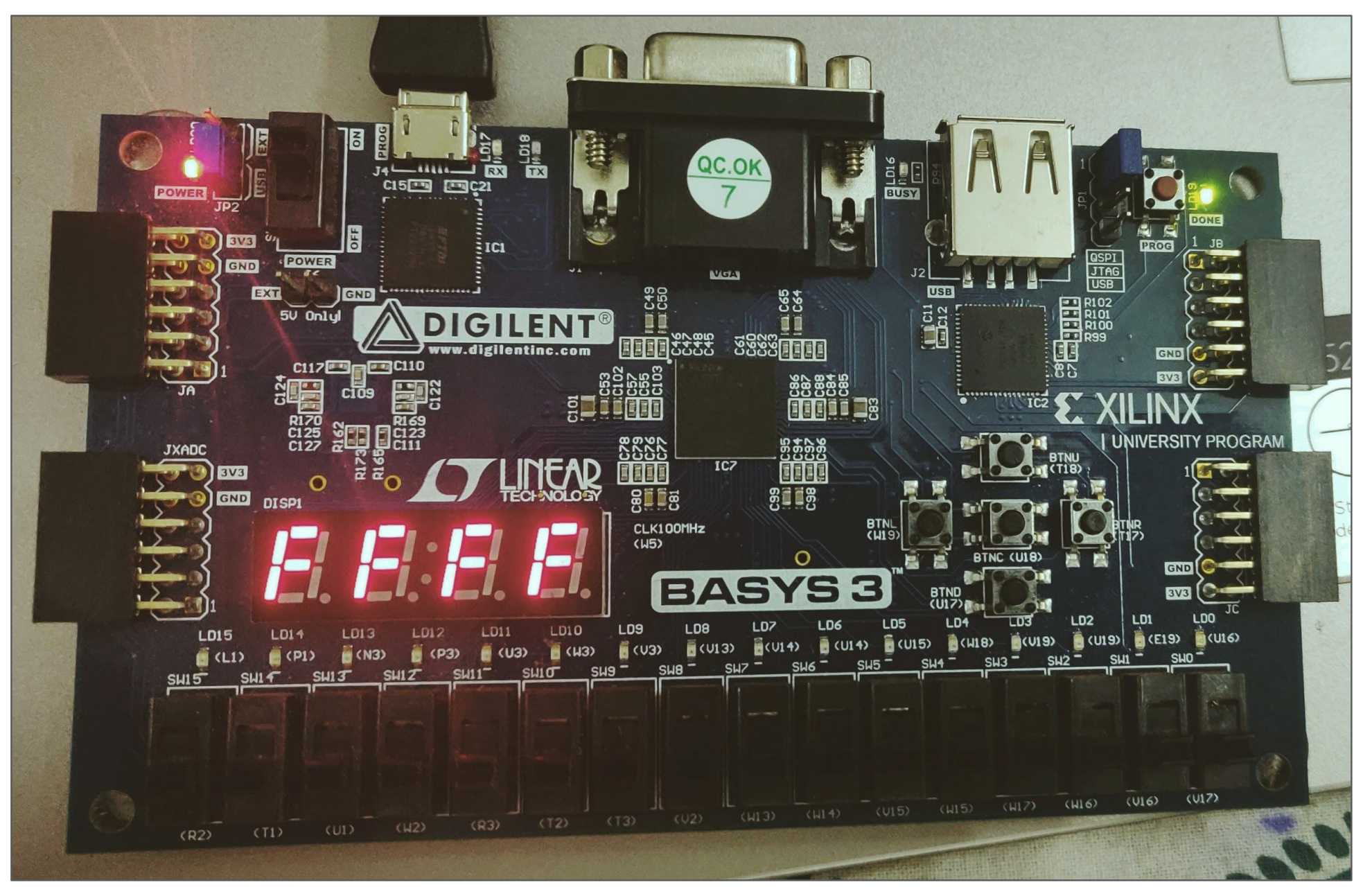
_1 - tb_StoreData

fake3.txt ; chk=0 because a fake note is compared

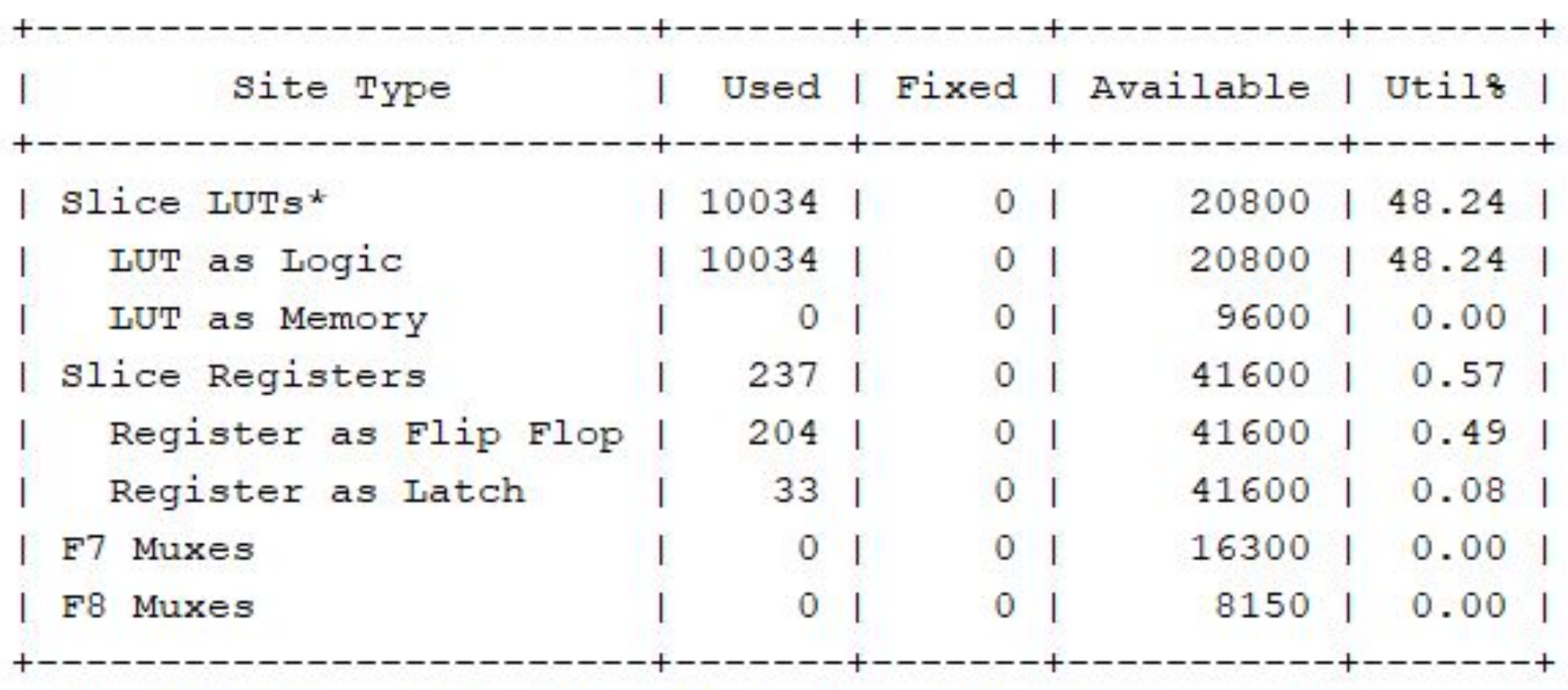
Name	Value
clk	1
chk	0
seg[6:0]	0e
flag[31:0]	1
k[31:0]	144
l[31:0]	X
number[31:0]	74
fakenumber[31:0]	34
ram[0:143][0:255][0:0	'{1,1,1,1,1,1,1,1,1,'
i[31:0]	256
j[31:0]	144
store[0:36863]	1,1,1,1,1,1,1,1,1,1,
douta	X
dina	Z
addra[15:0]	9000
count[31:0]	36862

Name	Value
clk	1
chk	0

SIMULATION GRAPH



FPGA IMPLEMENTATION



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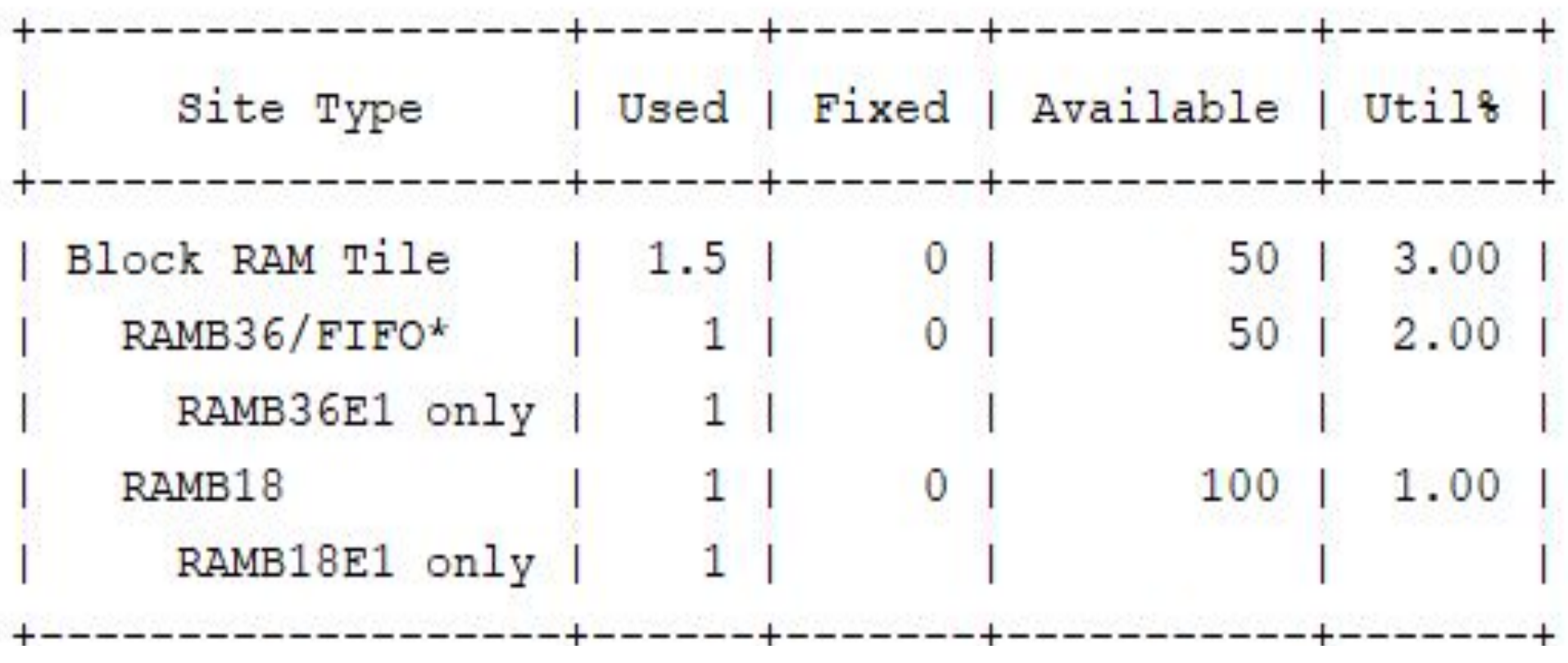
+-------------------------+-------+-------+-----------+-------+
|        Site Type        |  Used | Fixed | Available | Util% |
+-------------------------+-------+-------+-----------+-------+
| Slice LUTs*             | 10034 |     0 |     20800 | 48.24 |
|   LUT as Logic          | 10034 |     0 |     20800 | 48.24 |
|   LUT as Memory         |     0 |     0 |      9600 |  0.00 |
| Slice Registers         |   237 |     0 |     41600 |  0.57 |
|   Register as Flip Flop |   204 |     0 |     41600 |  0.49 |
|   Register as Latch     |    33 |     0 |     41600 |  0.08 |
| F7 Muxes                |     0 |     0 |     16300 |  0.00 |
| F8 Muxes                |     0 |     0 |      8150 |  0.00 |
+-------------------------+-------+-------+-----------+-------+
```



```
+-------------------+------+-------+-----------+-------+
|     Site Type     | Used | Fixed | Available | Util% |
+-------------------+------+-------+-----------+-------+
| Block RAM Tile    |  1.5 |     0 |        50 |  3.00 |
|   RAMB36/FIFO*    |    1 |     0 |        50 |  2.00 |
|     RAMB36E1 only |    1 |       |           |       |
|   RAMB18          |    1 |     0 |       100 |  1.00 |
|     RAMB18E1 only |    1 |       |           |       |
+-------------------+------+-------+-----------+-------+
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SYNTHESIS REPORT