## qHiPSTER: The Quantum High Performance Software Testing Environment

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#### **ABSTRACT**

We present qHiPSTER, the Quantum High Performance Software Testing Environment. qHiPSTER is a distributed high-performance implementation of a quantum simulator on a classical computer, that can simulate general single-qubit gates and two-qubit controlled gates. We perform a number of single- and multi-node optimizations, including vectorization, multi-threading, cache blocking, as well as overlapping computation with communication. Using the TACC Stampede supercomputer, we simulate quantum circuits ("quantum software") of up to 40 qubits. We carry out a detailed performance analysis to show that our simulator achieves both high performance and high hardware efficiency, limited only by the sustainable memory and network bandwidth of the machine.

#### 1. INTRODUCTION

Simulation has long been an invaluable tool for modeling classical computer systems, such as digital circuits, processor microarchitecture, or interconnection networks. For example, processor designers rely on cycle-accurate simulators to characterize the impact of new hardware features on application performance and CPU power [11, 24]. System designers use network simulators to quantify the impact of new network topologies on communication pattern of a distributed applications [35].

Similarly, using a classical computer to simulate a quantum system is important for better understanding its behavior. Such simulations can be used to validate the complexity of new quantum algorithms, to study quantum circuits that are difficult to characterize analytically, or to investigate the performance of circuits in the presence of noise.

For example, many algorithmic choices must be made in the design of a quantum circuit for calculating molecular energies [8, 33, 28]. There are multiple methods for mapping the problem onto a set of qubits[42, 36], as well as many possible gate sequences for approximating the operators [17, 9]. Using a high performance simulator, one can

System	Memory (PB)	Max qubits
TACC Stampede	0.192	43
Titan	0.71	45
K computer	1.4	46
APEX2020 [1]	4-10	48-49

Table 1: Examples of TOP500 supercomputing systems, their memory capacity (in Petabytes), and largest quantum system they can simulate.

study the effects of these parameters on the algorithm's performance. This in turn helps to minimize the quantity of quantum resources required to bound the error below a certain value. Alternatively, one may wish to implement various noise models to determine the minimum required decoherence times for a given level of accuracy. Simulating other proposed quantum algorithms, including the Hubbard model [41] and the finite element method [12], might provide similar insight.

While there exists number of techniques to simulate specific classes of quantum circuits efficiently [19, 26, 7, 39, 16], simulation of generic quantum circuits on classical computers is very inefficient, due to the exponential overhead [15]. Specifically, the fundamental challenge is that the size of state, or number of quantum amplitudes, grows exponentially with the number of qubits. Given n qubits, the size of the state vector is  $2^n$  complex amplitudes, or  $2^{n+4}$  bytes. Thus, the memory capacity of the classical system imposes an upper bound on the size of the simulation. In addition, the size of the quantum circuit (its number of gates) can result in significant run-time requirements on the classical system.

These challenges can be mitigated by taking advantage of high-performance distributed computation. Most existing quantum simulators run on a single CPU [2]. Such simulations are limited to  $\approx 30-33$  qubits due to limited memory capacity and bandwidth of a single node. Several distributed quantum simulators were developed which could simulate more qubits, compared to a single node, due to larger aggregate memory capacity of the system. One of the first distributed quantum simulators, developed in 2002, simulated up to 30 qubits on the Sun Enterprise 4500 system [31]. More recently, another simulator, called JUMPIQCS, developed to model impact of noise on quantum simulation, simulated 36 qubits on the JUMP IBM p690+ system [38].

<sup>&</sup>lt;sup>1</sup>Here and in the rest of the paper we assume complex double precision, with eight-byte real and eight-byte imaginary parts.

Table 1 shows examples of several supercomputers among the top ten systems in the most recent TOP500 list<sup>2</sup>, their aggregate memory capacity, and the number of qubits the system can simulate. We see that today's practical limit is 46 qubits. 48-49 qubit simulations will become possible in 2020 with the arrival of NERSC-9 and Crossroads pre-exascale systems [1].

While the aggregate capacity of a particular HPC system is fixed, the quantum simulation time can be further improved. Herein we describe the implementation of qHiPSTERand the optimization required to achieve high performance and high hardware efficiency on the Stampede supercomputer. Using 1024 nodes, the maximum available allocation, we simulate quantum circuits of up to 40 qubits. For a 40qubit system, when no communication is required, singleand two-qubit controlled gate operations are memory bandwidth bound and take 0.43 and 0.21 seconds, respectively. Cache blocking optimization results in an additional  $\approx 2.56 \times$ run-time reduction of these gate operations. When communication is required, these gate operations becomes network bandwidth bound, and their run-time increases by 10×, which is commensurate with the memory to network bandwidth ratio on Stampede. Finally, using 1024-node distributed simulation, we simulate the 40-qubit quantum Fourier transform, an important kernel of many quantum algorithms, in 997 seconds.

Section 2 briefly reviews single- and two- qubit gate operations. Section 3 describes the single and multi-node implementations of both of these operations in  $q\mathrm{H}i\mathrm{PSTER}$ . Section 4 discusses architectural and algorithmic optimizations, while Section 5 presents experimental results and detailed performance analysis of  $q\mathrm{H}i\mathrm{PSTER}$ . Future directions to further improve simulator performance are described in Section 6.

#### 2. BACKGROUND

The current version of qHiPSTER propagates only pure states. Hence, we operate on the  $2^N \times 1$  state vector instead of the  $2^N \times 2^N$  density matrix [30]. This approach does not preclude the simulation of mixed states when studying the effects of noise and gate errors. This is due to the fact that there are methods for reconstructing a density matrix from many iterations of simulated pure states [10].

We focus on implementing general single-qubit gates as well as two-qubit controlled gates (including, controlled-NOT gate), which are known to be universal [14]. A quantum single-qubit gate operation on qubit k can be represented by a unitary transformation:

$$U = I \otimes I \otimes ... \otimes Q \otimes ... \otimes I \otimes I \tag{1}$$

where Q is 2x2 unitary matrix,

$$Q = \left( \begin{array}{cc} q_{11} & q_{12} \\ q_{21} & q_{22} \end{array} \right)$$

However, one does not need to construct the entire U, and can perform Q transformation directly on the state vector, as shown in Figure 1, using an example of two qubits. Figure 1(a) shows the vector representation of a quantum state.

$$|\psi\rangle = \begin{pmatrix} \alpha_{00} \\ \alpha_{01} \\ \alpha_{10} \\ \alpha_{11} \end{pmatrix} - \begin{pmatrix} Q_{2x2}(1) & Q_{2x2}(0) \\ \alpha_{00} \\ \alpha_{01} \\ \alpha_{11} \end{pmatrix} \begin{pmatrix} Q_{00} \\ \alpha_{01} \\ \alpha_{10} \\ \alpha_{11} \end{pmatrix} \begin{pmatrix} Q_{00} \\ \alpha_{01} \\ \alpha_{10} \\ \alpha_{11} \end{pmatrix} \begin{pmatrix} Q_{00} \\ \alpha_{01} \\ \alpha_{11} \end{pmatrix} \begin{pmatrix} Q_{00} \\ \alpha_{11} \\ \alpha_{11} \\ \alpha_{11} \end{pmatrix} \begin{pmatrix} Q_{00} \\ \alpha_{11} \\ \alpha_{11} \\ \alpha_{11} \\ \alpha_{11} \end{pmatrix} \begin{pmatrix} Q_{00} \\ \alpha_{11} \\ \alpha_{11} \\ \alpha_{11} \\ \alpha_{11} \\ \alpha_{11} \end{pmatrix} \begin{pmatrix} Q_{00} \\ \alpha_{11} \\ \alpha_{11$$

(a) Quantum state

(b) Single-qubit gate

Figure 1: Example of (a) two-qubit quantum state, and (b) single-qubit gate operations, applied to qubits 0 and 1, respectively. Subscripts shows the binary representation of the state amplitude index. (b) also shows an example of distributed computation of gate operation on two processors,  $P_0$  and  $P_1$ .

Each amplitude has a subscript index in the binary representation. Figure 1(b) shows single-qubit gate operations on qubit 0 and 1, respectively. Applying a single-qubit gate to qubit 0 is equivalent to applying Q to every pair of amplitudes, whose indices have 0 and 1 in the first bit, while all other bits remain the same. Similarly, applying single-qubit gate to qubit 1 applies Q to every pair of amplitudes whose indices differ in their second bit. More generally, performing a single-qubit gate on qubit k of n-qubit quantum register applies Q to pairs of amplitudes whose indices differ in k-th bits of their binary index:

$$\alpha'_{*...*0_k*...*} = q_{11} \cdot \alpha_{*...*0_k*...*} + q_{12} \cdot \alpha_{*...*1_k*...*}$$

$$\alpha'_{*...*1_k*...*} = q_{21} \cdot \alpha_{*...*0_k*...*} + q_{22} \cdot \alpha_{*...*1_k*...*}$$
(2)

When the state vector is dense and stored sequentially in memory, the stride between  $\alpha_{*\dots*0_K*\dots*}$  and  $\alpha_{*\dots*1_k*\dots*}$  is  $2^k$ . For example, in Figure 1(b), the quantum gate applied to qubit 0 results in a stride of 1 ( $2^0$ ), while operating on qubit 1 results in stride of 2 ( $2^1$ ). Gate operations applied to high-order qubits result in large strides, and, as the result, pose challenges both to single and distributed implementations, as described in the later sections.

A generalized two-qubit *controlled-Q* gate, with a control qubit c and a target qubit t, works as follows: if c is set to  $|1\rangle$ , Q is applied to t; otherwise t is left unmodified:

$$\alpha'_{*1_c*0_t*...*} = q_{11} \cdot \alpha_{*1_c*0_t*...*} + q_{12} \cdot \alpha_{*1_c*1_t*...*} \alpha'_{*1_c*1_t*...*} = q_{21} \cdot \alpha_{*1_c*0_t*...*} + q_{22} \cdot \alpha_{*1_c*1_t*...*}$$
(3)

## 3. IMPLEMENTATION

This section describes the  $q{\rm H}i{\rm PSTER}$  implementation of single and controlled-Q gates for both single as well as multiple nodes.

## 3.1 Single node implementation

The single node implementation of a single-qubit gate is trivial, and directly follows from Equation 2, as shown in Figure 2 for an n-qubit quantum system. Namely, the outer loop iterates over consecutive groups of amplitudes of length  $2^{k+1}$ , while inner loop applies Q to every pair of amplitudes within the group, separated by the stride of  $2^k$ . The

<sup>&</sup>lt;sup>2</sup>TOP500 [29] ranks 500 most powerful commercially available supercomputers in the world, based on the scoring from LINPACK [34] benchmark. The list is compiled twice a year; the most recent compilation occurred in November, 2015.

Figure 2: Sinlge-qubit gate operation pseudo-code.

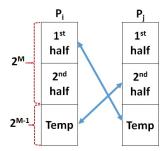


Figure 3: Distributed implementation of a singlequbit gate operation on qubit k. Communication occurs between pairs of processors,  $2^{k-m}$  apart. Each processor uses temporary storage to hold half of the state from the other processor. Processors exchange half of their states, compute on exchanged halves, and then perform another exchange.

controlled-Q operation is similar, except that it requires another (outer) loop to skip over the amplitudes which correspond to the controlled qubit of  $|0\rangle$  (or equivalently, a c-th bit of 0 in the binary representation of amplitude's index).

## 3.2 Distributed Implementation

In our distributed implementation, a state vector of  $2^n$  amplitudes  $(2^{n+4}$  bytes) is distributed among  $2^p$  nodes, such that each node stores a local state of  $2^{n-p}$  amplitudes. Let m = n - p. Naturally,  $2^{m+4}$  must be less than the total memory capacity of the node.

Given single-qubit gate operation Q on qubit k, if k < m, the operation is fully contained within a node. When  $k \ge m$ , the first and second elements of the pair are located on two different nodes and communication is required. Note that the distance between communicating processors in the virtual topology is  $2^{k-m}$ . We implement the communication scheme described in [38]. Our enhancements to this scheme are described in Section 4. Figure 3 demonstrates the scheme. Given a local state vector of  $2^m$  complex amplitudes, each node reserves an extra  $2^{m-1}$  words of memory as temporary storage. Each local state vector is logically partitioned into two halves. Both nodes perform pairwise exchange of these halves:  $P_i$  sends its first half to  $P_i$ , while  $P_i$  sends its second half to  $P_i$ . Each node places the received half into its own temporary storage. Next,  $P_i$  applies Q to its first half and the temporary storage (which contains first half of  $P_i$ ), while  $P_i$  applies Q to its second half and the temporary storage (which contains second half of  $P_i$ ). This results in  $P_i$  updating  $P_i$ 's second half, and  $P_i$ updating  $P_i$ 's first half. This is followed by another pairwise exchange, where  $P_i$  sends  $P_j$ 's updated half back to  $P_j$ , while  $P_j$  sends  $P_i$ 's updated half to  $P_j$ . This completes the

distributed state update. The advantage of this approach is that it distributes work evenly among pairs of nodes.

The distributed implementation of controlled gate operation with controlled qubit c and target qubit t is more involved. If t < m, there is no communication, while for  $t \ge m$  communication is required. In addition, for each of these two cases, we use different kernels, depending on whether c < m, or  $c \ge m$ . Therefore, there are total of four cases for a controlled qubit gate, as opposed to only two for single-qubit gate. We omit further details for brevity.

# 4. ARCHITECTURAL AND ALGORITHMIC OPTIMIZATION

In this section we describe several single- and multi-node performance optimizations we apply to achieve high performance in  $q{\rm H}i{\rm PSTER}$ .

#### 4.1 Vectorization

Both single and controlled gate operations have the same inner loop shown in Figure 2 (Lines 2-7). This loop is data parallel: every iteration performs the same operation on different set of data. One of the most common and energy efficient methods for exploiting data-level parallelism is via single-instruction-multiple-data (SIMD) execution. In SIMD execution, a single instruction operates on multiple data elements simultaneously. This is typically implemented by extending the width of registers and ALUs, allowing them to hold or operate on multiple data elements, respectively. The rest of the system is left untouched.

Modern Intel CPUs support SIMD (Single Instruction Multiple Data) instructions, such as AVX2 [4], which can perform 4 double-precision operations simultaneously on 4 elements of the input registers. We map every two iterations of the inner loop of Figure 2 to 4-wide SIMD instructions; each iteration, which operates on a complex number composed of real and imaginary parts, is mapped to two entries of the SIMD register. We developed specialized code, using compiler intrinsics, to efficiently perform complex arithmetic using SIMD instructions.

#### 4.2 Threading

Modern CPUs have multiple cores, and some have several threads per core. To achieve good performance it is important to parallelize the workload among these threads. There are two levels of parallelization of the code in Fig. 2: one over the inner loop and the other over the outer loop<sup>3</sup>. Note that the outer loop performs  $2^{n-k-1}$  iterations, while the inner loop performs  $2^k$  iterations; a smaller k results in more (less) outer (inner) loop iterations, while larger k has the opposite effect. For example, when k=n-4, the outer loop only performs eight iterations, which will leave some cores idle when this loop is parallelized on the CPU with more than eight threads. To choose which loop to parallelize, we dynamically check the number of iterations and parallelize at the nest level with the largest amount of work.

## 4.3 Improvement in Communication

We improve upon the communication scheme described in Section 3, which requires an extra  $2^{m-1}$  words of temporary storage per node. This implementation is wasteful.

 $<sup>^3</sup>$ Controlled gates introduce an additional loop nest and thus an additional level of parallelization

Consider, for example, a node with 48GB of main memory. In theory, one could use 32GB for state vector and remaining 16GB for temporary storage to simulate system with 31 qubits. In practice, no application can use the entire memory of the machine without significant performance impact due to paging, because some of the memory is reserved for the OS, system software, and other purposes. Hence we can only simulate quantum system with 30 qubits in this case.

To reduce the memory requirements of temporary storage, we divide the distributed phase into multiple steps. At each step we exchange and reserve temporary storage for only a small portion of the state vector, as opposed to the entire half as in the original approach. We apply gate operations only to this portion. Each steps reuses the same temporary storage, which is dramatically reduced. Continuing with the previous example, we can use 8GB of temporary storage instead of 16GB. It requires two steps, but enables simulating 31 qubits - one qubit more than with our original approach. As long as the amount of data exchanged within each step is large enough to saturate the network bandwidth, the overall run-time remains the same as in original approach.

The total run-time of the distributed application,  $T_{tot}$ , is a function of compute time,  $T_{comp}$ , and communication time,  $T_{comm}$ . The original implementation of the quantum simulator performs these phases separately, resulting in  $T_{tot} = T_{comp} + T_{comm}$ . Using a multistep approach, described above, we overlap communication and computation in step i with state exchange in steps i-1 and i+2. This results in  $T_{tot} = max(T_{comp}, T_{comm})$ , thus partially hiding overhead of communication.

## 4.4 Cache Blocking through Gate Fusion

Single and controlled qubit operations perform small amounts of computation. Therefore, their performance is limited by memory bandwidth when the size of the state vector exceeds the size of the Last Level Cache (LLC). Modern CPUs have large LLCs, tens of MBytes per socket. LLC has a much higher bandwidth than memory (albeit, much smaller capacity), but taking advantage of high LLC bandwidth requires restructuring the algorithm so that its working set fits in an LLC [23].

Using fused gates we can block computation in LLC as shown in Figure 4. Assume that LLC has a size of  $2^{l_c}$ . For a given quantum circuit, we identify groups of consecutive gates, where each gate operates on some qubit k,  $k < l_c$ . We iterate over blocks of  $2^{l_c}$  amplitudes of the state vector (Line 1). Each of the fused gates is applied to this block (Lines 2-4), while the block remains resident in LLC and

```
1: for gb \leftarrow 0; gb < 2^n; gb += 2^c do
            for group of gates, on some qubit k (k < l_c) do
 2:
                 for g \leftarrow gb; g < gb + 2^{l_c}; g += 2^{k+1} do for i \leftarrow g; i < g + 2^k; i + + do
 3:
 4:
 5:
                             \alpha_i' \leftarrow q_{11} \cdot \alpha_i + q_{12} \cdot \alpha_{i+2K}
 6:
                            \alpha'_{i+2K} \leftarrow q_{21} \cdot \alpha_i + q_{22} \cdot \alpha_{i+2K}
 7:
 8:
 9:
                       end for
10:
                  end for
11:
            end for
```

Figure 4: Pseudo-code shown gate fusion performed on a block of fused gates.

Case	Operation	Analytic	Stampede
	Single-qubit gate		
1	k < m	$\frac{2^{m+5}}{B_{mem}}$	$0.43~{ m sec}$
2	$k \ge m$	$\frac{2^{m+5}}{B_{net}}$	$3.12  \mathrm{sec}$
	Two-qubit gate		
3	t < m, c < m	$\frac{2^{m+4}}{B_{mem}}$	$0.21~{ m sec}$
4	$t < m, c \ge m$	$\frac{2^{m+5}}{B_{mem}}$	$0.43~{ m sec}$
5	$t \ge m, c < m$	$\frac{2^{m+4}}{B_{net}}$	$1.56  \sec$
6	$t \geq m, c \geq m$	$\frac{2^{m+5}}{B_{net}}$	$3.12  \sec$

Table 2: Lower bound ('best case') time per gate for single and two-qubit gates. The first column shows different cases. The second column shows the analytic expression, as the function of m,  $B_{mem}$ , and  $B_{net}$ . The third column shows specific times on our experimental platform for n=29,  $B_{mem}=40$  GB/s, and  $B_{net}=5.5$  GB/s.

therefore can benefit from the LLC's high bandwidth.

## 5. PERFORMANCE

#### **5.1** Experimental Setup

We evaluate the performance and scalability of qHiPSTER on the Stampede supercomputer. Stampede [6] at the Texas Advanced Computing Center (TACC)/Univ. of Texas, USA (# 10 in the current TOP500 list) consists of 6,400 compute nodes, each of which is equipped with two sockets of Xeon E5-2680 connected via QPI and 32GB of DDR4 memory per node (16GB per socket), as well as one Intel®Xeon Phi<sup>TM</sup>SE10P co-processor. Each socket has 8 cores, with hyperthreading disabled. We use OpenMP 4.0 [32] to parallelize computation among threads. The nodes are connected via a Mellanox FDR 56 Gb/s InfiniBand interconnect. Both sockets within the node share a single network card, connected via PCIe. Therefore, when both sockets communicate at the same time, each socket only gets half of the available network injection bandwidth.

In this evaluation we have used only 1000 nodes (2000 sockets), the maximum available allocation, and did not use Xeon Phi co-processors. With aggregate memory capacity of 32 Tbytes across 1000 nodes, we were able to simulate quantum system of up to 40 qubits.

#### 5.2 Lower Bounds on Achievable Performance

The run-time of data intensive application, such as a quantum circuit simulator, is bound either by memory bandwidth, when run on single node, or by network bandwidth, when run in distributed fashion. The memory bound is equal to the total required memory traffic divided by the sustainable memory bandwidth  $(B_{mem})$ , measured by STREAM Copy benchmark [27]. The network bound is equal to the total amount of network traffic divided by sustainable network bandwidth  $(B_{net})$ , measured by the OSU bandwidth benchmark [5]. On our system,  $B_{mem}=40~{\rm GB/s}$ , while the  $B_{net}=5.5~{\rm GB/s}$  (bidirectional), per socket. The closer the actual application run-time is to one of those two bounds, the higher its hardware efficiency is.

Table 2 shows lower run-time bounds for single and controlled qubit gates, with and without communication. For example, the expected lower bound for single-qubit operation when no communication is required (k < m, Case 1) is  $2^{m+5}/B_{mem}$  seconds. Here,  $2^{m+4}$  is the size of the state vector in bytes, while an additional factor of two is due to the fact that the state vector is both read and written, which doubles the amount of memory traffic. Since our system has 16GB of memory per socket, it can simulate at most 29 qubits within a socket, because the state vector occupies 8.5GB of memory. With stream bandwidth  $B_{mem} = 40$ GB/s, single socket memory bound is 0.43 seconds for 29qubit quantum simulation. Since the controlled qubit gate accesses only half of the state vector, its expected runtime is 0.22 seconds, also when there is no communication (Case 3). When communication is required, a pair of nodes performs two exchanges of half of the state with another node, as described in Section 3.2. This results in network bound of  $(2^{m+5})/B_{mem}$ . For m=29, the corresponding network bound is 3.12 seconds, which is 7.3× higher than memory bound, and is effectively a ratio between memory and network bandwidth.

In the remainder of the section we use these bounds to explain the results of our experiments.

## **5.3** Single Node Performance

Our single-qubit gate operation runs very close to memory bound, regardless of which qubit the gate is applied to. Figure 5 shows a runtime heatmap of two-qubit controlled gate operations for 29 qubits (n = 29), and all combinations of control and target qubits. Green corresponds to the high end of the performance spectrum, that is memory bound of 0.21 seconds (Case 3, Table 2). We see that low values of the control qubits result in suboptimal performance of 0.4 seconds ( $\approx 2 \times$  higher than memory bound). As the value of control qubit increases, the performance improves, and starting from control qubit 10 it approaches memory bound. The reason for suboptimal performance at a lower number of qubits is as follows. Recall that a control gate affects only the amplitudes whose c'th bit is set to 1. Thus, the memory access pattern only accesses the second half of every  $2^c$ -long memory region. These 'holes' break the stride and interrupt the hardware prefetcher which is trained to prefetch elements which are at a constant stride from each other [18]. Not only does the failure of the prefetcher to detect the stride expose cache miss latency, it also results in wasted memory bandwidth, due to prefetching useless data. This results in run-time increase.

Figure 7 shows performance of fusion optimization on a single node for the *Inverse Quantum Fourier Transform* (IQFT), as the number of qubits varies between 18 and 29. IQFT on n-qubit quantum register, shown in Figure 6, consists of n stages. At stage i, IQFT applies Hadamard gate as well as n-i-1 controlled rotation gates to qubit i, where control gates are controlled by qubits  $i+1,\ i+1,\ ...,\ n$ , respectively.

IQFT naturally benefits from gate fusion optimization: all stages from 0 to  $l_c$  can be fused and therefore blocked in LLC. Results of applying fusion optimization to IQFT are shown in Figure 7, for the quantum register sizes between 18 to 29 qubits. For a given number of qubits n, we report performance in terms of achieved bandwidth (GB/s),

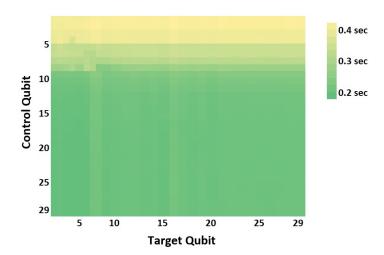


Figure 5: Performance of controlled single-qubit gate on a single node for a 29-qubit system (n = 29)

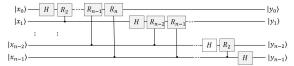


Figure 6: Inverse Quantum Fourier Transform circuit applied to an n-qubit quantum register.

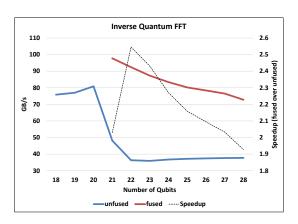


Figure 7: Performance of gate fusion optimization applied to Inverse Quantum Fourier Transform (IQFT).

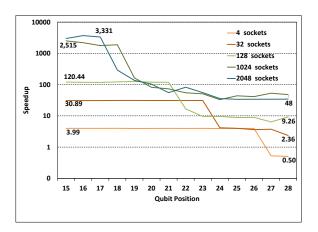


Figure 8: Strong scaling speedup over a single socket for single-qubit operation on 29 qubits. Results are shown for gate operations on qubits 15-28 for every configuration. Results for qubits 0-14 are similar to the results for qubit 15 and are omitted.

computed as an aggregate amount of memory traffic for all gates divided by the overall run-time of IQFT. The closer the achieved bandwidth is to STREAM bandwidth of 40 GB/s, the closer IQFT performance is to memory bound. Since on our system the LLC size is 20 MB,  $l_c=20$ , and thus we can fuse all the way to the 19th stage of IQFT, independent on n.

The "unfused" curve shows baseline performance without gate fusion. We see that IQFT performance for 18, 19 and 20 qubits is  $\approx 80~\mathrm{GB/s}$  per gate, which is 2x higher than the memory bandwidth of 40 GB/s. This is due to the fact that for these problem sizes, the full quantum state naturally fits into LLC and thus benefits from higher LLC bandwidth. As we increase the number of qubits, the state no longer fits into LLC, and we see a dramatic drop in performance to 40 GB/s, which is the expected STREAM bandwidth. The performance stays at 40 GB/s all the way to 29 qubits.

The "fused" curve shows performance with gate fusion. We see that for 21 qubits we achieve 100 GB/s memory bandwidth per gate, even though the state no longer fits into LLC. Thus, we see that fusion optimization increases performance by almost  $2.5\times$ , compared to "nofusion." As the number of qubits increases, the performance decreases gradually, due to the fact that the number of stages which cannot be fused increases. But even for 29 qubits, we achieve a bandwidth of 70 GB/s, which is nearly  $2\times$  compared to the "nonfused" version.

#### 5.4 Multi Node Performance

Strong Scaling: Figure 8 shows strong scaling speedup over a single socket, as we vary number of sockets from 1 to 2048. The results are shown for a single-qubit gate applied to qubits 0-28 of the 29-qubit system. The results for qubits 0-14 are similar to the results for the 15th qubit and we omit them for brevity.

We see that on 4 sockets we achieve almost linear speedup of  $4\times$  over a single socket, when the gate is applied to qubits 15 to 26, since there is no communication. Qubits 27 and 28,

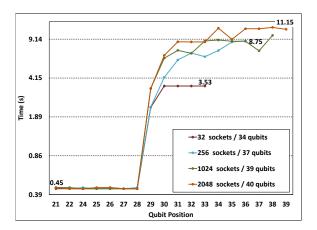


Figure 9: Multinode weak scaling of a single-qubit operation. Results are shown for gate operation on qubits 21-39. Results for qubits 0-20 are similar to the results for qubit 21 and are thus omitted.

on the other hand, require inter-socket communication. This results in  $2\times$  slow-down, compared to a single socket, whose performance is memory bound. This is expected. When communication is required, the performance is limited by network bandwidth, which is  $\approx 7.2\times$  lower than memory bandwidth (see Section 5.2). As the result, the  $7.2\times$  slow-down negates the expected  $4\times$  speedup, and results in a slowdown of  $0.5\times$  ( $\approx$  4/7.2).

We observe almost linear speedup for 32 and 128 sockets when no communication is required, followed by the commensurate drop in speedup when sockets have to communicate. However, in contrast to 4-socket case, the larger number of nodes overcompensates for performance drop due to lower network bandwidth, and as the result we observe speedups of  $2.4\times$  and  $9.3\times$ , on 32 and 128 sockets, respectively.

For 2048 sockets we observe superlinear speedup for qubits 15, 16, and 17. For example, speedup for qubit 17 is  $3331\times$ , an additional factor of  $1.6\times$  over linear speedup of 2048. This is also expected. As we increase number of sockets, the state size per socket decreases. In particular, on 2048 sockets the state occupies only 4.2MB of memory per socket (=  $2^{29+4-11}$ ), and thus fits into LLC. As described in Section 5.3, LLC-bound performance is  $2\times$  higher than memory bound performance of a single node, which results in commensurate performance gains at scale.

Weak Scaling: Figure 9 shows a single-qubit gate operation on multiple nodes. We report time per gate for 32, 256, 1K, and 2K sockets, which enable simulating quantum systems with 32, 37, 39, and 40 qubits, respectively. Note this is a weak scaling experiment. Specifically, we fix the local state vector to use maximum amount of memory available on a socket. As we increase number of qubits, we also use more sockets, and as the result the size of local state vector on a socket remains the same.

Gate operations applied to qubits 0-29 require no communication for all four quantum systems, and achieve the performance of  $\approx 0.44s$  per gate, which is very close to the memory bound of 0.43 seconds (Table 2, Case 1). Gates

	Target Qubit													
		27	28	29	30	31	32	33	34	35	36	37	38	39
c	27		0.25	3.14	6.12	6.61	8.97	11.22	11.01	10.93	13.98	11.37	13.95	13.61
	28	0.23		3.36	5.86	6.95	9.44	11.34	11.25	10.96	14.05	11.72	14.09	13.83
0	29	0.44	0.45		3.25	3.70	4.98	5.94	5.85	5.76	7.28	6.06	7.31	7.14
n	30	0.48	0.45	3.36		5.77	6.24	8.50	8.49	11.01	13.60	11.56	12.49	11.40
t r	31	0.45	0.45	3.36	4.71		6.61	8.55	7.41	6.87	8.85	9.32	7.19	11.10
0	32	0.51	0.51	3.47	5.98	5.92		7.59	9.35	6.86	8.82	8.58	9.52	11.06
ï	33	0.50	0.49	3.47	4.94	6.87	6.53		8.80	10.40	11.03	8.97	14.12	9.69
	34	0.45	0.44	3.36	6.13	6.78	9.55	9.69		8.43	11.17	8.65	8.86	8.73
Q	35	0.45	0.45	3.36	5.93	6.88	8.85	9.80	8.90		11.26	11.20	9.39	11.07
u	36	0.45	0.45	3.36	5.82	6.07	8.90	11.21	11.22	8.66		11.43	14.16	13.82
b	37	0.45	0.44	3.39	4.67	6.05	9.04	8.79	8.91	8.60	11.29		9.37	11.17
i	38	0.45	0.45	3.36	5.98	6.08	9.44	11.39	11.15	11.08	14.20	11.59		13.81
t	39	0.45	0.45	3.36	4.98	6.89	9.05	11.33	11.26	8.66	10.04	11.61	14.20	

Figure 10: Time per controlled qubit gate using 40 qubits on 1,024 compute nodes.

applied to higher qubits require communication. For the 32-node configuration we consistently see  $\approx 3.53$ s per gate which is within 88% from network bound of 3.12 seconds (Table 2, Case 2). As the number of nodes increases, time per gate also increases, compared to the network bound. For example, gate operations applied to qubit 35 on 256-nodes configuration takes 8.7 second, which is  $2.5 \times$  increase, compared to network bound. There are two reasons for such steep increase in time per gate. First, this is due to network contention. The Stampede system uses a two-level Clos fat-tree topology [13] with 20 nodes (40 sockets) to the first-level switches. As a result, sockets which are more than 40 sockets apart will communicate via second-level switches. The second level switches have lower bandwidth than first level switches, thus resulting in contention and increase in run-time. Simulations using 256, 1K and 2K sockets span multiple first-level switches. This requires communicating via second-level switched, and thus results in increased contention among communicating sockets<sup>4</sup>. In addition, there is interference with other jobs running on the system at the same time, as observed by some time variability between runs in our experiments. In the worst case, for 2K nodes, time per gate goes up to 11.15 seconds, which corresponds to  $3.5 \times (11.15/3.12)$  increase in time per gate, compared to network bound.

Finally, Figure 10 shows time per controlled gate operation for a 40 qubit circuit, simulated on 2K sockets. We only present the results for values of control and target qubits in the range of 27-39 (see Figure 5 for other combinations of c and t). The results follow general trends similar to a single-qubit operation, discussed above. For example, Case 4 in Table 2 shows the memory bound of 0.43 seconds when t < n, c < n. This matches the second columns of the table  $(t=28 \ {\rm and} \ c$  in the range 29-39), as expected. Similar to single-qubit operation, when communication is required, the time per controlled gate can go as high as 14 seconds, which is a  $4.5\times$  increase compared to network bound (Table 2).

		Total	Time per
nqubits	ngates	Time (s)	Gate (s)
29	435	116.6	0.27
30	465	141.6	0.30
31	496	167.9	0.34
32	528	200.9	0.38
33	561	245.0	0.44
34	595	297.4	0.50
35	630	339.7	0.54
36	666	445.4	0.67
37	703	540.2	0.77
38	741	643.8	0.87
39	780	766.1	0.98
40	820	997.2	1.22

Table 3: Performance of Quantum Fourier Transform (QFT) for 29-40 qubits. The second column shows total number of gates in a single QFT call. The third column shows total time per single QFT call. Column four shows average time per gate.

## 5.5 Performance of OFT

Finally, we report the performance of *Quantum Fourier Transform* (QFT). QFT is fundamental kernel of many quantum algorithms, such as Shor's algorithm for factoring [37], the quantum phase estimation algorithm for estimating the eigenvalues of a unitary operator [22], and algorithms for the hidden subgroup problem [25]. The QFT circuit is similar to the one for Inverse QFT (see Figure 6), except the order of qubits is reversed.

Table 3 shows the performance of QFT as the number of qubits varies from 29 to 40. Gate fusion was not used in these experiments. Note this is also a weak scaling experiment, as the size of the local state vector per node is fixed to be  $2^{29}$  complex amplitudes. We see that total QFT time varies from 116 seconds for 29 qubits up to 997 seconds for 40 qubits. This  $9\times$  increase in run time is due to the fact that some of the gate operations become network bound, as was explained in previous section. On average, for 40 qubits, each QFT gate operations takes  $\approx 1.22$  seconds, as shown in the last column of Table 3.

Understanding run-time requirements of a quantum algorithm is important, as it allows one to gauge the circuit complexity that can be simulated on an HPC system. For example, on Stampede cluster, a single user application is limited to a maximum run-time of 24 hours. For a 40-qubit system, this would allow  $\approx 86~(24\times3600/997)$  calls to QFT for the total of  $\approx 70,000$  quantum gates.

#### 6. FUTURE DIRECTIONS

The practical limit on the size of the quantum system that can be simulated in the next six years is 49 qubits, and can not be overcome for general-purpose circuit simulations, due to exponentially large memory requirements for storing the entire state vector.

The performance of a quantum simulator is limited by memory and especially network bandwidth. Recently introduced high bandwidth memory (HBM) delivers up to an order of magnitude more bandwidth than more tradi-

<sup>&</sup>lt;sup>4</sup>With topology-aware job placement, traffic on second-level switches can be prevented for gate operations on lower-order qubits that require communication. However, on a busy HPC cluster, job scheduler typically tries to maximize overall throughput, rather than individual job latency. As a result, it assigns jobs to the available CPUs, giving only secondary consideration to the job placement that minimizes the contention.

tional DRAM<sup>5</sup> [21] and is gaining wide traction in commercial computer systems. Network bandwidth has also been improving, but at a more modest rate of 26% per year. More concretely, an upcoming NERSC Cori Phase-2 system, a Cray system based on the second generation of Intel®Xeon Phi<sup>TM</sup>Product Family, will have an on-package, high-bandwidth memory, up to 16GB capacity and > 400 GB/s bandwidth [3]. The system will also employ the Cray Aries high speed dragonfly topology interconnect. These technological trends will result in performance improvement of quantum simulators.

However, the network contention challenge observed in the Stampede system will be inherent to low-diameter multilevel networks, such as dragonfly [20], widely believed to be scalable topology for exascale systems. On such networks, when gate operations affect high-order qubits, communicating processors are separated by a longer stride, which will cause congestion on the global links. This limits the overall performance of the simulator.

Major opportunities for further accelerating qHiPSTERcomes from communication-avoiding approaches. These approaches combine ideas of cache blocking, described in Section 4.4, and state reordering. Cache blocking using gate fusion reduces the amount of memory traffic, but the fusion opportunities are circuit-specific and limited in scope. State reordering, on the other hand, exposes additional fusion opportunities, as described in [40]. Specifically, qubit reordering permutes the state in such a way that high-order qubits, which require inter-node communication, become low-order qubits, thus avoiding communication for quantum gates that operate on these qubits. The main challenge is to maximize reordering opportunities for a given quantum circuit, while minimizing computational overhead of reordering. Lastly, we note that reordering optimization may allow for storing the state vector in a higher capacity secondary device, such as disk, while reducing the cost of data transfers to and from main memory. In principle, this could enable quantum simulations with more than 49 qubits.

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