17/05/19 FN

Reg. No. :

Question Paper Code : 80098

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2019.

Fourth Semester

Computer Science and Engineering

CS 8491 – COMPUTER ARCHITECTURE

(Common to Information Technology/Computer and Communication Engineering)

(Regulation 2017)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Define Amdahl's law.
2. Suppose that we are considering an enhancement to the processor of a server system used for Web Serving. The new CPU is 10 times faster on computation in the Web serving application than the original processor. Assuming that the original CPU is busy with computation 40% of the time and is waiting for I/O 60% of the time, what is the overall speedup gained by incorporating the enhancement?
3. Convert $(1.00101)_2$ to decimal.
4. Perform subtraction by two's complement method : 100 – 110000.
5. Convert the following code segment in C to MIPS instructions, assuming all variables are in memory and are addressable as offsets from $t0:

   $a = b + e;$ $c = b + f;$
6. Write down the five stages of instruction executions.
7. List the four multicore systems.
8. What is shared memory multiprocessor?
9. Draw the basic structure of a memory hierarchy.
10. How many total bits are required for a direct-mapped cache with 16KB of data and 4-word blocks, assuming a 32-bit address?

PART B — (5 × 13 = 65 marks)

11. (a) (i) Describe the different types of addressing mode with example. (7)

(ii) Explain the components of a computer with the block diagram in detail. (6)

Or

(b) (i) Explain the eight ideas of the Computer architecture which empowered the computer design over the past decades. (7)

(ii) Tabulate the difference between the RISC and CISC processor. (6)

12. (a) Calculate the following problems using BOOTH'S ALGORITHM (13)

(i) (+13) × (–6)

(ii) (+13) × (+6)

(iii) (–13) × (–6)

(iv) (-13) × (+6)

Or

(b) Calculate 10011 (–13) × 01011 (+11) using Signed-Operand Multiplication. (13)

13. (a) Explain the basic MIPs implementation with necessary multiplexers and control lines. (13)

Or

(b) Explain how the instruction pipeline works? What are the various situation where an instruction pipeline stalls? Illustrate with an example. (13)

14. (a) Explain in detail Flynn's classification of parallel hardware. (13)

Or

(b) Discuss the principle of hardware multithreading and elaborate its types. (13)

15. (a) Explain the various mapping functions that can be applied on cache memories in detail. (13)

Or

(b) (i) With a neat sketch explain the working principle of DMA. (8)

(ii) Explain about input-output processor (IOP) (5)

PART C — (1 × 15 = 15 marks)

16. (a) In a small town, there are three temples in a row and a well in front of each temple. A pilgrim came to the town with certain number of flowers.

Before entering the first temple, he washed all the flowers he had with the water of well. To his surprise, flowers doubled. He offered few flowers to the God in the first temple and moved to the second temple. Here also, before entering the temple he washed the remaining flowers with the water of well. And again his flowers doubled. He offered few flowers to the God in second temple and moved to the third temple. Here also, his flowers doubled after washing them with water. He offered few flowers to the God in third temple.

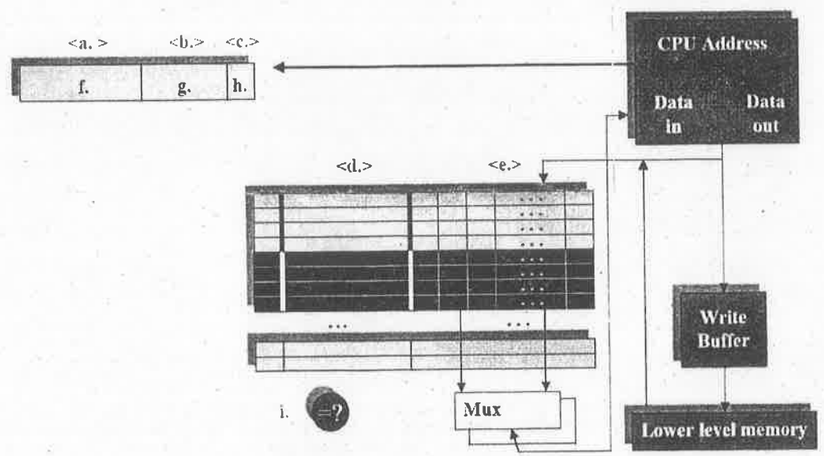
There were no flowers left when pilgrim came out of third temple and he offered same number of flowers to the God in all three temples. What is the minimum number of flowers the pilgrim had initially (X)? And find the value of (X/3) using Restoring Division method? How many flower did he offer to each God (Y)? And find the value of (Y/3) using Non-Restoring Division method? (15)

Or

(b) (i) You have been asked to design a cache with the following properties : (8)

(1) Data words are 32 bits each
(2) A cache block will contain 2048 bits of data
(3) The cache is direct mapped
(4) The address supplied from the CPU is 32 bits long
(5) There are 2048 blocks in the cache
(6) Addresses are to the word.

(ii) In the below picture, there are 8 fields (labeled a, b, c, d, e, f, g, and h), you will need to indicate the proper name or number of bits for a particular portion of this cache configuration. Explain the process of accessing data using this design. (7)



8/11/19/AN

Reg. No. :

Question Paper Code : 90155

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2019

Fourth/Fifth Semester

Computer Science and Engineering

CS8491 – COMPUTER ARCHITECTURE

(Common to : Robotics and Automation Engineering/Computer and Communication Engineering/Information Technology)

(Regulations 2017)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A (10×2=20 Marks)

1. What is register indirect addressing mode ? When it is used ?
2. Define word length.
3. What is half adder ?
4. What are the main features of Booth's algorithm ?
5. Define datapath in the processor unit.
6. What is the role of cache memory in pipeline ?
7. What do you mean by static memories ?
8. Define Hit and Miss in cache.
9. What is Flynn's classification ?
10. What are the properties of Multi-Core Systems ?

PART – B (5×13=65 Marks)

11. a) Explain in detail the various components of computer system with neat diagram.

(OR)

b) Mr. Thomas has got a new laptop, at memory address 101 Add A, B instruction is residing. How will the processor fetch the instruction from the memory and execute the instruction based on various registers in the CPU. Also draw the architectural diagram for the above scenario.

12. a) Mr. John has been assigned a project by his Team Leader in ALS Technologies. His project is to design an algorithm for two's complement division using addition and subtraction operations. Help Mr. John in designing an algorithm by sketching the flowchart for restoring division and also check the working of it with the following numbers : 21 ÷ 4.

(OR)

b) Mr. David is Processor Designer at IBM and he is visiting your college for an internship interview. During the interview Mr. David asks you to sketch the flow chart for floating point multiplication and also check the working of it with the following numbers : $X = 4.5_{(10)}$ and $Y = 11.25_{(10)}$. Provide an appropriate solution.

13. a) Explain data path and its control in detail.

(OR)

b) What is pipelining ? Discuss about pipelined data path control.

14. a) Discuss about SISD, MIMD, SIMD, SPMD and vector systems.

(OR)

b) What is hardware multithreading ? Compare and contrast fine grained multi-threading and coarse grained multi-threading.

15. a) Consider a cache of 256 blocks in size, each block has 2^4 words. The main memory size is 2^{12} blocks, each block has 2^4 words. How many bits are required for each of the TAG, SET/BLOCK and WORD FIELDS for different mapping techniques ? Wherever needed assume that there are 8 ways in each set.

(OR)

b) Consider a system which transfers 2 MB file from memory to pendrive.

i) If memory is using Handshaking Protocol to send the file, depict clearly how the data transfer takes place in case of source initiated and destination initiated data transfer. **(7)**

ii) When the file is being transferred there should be minimal intervention of the processor. Suggest a suitable technique for the above operation and explain it with proper justification and diagrams. **(6)**

PART – C **(1×15=15 Marks)**

16. a) What is an addressing mode ? Explain the various addressing modes with suitable examples.

(OR)

b) Explain in detail about centralized shared memory and distributed memory multiprocessor.

Reg. No. | | | | | | | | | | | | |

4/6/16 AN

Question Paper Code : 57241

B.E/B.Tech. DEGREE EXAMINATION, MAY/JUNE 2016

Sixth Semester

Electronics and Communication Engineering

CS 6303 – COMPUTER ARCHITECTURE

(Common to Information Technology)

(And also common to Fifth Semester Elective – Electronics and Instrumentation Engineering, Instrumentation and Control Engineering, Fifth Semester – Robotics and Automation Engineering and Third Semester Computer Science and Engineering)

(Regulations 2013)

Time : Three Hours **Maximum : 100 Marks**

Answer ALL questions.

PART – A (10 × 2 = 20 Marks)

1. How to represent Instruction in a Computer System ?
2. Distinguish between auto increment and auto decrement addressing mode.
3. Define ALU.
4. What is Subword Parallelism ?
5. What are the advantages of pipelining ?
6. What is Exception ?
7. State the need for Instruction Level parallelism.
8. What is Fine grained Multithreading ?
9. Define Memory hierarchy.
10. State the advantages of virtual memory.

PART – B (5 × 16 = 80 Marks)

11. (a) Discuss about the various components of a computer system. **(16)**

OR

(b) Elaborate the different types of addressing modes with a suitable example. **(16)**

12. (a) Explain briefly about floating point addition and Subtraction algorithms. **(16)**

OR

(b) Define Booth Multiplication algorithm with suitable example. **(16)**

13. (a) What is pipelining ? Discuss about pipelined data path and control. **(16)**

OR

(b) Briefly explain about various categories of hazards with examples. **(16)**

14. (a) Explain in detail about Flynn's classification. **(16)**

OR

(b) Write short notes on : **(16)**

(i) Hardware multithreading

(ii) Multicore processors.

15. (a) Define Cache Memory ? Explain the Various Mapping Techniques associated with cache memories. **(16)**

OR

(b) Explain about DMA controller, with the help of a block diagram. **(16)**

Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 71675

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2017

Third/Fifth/Sixth Semester

Computer Science and Engineering

CS 6303 — COMPUTER ARCHITECTURE

(Common to Electronics and Communication Engineering , Electronics and Instrumentation Engineering, Instrumentation and Control Engineering, Robotics and Automation Engineering, Information Technology)

(Regulations 2013)

Time : Three hours • Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. List the major components of a computer system.
2. State the need for indirect addressing mode. Give an example.
3. Subtract $(11010)_2 - (10000)_2$ using 1's complement and 2's complement method.
4. Write the rules to perform addition on floating point numbers.
5. Name the control signals required to perform arithmetic operations.
6. Define hazard. Give an example for data hazard.
7. What is instruction level parallelism?
8. Distinguish implicit multithreading and explicit multithreading.
9. Define memory interleaving.
10. Summarize the sequence of events involved in handling an interrupt request from a single device.

PART B — (5 × 13 = 65 marks)

11. (a) Explain the important measures of the performance of a computer and derive the basic performance equation. (13)

Or

(b) Explain direct, immediate, relative and indexed addressing modes with examples. (13)

12. (a) (i) Demonstrate multiplication of two binary numbers with an example. Design an arithmetic element to perform this multiplication. (7)

(ii) Describe non restoring division with an example. (6)

Or

(b) (i) Design an arithmetic element to perform the basic floating point operations. (7)

(ii) What is meant by sub word parallelism? Explain. (6)

13. (a) Discuss the modified data path to accommodate pipelined executions with a diagram. (13)

Or

(b) (i) Explain the hazards caused by unconditional branching statements. (7)

(ii) Describe operand forwarding in a pipeline processor with a diagram. (6)

14. (a) (i) Discuss the challenges in parallel processing with necessary examples. (6)

(ii) Explain Flynn's classification of parallel processing with necessary diagrams. (7)

Or

(b) Explain the four principal approaches to multithreading with necessary diagrams. (13)

15. (a) Explain the different mapping functions that can be applied on cache memories in detail. (13)

Or

(b) (i) Explain virtual memory address translation in detail with necessary diagrams. (7)

(ii) What is meant by Direct Memory Access? Explain the use of DMA controllers in a computer system. (6)

PART C — (1 × 15 = 15 marks)

16. (a) (i) Explain mapping functions in cache memory to determine how memory blocks are placed in cache. (8)

(ii) Explain in detail about the Bus Arbitration techniques in DMA. (7)

Or

(b) A pipelined processor uses delayed branch technique. Recommend any one of the following possibility for the design of the processor. In the first possibility, the processor has a 4-stage pipeline and one delay slot. In the second possibility, it has a 6-stage pipeline and two delay slots. Compare the performance of these two alternatives, taking only the branch penalty into account. Assume that 20% of the instructions are branch instructions and that an optimizing compiler has an 80% success rate in filling in the single delay slot. For the second alternative, the compiler is able to fill the second slot 25% of the time.

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Reg. No. :

Question Paper Code : 40902

05/05/18

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2018
Third/Fifth/Sixth Semester
Computer Science and Engineering
CS 6303 – COMPUTER ARCHITECTURE
(Common to : Electronics and Communication Engineering/Electronics and Instrumentation Engineering/Instrumentation and Control Engineering/Robotics and Automation Engineering/Information Technology)
(Regulations 2013)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. Write the equation for the dynamic power required per transistor.
2. Classify the instructions based on the operations they perform and give one example to each category.
3. Show the IEEE 754 binary representation of the number $(-0.75)_{10}$ in single precision.
4. Define a datapath in a CPU.
5. What is the ideal CPI of a pipelined processor ?
6. What is meant by exception ? Give one example of MIPS exception.
7. Protein String Matching Code has 4 days execution time on current machine doing integer instructions in 20% of time, doing I/O in 35% of time and other operations in the remaining time. Which is the better tradeoff among the following two proposals ? First : Compiler optimization that reduces number of integer instructions by 25% (assume each integer instruction takes the same amount of time); Second : Hardware optimization that reduces the latency of each IO operations from 6μs to 5μs.
8. Give example for each class in Flynn's classification.
9. Distinguish SRAM and DRAM.
10. What is the use of DMA Controller ?

PART – B (5×13=65 Marks)

11. a) i) Consider three different processors P1, P2 and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2.

a) Which processor has the highest performance expressed in instructions per second ?

b) If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions in each processor. (5)

ii) Explain in detail the components of a computer system. (8)

(OR)

b) i) Translate the following C code to MIPS assembly code. Use a minimum number of instructions. Assume that i and k correspond to registers $s3 and $s5 and the base of the array save is in $s6. What is the MIPS assembly code corresponding to this C segment ?

```
while (save[i] = = k)
i + = 1;
```

(5)

ii) What is an addressing mode in a computer ? Classify MIPS addressing modes and give one example instruction to each category. (8)

12. a) i) Perform X + Y and Y – X using 2's complements for given the two binary numbers X = 0000 1011 1110 1111 and Y = 1111 0010 1001 1101. (5)

ii) Multiply the following signed 2's compliment numbers using the Booth algorithm. A = 001110 and B = 111001 where A is multiplicand and B is multiplier. (8)

(OR)

b) i) Draw the block diagram of integer divider and explain the division algorithm. (5)

ii) Add the numbers $(0.75)_{10}$ and $(-0.275)_{10}$ in binary using the Floating point addition algorithm. (8)

13. a) Design a simple datapath with the control unit and explain in detail. (13)

(OR)

b) Discuss the limitations of pipelining a processor's datapath. Suggest the methods to overcome them. (13)

14. a) i) List the limitations of instruction level parallelism. (5)

ii) What are the challenges in parallel processing ? (8)

(OR)

b) i) Compare and contrast fine-grained multi-threading, coarse-grained multi-threading and simultaneous multi-threading. (9)

ii) Classify shared memory multiprocessor based on the memory access latency. (4)

15. a) i) What is the need for Cache memory ? List the three mapping methods of Cache memory and explain any two. (10)

ii) Define virtual memory. What is the advantage of using virtual memory ? (3)

(OR)

b) i) Discuss about Programmed I/Os associated with computers. (6)

ii) Write the sequence of operations carried out by a processor when interrupted by a peripheral device connected to it. (7)

PART – C (1×15=15 Marks)

16. a) The following sequence of instructions are executed in the basic 5-stage pipelined processor :

```
or r1, r2, r3
or r2, r1, r4
or r1, r1, r2
```

a) Indicate dependences and their type.

b) Assume there is no forwarding in this pipelined processor. Indicate hazards and add NOP instructions to eliminate them.

c) Assume there is full forwarding. Indicate hazards and add NOP instructions to eliminate them. (15)

(OR)

b) Explain the detail of DMA control with suitable diagrams. Discuss how it improve the overall performance of the system. (15)

2/5/19 AN

Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 52859

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2019.

Third/Fifth/Sixth Semester

Computer Science and Engineering

CS 6303 – COMPUTER ARCHITECTURE

(Common to: Electronics and Communication Engineering/Electronics and Communication Engineering/Electronics and Instrumentation Engineering/Instrumentation and Control Engineering/Robotics and Automation Engineering /Information Technology)

(Regulation 2013)

Also common to PTCS 6303 – Computer Architecture for Computer Science and Engineering (Fifth Semester – Regulation 2014)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Write the components of a computer system and list their functions.
2. Give the MIPS code for the statement f = (g + h) - (i + j).
3. State the rules to add two integers.
4. Define scientific notation and normalized notation.
5. Define edge triggered clocking.
6. Identify the hazards with respect to a processor function.
7. Neatly sketch the three primary units of dynamically scheduled pipeline.
8. Define speculation with example.
9. What is miss penalty?
10. How many total bits are required for a direct-mapped cache with 16 KB of data and 4-word blocks, assuming a 32-bit address?

PART B — (5 × 13 = 65 marks)

11. (a) Explain how performance is calculated in a computer system and derive the necessary performance equations.

Or

(b) Explain how instructions that involve decision making are executed with an example.

12. (a) Discuss how ALU performs division with the flow chart and the block diagram.

Or

(b) Explain floating point addition with a neat block diagram of ALU unit.

13. (a) Explain the process of building a single data–path with a neat diagram.

Or

(b) Explain data hazards and stalls with neat diagrams and suitable examples.

14. (a) Explain Flynn's classification with neat diagrams.

Or

(b) Explain hardware multithreading with neat diagrams.

15. (a) Explain the process of measuring the performance of cache memory with required metrics?

Or

(b) Explain the virtual memory organization followed in digital computers.

PART C — (1 × 15 = 15 marks)

16. (a) (i) Assume a two address format specified as source, destination. Examine the following sequence of instructions and explain the addressing modes used and the operation done in every instruction.

(1) Move (R5)+,R0

(2) ADD (R5)+,R0

(3) MOVE RO, (R5)

(4) Move 16(R5), R3

(5) Add #40, R5 (5)

(ii) Consider the following code segment in C:

a = b + e;

c = b + f;

Here is the generated MIPS code for this segment, assuming all variables are in memory and are addressable as off sets from $t0:

```
lw   $t1,  0($t0)
lw   $t2,  4($t0)
add  $t3,  $t1,$t2
sw   $t3,  12($t0)
lw   $t4,  8($t0)
add  $t5,  $t1,$t4
sw   $t5,  16($t0)
```

Find the hazards in the preceding code segment and reorder the instructions to avoid any pipeline stalls? (10)

Or

(b) (i) Analyze the merits and demerits of microprogrammed control over hardwired control. (7)

(ii) Analyze and tabulate the major features of programmed I/O, DMA and interrupts. (8)

Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 80289

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2016.

Sixth Semester

Electronics and Communication Engineering

CS 6303 — COMPUTER ARCHITECTURE

(Common to Third Semester Information Technology and Computer Science and Engineering)

(Regulations 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is an instruction register?

2. Give the formula for CPU execution time for a program.

3. What is a guard bit and what are the ways to truncate the guard bits?

4. What is arithmetic overflow?

5. What is meant by pipeline bubble?

6. What is a data path?

7. What is instruction level parallelism?

8. What is multithreading?

9. What is meant by address mapping?

10. What is cache memory?

PART B — (5 × 13 = 65 marks)

11. (a) Explain in detail the various components of computer system with neat diagram.

Or

(b) Explain the different types of Addressing modes with suitable examples.

12. (a) Explain Booth's Algorithm for the multiplication of signed two's complement numbers.

Or

(b) Discuss in detail about division algorithm in detail with diagram and examples.

13. (a) Why is branch prediction algorithm needed? Differentiate between the static and dynamic techniques.

Or

(b) Explain how the instruction pipeline works. What are the various situations where an instruction pipeline can stall?

14. (a) Explain in detail about Flynn's classification of parallel hardware.

Or

(b) Discuss Shared memory multiprocessor with a neat diagram.

15. (a) Discuss DMA controller with block diagram.

Or

(b) Discuss the steps involved in the address translation of virtual memory with necessary block diagram.

PART C — (1 × 15 = 15 marks)

16. (a) What is the disadvantage of Ripple carry addition and how it is overcome in carry look ahead adder and draw the logic circuit CLA.

Or

(b) Design and explain a parallel priority interrupt hardware for a system with eight interrupt sources.

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Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 50384

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2017
Third/Fifth/Sixth Semester
Computer Science and Engineering
CS6303 – COMPUTER ARCHITECTURE
Common to : Electronics and Communication Engineering, Electronics and Instrumentation Engineering, Instrumentation and Control Engineering, Robotics and Automation Engineering, Information Technology
(Regulations 2013)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A (10×2=20 Marks)

1. What are components of a computer system ?
2. What are the addressing modes ?
3. Subtract $(11011)_2 - (10011)_2$ using 2's complement.
4. Devide $(1001010)_2 \div (1000)_2$.
5. Mention the various types of pipelining.
6. Mention the various phase in executing an instruction.
7. Define strong scaling and weak scaling.
8. Difference between Fine-grained multithreading and Coarse-grained multithreading.
9. What is virtual memory ?
10. How many total bits are required for a direct-mapped cache with 16 KB of data and 4-word blocks, assuming a 32-bit address ?

PART – B (5×13=65 Marks)

11. a) Explain various instruction formats and illustrate the same with an example. (13)

(OR)

b) Explain with an example about the operations and Operands of the Computer Hardware ? (13)

12. a) Illustrate the division algorithm with an example. **(13)**

(OR)

b) i) Add the numbers $(0.5)_{10}$ and $(0.4375)_{10}$ using the floating point addition. **(6½)**

ii) Multiply the numbers $(0.5)_{10}$ and $(0.4375)_{10}$ using the floating point multiplication. **(6½)**

13. a) Explain in detail the operation of the data path. **(13)**

(OR)

b) Explain the pipeline hazard in detail. **(13)**

14. a) Explain with diagrammatic illustration Flynn's classification. **(13)**

(OR)

b) Describe Simultaneous Multithreading (SMT) with an example. **(13)**

15. a) Explain in detail about the memory technologies. **(13)**

(OR)

b) What is cache memory ? How to improve cache performance ? Discuss. **(13)**

PART – C **(1×15=15 Marks)**

16. a) i) Suppose you want to achieve a speed-up of 90 times faster with 100 processors. What percentage of the original computation can be sequential ? **(8)**

ii) Suppose you want to perform two sums : one is a sum of 10 scalar variables and one is a matrix sum of a pair of two-dimensional arrays, with dimensions 10 by 10. For now let's assume only the matrix sum is parallelizable; we'll see soon how to parallelize scalar sums. What speed-up do you get with 10 versus 40 processors ? Next, calculate the speed-ups assuming the matrices grow to 20 by 20. **(7)**

(OR)

b) Assume the miss rate of an instruction cache is 2% and the miss rate of the data cache is 4%. If a processor has a CPI of 2 without any memory stalls and the miss penalty is 100 cycles for all misses, determine how much faster a processor would run with a perfect cache that never missed. Assume the frequency of all loads and stores is 36%. **(15)**

PART C — (1 × 15 = 15 marks)

16. (a) (i) Consider web browsing application. Assuming both client and server are involved in the process of web browsing application, where can caches be placed to speed up the process? Design a memory hierarchy for the system. Show the typical size and latency at various levels of the hierarchy. What is the relationship between cache size and its access latency? What are the units of data transfers between hierarchies? What is the relationship between the data location, data size, and transfer latency?

(ii) The following sequence of instructions are executed in the basic 5-stage pipelined processor:

lw $1, 40($6)

add $6, $2, $2

sw $6, 50($1)

Indicate dependences and their type. Assuming there is no forwarding in this pipelined processor, indicate hazards and add NOP instructions to eliminate them.

Or

(b) Compare hardwired and microprogrammed control unit designs in terms of their mechanism of generating control signals with diagram. (15)

14/11/18

Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 20360

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2018.

Third/Fifth Semester

Computer Science and Engineering

CS 6303 — COMPUTER ARCHITECTURE

(Common to Electronics and Communication Engineering, Electronics and Instrumentation Engineering, Instrumentation and Control Engineering, Robotics and Automation Engineering, Information Technology).

(Regulations 2013)

(Also common to PTCS 6303 Computer Architecture B.E. (Part-Time) Third Semester – Computer Science and Engineering, Electronics and Communication Engineering — Regulations 2014)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Consider three processors P1, P2, and P3 executing the same instruction set. They have clock rates of 3 GHz, 2.5 GHz and 4.0 GHz respectively and CPI of 1.5, 1.0 and 2.2 respectively. Which processor has the highest performance expressed in instructions per second?

2. Classify the instructions based on the operations they perform and give one example to each category.

3. Perform X-Y using 2's complement arithmetic for the given two 16-bit binary numbers X = 0000 1011 1110 1111 and Y = 1111 0010 1001 1101.

4. Define sub-word parallelism.

5. Write the two steps that are common to implement any type of instruction.

6. What is an exception? Give one example for MIPS exception.

7. Web server is to be enhanced with a new CPU which is 10 times faster on computation than old CPU. The original CPU spent 40% of its time processing and 60% of its time waiting for I/O. What will be the overall speedup?

8. Classify shared memory multiprocessor based on the memory access latency.

9. Draw the memory hierarchy in a typical computer system.

10. What is meant by memory–mapped I/O?

PART B — (5 × 13 = 65 marks)

11. (a) (i) Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C, and D). P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3 respectively, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2 respectively. Given a program with a dynamic instruction count of 1.0×10^6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster? What is the global CPI for each implementation? Find the clock cycles required in both cases. (7)

(ii) Explain the three broad classes of applications of computers. (6)

Or

(b) (i) Assume that the variables f and g are assigned to registers \$s0 and \$s1 respectively. Assume that the base address of the array A is in register \$s2. Assume f is zero initially.

$f = -g - A[4]$

$A[5] = f + 100$;

Translate the above C statements into MIPS code. How many MIPS assembly instructions are needed to perform the C statements and how many different registers are needed to carry out the C statements? (5)

(ii) Define addressing mode in a computer. What are the different MIPS addressing modes? Give one example instruction to each category. (8)

12. (a) (i) Multiply the following signed numbers using Booth algorithm. $A = (-34)_{10} = (1011110)_2$ and $B = (22)_{10} = (0010110)_2$ where B is multiplicand and A is multiplier. (6)

(ii) Draw the block diagram of integer divider and explain the division algorithm. (7)

Or

(b) (i) How IEEE 752 32-bit single precision floating print numbers represented? Example. How are print numbers represented? (3)

(ii) Explain floating point addition algorithm with a neat block diagram? (10)

13. (a) Draw a simple MIPS datapath with the control unit and explain the execution of ALU instructions. (13)

Or

(b) (i) A processor has five individual stages, namely, IF, ID, EX, MEM, and WB and their latencies are 250ps, 350ps, 150ps, 300ps, and 200ps respectively. The frequency of the instructions executed by the processor are as follows ; ALU : 40%, Branch : 25%, load : 20% and store:15% What is the clock cycle time in a pipelined and non-pipelined processor? If you can split one stage of the pipelined datapath into two new stages, each with half the latency of the original stage, which stage would you split and what is the new clock cycle time of the processor? Assuming there are no stalls or hazards, what is the utilization of the data memory? Assuming there are no stalls or hazards, what is the utilization of the write-register port of the "Registers" unit? (6)

(ii) List the hazards in pipelining a processor and give one example for each. (7)

14. (a) (i) List the software and hardware techniques to achieve Instruction Level Parallelism (ILP). (4)

(ii) Discuss the challenges in parallel processing in enhancing computer architecture. (9)

Or

(b) (i) Explain any three types of hardware multithreading. (9)

(ii) Define the classes in Flynn's Taxonomy of computer architectures. Give one example for each class. (4)

15. (a) (i) Discuss the three mapping techniques in memory hierarchy. Explain with examples. (10)

(ii) Define Translation Lookaside Buffer (TLB). What is its use? (3)

Or

(b) Explain mechanisms Direct Memory Access and Interrupt handling. (6 + 7)

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Question Paper Code : 91394

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2019

Third/Fifth/Sixth Semester

Computer Science and Engineering

CS 6303 – COMPUTER ARCHITECTURE

(Common to Electronics and Communication Engineering/Electronics and Instrumentation Engineering/Instrumentation and Control Engineering/Robotics and Automation Engineering/Information Technology)

(Regulations 2013)

(Also Common to PTCS 6303 – Computer Architecture for B.E. Part-Time – Computer Science and Engineering – Second Semester, Fifth Semester – Electronics and Communication Engineering – Regulations 2014)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. List the operating systems functions.
2. Define performance.
3. Tell the principle of alignment restriction.
4. Identify the MIPS fields.
5. List the MIPS addressing modes.
6. Define Data Hazards.
7. Identify the MIPS instruction classification.
8. Draw the Program Execution Order.
9. Define Miss Penalty.
10. Tell about the EPC and Cause Register.

PART – B **(5×13=65 Marks)**

11. a) Describe the components of the computer with diagram.

(OR)

b) Explain the various types of addressing modes with example.

12. a) Illustrate about the Signed and Unsigned Numbers.

(OR)

b) Convert Binary to Hexadecimal and back analyze the design principles.

13. a) Analyze the working principles of multiplication operations.

(OR)

b) What are the various types of data hazards ? Explain with example.

14. a) Illustrate about the four states of the simple controller.

(OR)

b) Describe about the instruction level parallelism.

15. a) Explain about DMA and Interrupt with necessary diagram.

(OR)

b) Explain how Cache performance can be measured and improved.

PART – C **(1×15=15 Marks)**

16. a) Analyze the process of reordering the code to avoid pipeline stalls.

(OR)

b) Analyze the compilation of floating-point C procedure with the example of Two-Dimensional Matrices.