Marker-Free Direct-Write Patterning of Quantum Chips

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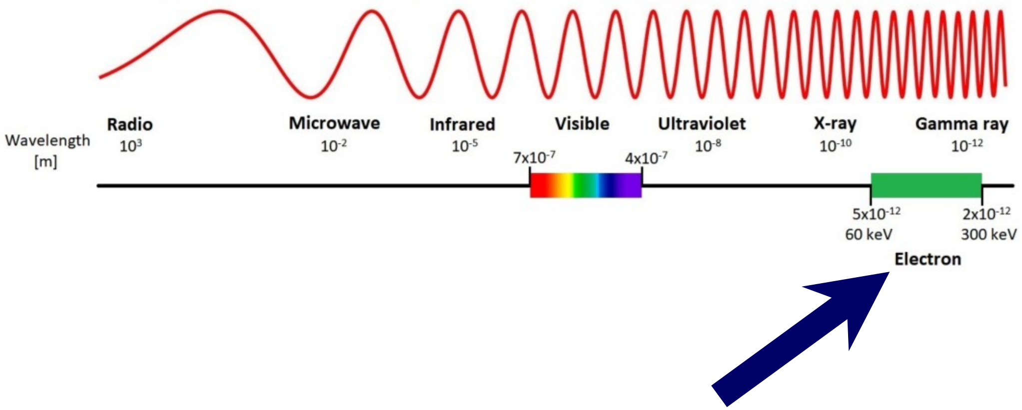
Background & Motivation

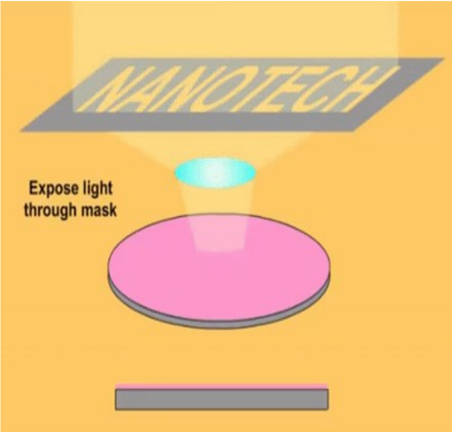
- Reminder that it is generally agreed that **100 nm** or less is considered **nanoscale**.
  - <100 nanometers vertically + micrometer(s) laterally.
  - <100 nanometer dimensions vertically + laterally.
- Making quantum devices involves a balance between:
  - Building up.
  - Tearing down.
  - Inspecting for **desired** or **undesired** defects.
- Focus can be on:
  - (Metals & insulators) or (metals, insulators, & semiconductors).

1. National Nanotechnology Initiative

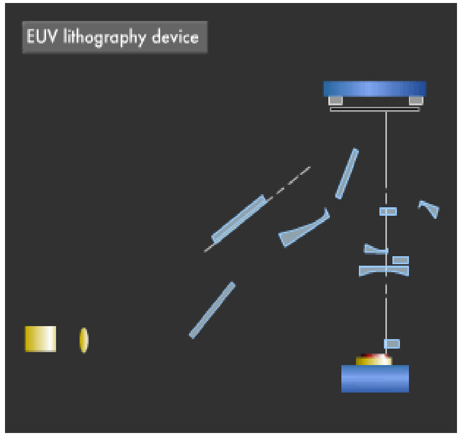
Background & Motivation

- Conventional optical lithography = ultraviolet **photon** exposure.
- Electron beam lithography = **electron** beam exposure.
- Ultimately, the *wavelength* of the energy being applied to a resist coating determines the feature size.
- It's possible to obtain 3-5 nm resolution with electron-beam lithography
  - Depends on your skill level (abstract).

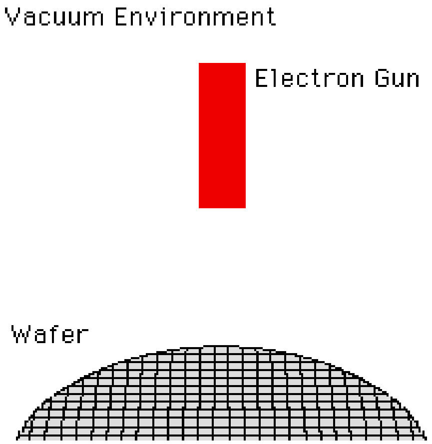




Masked Ultraviolet Lithography



Masked Extreme Ultraviolet Lithography

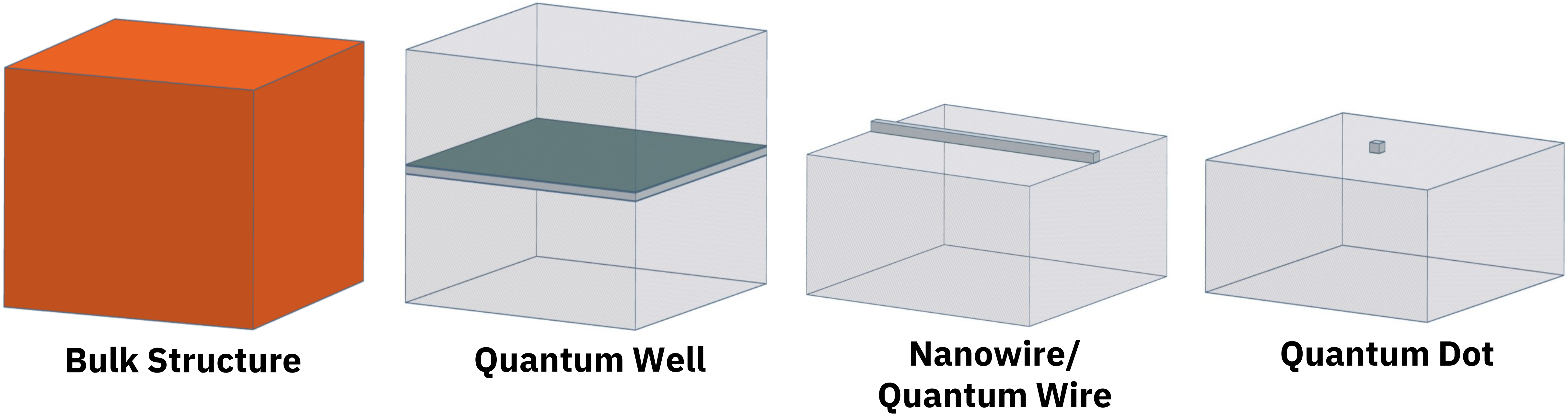


Maskless Electron-Beam Lithography

1. Venturi, *PhD Thesis* (2017)
2. Taken from: thumbs.gfy.com
3. Taken from: *Wikimedia Commons*

Quantum Devices Can Come in Basic Shapes

- In manufacturing, building quantum devices are continuously shaped to achieve desired size.
- A bulk material is selected ➔ nano scale structure ➔ quantum properties exploited.

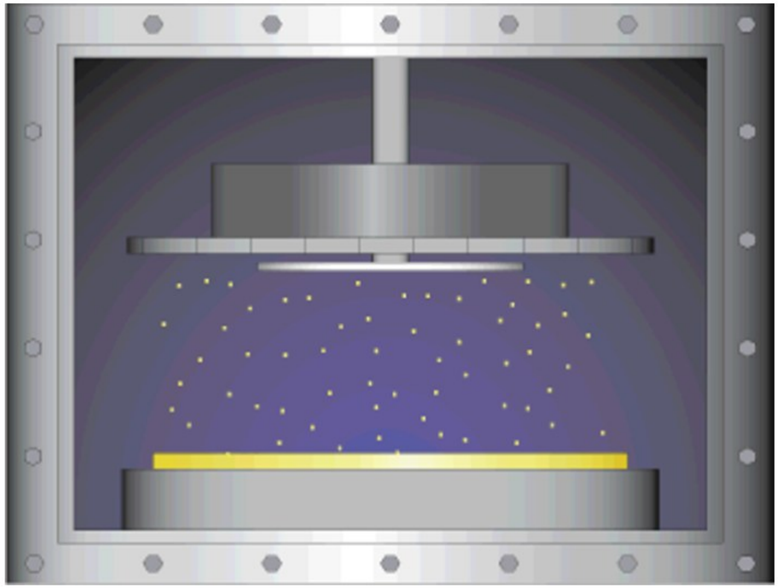


*Leads to quantum confinement

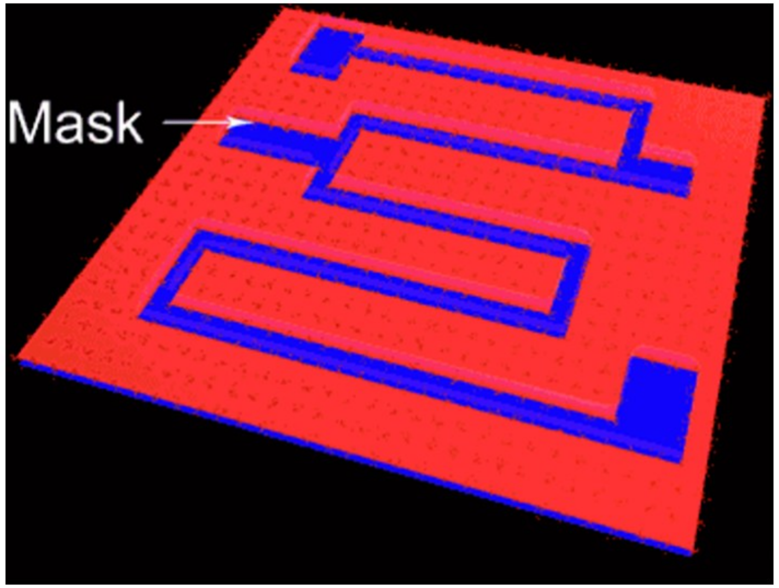
Key Ingredients for Thin Films

- Adhesion layer = “**glue**” between 2 different materials.
    - Ex: For every interface of SiO2 and Au, a metal "glue" layer must be added between.
    - Common adhesion metals: Ti, Cr, Al, Ta, Mo, Nb, V, Hf.
    - 5-10 nm thickness is used to get good adhesion.
- Diffusion barrier = prevents material or impurities from “**melting**” into nearby layers.
- **Coulomb** blockade = filters or blocks out **charge** type.
- Pauli **spin** blockade = filters or blocks out **spin** orientation.
- **Phonon** blockade = filters or blocks out excitation/ **lattice vibration**.
- Bonus 1: seed layer = help with crystalline growth.
- Bonus 2: thermal annealing = reorganizing atoms using heat.

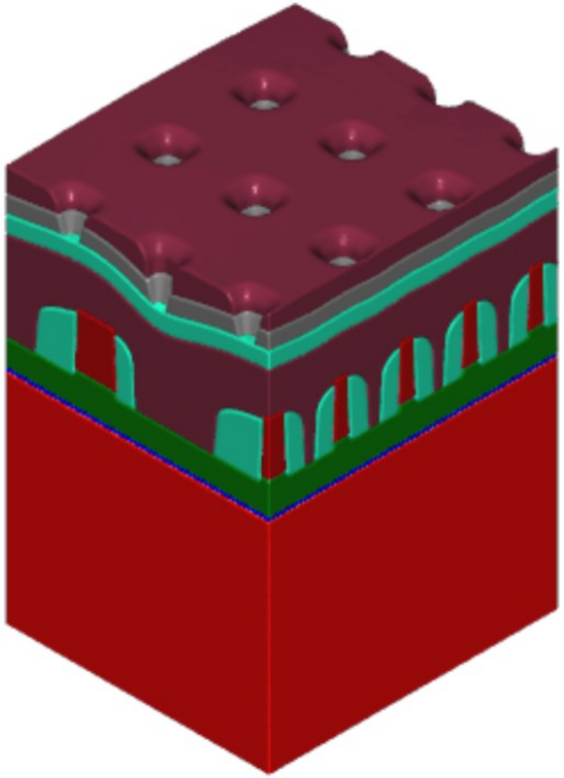
Material Deposition & Etching Visualizations



For depositing or growing materials



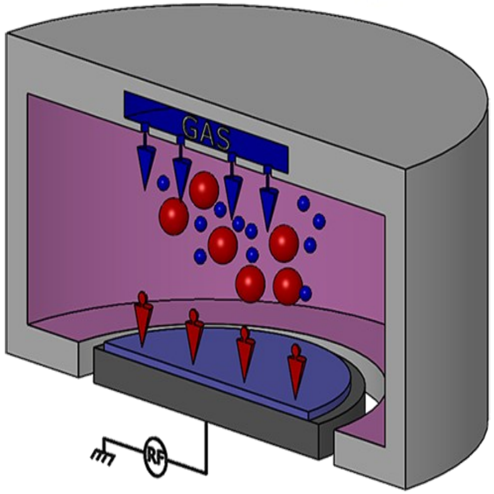
For removing or etching materials

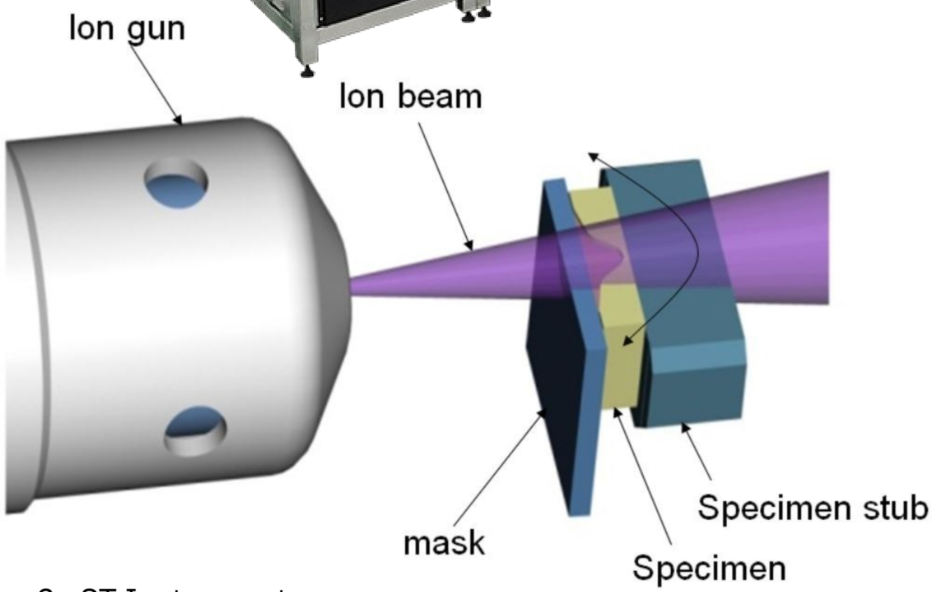


Result

1. *AJA International Inc.*
2. Taken from: tenor.com
3. Taken from: Wikimedia Commons

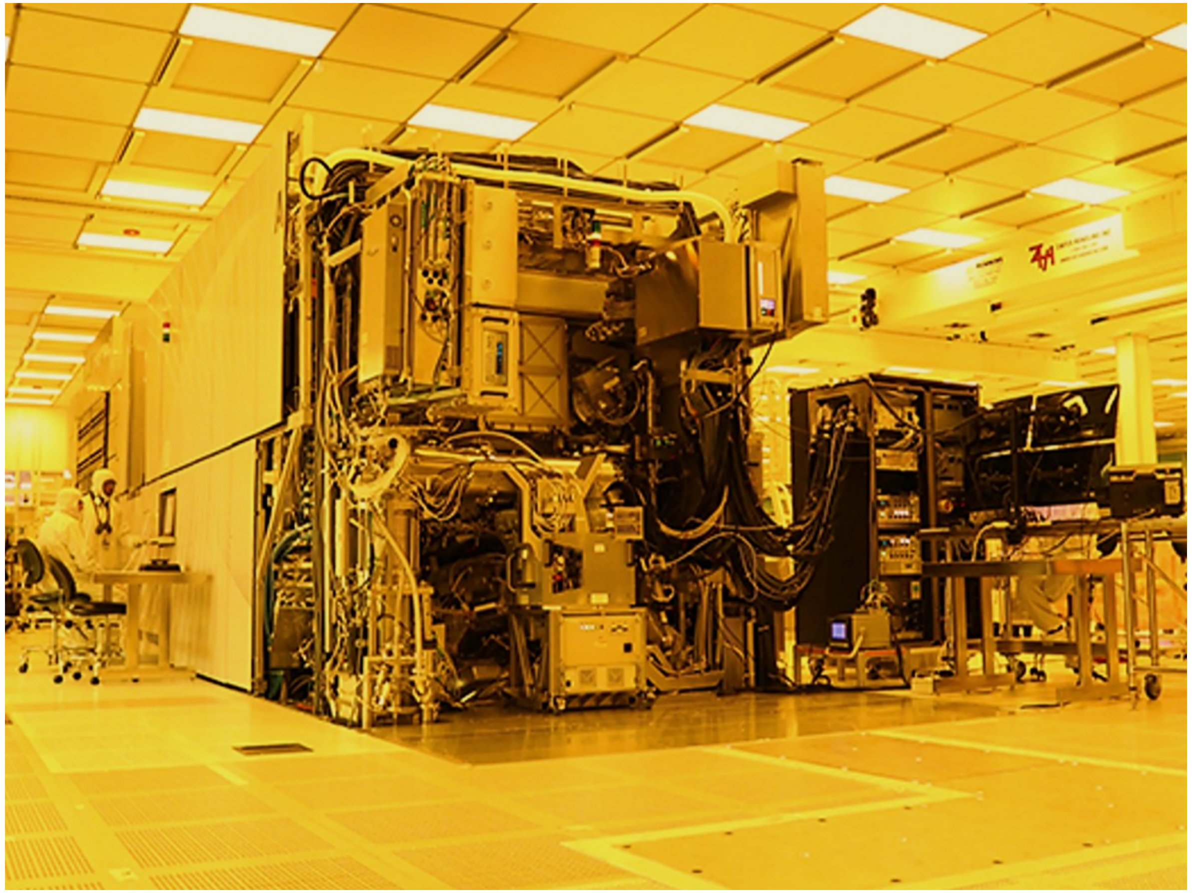
Reactive Ion Etching System vs. Ion Beam Etching System





1. Corial-Plasma-Therm.
2. Intl Vac
3. ST Instruments

Extreme Ultraviolet Lithography System vs. Electron-Beam Lithography System



ASML NXE 3300B (EUV)

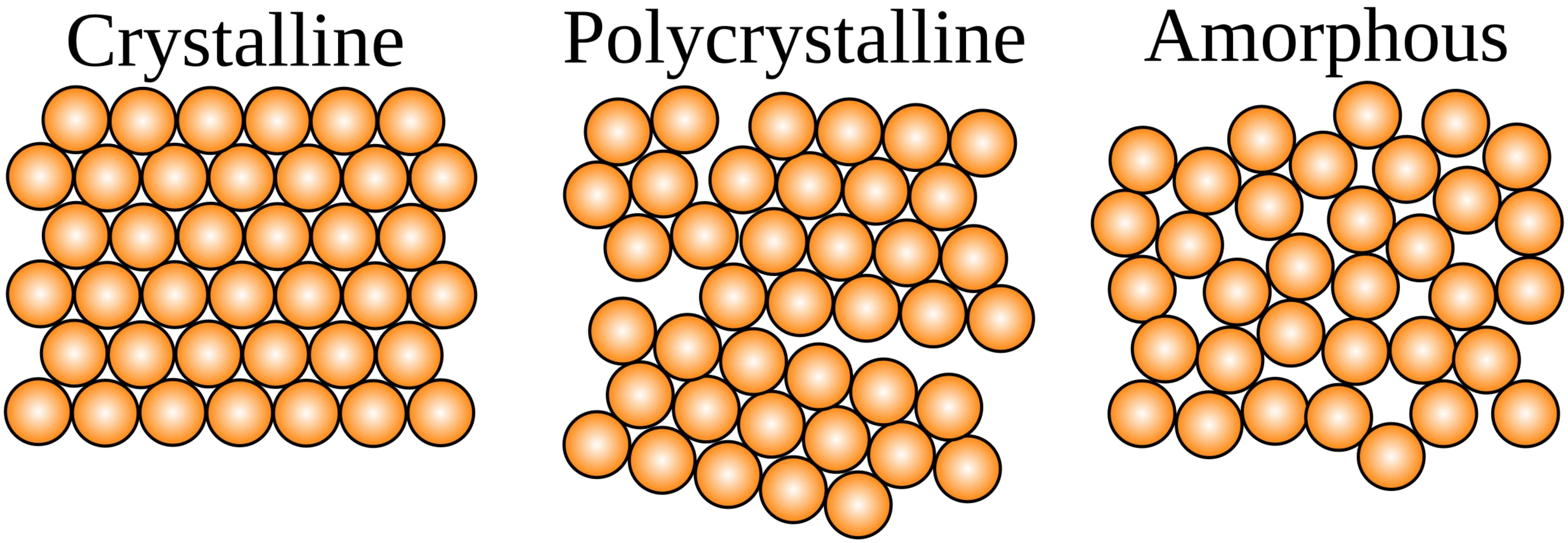
Raith EBPG-5000+ (EBL)

1. ASML, *NXE:3300B*

E-Beam Equipment Advantages & Disadvantages

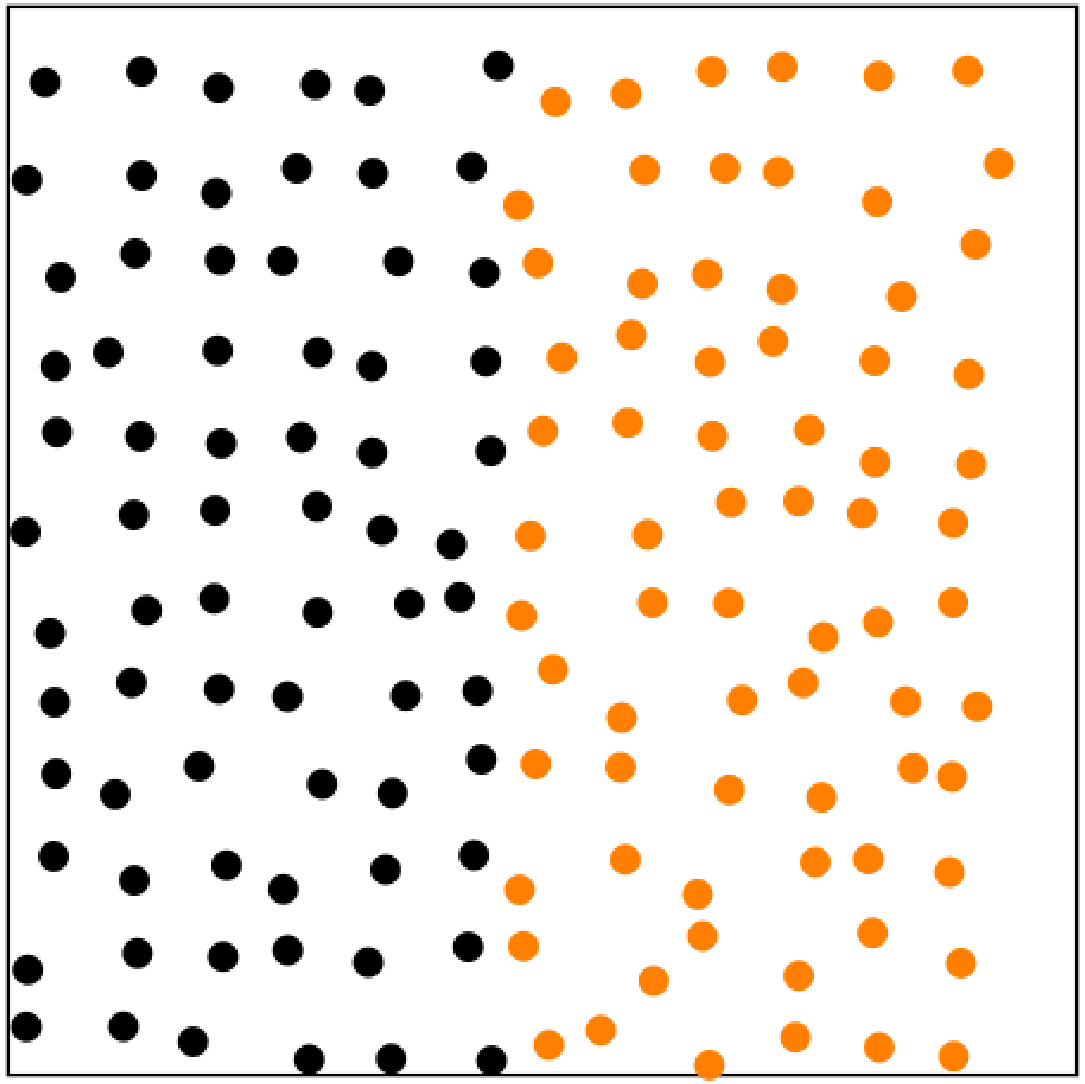
- Advantages:
  - Relatively high-resolution lithography.
  - Maskless procedure allows for indirectly importing AutoCAD drawings.
  - Fast design modification.
  - Vacuum environment leads to better control of contamination.
  - Markers can be avoided.
- Disadvantages:
  - Vacuum environment required.
  - Charge build-up, even during SEM inspection.
  - Low throughput.
  - Proximity effects.

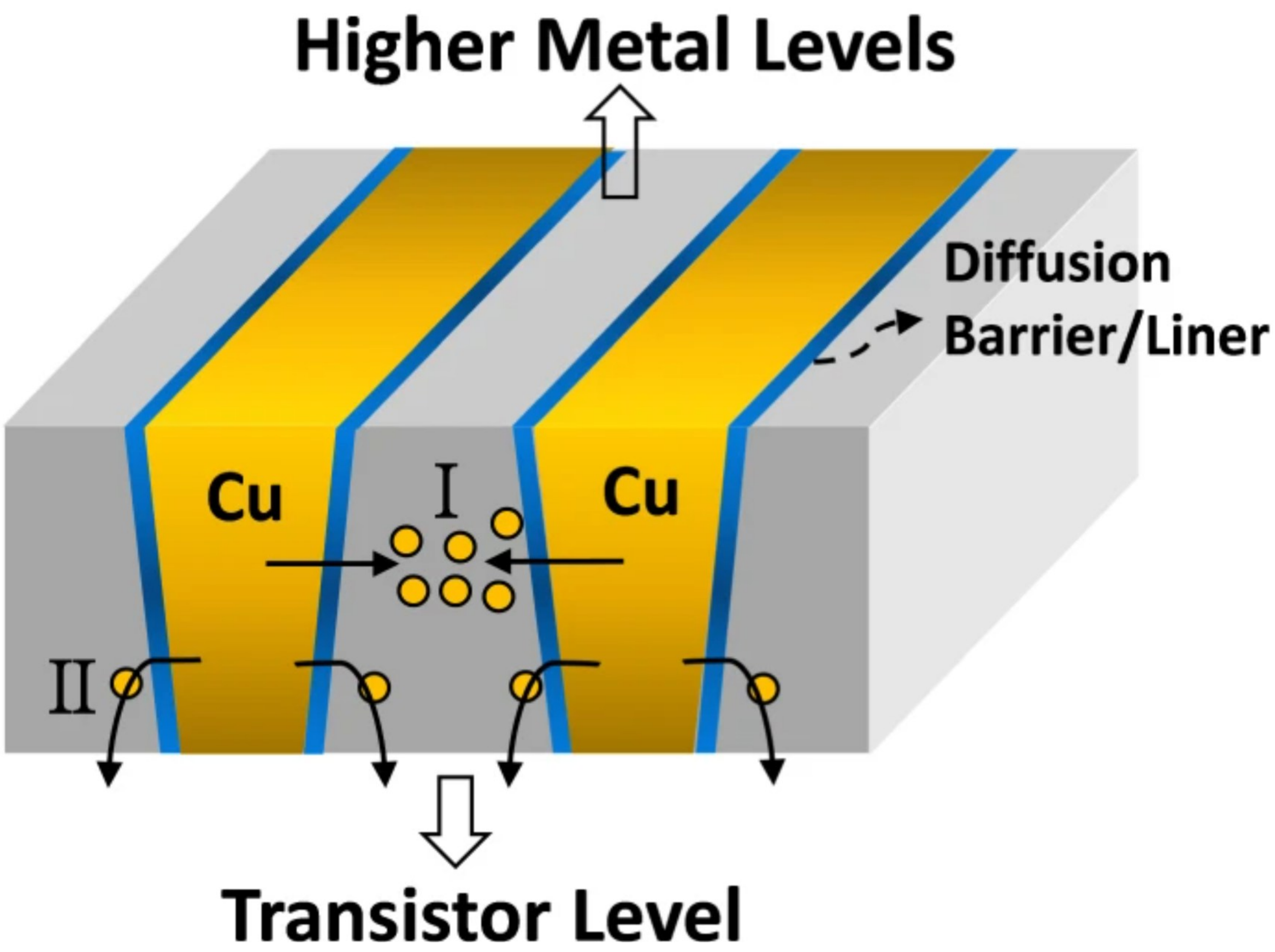
Crystalline vs. Polycrystalline vs. Amorphous Layers



1. Wikimedia Commons

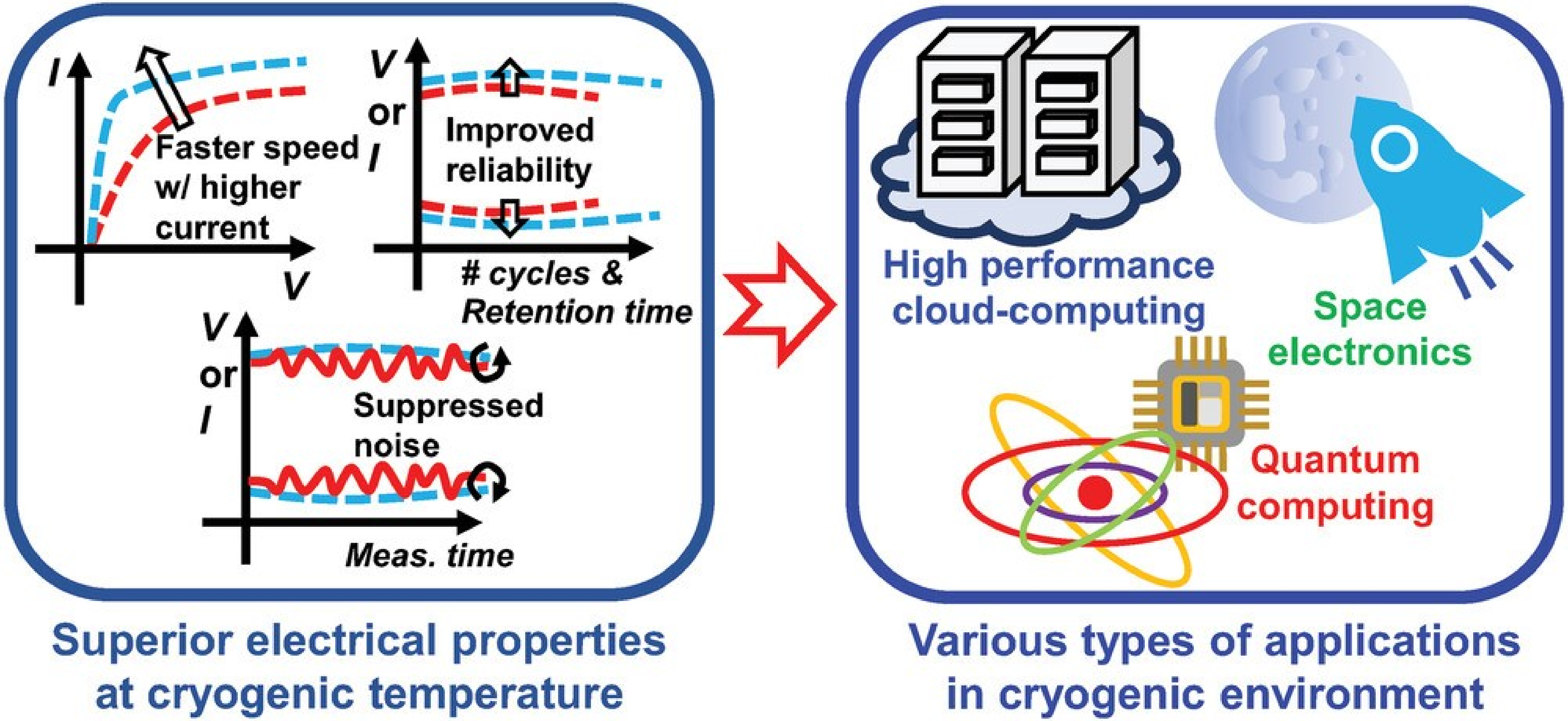
Diffusion vs. Diffusion Barrier





1. Wikimedia Commons
2. [Lo et al., *npj 2D Mater Appl* (2017)]

Cryogenic Effects on Electronics

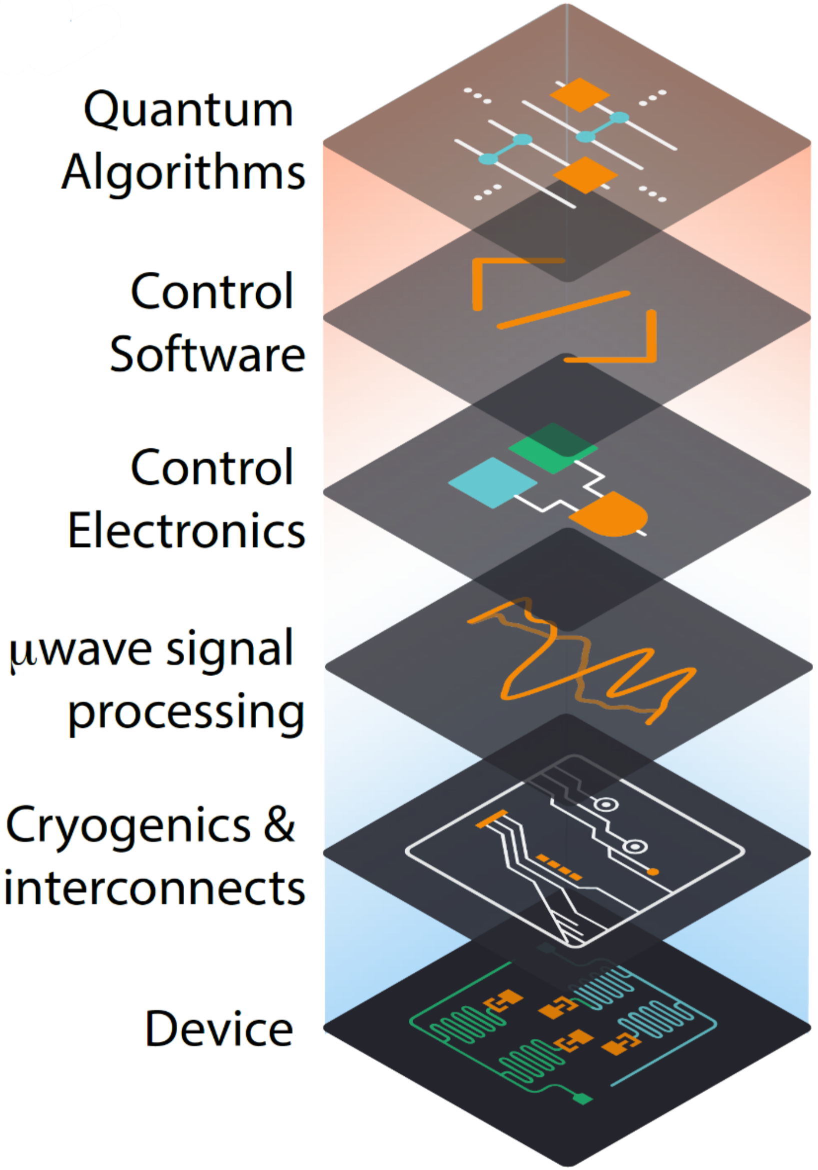


1. Hur et al., Adv. Electron. Mater. 2023, 0, 2201299 (2023)

Quantum Stack

Software

Hardware



1. Gao et al., *PRX Quantum* 2, 040202 (2021)

How to Build a Superconducting Quantum Computer

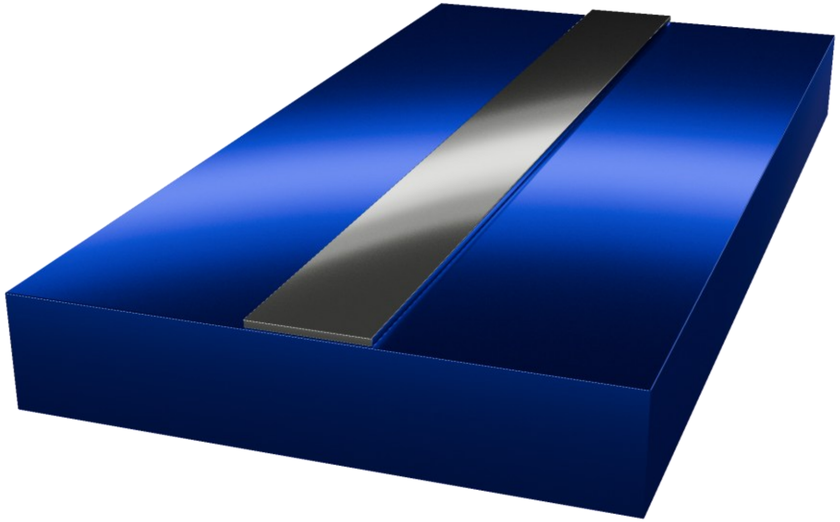
- 300 K: Classical computer interface (desktop).
- 4 K: [High gain, low noise semiconductor amplifier] << digital I/O (assembly) <> interconnects <> quantum control/ readout (cryogenic CMOS array, DAC, ADC, mixers, isolators, circulators, etc.).
- 10 mK: Interconnects + filters + thermal isolation <> quantum-limited amplifiers <> directional coupler <> isolator <> **quantum processor**.

Analog starting from the bottom, slowly turns to digital on the way up!

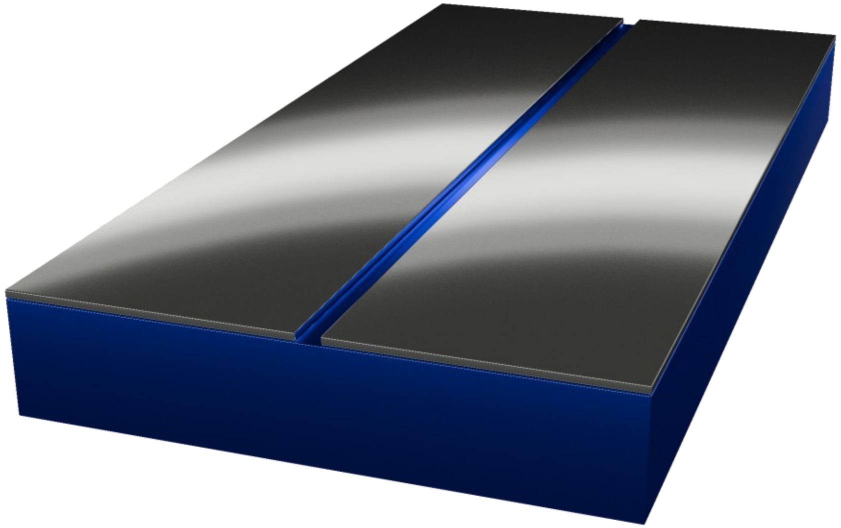
Key: Conversion, conversion, conversion…

*Most of these components are compatible with spin-based quantum computers

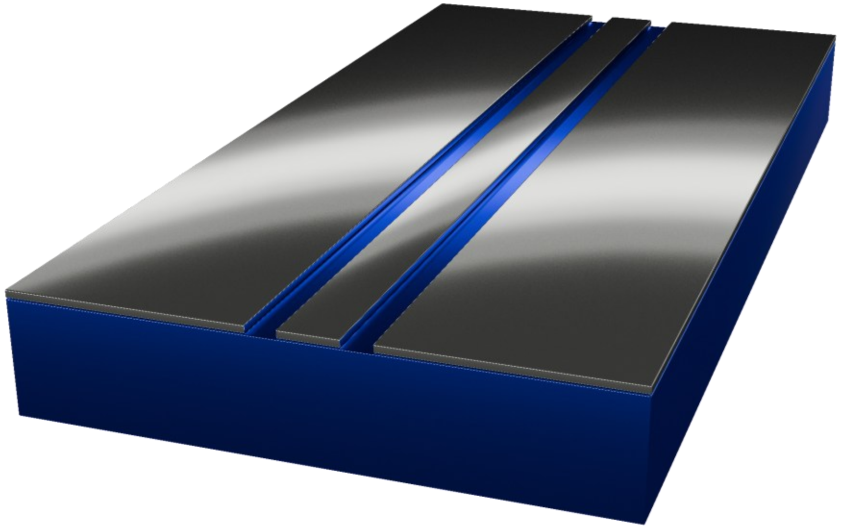
Some Common Planar Transmission Lines Rendered in Blender



Microstrip

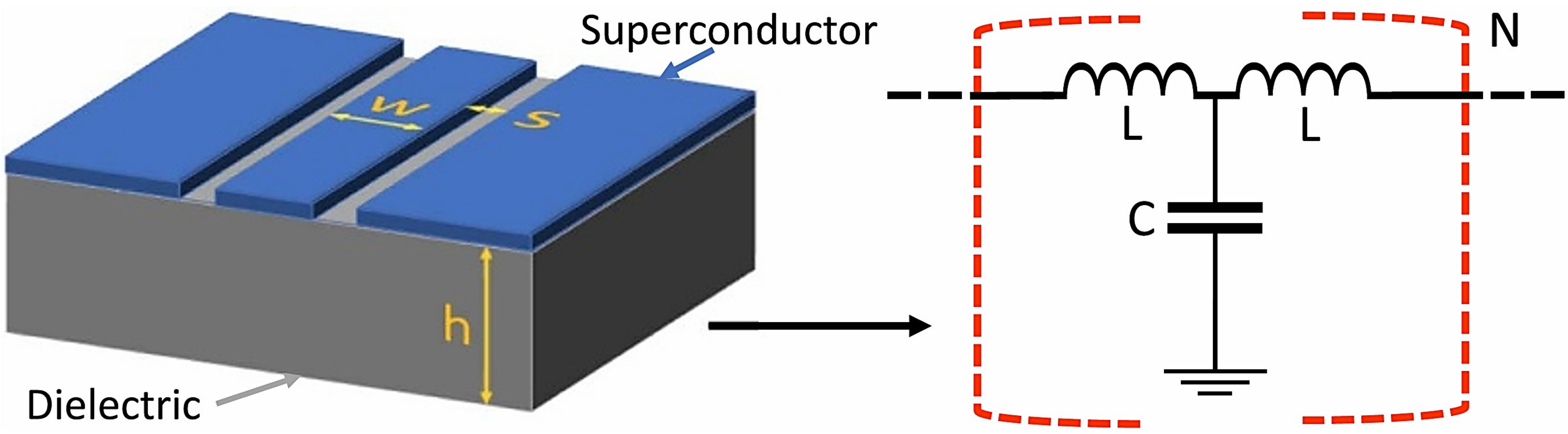


Slot Line



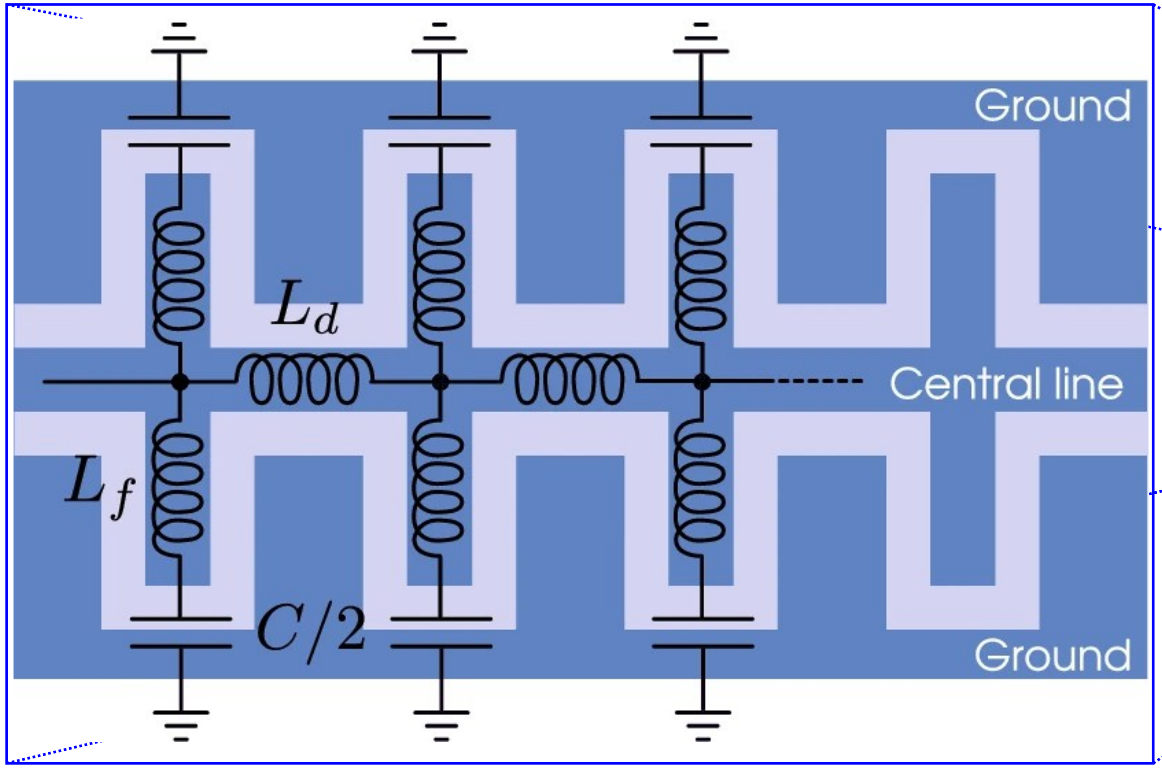
Co-planar Waveguide (CPW)

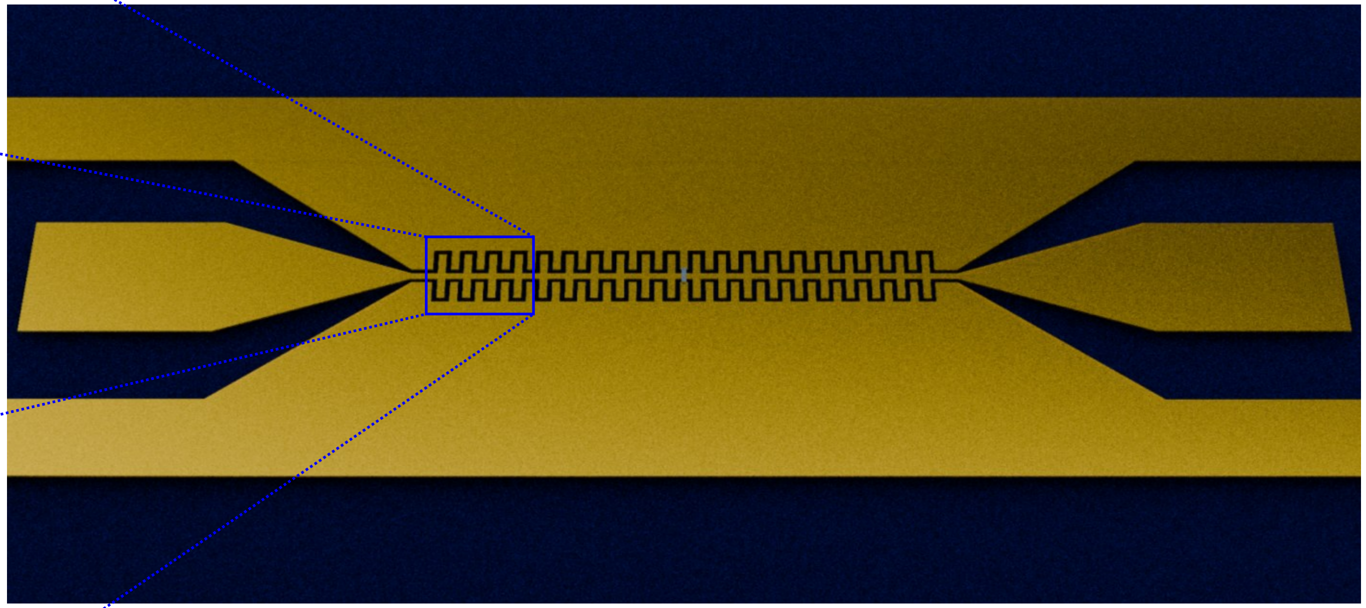
The Beauty of Abstractions in Superconducting Circuits



1. [Sweetnam et al., *Supercond. Sci. Technol.* 35 095011 (2022)]

The Beauty of Abstractions in Superconducting Circuits





Kinetic Inductance Traveling Wave Parametric Amplifier (KI-TWPA) Rendered in Blender

1. Adapted from: Giachero et al., *J Low Temp Phys* 209, 658–666 (2022)

The Beauty of Abstractions in Superconducting Circuits

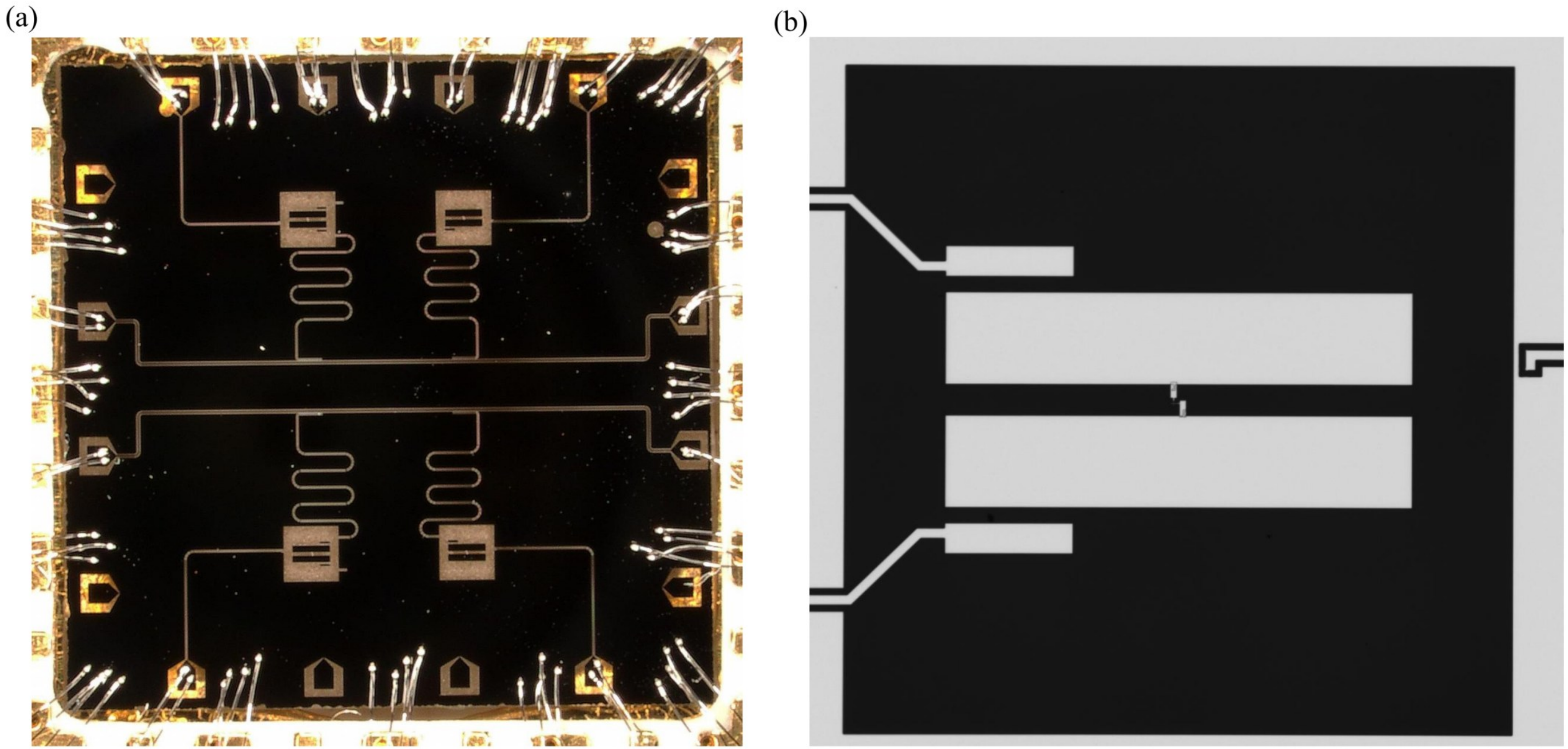
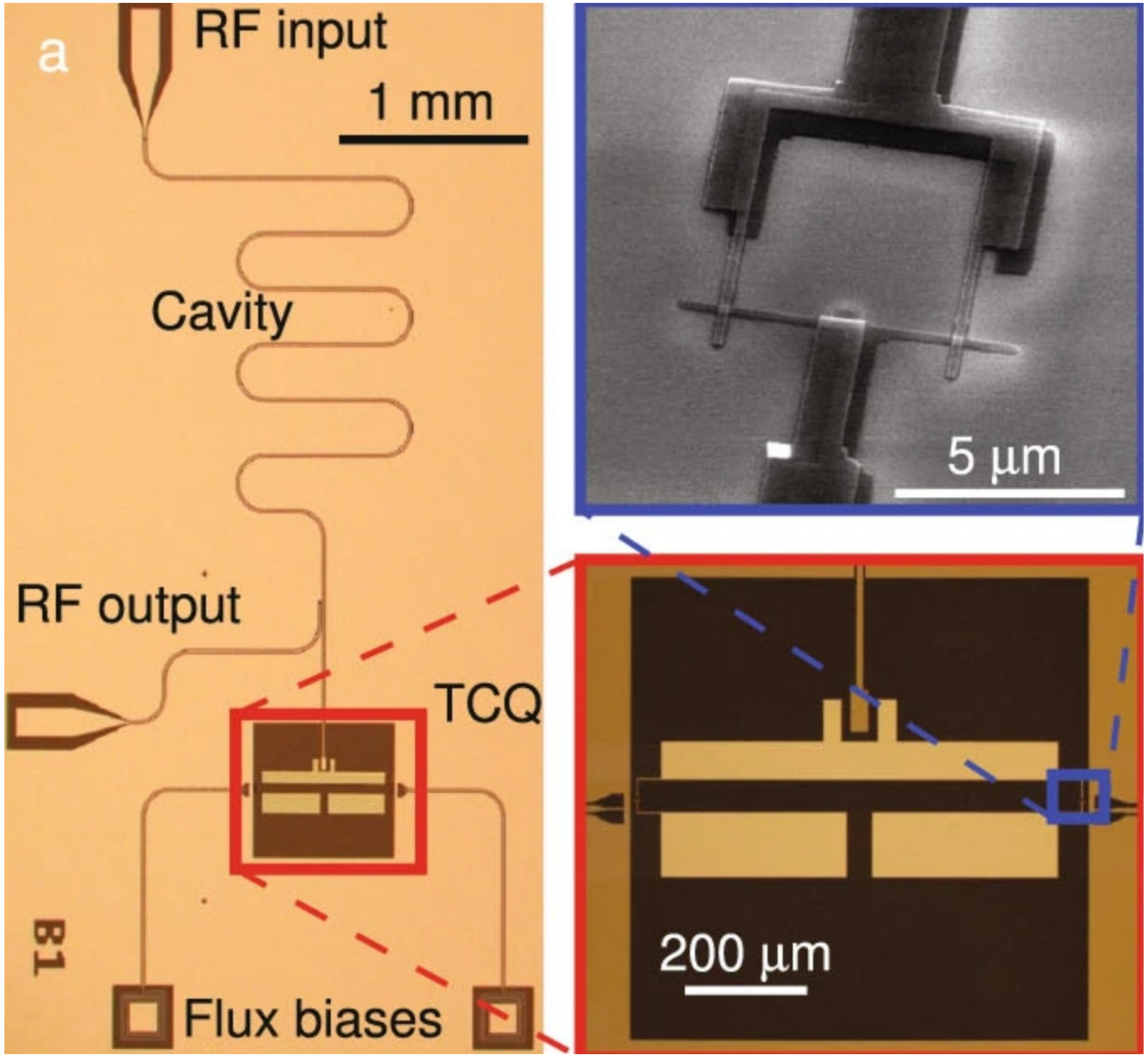


Figure 2. (**a**) Optical microscope photo of the chip. (**b**) Microscope photo of Transmon qubit.

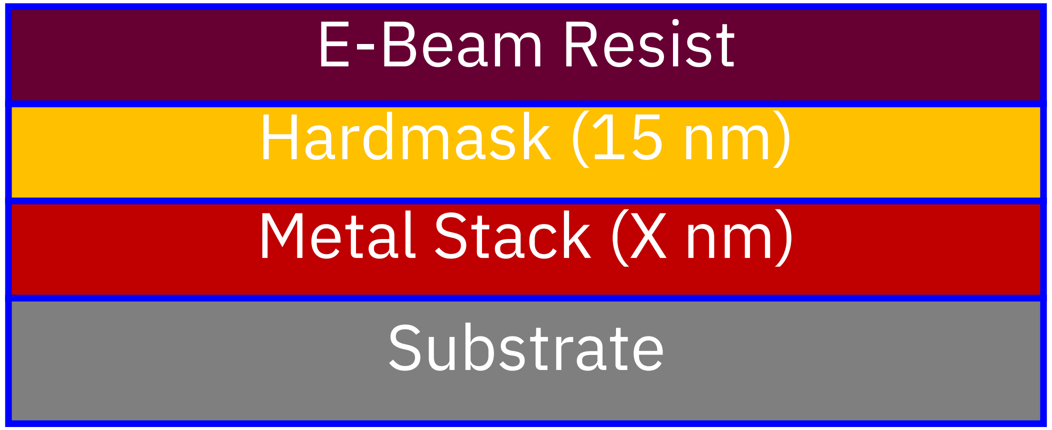
1. [Yuan et al., *Entropy* 24(6), 792 (2022)]

The Beauty of Abstractions in Superconducting Circuits



1. Zhang et al., *npj Quantum Inf* 3, 1 (2017)

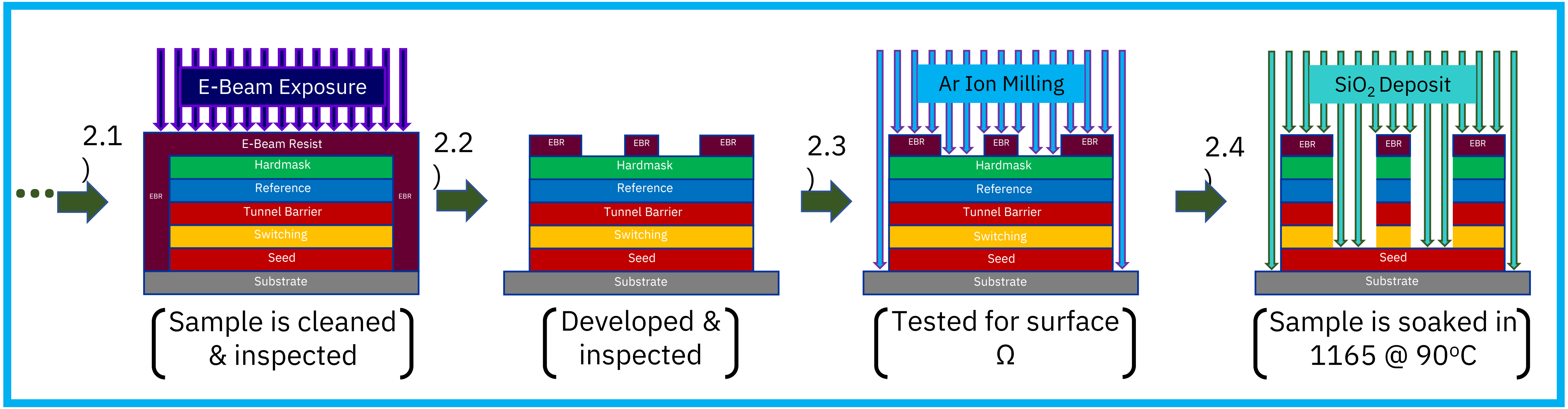
Stack Composition



Sample can contain any stack (deposited on substrate) for hardmask testing purposes

Hardmask layer can help reduce dimension size or increase the density of device drive lines & other fine features as needed.

Generic E-Beam Patterning Flow for Tunnel Junction



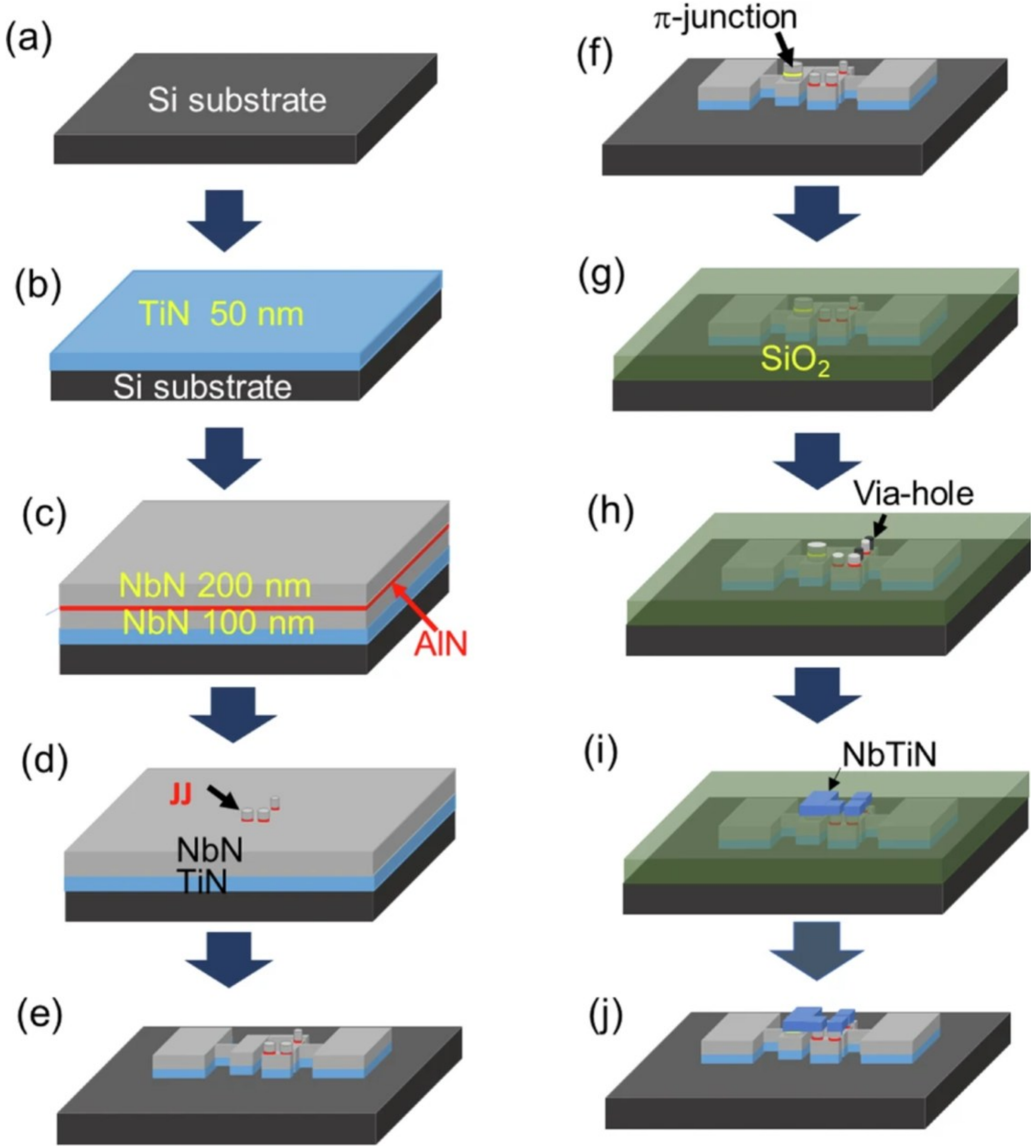
Here, the seed layer doubles as an adhesion layer

PR: Photoresist
Ω: Resistance

EBR: Electron-Beam Resist
1165: Strong Solvent

* For more details on basics of thin films for quantum chips, see "Onri's_Quantum_Hardware_Tutorial_Part_2_of_5" on GitHub.

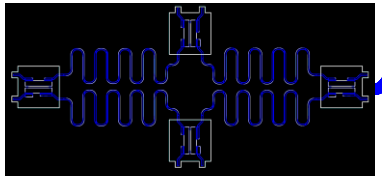
Example of a NbN-Based Flux Qubit Patterning Flow

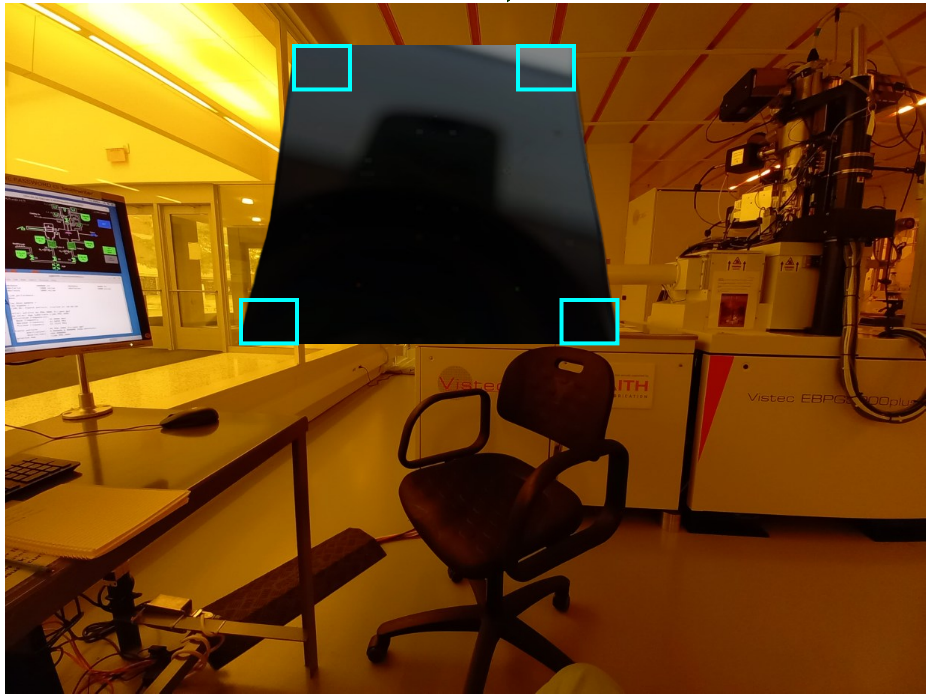


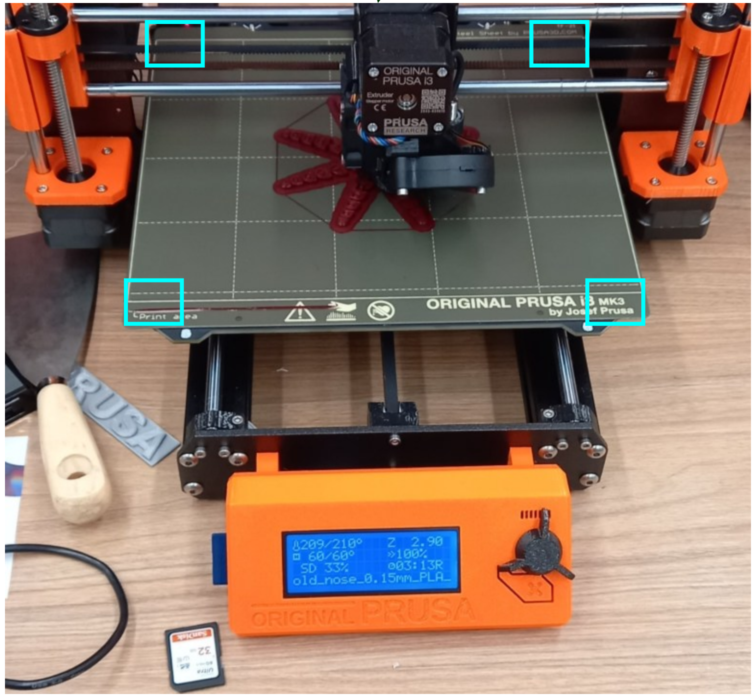
1. [Kim et al., Commun Mater 5, 216 (2024).]

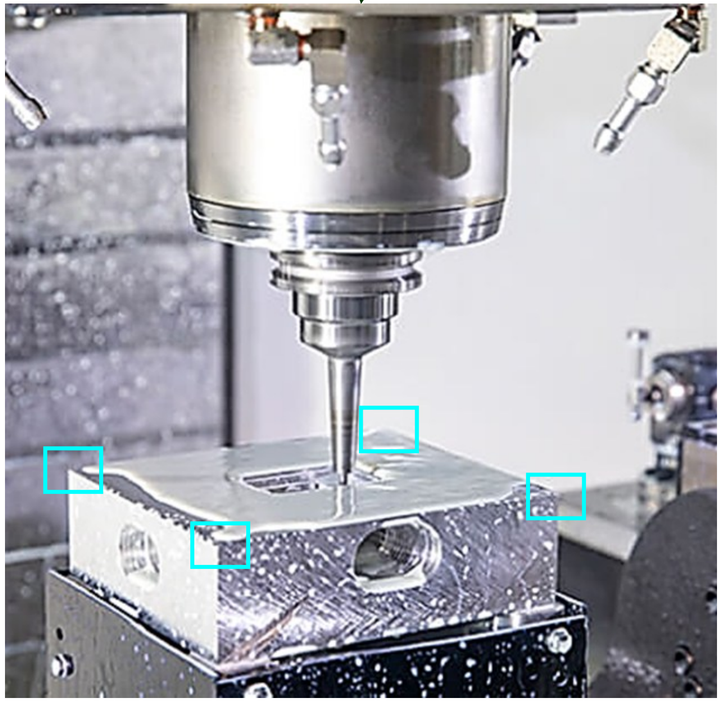
E-Beam vs. 3D Printing vs. CNC Machining

- Similarities:
  - Uses of a type of **G-CODE** or coordinate system.
  - Initial preparation procedure (pick reference points).
  - CAD **DWG** ➔ **DXF** ➔ “the **G-CODE**”.









*E-Beam = Electron-Beam
**CNC = Computer Numerical Control
*3D = 3 Dimensional

1. Taken from: howtomechatronics.com
2. Taken from: protolabs.co.uk

Design Process Flow to Test Pattern Quality

- Design file conversion is a bit extensive.
- **GDS II** ➔ CAD **DXF** ➔ **GDS II** ➔ **BEAMER** ➔ **GPF** ➔ **CJOB** ➔ **JOB** File

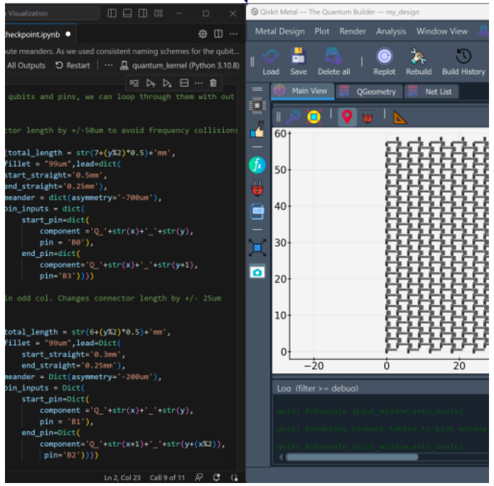
Export GDS file from Qiskit Metal.

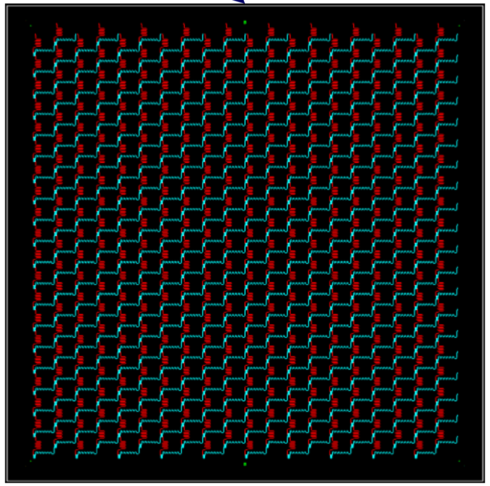
For modifiable polygons & layer separation. (Pattern editors allow GDS-to-DXF conversion & some degree of layer separation).

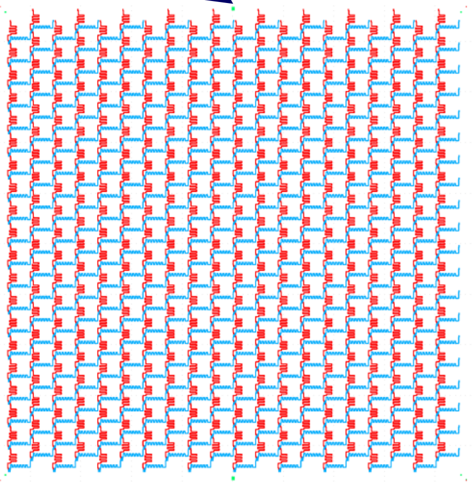
At this point, each layer should be labeled based on their feature sizes, ready for lithography software.

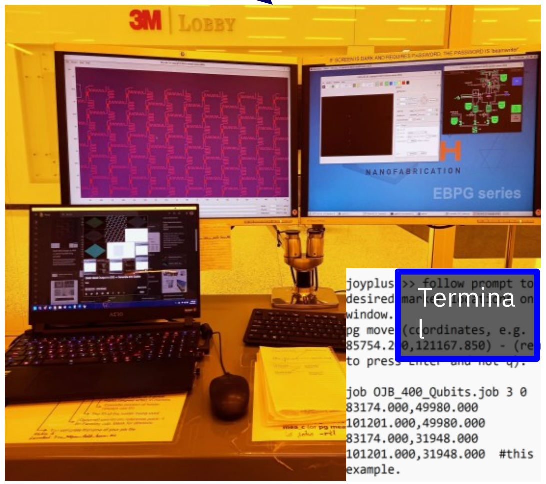
Additional Parameters (dosage, sub. size, etc.)

During final setup, machine actually uses this one.







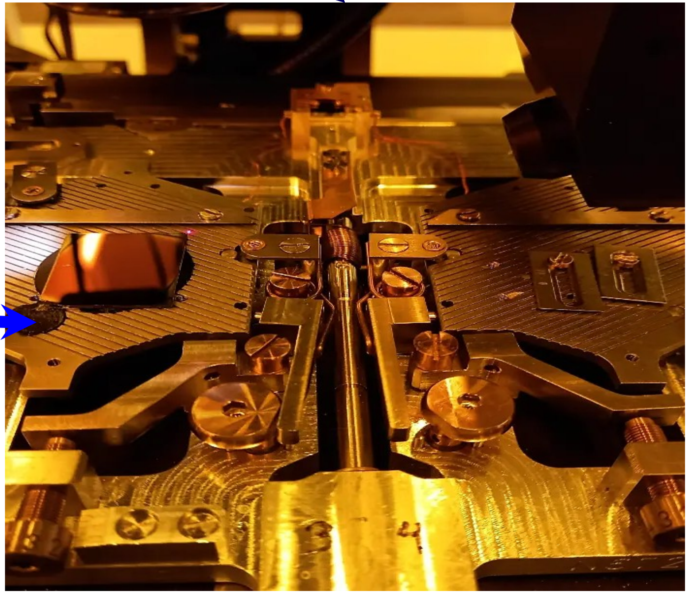


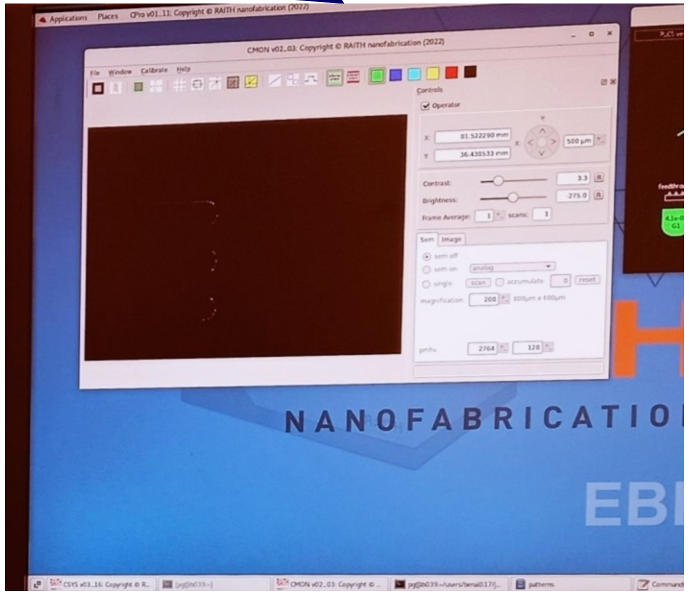
Maskless Direct Writing Using “Joyplus”

- Doses:
  - For relatively larger features (**pads** & **stripes**): 450 μC/cm^2.
  - For smaller features (**pillars** & **junctions**): 825-875 μC/cm^2.
- Basically:
  - Locate 4 Points ➔ SEM-Aided ‘Marker’ Location ➔ Record Final Marker Position ➔ **Confirm & Write!**

(joyplus)

Conductive carbon tape





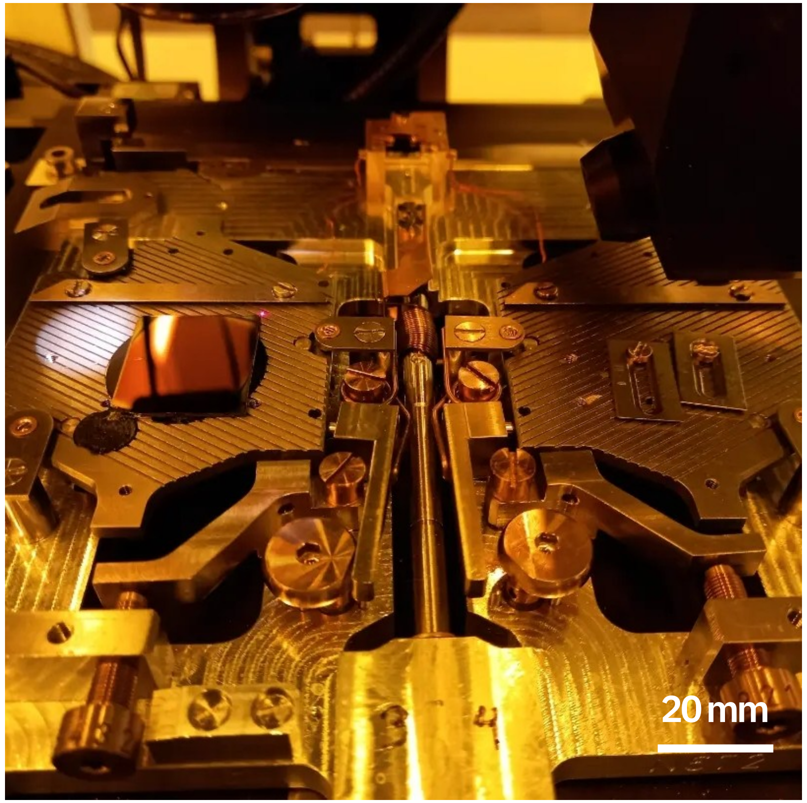
Terminal

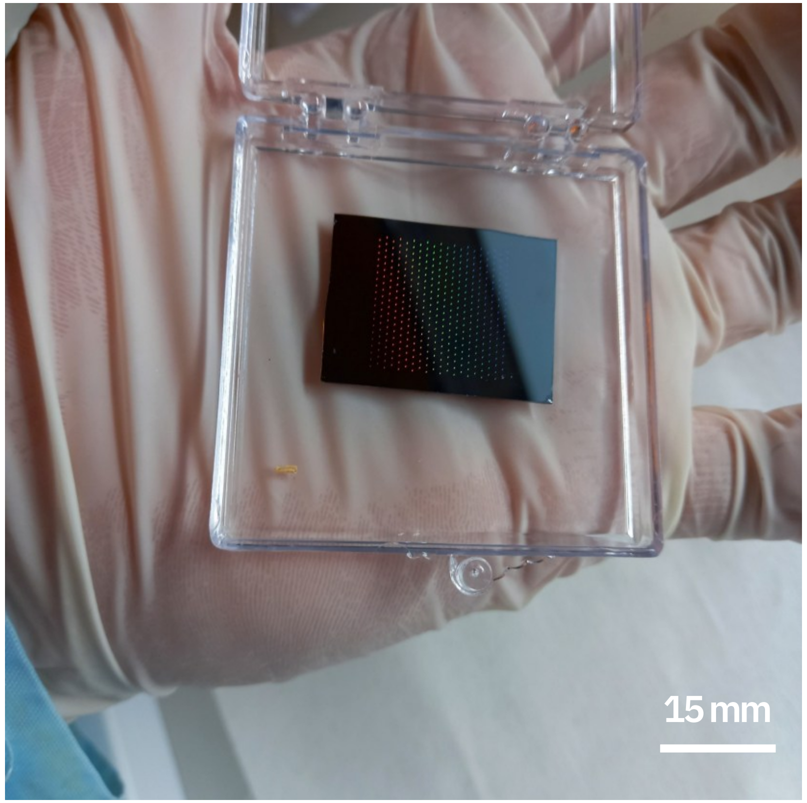
```
joyplus >> follow prompt to center
desired marker locations on SEM
window.
pg move (coordinates, e.g.
85754.200,121167.850) - (remember
to press Enter and not q).

job OJB_400_Qubits.job 3 0
83174.000,49980.000
101201.000,49980.000
83174.000,31948.000
101201.000,31948.000  #this is an
example.
```

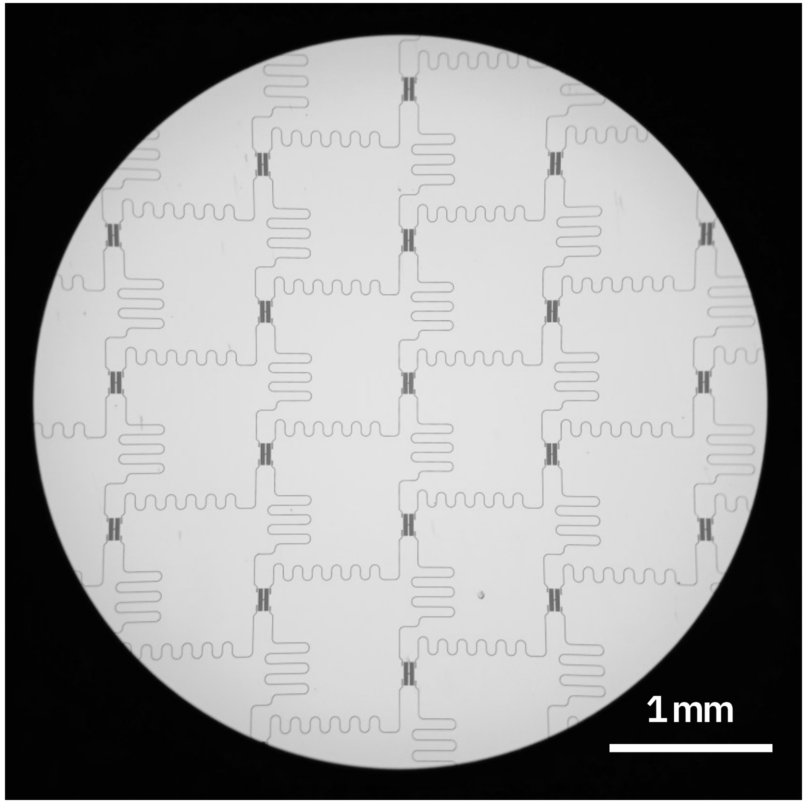
Basic Flow Summary of “Joyplus” for E-Beam

- Enter relative coordinates >> locate desired marker reference points >> record real coordinates found >> enter (pg move position) of real coordinates >> type (joyplus) >> confirm real coordinates of marker locations by inspecting SEM scan >> press Enter.
- You may now continue with job file locations and other parameters for stage selection >> copy-paste job command into teminal >> press Enter >> watch 1st few steps of exposure >> Done!

Results







On the sample holder, conductive carbon tape is used to stick sample to grounded metal to prevent charge build-up. Charge build-up deflects the electron-beam & causes undesired patterns on the chip.

Results (Continued)