L6235 THREE PHASE BRUSHLESS DC MOTOR DRIVER

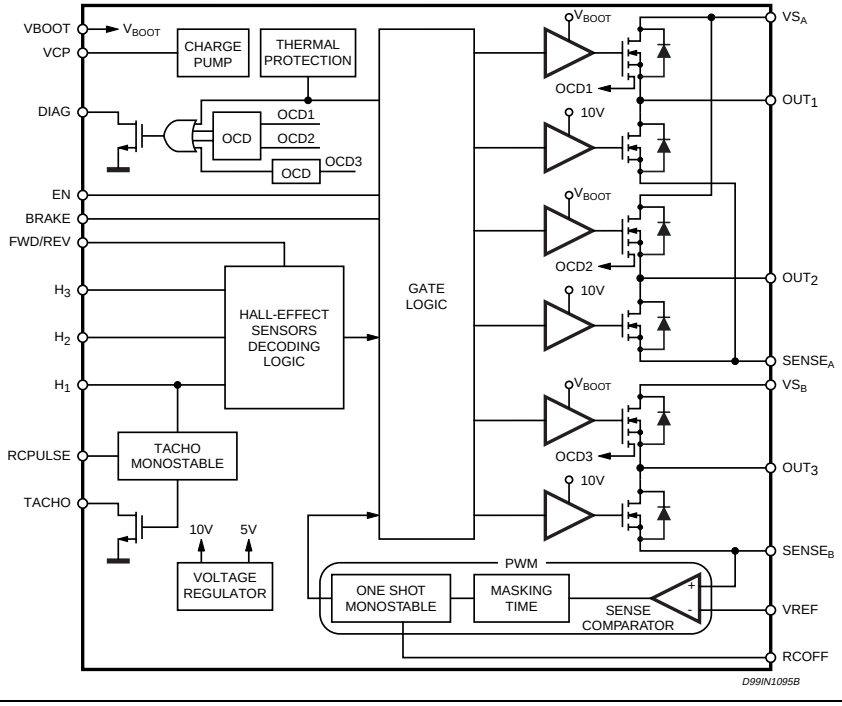
by Vincenzo Marano

Modern motion control applications need more flexibility that can be addressed only with specialized ICs products. The L6235 is a fully integrated motor driver IC specifically developed to drive a wide range of BLDC motors with Hall effect sensors. This IC is a one-chip cost effective solution that includes several unique circuit design features. These features, including a universal decoding logic that allows the device to be used with most common Hall effect spacing, will be described. The principal aim of this development project was to produce an easy to use, fully protected power IC. In addition several key functions as protection circuit and high speed PWM current control allow to drastically reduce the external components count to meet requirements for many different applications.

1 INTRODUCTION

For small-motor applications many appliance designers favor modern three phase brushless DC motors because of the high efficiency (as great as 95%) and small size for a given delivered power. Designers have to handle control logic, torque and speed control, power-delivery issues and ensure safe operation in every load condition. The L6235 is a highly integrated, mixed-signal power IC that allows to easily design a complete motor control system for BLDC motor. Figure 1 shows the L6235 block diagram. The IC integrates six Power DMOS, a centralized logic circuit to decode hall effect sensors and a constant t_{OFF} PWM current control technique (Synchronous mode) plus other added features for safe operation and flexibility.

Figure 1. L6235 Block Diagram.



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2 DESIGNING AN APPLICATION WITH L6235

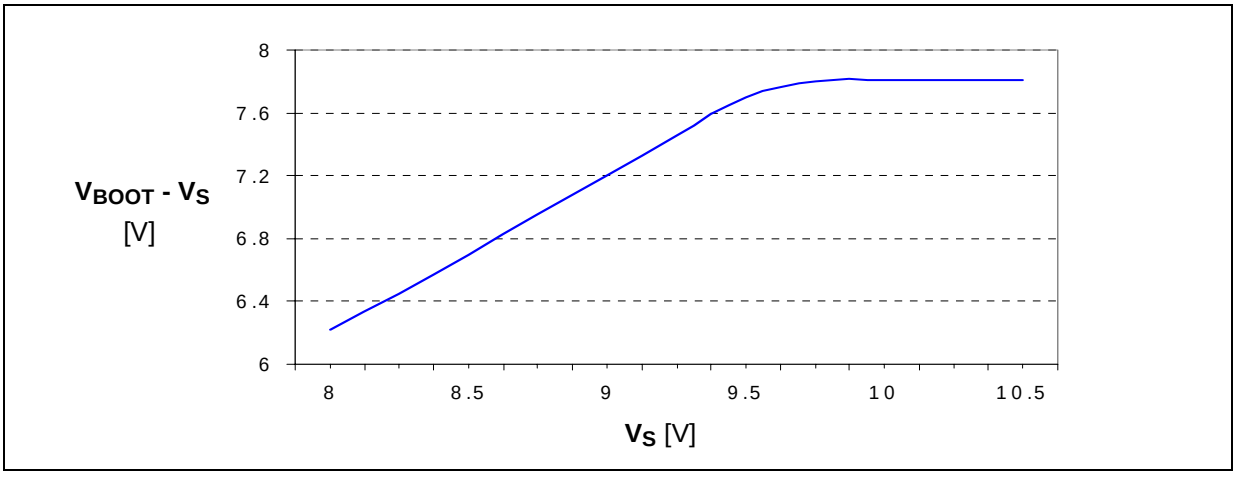
2.1 Current Ratings

With MOSFET (DMOS) devices, unlike bipolar transistors, current under short circuit conditions is, at first approximation, limited by the $R_{DS(ON)}$ of the DMOS themselves and could reach very high values. L6235 Out pins and the two V_{SA} and V_{SB} pins are rated for a maximum of 2.8 A r.m.s. and 5.6 A peak (typical values). These values are meant to avoid damaging metal structures, including the metallization on the die and bond wires. In practical applications, though, maximum allowable current is less than these values, due to power dissipation limits (see Power Management section).
The device has a built-in Over Current Detection (OCD) that allows protection against short circuits between the outputs and between an output and ground (see Over Current Detection Section).

2.2 Voltage Ratings and Operating Range

The L6235 requires a single supply voltage (V_S), for the motor supply. Internal voltage regulators provide the 5V and 10 V required for the internal circuitry. The operating range for V_S is 8 to 52 V. To prevent working into undesirable low supply voltage an Under Voltage Lock Out (UVLO) circuit shuts down the device when supply voltage falls below 6 V; to resume normal operating conditions, V_S must then exceed 7 V. The hysteresis is provided to avoid false intervention of the UVLO function during fast V_S ringings. It should be noted, however, that DMOS's $R_{DS(ON)}$ is a function of the V_S supply voltage. Actually, when V_S is less than 10V, $R_{DS(ON)}$ is adversely affected, and this is particularly true for the High Side DMOS that are driven from V_{BOOT} supply. This supply is obtained through a charge pump from the internal 10V supply, which will tend to reduce its output voltage when V_S goes below 10V. Figure 2 shows the supply voltage of the high side gate drivers (V_{BOOT} - V_S) versus the supply voltage (V_S).

Figure 2. High side gate drivers supply voltage versus supply voltage.



Note that V_S must be connected to both V_{SA} and V_{SB} because the bootstrap voltage (at V_{BOOT} pin) is the same for the two H-bridges. The integrated DMOS have a rated Drain-Source breakdown voltage of 60 V. However V_S should be kept below 52 V, since in normal working conditions the DMOS see a Vds voltage that will exceed V_S supply. In particular when a high-side DMOS turns off due to a phase change (OUT1 in Figure 3), if one of the other outputs (OUT2 in Figure 3) is high (during the off-time all active bridges turn their high-side on) the load current starts flowing in the low-side freewheeling diode and the SENSE pin sees a negative spike due to a not negligible parasitic inductance of the PCB path from the pin to GND. This spike is followed by a stable negative voltage due to the drop on R_{SENSE}. The output pin sees a similar behavior, but with a slightly larger voltage due to the forward recovery time of the integrated freewheeling diode and the forward voltage drop across it. Typical duration of this spike is 30 ns. At the same time, the OUT2 pin (in the example of Figure 3)

sees a voltage above V_S, due to voltage drop across the high-side (integrated) freewheeling diode, as the current reverses direction and flows into the bulk capacitor. It turns out that the highest differential voltage is observed between two OUT pins when a phase change turns a high-side off during an off-time, and this must always be kept below 60 V [2].

Figure 3. Currents and voltages if a phase change turns a high-side off during off-time.

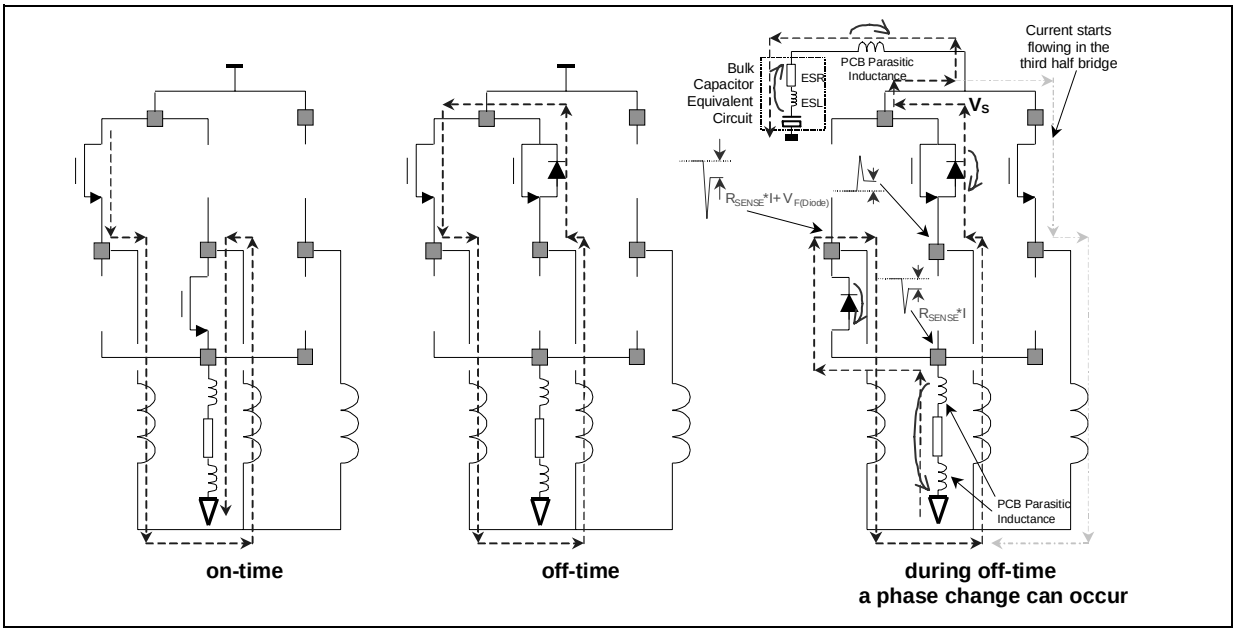
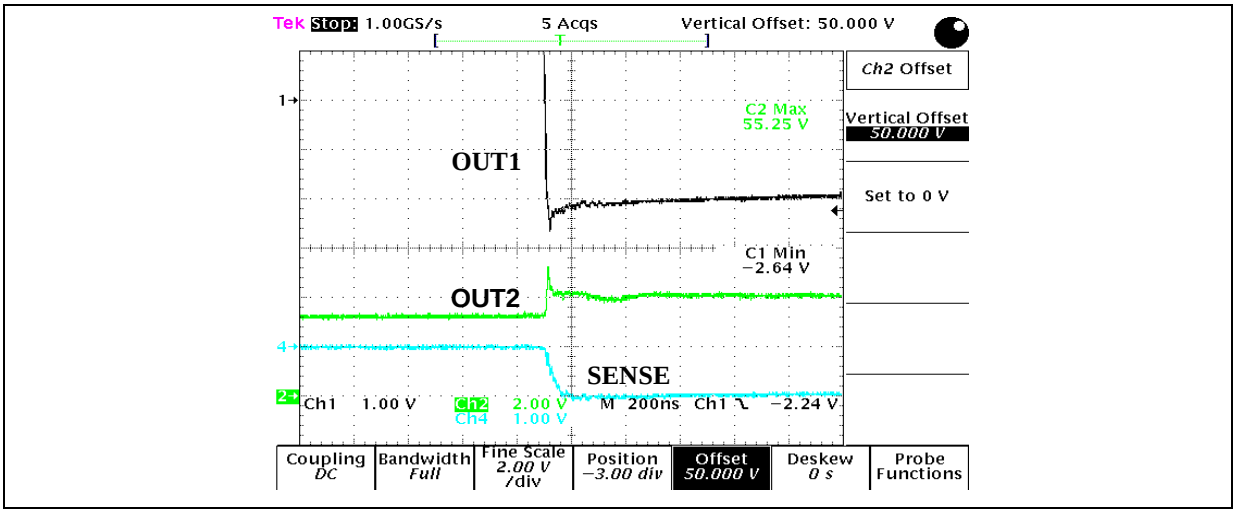


Figure 4 shows the voltage waveforms at the OUT pins referring to a possible practical situation, with a peak output current of 2.8 A, V_S = 52 V, R_{SENSE} = 0.33 Ω, TJ = 25 °C (approximately) and a good PCB layout. Below ground spike amplitude is -2.64 V for one output; the other OUT pin is at about 55 V. In these conditions, total differential voltage reaches almost 60 V, which is the absolute maximum rating for the DMOS. Keeping differential voltage between two Output pins within rated values is a must that can be accomplished with proper selection of Bulk capacitor value and equivalent series resistance (ESR), according to current peaks and adopting good layout practices to minimize PCB parasitic inductances (see below) [2].

Figure 4. Voltage at the two outputs if a phase change turns a high-side off during off-time.



2.3 Choosing the Bulk Capacitor

Since the bulk capacitor, placed between V_S and GND pins, is charged and discharged during IC operation, its AC current capability must be greater than the r.m.s. value of the charge/discharge current. This current flows from the capacitor to the IC during the on-time (t_{ON}) and from the IC (during some phase changes; from the power supply during off-time) to the capacitor during the off-time (t_{OFF}). The r.m.s. value of the current flowing into the bulk capacitor depends on peak output current, output current ripple, switching frequency, duty-cycle. It also depends on power supply characteristics. A power supply with poor high frequency performances (or long, inductive connections to the IC) will cause the bulk capacitor to be recharged slowly: the higher the current control switching frequency, the higher the current ripple in the capacitor; r.m.s. current in the capacitor, however, does not exceed the r.m.s. output current. Bulk capacitor value (C) and the ESR determine the amount of voltage ripple on the capacitor itself and on the IC. Neglecting the output current ripple and assuming that during the on-time the capacitor is not recharged by the power supply, the voltage at the end of the on-time is

$$V_S - I_{OUT} \cdot \left(ESR + \frac{t_{ON}}{C} \right)$$

where I_{OUT} is the output current. Usually (if C>100 µF) the capacitance role is much less than the ESR, then supply voltage ripple can be estimated as

$$I_{OUT} \cdot ESR$$

For Example, if a maximum ripple of 500 mV is allowed and I_{OUT} = 2 A, the capacitor ESR should be lower than

$$ESR < \frac{0.5V}{2A} = 250m\Omega$$

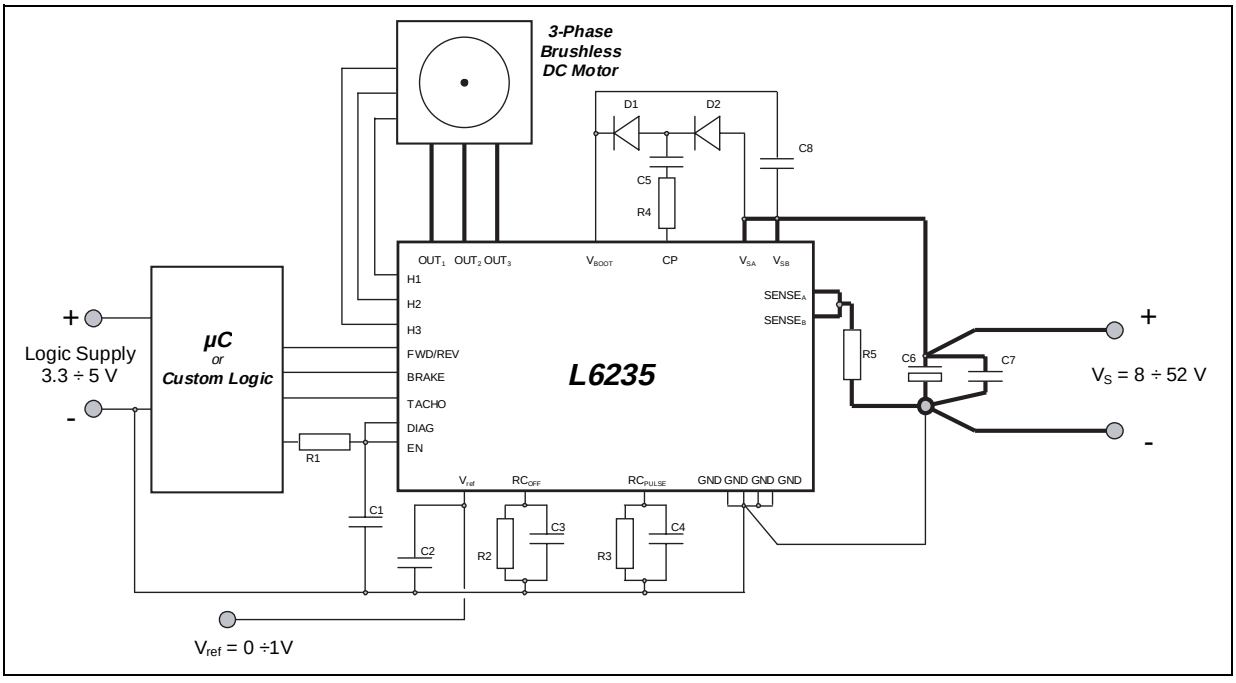
Note that additional ripple is due to parasitic inductances on V_S PCB tracks (see Voltage Ratings and Operating Range section).

Actually, current sunk by V_{SA} and V_{SB} pins of the device is subject to higher peaks due to reverse recovery charge of internal freewheeling diodes. Duration of these peaks is, tough, very short (100÷200 ns) and can be filtered using a small value (100÷200 nF), good quality ceramic capacitor, connected as close as possible to the V_{SA}, V_{SB} and GND pins of the IC. Bulk capacitor will be chosen with maximum operating voltage 25% greater than the maximum supply voltage, considering also power supply tolerances. For example, with a 48 V nominal power supply, with 5% tolerance, maximum voltage is 50.4 V, then operating voltage for the capacitor should be at least 63 V.

2.4 Layout Considerations

Working with devices that combine high power switches and control logic in the same IC careful attention has to be paid to the PCB layout. In extreme cases, Power DMOS commutation can induce noises that could cause improper operation in the logic section of the device. Noise can be radiated by high dv/dt nodes or high di/dt paths, or conducted through GND or Supply connections. Logic connections, especially high-impedance nodes (actually all logic inputs, see further), must be kept far from switching nodes and paths. With the L6235, in particular, external components for the charge pump circuitry should be connected together through short paths, since these components are subject to voltage and current switching at relatively high frequency (600 kHz). Primary mean in minimizing conducted noise is working on a good GND layout (see Figure 5).

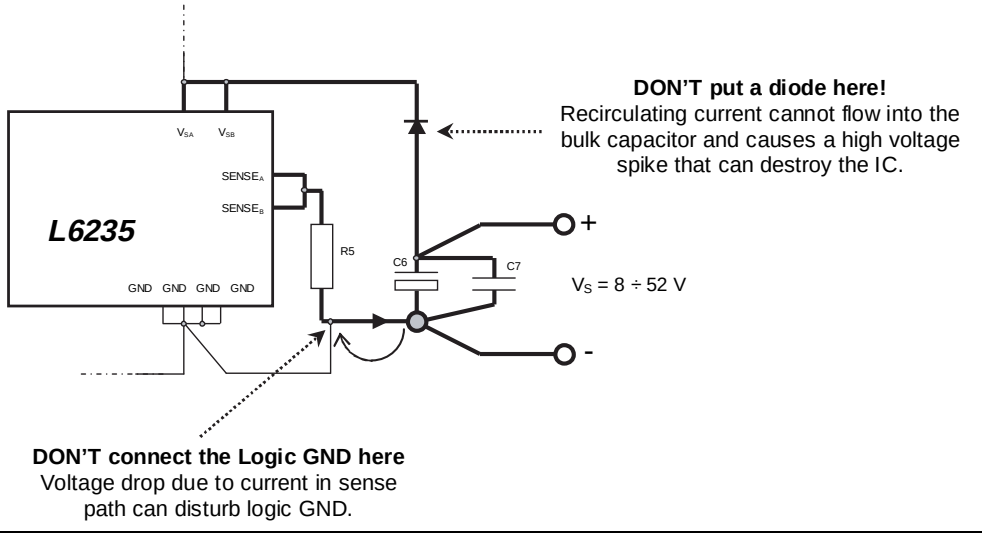
Figure 5. Typical Application and Layout suggestions.



High current GND tracks (i.e. the tracks connected to the sensing resistor) must be connected directly to the negative terminal of the bulk capacitor. A good quality, high-frequency bypass capacitor is also required (typically a 100 nF÷200 nF ceramic would suffice), since electrolytic capacitors show a poor high frequency performance. Both bulk electrolytic and high frequency bypass capacitors have to be connected with short tracks to V_{SA}, V_{SB} and GND. On the L6235 GND pins are the Logic GND, since only the quiescent current flows through them. Logic GND and Power GND should be connected together in a single point, the bulk capacitor, to keep noise in the Power GND from affecting Logic GND. Specific care should be paid layouting the path from the SENSE pins through the sensing resistor to the negative terminal of the bulk capacitor (Power Ground). These tracks must be as short as possible in order to minimize parasitic inductances that can cause dangerous voltage spikes on SENSE and OUT pins (see the Voltage Ratings and Operating Range section); for the same reason the capacitors on V_{SA}, V_{SB} and GND pins should be very close to the GND and supply pins. Refer to the Sensing Resistors section for information on selecting the sense resistors. Traces that connect to V_{SA}, V_{SB}, $SENSE_A$, $SENSE_B$, and the three OUT pins must be designed with adequate width, since high currents are flowing through these traces, and layer changes should be avoided. Should a layer change prove necessary, multiple and large via holes have to be used. A wide GND copper area can be used to improve power dissipation for the device.

Figure 6 shows two typical situations that must be avoided. An important consideration about the location of the bulk capacitor is the ability to absorb the inductive energy from the load, without allowing the supply voltage to exceed the maximum rating. The diode shown in Figure 6 prevents the recirculation current from reaching the capacitors and will result in a high voltage on the IC pins that can destroy the device. Having a switch or a power connection that can disconnect the capacitors from the IC, while there is still current in the motor, will also result in a high voltage transient since there is no capacitance to absorb the recirculation current.

Figure 6. Two situations that must be avoided.



2.5 Sensing Resistor

Motor winding current flows through the sensing resistor, causing a voltage drop that is used, by the logic, to control the peak value of the load current. Two issues must be taken into account when choosing the R_{SENSE} value:

- The sensing resistor dissipates energy and provides dangerous negative voltages on the SENSE pins during the current recirculation. For this reason the resistance of this component should be kept low.
- The voltage drop across R_{SENSE} is compared to the reference voltage (on Vref pin) by the internal comparator. The lower is the R_{SENSE} value, the higher is the peak current error due to noise on Vref pin and to the input offset of the current sense comparator: too small values of R_{SENSE} must be avoided.

A good compromise is calculating the sensing resistor value so that the voltage drop, corresponding to the peak current in the load (Ipeak), is about 0.5 V: R_{SENSE} = 0.5 V / Ipeak.

It should be clear that sensing resistor must absolutely be non-inductive type in order to avoid dangerous negative spikes on SENSE pins. Wire wounded resistors cannot be used here, while Metallic film resistors are recommended for their high peak current capability and low inductance. For the same reason the connections between the SENSE pins, C6, C7, V_{SA}, V_{SB} and GND pins (see Figure 5) must be taken as short as possible (see also the Layout Considerations section).

The average power dissipated by the sensing resistor is:

$$P_R \approx I_{rms}^2 \cdot R_{SENSE} \cdot D \ ;$$

D is the duty-cycle of the PWM current control, I_{rms} is the r.m.s. value of the load current.

Nevertheless, sensing resistor power rating should be chosen taking into account the peak value of the dissipated power:

$$P_R \approx I_{pk}^2 \cdot R_{SENSE} \quad ,$$

where I_{pk} is the peak value of the load current.

Using multiple resistors in parallel will help obtaining the required power rating with standard resistors, and re-

duce the inductance.

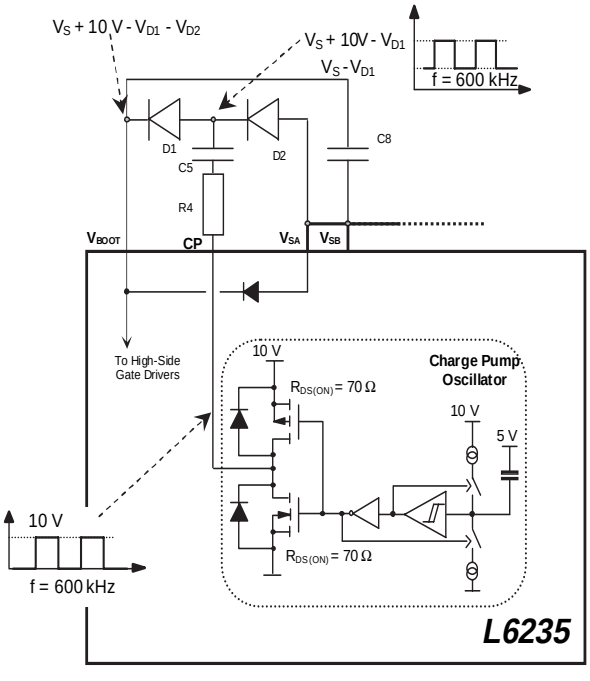
R_{SENSE} tolerance reflects on the peak current error: 1% resistors should be preferred.
The following table shows R_{SENSE} recommended values (to have 0.5V drop on it) and power ratings for typical examples of current peak values.

I_{pk}	R_{SENSE} Value [Ω]	R_{SENSE} Power Rating [W]	Alternatives
0.5	1	0.25	
1	0.5	0.5	2 X 1Ω, 0.25W paralleled
1.5	0.33	0.75	3 X 1Ω, 0.25W paralleled
2	0.25	1	4 X 1Ω, 0.25W paralleled

2.6 Charge pump external components

An internal oscillator, with its output at CP pin, switches from GND to 10 V with a typical frequency of 600 kHz (see Figure 7).

Figure 7. Charge Pump.



When the oscillator output is at ground, C5 is charged by V_S through D2. When it rises to 10 V, D2 is reverse biased and the charge flows from C5 to C8 through D1, so the V_{BOOT} pin, after a few cycles, reaches the maximum voltage of V_S + 10 V - V_{D1} - V_{D2}, which supplies the high-side gate drivers.

With a differential voltage between V_S and V_{BOOT} of about 9V and the bridges switching at 50 kHz, the typical current drawn by the V_{BOOT} pin is 1.85mA.

Resistor R4 is added to reduce the maximum current in the external components and to reduce the slew rate of the rising and falling edges of the voltage at the CP pin, in order to minimize interferences with the rest of the circuit. For the same reason care must be taken in realizing the PCB layout of R4, C5, D1, D2 connections (see also the Layout Considerations section). Recommended values for the charge pump circuitry are:

D1, D2 : 1N4148

R4 : 100 Ω (1/8 W)

C5 : 10 nF 100V ceramic

C8 : 220 nF 35V ceramic

Due to the high charge pump frequency, fast diodes are required. Connecting the cold side of the bulk capacitor (C8) to V_S instead of GND the average current in the external diodes during operation is less than 10 mA (with R4 = 100 Ω); at startup (when V_S is provided to the IC) is less than 200 mA while the reverse voltage is about 10 V in all conditions. 1N4148 diodes withstand about 200 mA DC (1 A peak), and the maximum reverse voltage is 75 V, so they should fit for the majority of applications.

2.7 Sharing the Charge Pump Circuitry

If more than one device is used in the application, it's possible to use the charge pump from one L6235 to supply the V_{BOOT} pins of several ICs. The unused CP pins on the slaved devices are left unconnected, as shown in Figure 8. A 100 nF capacitor (C8) should be connected to the V_{BOOT} pin of each device.

Supply voltage pins (V_S) of the devices sharing the charge pump must be connected together.

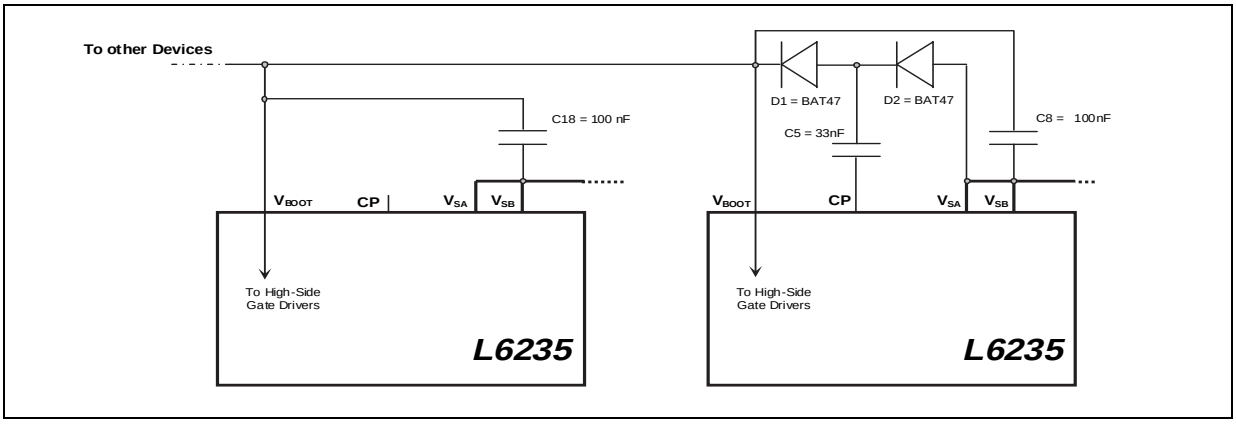
The higher the number of devices sharing the same charge pump, the lower will be the differential voltage available for gate drive (V_{BOOT} - V_S), causing a higher $R_{DS(ON)}$ for the high side DMOS, so higher dissipating power.

In this case it's recommended to omit the resistor on the CP pin, obtaining a higher current capability of the charge pump circuitry.

Better performance can also be obtained using a 33 nF capacitor for C5 and using schottky diodes (for example BAT47).

Sharing the same charge pump circuitry for more than 3÷4 devices is not recommended, since it will reduce the V_{BOOT} voltage increasing the high-side MOS on-resistance and thus power dissipation.

Figure 8. Sharing the charge pump circuitry.

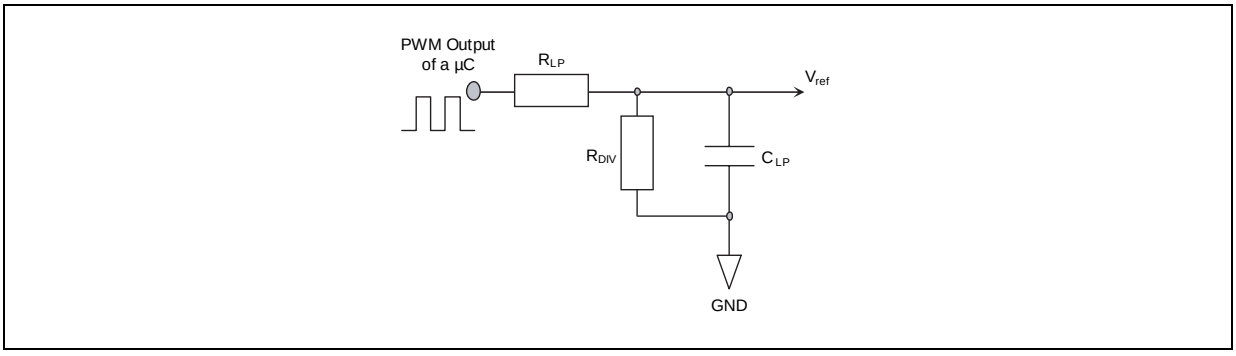


2.8 Reference Voltage for PWM Current Control

The device has an analog input, Vref, connected to the internal sense comparator, to control the peak value of the motor current through the integrated PWM circuitry. A fixed reference voltage can be easily obtained through a resistive divider from an available 5 V voltage rail (maybe the one supplying the µC or the rest of the application) and GND.

A very simple way to obtain a variable voltage without using a DAC is to low-pass filter a PWM output of a µC (see Figure 9).

Figure 9. Obtaining a variable voltage through a PWM output of a µC.



Assuming that the PWM output swings from 0 to 5V, the resulting average voltage will be

$$V_{ref} = \frac{5V \cdot D_{\mu C} \cdot R_{DIV}}{R_{LP} + R_{DIV}}$$

where $D_{\mu C}$ is the duty-cycle of the PWM output of the µC.

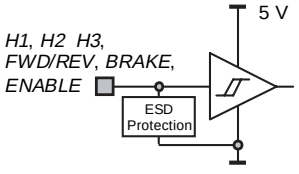
Assuming that the µC output impedance is lower than 1kΩ, with R_{LP} = 56kΩ, R_{DIV} = 15kΩ, C_{LP} = 10nF and a µC PWM switching from 0 to 5V at 100kHz, the low pass filter time constant is about 0.12 ms and the remaining ripple on the V_{ref} voltage will be about 20 mV. Using higher values for R_{LP}, R_{DIV} and C_{LP} will reduce the ripple, but the reference voltage will take more time to vary after changing the duty-cycle of the µC PWM, and too high values of R_{LP} will also increase the impedance of the V_{ref} net at low frequencies, causing a poor noise immunity.

As sensing resistor value is typically kept small, a small noise on V_{ref} input pins might cause a considerable error in the output current. It's then recommended to decouple this pin with a ceramic capacitor of some tens of nF, placed very close to Vref and GND pins. Note that Vref pin cannot be left unconnected, while, if connected to GND, zero current is not guaranteed due to voltage offset in the sense comparator. The best way to cut down (IC) power consumption and clear the load current is pulling down the EN pin. With very small reference voltage, PWM integrated circuitry can loose control of the current due to the minimum allowed duration of t_{ON} (see the Programmable off-time Monostable section).

2.9 Input Logic pins

H1, H2, H3, FWD/REV, BRAKE, ENABLE, are CMOS/TTL compatible logic input pins. The input comparator has been realized with hysteresis to ensure the required noise immunity. Typical values for turn-on and turn-off thresholds are $V_{TH(ON)}$ = 1.8 V and $V_{TH(OFF)}$ = 1.3 V. Pins are ESD protected (see Figure 10) (2kV human-body electro-static discharge), and can be directly connected to the logic outputs of a µC; a series resistor is generally not recommended, as it could help inducted noise to disturb the inputs. All logic pins enforce a specific behavior and cannot be left unconnected. If connected to the DIAG pin, EN pin must be driven through a series resistor of 2.2 kΩ minimum (for 5 V logic), to allow the voltage at the pin to be pulled below the turn-off threshold (see below).

Figure 10. Logic input pins.

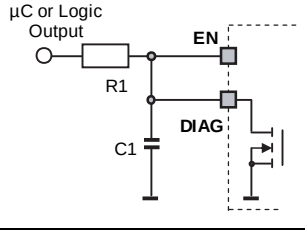


2.10 DIAG pin

DIAG pin is an open-drain output pulled to GND in case of overcurrent or over temperature conditions. Connecting this pin to EN will allow the internal open drain to disable all the power DMOS of the L6235, provided that the EN pin is driven through a resistor (see Input Logic pins).

A capacitor (C1 in Figure 5 and Figure 11) connected between EN and DIAG pins and GND is also recommended, to reduce the r.m.s. value of the output current when overcurrent conditions persist (see Over Current Protection section).

Figure 11. DIAG pin.



2.11 Programmable off-time Monostable

The L6235 includes a constant off time PWM Current Controller. The current control circuit senses the bridge current by sensing the voltage drop across an external sense resistor connected between the source of the three lower power MOS transistors and ground, as shown in Figure 12. As the current in the motor increases the voltage across the sense resistor increases proportionally. When the voltage drop across the sense resistor becomes greater than the voltage at the reference input pin VREF the sense comparator triggers the monostable switching the bridge off. The power MOS remain off for the time set by the monostable and the motor current recirculates around the upper half of the bridge in Slow Decay Mode as described in the next section. When the monostable times out, the bridge will again turn on. Since the internal dead time, used to prevent cross conduction in the bridge, delays the turn on of the power MOS, the effective Off Time t_{OFF} is the sum of the monostable time plus the dead time.

Figure 13 shows the typical operating waveforms of the output current, the voltage drop across the sensing resistor, the pin RC voltage and the status of the bridge. More details regarding the Synchronous Rectification and the output stage configuration are included in the next section.

Immediately after the Power MOS turn on, a high peak current flows through the sense resistor due to the reverse recovery of the freewheeling diodes. The L6235 provides a 1µs Blanking Time t_{BLANK} that inhibits the comparator output so that the current spike cannot prematurely retrigger the monostable.

Figure 12. PWM Current Controller Simplified Schematic

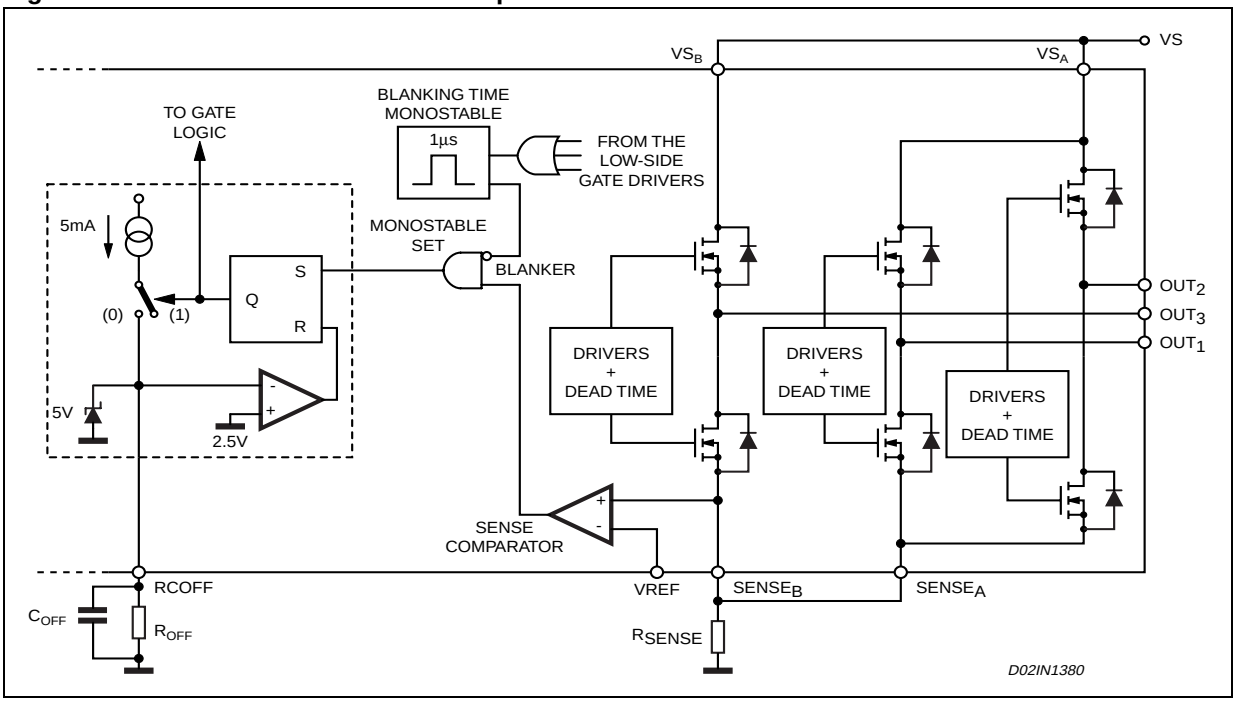


Figure 13. Output Current Regulation Waveforms

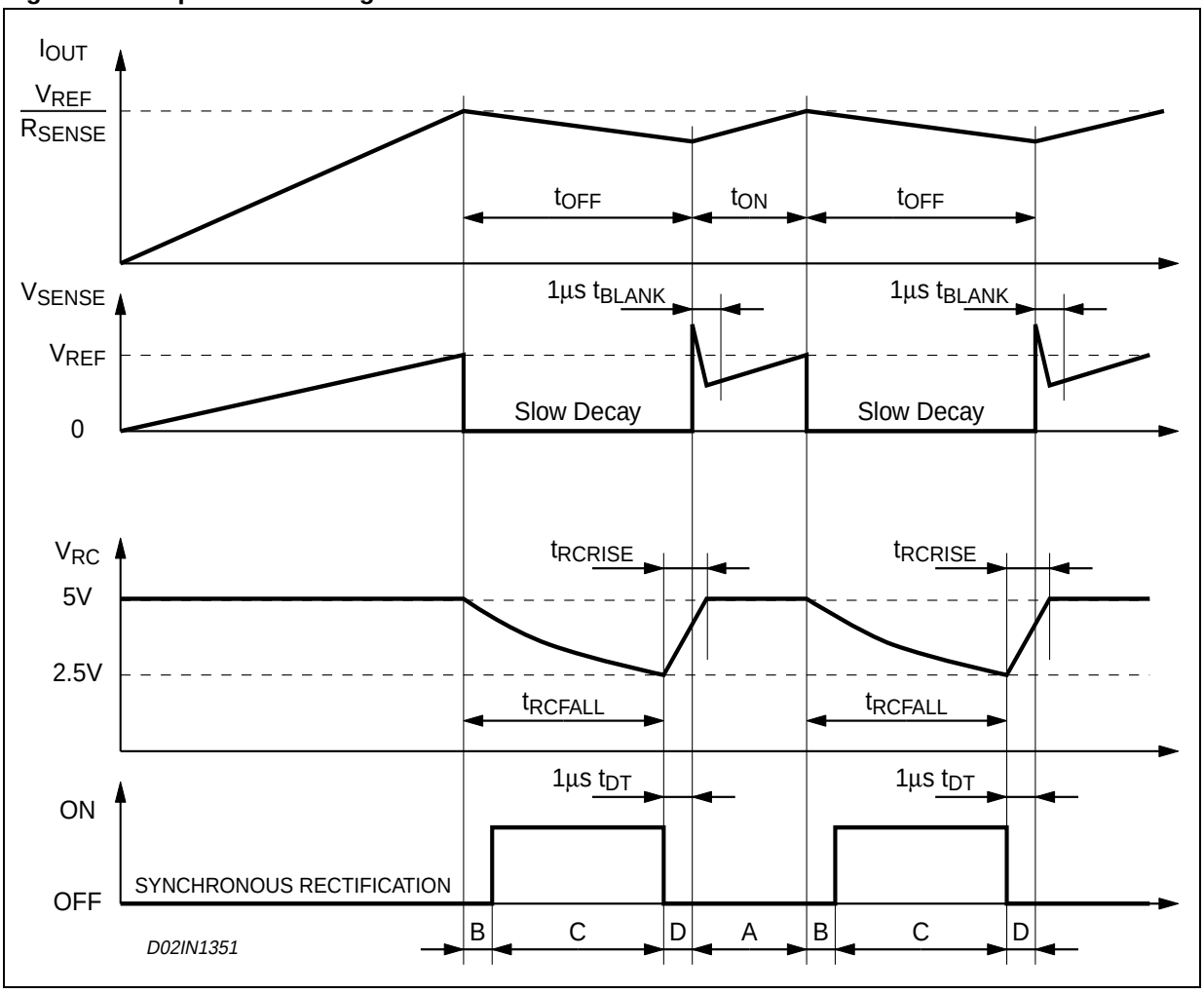


Figure 14 shows the magnitude of the Off Time t_{OFF} versus C_{OFF} and R_{OFF} values. It can be approximately calculated from the equations:

$t_{RCFALL} = 0.6 \cdot R_{OFF} \cdot C_{OFF}$

$t_{OFF} = t_{RCFALL} + t_{DT} = 0.6 \cdot R_{OFF} \cdot C_{OFF} + t_{DT}$

where R_{OFF} and C_{OFF} are the external component values and t_{DT} is the internally generated Dead Time with:

$20K\Omega \leq R_{OFF} \leq 100K\Omega$

$0.47nF \leq C_{OFF} \leq 100nF$

$t_{DT} = 1\mu s$ (typical value)

Therefore:

$t_{OFF(MIN)} = 6.6\mu s$

$t_{OFF(MAX)} = 6ms$

These values allow a sufficient range of t_{OFF} to implement the drive circuit for most motors.

The capacitor value chosen for C_{OFF} also affects the Rise Time t_{RCRISE} of the voltage at the pin RC_{OFF}. The Rise Time t_{RCRISE} will only be an issue if the capacitor is not completely charged before the next time the monostable is triggered. Therefore, the On Time t_{ON}, which depends by motors and supply parameters, has to be bigger than t_{RCRISE} for allowing a good current regulation by the PWM stage. Furthermore, the On Time t_{ON} can not be smaller than the minimum on time $t_{ON(MIN)}$.

$$\begin{cases} t_{ON} > t_{ON(MIN)} = 1.5\mu s \text{ (typ. value)} \\ t_{ON} > t_{RCRISE} - t_{DT} \end{cases}$$

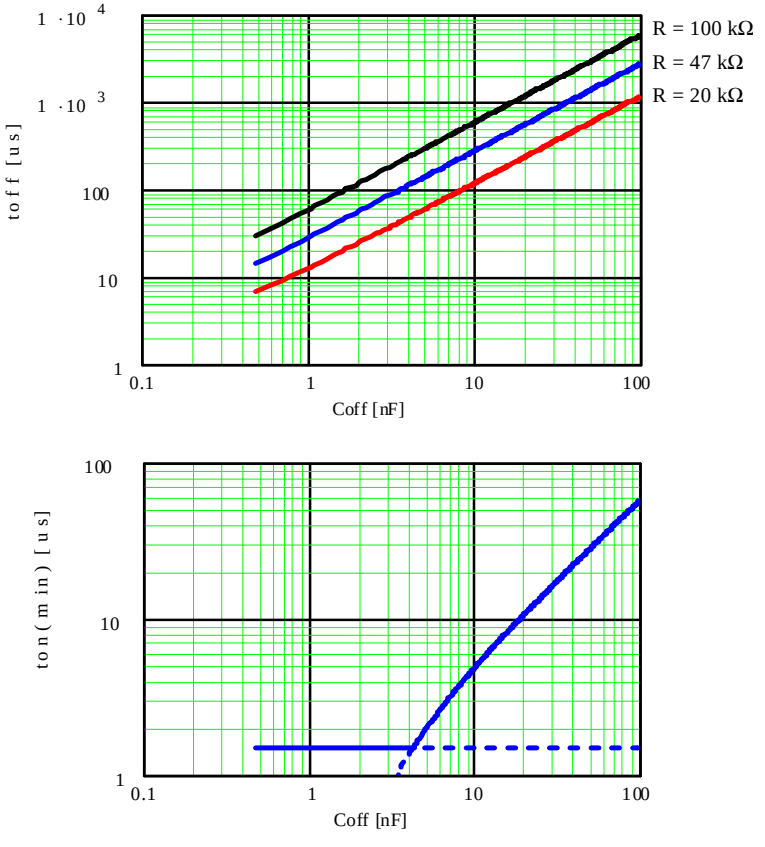
$$t_{RCRISE} = 600 \cdot C_{OFF}$$

2.11.1 Off-time Selection and minimum on-time

Figure 14 also shows the lower limit for the On Time t_{ON} for having a good PWM current regulation capacity. It has to be said that t_{ON} is always bigger than $t_{ON(MIN)}$ because the device imposes this condition, but it can be smaller than t_{RCRISE} - t_{DT}. In this last case the device continues to work but the Off Time t_{OFF} is not more constant.

So, small C_{OFF} value gives more flexibility for the applications (allows smaller On Time and, therefore, higher switching frequency), but, the smaller is the value for C_{OFF}, the more influential will be the noises on the circuit performance.

Figure 14. Off-time selection and minimum on-time.

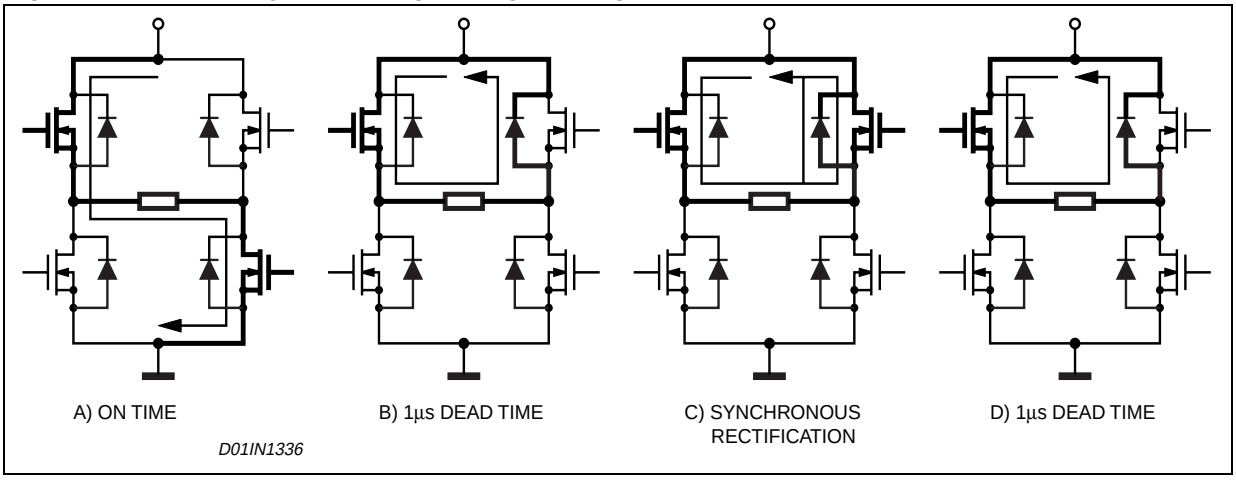


2.11.2 Slow Decay Mode

Figure 15 shows the operation of the bridge in the Slow Decay mode during the Off Time. At any time only two legs of the three-phase bridge are active, therefore only the two active legs of the bridge are shown in the figure and the third leg will be off. At the start of the Off Time, the lower power MOS is switched off and the current

recirculates around the upper half of the bridge. Since the voltage across the coil is low, the current decays slowly. After the Dead Time the upper power MOS is operated in the synchronous rectification mode reducing the impedance of the freewheeling diode and the related conducting losses. When the monostable times out, upper MOS that was operating the synchronous mode turns off and the lower power MOS is turned on again after some delay set by the Dead Time to prevent cross conduction.

Figure 15. Slow Decay Mode Output Stage Configurations

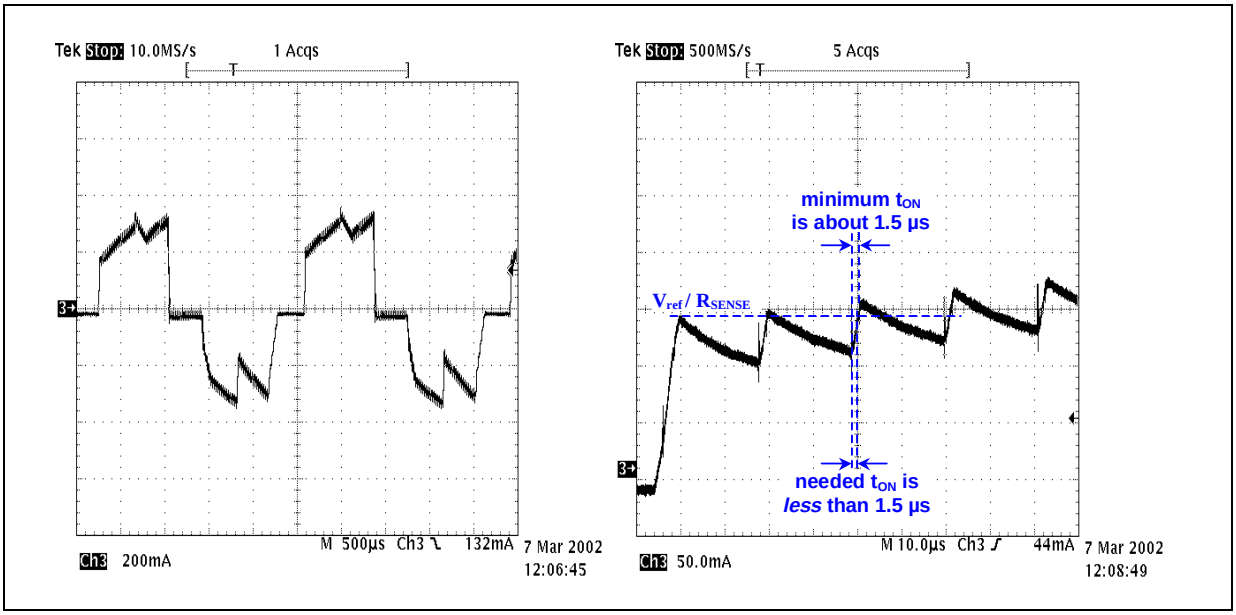


In some conditions (short off-time, very low regulated current, high motor winding L / R) the system may need an on-time shorter than 1.5 µs. In these cases the PWM current controller can loose the regulation.

Figure 16 shows the operation of the circuit in this condition. When the current first reaches the threshold, both the high-side are turned on for a fixed time and the current decays.

During the following on-time current increases above the threshold, but the bridge cannot be turned off until the minimum on-time expires. Since current increases more in each on-time than it decays during the off-time, it keeps growing during each cycle, with steady state asymptotic value set by duty-cycle and load DC resistance: the resulting peak current will be $I_{pk} = V_S \times D / R_{LOAD}$, where $D = t_{ON} / (t_{ON}+t_{OFF})$ is the duty-cycle and R_{LOAD} is the load resistance.

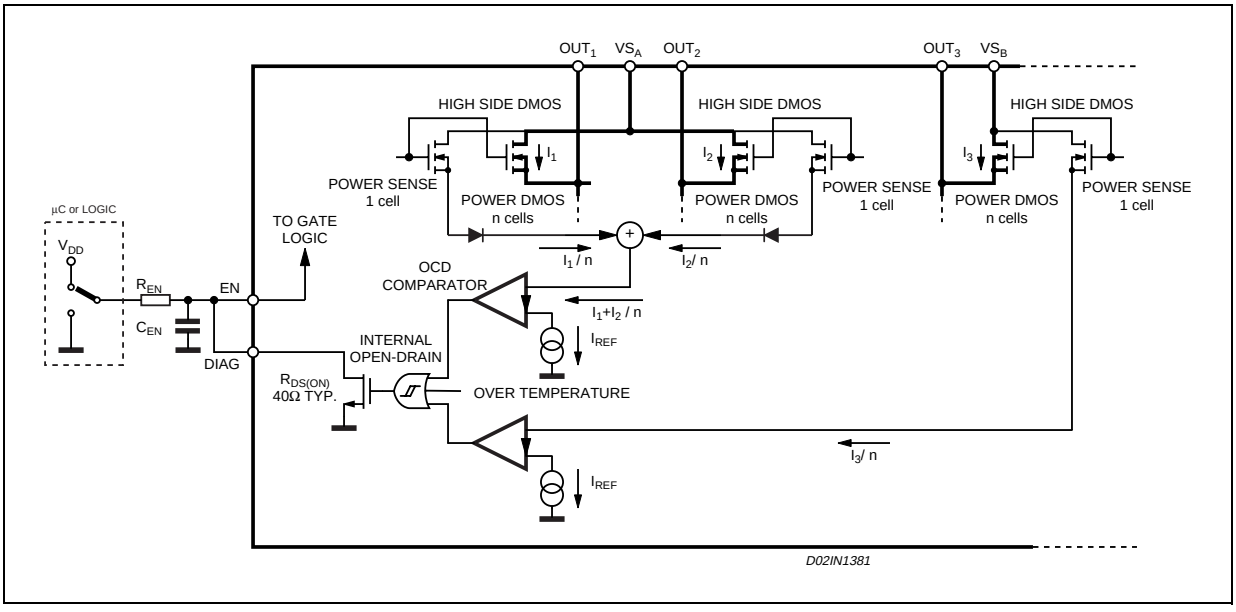
Figure 16. Minimum on-time can cause the PWM controller to loose the regulation.



2.12 Over Current Detection

To implement an Over Current (i.e. short circuit) Protection, a dedicated Over Current Detection (OCD) circuitry (see Figure 17 for a simplified schematic) senses the current in each high side. Power DMOS are actually made up with thousands of individual identical cells, each carrying a fraction of the total current flowing. The current sensing element, connected in parallel to the Power DMOS, is made only with few such cells, having a 1:N ratio compared to the power DMOS. The total drain current is split between the output and the sense element according to the cell ratio. Sensed current is, then, a small fraction of the output current and will not contribute significantly to power dissipation.

Figure 17. Over Current Detection simplified circuitry.



This sensed current is compared to an internally generated reference to detect an over current condition. An internal open drain mosfet turns on when the sum of the currents in the bridges 1 and 2 or the current in the bridge 3 reaches the threshold (5.6A typical value); the open drain is available at the DIAG pin for diagnostic purposes or to ensure an over current protection, connecting EN and DIAG together and using an RC network (see Figure 17).

Figure 18. Over Current Operation after a short circuit between an OUT pin and GND. EN and DIAG pins are connected together.

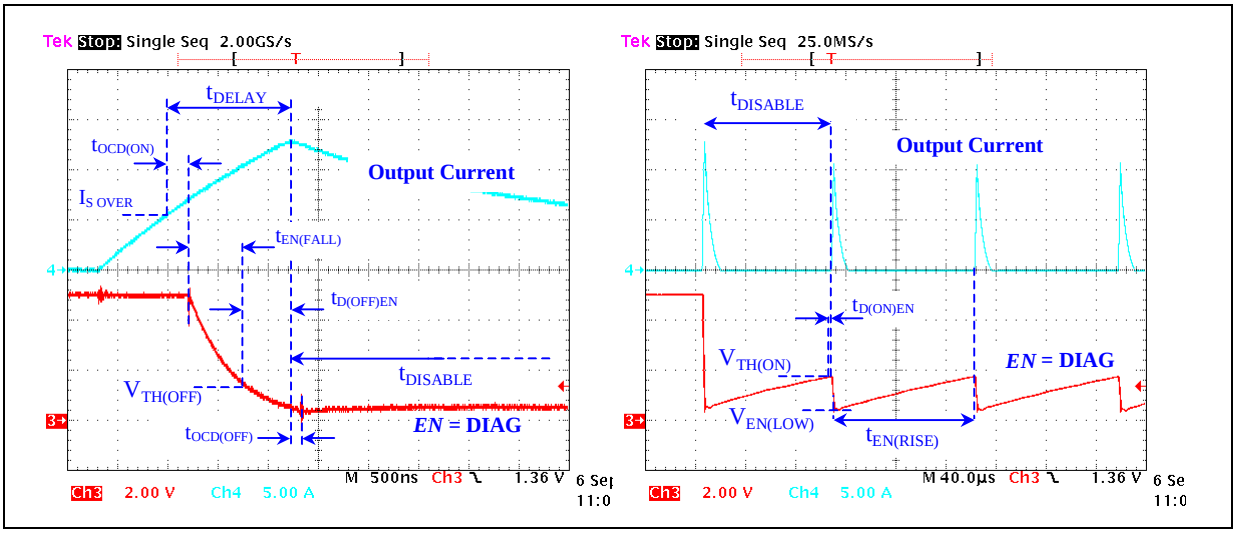


Figure 18 shows the device operating in overcurrent condition (short to ground). When an over current is detected the internal open drain mosfet pulls the EN pin to GND switching off all 6 power DMOS of the device and allowing the current to decay. Under a persistent over current condition, like a short to ground or a short between two output pins, the external RC network on the EN pin (see Figure 17) reduces the r.m.s. value of the output current by imposing a fixed disable-time after each over current occurrence. The values of R_{EN} and C_{EN} are selected to ensure proper operation of the device under a short circuit condition. When the current flowing through the high side DMOS reaches the OCD threshold (5.6 A typ.), after an internal propagation delay ($t_{OCD(ON)}$) the open drain starts discharging C_{EN}. When the EN pin voltage falls below the turn-off threshold ($V_{TH(OFF)}$) all the Power DMOS turn off after the internal propagation delay ($t_{D(OFF)EN}$). The current begins to decay as it circulates through the freewheeling diodes. Since the DMOS are off, there is no current flowing through them and no current to sense so the OCD circuit, after a short delay ($t_{OCD(OFF)}$), switches the internal open drain device off, and R_{EN} can charge C_{EN}. When the voltage at EN pin reaches the turn-on threshold ($V_{TH(ON)}$), after the $t_{D(ON)EN}$ delay, the DMOS turn on and the current restarts. Even if the maximum output current can be very high, the external RC network provides a disable time ($t_{DISABLE}$) to ensure a safe r.m.s. value (see Figure 18).

The maximum value reached by the current depends on its slew-rate, so on the short circuit nature and supply voltage, and on the total intervention delay (t_{DELAY}). It can be noticed that after the first current peak, the maximum value reached by the output current becomes lower, because the capacitor on EN and DIAG pins is discharged starting from a lower voltage, resulting in a shorter t_{DELAY}.
The following approximate relations estimate the disable time and the first OCD intervention delay after the short circuit (worst case).

The time the device remains disabled is:

$$t_{DISABLE} = t_{OCD(OFF)} + t_{EN(RISE)} + t_{D(ON)EN}$$

$$t_{EN(RISE)} = R_{EN} \cdot C_{EN} \cdot \ln\left(\frac{V_{DD} - V_{EN(LOW)}}{V_{DD} - V_{TH(ON)}}\right)$$

$V_{EN(LOW)}$ is the minimum voltage reached by the EN pin, and can be estimated with the relation:

$$V_{EN(LOW)} = V_{TH(OFF)} \cdot e^{\left(\frac{t_{D(OFF)} + t_{OCD(OFF)}}{R_{OPDR} \cdot C_{EN}}\right)}$$

The total intervention time is

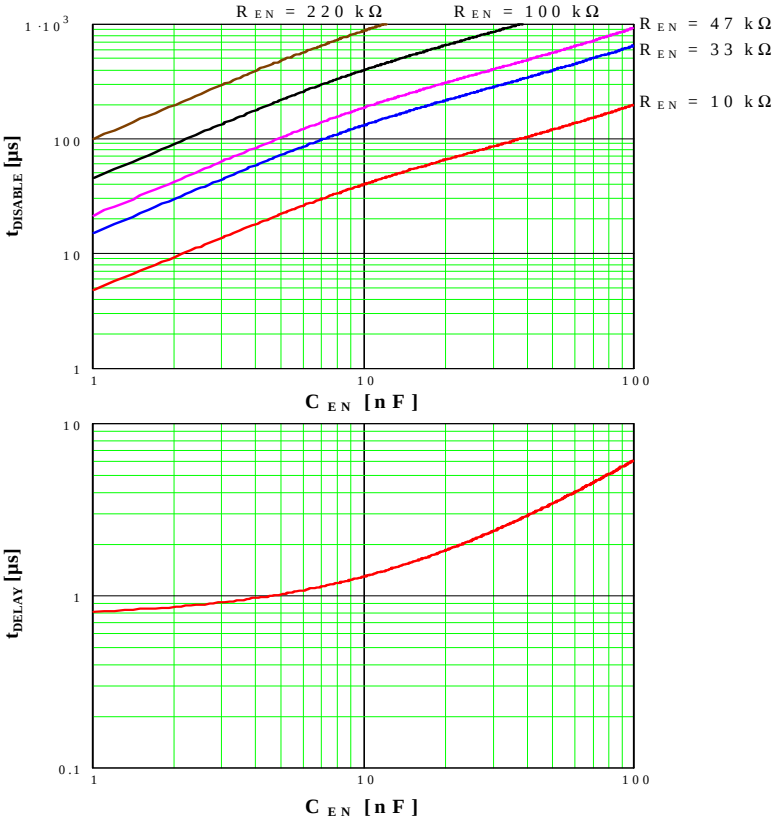
$$t_{DELAY} = t_{OCD(ON)} + t_{EN(FALL)} + t_{D(OFF)EN}$$

where

$$t_{EN(FALL)} = R_{OPDR} \cdot C_{EN} \cdot \ln\left(\frac{V_{DD}}{V_{TH(OFF)}}\right)$$

$t_{OCD(OFF)}$, $t_{OCD(ON)}$, $t_{D(ON)EN}$, $t_{D(OFF)EN}$, and R_{OPDR} are device intrinsic parameters, V_{DD} is the pull-up voltage applied to R_{EN}.
The external RC network, C_{EN} in particular, must be chosen obtaining a reasonable fast OCD intervention (short t_{DELAY}) and a safe disable time (long $t_{DISABLE}$). Figure 19 shows both $t_{DISABLE}$ and t_{DELAY} as a function of C_{EN}: at least 100µs for $t_{DISABLE}$ are recommended, keeping the delay time below 1÷2µs at the same time.
The internal open drain can also be turned on if the device experiences an over temperature (OVT) condition. The OVT will cause the device to shut down when the die temperature exceeds the OVT threshold (T_J>165 °C typ.).
Since the OVT is also connected directly to the gate drive circuit (see Figure 1), all the Power DMOS will shut down, even if EN pin voltage is still over $V_{th(OFF)}$. When the junction temperature falls below the OVT turn-off threshold (150 °C typ.), the open drain turns off, C_{EN} is recharged up to $V_{TH(ON)}$ and then the PowerDMOS are turned on back.

Figure 19. Typical disable and delay time as a function of C_{EN}, for several values of R_{EN}.

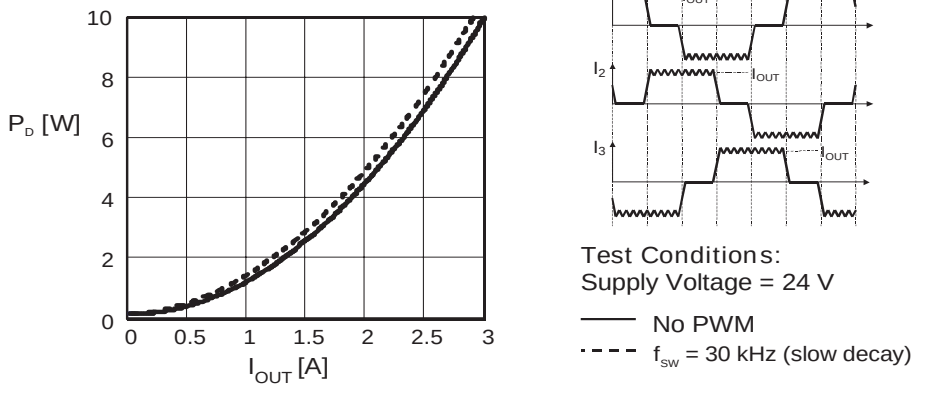


2.13 Power Management

Even when operating at current levels well below the maximum ratings of the device, the operating junction temperature must be kept below 125 °C.

Figure 20 shows the IC dissipated power versus the r.m.s. load current, in 4 different driving sequences, assuming the supply voltage is 24V.

Figure 20. IC Dissipated Power versus Output Current.

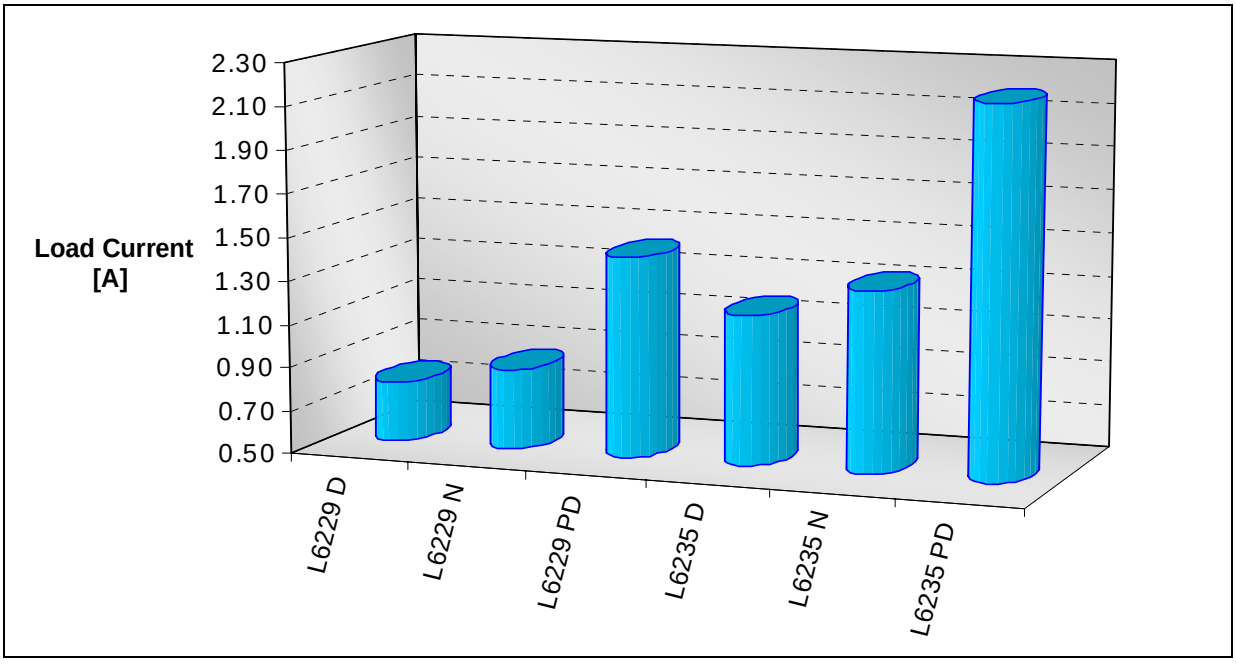


2.13.1 Maximum output current vs. selectable devices

Figure 21 reports a performance comparison between L6229 (std. power) and L6235 (high power) for different packages, with the following assumptions:

- Supply voltage: 24 V; Switching frequency: 30 kHz.
- T_{amb} = 25 °C, T_J = 125 °C.
- Maximum $R_{DS(ON)}$ (taking into account process spread) has been considered, @ 125 °C.
- Maximum quiescent current I_Q (taking into account process spread) has been considered.
- PCB is a FR4 with a dissipating copper surface on the top side of 6 cm^2 (with a thickness of 35 µm) for SO and PowerDIP packages (D, N suffixes).
- PCB is a FR4 with a dissipating copper surface on the top side of 6 cm^2 (with a thickness of 35 µm), 16 via holes and a ground layer for the PowerSO package (PD suffix).
- For each device (on the x axis) y axis reports the maximum output current.

Figure 21. Maximum output current vs. selectable devices.



2.13.2 Power Dissipation Formulae

Figure 22 to Figure 25 are screenshots of a spreadsheet that helps calculating power dissipation in specified conditions (application and motor data), and estimates the resulting junction temperature for a given package and copper area available on the PCB [3].

The model considers power dissipation during the on-time and the off-time, taking into account the selected decay, rise and fall time (when a phase change occurs), the switching losses and the quiescent current power dissipation.

Figure 22. Current in the three phases and the signal of one of the hall effect sensors.

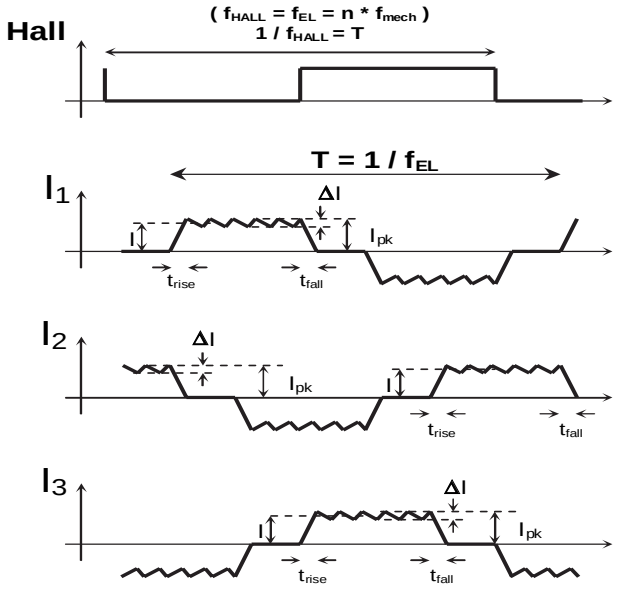


Figure 23. Input Data.

Input Data

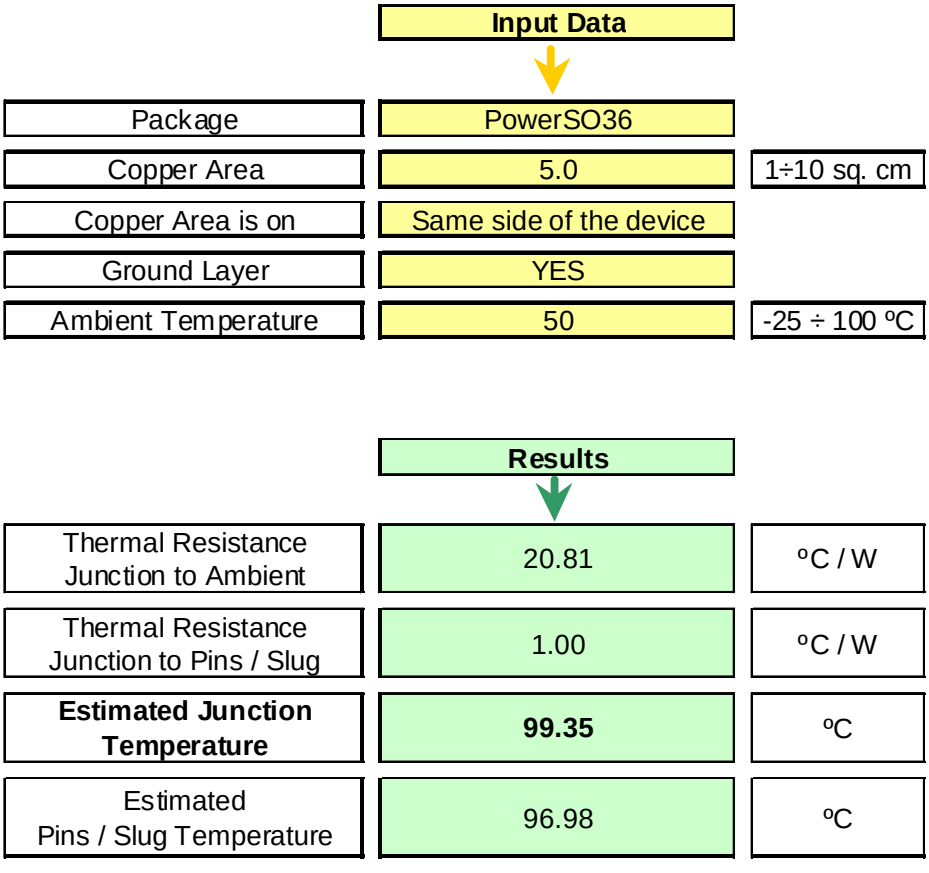
Device Input Values				
Maximum Drain-Source ON Resistance	Ron	=	5.60E-01	[Ω]
Maximum diode voltage	Vd	=	1.20E+00	[V]
Quiescent Current	Iq	=	5.50E-03	[A]
Motor Input Values				
Maximum BEMF Voltage	Vb	=	1.00E+01	[V]
Motor Inductance	Lm	=	8.00E-04	[H]
Motor Resistance	Rm	=	2.10E+00	[Ω]
Polar Couples	n	=	1	-
Application Input Values				
Supply Voltage	Vs	=	2.40E+01	[V]
Peak Current	Ipk	=	1.50E+00	[A]
Off-Time	tOFF	=	8.00E-06	[s]
Sensing Resistance	Rs	=	3.30E-01	[Ω]
Motor Speed	sp	=	1.00E+04	[rpm]

Average Value between High-Side and Low-Side

Figure 24. Power Dissipation formulae and results.

		Result		
PowerDMOS Commutation Time	Tcom =	9.60E-08	[s]	Vs / (250V/µs)
Electrical frequency	Fel =	1.67E+02	[Hz]	n*sp/60
Rise Time	Trise =	5.65E-5	[s]	$-\ln\left[\frac{(-Ipk\cdot Rm-2\cdot 2Ipk\cdot Ron-Ipk\cdot Rs+Vs)}{Vs}\right]\cdot\frac{Lm}{Rm+Rs+2Ron}$
Fall Time	Tfall =	5.13E-05	[s]	$-\ln\left[\frac{Vs-2\cdot Vd}{(Ipk\cdot Rm+Ipk\cdot Rs+Vs-(2\cdot Vd))}\right]\cdot\frac{Lm}{(Rm+Rs)}$
Duty Cycle	D =	6.08E-01	-	Vb+I(2*Ron+Rm))/(Vs -I*Rs)
Switching Frequency	fSW =	4.90E+04	[Hz]	(1-D) / tOFF
Current Ripple	ΔI =	3.19E-01	[A]	2.1*((2Ron+Rm)*Ipk+Vb)*toff/Lm
Period	T =	6.00E-03	[s]	1 / fel
Load Time	Tload =	5.66E-03	[s]	T-6Trise
Average Current during Load Time	I =	1.34E+00	[A]	$Ipk-\frac{\Delta I}{2}$
r.m.s. Current during Load Time	Irms =	1.34E+00	[A]	$\sqrt{Ipk\cdot(Ipk-\Delta I)+\frac{\Delta I^2}{3}}$
Rise Time Dissipating power	Prise =	1.58E-02	[W]	$\left(2Ron\cdot Ipk^2\cdot\frac{Trise}{3}\right)\cdot\frac{2}{T}$
Fall Time Dissipating power	Pfall =	3.00E-02	[W]	$\frac{2}{T}\cdot 2\cdot Vd\left[Tfall\cdot\frac{(-Vs+2\cdot Vd)}{(Rm+Rs)}+Lm\cdot(Ipk\cdot Rm+Ipk\cdot Rs+Vs-2\cdot Vd)\cdot\frac{\left[1-\exp\left[\frac{-Tfall}{Lm}\cdot(Rm+Rs)\right]\right]}{(Rm+Rs)^2}\right]$
Load Time Diss. Power	Pload =	1.91E-00	[W]	$(2Ron\cdot Irms^2\cdot Tload)/T$
Commutation Dissipating Pw	Pcom =	2.86E-01	[W]	(2Vs · I · Tcom · Tload · fSW) / T
Quiescent Dissipating Pw	Pq =	1.32E-01	[W]	Vs · Iq
Total Dissipating Power	P =	2.37E+00	[W]	Pq + Pcom + Pload + Pfall + Prise

Figure 25. Thermal Data inputs and results



2.14 The decoding logic

The L6235 integrated decoding logic provides the correct sequence on the three outputs for motors with both 60° and 120° spaced hall effect sensors signals. The sensors' outputs are directly connected to the H1, H2, H3 inputs of the device. The table below reports the output configurations for all possible hall effect input signals.

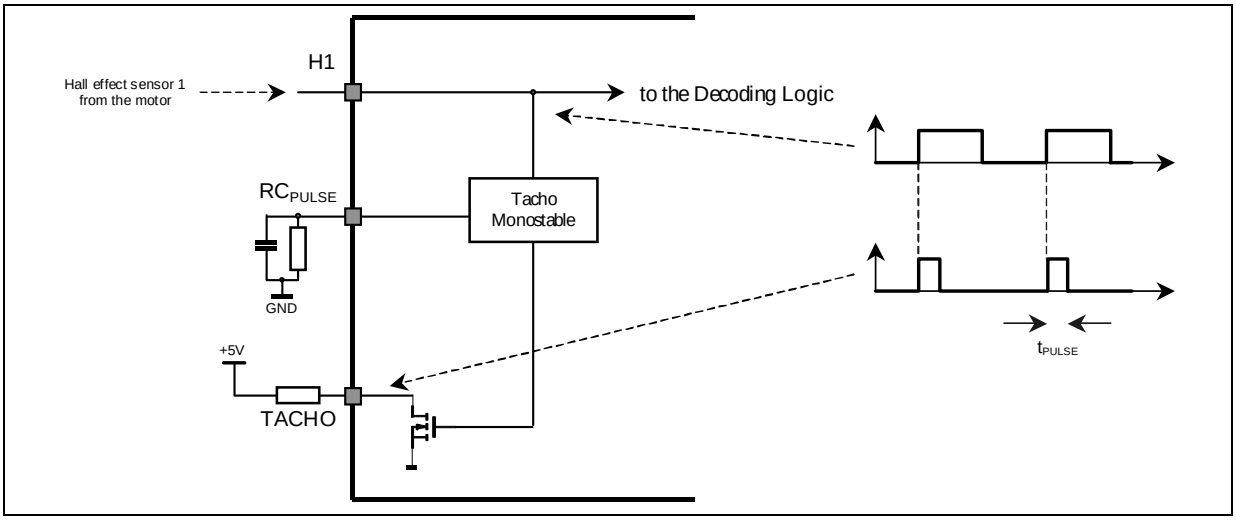
Hall 120°	1	2	3a	-	4	5	6a	-
Hall 60°	1	2	-	3b	4	5	-	6b
H_1	H	H	L	H	L	L	H	L
H_2	L	H	H	H	H	L	L	L
H_3	L	L	L	H	H	H	H	L
OUT_1	Vs	High Z	GND	GND	GND	High Z	Vs	Vs
OUT_2	High Z	Vs	Vs	Vs	High Z	GND	GND	GND
OUT_3	GND	GND	High Z	High Z	Vs	Vs	High Z	High Z
Phasing	1->3	2->3	2->1	2->1	3->1	3->2	1->2	1->2

2.15 Tacho Output and Speed Loop

H1 input is internally connected to a monostable that provides, through an open drain mosfet, a fixed width pulse on the tacho output (see Figure 26). Through this output realizing a speed loop is very easy and inexpensive.

Providing an external pull-up resistor on this open drain output, the resulting waveform at the pin will be a square-wave whose frequency is proportional to the motor rotation speed, with a fixed on-time (t_{PULSE}) set by an external RC network connected at the RC_{PULSE} pin.

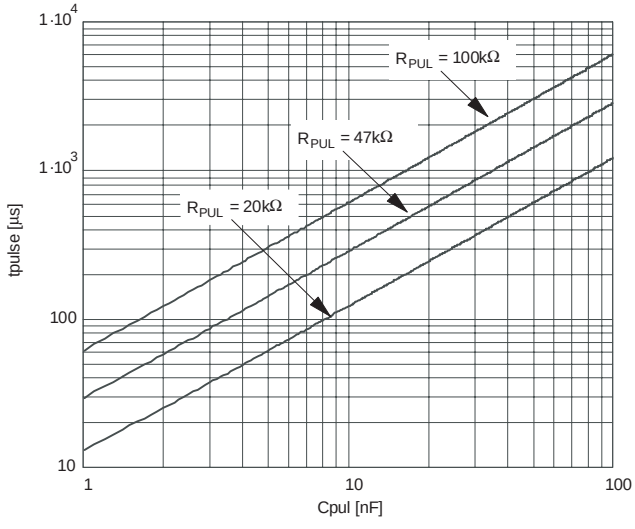
Figure 26. Tacho monostable.



Tacho monostable is identical to RCoff monostable, and the fixed pulse time is defined by:

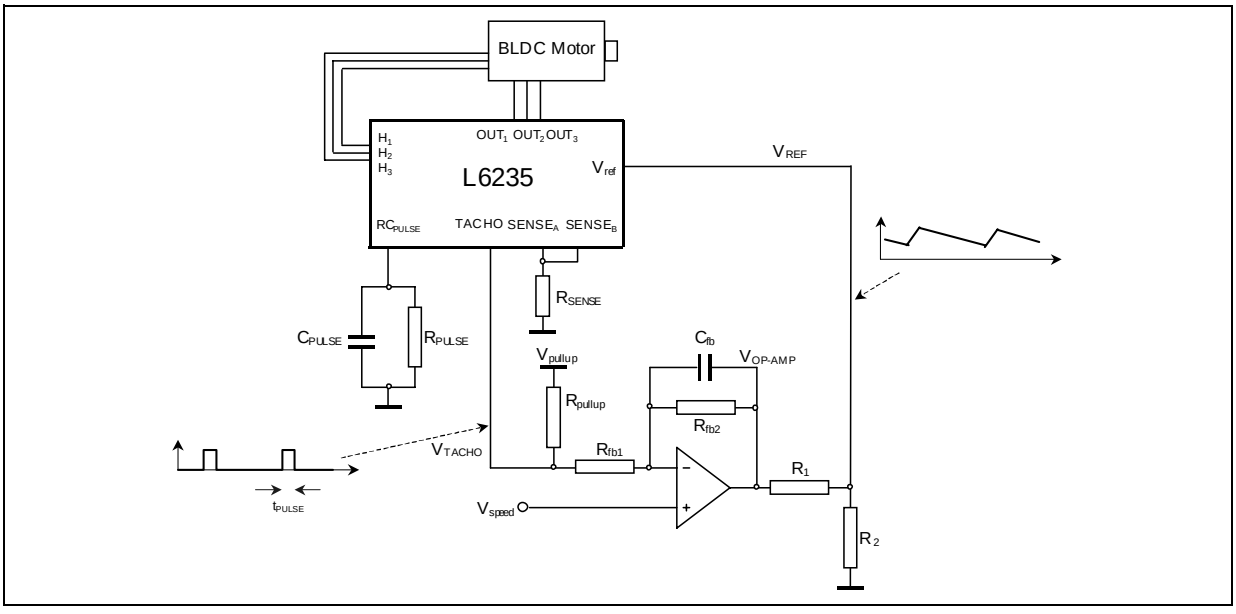
$$t_{pulse} \cong 0.6 R_{PULSE} C_{PULSE}$$

Figure 27. tacho pulses selection.



Also the duty cycle of this signal, so its average value is proportional to the motor rotation speed. Simply integrating the square-wave a voltage proportional to the motor speed will be available to realize a speed loop, as in Figure 28: R_{PULSE} and C_{PULSE} define the fixed on-time (t_{PULSE}) of the tacho output, integrated and compared to a voltage proportional to the desired speed (V_{speed}) by the op-amp; the output of the op-amp represents the speed error signal. Providing this signal to the Vref input of the L6235, which sets the current in the motor windings, the speed error will act on the motor modifying its torque, in order to maintain the speed at a constant value. R1 and R2 set the maximum current in the motor by limiting the voltage at the V_{ref} pin.

Figure 28. Tacho output allows easy implementation of a speed loop.



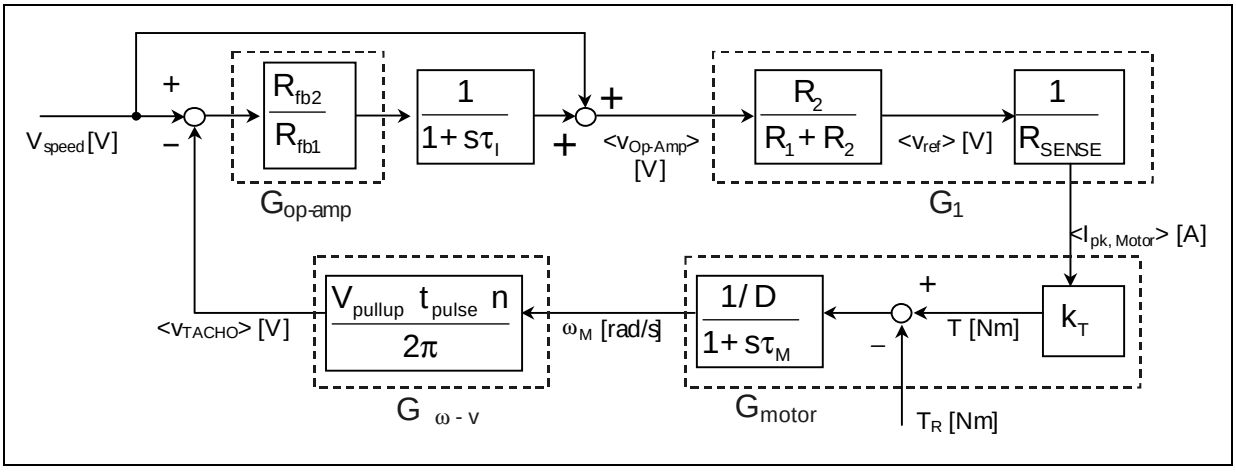
Defining

K_T	Motor torque constant	[Nm/A]
D	Dynamic friction torque	[Nms/rad]
J	Motor + Load inertia moment	[kgm2]
T_R	Load resistant torque	[Nm]
$\tau_M = J/D$	Mechanical time constant	[s]
n	Number of polar couples	
ω_m	Motor rotation speed	[rad/s]
$f_{tacho} = n\omega_m / 2\pi$	Tacho output frequency	[Hz]
$\tau_I = C_{fb} \cdot R_{fb2}$	Integrator time constant	[s]
$G_{op\text{-}amp} = R_{fb2} / R_{fb1}$		
$G_{w\text{-}v} = V_{pullup} \cdot n \cdot t_{pulse} / 2\pi$		[Vs/rad]
$G_1 = R_2 / R_{SENSE} \cdot (R_1 + R_2)$		[1/Ω]

and neglecting the current ripple due to PWM control, the expression of the control loop transfer function (see Figure 29) is:

$$G_{loop}(s) = \frac{-G_{op-amp} \cdot G_{\omega-v} \cdot G_1 \cdot k_T}{D \cdot (1 + s\tau_I) \cdot (1 + s\tau_M)}$$

Figure 29. Control loop block diagram.



Can be noticed that since the motor is current controlled, the electrical time constant of the motor (L/R) does not appear in any transfer function.

With the following values, module and phase of G_{loop} are shown in Figure 30.

K_T = 9.8 mNm/A

D = 3.34 µNms/rad

J = 6.5 µkgm^2

T_R = 4 mNm

τ_M = J/D = 1.95 s (mechanical pole at 0.08 Hz)

n = 2

ω_m = 2618 rad/s (25000 r.p.m.)

$f_{tacho} = n\omega_m / 2\pi$ = 833 Hz

V_{pullup} = 5V

t_{pulse} = 1 ms

R_{fb1} = 100 kΩ

R_{fb2} = 1 MΩ

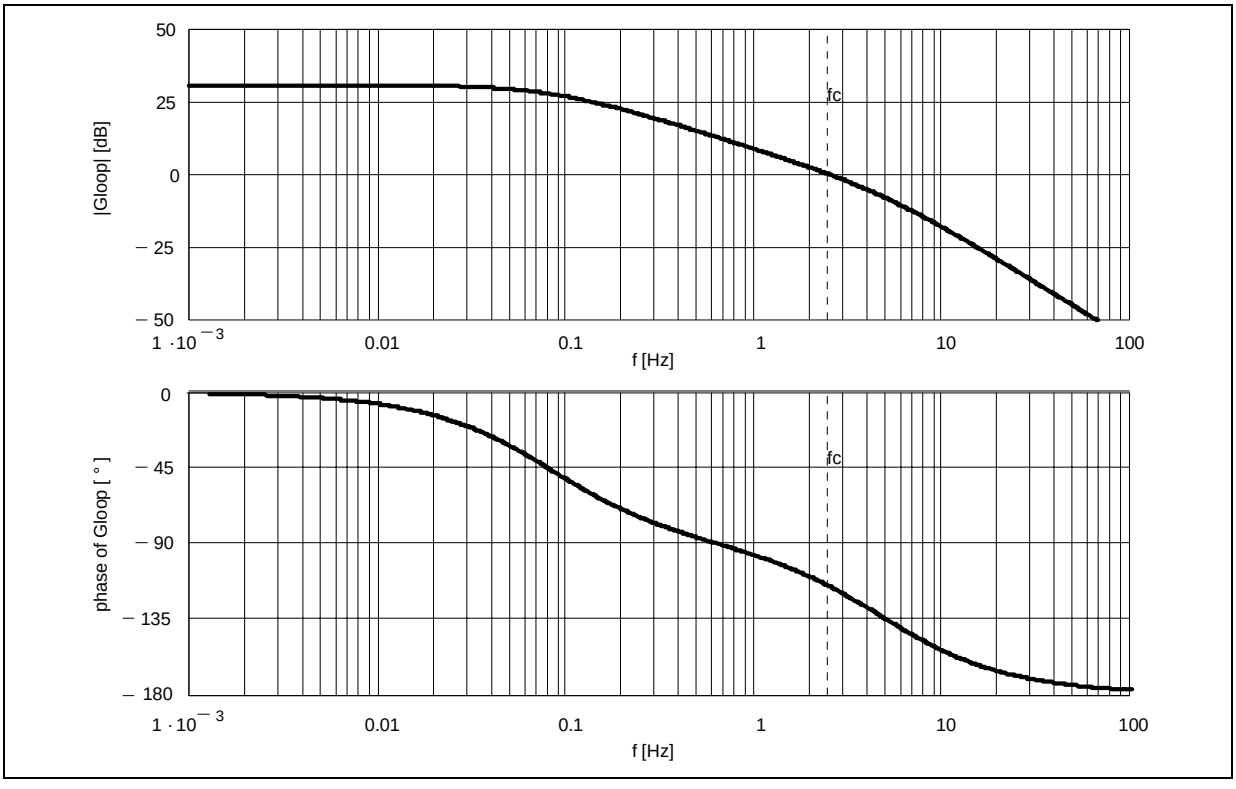
C = 33 nF

R_1 = 5.6 kΩ

R_2 = 1.8 kΩ

R_{SENSE} = 0.33Ω

Figure 30. G_{loop} module and phase.



The relation between the speed reference voltage (V_{speed}), the load resistant torque (T_b) and the motor speed (ω_M) is given by the expression:

$$\omega_M = \frac{V_{speed} \cdot \left(1 + \frac{G_{op-amp}}{1 + s\tau_I}\right) \cdot G_1 \cdot k_T - T_b}{D + (1 \cdot s\tau_M) + G_{\omega-v} \cdot G_1 \cdot k_T \cdot \frac{G_{op-amp}}{1 + s\tau_I}}$$

for a given speed, the speed reference voltage to apply is:

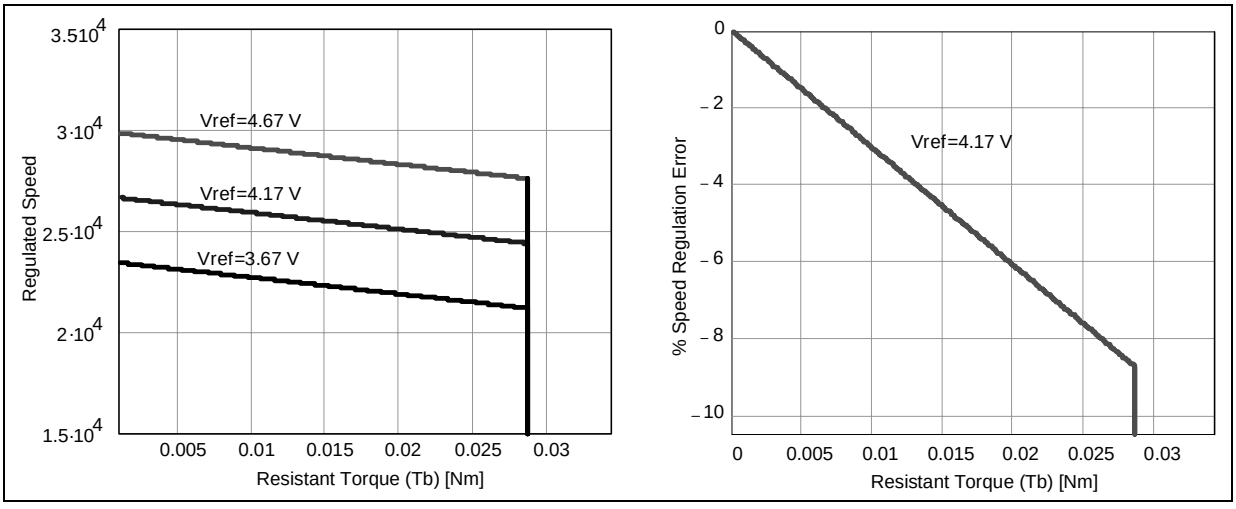
$$V_{speed} = \frac{\omega_M \cdot (D + G_{\omega-v} \cdot G_1 \cdot k_T \cdot G_{op-amp}) + T_b}{(1 + G_{op-amp}) \cdot G_1 \cdot k_T}$$

Designing the speed loop, care must be taken choosing the values of R_{pullup}, R_{fb1}, R_{fb2}, C_{fb}, R_1 and R_2 obtaining a good compromise between static performance, dynamic performance, stability and torque ripple:

2.15.1 Static performance - Speed Regulation vs. Resistant Torque:

The relation between V_{speed}, T_b and ω_M shows that for a fixed speed reference, the load torque (T_b) affects the speed. To minimize the resistant torque effect the term ($D + G\omega\text{-}v \cdot G_1 \cdot k_T \cdot G_{op\text{-}amp}$) must be kept as high as possible.
Figure 31 shows how the speed changes with the load torque, and percentage regulation error.
Due to the op-amp output voltage saturation, beyond a certain load torque value the system cannot produce further torque, then the motor speed drastically decreases.

Figure 31. Regulated speed variations versus mechanical load.



2.15.2 Dynamic performance:

The loop bandwidth is the frequency range in which the loop gain is greater than 1 (0 dB). In the example it's about 2.5 Hz. It expresses how fast will the loop regulate the speed after load changes.

The transfer function between the resistant torque and the motor speed is

$$\frac{\omega_M(s)}{T_b(s)} = \frac{\frac{-(1+s\tau_1)}{D}}{(1+s\tau_M)\cdot(1+s\tau_l)+\frac{1}{D}\cdot G_{\omega-v}\cdot G_{op-amp}\cdot G_1\cdot k_T} \quad ,$$

while between speed reference voltage and speed we have:

$$\frac{\omega_M(s)}{V_{speed}(s)} = \frac{\left(1+\frac{G_{op-amp}}{1+s\tau_l}\right)\cdot G_1\cdot k_T}{D\cdot(1+s\tau_M)+G_{\omega-v}\cdot G_1\cdot k_T\cdot\frac{G_{op-amp}}{1+s\tau_l}}$$

Figure 32 and Figure 33 show how the speed changes after applying a 1mN resistant torque step and a 1V speed voltage step, respectively

Figure 32. Speed response to a 1mNm resistant torque step

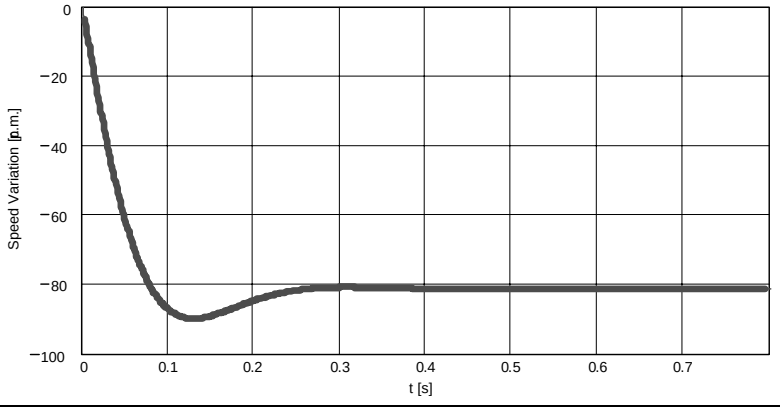
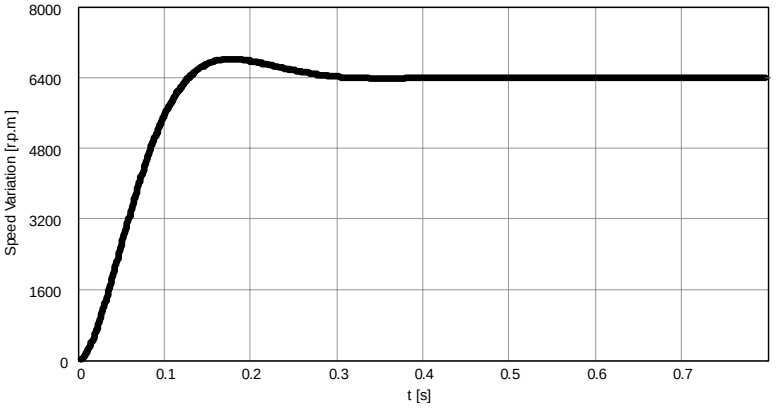


Figure 33. Speed response to a 1V speed voltage step.



2.15.3 Loop Stability:

The phase margin is defined as 180° minus the phase of Gloop at the cut frequency (where Gloop=1). It should be at least 45° to guarantee the stability. In the example it's about 65°.

2.15.4 Reference voltage ripple:

Due to the tacho waveform integration, the reference voltage provided to the L6235 V_{ref} input is a triangular wave (see Figure 27). The ripple can be calculated through the approximate relation:

$$\Delta V_{ref} = \frac{speedref \cdot (1 - DC)}{R_{fb1} \cdot f_{tacho} \cdot C_{fb}} \cdot \frac{R_2}{R_1 + R_2},$$

where DC is the duty-cycle of the square wave at the tacho output:

$$DC = \frac{n \cdot t_{pulse} \cdot \omega_m}{2\pi}$$

Since this reference voltage is the torque control voltage, the ripple should be kept as low as possible, accordingly to others main parameters. In the example the ripple is about 60 mV.

The limits of this system depend on the fact that the speed information is obtained by an analog integration of the TACHO output. This operation introduces a low frequency pole in the GI_{oop} function, and a ripple in the reference voltage. The introduced pole, in conjunction with the very low frequency mechanical pole of the motor, strongly affects loop stability, system bandwidth and static speed regulation error: to preserve stability a DC loop gain ($G_{loop}(0)$) diminution may be needed. At the same time, decreasing the reference voltage ripple requires to reduce the frequency of the integrator pole, cutting the bandwidth and reducing the phase margin.

A full digital approach to convert the tacho frequency in a voltage can give further improvement in static and dynamic speed regulation: a microcontroller can measure the frequency of the tacho output and provide the reference voltage to the L6235 through a D/A converter or a low-pass filtered (see Reference Voltage section) PWM output (whose frequency can be much higher than the hall effect signals frequency, resulting in a strongly reduced Vref ripple).

Another possibility is using a PLL to generate a voltage proportional to the speed (or used directly, taking a frequency input as the command).

2.16 Brake

In general, motor braking can be achieved making a short circuit across the windings: the BEMF forces a current, proportional to the braking torque, that flows in the opposite direction than in normal running mode. For high BEMF and inertia moment the current may reach very high values: a power resistor is often used to reduce the maximum braking current and dissipate the motor energy.

L6235 Brake pin can be used to quickly stop the motor while it is running: providing a low logic level to this pin all the high-side DMOS switch on, making a short-circuit across the motor windings.

A power resistor is not used: while the motor is braking, both Thermal and Over Current protections still work, avoiding BEMF to cause a current exceeding the device's maximum ratings.

Connecting EN and DIAG pins together and using a RC network (see Over Current Detection section) a disable time between each over current event can be set, reducing the maximum r.m.s. value of the current.

Figure 34 and Figure 35 show what happens if the current exceeds the OCD threshold while the motor is braking: as soon as the current in one of the three motor phases reaches the OCD threshold (5.6 A typ.) the open drain mosfet internally connected to the DIAG pin discharges the external capacity; the EN pin voltage falls to GND and all the bridges of the device are disabled for a time that depends on the RC network values. During this disable time the current forced by the BEMF decreases, and so the braking torque; when the current becomes zero (because the motor inductances have been fully discharged), if the BEMF is less than the supply voltage there is no braking effect (since the freewheeling diodes cannot be turned on) until the disable time expires and all the high side PowerDMOS turn on again

Figure 34. Overcurrent during motor braking.

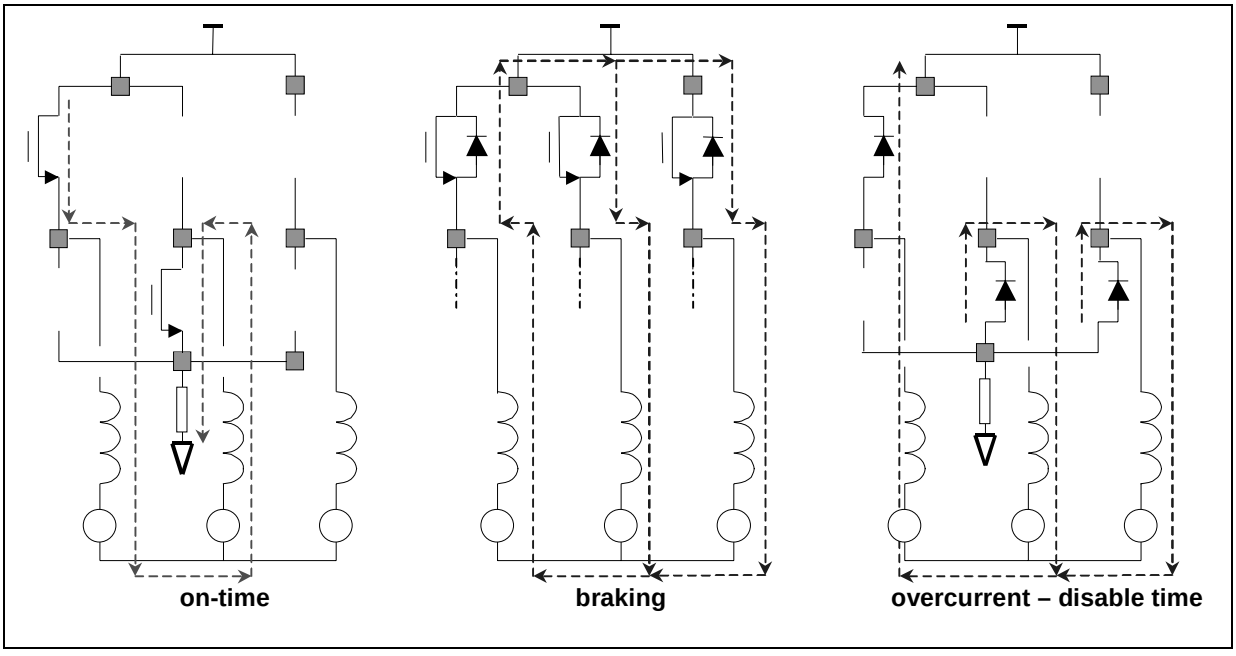
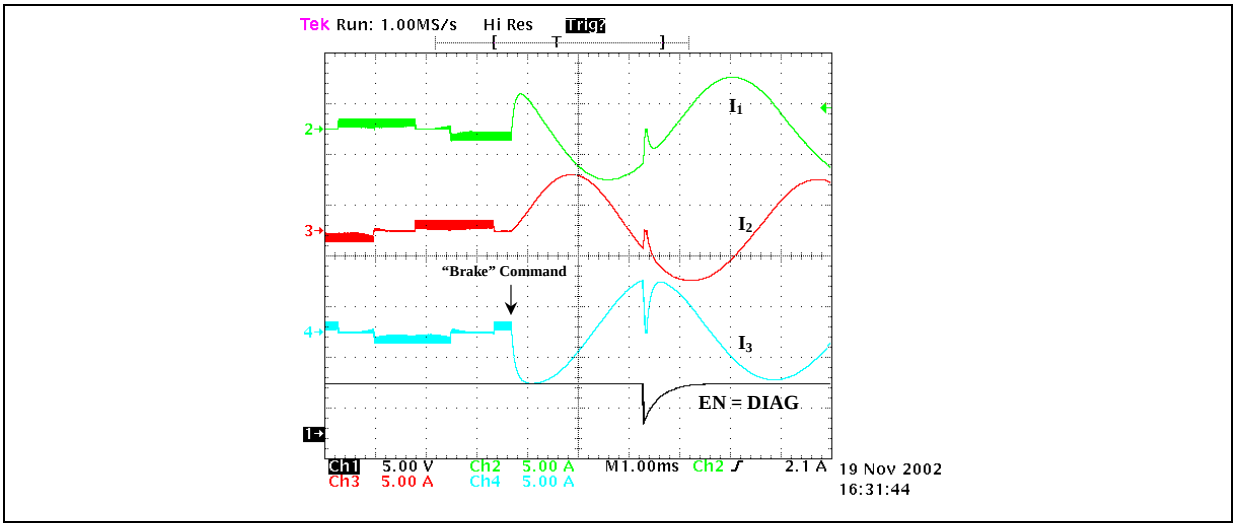


Figure 35. Overcurrent during motor braking.



3 APPLICATION EXAMPLE

Application Data

Rotation Speed:	10000 rpm (f_{EL}=167Hz)
Winding peak Current:	1.5 A
Maximum Ripple:	350mA
Maximum BEMF at 10000rpm:	10 V

Motor Data

Winding Resistance (2 phases): 2 Ω

Winding Inductance (2 phases): 800 µH

Supply Voltage: 24 V +/- 5%

Polar Couples: 1

Referring to approximated formulae in Figure 24, it's possible to calculate the Duty Cycle (D), the Switching Frequency (f_{SW}), the Current Ripple (ΔI). With a 8 µs off-time, we will have:

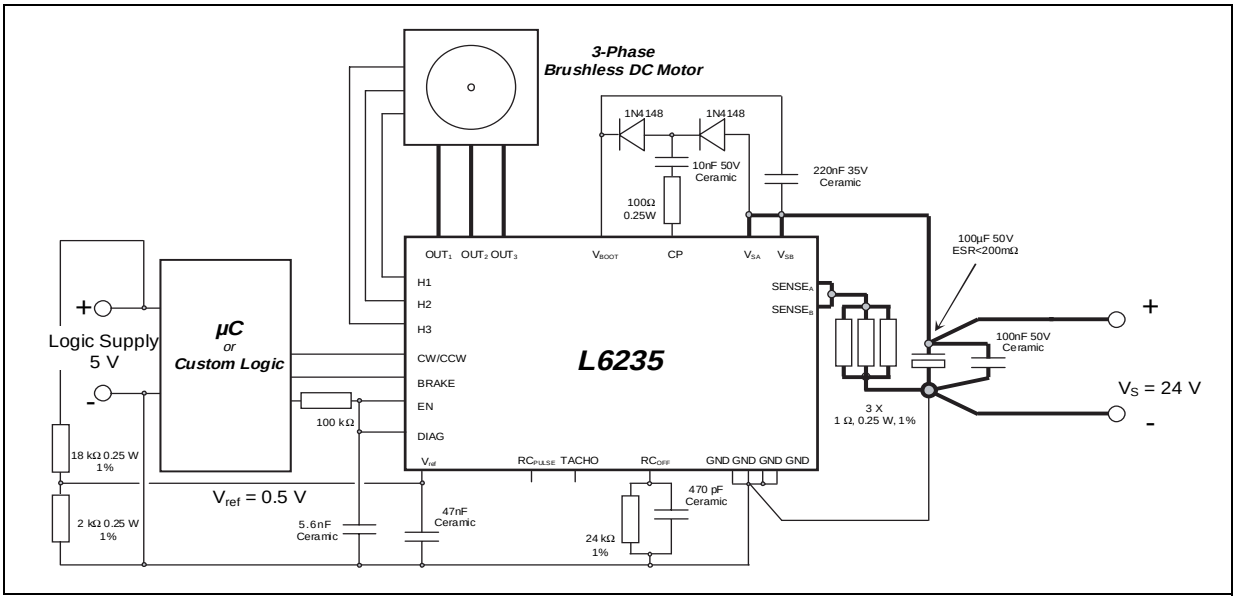
$$D \cong 61\%,\ f_{SW} \cong 49\ kHz,\ \Delta I \cong 320\ mA.$$

The on-time is $t_{ON} = D / f_{SW} \cong 12.5$ µs, which is far from the minimum allowed (1.5 µs).

The bulk capacitor needs to withstand at least 24 V + 5% + 25% ≅ 32 V. A 50 V capacitor will be used. Allowing a voltage ripple of 200 mV, the capacitor ESR should be lower than 200 mV / 1A = 200 mΩ; the AC current capability should be about 1.5 A (worst case).

Providing a reference voltage of 0.5 V, 0.33 Ω sensing resistor are needed. The resistors power rating is about $PR \cong Irms^2 \cdot R_{SENSE} \cdot D \cong 0.37$ W. Three 1 Ω / 0.25 W - 1% resistors in parallel are used. The charge pump uses recommended components (1N4148 diodes, ceramic capacitors and a 100 Ω resistor to reduce EMI).
R = 24 kΩ, C = 470 pF are connected to the RC pins, obtaining $t_{OFF} \cong 7.8$ µs. On the EN pin a 5.6 nF has been placed, and the pin is driven by the µC through a 100 kΩ resistor.
With these values, in case of short circuit between two OUT pins or an OUT pin and GND, the PowerDMOS turns off after about 1 µs, and $t_{DISABLE} \cong 240$ µs.

Figure 36. Application Example.



Referring to Figure 23, Figure 24, Figure 25, the dissipating power is about 2.37 W. If the ambient temperature is lower than 50 °C, with 5 cm^2 of copper area on the PCB, a ground layer and a PowerSO36 package, the estimated junction temperature is about 97 °C.

4 APPENDIX - EVALUATION BOARDS

4.1 PractiSPIN

PractiSPIN is an evaluation and demonstration system that can be used with the PowerSPIN family (L62XX) of devices. A Graphical User Interface (GUI) (see Figure 37) program runs on an IBM-PC under windows and communicates with a common ST7 based interface board (see Figure 38) through the RS232 serial port. The ST7 interface board connects to a device specific evaluation board (target board) via a standard 34 pin ribbon cable interface.

Depending on the target device the PractiSPIN can drive a stepper motor, 1 or 2 DC motors or a brushless DC (BLDC) motor, operating significant parameters such as SPEED, CURRENT, VOLTAGE, DIRECTION, ACCELERATION and DECELERATION RATES from a user friendly graphic interface, and programming a sequence of movements.

The software also allows evaluating the power dissipated by the selected device and, for a given package and dissipating copper area on the PCB, estimates the device's junction temperature.

Figure 37. PractiSPIN PC Software

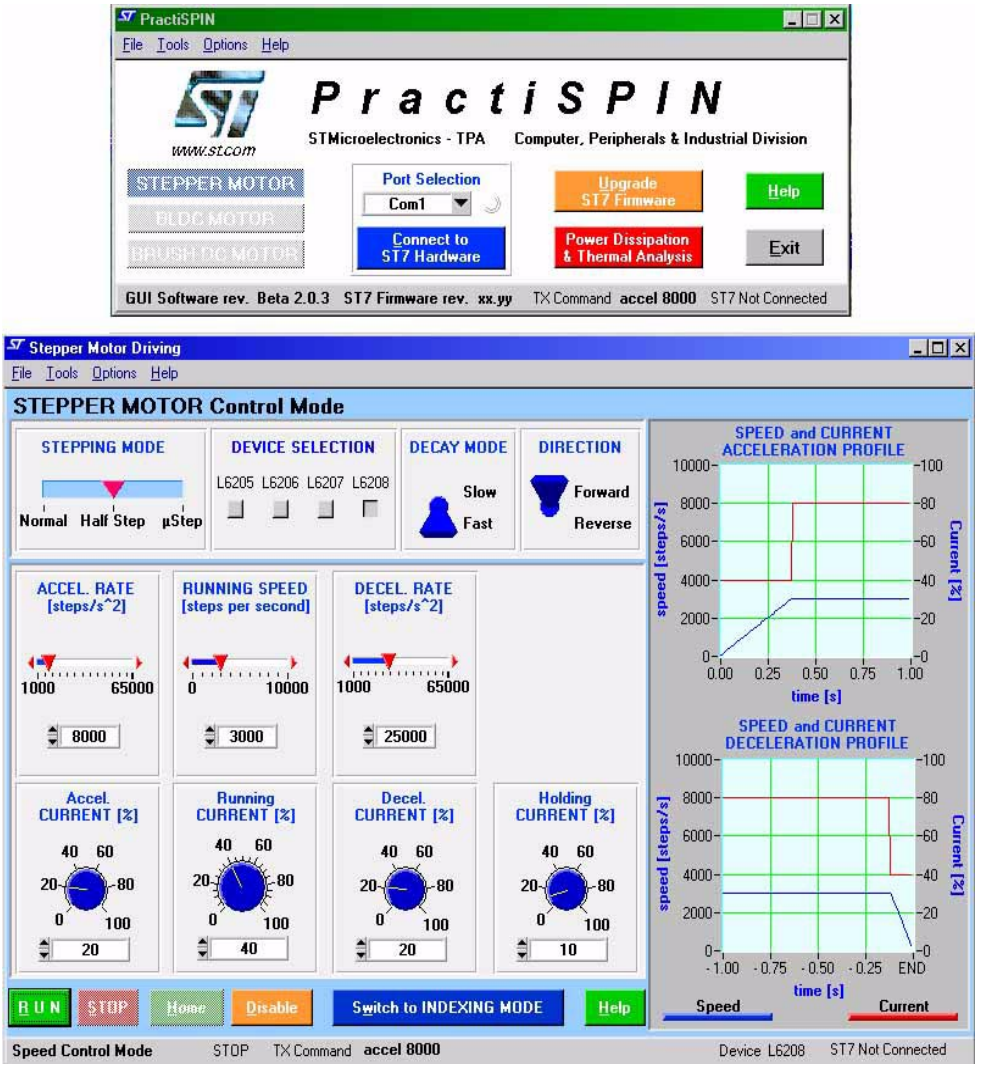
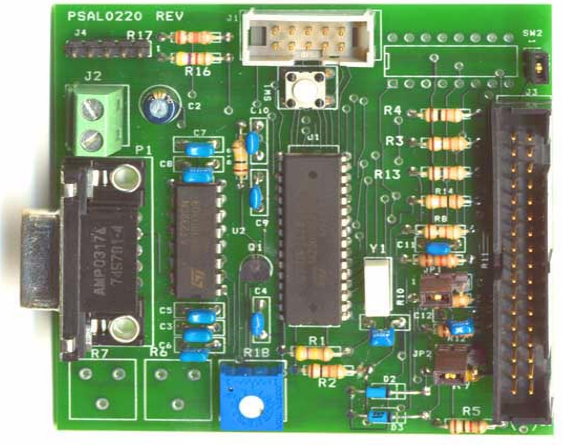


Figure 38. PractiSPIN ST7 Evaluation Board



4.2 EVAL6235N

An evaluation board has been produced to help the evaluation of the device in PowerDIP package. It implements a typical application with several added components. Figure 40 shows the electrical schematic of the board; in the table below the part list is reported.

CN1, CN2	2-poles connector	JP1, JP2	2-pin jumper
CN3	3-poles connector	R1	700Ω 0.6W resistor
CN4	34-poles connector	R2,R3,R4,R7,R8,R9	10kΩ resistor
C1	220nF/100V Ceramic or Polyester capacitor	R5	100Ω resistor
C2	220nF/100V Ceramic or Polyester capacitor	R15,R6	1kΩ resistor
C3	100µF/63V capacitor	R11,R10	100kΩ trimmer
C4	10nF/100V Ceramic capacitor	R12,R13,R14	1Ω 1% resistor
C5	10µF/16V Capacitor	R16	1MΩ resistor
C6	33nF Capacitor	R17	20kΩ resistor
C7	1nF Capacitor	R18	4.7kΩ resistor
C8	820pF Capacitor	R19	5.6kΩ resistor
C9	10nF Capacitor	R20	2.2kΩ resistor
C10	220nF Capacitor	R21	1.8kΩ resistor
C11	68nF Capacitor	R22	5kΩ trimmer
C12	100nF Capacitor	S1	quad switch
D1, D2	1N4148 Diode	U1	L6235N
D3	BZX79C5V1 5.1V Zener Diode	U2	LM358

The Evaluation Board provides external connectors for the supply voltage, an external 5 V reference for the logic inputs, three outputs for the motor and a 34-pin connector to control the main functions of the board through an external µC board.

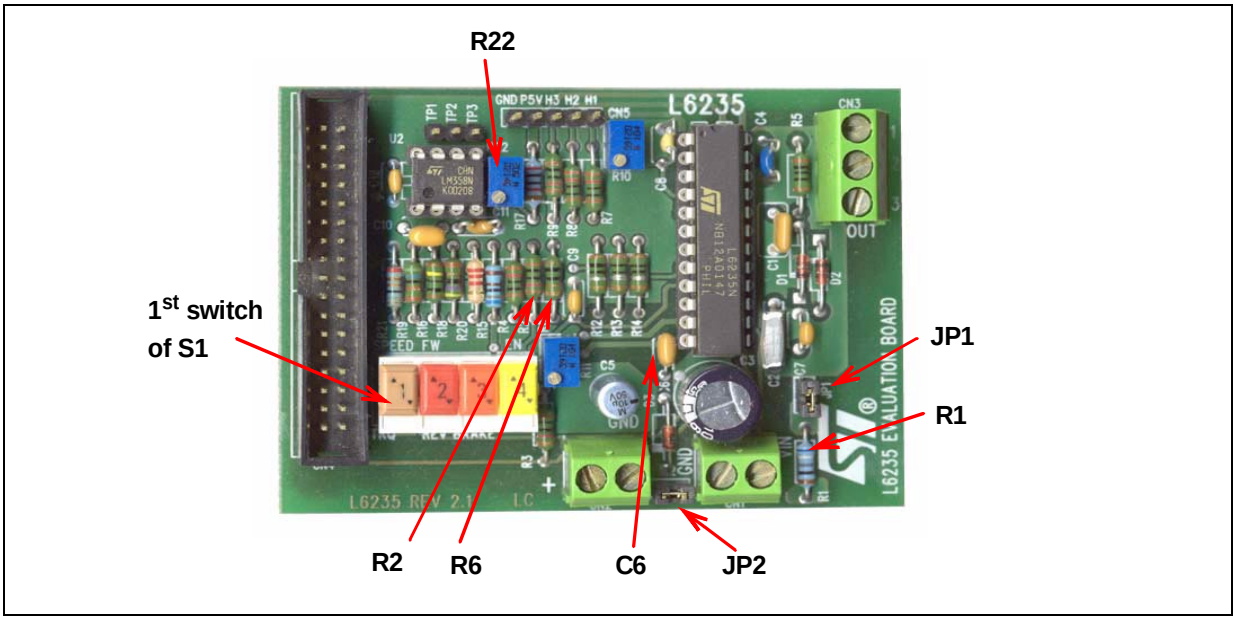
Running the evaluation board in stand-alone mode, instead, four switches (S1) allow enabling the device, setting the direction of the rotation, braking the motor, choosing to run in torque or speed mode. R17 and R22 set

the reference voltage provided to the Vref pin of the L6235 (in torque mode) or to the error amplifier, U2 (in speed mode); R20, C11 make up a low-pass filters to provide an external reference voltage by a PWM output of a µC (see also the Reference Voltage section). R10, C8 are used to set the off-time and R11, C9 set the duration of the TACHO output pulses.

The 5V voltage for logic inputs and for the reference voltage is obtained from R1, D3. For supply voltages greater than 20V, R1 must be replaced with a higher value resistor. The jumper JP1 and JP2 allow disconnecting the internal zener diode network, in case the 5V voltage is provided through pin 11 of CN5 (for example an external µC board can provide 5 V to the evaluation board). Also CN2 connector can be used to provide an external 5 V voltage to the board. CN2, or pin 1 of CN5, can also be used to provide a 5 V voltage to external circuits. In this case only a small current can be drawn form the board, depending on the supply voltage and R1 value. Figure 41, Figure 42, Figure 43 show the component placement and the two layers layout of the L6235N Evaluation Board.

A large GND area has been used, to guarantee minimal noise and good power dissipation for the device.

Figure 39. EVAL6235N.



4.2.1 Important Notes

JP1 : close for use with PractiSPIN ST7 board

JP2 : close for use with PractiSPIN ST7 board

C6 : recommended change to 5.6 nF for safe Overcurrent protection

R2 : recommended change to 100 k for safe Overcurrent protection

R6 : recommended change to 100 k (and remove R2) if EN pin is driven from the CN4 connector (for example with PractiSPIN ST7 board) for safe Overcurrent protection

R22 : set the maximum current obtainable through PractiSPIN (see PractiSPIN documentation)

R1 : recommended change to adequate value (depending on supply voltage) to obtain 5V across D3

S1 : move first switch in TRQ position for use with PractiSPIN ST7 board

Figure 40. L6235N Evaluation Board Electrical schematic.

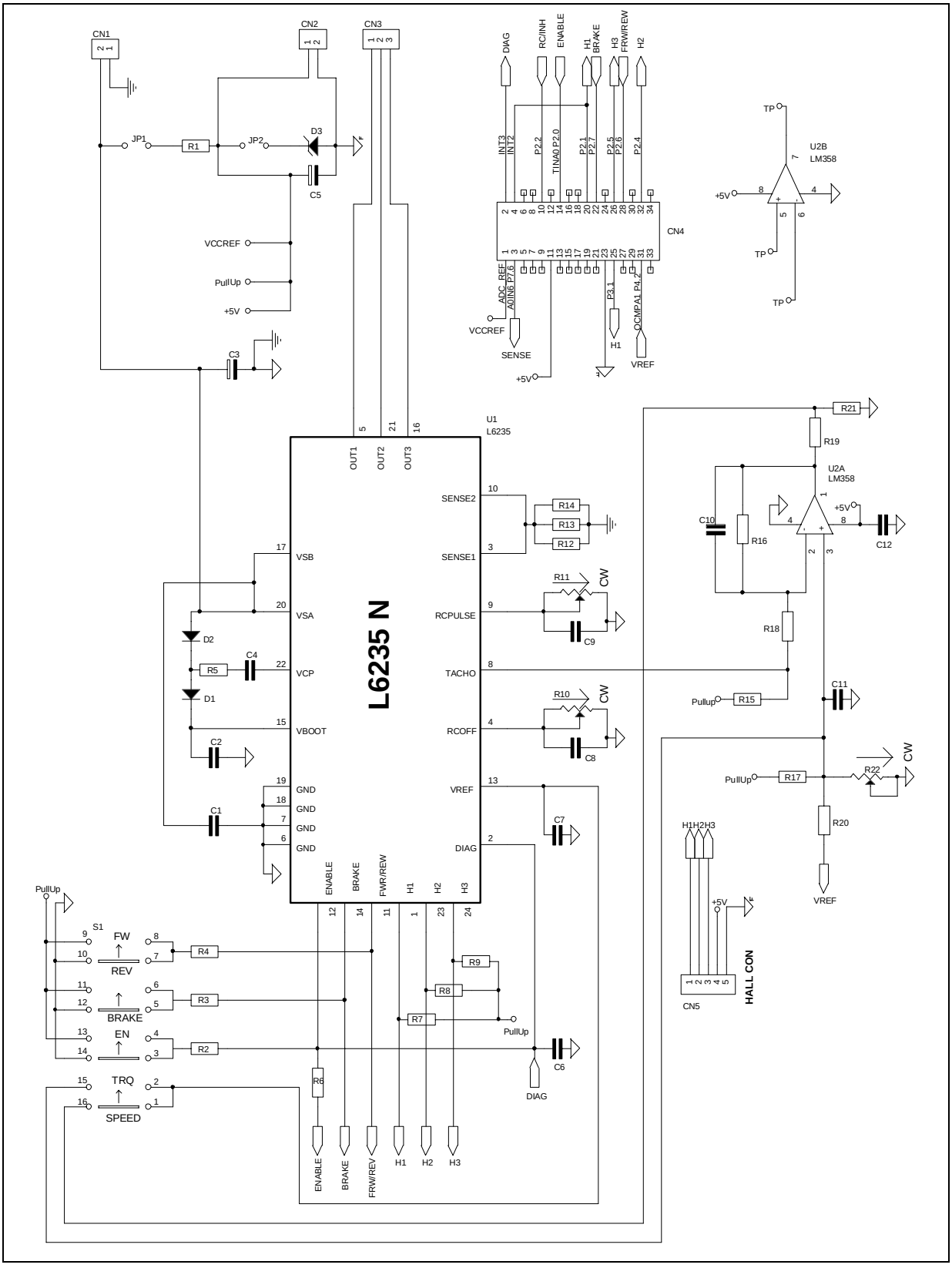


Figure 41. L6235 Evaluation Board Component placement.

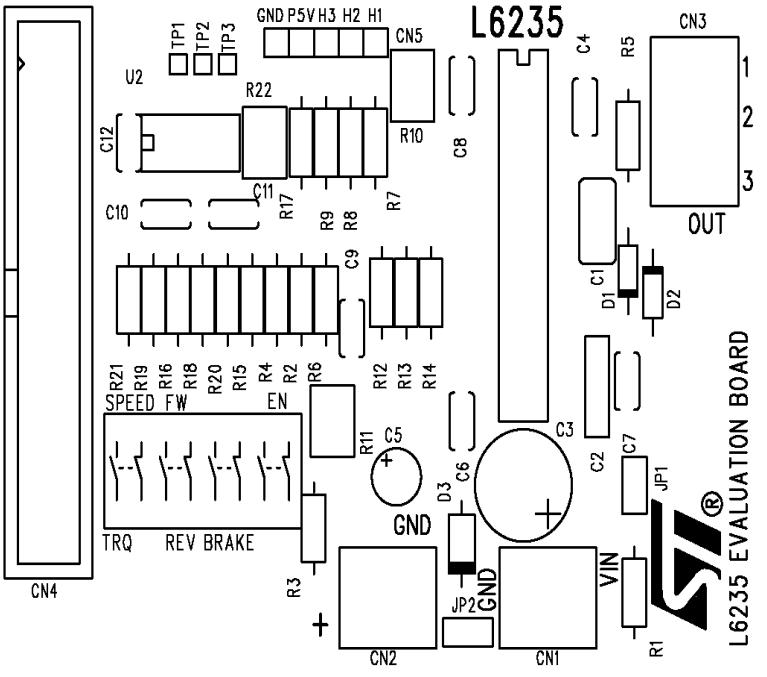


Figure 42. L6235 Evaluation Board Top Layer Layout.

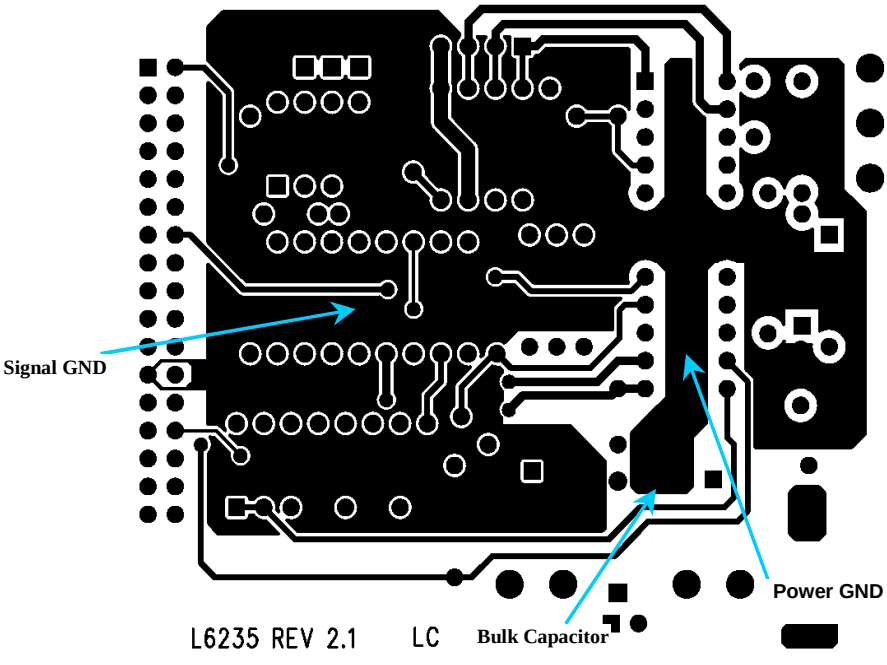
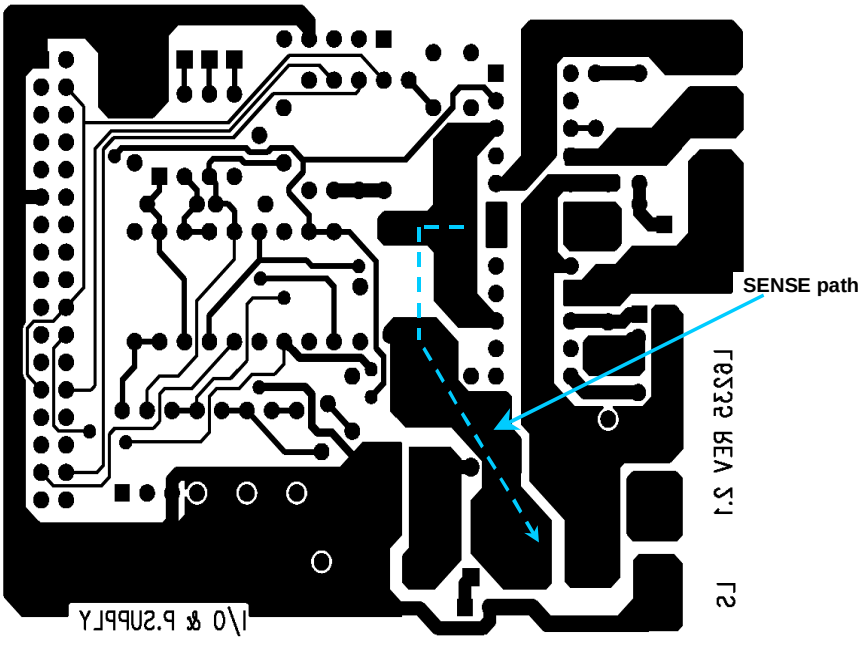


Figure 43. L6235 Evaluation Board Bottom Layer Layout.



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