UX481FL Series SCHEMATIC Revision 2.0

Connected Standby

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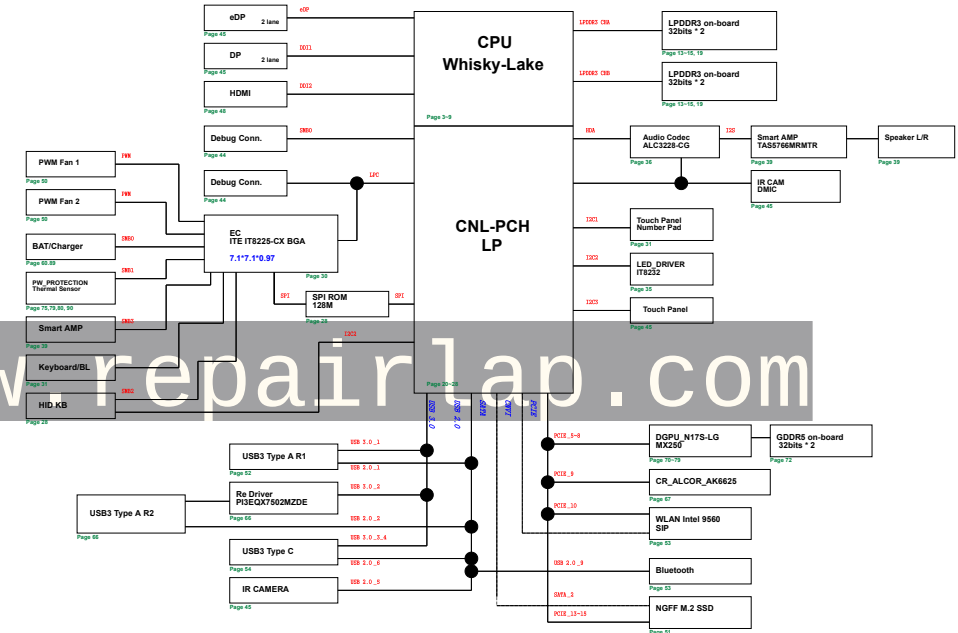


PCH_GPIO

PCH_3REX GPIO	Use As	Signal Name	Power on Default States	In/Out Pull up / down	Power
GPP_A0	NativeL	RC_INT		EXT PU 10K	+3VS
GPP_A1	NativeL	LPC_AD0			+3VS
GPP_A2	NativeL	LPC_AD1			+3VS
GPP_A3	NativeL	LPC_AD2			+3VS
GPP_A4	NativeL	LPC_AD3			+3VS
GPP_A5	NativeL	LPC_FRAMEB			+3VS
GPP_A6	NativeL	INT_SERIRQ		EXT PU 10K	+3VS
GPP_A7	NativeL	PIRQAB		EXT PU 10K	+3VS
GPP_A8	NativeL	PM_CLKRUNB		EXT PU 3.2K	+3VS
GPP_A9	NativeL	CLK_48CPCI_PCH			
GPP_A10	NativeL	CLK_3REGI			
GPP_A11	GPO				
GPP_A12	GPO				
GPP_A13	NativeL	M6_BiosProtect_N		EXT PU 10K	+3VDUS
GPP_A14	NativeL	SUS_STATB			
GPP_A15	NativeL	SUSACK_NB			
GPP_A16	GPO				
GPP_A17	GPO				
GPP_A18	GPO				
GPP_A19	GPO				
GPP_A20	GPO				
GPP_A21	GPO				
GPP_A22	GPO				
GPP_A23	GPO				
GPP_B0	GPO				
GPP_B1	GPO				
GPP_B2	GPO				
GPP_B3	GPO				
GPP_B4	GPO				
GPP_B5	NativeL	CLK_REQ_C6B		EXT PU 10K	+3VS
GPP_B6	NativeL	CLK_REQ_SSDB		EXT PU 10K	+3VS
GPP_B7	NativeL	CLK_REQ_WLANB		EXT PU 10K	+3VS
GPP_B8	GPO				
GPP_B9	GPO				
GPP_B10	NativeL	CLK_REQ_VGAB		EXT PU 10K	+3VS
GPP_B11	GPO	PCPAT_PERSTB		EXT PU 8.2K	+3VSUS
GPP_B12	NativeL	PCH_SLP_SUSB		EXT PU 8.2K	+3VSUS
GPP_B13	NativeL	PLT_RSTB			
GPP_B14	GPO				
GPP_B15	GPO				
GPP_B16	GPO				
GPP_B17	GPO	CASC_EN			
GPP_B18	GPI	TPADAL_INTF_2ND		EXT PU 10K	+3VS
GPP_B19	GPO	AT_GA_PCH			
GPP_B20	GPO	LPC_SUSSTB		EXT PU 10K	+3VS
GPP_B21	GPO	SCX_EN_EN 2.3			
GPP_B22	GPO				
GPP_B23	NativeL	SMLIALERTB		EXT PU 10K	+3VS
GPP_C0	NativeL	SMB_CK		EXT PU 2.2K	+3VSUS
GPP_C1	NativeL	SMB_DATA		EXT PU 2.2K	+3VSUS
GPP_C2	GPO				
GPP_C3	NativeL	SMLI_CK (NC)		EXT PU 2.2K	+3VSUS
GPP_C4	NativeL	SMLI_DATA (NC)		EXT PU 2.2K	+3VSUS
GPP_C5	GPO	GPP_C5	EXT PU 01/PD 510K		+3VA_S5M
GPP_C6	NativeL	SMLI_CK (NC)		EXT PU 2.2K	+3VSUS
GPP_C7	NativeL	SMLI_DATA (NC)		EXT PU 2.2K	+3VSUS
GPP_C8	GPO				
GPP_C9	GPO				
GPP_C10	GPO				
GPP_C11	GPO				
GPP_C12	GPI	DIMM_SELO		EXT PU/PD 10K	+3VSUS
GPP_C13	GPI	DIMM_SEL1		EXT PU/PD 10K	+3VSUS
GPP_C14	GPI	DIMM_SEL2		EXT PU/PD 10K	+3VSUS
GPP_C15	GPO				
GPP_C16	GPO				
GPP_C17	GPO				
GPP_C18	NativeL	I2C1_SDA_TCH_PAD		EXT PU 4.7K	+3VS
GPP_C19	NativeL	I2C1_SCL_TCH_PAD		EXT PU 4.7K	+3VS
GPP_C20	GPI	SSPI_FWSCK			
GPP_C21	GPO	SSPI_RSTB		EXT PU 10K	
GPP_C22	GPO	SSPI_PWR_EN#		EXT PU 8104	+3VSUS
GPP_C23	GPO				
GPP_D0	GPO				
GPP_D1	GPO				
GPP_D2	GPO				
GPP_D3	GPO				
GPP_D4	GPO				
GPP_D5	GPO				
GPP_D6	GPO				
GPP_D7	GPO				
GPP_D8	GPO				
GPP_D9	GPO	PCH_I2C	EXT 01/08K/PU 10K		+3VS
GPP_D10	GPI	PCH_I2C	EXT 01/08K/PU 10K		+3VS
GPP_D11	GPO				
GPP_D12	GPO	SPI1_MOSI		EXT PU 10K	+3VSUS
GPP_D13	GPI	TOUCHPAD_INTRB		EXT PU 10K	+3VS
GPP_D14	GPO	HID_KB_INTB		EXT PU 8104	+3VS
GPP_D15	GPO				
GPP_D16	GPO				
GPP_D17	NativeL	SMI2_CLK1_PCH_R			
GPP_D18	NativeL	SMI2_DATA1_PCH_R			
GPP_D19	NativeL	SMI2_CLK_PCH_R1			
GPP_A20	NativeL	SMI2_DATA_PCH			
GPP_D21	GPO				
GPP_D22	GPO				
GPP_A23	GPO				

PCH_3REX GPIO	Use As	Signal Name	Power on Default States	In/Out Pull up / down	Power
GPP_E0	GPO	SATAGP0			
GPP_E1	GPO				
GPP_E2	NativeL	SATA3X_SPCIE_DET#		EXT PU 8104	+3VSUS
GPP_E3	GPO				
GPP_E4	GPO				
GPP_E5	GPO				
GPP_E6	NATIVE	SATA2 DEVSLP			
GPP_E7	GPO				
GPP_E8	GPO				
GPP_E9	NATIVE	USB_OC_1_2#		EXT PU 2.2K	+3VSUS
GPP_E10	NATIVE	USB_OC_3_4#		EXT PU 2.2K	+3VSUS
GPP_E11	NATIVE	USB_OC_5_6#		EXT PU 2.2K	+3VSUS
GPP_E12	NATIVE	USB_OC_7_8#		EXT PU 2.2K	+3VSUS
GPP_E13	NATIVE	DP_HPD_PCH	EXT PU 01/PD 100K		+3VS
GPP_E14	NATIVE	EDP_BKLTEN	EXT PU 10K	EXT PU 10K	+3VS
GPP_E15	GPI	EXT_SMIB	EXT PU 10K		+3VS
GPP_E16	GPI	EXT_SCIB	EXT PU 10K		+3VS
GPP_E17	NATIVE	EDP_BKL_PCH	EXT PU 100K		
GPP_E18	NATIVE	EDPB_SCL_PCH	EXT PU 2.2K		+3VS
GPP_E19	NATIVE	EDPB_SDA_PCH	EXT PU 2.2K		+3VS
GPP_E20	NATIVE	DDPC_HCL_PCH	EXT PU 2.2K		+3VS
GPP_E21	NATIVE	DDPC_HDA_PCH	EXT PU 2.2K		+3VS
GPP_E22	GPO				
GPP_E23	GPO				
GPP_F0	GPO				
GPP_F1	GPO				
GPP_F2	GPO				
GPP_F3	GPO				
GPP_F4	NATIVE	CNV_BRI_DT		EXT PU 8104	+1.8VSUS
GPP_F5	NATIVE	CNV_BRI_RST		EXT PU 8204	+1.8VSUS
GPP_F6	NATIVE	CNV_RGI_DT		EXT PU 204	+1.8VSUS
GPP_F7	NATIVE	CNV_RGI_RST		EXT PU 8204	+1.8VSUS
GPP_F8	GPO				
GPP_F9	GPO				
GPP_F10	GPO				
GPP_F11	GPO				
GPP_F12	GPO				
GPP_F13	GPO				
GPP_F14	GPO				
GPP_F15	GPO				
GPP_F16	GPO				
GPP_F17	GPO				
GPP_F18	GPO				
GPP_F19	GPO				
GPP_F20	GPO				
GPP_F21	GPO				
GPP_F22	GPO				
GPP_F23	NATIVE	XTPP_PRESENT	EXT PU 10K	EXT PU 75K	
GPP_G0	GPO				
GPP_G1	GPO				
GPP_G2	GPO				
GPP_G3	GPO				
GPP_G4	GPO				
GPP_G5	GPO				
GPP_G6	GPO				
GPP_G7	GPO				
GPP_H0	GPO				
GPP_H1	GPO				
GPP_H2	GPO				
GPP_H3	GPO				
GPP_H4	GPO				
GPP_H5	GPO				
GPP_H6	GPO				
GPP_H7	GPO				
GPP_H8	GPO				
GPP_H9	GPO				
GPP_H10	GPO				
GPP_H11	GPO				
GPP_H12	GPO				
GPP_H13	GPO				
GPP_H14	GPO				
GPP_H15	GPO				
GPP_H16	GPO				
GPP_H17	GPO				
GPP_H18	GPO				
GPP_H19	GPO				
GPP_H20	GPO				
GPP_H21	NativeL	SSPI_M21		EXT PU 4.7K	+3VSUS
GPP_H22	GPO				
GPP_H23	GPO	SSPI_M23	EXT PU 84.7K/PD 84.7K		+3VA_S5M

EC IT8225 GPIO

*1: EC config SPI: Function output

Pin Name	Config	Signal Name	Default	OD	Ext Pull up / down	Power
GPA0	O	PWR_LED	LOW	PP	2K2 ~2K7 PU +3S	
GPA1	O	CAPS_LED#	HIGH	OD		
GPA2	O	CAPS_PULL_LED#	HIGH	OD		
GPA3	A15	FAN2_PWM	LOW	PP		
GPA4	I	N/A	LOW	PP		
GPA5	A15	FAN1_PWM	LOW	PP		
GPA6	A15	KB_LED_PWM	LOW	PP		
GPA7	A15	I2F_PWM	LOW	PP	40K ~50K PU +3S	
GPB0	A15	AC_IN_OCB	LOW	PP	4K7 100K PU +3S	+3S
GPB1	I	LID_SWB	LOW	PP	4K7 100K PU	+3S
GPB2	O	SP_AL_EN	LOW	PP	40K ~50K PU +3S	
GPB3	A15	PWR_SWF	LOW	PP	4K7 100K PU	+3S
GPB4	I	PS_ON_EC	HIGH	PP		
GPB5	I	N/A	LOW	PP		
GPB6	O	EC_ISH	LOW	OD	4K7 10K PU	+3S
GPC0	O	TP_disablef	LOW	PP		
GPC1	A15	SMB1_CLK	LOW	OD	4K7 4.7K PU	+3A_S5
GPC2	A15	SMB1_DAT	LOW	OD	4K7 4.7K PU	+3A_S5
GPC3	I	PM_PWRBTNB	LOW	PP	4K7 100K PU	
GPC4	I	PM_SLP_S4#B	LOW	PP	4K7 100K PU	
GPC5	I	PM_SLP_S3B	LOW	PP	4K7 100K PU	
GPC6	A15	SMB_CK_OCB	LOW	OD	4K7 10K PU	
GPC7	A15	SMB2_CLK	LOW	PP	4K7 4.7K PU (S3/S4/S5)	+3A_S5
GPD0	I	CPU_CIO_GATE#	LOW	PP		
GPD1	O	MB_EC_PRESENT	LOW	PP	4K7 100K PU	+3A_S5M
GPD2	A15	BKP_PLT_RST#	LOW	PP	4K7 100K PU	
GPD3	O	EXT_SCI#	LOW	OD	4K7 10K PU	+3VS
GPD4	O	EXT_SMI#	LOW	OD	4K7 10K PU	+3VS
GPD5	O	LP_SLP#	LOW	PP	4K7 100K PU	+3VS
GPD6	A15	FAN2_TACH	LOW	PP	4K7 10K PU	+3VS
GPD7	A15	FAN1_TACH	LOW	PP	4K7 10K PU	+3VS
GPE0	O	SIO2C_ECS	LOW	PP	4K7 10K PU	
GPE1	O	SIO2C_ECK	LOW	PP	4K7 10K PU	
GPE2	O	I_SCI_OB	LOW	PP	40K ~50K PU +3S	+3A_S5
GPE3	O	SVIDD_CB	LOW	PP	40K ~50K PU +3S	+3A_S5
GPE4	O	VSSD_CB	LOW	PP	4K7 100K PU	+3A_S5
GPE5	O	SVIDDM_CB	LOW	PP	4K7 100K PU	+3A_S5
GPE6	O	N/A	LOW	PP		
GPE7	O	TPAD_CP1#	HIGH	OD	4K7 10 PU	+3VSUS
GPF0	O	CAP_LED#	HIGH	OD	4K7 100K PU	
GPF1	I	N/A	LOW	PP		
GPF2	A15	P_SMB2_CLK	LOW	OD	4K7 4.7K PU	+3A_S5
GPF3	A15	P_SMB2_DAT	LOW	OD	4K7 4.7K PU	+3A_S5
GPF4	I	DP_HPD#	LOW	PP		
GPF5	O	PM_LED#	HIGH	OD	4K7 10K PU	+3VS
GPF6	A15	TPAD_BI	LOW	PP	4K7 10K PU (S3/S4/S5)	+3A_S5
GPF7	A15	TPAD_CLK	LOW	PP	4K7 10K PU (S3/S4/S5)	+3A_S5
GPG0	I	N/A	LOW	PP	4K7 100K PU	+3A_S5
GPG1	I	N/A	LOW	PP	4K7 100K PU	+3A_S5
GPG2	A15	SMB3_CLK	LOW	PP	4K7 4.7K PU	+3A_S5
GPG3	A15	SMB3_DAT	LOW	PP	4K7 4.7K PU	+3A_S5
GPG4	O	PM_RSMRST#	LOW	PP	4K7 10K PU	
GPG5	O	SPIROM_EC	LOW	PP	4K7 10K PU	
GPG6	O	PM_PWROK	LOW	PP	4K7 100K PU	
GPG7	O	PM_SYSPWROK	LOW	PP	4K7 PU 10K	
GPH0	O	LCD_BACKOFF#	LOW	PP	4K7 100K PU	
GPH1	I	PM_SLP_S03#	LOW	PP	4K7 100K PU	
GPH2	I	SVIDD_PWRGD	LOW	PP	4K7 100K PU	+3VSUS
GPH3	I	ALL_SYSTEM_PWRGD	LOW	PP	4K7 10K PU	+3VS
GPH4	I	SVDDV_PWRGD	LOW	PP	4K7 100K PU	+3VS
GPH5	I	3VA_S5M_PWRGD	LOW	PP	4K7 100K PU	+3A_S5M
GPH6	I	N/A	LOW	PP		
GPH7	A15	A/D_MAX_POWER	LOW	PP	4K7 100K PU	+3VALW
GPI7	A15	MB_MAX_POWER	LOW	PP	4K7 100K PU/PD 1M PU	+3VALW
GPJ0	O	SSPI_RSTB_EC	LOW	PP	4K7 100K PU	
GPJ1	I	SCX_EN_EN 2.3	LOW	PP		
GPJ2	O	PCH_SPI_OV	HIGH	PP		
GPJ3	O	LED_RST	LOW	PP	4K7 100K PU	+3VS
GPJ4	O	SSPI_PWR_EN# EC	HIGH	PP	4K7 10K PU	+3VSUS
GPJ5	O	N/A	HIGH	OD	4K7 10K PU (S3/S4/S5)	+3VS
GPJ6	I	1P VDD_EN	LOW	PP		
GPJ7	O	CAP2 EN	HIGH	PP		

SMB Address

EC Master	
EC Master (SMB0)	**SM-Bus Address**
Charger (IL 1) 3/5/2857	12h
Charge IL 1) 8/2857	09h
EC Master (SMB1)	**SM-Bus Address**
9V30VA	80h
NUVOTON ec3712	98h
GPU(82) (1st/2nd)	7Eh 7Fh
EC Master (SMB2)	**SM-Bus Address**
M1	98h 9Ch
M2(last thing 1K5/1.5Q)M	98h 9Ch

PCH Master	
PCH Master (SMB0)	**SM-Bus Address**
PCH Master (SMB1)	**SM-Bus Address**

PCI Express

PCIE 6	GSPU	
PCIE 7		
PCIE 8		
PCIE 9	Card Reader	
PCIE 10	WLAN	
PCIE 11		
PCIE 12		
PCIE 13	SSD x4	
PCIE 14		

SATA Port

SATA 0	
SATA 1	
SATA 2	SSD
SATA 3	

USB 3.0

USB 1	USB 3.0 Type A (MB)
USB 2	USB 3.0 Type A (MB)
USB 3	USB 3.0 Type C (MB)
USB 4	

USB 2.0

USB 1	Camera
USB 2	
USB 6	USB 3.0 Type C (MB)
USB 7	
USB 8	
USB 9	BT
USB 10	

Device Identification

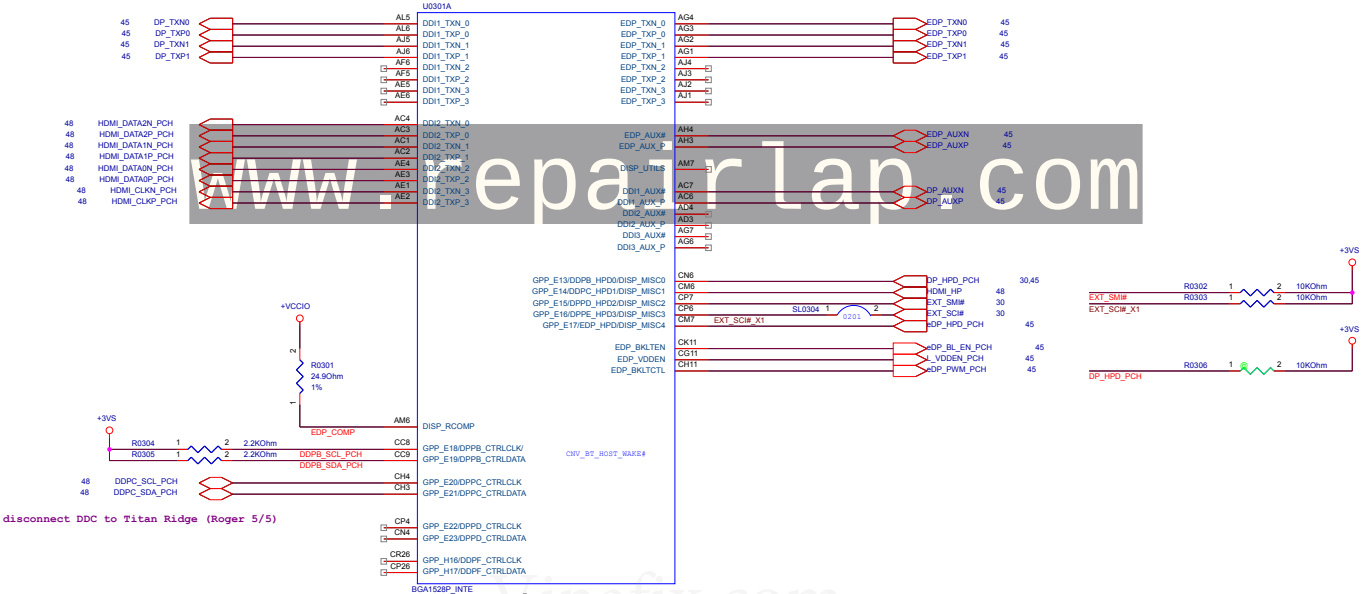
CPU Thermal Sensor			
Ref			
2nd			
Memory Thermal Sensor			
Ref	30021-00100000		0x1777Fh
2nd			

Display Port

A	EDP, First Panel
B	DP, Second Panel
C	HDMI

Intel Version	ASUS P/N
ES-0	01001-01540000

	HDMI
DDI_0	Lane2
DDI_1	Lane1
DDI_2	Lane0
DDI_3	CLK



disconnect DDC to Titan Ridge (Roger 5/5)

PDG#543016 DDI1 mapping DDPB
DDI2 mapping DDPC

LPDDR3 Non-Interleaved

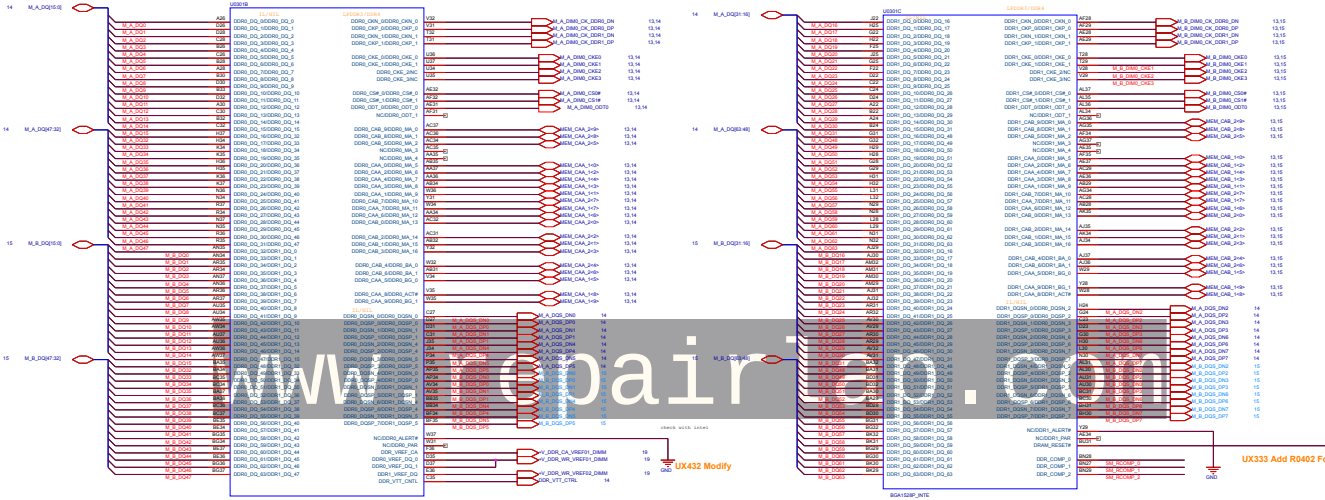
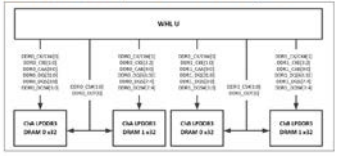
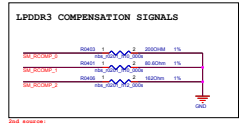
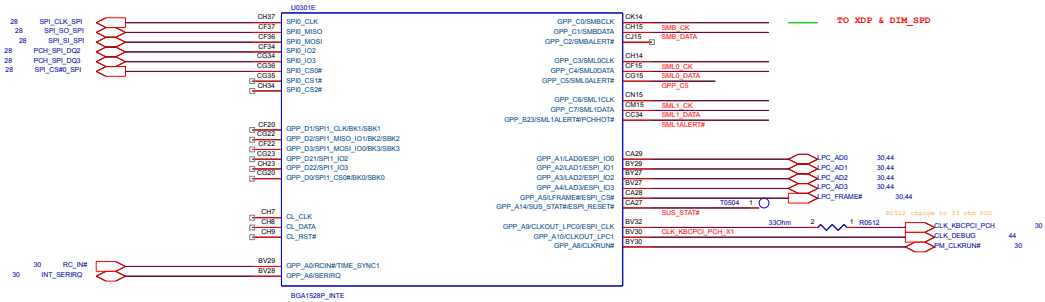


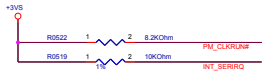
Figure 2-2. WHL U LPDDR3 x32 Memory Down Placement and Block Diagram



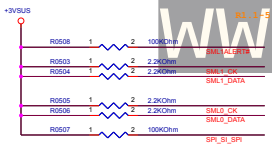
RCOMP[0]	M	SI_MS	VSS	5	12-15			20	25	500	500	200
RCOMP[1]	M	SI_MS	VSS	5	12-15			20	25	500	500	80.6
RCOMP[2]	M	SI_MS	VSS	5	12-15			20	25	500	500	162

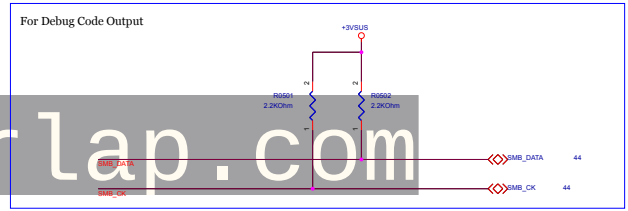




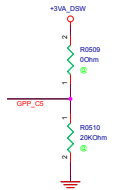


UX305UA CRB 1.1 P.20 150K PU ok 0318 change to 100K 0324





UX391RA add



GPP_C5: weak internal pull down	
PU	ESPI BUS
PD	LPC is selected for EC (Default)

Transport Layer Security (TLS) Confidentiality

UX305UA remove 0429

GPP_C2: weak internal pull down	
PU	Enable
PD	Disable Intel ME TLS ipher suite (no confodentiality)(Default)

TP for Boundary Scan Test

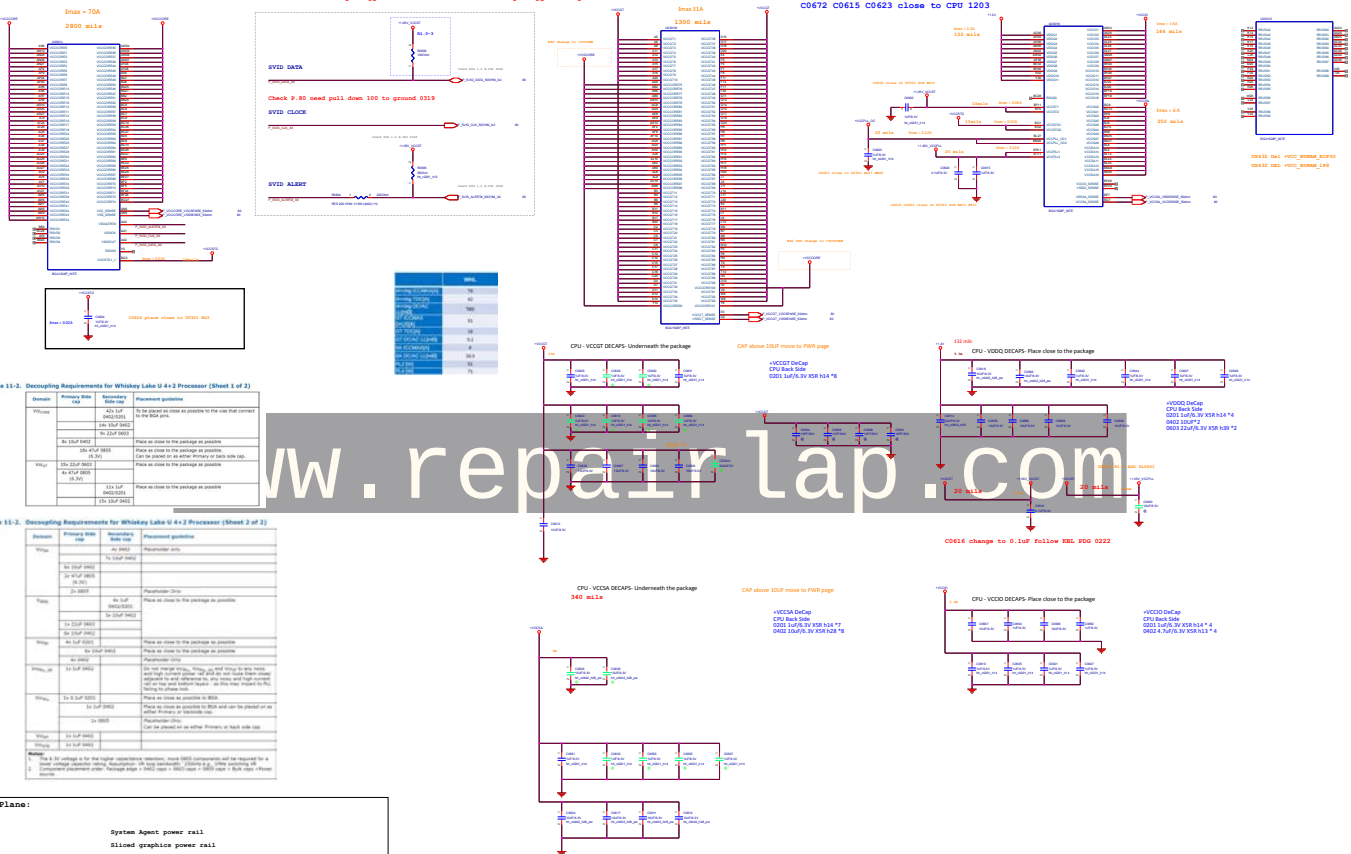


Table 11-2. Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 1 of 2)

Domain	Primary Side Cap	Secondary Side cap	Placement guideline
$V_{CC_{CORE}}$	42x 1uF 0402/0201		To be placed as close as possible to the vias that connect to the BGA pins.
		14x 10uF 0402	
		9x 22uF 0603	
	8x 47uF 0805		Place as close to the package as possible
	10x 47uF 0805 (6.3V)		Place as close to the package as possible. Can be placed on as either Primary or back side cap.
V_{NN}	15x 22uF 0603		Place as close to the package as possible
	4x 47uF 0805 (6.3V)		
		11x 1uF 0402/0201	Place as close to the package as possible
		15x 10uF 0402	

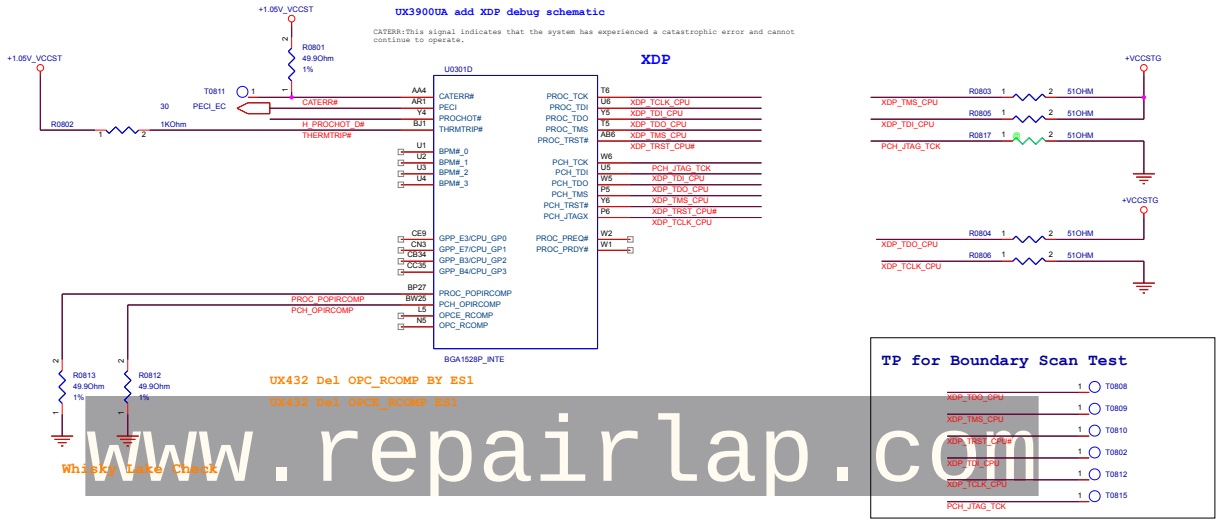
Table 11-2. Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 2 of 2)

Domain	Primary Side cap	Secondary Side cap	Placement guideline
V_{CCSA}	4x 0402	Placeholder only	
		7x 10uF 0402	
	8x 10uF 0402		
	2x 47uF 0805 (6.3V)		
	2x 0805	Placeholder Only	
V_{CCIO}		4x 1uF 0402/0201	Place as close to the package as possible.
		3x 10uF 0402	
	1x 22uF 0603		
	6x 10uF 0402		
V_{CCSTG}	4x 1uF 0201		Place as close as possible to the package as possible
		5x 10uF 0402	Place as close to the package as possible
	4x 0402	Placeholder Only	
V_{CCPLL_OC}	1x 1uF 0402		Do not merge V_{CCPLL_OC} and V_{CCSA} to any rails. Isolate V_{CCPLL_OC} from V_{CCSA} by 0 ohm resistor placed adjacent to and reference to, any noisy and high current rail on top and bottom layers - as this may impact to R_{ON} failing to phase lock.
V_{CCPLL}	1x 1uF 0201		Place as close as possible to BGA.
		1x 10uF 0402	Place as close as possible to BGA and can be placed on as either Primary or backside cap.
		1x 0805	Placeholder Only. Can be placed on as either Primary or back side cap.
V_{CCSFR}	1x 1uF 0402		
V_{CCAPLL}	1x 1uF 0402		

Notes:
1. The 6.3V voltage is for the higher capacitance selection, more 0805 components will be required for a lower voltage capacitor rating. Assumption: VR loop bandwidth: 250kHz e.g., CPM switching fq = 1MHz, inductor placement order: Package edge > 0402 caps > 0603 caps > 0805 caps > Bulk caps > Power source.

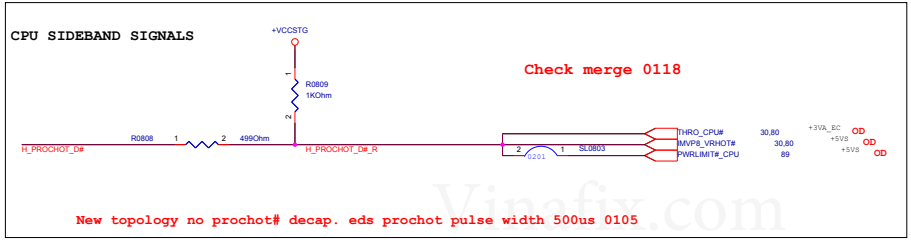
Power Plane:

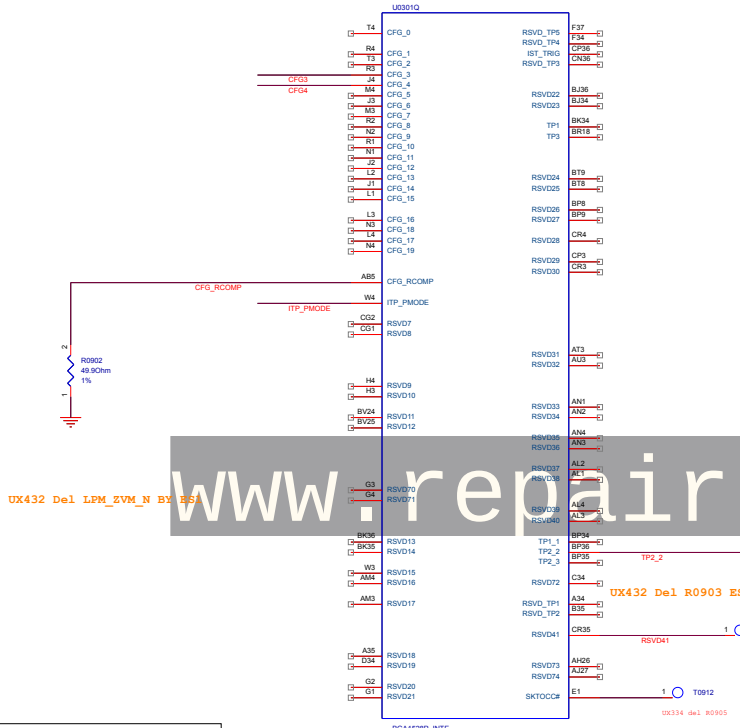
+VCCCORE	
+VCCSA	System Agent power rail
+VCCGT	Sliced graphics power rail
+1.05V_VCCPLL=+VCCST	CPU PLL power rails
VCCSTG =1.05V	IO power rail
+VCCPLL_OC=+1.2V	CPU digital PLL power rails
+VDDQ_CPU=+1.2V	CPU Memory power rail, voltage dependent on memory technology
+VCCST	Sustain voltage for processor in Standby modes
+VCCIO = 1.05V	Voltage for the memory controller and shared cache



On Package Cache resistance Compensation
from processor: Refer to the appropriate platform
design guide for implementation details and values.
Unconnected for Processors without OPC.

No OPC Check remove 且R0811 R0810量測兩端為0V 0126





6.2 Reset and Miscellaneous Signals

Table 6-5. Reset and Miscellaneous Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted: — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • **CFG[1]**: Reserved configuration lane. • **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal. — 1 = Normal operation — 0 = Lane numbers reversed. • **CFG[3]**: Reserved configuration lane. • **CFG[4]**: eDP enable: — 1 = Disabled. — 0 = Enabled. • **CFG[6:5]**: PCI Express* Bifurcation — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • **CFG[7]**: PEG Training: — 1 = (default) PEG Train immediately following RESET# de assertion. — 0 = PEG Wait for BIOS for training. • **CFG[19:8]**: Reserved configuration lanes.	I	GTL	SE	U - Processor Lines. CFG[2], CFG[6:5] and CFG[7] are not relevant for U - Processor Lines.
CFG_RCOMP	**Configuration Resistance Compensation**	N/A	N/A	SE	U-Processor Line
PROC_POPIRCOMP	**POPIO Resistance Compensation**	N/A	N/A	SE	U-Processor Line
IST_TRIG	**Impedance Spectrum Tool Trigger:** trigger point to support debug of possible power issues. Refer to the appropriate processor Platform Design Guide (see Related Documents section) for complete implementation details.	O	GTL	SE	U-Processor Line

TP for Boundary Scan Test

T0910 1 — CFG3
T0911 1 — ITP_PMODE

CFG STRAPS

CFG4 — R0901 1 2 1KOhm

	1	0	NOTE
CFG4	DISABLE	ENABLE	eDP ENABLE

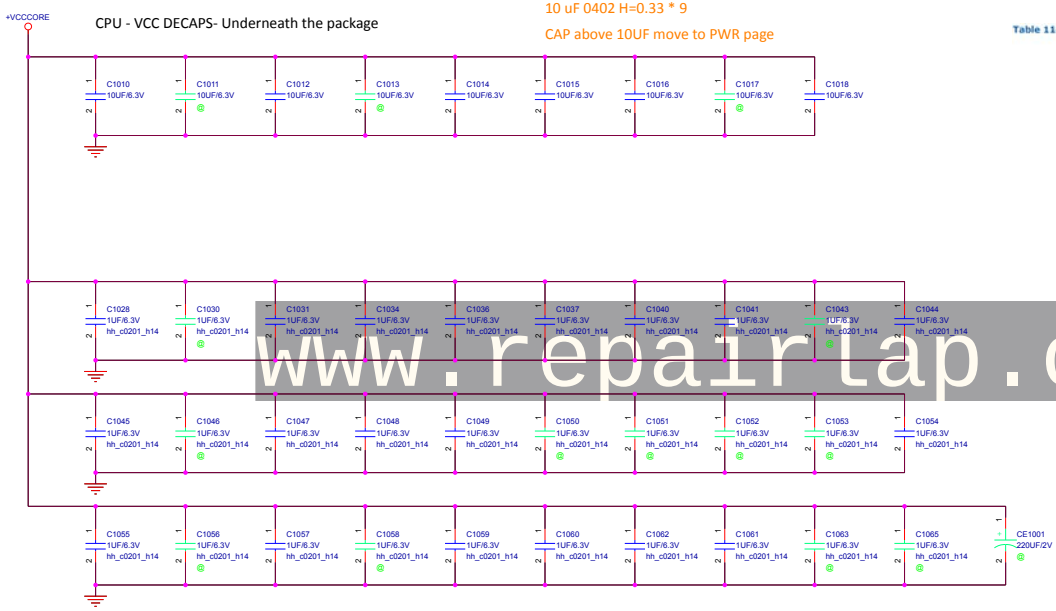
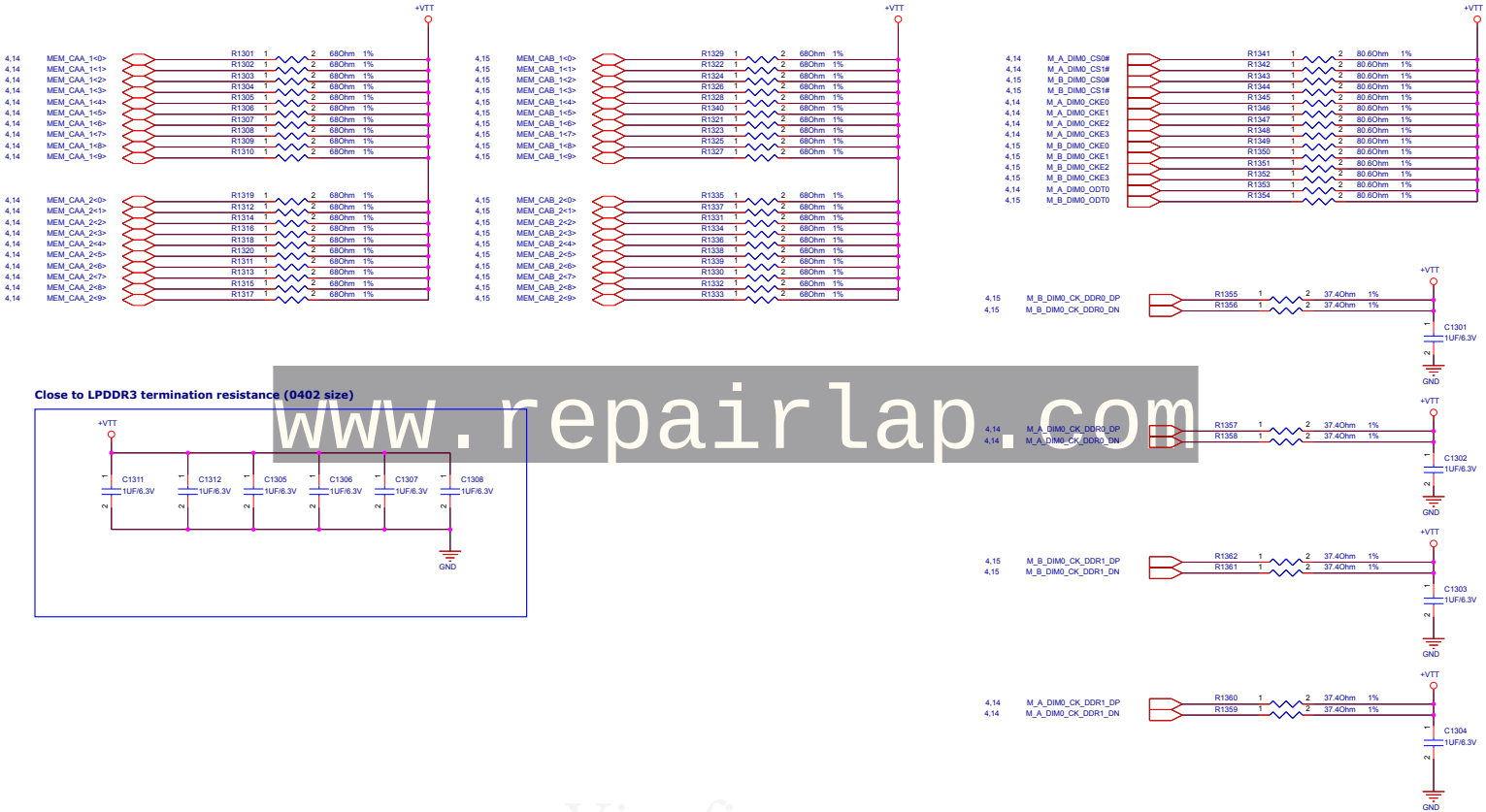


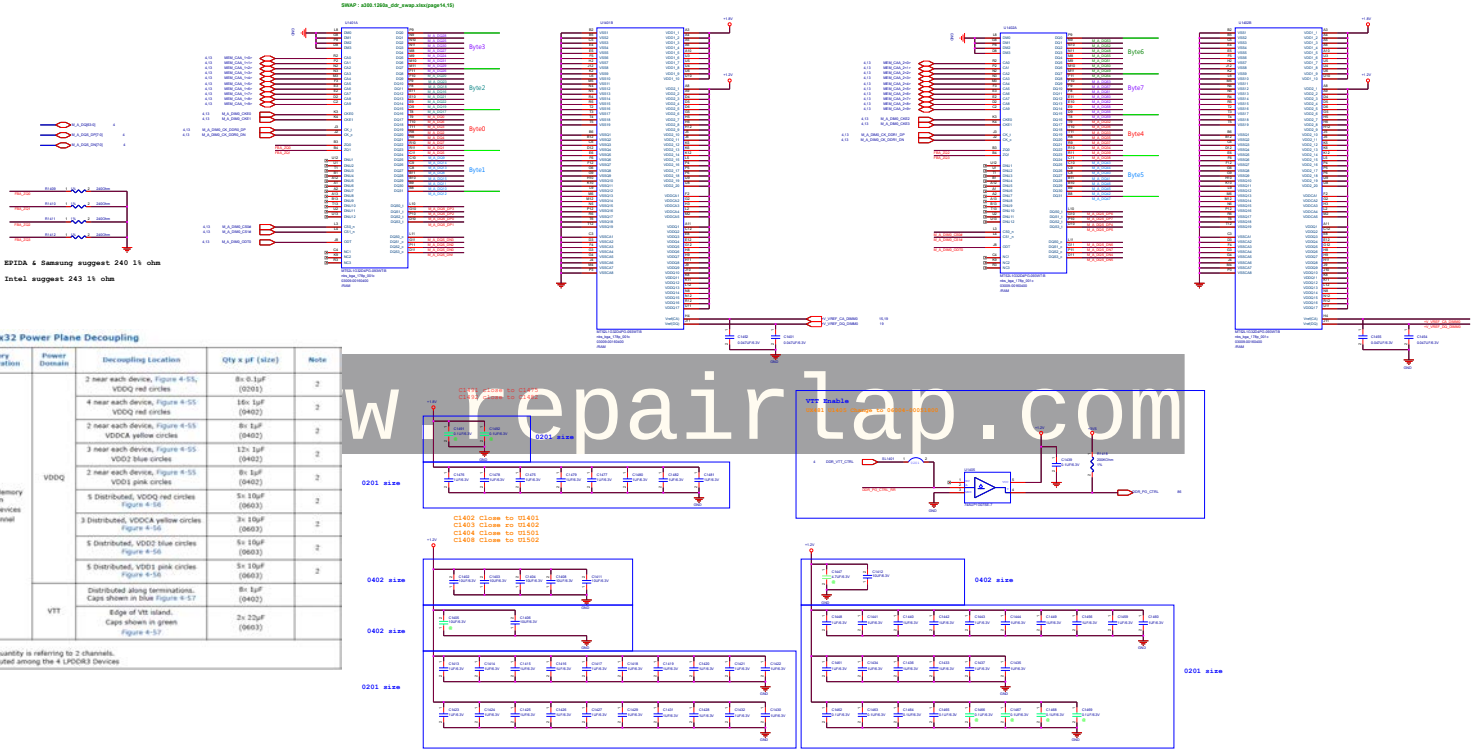
Table 11-2. Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 1 of 2)

Domain	Primary Side cap	Secondary Side cap	Placement guideline
$V_{CC_{CORE}}$		42x 1uF 0402/0201	To be placed as close as possible to the vias that connect to the BGA pins.
		14x 10uF 0402	
		9x 22uF 0603	
	8x 10uF 0402		Place as close to the package as possible
	18x 47uF 0805 (6.3V)		Place as close to the package as possible. Can be placed on as either Primary or back side cap.
$V_{CC_{GT}}$	15x 22uF 0603		Place as close to the package as possible
	4x 47uF 0805 (6.3V)		
		11x 1uF 0402/0201	Place as close to the package as possible
		15x 10uF 0402	

+VCCCORE DeCap
0201 1uF/6.3V X5R h14 *30
0402 10uF/6.3V X5R h13 * 9



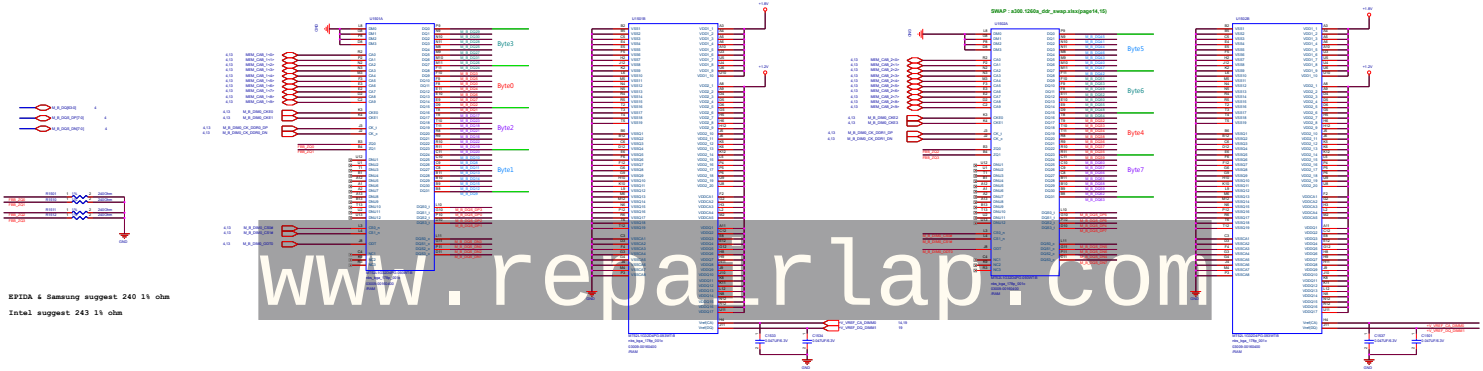
Close to LPDDR3 termination resistance (0402 size)



LPDDR3 x32 Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
LPDDR3 Memory Down x32 - 2 Devices per Channel	VDDQ	2 near each device, Figure 4-55, VDDQ red circles	8x 0.1µF (0201)	2
		4 near each device, Figure 4-55 VDDQ red circles	16x 1µF (0402)	2
		2 near each device, Figure 4-55 VDDCA yellow circles	8x 1µF (0402)	2
		3 near each device, Figure 4-55 VDD2 blue circles	12x 1µF (0402)	2
		2 near each device, Figure 4-55 VDD1 pink circles	8x 1µF (0402)	2
		5 Distributed, VDDQ red circles Figure 4-56	5x 10µF (0603)	2
		3 Distributed, VDDCA yellow circles Figure 4-56	3x 10µF (0603)	2
		5 Distributed, VDD2 blue circles Figure 4-56	5x 10µF (0603)	2
		5 Distributed, VDD1 pink circles Figure 4-56	5x 10µF (0603)	2
	VTT	Distributed along terminations. Caps shown in blue Figure 4-57	8x 1µF (0402)	
		Edge of VTT island. Caps shown in green Figure 4-57	2x 22µF (0603)	

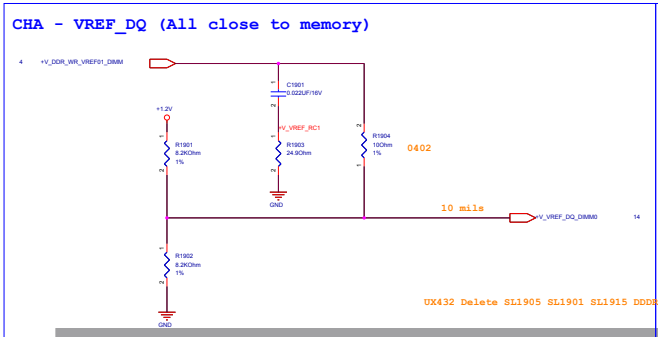
Notes:
1. Total quantity is referring to 2 channels.
2. Distributed among the 4 LPDDR3 Devices



EPIDA & Samsung suggest 240 1% ohm

Intel suggest 243 1% ohm

Power plan:1.2V



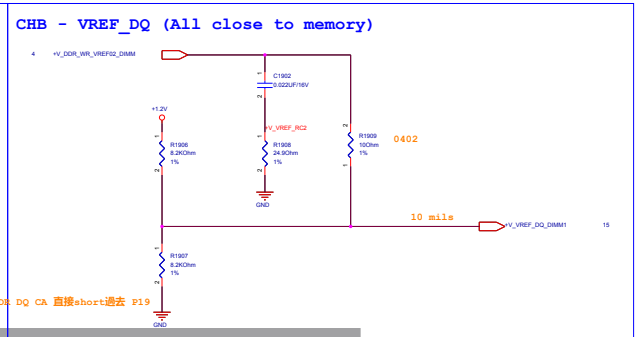
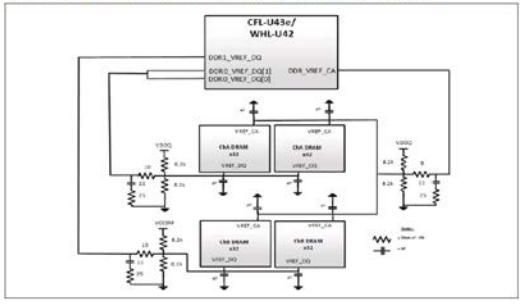
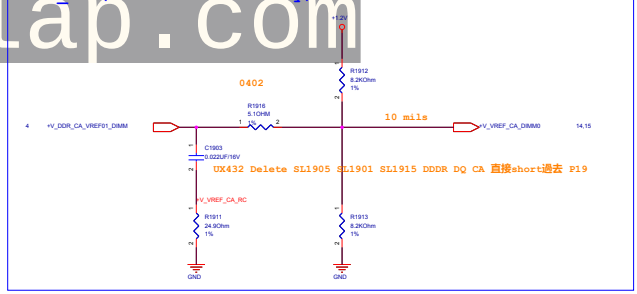
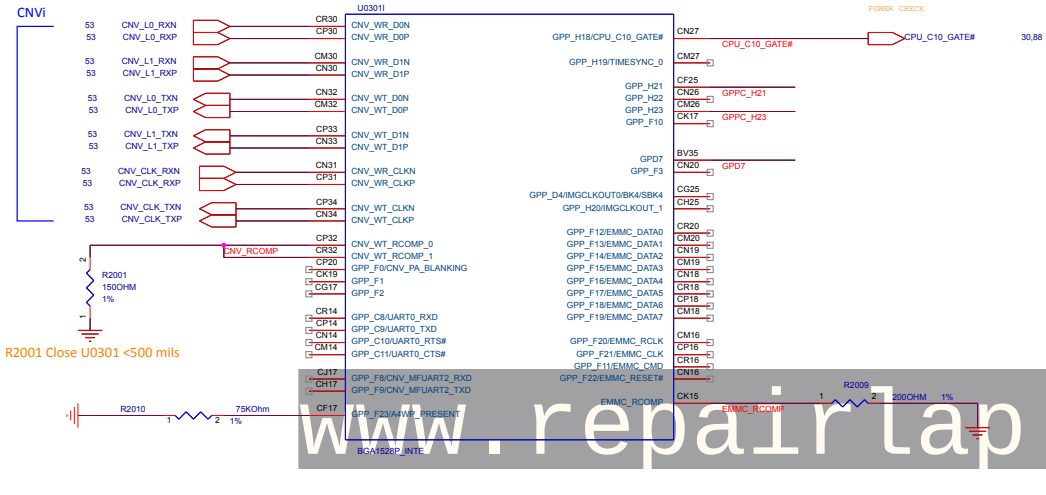


Figure 3-1. WHL U LPDDR3 x32 Memory Down V_{REF-DQ} and V_{REF-CA} Overview

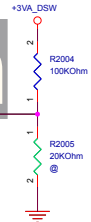






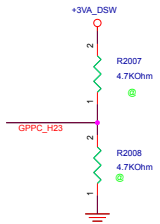
CFL CRB v0.8 page#44

GPPC_H21:	
PU	24Mhz
PD	38.4/19.2MHZ



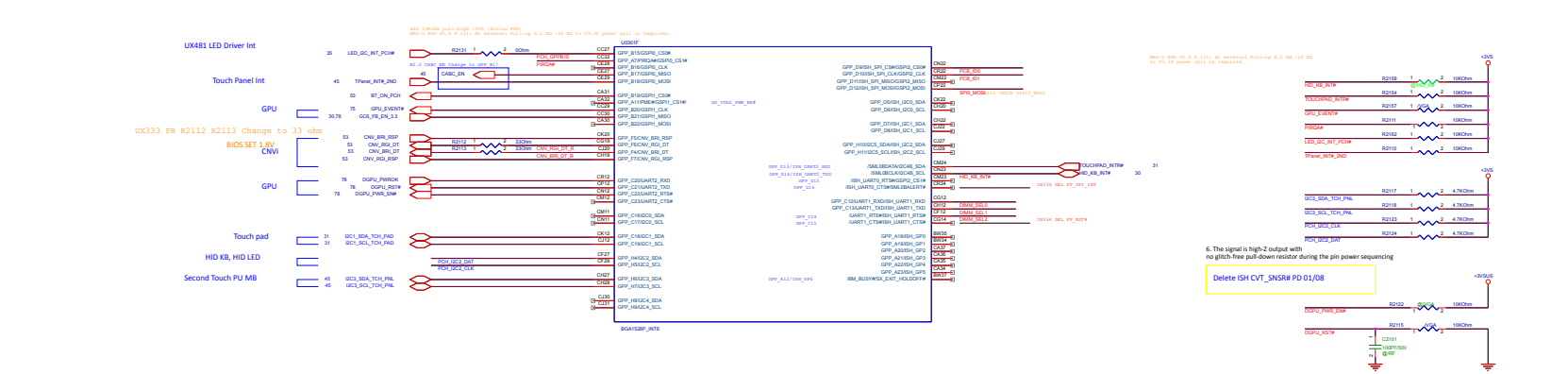
GPD7:	
PD	XTAL INPUT IS SINGLE ENDED
PU	XTAL IS ATTACHED

ESPI

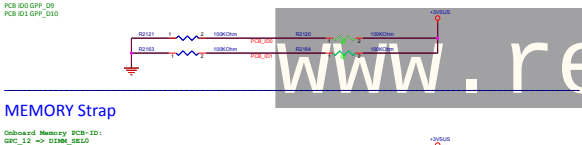


GPPC_H23: INTERNAL WEAK PD	
PU	SAF
PD	MAF

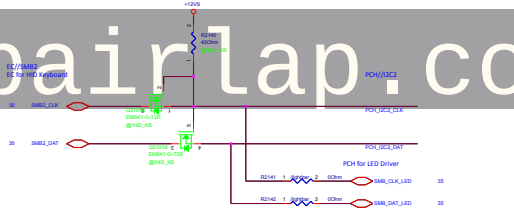
UX432UA Change Follow CRB



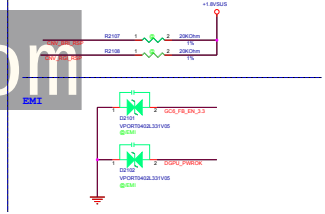
PCB ID



System Management Interface



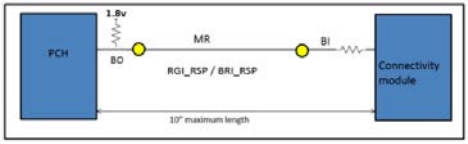
UX432 ADD R2108 Intel Feedback



MEMORY Strap

2133	SAM 8G	Micron 8G	Hynix 8G	SAM 16G	Micron 16G	Hynix 16G
DIMM_SEL0	L,R2101	L,R2101	H,R2102	L,R2101	L,R2101	H,R2102
DIMM_SEL1	L,R2103	H,R2104	H,R2104	L,R2103	H,R2104	H,R2104
DIMM_SEL2	L,R2105	L,R2105	L,R2105	H,R2106	H,R2106	H,R2106

Memory LPDDR3	2133-8G (16Gb)	03009-00030900	//MICRO/MT52L512M32D2PF-093 WT:B
		03009-00031200	//SAMSUNG/K4E6E304EC-EGCG
		03009-00031000	//HYNIX/H9CCNNNBJTALAR-NVD
	2133-16G (32Gb)	03009-00160400	//MICRON/MT52L1G32D4PG-093 WT:B
		03009-00160700	//SAMSUNG/K4EBE304EC-EGCG
		03009-00160500	//HYNIX/H9CCNNNCLGALAR-NVD



Boot BIOS Strap Bit BBS

UX305UA remove 0429

PCH_GPPB22: weak internal pull down	
PU	LPC
PD	SPI (Default)

No Reboot

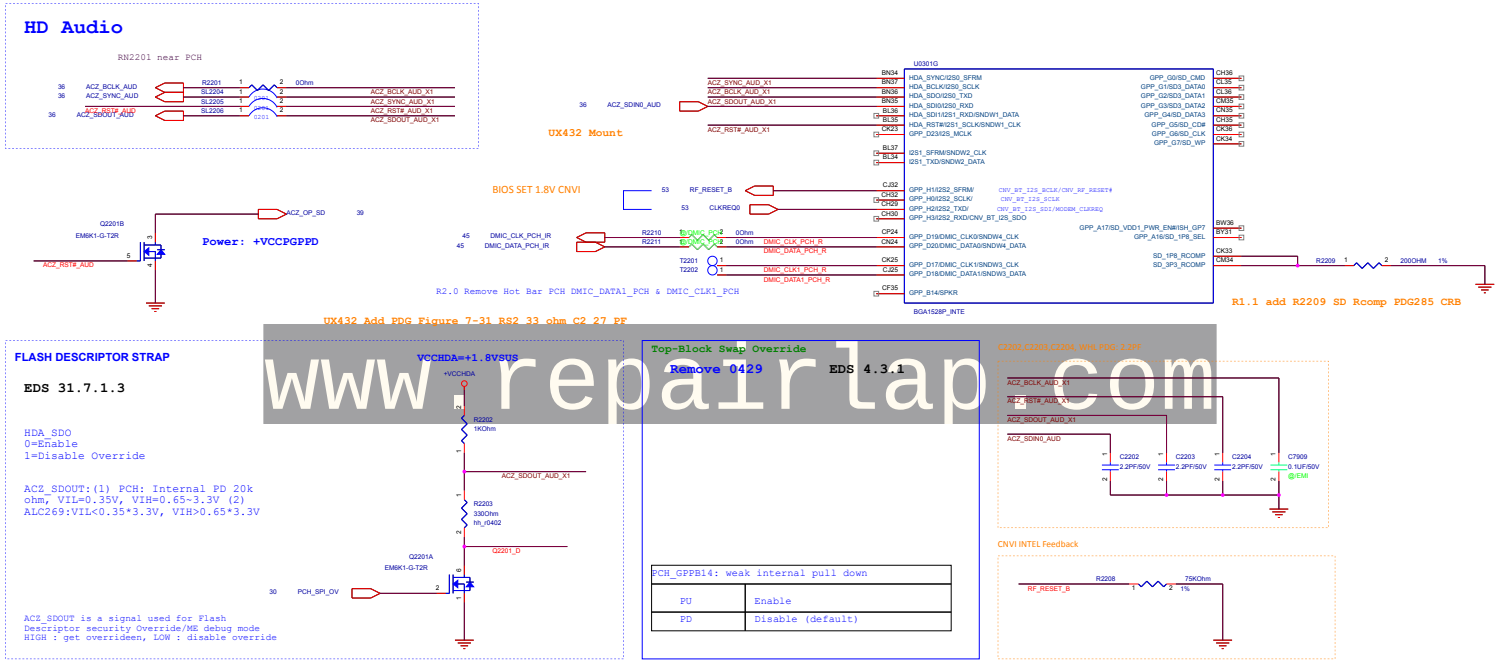
UX305UA remove 0429

NOTE: Enable No Reboot
PCH will disable the TCO
Timer system reboot feature.
This function is useful when running ITP/XDP.

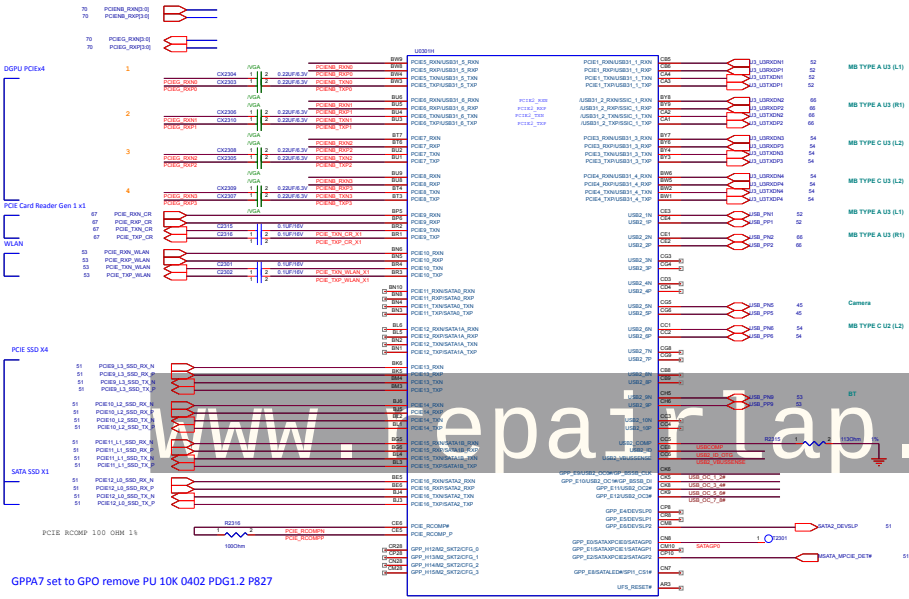
PCH_GPPB18: weak internal pull down	
PU	Enable
PD	Disable

UX391RA add 0803

PCH_GPPD12:
External pull-up is required
(CNL_PCH EDS 0.7 #56)



Intel: To enable Flash Descriptor Security Override, this signal should be pulled up to VCCHDA through a 1 KΩ to 2.2 KΩ ±5% resistor.



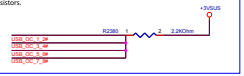
GPPA7 set to GPO remove PU 10K 0402 PDG1.2 P827

PCI-E* X1	PCIE USAGE DEFAULT/OPTION	Co-lay	Clock
PCIE 5	DGPU		Port 5
PCIE 6			
PCIE 7			
PCIE 8			
PCIE 9	Card Reader		Port 0
PCIE 10	WLAN		Port 2
PCIE 11			
PCIE 12			
PCIE 13	PCIE SSD		Port 1
PCIE 14			
PCIE 15 / SATA 1			
PCIE 16/ SATA 2		SATA SSD	

	USB 2.0		USB 3.0
1	USB 3.0 Type A (L1)	USB3_1	USB 3.0 Type A (L1)
2	USB 3.0 Type A (R1)	USB3_2	USB 3.0 Type A (R1)
3		USB3_3	USB 3.0 Type C (L2)
4		USB3_4	USB 3.0 Type C (L2)
5	Camera		
6	USB 3.0 Type C (L2)		
7			
8			
9	BT		
10			

Merge 0119

If unused, DC [x] pins require a pull-up to V3.3A with 8.2~10 KΩ resistors.



PE_DET

SATA General Purpose

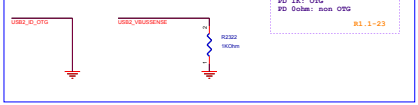
When used as DEVSLP, no external pull-up or pull-down terminaon r equired from SATA Host DEVSLP.

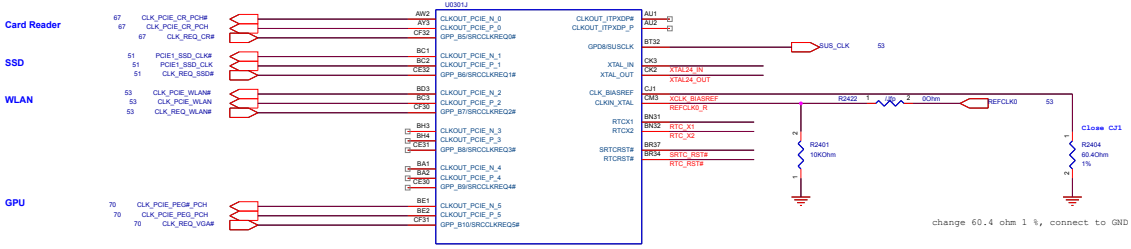
R1.2 SATA_DEVSLP change to DEVSLP2

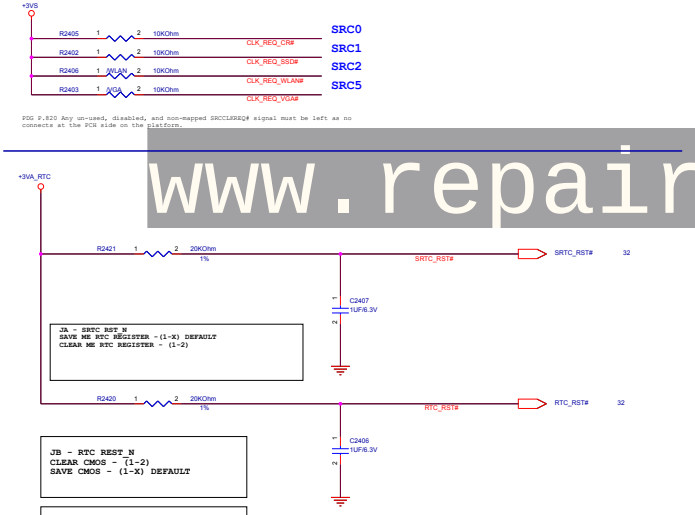
SATA PORT2 0323

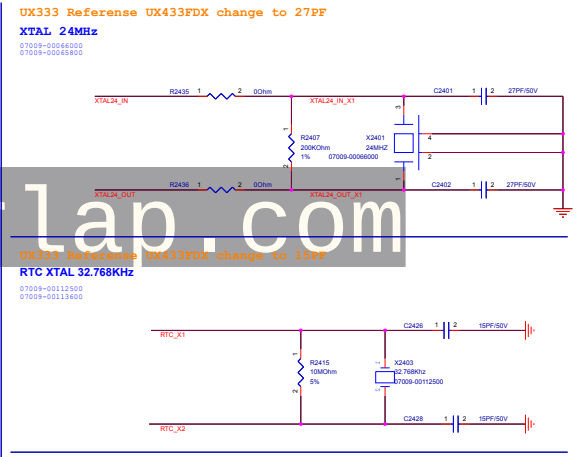
PDG1.2 P.848 Unused SATAGP[2:0] pins can be left as no connect and need to be default to GPIO func onality, refer to an unused GPIO for termina on guidance.

UX390 Remove SL 1203









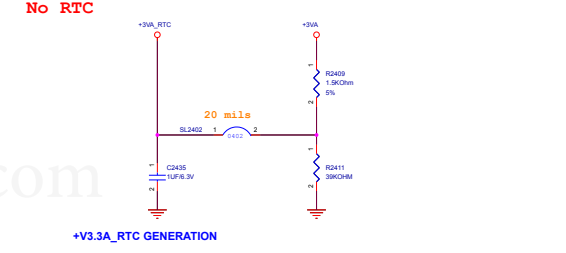
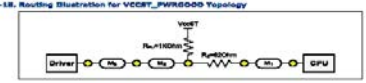
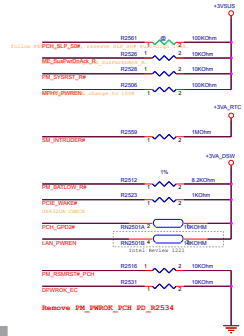


Figure 7-18. Routing Illustration for VCCST_PWRGOOD Topology



PDG 1.2 F.572 PROCPWRGD is used only for power sequence debug and is not required to be connected to anything on the platform.



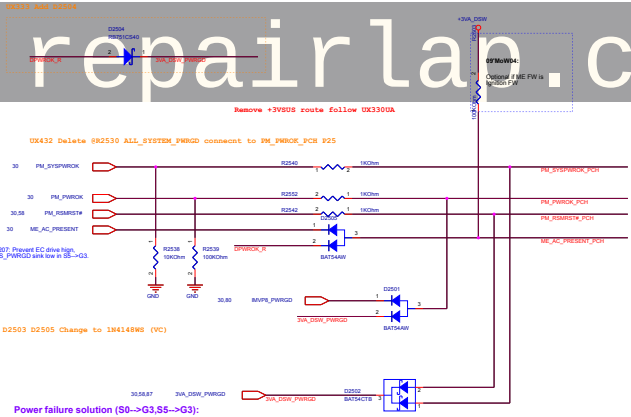
UX432 Delete @U2501 @R2501 R2508 (UX370)

UX432 U2503 Change to D2504 Del @R2504 R2502 Add R2511 R2507

MS Gate for VCCIO

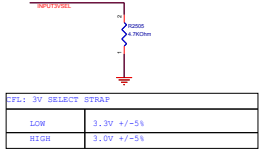
UX431 DEL D2504

Power Sequence



PCH STRAPS

Roger 3/21
UX334 del R2504



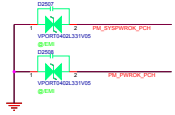
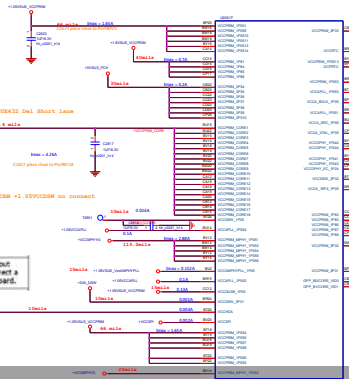


Table 10-3. PCH-U Estimated I_{CC} [4] (Sheet 1 of 2)

Voltage Rail	Voltage (V)	S0 Scenario Current [3] (A)	S0 for Idle Scenario [3] (mA)	Deep Sx Iccmax Value Expected (mA)	S3 (µA)
VCCA_1P05_UPDS	1.05	0.017	0.007	0	0
VCCAPLL_1P05	1.05	0.102	0.058	0	0
VCCA_BCLK_1P05	1.05	0.059	0.034	0	0
VCCA_OSC_1P05	1.05	0.034	0.012	0	0
VCCA_XTAL_1P05	1.05	0.002	1	0	0
VCCPRIM_1P05	1.05	1.425	2.432	0	0
VCCPRIM_MPHY_1P05	1.05	2.878	2	0	0
VCCAMPHYPLL_1P05	1.05	0.102	1	0	0
VCCPRIM_1V8S	1.85	4.36	30.987	0	0
VCCCLOCK_1P85	1.85	0.139	0.126	0	0
VCCCSME_1P85	1.85	0.819	1	0	0
VCCPRIM_1V8	1.8	0.498	1	0	0
VCCPRIM_1P0	1.0	0.199	1	0	0
VCCHDA	3.3	0.008	±0.001	0	0
	1.8	0.004	±0.001	0	0
	1.0	0.002	±0.001	0	0
VCCSPI	3.3	0.002	±0.001	0	0
	1.8	0.002	±0.001	0	0
VCCCSME_3P3	3.3	0.001	1	1	0
VCCCSME_1P05	1.0	0.007	1	1	0
VCCRTC	3.0	0.002	0.004	1824	6
VCCSPI1_1P8	1.24	0.01	0.078	0	0

Notes:
1. S3 state shown to provide an estimate of battery life.
2. Sx (S5) data is taken with VCCRTC at 3.0V while the system is in a mechanical-off (G3) state at room temperature.
3. Platform application assumes Low R_{DS}.
4. The Iccmax value is a steady state current that can happen after respective power sit has asserted (or reset signal has de-asserted).
5. Sx (or Idle assumes PCH is idle and not in power gate).

VCCDSW_1P05	**Deep Sx Well**: 1.05V. This rail is generated by on die DSW low dropout (LDO) linear regulator to supply DSW core logic. Board needs to connect a 1uF capacitor to this rail and power should NOT be driven from the board.



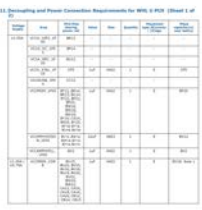
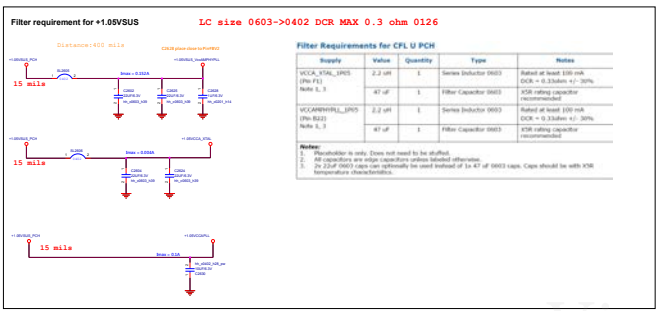


Table 11-11. Decoupling and Power Connection Requirements for WHL U PCH (Sheet 2 of 2)

Voltage Supply	Area	PCH Pins Sharing Power Rail	Value	Size	Quantity	Placement Note (Closest to Pin/Ball)	Place capacitor (x) near ball(s)
V1.8A	VCCPRIM_1P8	CC18, CC19, CD18, CF23, CC15, CD15, CD16, CF17	1uF	0402	1	B	CF17
			1uF	0402	1	B	CF23, Note 1
V1.1A	VCCPRIM_3P3	CB16, CB15, CC22, CC23, CD17, CF19, BP15, CF18	0.1uF	0402	1	B	CF23, Note 2
			1uF	0402	1	B	CF23, Note 1
V3.3A/ V1.8A	VCCSPI	BV23	-	-	-	-	-
V3.3A/ V1.8A	VCCHDA	BT20	-	-	-	-	-
V3.3DS	VCCDSW_1P05	BK24, BT23	1uF	0402	1	B	BK24, Note 3
V3.3RTC	VCCRTC	BN23	1uF	0402	1	B	BN23
			0.1uF	0402	1		
PCH Internal use	VCCDSW_1P05	BT24	1uF	0402	1	B	BT24
	VCCRTCEXT	BP24	0.01	0402	1	B	BP24, Note 1
	VCCDPHY_1P1	BY15, CA15, CP23, BY24, CA24	4.7uF	0402	1	B	CP23

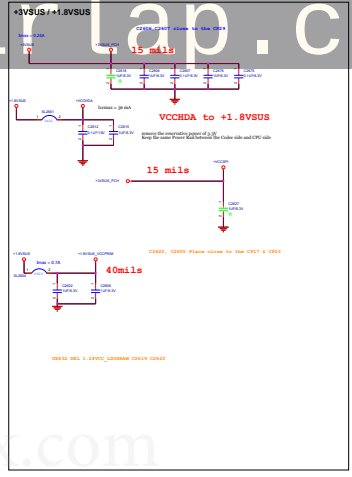
Notes:
1. Placeholder only. Does not need to be stuffed.
2. Note that some decoupling capacitors are shared between more than 1 rail. Follow the "Place capacitors near balls" instructions above to ensure the sharing is optimized.
3. Place capacitor on the same side of the PCB as the PCH and as close to the edge of package.
4. For description of [P]ullnote, and [C]ap decoupling capacitor placement, refer to "Loop Inductance Reduction Decoupling"
5. Refer to Electromagnetic Interference chapter for recommended placement
6. Please refer to the vendor requirements for bulk decoupling which will be in addition to the recommendation mentioned in the table above.

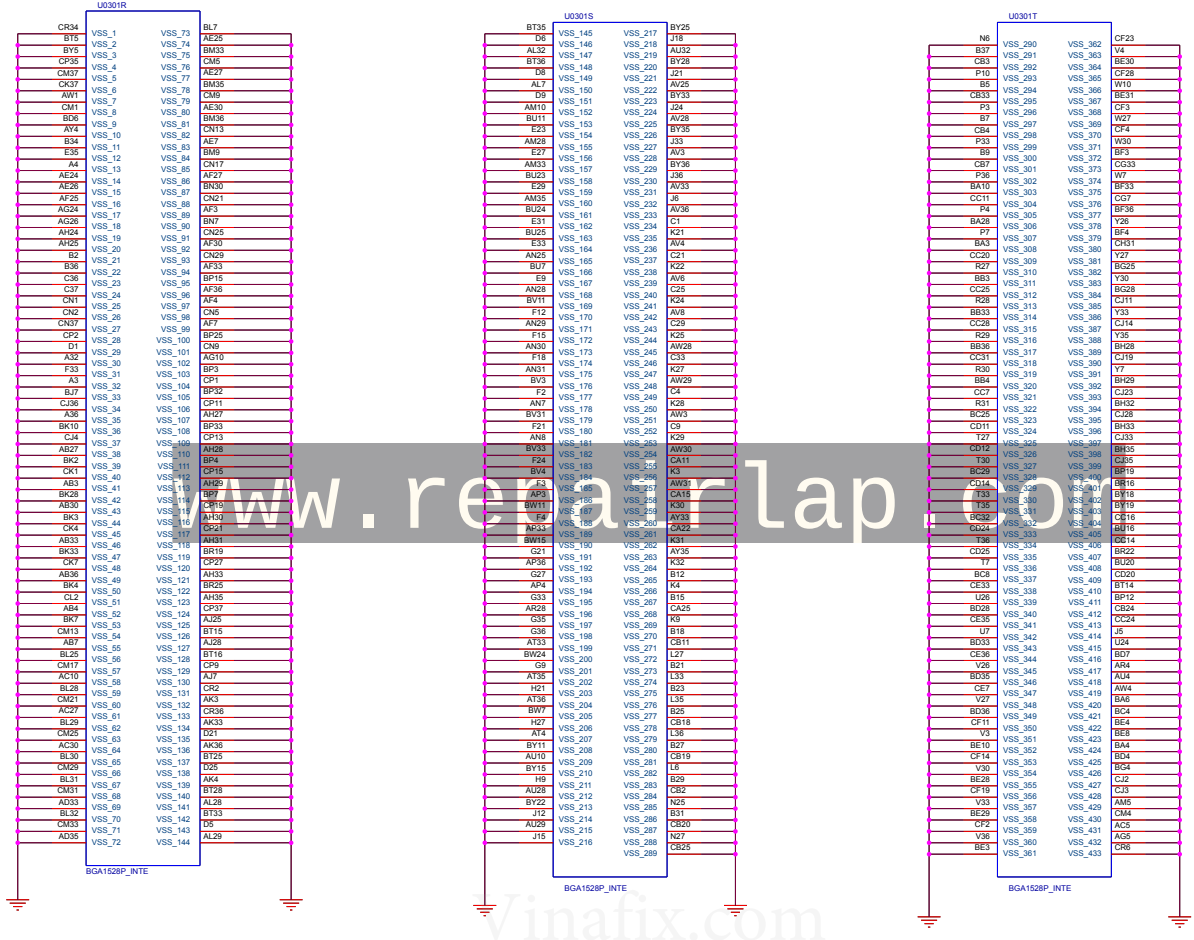


Filter Requirements for CFL U PCH

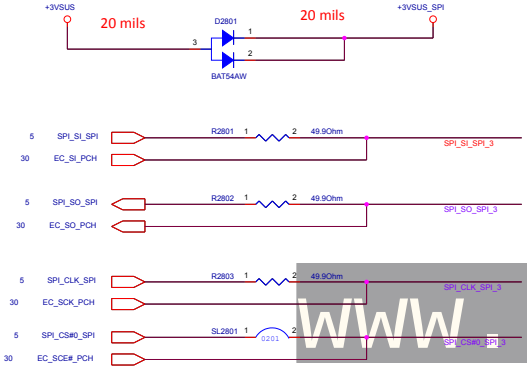
Supply	Value	Quantity	Type	Notes
VCCA_XTAL_1P05 (Pin F1) Note 1, 3	2.2 uH	1	Series Inductor 0603	Rated at least 100 mA DCR = 0.33ohm +/- 30%
	47 uF	1	Filter Capacitor 0603	X5R rating capacitor recommended
VCCAMPHYPLL_1P05 (Pin B22) Note 1, 3	2.2 uH	1	Series Inductor 0603	Rated at least 100 mA DCR = 0.33ohm +/- 30%
	47 uF	1	Filter Capacitor 0603	X5R rating capacitor recommended

Notes:
1. Placeholder is only. Does not need to be stuffed.
2. All capacitors are edge capacitors unless labelled otherwise.
3. 2x 22uF 0603 caps can optionally be used instead of 1x 47 of 0603 caps. Caps should be with X5R temperature characteristics.



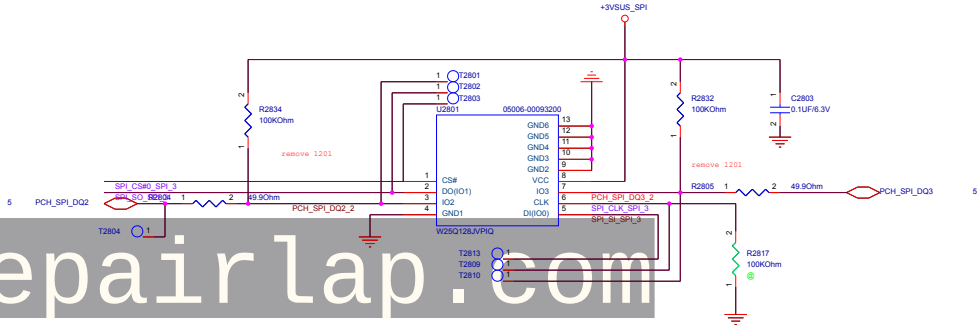


SPI PCH Power

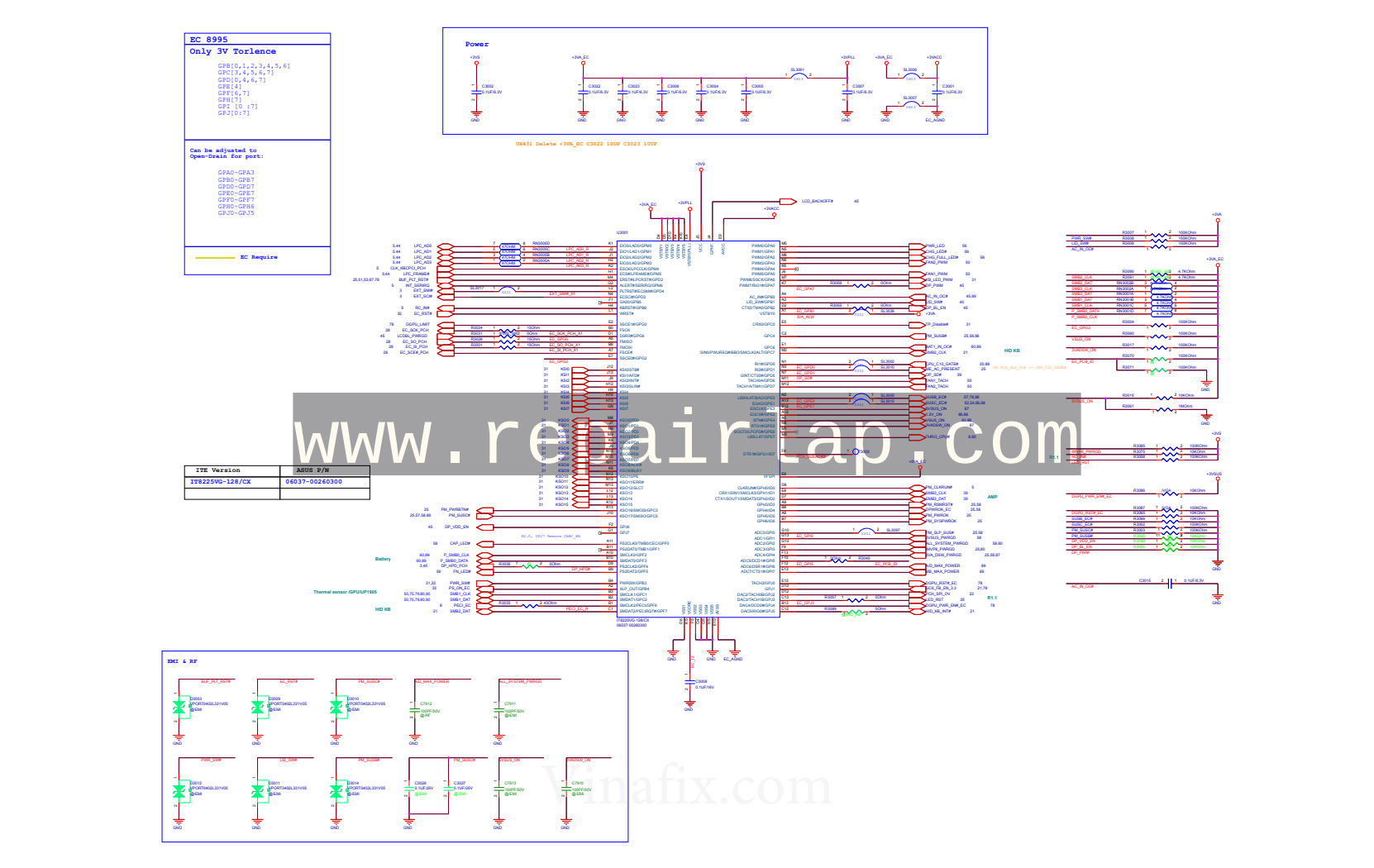


PCH SPI 128M (for IT8225)

Main:05006-00093200
2nd:05006-00093700

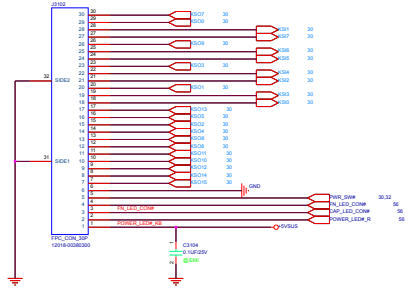


System Management Interface


EC 8995
Only 3V Torlence
GPB[0,1,2,3,4,5,6]
GPC[3,4,5,6,7]
GPD[0,4,6,7]
GPE[4]
GPF[6,7]
GPH[7]
GPI [0 :7]
GPJ[0:7]
Can be adjusted to
Open-Drain for port:
GPA0-GPA3
GPB0~GPB7
GPD0~GPD7
GPE0~GPE7
GPF0~GPF7
GPG0~GPG6
GPJ0~GPJ5
EC Require
Power
UX431 Delete +3VA_EC C3022 10UF C3023 10UF
EMI & RF
ITE Version
ASUS P/N
IT8225VG-128/CX
90037-00260300
www.repair ap com
Vinafix.com

Keyboard_CON.

1st,12018-00380000
2nd,12018-00380300



Keyboard ESD

BL_CON.

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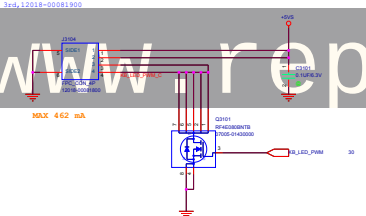
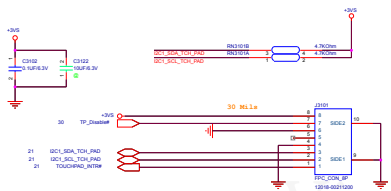
2nd,12018-00081600
3rd,12018-00081900

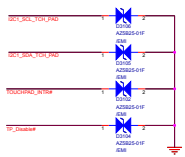


Touch Pad//Number Pad

1st,12018-00211200
2nd,12018-00212200
3rd,12018-00212400

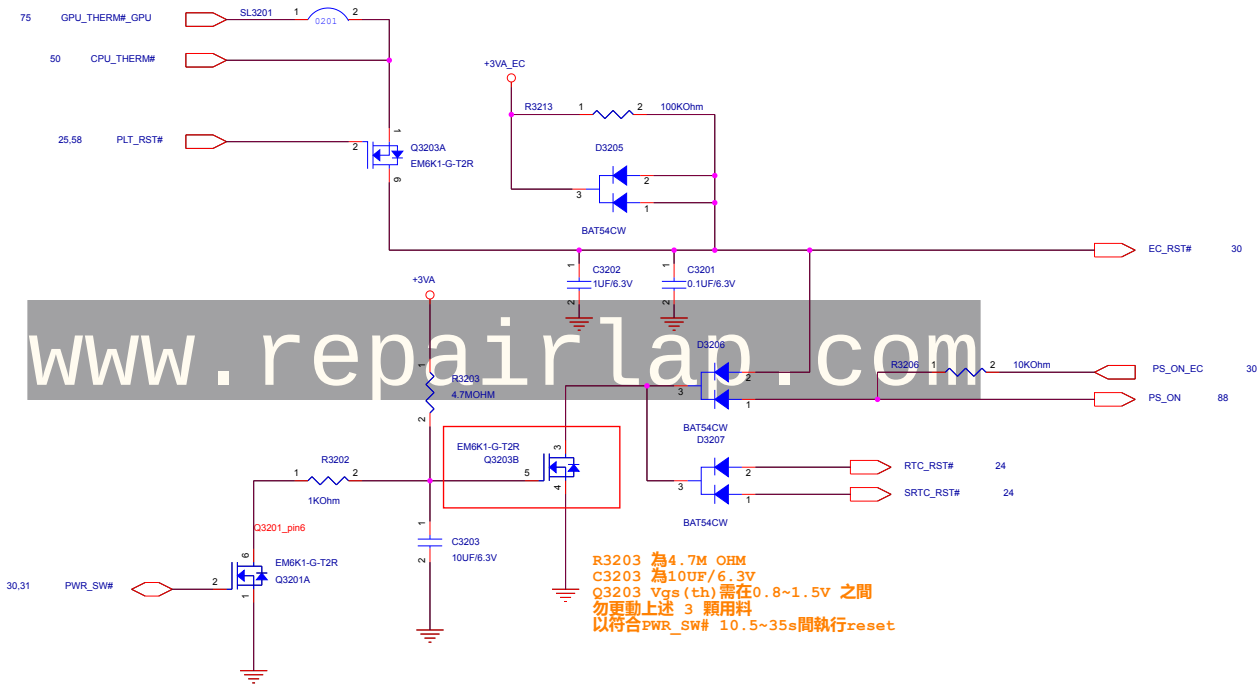


Touch Pad ESD

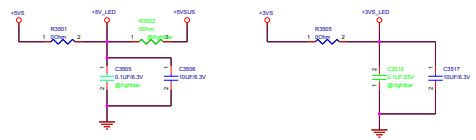


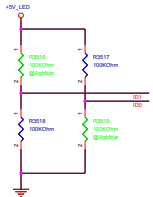
UX481	1	2	3	4	5	6	7	8
CN1	VDD_3.3V	LID_CLOSE	GND	NC	GND	SDA	SCL	INT

Thermal Policy

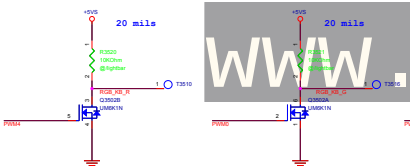


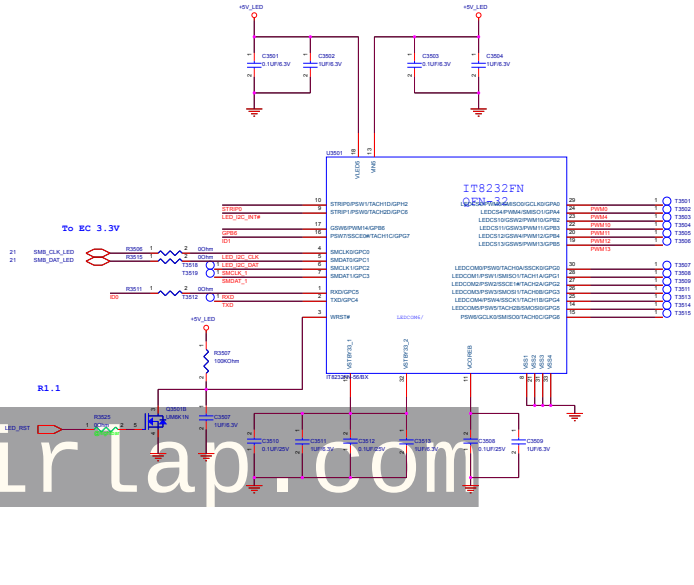
battery embedded (press pwr_sw 40sec, then reset ec & RTC)

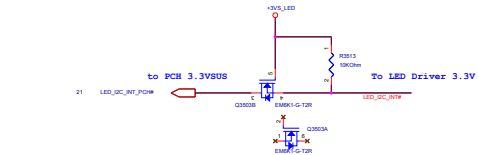


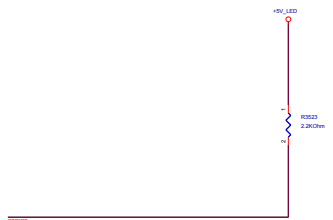


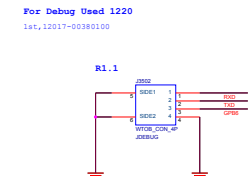
ID0	ID1	Pesture
L	L	5 LEDs
L	H	1 LEDs
H	L	STRIP
H	H	

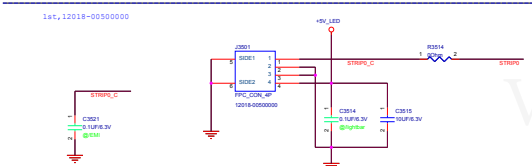




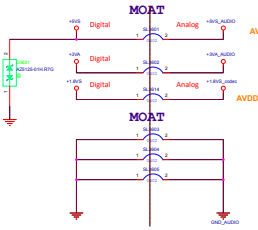




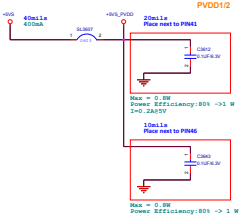




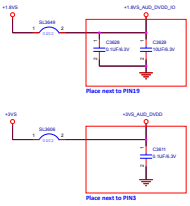
UX432 Del @D3601



UX432 Del @C3601 @C3602 @C3642



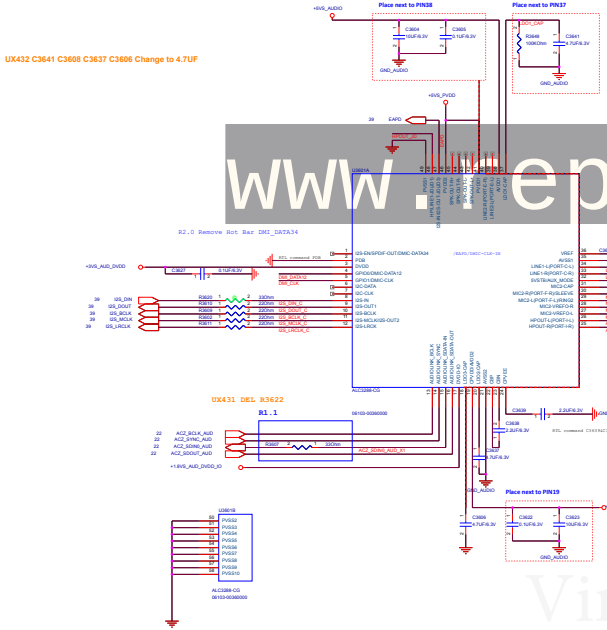
UX432 SL3601 SL3602 SL3614 SL3603 SL3604 SL3605 SL3649 SL3606 0603 change to 0402

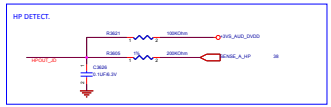


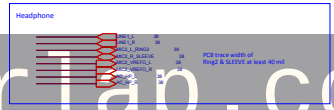
UX432 Del @C3610

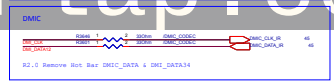
		DVDD (1.8V/3.3V) (mA)	DVDD-IO (1.5V/3.3V) (mA)	AVDD1 (5V) (mA)	AVDD2+CPVDD (1.8V) (mA)	PVDD1/2 (5V) (mA)	Total Power (mW)
1	DVDD=1.8V, DVDD-IO=1.5V	3.399	0.0897	14.45	70.4	1060	5505.14775
2	DVDD=3.3V, DVDD-IO=3.3V	5.905	0.172	14.46	70.66	1080	5610.375

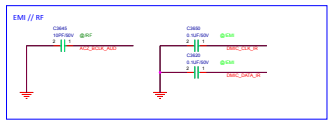
UX432 C3641 C3608 C3637 C3606 Change to 4.7UF

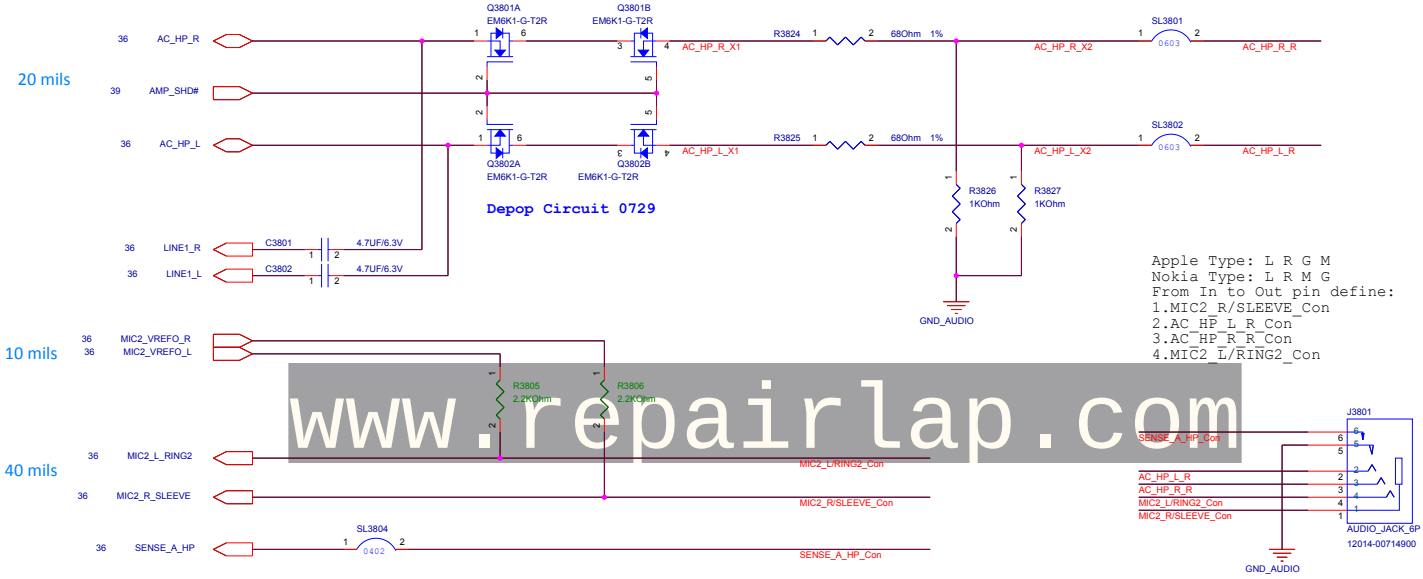




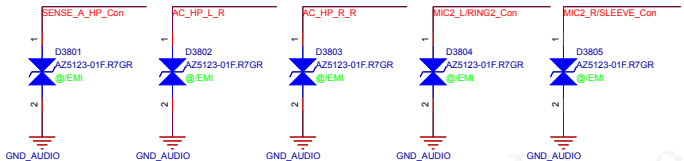




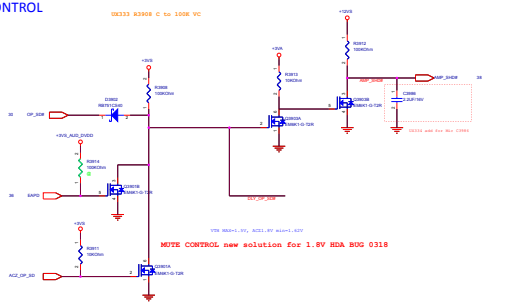




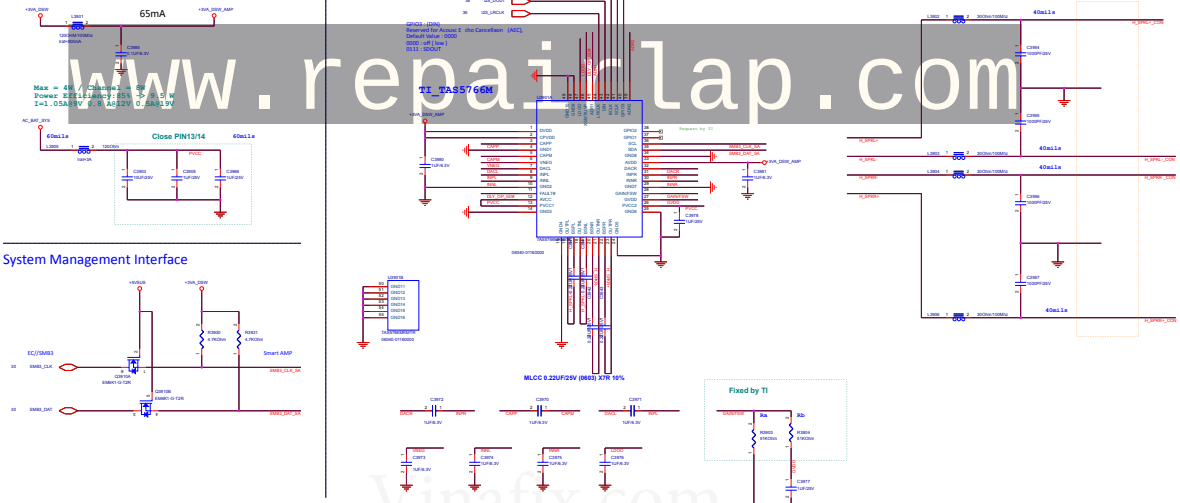
Phone Jack ESD



MUTE CONTROL

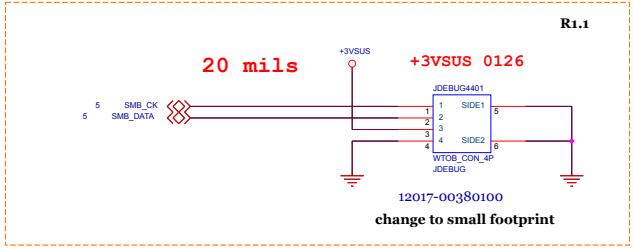


Smart AMP Power



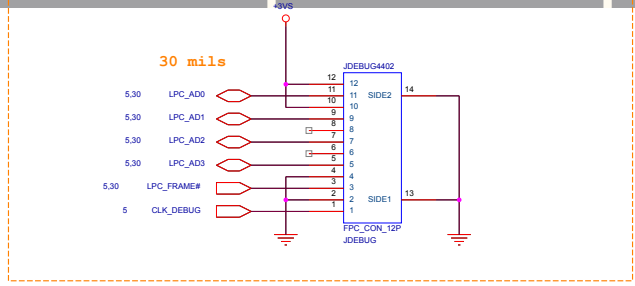
System Management Interface

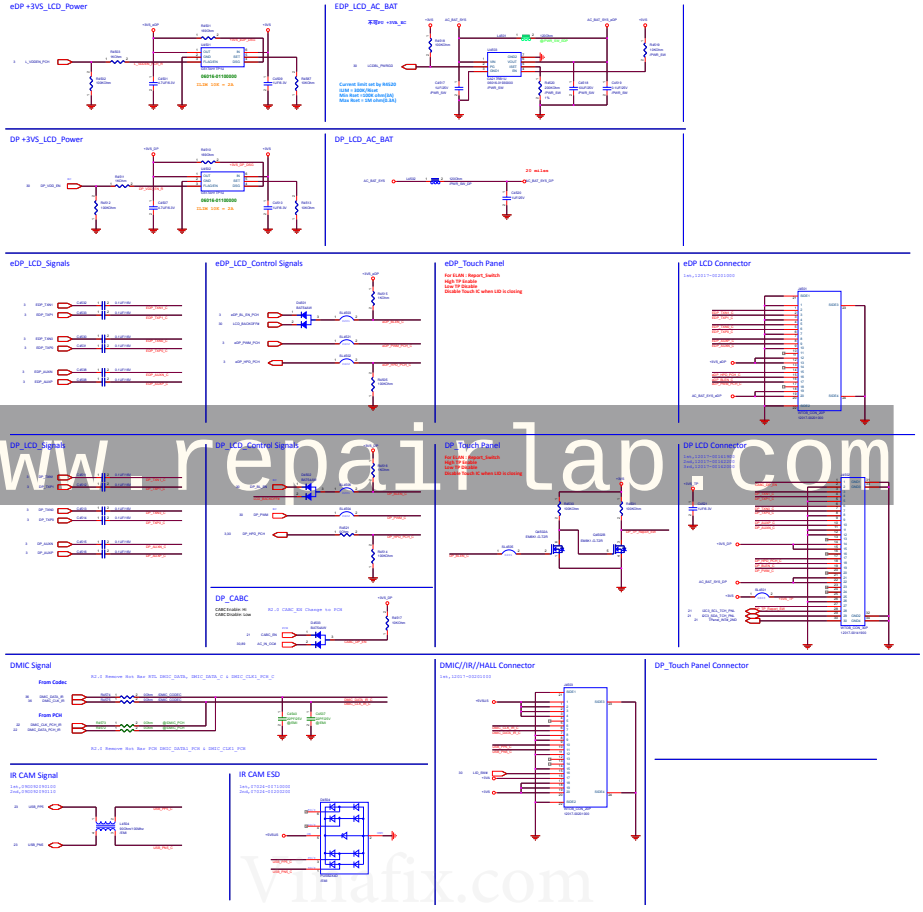
New Design Debug Port



LPC Debug Port

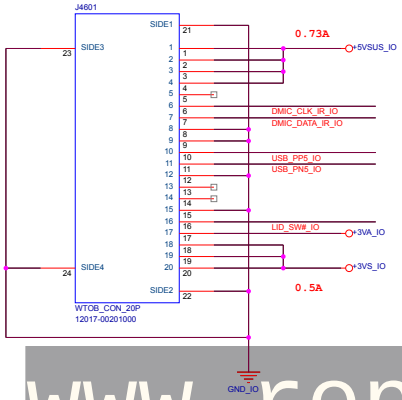
Follow UX370UAR 12018-00102300





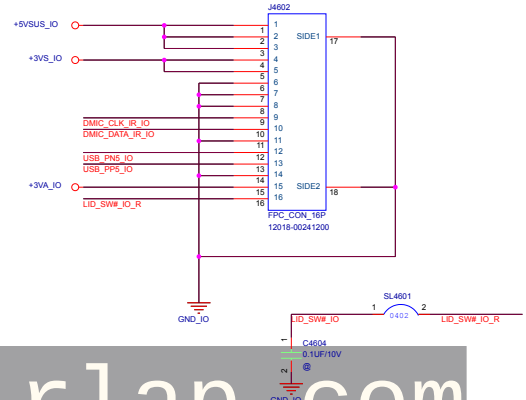
DMIC//IR//HALL Connector

1st,12017-00201000



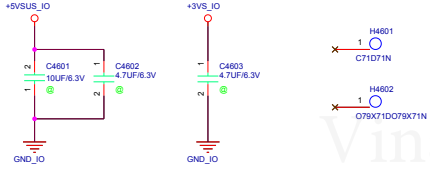
IR Connector

1st,12018-00241200



DMIC CLK Signal

R2.0 Remove Hot Bar DMIC_CLK

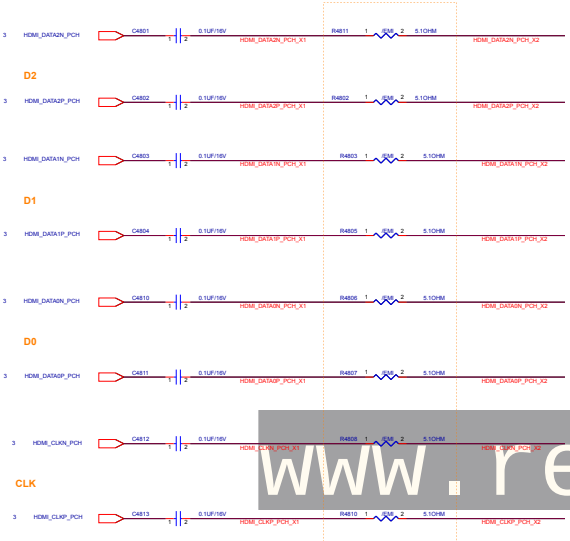


DMIC Connector

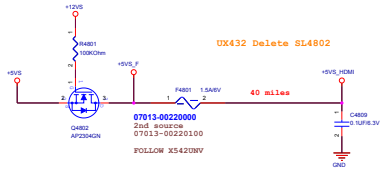
1st,12018-00082900

R2.0 Remove Hot Bar DMIC Connector & DMIC_DATA_IO

HDMI Signals



HDMI Power

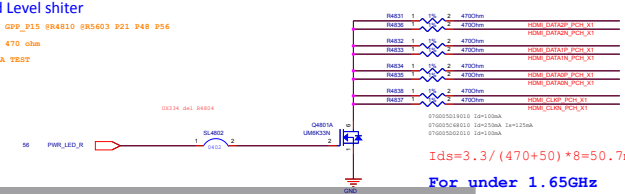


HDMI Cost-reduced Level shiter

UX432 Delete KB_PWR_LED_EN GPP_P15 @R4810 @R5603 P21 P48 P56

HDMI 1.4 WHL PDG Change to 470 ohm

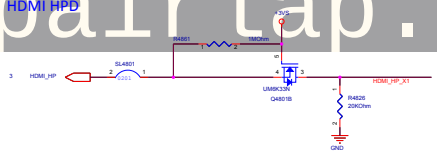
PWR_LED_R For HDMI SLEEP EA TEST



Ids=3.3/(470+50)*8=50.7mA

For under 1.65GHz

HDMI HPD

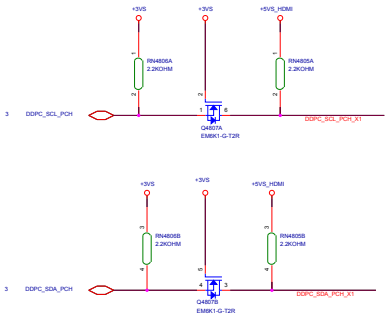


HDMI ESD

070D2807633D

HDMI DDC Level-shifter

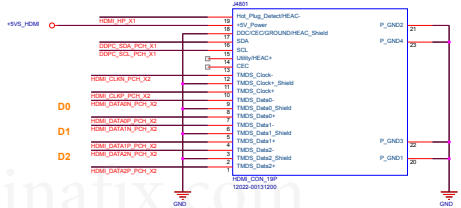
UX432 Delete D4801 D4802



HDMI CON.

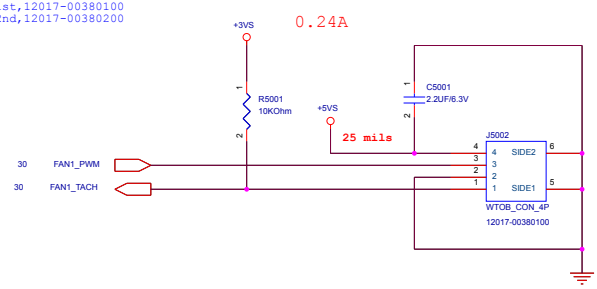
1st,12022-00131200
2nd,12022-00131300

R1.1



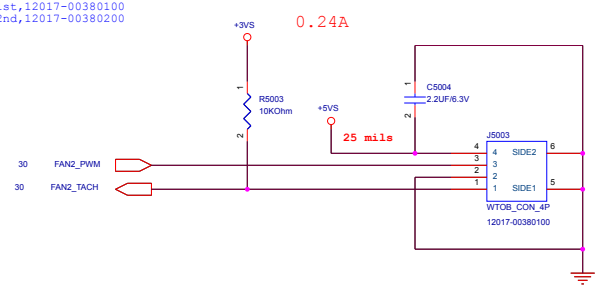
DC FAN Control 1

1st,12017-00380100
2nd,12017-00380200

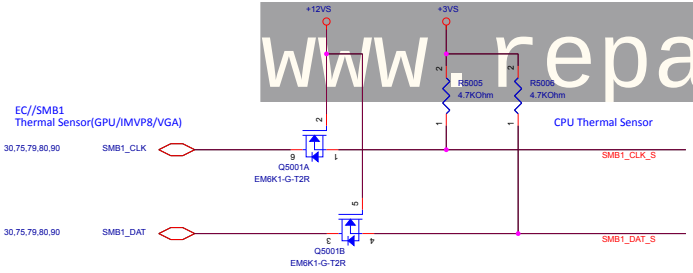


DC FAN Control 2

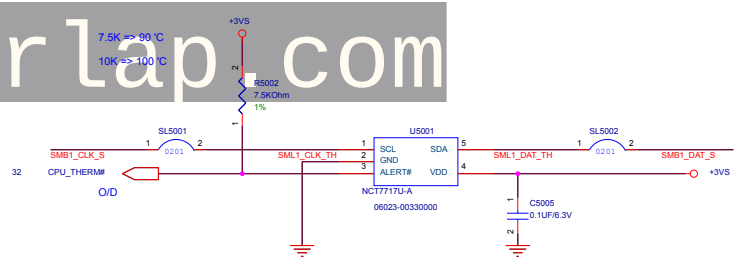
1st,12017-00380100
2nd,12017-00380200



System Management Interface



CPU Thermal Sensor



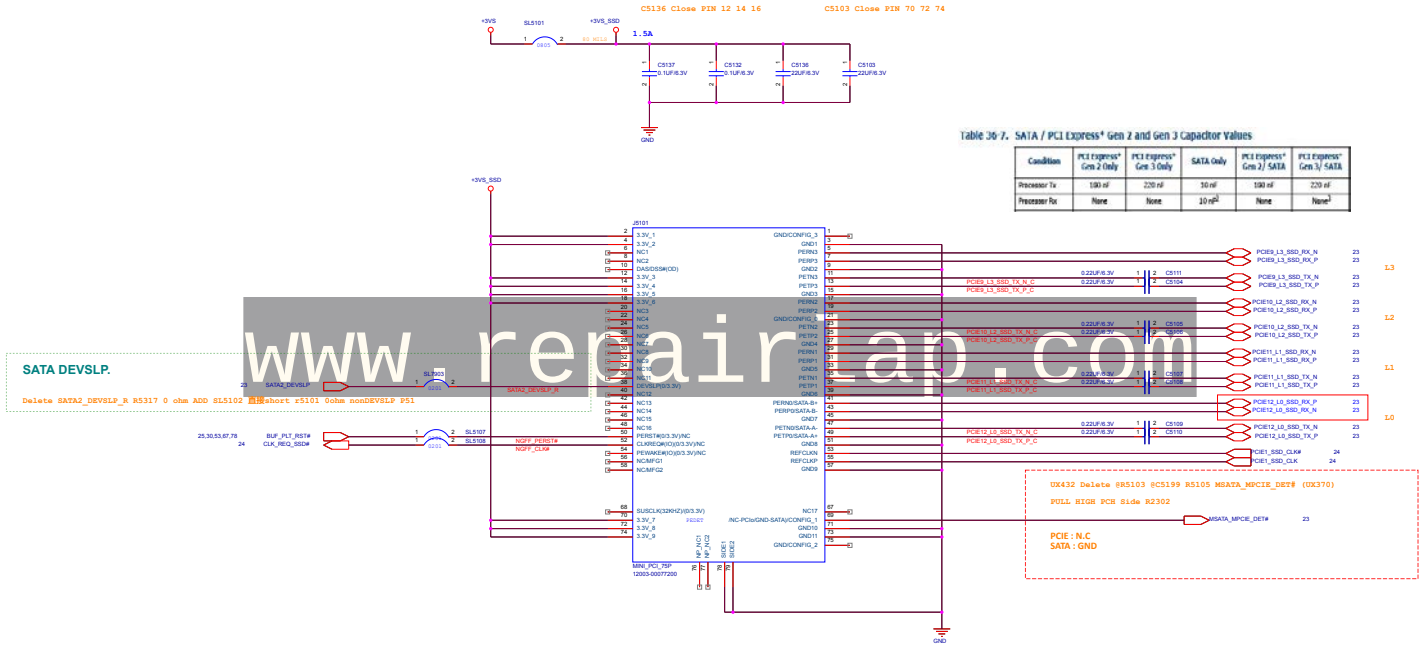
5.3 Address Setting

NCT7717U I2C/SMBus address is 1001000xb (x is R/W bit).

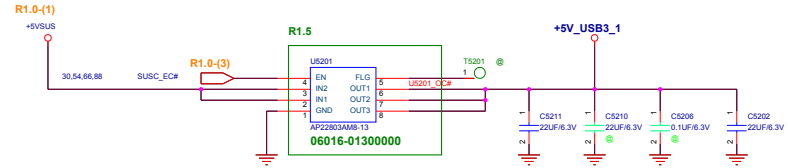
5.6 ALERT# point hardware power-on setting (TBD)

The default value could be set after power up 100ms by different pull-up resistor of ALERT# pin :

PULL-UP RESISTOR		TEMPERATURE (℃)
ALERT	2KΩ	75
	7.5KΩ	90
	10.5KΩ	100
	14KΩ	105
	18.7KΩ	110



USB3.0 Power Switch

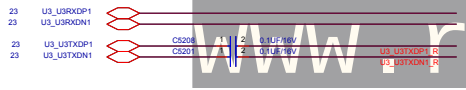


MSOP-8 PWR Switch of New Pool List :
1st : P/N: 06016-01300000 POWER SW. AP22803AM8-13/DIODES MSOP-8.
2nd : P/N: 06G030046024 POWER SW. G547E1P81U/GMT MSOP8.

USB3.0 Signal

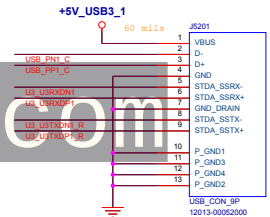
BOM 上09022-00110000

R1.1, Remove EMPASS
R2.0, Remove RN5204 & RN5205 (10G302000004030)



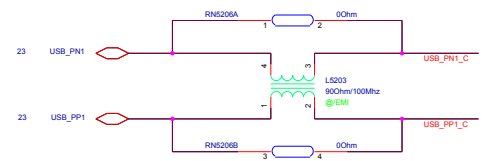
USB3.0 Type A Connector (GEN2_10G)

1st,12013-00052000



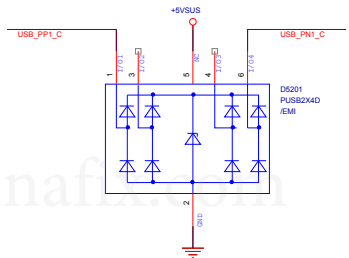
USB 2.0 Signal & Common choke Protection

1st,09G092090100
2nd,09G092090110



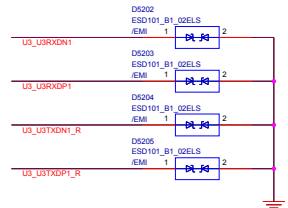
USB2.0 ESD-Protection

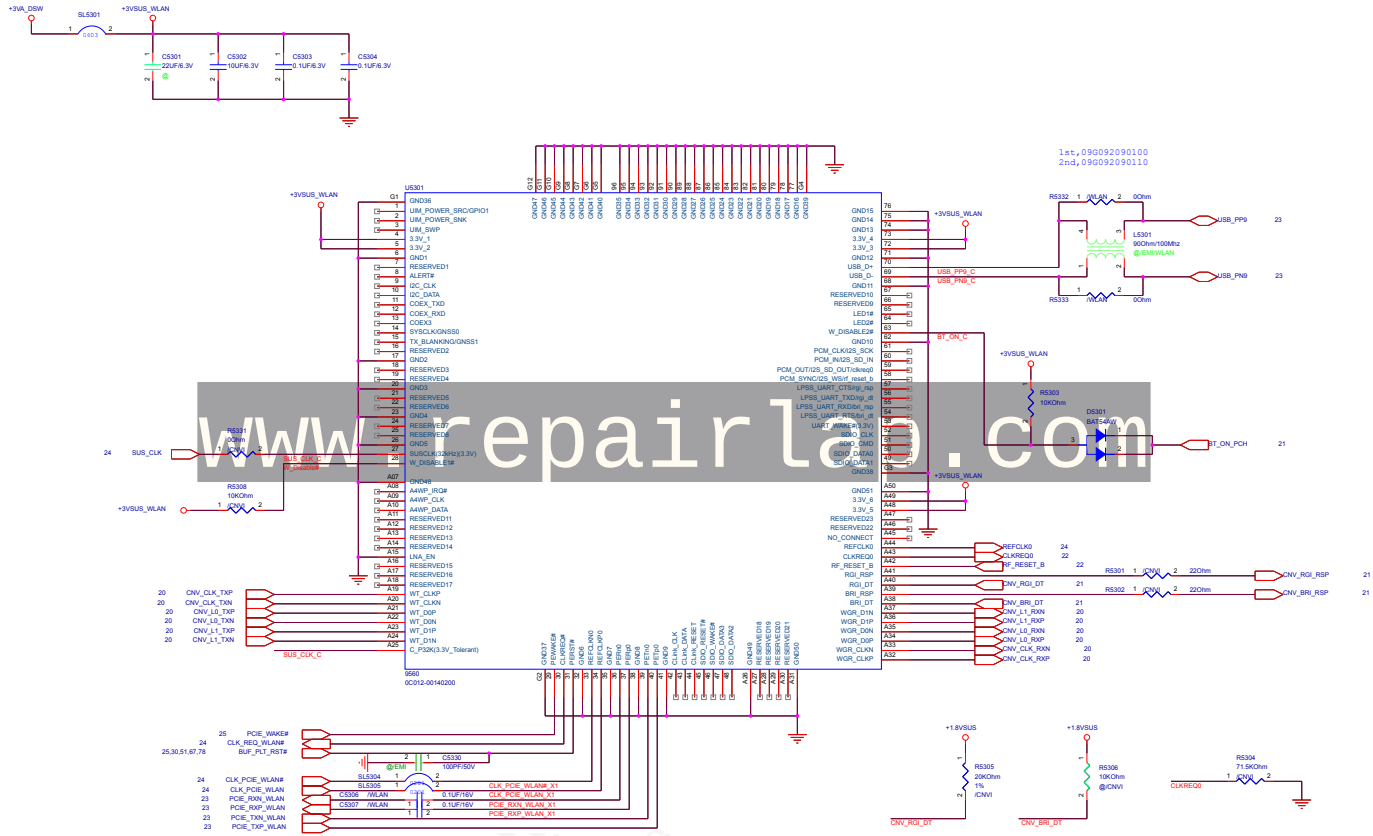
1st,07024-00710000
2nd,07024-00200200



USB3.0 ESD-Protection

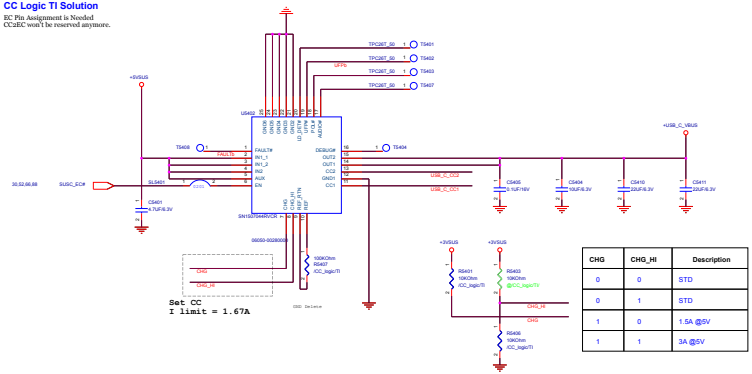
07024-01050000





CC Logic TI Solution

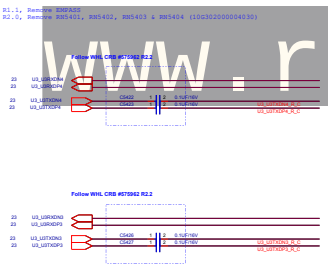
EC Pin Assignment is Needed
CC2:EC won't be reserved anymore.



CHG	CHG_HI	Description
0	0	STD
0	1	STD
1	0	1.5A @5V
1	1	3A @5V

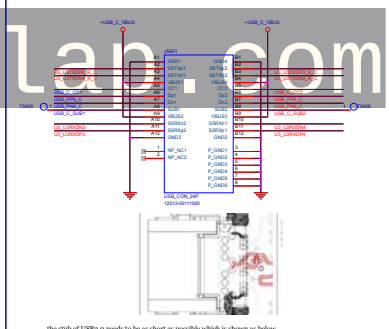
USB3.0 Common choke RF

R1.1, Remove EMPASS
R2.0, Remove RN5401, RN5402, RN5403 & RN5404 (10G3020000040030)



Type-C Connector

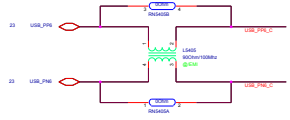
1st,12013-00111000
2nd,12013-00116300
3rd,12013-00119300



the stub of USB2.0 needs to be as short as possible which is shown as below

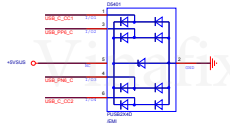
USB 2.0 Common choke EMI-Protection

1st,09009209100
2nd,09009209110



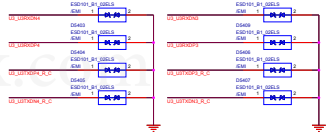
USB 2.0 ESD-Protection

1st,07024-00710000
2nd,07024-00200200

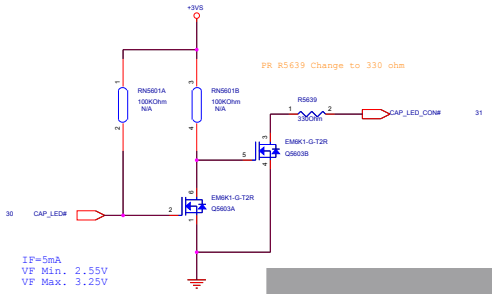


USB3.0 ESD-Protection

07024-01050000

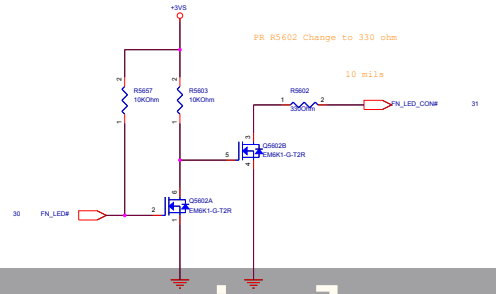


CAPS_LOCK LED (KB)

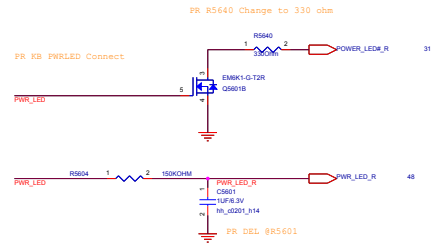


FN LED (KB)

UX391UA FN LED



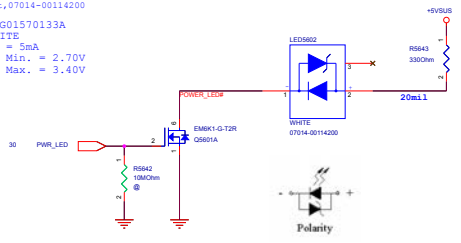
PWR LED (KB)



PWR LED (MB)

1st,07014-00114200

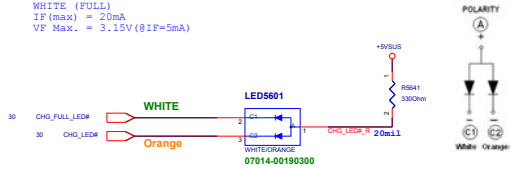
07G01570133A
WHITE
IF = 5mA
VF Min. = 2.70V
VF Max. = 3.40V



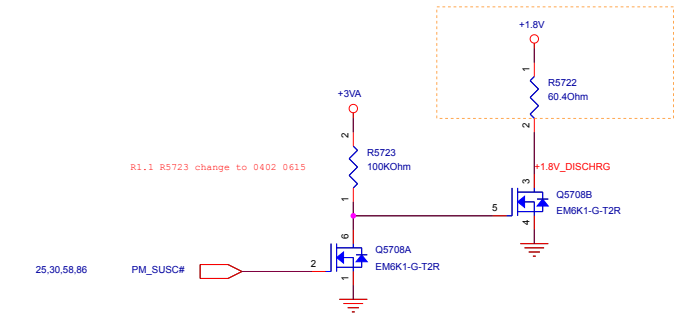
Charger LED (MB)

1st,07014-00190300

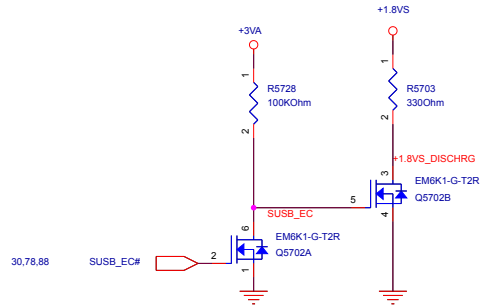
WHITE (FULL)
IF(max) = 20mA
VF Max. = 3.15V(@IF=5mA)

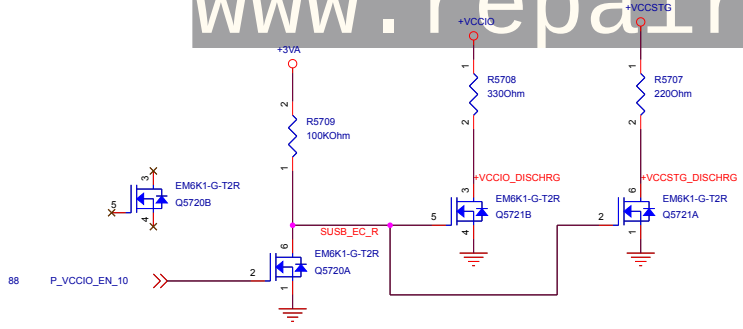


+1.2V Change to +1.8V



VS discharge

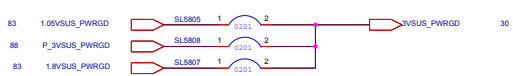




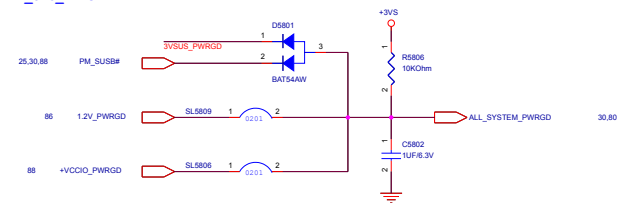
DEL +1.05VSUS Discharge

3VSUS_PWRGD

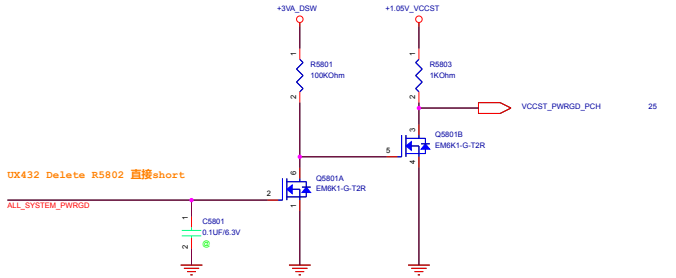
UX432 R1.1 Delete @D5804

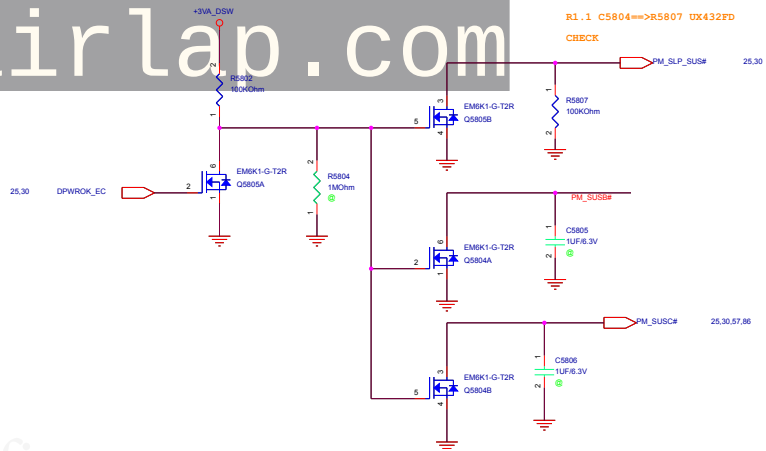


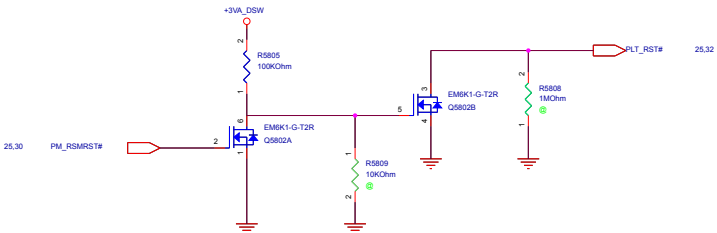
ALL_SYS_PWRGD



VCCST_PWRGD for PCH

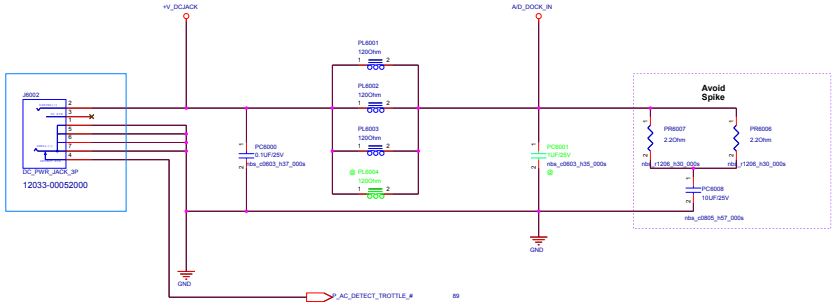






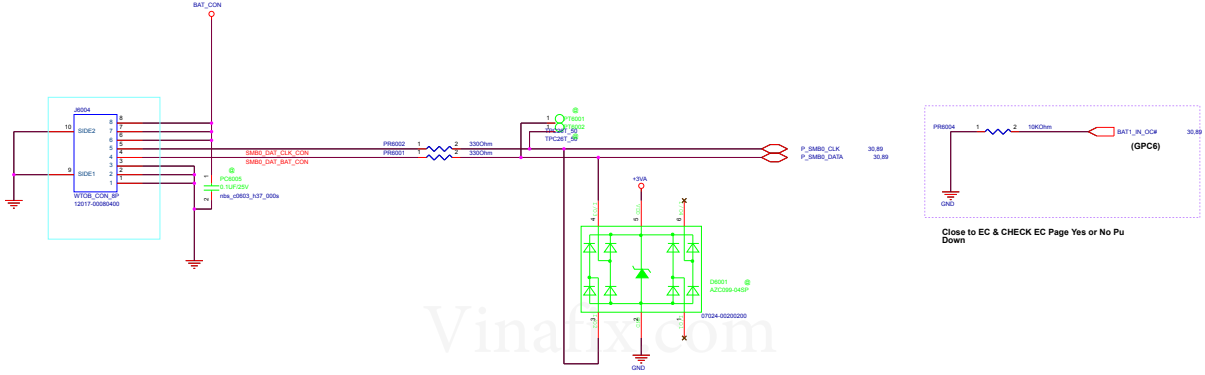
DC Jack

1st,12033-00052000

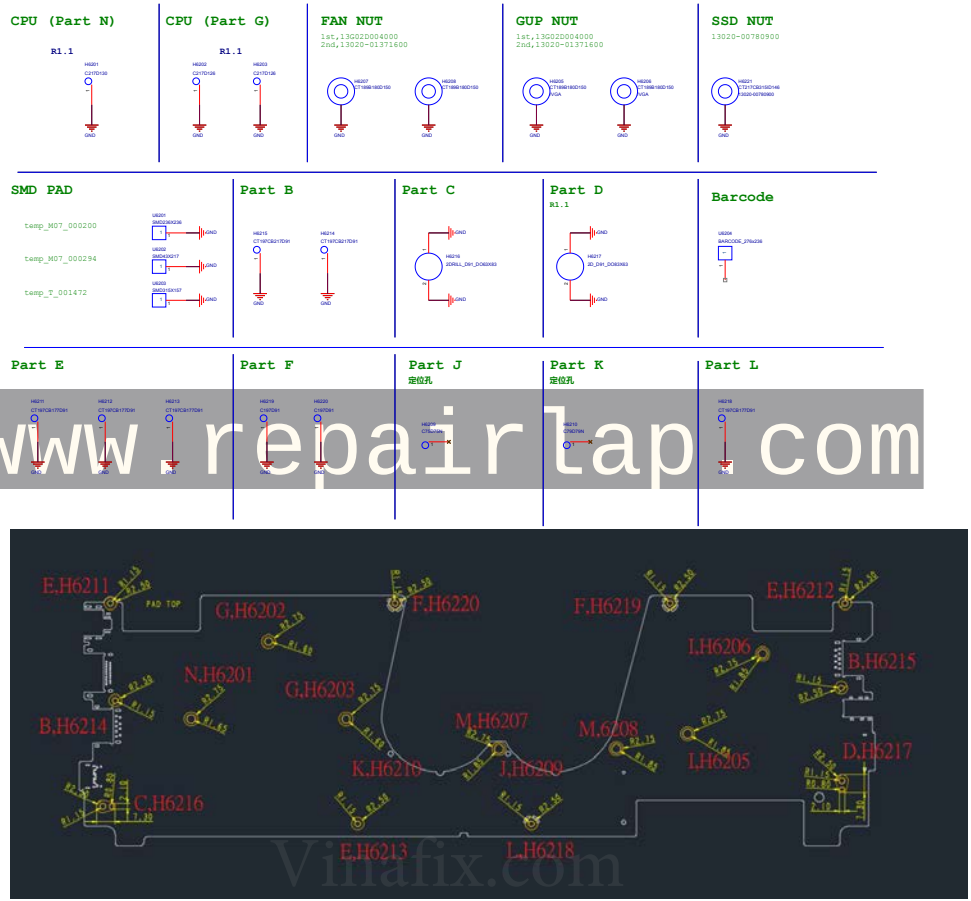


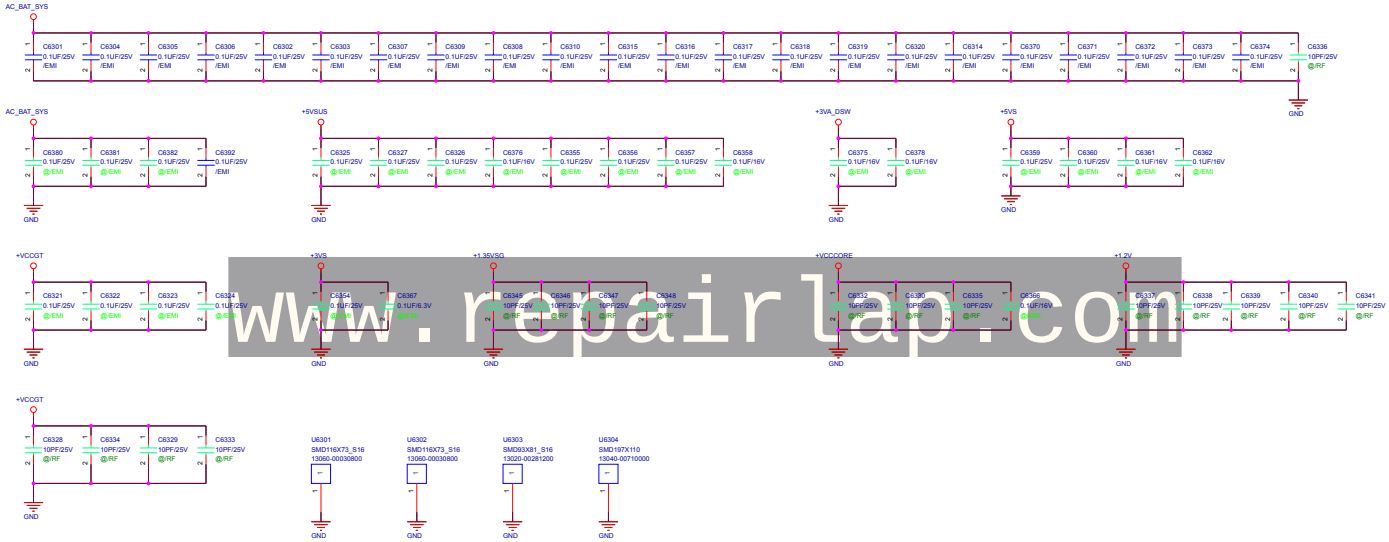
Battery Connector

1st,12017-00080400

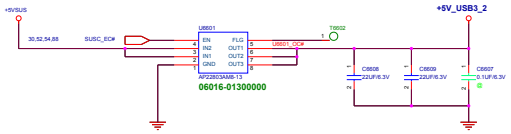


Close to EC & CHECK EC Page Yes or No Pu Down

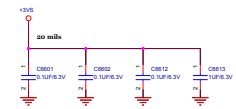

CPU (Part N)
R1.1
CPU (Part G)
R1.1
FAN NUT
1st,13G02D004000
2nd,13020-01371600
GUP NUT
1st,13G02D004000
2nd,13020-01371600
SSD NUT
13020-00780900
SMD PAD
temp_M07_000200
temp_M07_000294
temp_T_001472
Part B
Part C
Part D
R1.1
Barcode
Part E
Part F
Part J
定位孔
Part K
定位孔
Part L
www.repairlap.com
E,H6211
PAD TOP
G,H6202
F,H6220
F,H6219
E,H6212
I,H6206
B,H6215
N,H6201
G,H6203
B,H6214
M,H6207
M,6208
D,H6217
K,H6210
J,H6209
I,H6205
C,H6216
E,H6213
L,H6218
Vinafix.com



USB3.0 Power Switch

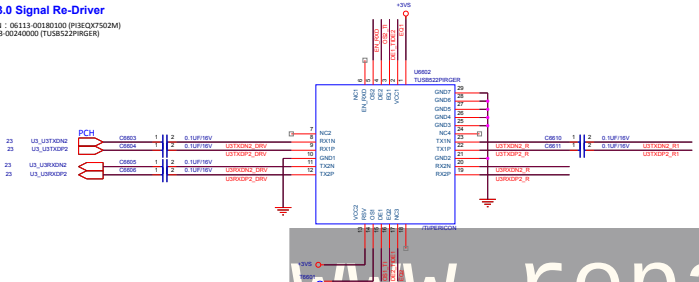


USB3.0 Power Re-Driver



USB3.0 Signal Re-Driver

PERICON : 06113-00180100 (PI3EQX7502M)
TI: 06113-00240000 (TUSB522PIRGER)



USB3.0 Signal

BOM 上09022-00110000

R2.0, Remove EMPASS L6602 & L6603
R2.0, Remove RN5401, RN5402, RN5403 & RN5404 (10G302000004030)

< EQ / DE > and < Other Pin Funcon >

< Fine tune table for PERICON (One Port Gen1) >

(Opon)

Equalizer seng

EQ_A/B	@ 2.5GHz
Open	3 dB (default)
0	6 dB
1	9 dB

Output De-emphasis seng

DE_A/B	De-emphasis
Open	0 dB (default)
0	-3.5 dB
1	-6 dB

Output De-emphasis seng

USB3R_P10/21 EN_x#	USB3R_P5 RxD_EN	Input R	Output R
1	X	Hi-Z	Hi-Z
0	1	500hm / 60K to GND	500hm / 2KOhm
0	0	50 Ohm	50 Ohm

Note :
NC Pin : Pin 4, 6, 7, 14, 15, 18, 24
RxD_EN has internal pull-up, so if it is NC, RxD_EN = 1.

< Fine tune table for TI (One Port Gen1) >

(Opon)

Equalizer seng

EQ_1/2	@ 2.5GHz
0	3 dB
Open	6 dB (default)
1	9 dB

Output De-emphasis seng

DE_1/2	De-emphasis(OS=H)	De-emphasis(OS=L)
0	0 dB	-2.6dB
Open	-3.5 dB (default)	-5.9 dB (default)
1	-6.2 dB	-8.3 dB

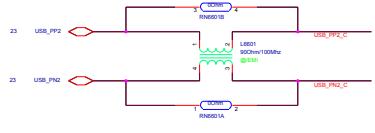
Output Swing seng

OS_1/2	Output Swing
0	0.9 Vpp
Open	0.9 Vpp
1	1.1 Vpp

Note :
NC Pin : Pin 6, 7, 18, 24
RxD_EN has internal pull-down, so if it need to be pull-up by VCC.

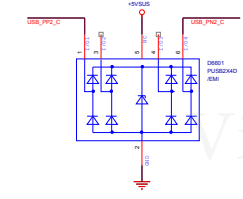
USB 2.0 Signal & Common choke Protection

1st,09G092090100
2nd,09G092090110



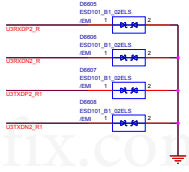
USB2.0 ESD-Protection

1st,07024-00710000
2nd,07024-00200200



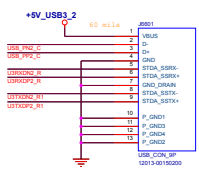
USB3.0 ESD-Protection

07024-01050000



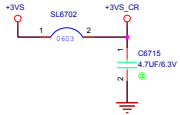
USB3.0 Type A Connector (GEN1_5G)

1st,12013-00150200



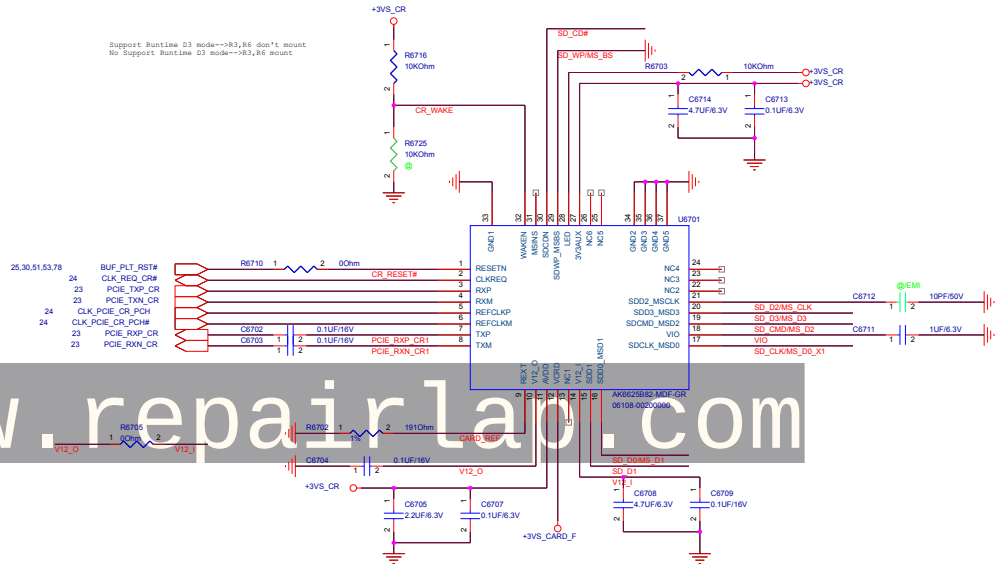
Power Source (MAX 500mA)

Power Trace:
+3VS 40 mils source
+3VS_CR 40 mils
+3VS_CARD_F 30 mils
+3VS_CARD 30 mils

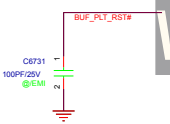


Card Reader IC_AK6625

1st,06108-00200000

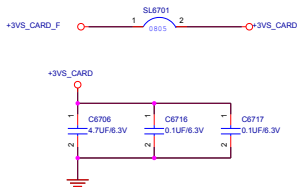


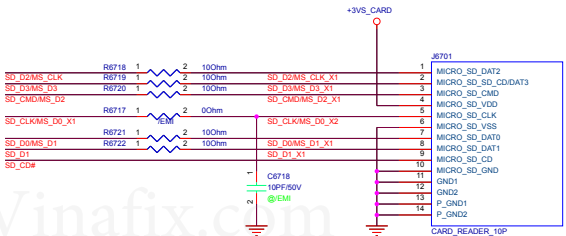
EMI

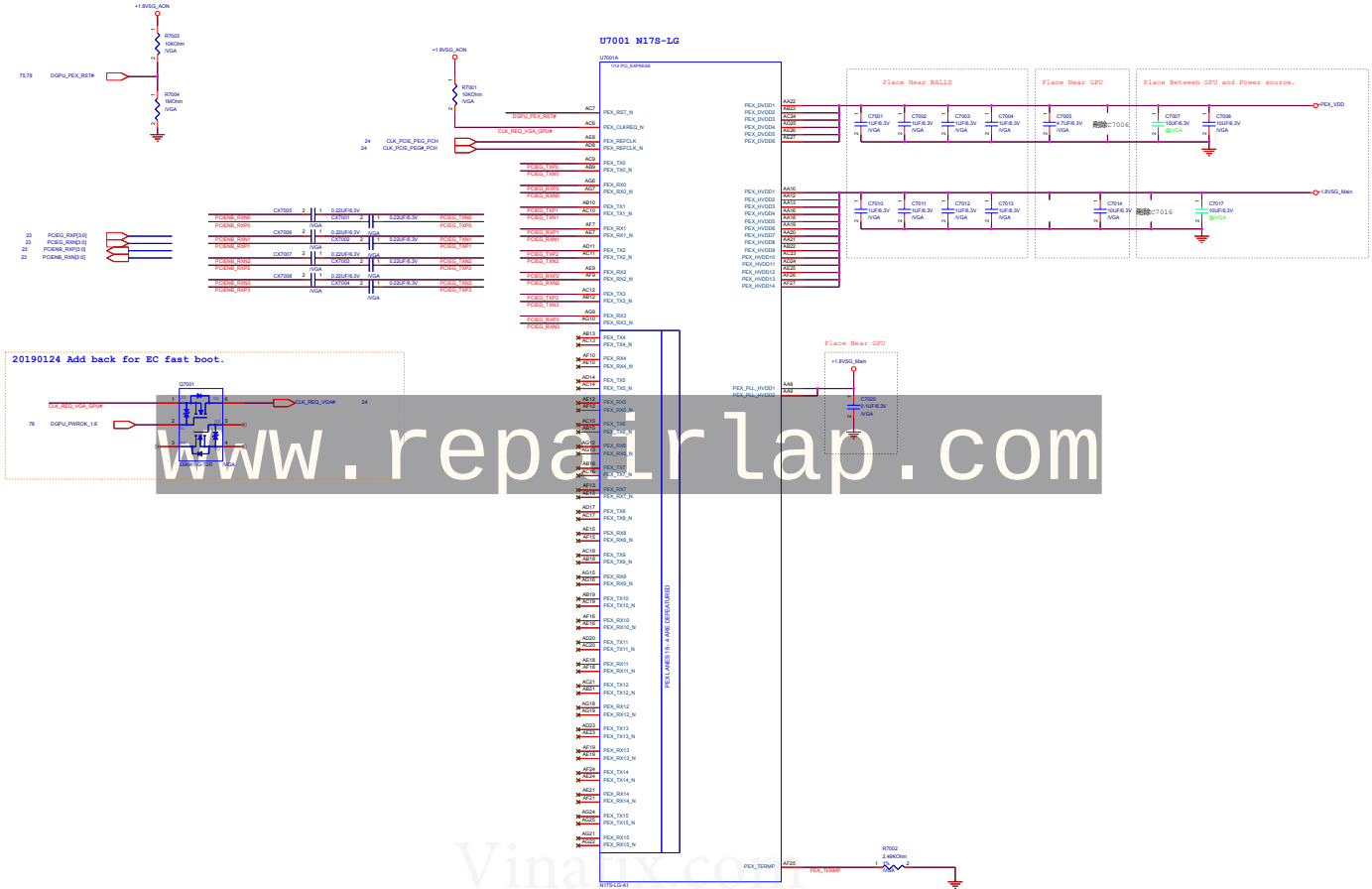


Micro SD Connector

1st,12023-00100100
2nd,12023-00018300







GPU MEMORY INTERFACE

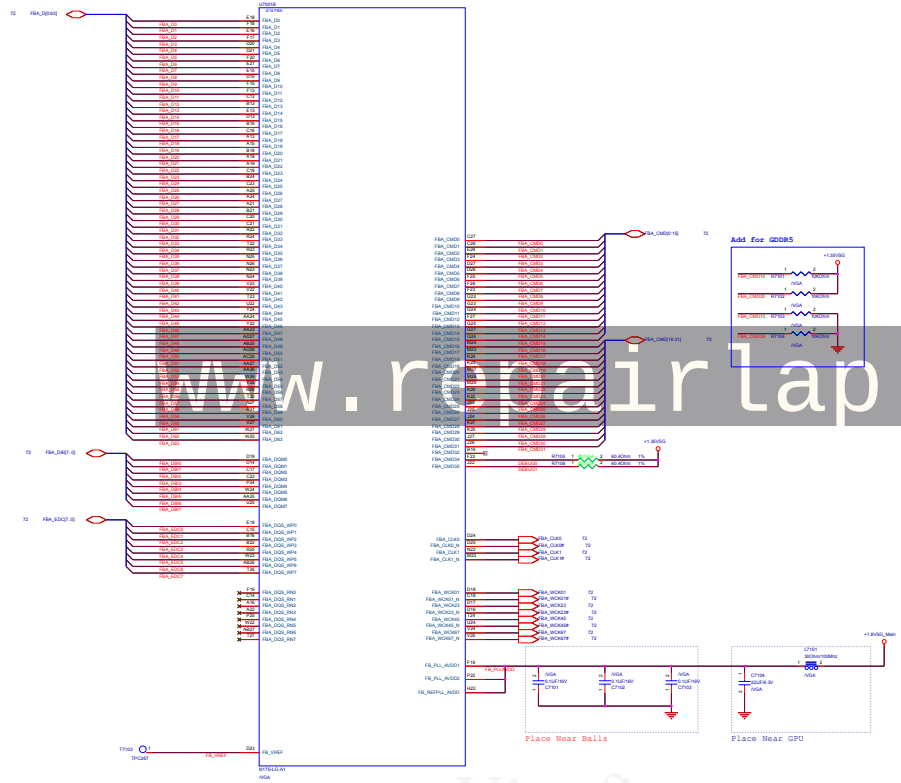


Table 9.5 GDDR5 Command Mapping (GB2C-64 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	ABI*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

UX334 GPU memory clock change to 3GHz

Samsung, GDDR5, 03008-00050000
Micron, GDDR5, 03008-00050400

Table 9.5 GDDR5 Command Mapping (GB2C-64 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	ABI*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

MF=0 non-Mirror

MF=0 non-Mirror

Power Button
(ER or PR板移植)

For VRAM — Place Under DRAM U7201

For VRAM — Place Near DRAM U7201

For GPU — Place Under GPU

Place Under DRAM U7202

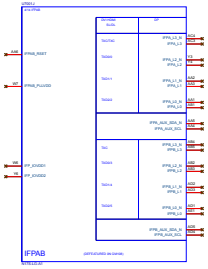
Place Near DRAM U7202

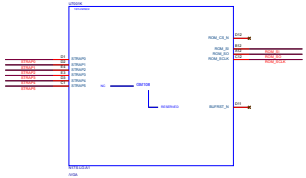
Place Near GPU

Ensure at least 2 GND vias and 2 power vias for each capacitor

GPU

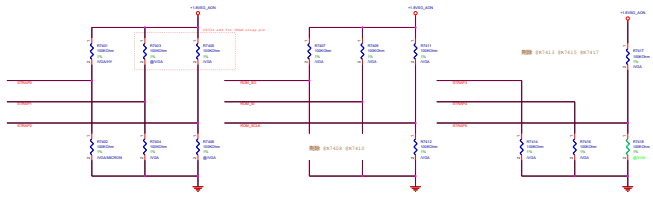
Byte0
Byte1
Data Byte2
Byte3
ADDR CMD
MF





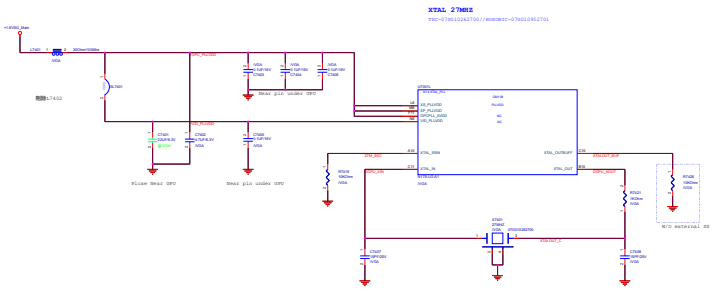
Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR1_ EXPOSED	SOR2_ EXPOSED	SOR1_ EXPOSED	SOR0_ EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
0	H	H	M	disabled	disabled	disabled	disabled

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
H	L	L	0	1	0	0

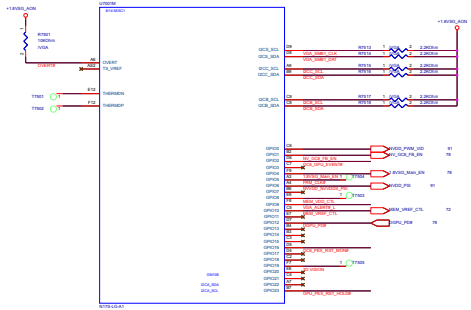


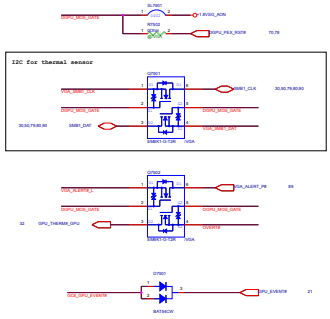
Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)

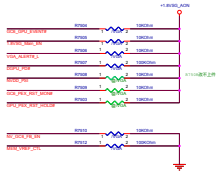
Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V	Micron	MT51J256M32HF-80:B	B-die	0x4	8 Gbps	N/A	N/A	Substitution allowed with waiver[1]
			Hynix	H5GC8H24AJR-R2C	A-die	0x5	8 Gbps	N/A	N/A	Substitution allowed with waiver[1]



- **SMB_ALT_ADDR Enable**: This strap function allows an alternate SMBus address to be configured, so that graphics circuits with multiple GPUs can have separate SMBus connections for each GPU. In dual GPU configurations, use of the alternate address on one GPU (by setting this function to '1') avoids conflicts between the two GPUs on an SMBUS port. The "SMB_ALT_ADDR disabled" setting ('0') is correct for single-GPU graphics circuits. (see Section 13.2.2.1 for the SMBus address.)
- **DEVID_SEL**: NVIDIA defines an original and a re-brand Device ID on a per-GPU basis. This Device ID Select strap function allows selection between the original PCIe Device ID defined for the GPU (via a function setting of '0'), and the alternate "re-brand" Device ID defined for the GPU (via a function setting of '1').
- **PCIE_CFG**: This function sets electrical characteristics of PCIe lanes, in particular signal amplitude (swing). A setting of '0' selects normal (full) signal swing. N17x graphics circuits should strap for this setting. (A setting of '1' designates reduced signal amplitude, available if special concerns require. Consult NVIDIA for guidance.)
- **VGA_DEVICE**: This strap function is used to report the graphics circuit either as a 3D device (class code 302, designated by a setting of '0' for this strap) or as a VGA device (class code 300, designated by a setting of '1') to the host system. The 3D Device (class code 302, strap="0") setting is correct for most MS-Hybrid notebook GeForce graphics circuits.







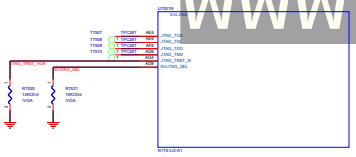
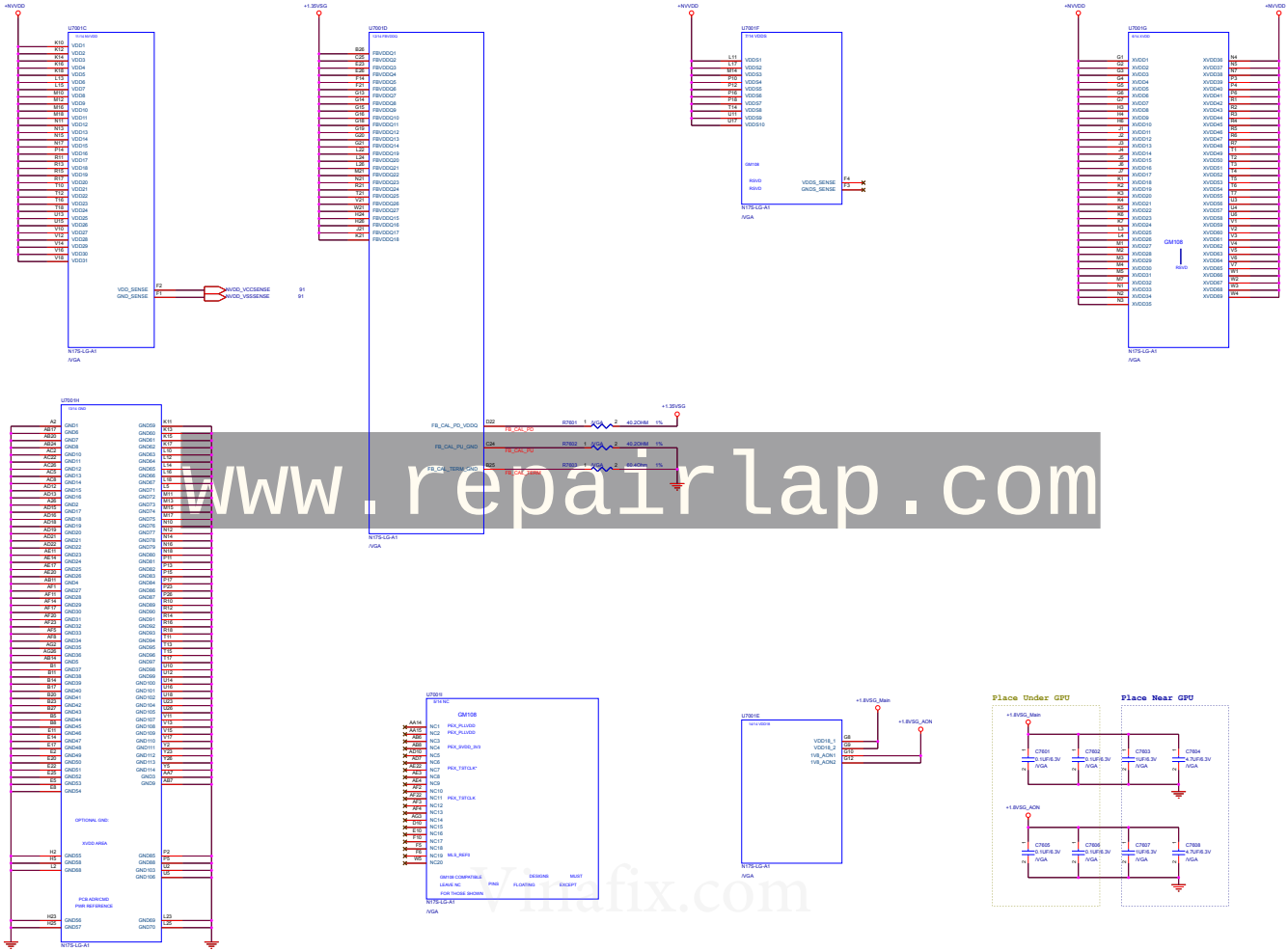


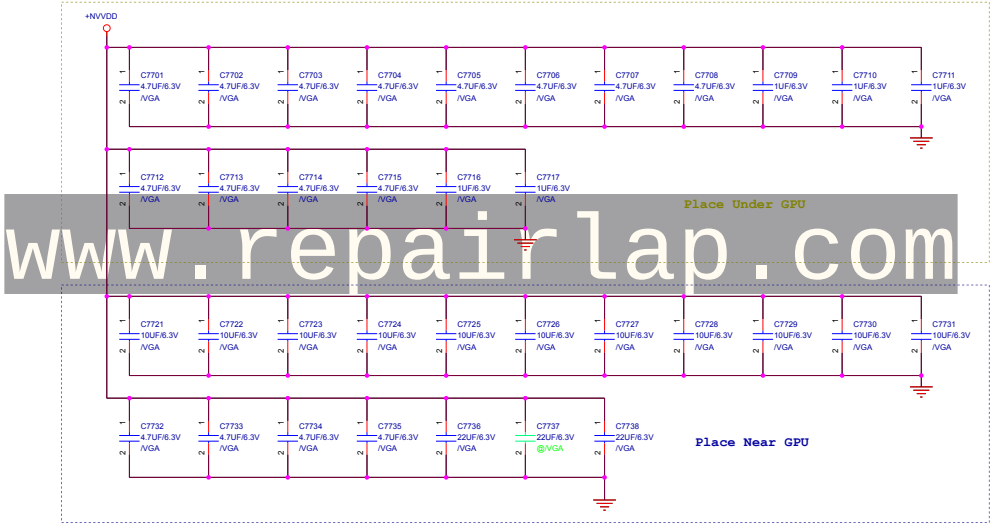
Table 14.1 GPIO Descriptions for GB2C-64 Packages

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	HVVDD_PWM	O	PWM Output to control HVVDD	0 to1V8 PWM output
GPIO1	GC6M: GC6_FB_EN	O	FB Enable for GC6 2.1	Open Source 10 kΩ pull-down
GPIO2	GC6M: GPU_EVENT*/ WAKE*	I	GPU wake signal for GC6 2.1	10 kΩ pull-up to 1V8_AON, unless driven actively.
GPIO3	HVVDD5_PWM	I/O	PWM output to control the HVVDD5 power supply	0 to 1V8 output
GPIO4	GC6M: 1V8_MAIN_EN	O	GPU power sequencing for GC6 2.1	Open Drain 10 kΩ pull-up to 1V8_AON
GPIO5	FRM_LCK*	I	Active low Frame Lock	Open Drain 10 kΩ pull-up to 1V8_AON
GPIO6	HVVDD_PSI*/ HVVDD5_PSI*	O	Phase Shedding (see Section 14.3.3)	10 kΩ pull-up to 1V8_AON to enable multiple phases
GPIO7	LCD_BL_PWM	O	Panel Backlight enable	100 kΩ pull-down
GPIO8	MEM_VDD_CTL	O	Memory voltage control	Pull-up/pull-down to set the FBVDD/Q power-on voltage
GPIO9	THERM_ALERT*	I/O	Active Low Thermal Alert	Open Drain 10 kΩ pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down

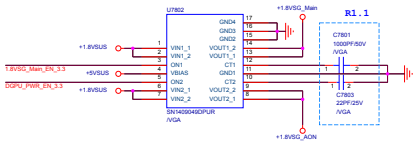
GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO11	LCD_VDD_ QuadricPower_Brake*	O	Panel Power enable	100 kΩ pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100 kΩ pull-up to 1V8_AON
GPIO13	LCD_BLEN	O	LCD Panel Backlight Enable	Panel Backlight Enable
GPIO14	HPD_IFPA*	I	Hot Plug Detect for IFPA	Inverted Input. See Figure 14.5
GPIO15	HPD_IFPB*	I	Hot Plug Detect for IFPB	Inverted Input. See Figure 14.5
GPIO16	GC6M: SYS_PEX_RST_MON*	I	System side PCIe reset monitor	10 kΩ pull-up to 1V8_AON unless actively driven
GPIO17	UNUSED	I/O		
GPIO18	UNUSED	I/O		
GPIO19	3D Vision	O	3D Vision L/R Signal	100 kΩ pull-down
GPIO21	MEM_VDD_CTL	O	Frame Buffer VDD select	Open Drain; Pull-up/pull-down to set the FBVDD/Q power-on voltage at boot up
GPIO22	UNUSED	I/O		
GPIO23	GC6M: GPU_PEX_RST_HOLD*	O	GPU PCIe self-reset control	Open Drain 10 kΩ pull-up to gated 3V3



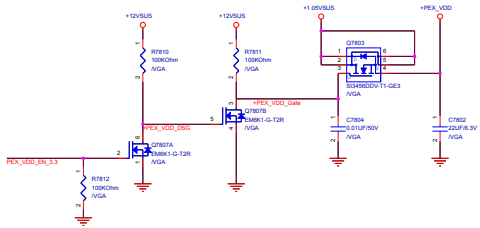
NVVDD POWER AND DECOUPLING



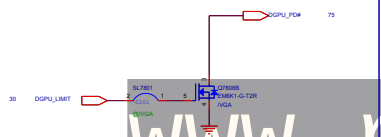
+1.8VSG_AON
+1.8VSG_Main



+PEX_VDD

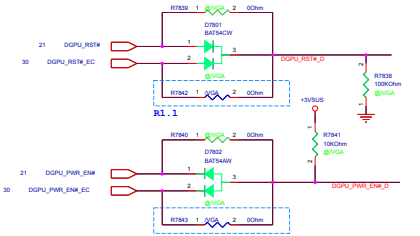


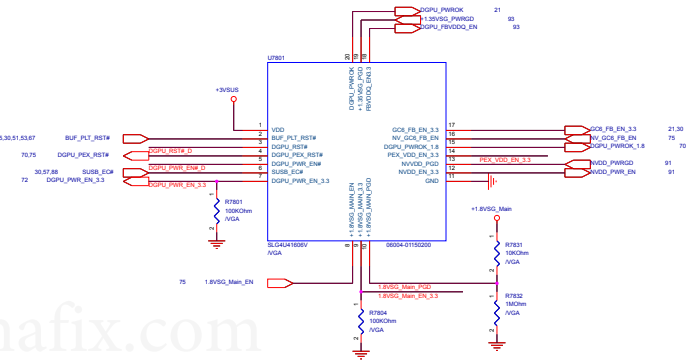
DGPU_PD#

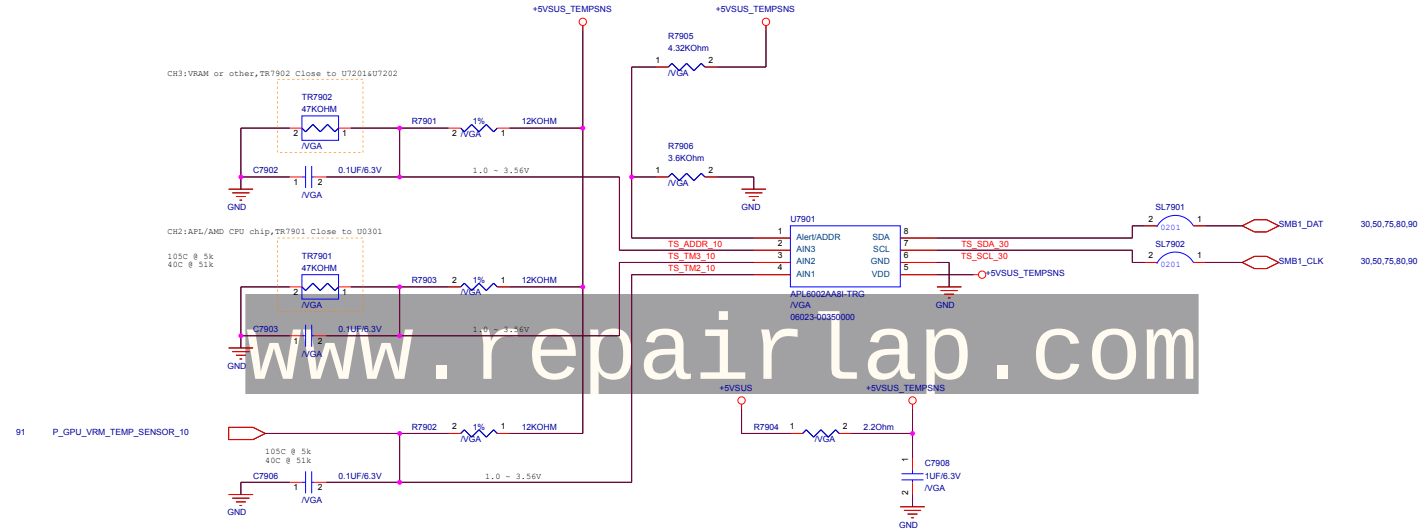


Discharge

For Post time

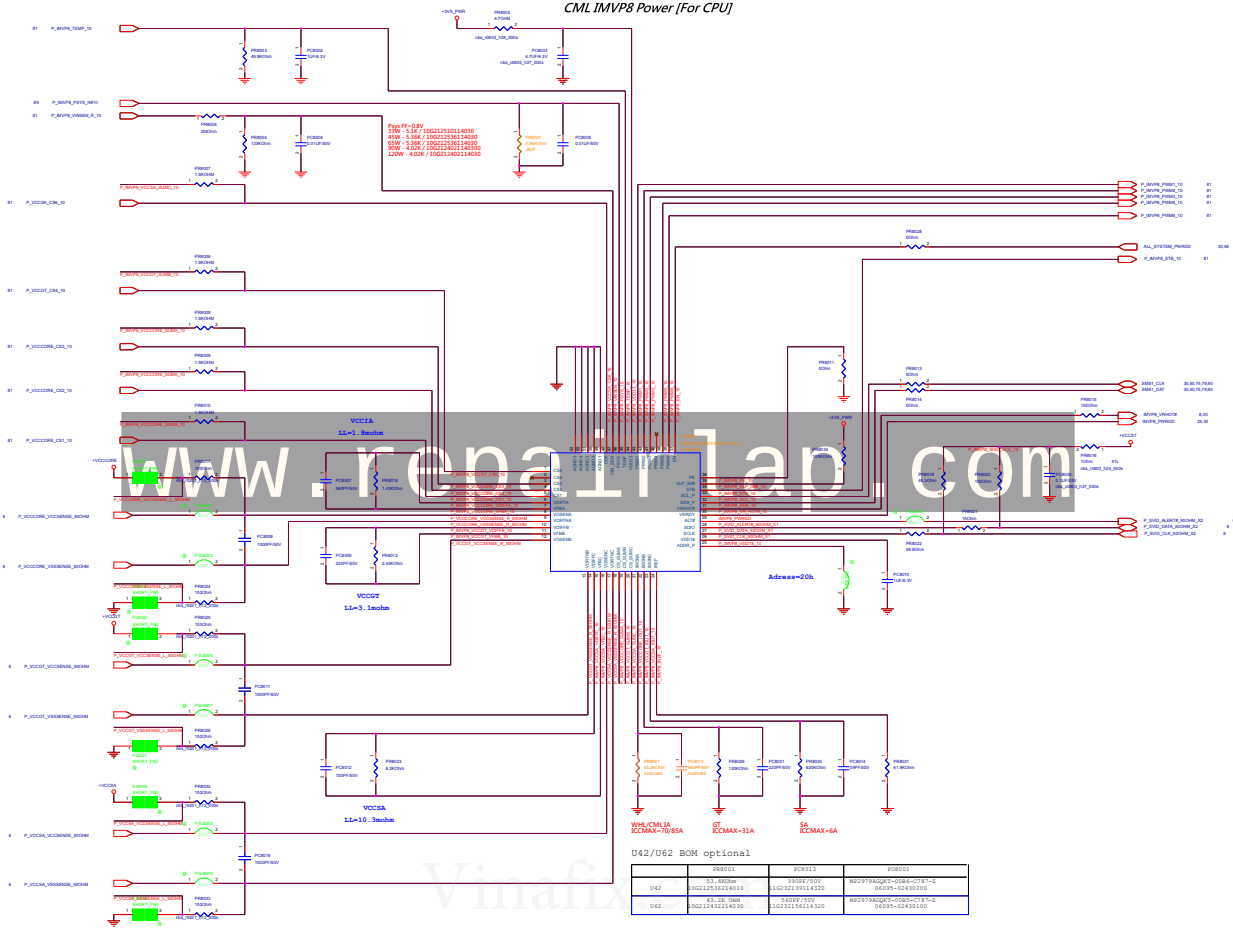






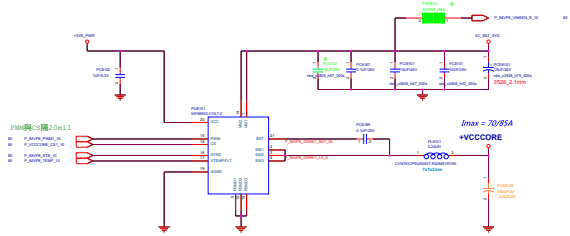
Address Selection Table

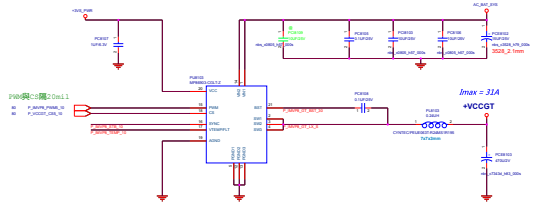
Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
R7905	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
R7906	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

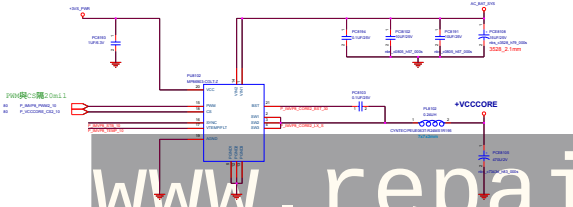


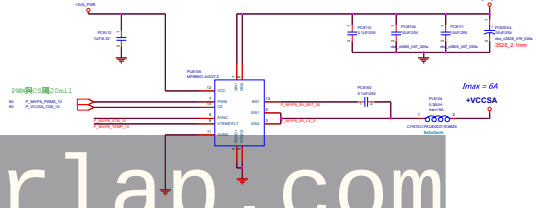
U42/U62 BOM optional

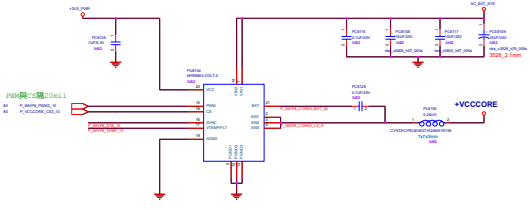
	PR8001	PC8013	PC8031
U42	53.6R2km 10G21253614010	330PF/50V 10G2331351143 20	MP2979AGQKT-0068-C787-Z 06095-02430200
U42	63.2K 0604 10G21243214030	560PF/50V 10G2321561143 20	MP2979AGQKT-0065-C787-Z 06095-02430100

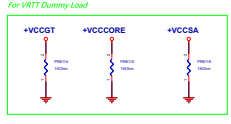


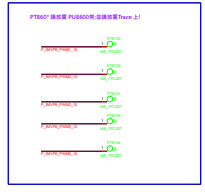


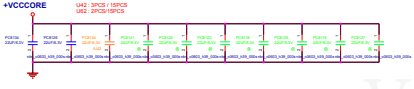


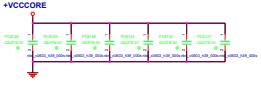








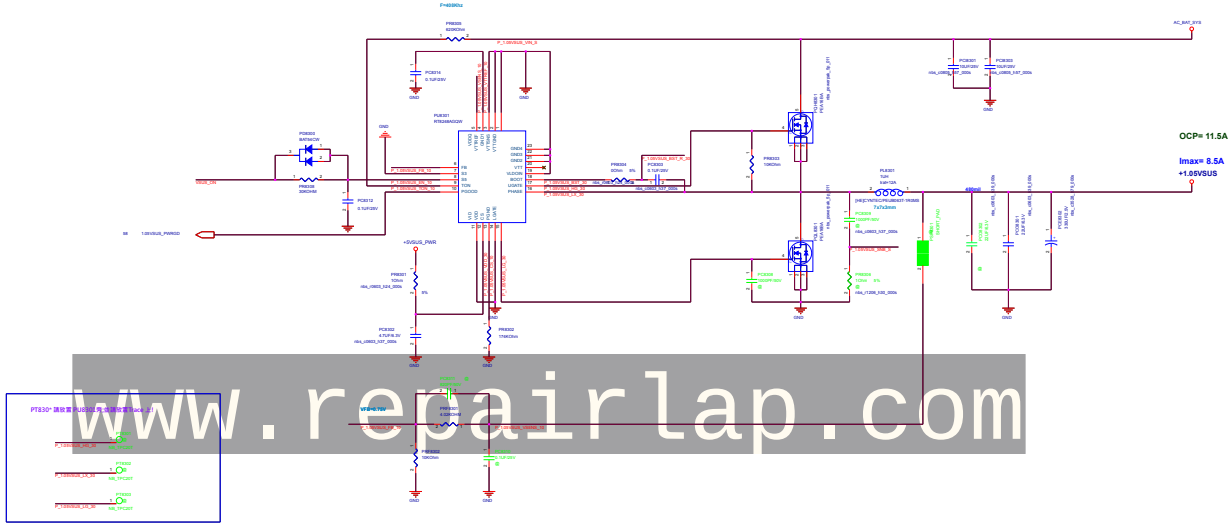




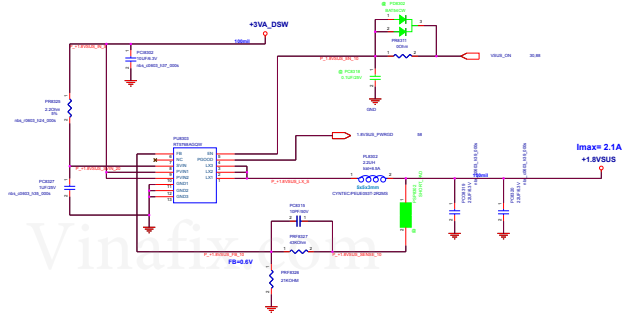
U42/U62 BOM optional

	PCB5104	PCB124
U42	470UF/2V 11020-00356030	220UF/4V 11023322A253220
U62	220UF/2V 11020-00355150	@

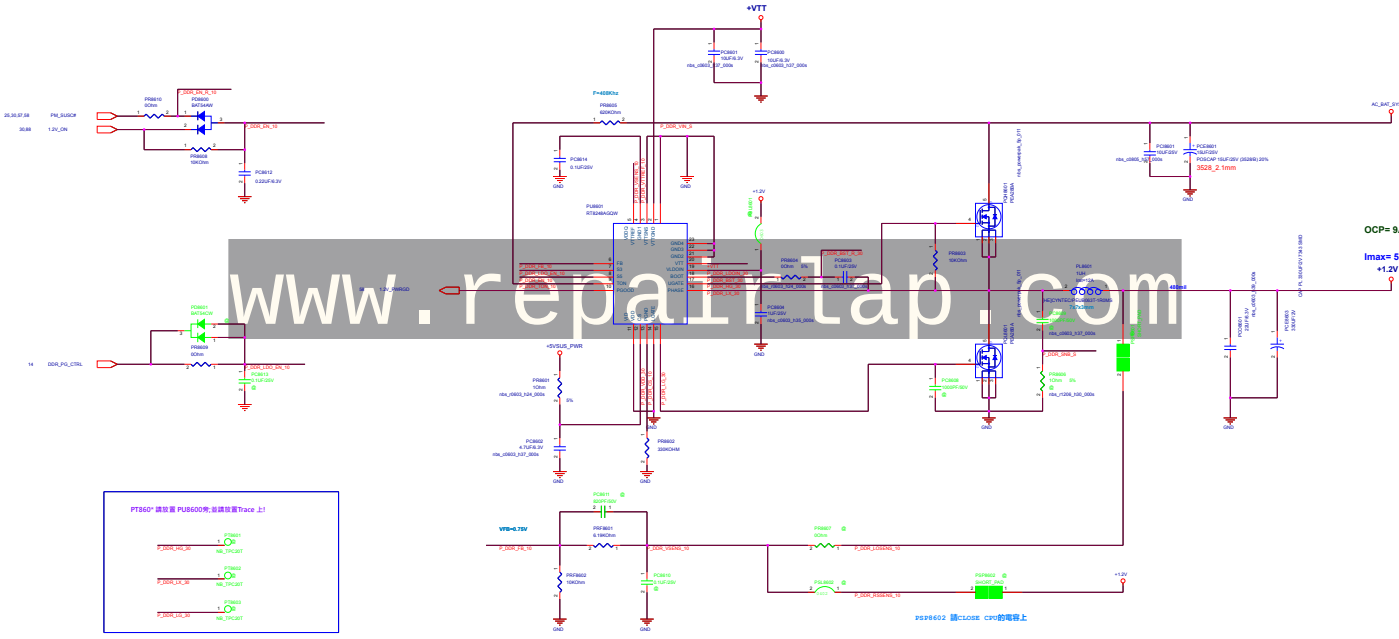
+1.05VSUS [For PCH]



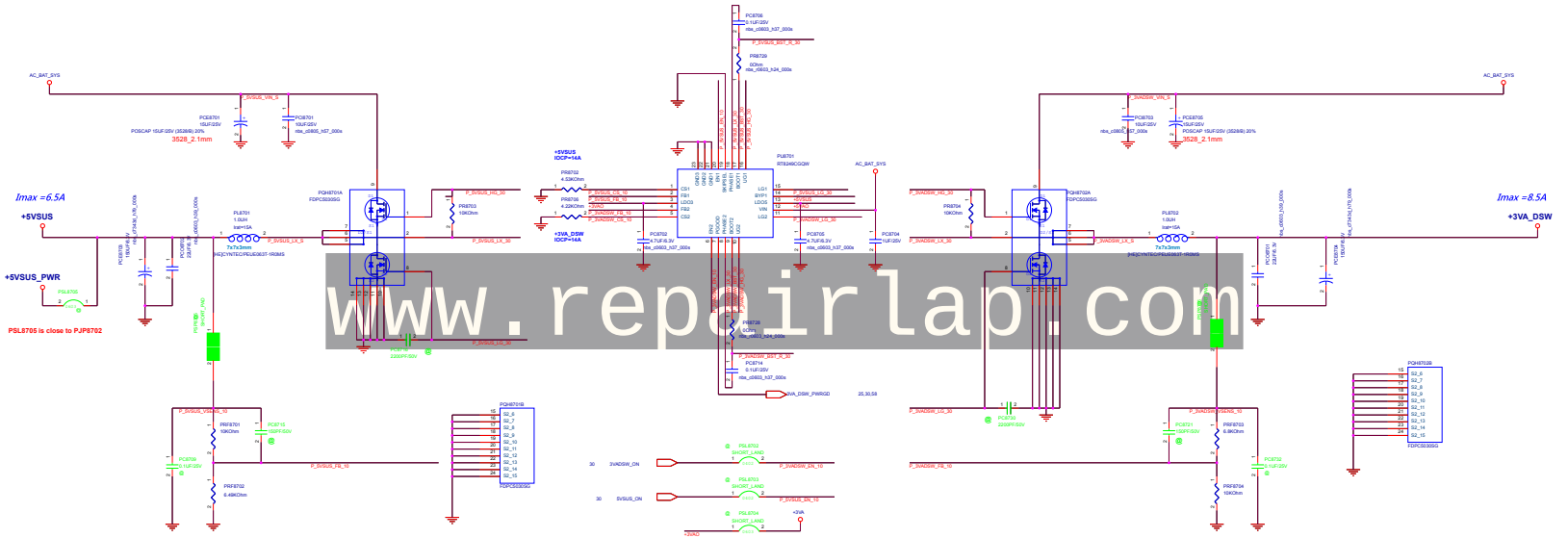
+1.8VSUS [For PCH]



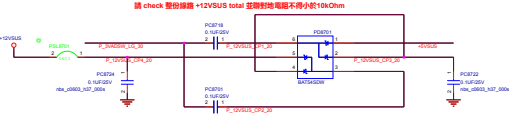
+1.2V / +VTT [For Memory]



+3VA_DSW / +5VSUS [System Power]



請 check 整份線路 +12VSUS total 並聯對地電阻不得小於10kOhm



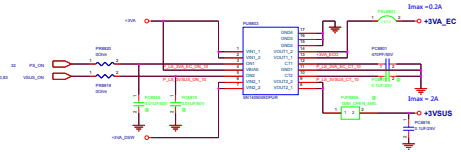
Adaptor Mode (IMVP8)

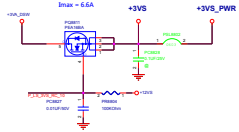
	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-	0	-	0
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0
SUSC_EC#	1	-	1	-	0	-	0
SUSB_EC#	1	-	0	-	0	-	0

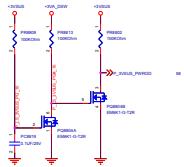
Battery Mode (IMVP8)

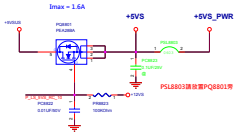
	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	1	1	0	0	1
3VADSW_ON	1	-	1	1	0	0	0
3VSUS_ON	1	-	1	0	0	0	0
5VSUS_ON	1	-	1	1	0	0	1
1.35V_ON	1	-	1	1	0	0	0
SUSC_EC#	1	-	1	0	0	0	0
SUSB_EC#	1	-	0	0	0	0	0

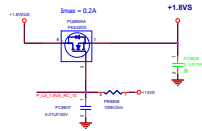
PT870* 請放置 PU8701旁;並請放置Trace 上!

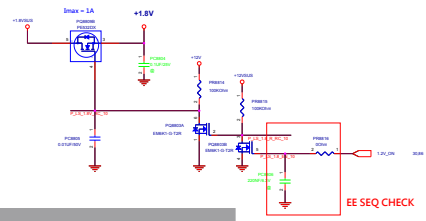


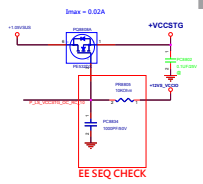


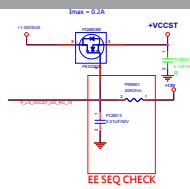


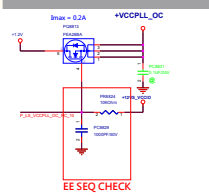


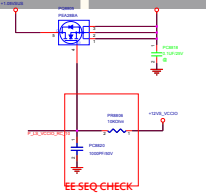


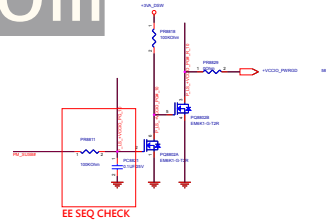


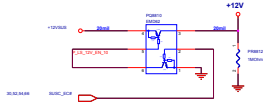


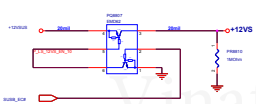


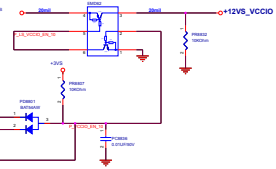


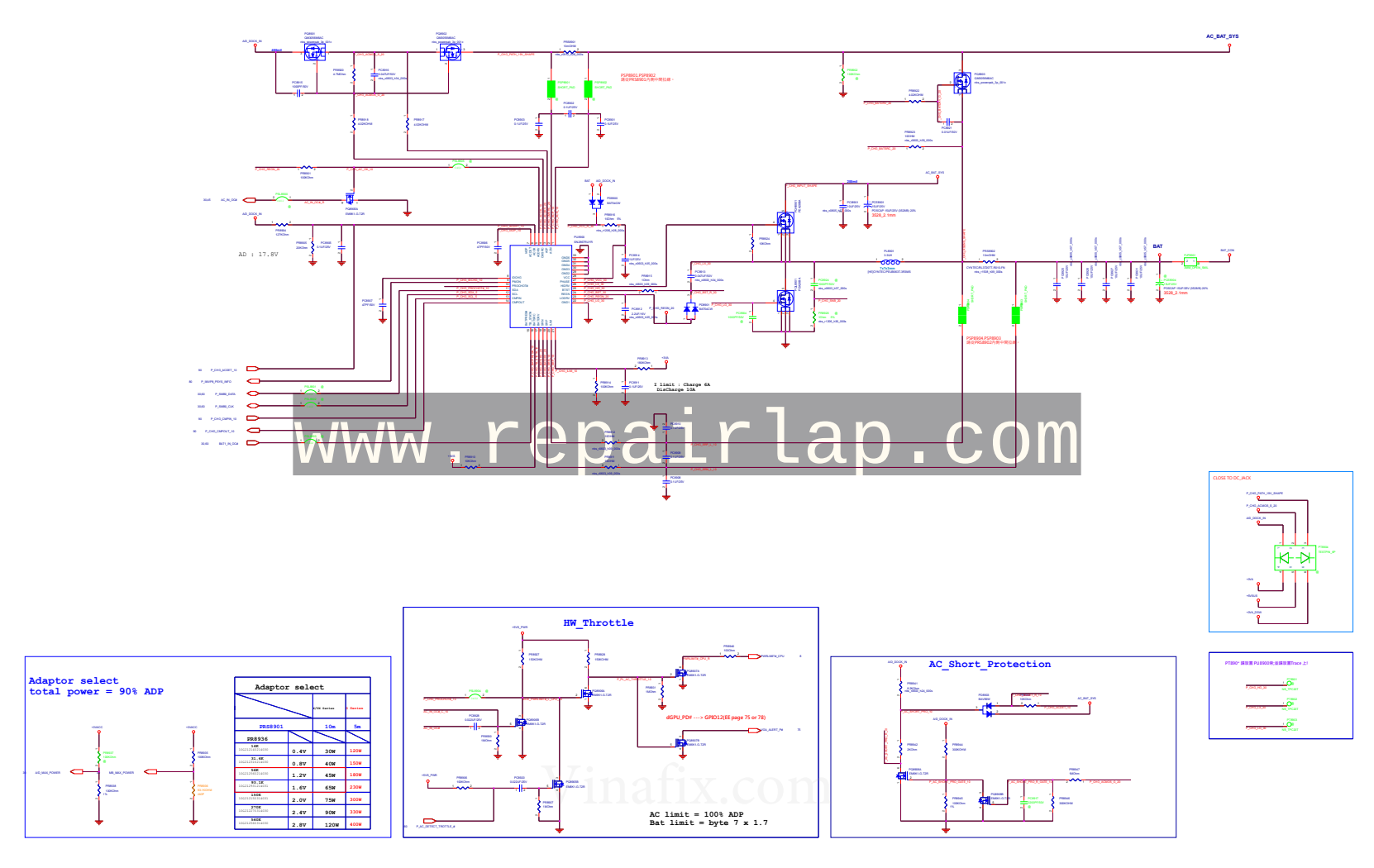










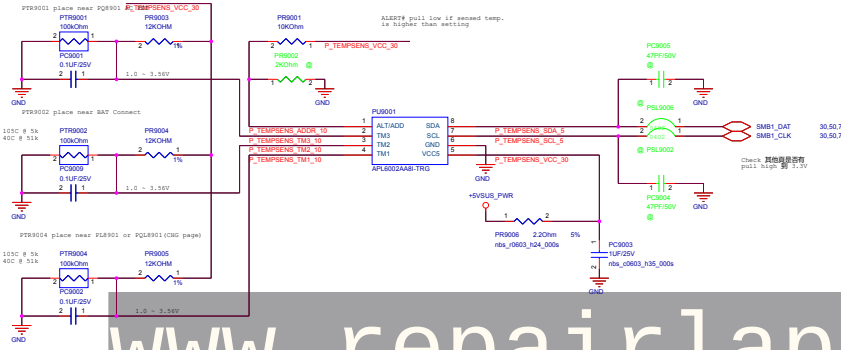


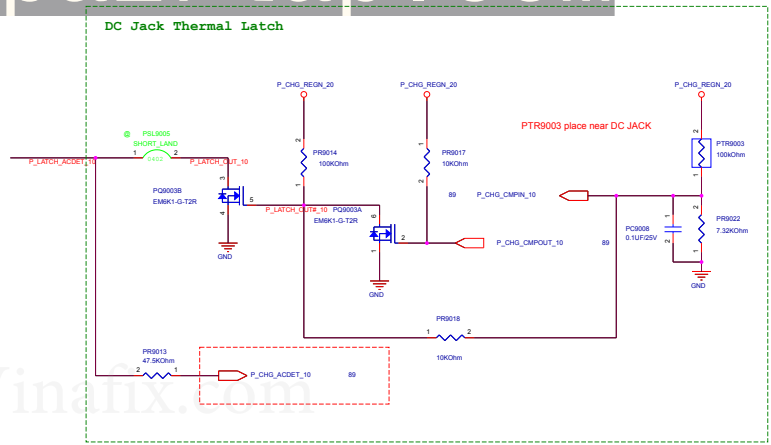
Address Selection Table

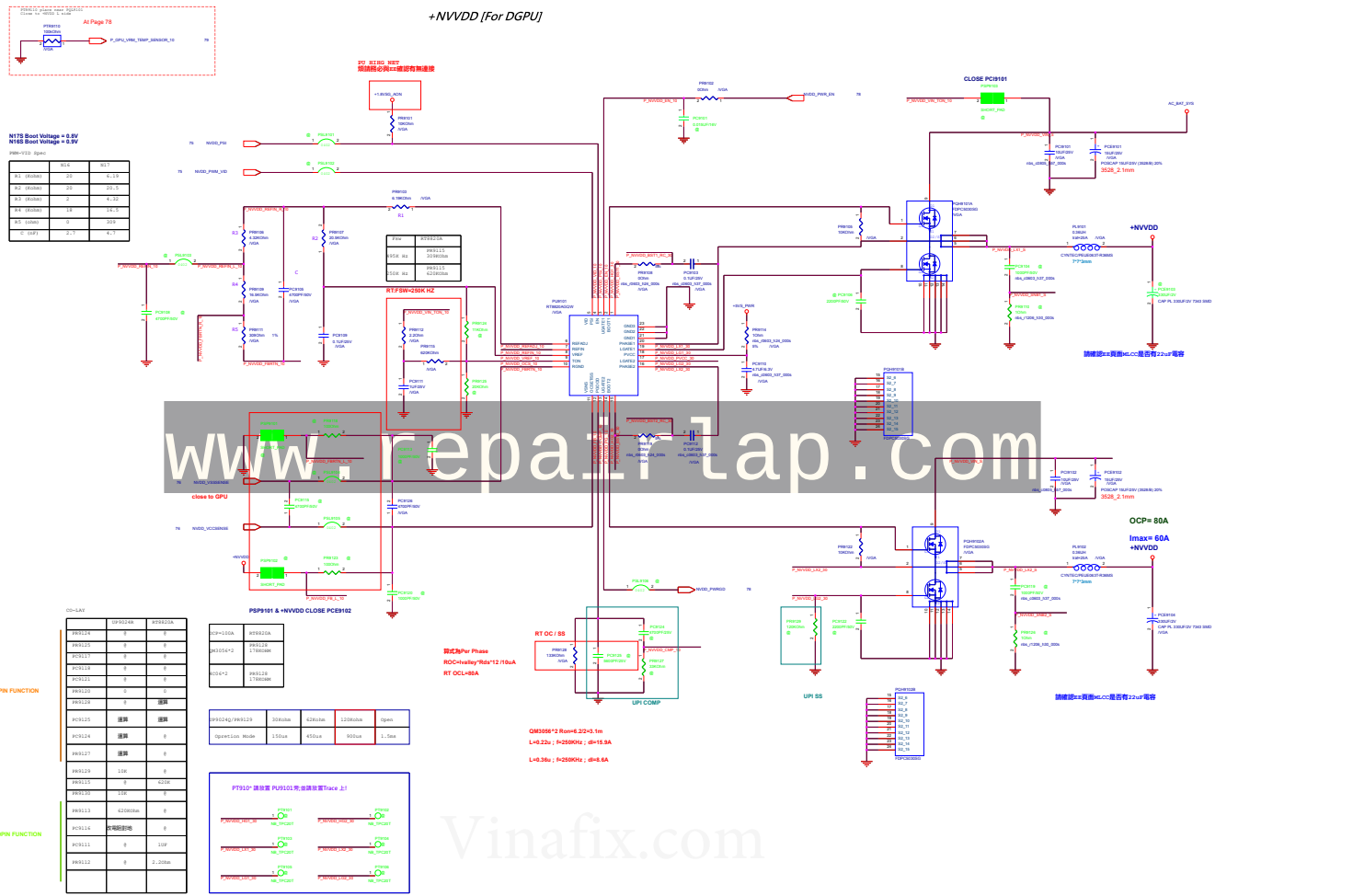
Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR9001	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR9002	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

Register Address

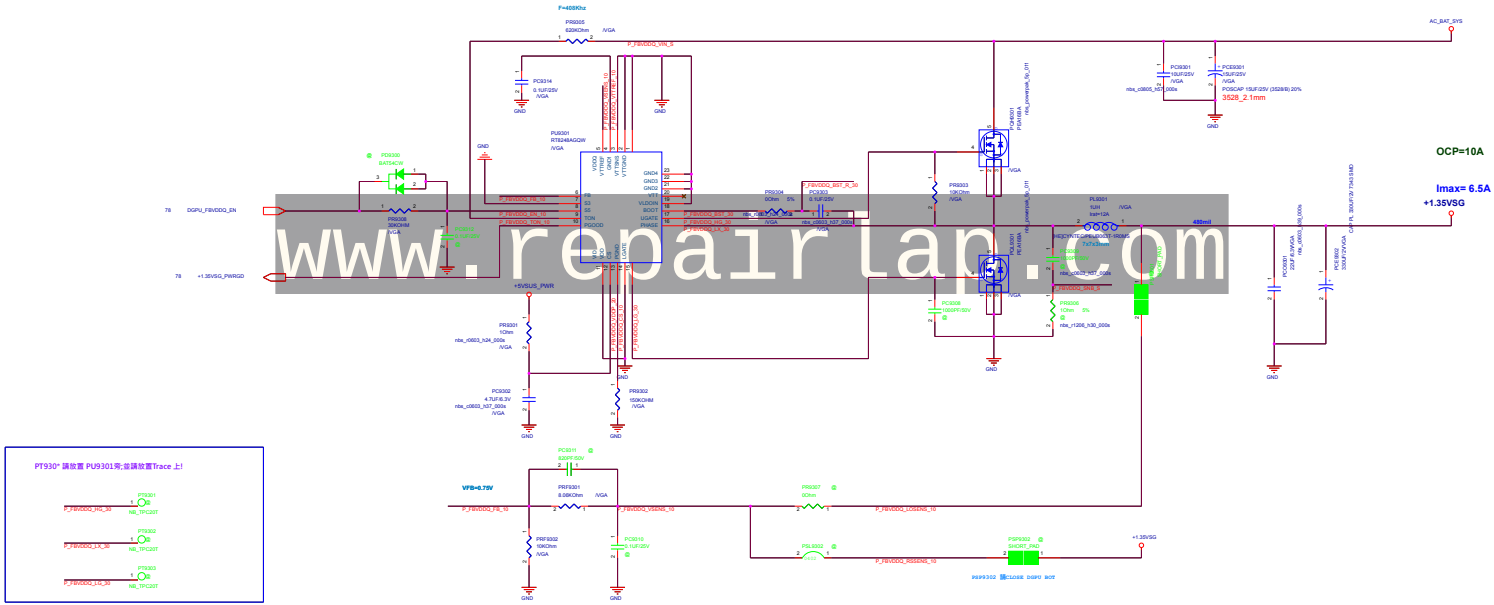
Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06
R/W	W	W	W	R	R	R	R
Function	Temp. alert threshold setting			Sensed temp. data			bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert

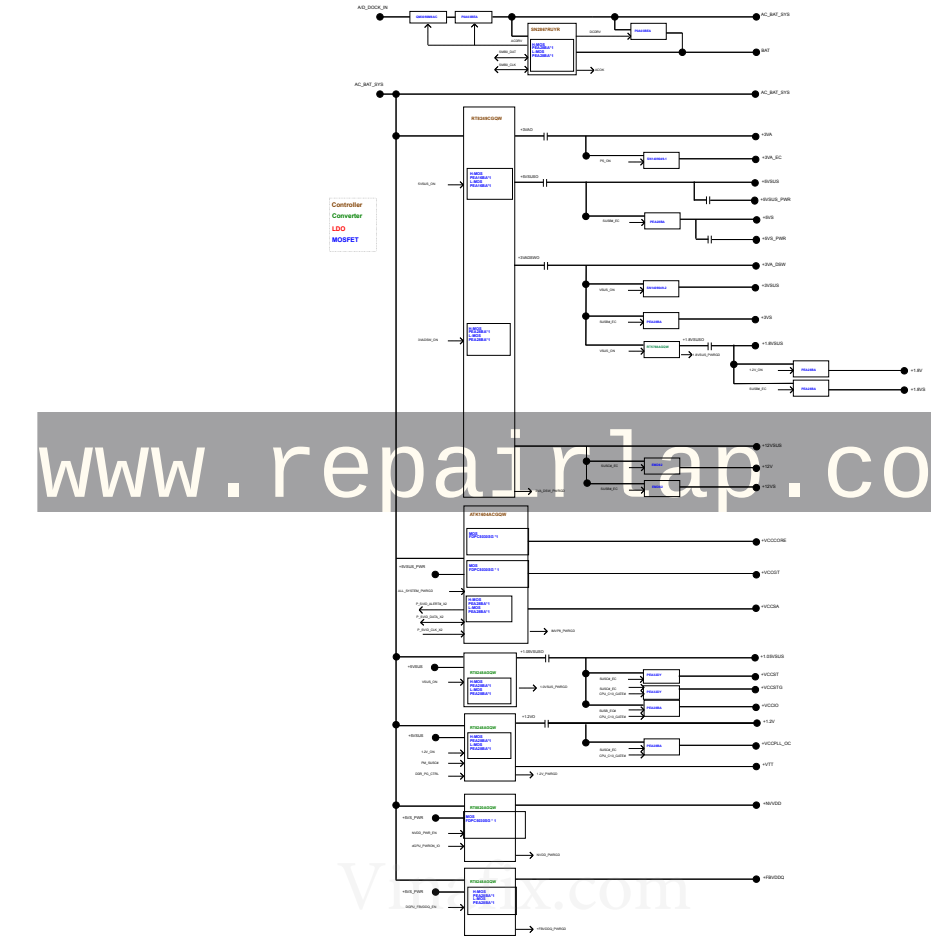


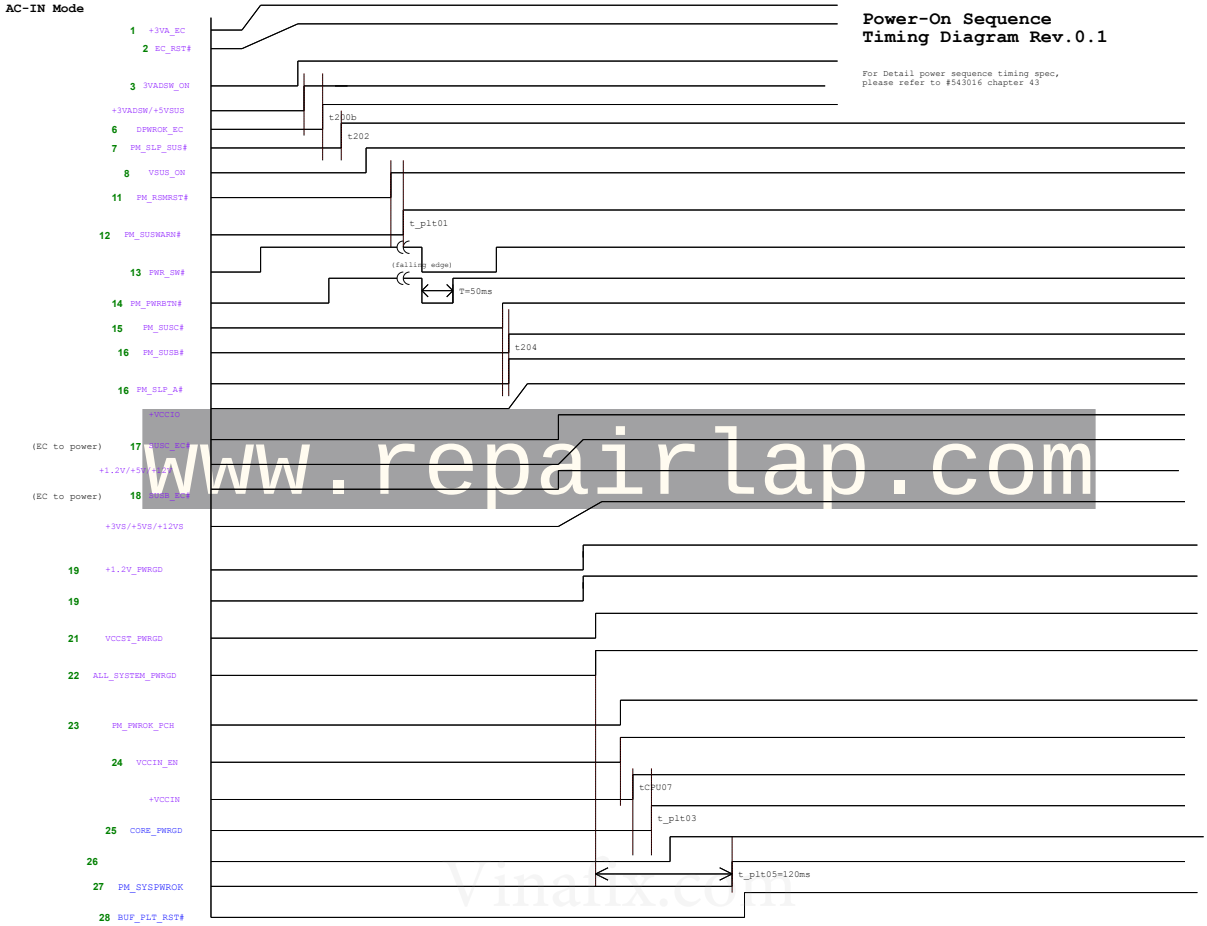



+NVVDD [For DGPU]
CPU_HIRG_MET
N17S Boot Voltage = 0.8V
N16S Boot Voltage = 0.9V
PWM-VID Spec
CLOSE PCI9101
+NVVDD
close to GPU
PSP9101 & +NVVDD CLOSE PCE9102
RTFSW=250K HZ
RT OC / SS
UPI COMP
UPI SS
OCP= 80A
Imax= 60A
12PIN FUNCTION
5PIN FUNCTION
PT910* 請放置 PU9101旁;並請放置Trace 上!
www.repairlap.com
Vinafix.com

+FBVDDQ [For VRAM]







AC-IN Mode

Power On Sequence Diagram Rev.2.0