

Temple University
College of Engineering
Department of Electrical and Computer Engineering (ECE)

Student Lab Report Cover Page

Course Number : 3613

Course Section : 002

Experiment # : Lab 8

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Date : 10/21/20

Grade : _____ /100

TA Name : Sung Choi

ACTIVITIES:

Activity 1

1. Code and Description

(1) Code (Full-Comment):

```
//ROBERT BARA Activity 1. 7-Segment Display
//CREATING THE SEGMENT DISPLAY BY USING .EQU
.EQU F=0B01110001
.EQU A=0B01110111
.EQU L=0B00111000
.EQU TWO=0B01011011
.EQU ZERO=0B00111111
//STACK POINTER
LDI R16,HIGH(RAMEND)
OUT SPH,R16
LDI R16,LOW(RAMEND)
OUT SPL,R16
//CONFIG FOR I/O
LDI R16,0XFF
OUT DDRA,R16
LDI R17,0X00 ;LED OFF
//CALLING EACH LETTER FOR 0.5 SEC, THEN TURNING IT OFF FOR 0.5 SEC, DISPLAYING "F A L L
2 0 2 0"
MAIN: LDI R16,F
      OUT PORTA,R16
      CALL delay_halfsec
      OUT PORTA,R17
      CALL delay_halfsec
      LDI R16,A
      OUT PORTA,R16
      CALL delay_halfsec
      OUT PORTA,R17
      CALL delay_halfsec
      LDI R16,L
      OUT PORTA,R16
      CALL delay_halfsec
      OUT PORTA,R17
      CALL delay_halfsec
      LDI R16,L
      OUT PORTA,R16
      CALL delay_halfsec
      OUT PORTA,R17
      CALL delay_halfsec
      LDI R16,TWO
      OUT PORTA,R16
      CALL delay_halfsec
      OUT PORTA,R17
      CALL delay_halfsec
      LDI R16,ZERO
      OUT PORTA,R16
```

```

CALL delay_halfsec
OUT PORTA,R17
CALL delay_halfsec
LDI R16,TWO
OUT PORTA,R16
CALL delay_halfsec
OUT PORTA,R17
CALL delay_halfsec
LDI R16,ZERO
OUT PORTA,R16
CALL delay_halfsec
OUT PORTA,R17
CALL delay_halfsec
JMP MAIN

```

delay_halfsec: ;subroutine to delay program by 0.5 seconds

```

LDI r30, 32
L4: LDI R31, 200
L5: LDI R29, 250
L6: NOP
NOP
DEC R29
BRNE L6
DEC R31
BRNE L5
DEC R30
BRNE L4
RET

```








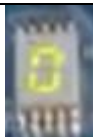
2. Result

(1) Tables

Activity 2 Result Table 1 – 7-Segment Display Operation

Port Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Segments	DP	G	F	E	D	C	B	A
EX. Letter 'F'	off	on	on	on	on	off	off	On
Binary (CC)	0	1	1	1	0	0	0	1
Letter 'A'	OFF	ON	ON	ON	OFF	ON	ON	ON
Binary (CC)	0	1	1	1	0	1	1	1
Letter 'L'	OFF	OFF	ON	ON	ON	OFF	OFF	OFF
Binary (CC)	0	0	1	1	1	0	0	0
Letter '2'	OFF	ON	OFF	ON	ON	OFF	ON	ON
Binary (CC)	0	1	0	1	1	0	1	1
Letter '0'	OFF	OFF	ON	ON	ON	ON	ON	ON
Binary (CC)	0	0	1	1	1	1	1	1

Activity 2 Result Table 2 – 7-Segment Display Result and Time Delay

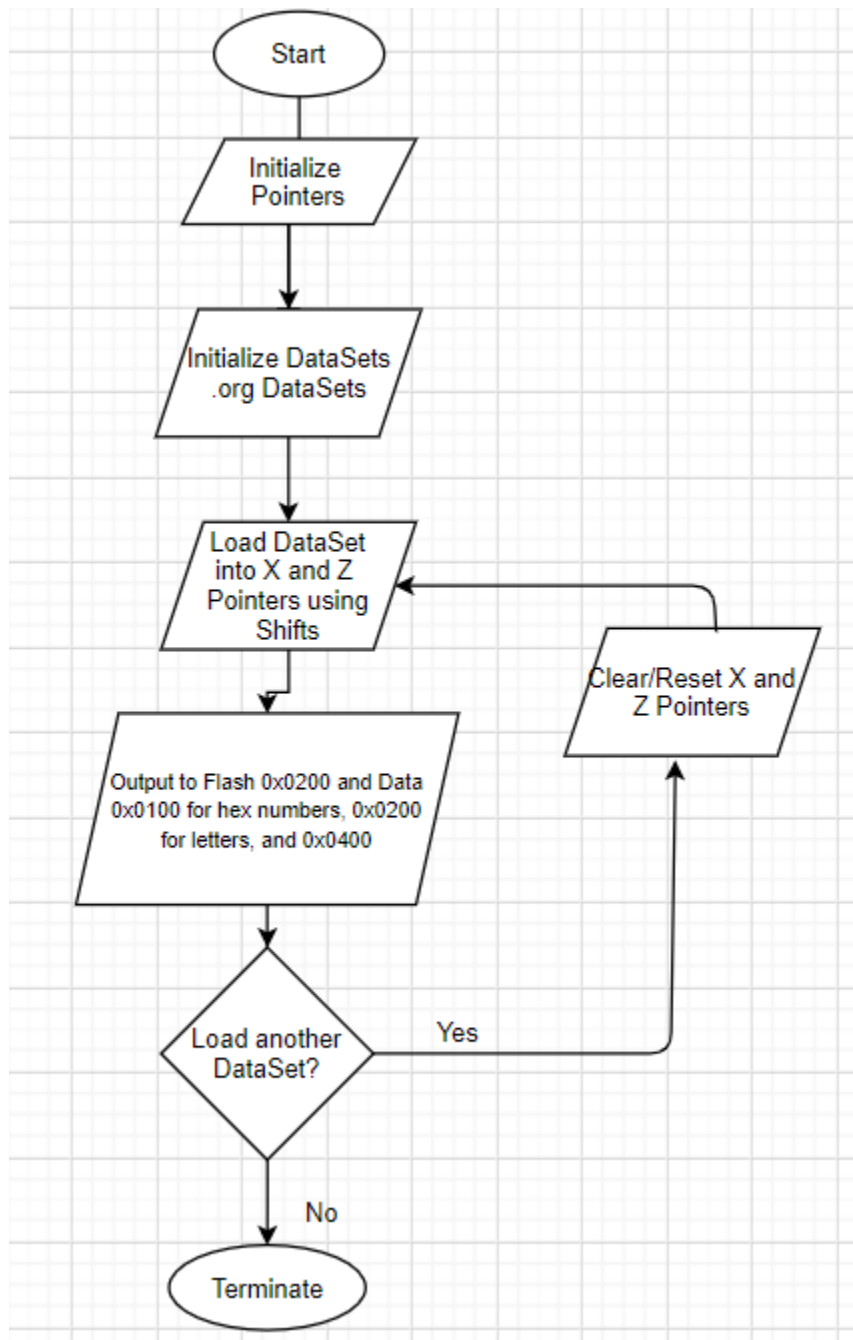
Output	Output PORTA	7-Segment Display view
Example		
F	01110001	
Task		
A	01110111	
L	00111000	
L	00111000	
2	01011011	
0	00111111	
2	01011011	
0	00111111	

(2) Result Video Link:

<https://youtu.be/wRa6cwhx87Y>

Activity 2

1. Flowchart



2. Code and Description

(1) Code with full-Comment

//ROBERT BARA Activity 2 Pointers USE Atmega324PB

.CSEG
START:

```

//loading in Dataset 1
//Initializing the Z pointer
LDI ZH,HIGH(0x080<<1) ;higher byte of the address, 0x080
LDI ZL,LOW(0x080<<1) ;lower byte of the address, 0x080
LDI XH,HIGH(0x0100); higher byte of the address, 0x0100
LDI XL,LOW(0x0100); lower byte of the address, 0x0100
//Resetting the pointers
LPM R18, Z+
ST X+, R18
LPM R18, Z+
ST X+, R18
LPM R18, Z+
ST X+, R18
LPM R18, Z+
ST X+, R18
NOP

//loading in Dataset 2
LDI ZH,HIGH(0x0100<<1) ;higher byte of the address, 0x0100
LDI ZL,LOW(0x0100<<1) ;lower byte of the address, 0x0100
LDI XH,HIGH(0x0200); higher byte of the address, 0x0200
LDI XL,LOW(0x0200); lower byte of the address, 0x0200
//Resetting the pointers
LPM R18, Z+
ST X+, R18
LPM R18, Z+
ST X+, R18
LPM R18, Z+
ST X+, R18
LPM R18, Z+
ST X+, R18
LPM R18, Z+
ST X+, R18
LPM R18, Z+
ST X+, R18
NOP

//loading in Dataset 3
LDI ZH,HIGH(0x0200<<1) ;higher byte of the address, 0x0200
LDI ZL,LOW(0x0200<<1) ;lower byte of the address, 0x0200
LDI XH,HIGH(0x0400); higher byte of the address, 0x0400
LDI XL,LOW(0x0400); lower byte of the address, 0x0400
//Resetting the pointers
LPM R18, Z+
ST X+, R18
LPM R18, Z+
ST X+, R18
LPM R18, Z+
ST X+, R18
LPM R18, Z+
ST X+, R18
LPM R18, Z+
ST X+, R18
LPM R18, Z+
ST X+, R18
NOP

```

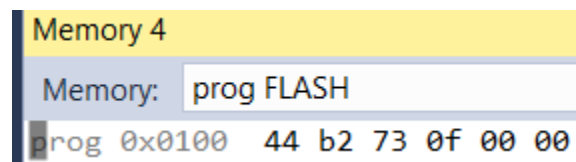
```
//DATASETS in the program memory locations 0x080, 0x0100, 0x0200 (physical address:
0x0100, 0x0200, 0x0400)
.ORG 0x080
DataSet1: .DB $44,$B2,$73,$0F,0,0
.ORG 0x0100
DataSet2: .DB 'T', 'E', 'M', 'P', 'L', 'E', 0, 0
.ORG 0x0200
DataSet3: .DB "Engr",0

.EXIT
```

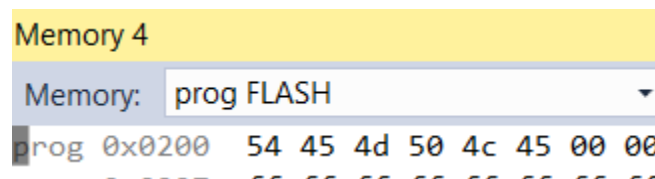
3. Result

Result screenshots – Flash memory contents, data memory contents

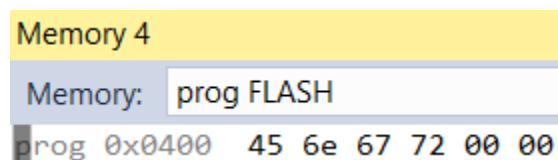
Flash Memory Contents:



[DataSet1: Flash Memory Contents]

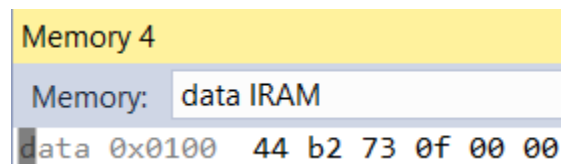


[DataSet2: Flash Memory Contents]



[DataSet3: Flash Memory Contents]

Data Memory Contents:



[DataSet1: Data Memory Contents]

Memory 4									
Memory:		data IRAM							
data	0x0200	54	45	4d	50	4c	45	00	00
...

[DataSet2: Data Memory Contents]

Memory 4									
Memory:		data IRAM							
data	0x0400	45	6e	67	72	00	00

[DataSet3: Data Memory Contents]

ECE3613 Processor System Laboratory Rubric

Lab #: 8

Section: 001/002

Name: _____

Activity	Task	Full Points	Earned Points	Comment
1	Code (Full comments)	10		
	Result: Tables	30		Result Table 1(10 points) and 2 (20 points)
	Video	10		Result video link
2	Flowchart	10		
	Code (full comments)	20		
	Result – memory values	20		Program Memory and Data Memory Screenshots
Total		100		