

**Title:** Lab 7. DC Models for Bipolar Transistors**Name:** Robert Bara**Partner:** Dalton Hamilton, Mohamad Asaf, Abdulaziz Almersi

**General Objective:** Lab 7 serves to examine the DC characteristics of a Bipolar Junction Transistor (BJT) by simulating a DC Sweep and examining the BJT's IV curve. By examining the IV curve of a BJT, the regions of operation can be concluded and referred to when using the BJT to design amplifiers or upon using the transistor as a switch.

**Background Activities:**

A Bipolar Junction Transistor differs from the MOSFET transistor by using current to control the transistor similar to how a faucet controls water flow. The BJT can operate in 4 regions: cut-off and saturation which acts as if it is switching between and open and close circuit, as well as forward and reverse active regions. In the cutoff mode, both junctions are reversed biased, leading to an extremely small reverse current, and 0 forward current. In the Active/Saturation regions, one of the junctions is forward biased while the other is reversed biased, therefore current will flow and act as a switch. BJT's are made up of three layers either consisting of N-type or P-type doped semi-conducting material to form either an NPN or PNP transistor. Both transistors use 3 terminals from top to bottom based upon the schematic, the Collector (C), Base (B) in the middle, and Emitter (E) on the bottom:

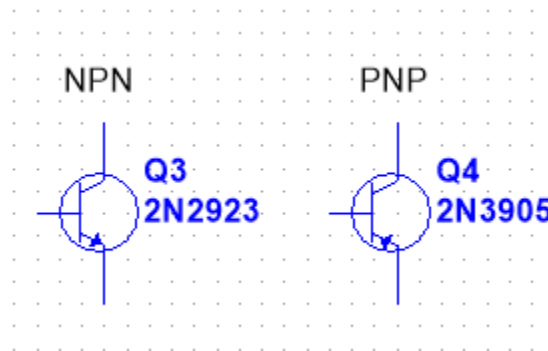


Figure 1. Example of NPN and PNP

BJTs came into the world electronics during the late 1940s as germanium transistors, well into the silicon revolution, as an answer to replace large, fragile vacuum tubes. THE BJT operates by controlling the flow of negatively charged electrons and positively charged holes within a doped semiconductor. Realistically, the BJT is two PN junctions merged together with opposite polarities, so the BJT can be thought of as two diodes. Upon injecting a positive or negative current within the middle layer, the bias voltage will be manipulated to control the current flowing from the emitter to the collector.

**Procedure****PART I**

Begin by launching Multisim and creating a circuit with a 1A DC current source running into the base of the NPN 2N2923 Transistor, while a DC voltage of 12V runs connecting from the collector to emitter. Ground the circuit and place a current probe going into the collector:

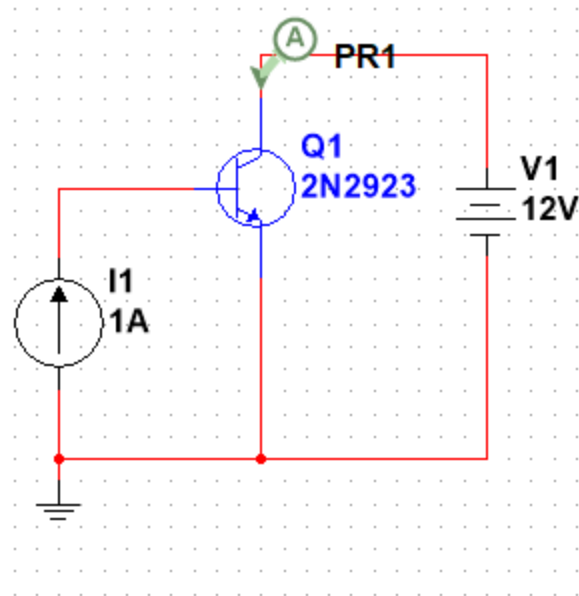


Figure 2. Testing an NPN circuit

Select a DC Sweep analysis and configure the parameters so that the X-axis shows the collector voltage  $V_C$  with the following parameters: Start value=0V, Stop value=1V, Increments by 0.005V. Enable source 2 and plot the Base current  $I_B$  with the parameters: Start value=0.15mA, stop value=0.6mA, and increments by 0.1125mA. Then head over to the output tab and add  $I(Q1[IC])$  from the variable's list to plot the base current as the Y-Axis. Below appears to be the parameters:

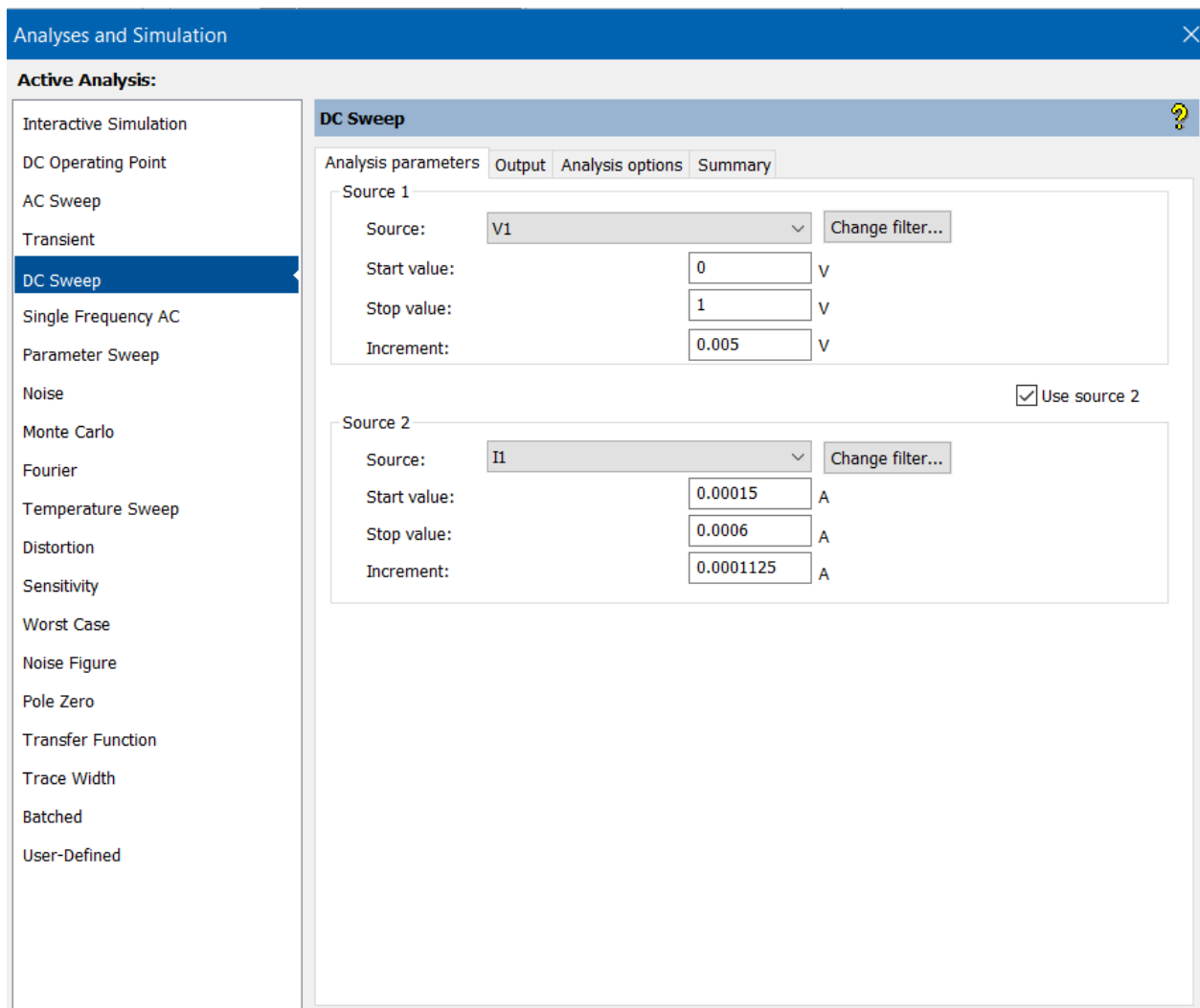


Figure 3. DC Sweep parameters

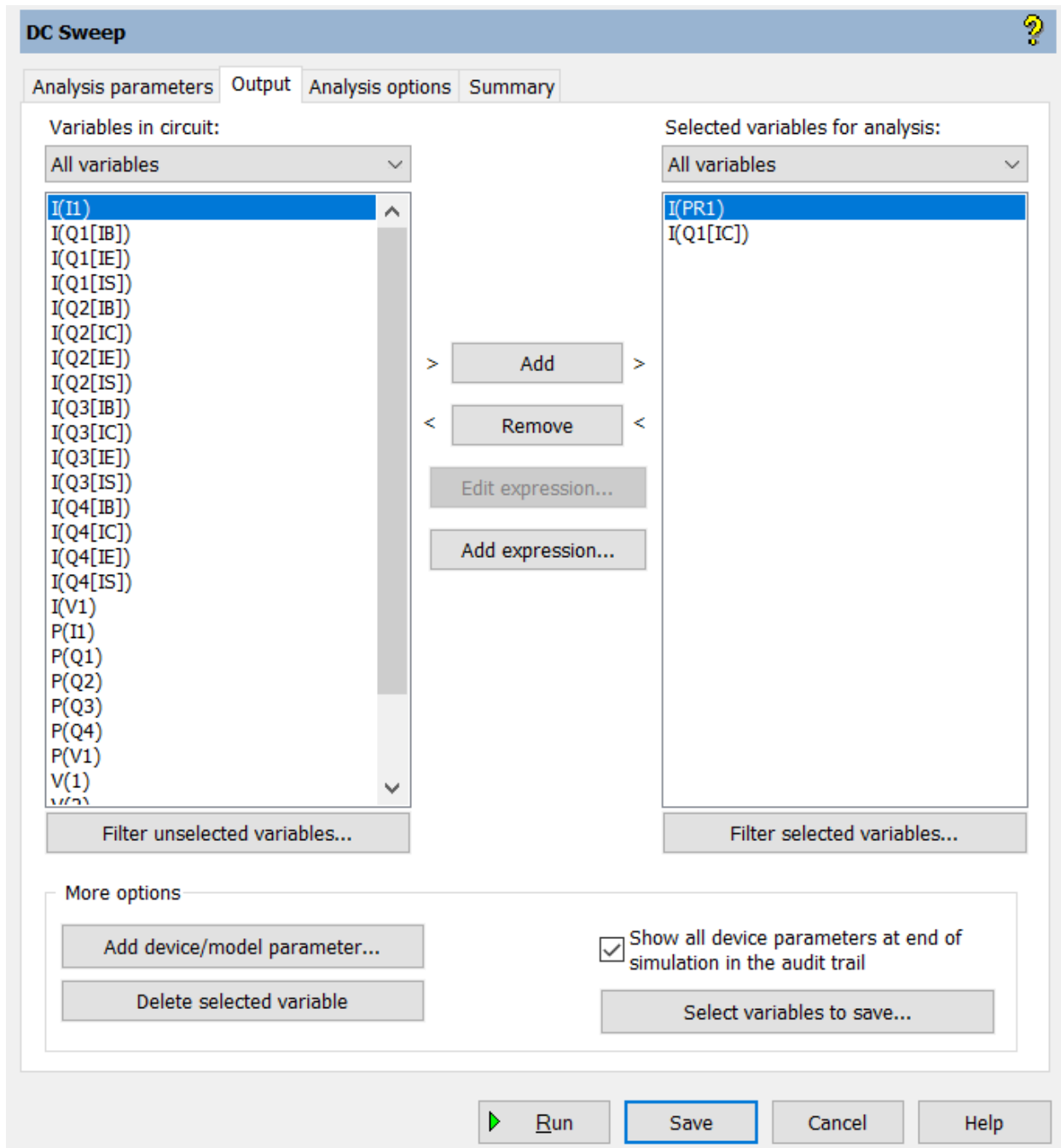


Figure 4. Selecting the correct parameters to output to graph

Run the simulation and use the cursors and zoom functions to approximate the voltage that the plots begin to separate.

## PART II

Simply add a PNP 2N3905 transistor and hook Multisim's IV analyzer up to the BJT as follows:

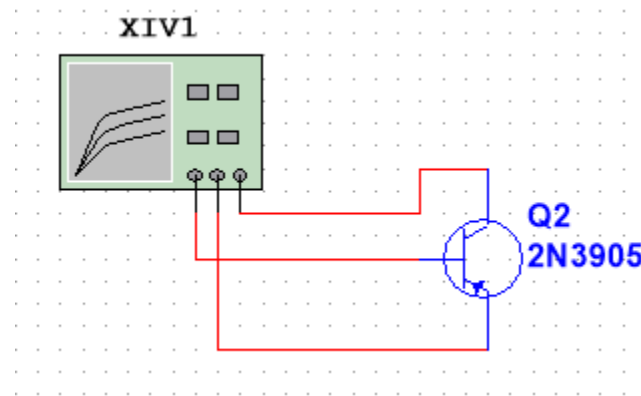


Figure 5. Wiring the IV Analyzer to a PNP

Open the IV Analyzer and set the component parameter to PNP. Select simulate parameter and change the  $V_{ce}$  values to start at 0V, stop at 1V, and increment by 50mV. Also set the  $I_b$  values to start at 1mA, stop at 10mA, and step by a factor of 5. An outputted IV graph should generate similar to the one used within PART I for the NPN. This graph will be able to show the 3 regions of operation: cutoff, saturation, and active. Using the simulation results, compare the voltage when current begins to flow and when the graphs start to differ from the PNP and NPN graphs.

## Results:

### 1.1 Simulation Results:

#### PART I

Below is the circuit I built to simulate part I:

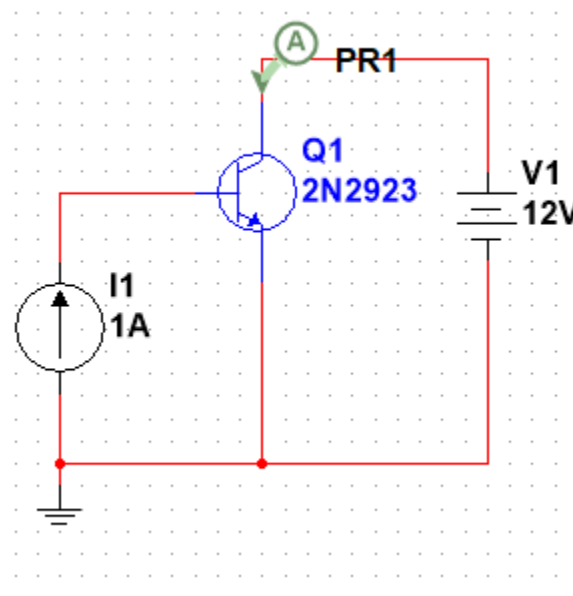


Figure 6. Circuit built for Part I

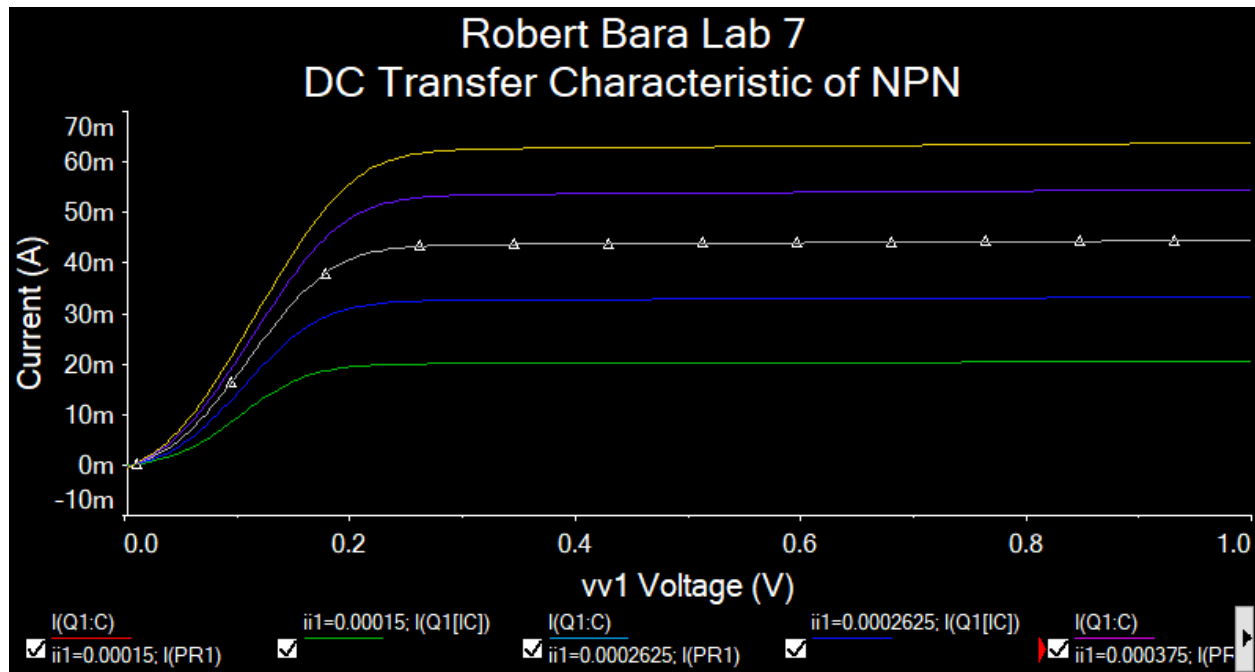


Figure 7. IV curve from DC Sweep of NPN

Judging from the DC Sweep, it is apparent where the active region levels out after about 0.2V, while the saturation region is when the current and voltage increases non-linearly. The cutoff region is not shown by the IV analyzer. Furthermore, the graph can be zoomed in to further approximate the voltage that the transistor enters the saturation region.

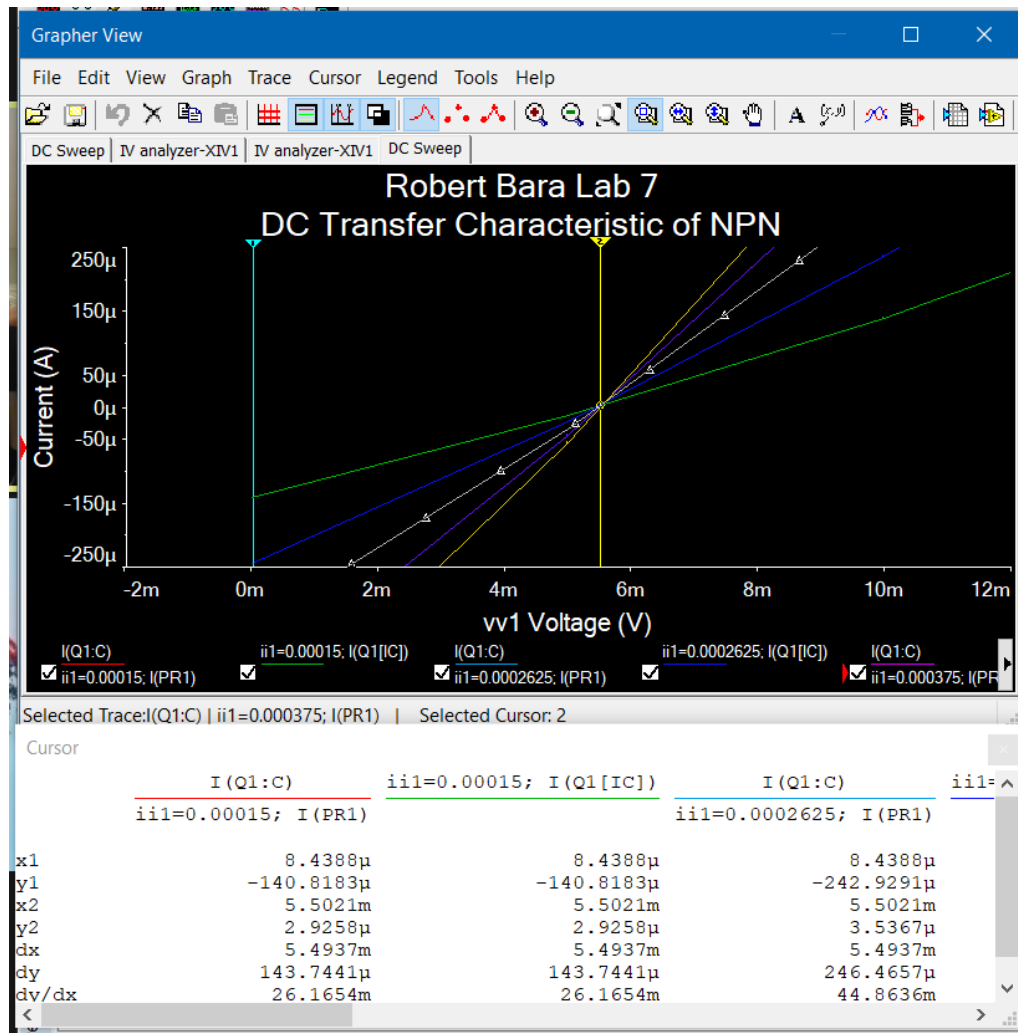


Figure 8. Zooming into DC sweep to approximate voltage

The graphs start to differ at approximately 5.5mV and current begins to flow.

## PART II

The circuit for part II is as follows:

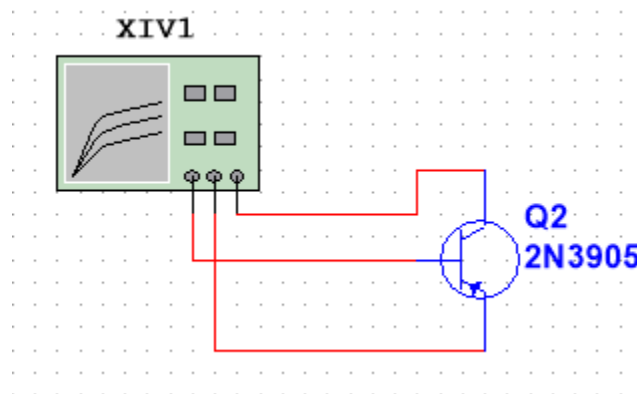


Figure 9. Circuit used for PART II

Using the IV analyzer, the following graph was collected, noting that the saturation region is larger and more linear in contrast to the NPN transistor used within PART I:



Figure 10. IV curve of PNP transistor

Using the cursor, the voltage in which the PNP enters the saturation region can be approximated as follows:



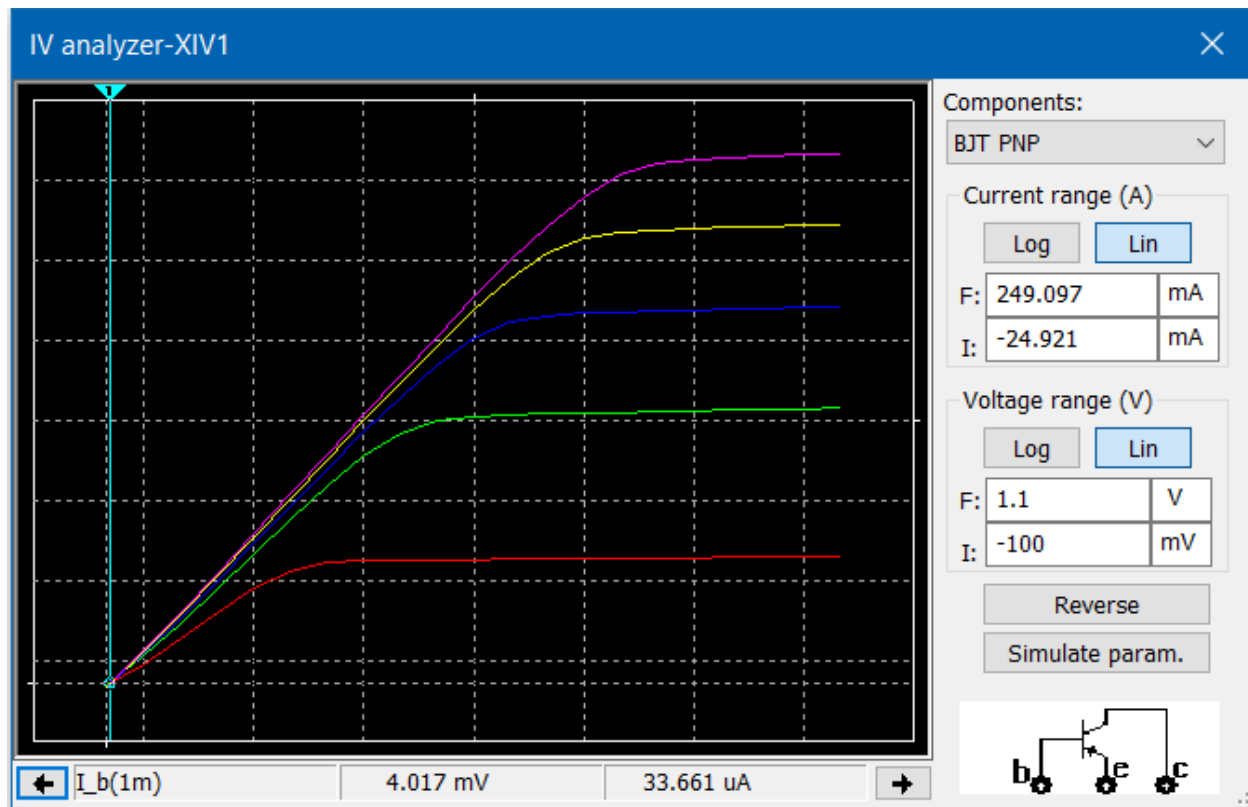


Figure 11. Estimated voltage of 4.017mV when current begins to flow

This voltage is approximately 4.017mV, it corresponds to when current begins to flow. This differs by approximate 1.5mV compared to the NPN transistor that was analyzed within the first part of this lab.

## 2.0 Conclusion:

The primary purpose of this lab was to explore multiple ways to analyze the IV characteristics between BJT transistors. This lab verified the operational regions of BJTs by examining two very different kinds of BJT's: a 2N2923 NPN transistor vs a 2N3905 PNP transistor. Utilizing this lab further demonstrated the building blocks of how a BJT can be used within amplifier and switching circuits, which will pave way for the SPICE project to come.