ECE3623 Embedded System Design Laboratory

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Vivado AXI Timer and Interrupts

In this Laboratory you will utilize to the embedded development of a Vivado Zynq Processor System (PS) with the AXI Timer and interrupts. The tasks are described in detailed in Chapter 2 of the eText *The Zynq Book Tutorials* with the supporting files in the *The Zynq Book Tutorials Sources* both of which are posted on *Canvas* and the Lecture PowerPoints.

The Laboratory requires you to study and execute the fourth section of Chapter 2 of the *Next Steps in Zynq SoC Design*. Exercise 2D extends the previous projects in Chapter 2 of *The Zynq Book Tutorials* by adding the AXI Timer IP block as additional interrupt source and the Concat (concatenation) IP block to configure and complete the Zynq PS configuration.
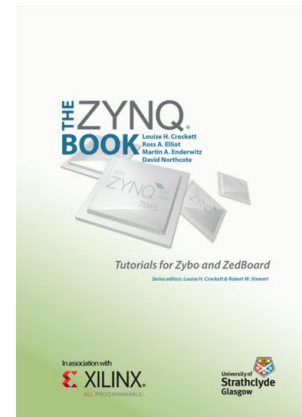
The final section of Exercise 2D of *Next Steps in Zynq SoC* results in a task that increments a counter with interrupts from both the AXI Timer and the push buttons and displays the unsigned 4-bit binary count on the LEDs.

The Laboratory tasks are as follows:

1. Describe in detail the modules and complete operation of the unmodified *interrupt_controller_tut_2D.c* project. This will require that you research the various Xilinx Zynq C functions and parameters. Run the complete exercise without modification to verify its performance.

2. You are to add a GPIO to interface the four slide switches (SW) to the project *without interrupts*. SW3 ON disables all push button interrupts (BTN0, BTN1, BTN2 and BTN3). SW3 OFF enables all push button interrupts. This will require you to locate the parameter description of this added GPIO.

3. If SW2 is ON a reset process executes which ensures that the number of times the AXI Timer will interrupt the process is set to 3 (default) and that all other slide slides are OFF and no push button are pushed. A reset error is indicated by flashing all four LEDs ON for about 1 second ON and OFF for about 1 second until the other slide switches are OFF and no push buttons are depressed. SW2 OFF begin normal execution as in Tasks 2, 4 and 5. Test and demonstrate this reset procedure.

4. BTN0 when an interrupt occurs increments the current number of times the AXI Timer will interrupt the process before it increments the count autonomously (originally set to 3 interrupts) with a maximum count of 7 interrupts. SW0 must be ON for BTN0 to be an effective interrupt. The current incremented number of times are to be displayed in the LEDs for about 2 seconds. The LEDs then return to the displaying the current count.

5. BTN1 when an interrupt occurs decrements the current number of times the AXI Timer will interrupt the process before it increments the count autonomously (originally set to 3 interrupts) with a minimum count of 1 interrupt. SW1 must be ON for BTN1 to be effective. The current decremented number of times are to be displayed in the LEDs for about 2 seconds. The LEDs then return to the displaying the current count.

6. BTN2 and BTN3 interrupts are ignored.

Describe in detail and list the modifications to the *interrupt_controller_tut_2D.c* project file to accomplish each of these Laboratory tasks referenced by *number in the Laboratory report.*

This Laboratory is for the week starting February 16th and due no later than February 23rd 11:59 PM with an upload to Canvas.