# Temple University College of Engineering Department of Electrical and Computer Engineering (ECE)

### **Student Lab Report Cover Page**

Course Number : 3613

Course Section : 002

Experiment # : Lab #7

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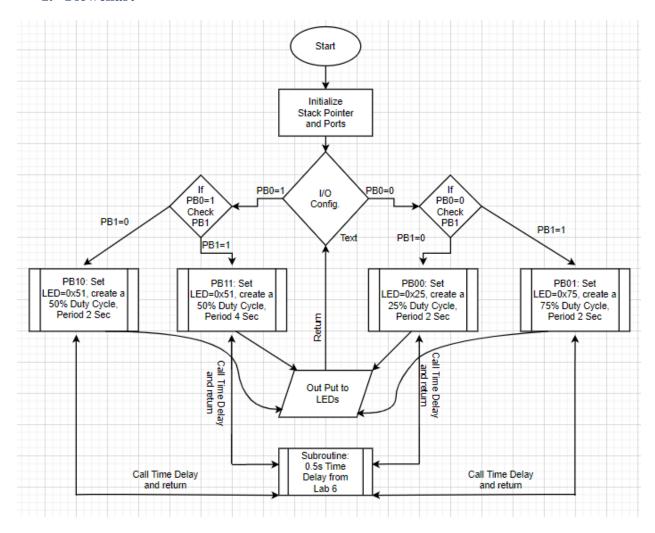
Date : 10/14/2020

Grade : \_\_\_\_\_ /100

TA Name : Sung Choi

#### **ACTIVITY:**

#### 1. Flowchart



[Figure. Flow Chart for Overall Program Process]

#### 2. Code and Description

Code must be with the full-comment: each section description and line description

## //Stack Pointer LDI R16,LOW(RAMEND) OUT SPL,R16

start:

LDI R16, HIGH(RAMEND)

OUT SPH, R16

//PORT CONFIGURATION

LDI R16,0X00 OUT DDRB,R16

LDI R16,0XFF

```
OUT DDRA,R16
OUT PORTB,R16 ; setup pullup resistor
//CONDITIONING FOR I/O
IO:
       SBIC PINB,0 //CHECK PB0=0
       CALL PB_1 //IF PB0=0, PB0=1
       SBIS PINB,0 //CHECK PB1=1
       CALL PB 2
                    //IF PB0=0
       rjmp start
//CASE OF PB0=1
PB_1: SBIC PINB,1 //CHECK PB1=0
       CALL PB11 //IF PB1=1,PB1=1
       SBIS PINB,1 //CHECK PB1=1
       CALL PB10 //IF PB0=1,PB1=0
      RET
//CASE OF PB0=0
PB_2: SBIC PINB,1
      CALL PB01
                    //IF PB0=0,PB1=1
       SBIS PINB,1
      CALL PB00
                    //IF PB0=0,PB1=0
       RET
       //PB0=0, PB1=0, LED=0X25
PB00: SBI PORTA,0
      SBI PORTA,0
       SBI PORTA, 2
       SBI PORTA, 5
      CALL DELAY //25% DUTY CYCLE
      CBI PORTA,0
      CBI PORTA, 2
      CBI PORTA, 5
       CALL DELAY //PERIOD 2 SEC
       CALL DELAY
       CALL DELAY
      RET
//PB0=1, PB1=0, LED=0X51
PB10: SBI PORTA,0
       SBI PORTA,4
       SBI PORTA,6
      CALL DELAY //50% DUTY CYCLE
      CALL DELAY
      CBI PORTA, 0
      CBI PORTA,4
      CBI PORTA,6
       CALL DELAY //PERIOD 2 SEC
       CALL DELAY
       RET
//PB0=0, PB1=1, LED=0X75
PB01: SBI PORTA,0
       SBI PORTA, 2
       SBI PORTA,4
      SBI PORTA,5
      SBI PORTA,6
      CALL DELAY //75% DUTY CYCLE
      CALL DELAY
      CALL DELAY
      CBI PORTA, 0
      CBI PORTA, 2
```

```
CBI PORTA,4
       CBI PORTA,5
       CBI PORTA,6
       CALL DELAY //PERIOD 2 SEC
       CALL DELAY
       RET
//PB0=1, PB1=1, LED=0X51
PB11: SBI PORTA,0
      SBI PORTA,4
       SBI PORTA,6
       CALL DELAY //DUTY CYCLE 50%
       CALL DELAY
       CBI PORTA, 0
       CBI PORTA,4
       CBI PORTA,6
       CALL DELAY //4 SEC PERIOD
       CALL DELAY
       CALL DELAY
       RET
//TIME DELAY FOR 0.5 SEC
DELAY: LDI R20,32
              L1: LDI R21, 200
              L2: LDI R22, 250
              L3:
                     NOP
                     NOP
                     DEC R22
                     BRNE L3
                     DEC R21
              BRNE L2
              DEC R20
              BRNE L1
              RET
```

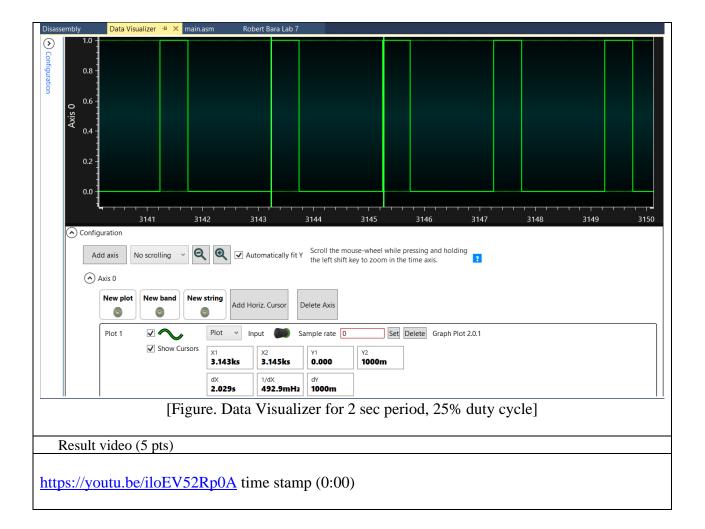
- 3. Result: Result Picture, Table, and Description:
  - Case 1: PB0=0, PB1=0



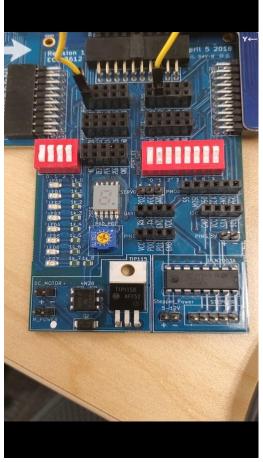
[Figure. Input switches PB0=0, PB1=0]



[Figure. LED results PB0=0, PB1=0]



• Case 2: PB0=1, PB1=0



[Figure. Input switches PB0=1, PB1=0]



[Figure. LED results PB0=1, PB1=0]



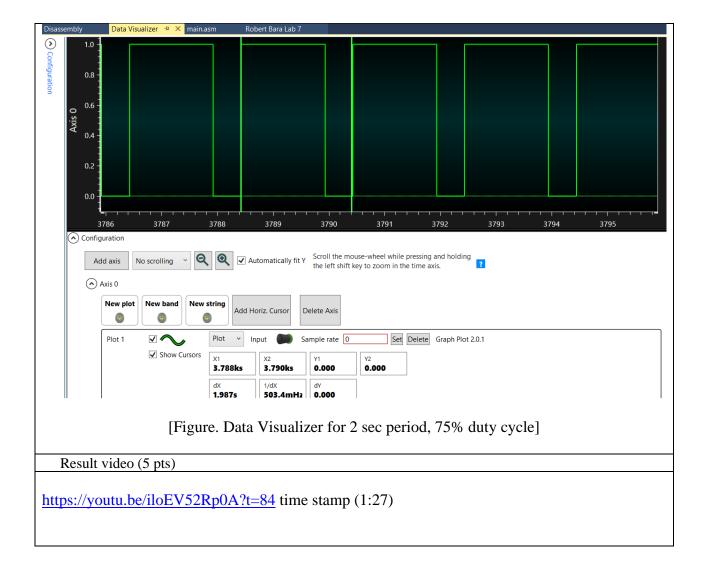
• Case 3: PB0=0, PB1=1



[Figure. Input switches PB0=0, PB1=1]



[Figure. LED results PB0=0, PB1=1]



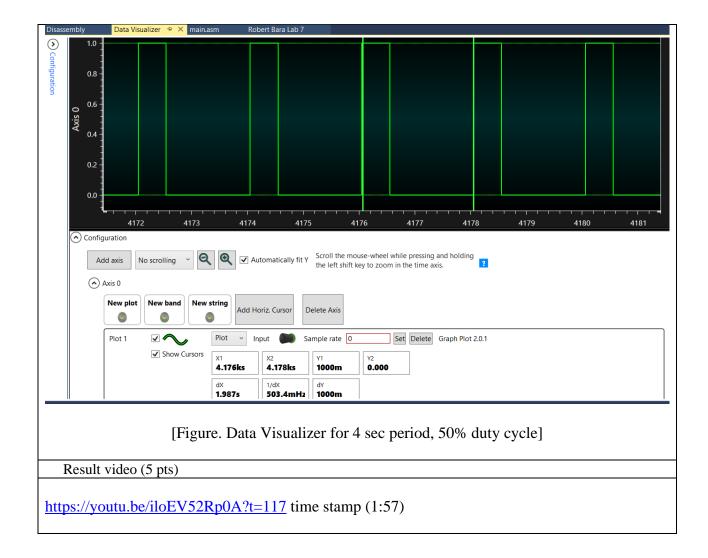
• Case 4: PB0=1, PB1=1



[Figure. Input switches PB0=1, PB1=1]



[Figure. LED results PB0=1, PB1=1]



#### **ECE3613 Processor System Laboratory Rubric**

Lab #: 7

**Section: 01 / 02** 

Name: \_\_\_\_\_

Activity	Task	Full Points	Earned Points	Comment
1	Flowchart	10		

	Code and Description	10	Code (5 pts), Comments (5 pts)
	Result 1	20	Resulted pictures of input switches (5 pts), output LEDs (5 pts), and the reading of data visualizer (5 pts), and result video (5 pts)
	Result 2	20	Resulted pictures of input switches (5 pts), output LEDs (5 pts), and the reading of data visualizer (5 pts), and result video (5 pts)
	Result 3	20	Resulted pictures of input switches (5 pts), output LEDs (5 pts), and the reading of data visualizer (5 pts), and result video (5 pts)
	Result 4	20	Resulted pictures of input switches (5 pts), output LEDs (5 pts), and the reading of data visualizer (5 pts), and result video (5 pts)
Tot	al		