

**PROGRAMMING, PC-CONNECTING & CLOCK**

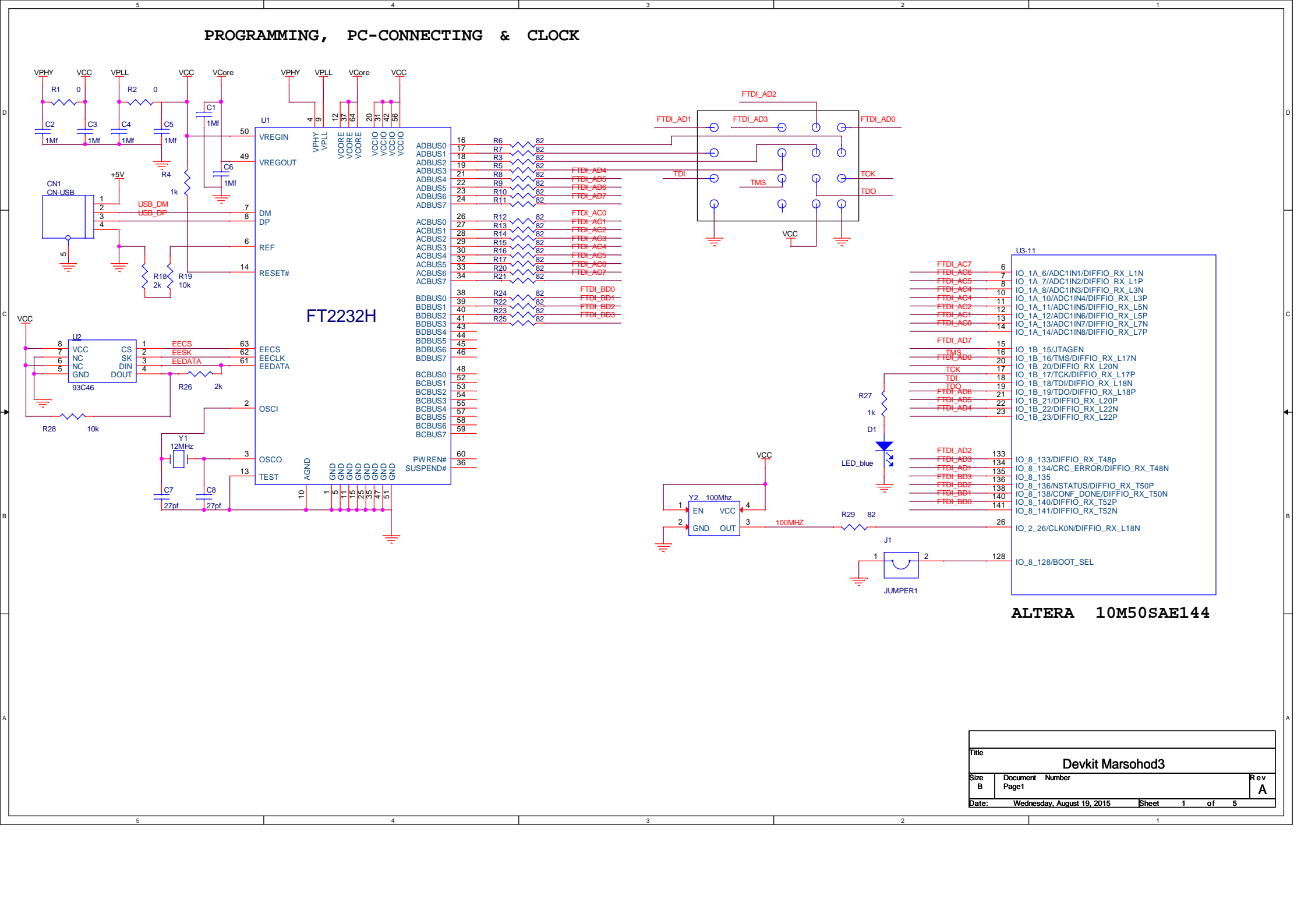
The schematic diagram illustrates the programming, PC-connecting, and clock circuit for the FT2232H chip (U1). The circuit includes the following components and connections:

- Power Supplies:** VPHY, VPLL, VCore, and VCC are connected to the FT2232H chip. VPHY and VPLL are connected to the VREGIN and VREGOUT pins, respectively. VCore is connected to the VCC pin. VCC is connected to the VCC pin.
- USB Connector (CN1):** The USB connector is connected to the FT2232H chip. The USB\_DM and USB\_DP pins are connected to the DM and DP pins, respectively. The USB\_GND pin is connected to the GND pin.
- USB-to-UART Bridge (U2):** The USB-to-UART bridge is connected to the FT2232H chip. The VCC, NC, and GND pins are connected to the VCC, NC, and GND pins, respectively. The CS, SK, DIN, and DOUT pins are connected to the EECS, EESK, EEDATA, and EEDATA pins, respectively.
- 12MHz Oscillator (Y1):** The 12MHz oscillator is connected to the FT2232H chip. The OSCIN and OSCOUT pins are connected to the OSCIN and OSCOUT pins, respectively. The GND pin is connected to the GND pin.
- FTDI Chip (U3-11):** The FTDI chip is connected to the FT2232H chip. The FTDI\_AD0, FTDI\_AD1, FTDI\_AD2, FTDI\_AD3, FTDI\_AD4, FTDI\_AD5, FTDI\_AD6, and FTDI\_AD7 pins are connected to the FTDI\_AD0, FTDI\_AD1, FTDI\_AD2, FTDI\_AD3, FTDI\_AD4, FTDI\_AD5, FTDI\_AD6, and FTDI\_AD7 pins, respectively. The FTDI\_TMS, FTDI\_TDI, and FTDI\_TDO pins are connected to the TMS, TDI, and TDO pins, respectively. The FTDI\_VCC pin is connected to the VCC pin.
- 100MHz Oscillator (Y2):** The 100MHz oscillator is connected to the FTDI chip. The EN, VCC, and GND pins are connected to the EN, VCC, and GND pins, respectively. The OUT pin is connected to the FTDI\_TDI pin.
- Jumper (J1):** The jumper is connected to the FTDI chip. The J1 pin is connected to the FTDI\_TDI pin.

The diagram also shows the connection of the FT2232H chip to the Altera 10M50SAE144 chip. The FT2232H chip is connected to the Altera chip via the FTDI chip. The FTDI chip is connected to the Altera chip via the FTDI\_AD0, FTDI\_AD1, FTDI\_AD2, FTDI\_AD3, FTDI\_AD4, FTDI\_AD5, FTDI\_AD6, and FTDI\_AD7 pins. The FTDI\_TMS, FTDI\_TDI, and FTDI\_TDO pins are connected to the TMS, TDI, and TDO pins, respectively. The FTDI\_VCC pin is connected to the VCC pin.

**ALTERA 10M50SAE144**

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**PROGRAMMING, PC-CONNECTING & CLOCK**

The schematic diagram illustrates the FT2232H interface circuit for the Altera 10M50SAE144. The FT2232H (U1) is connected to the Altera 10M50SAE144 (U3-11). The circuit includes power supply connections (VPHY, VPLL, VCore, VCC), a USB-DP connector (CN1), and various pins for ADBUS, ACBUS, BDBUS, and BCBUS. The FT2232H is configured with various pins for ADBUS, ACBUS, BDBUS, and BCBUS. The Altera 10M50SAE144 is configured with various pins for IO\_1A, IO\_1B, IO\_8, and IO\_14. The diagram also shows a 100MHz clock source (Y2) and a 100MHz output (R29).

**ALTERA 10M50SAE144**

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The schematic diagram illustrates the hardware setup for programming, PC-connecting, and clocking the Altera 10M50SAE144 using the FT2232H interface chip.

**FT2232H (U1) Connections:**

- Power Supply:** VPHY, VPLL, VCore, and VCC are connected to the appropriate pins. A 1Mf capacitor (C1) is connected to VCore.
- USB-DP Connector (CN1):** The USB-DP connector is connected to the FT2232H pins. A 5V supply is connected to the USB-DP pin.
- Control Signals:** DM, DP, REF, and RESET# are connected to the FT2232H pins.
- Serial Interface:** The FT2232H is configured with various pins for ADBUS, ACBUS, BDBUS, and BCBUS.
- Clock and Test:** The OSCI, OSCO, and TEST pins are connected to the FT2232H pins. A 12MHz crystal (Y1) is connected to the OSCI and OSCO pins.

**Altera 10M50SAE144 (U3-11) Connections:**

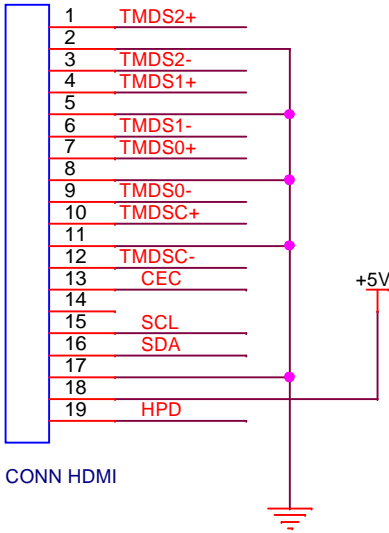
- FTDI Interface:** The FTDI pins (FTDI\_AD0 to FTDI\_AD7) are connected to the Altera 10M50SAE144 pins.
- JTAG Interface:** The JTAG pins (TMS, TCK, TDO) are connected to the Altera 10M50SAE144 pins.
- LED:** A blue LED (D1) is connected to the Altera 10M50SAE144 pins.
- 100MHz Clock:** A 100MHz clock source (Y2) is connected to the Altera 10M50SAE144 pins.
- Other Signals:** The Altera 10M50SAE144 is configured with various pins for IO, ADC, and other functions.

**ALTERA 10M50SAE144**

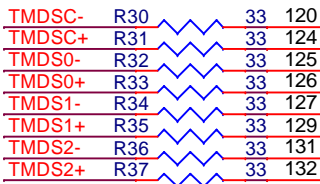
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HDMI & CONNECTORS

J2



CONN HDMI



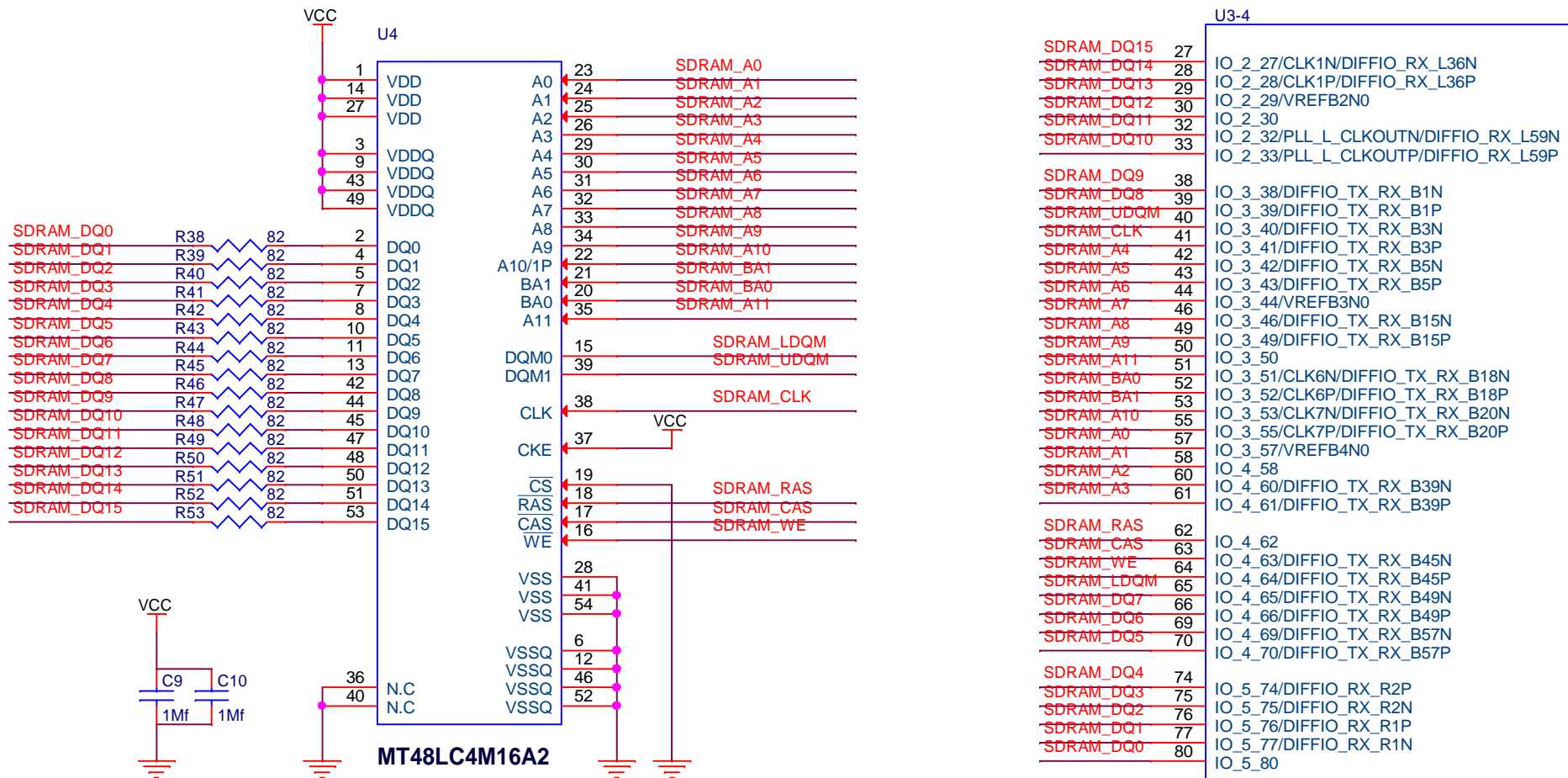
U3-9

IO\_8\_120/DIFFIO\_RX\_T30N  
IO\_8\_124/DEV\_CLRN/DIFFIO\_RX\_T42N  
IO\_8\_125/DEV\_OE  
IO\_8\_126/VREFB8N0  
IO\_8\_127/DIFFIO\_RX\_T45P  
IO\_8\_129/DIFFIO\_RX\_T45N  
IO\_8\_131/DIFFIO\_RX\_T46P  
IO\_8\_132/DIFFIO\_RX\_T46N

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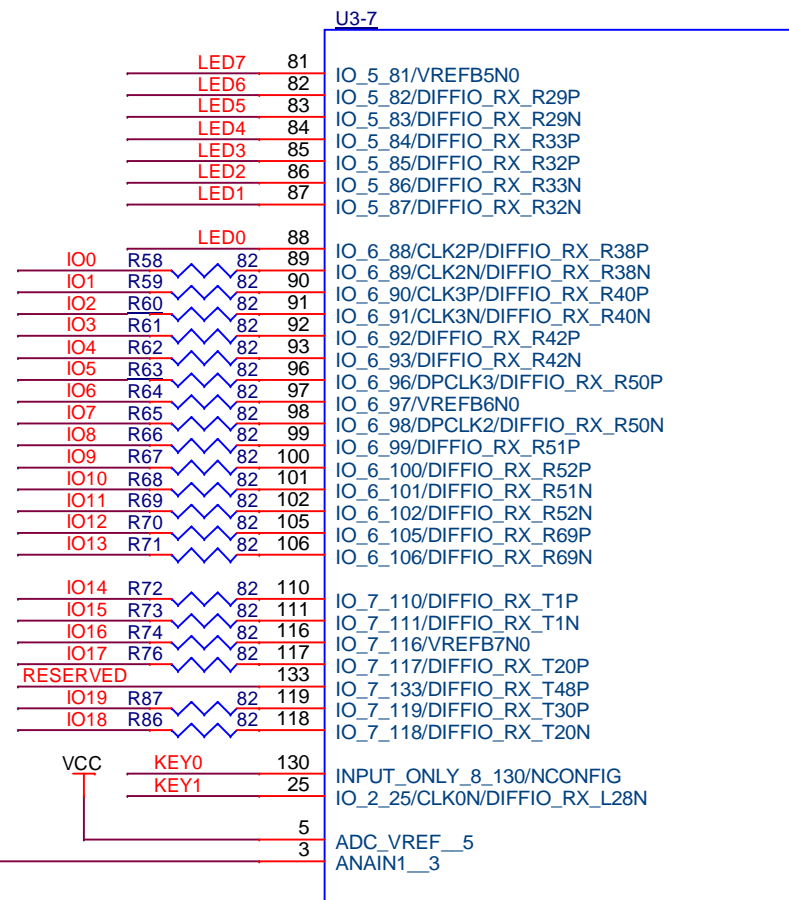
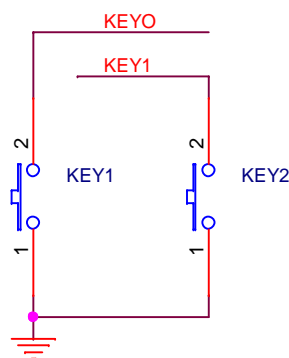
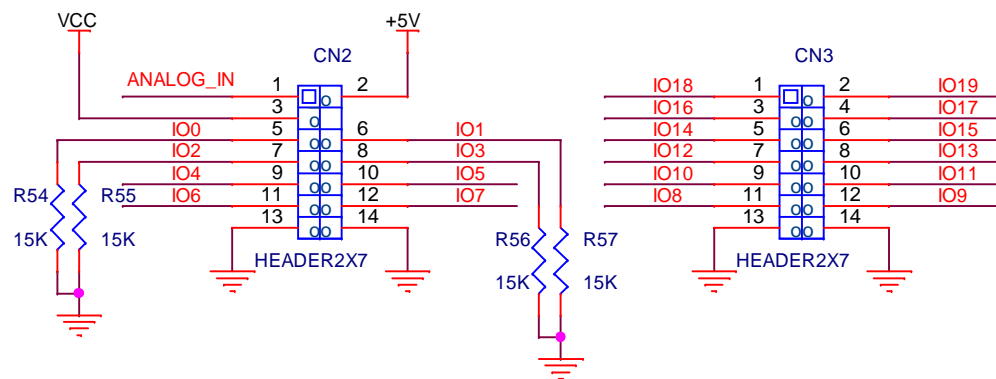
# SDR SDRAM INTERFACE



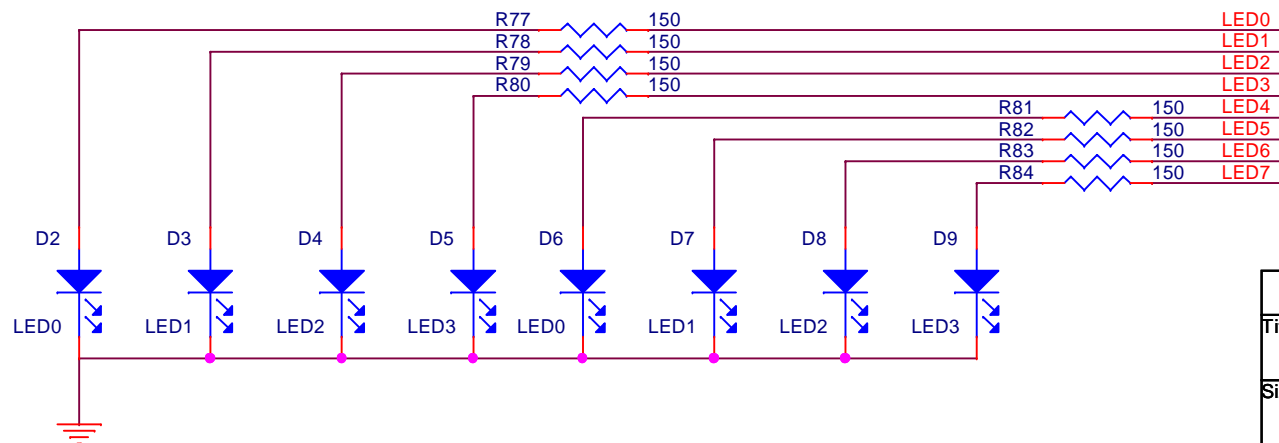
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## SHIELD CONNECTOR, KEYS & LEDS

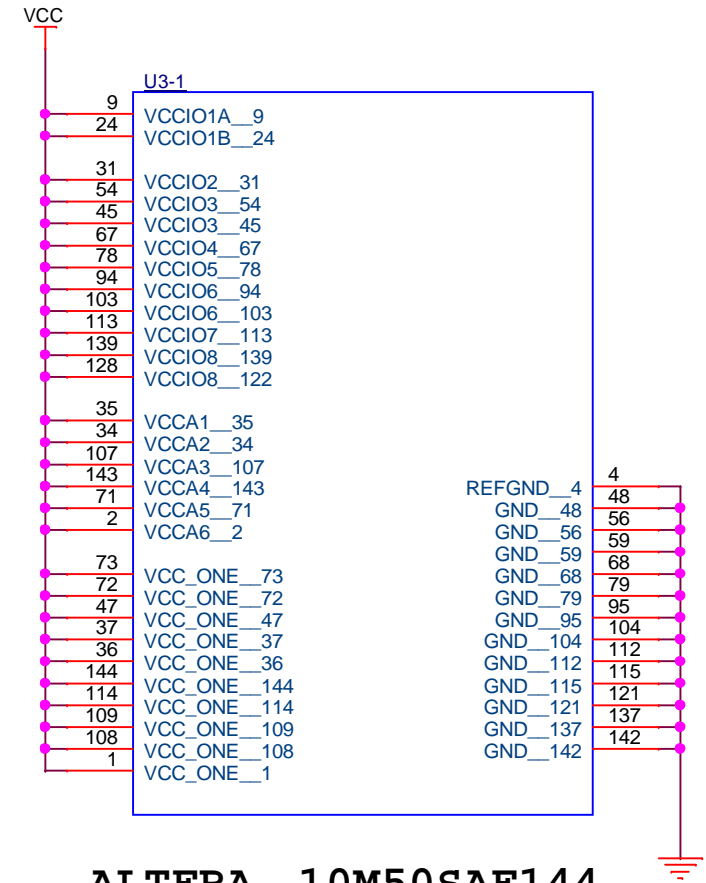
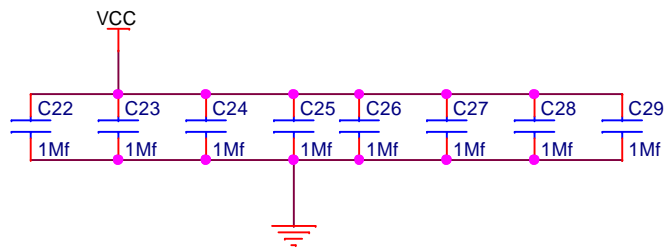
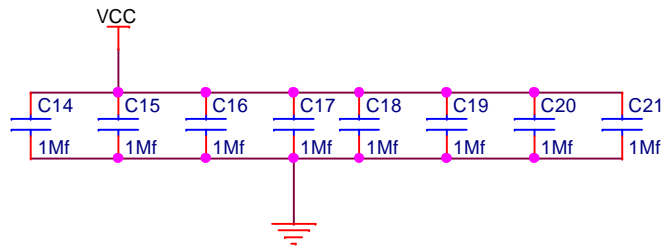
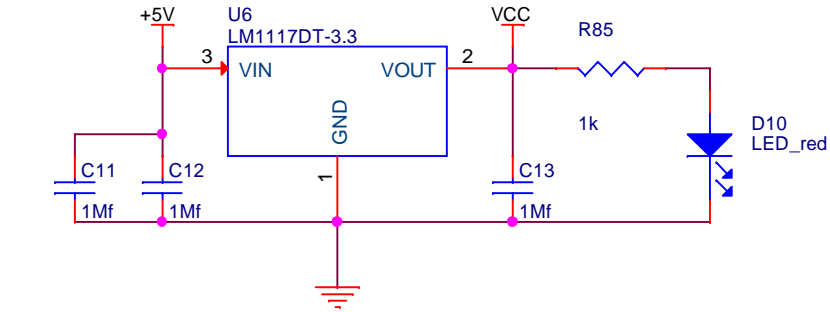


**ALTERA 10M50SAE144**



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# MAX10 POWERING



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