Politecnico di Torino

Microelectronic Systems

DLX Microprocessor: ALU

Master degree in Embedded Systems Engineering

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ALU

ALU is the core of all operations, it is collocated in the execution unit and elaborate two operands coming from the previous stage. It performs logical and arithmetic operations based on the instruction passed to it by the CU. ALU is also used to calculate memory addresses to perform DRAM accesses.

The operations that the ALU is able to do are:

- Addition and Subtraction. (Signed and Unsigned, with overflow detection)
- Logic Operations. (AND, OR, XOR)
- Comparison operations. $(=, \neq, >, <, \leq, \geq)$
- Shift Operations. (Left or Right, Logic or Arith)

Each of this operations are performed by a different unit that is part of ALU environment, described below.

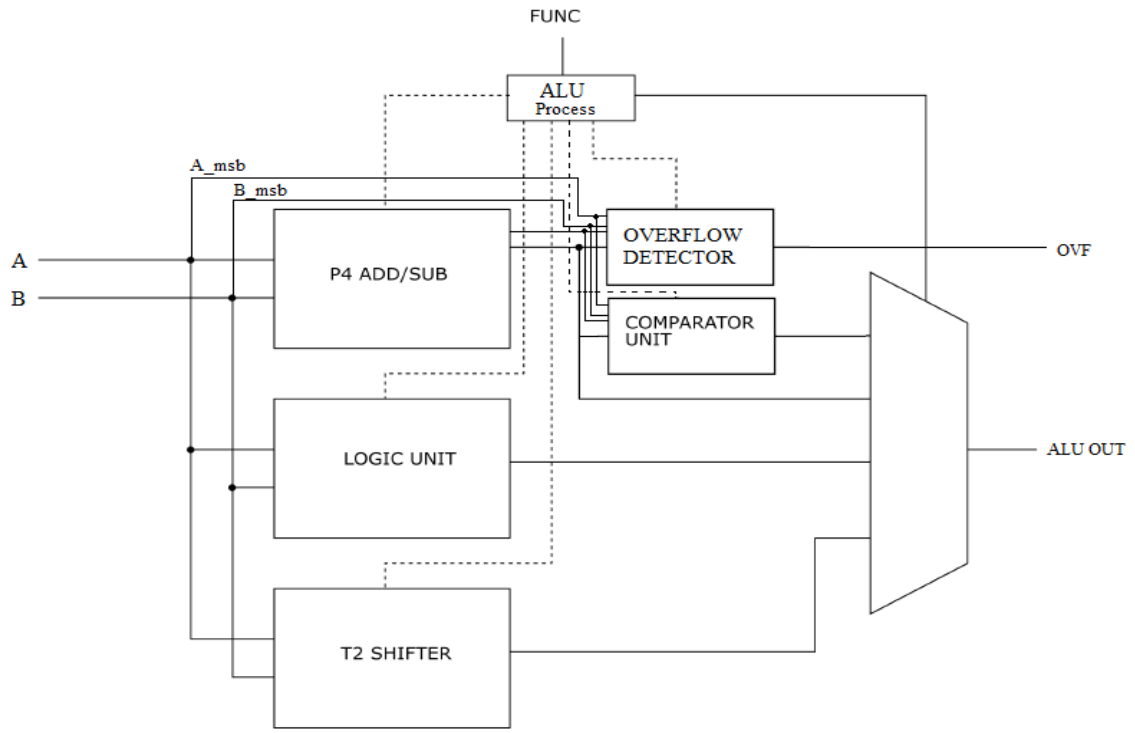

Figure 1: Schematic of the ALU.

Adder

The adder that we have inserted inside the ALU is that of P4 which uses a sparse tree carry-generator and 4-bit carry-select blocks to improve the performance over traditional adders.

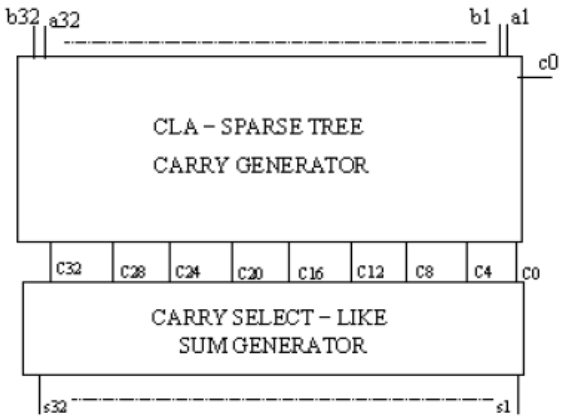

Figure 2: P4 Adder schematic.

This is a particular type of adder, 32-bit, which generates the carry every four bits. Each carry enters into a carry select adder which generates the corresponding output. The combination of all these outputs represents the final sum.
Inside, the carry select adder is made up of two RCAs, where one uses 0 and the other 1 as carry-in, while the carry that comes from the previous state is used to select one of these two sums.

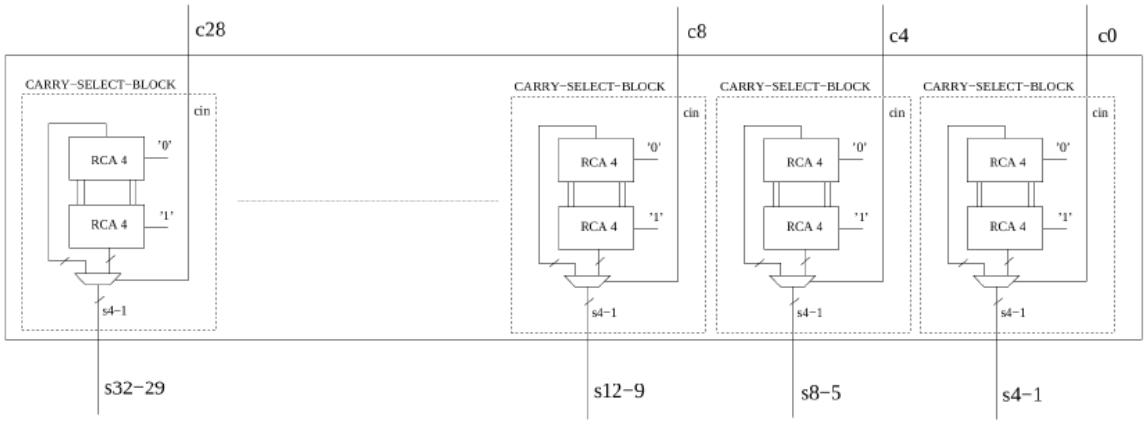

Figure 3: Carry Select Block.

The carry generator is based on the concept of generation and propagation.
A generation happens when a carry bit is generated by the sumof two bits, so they are both one.
A propagation happens when one of the two bits are 1 so that a carry can propagates through.
These values are calculated in the first step of the PG network.
After the PG network we have the carry generation (one every four PG block), this structure use two

types of blocks: PG that implements both the general generation and the general propagation and G that implements only the general generation.
Their organization can be seen in the figure below.

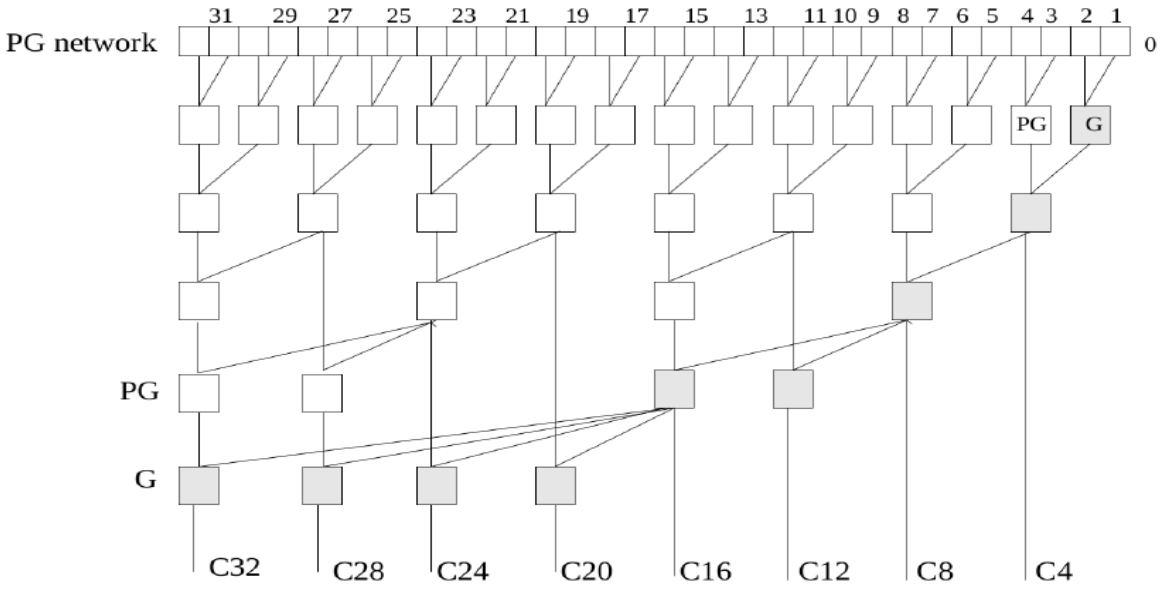

Figure 4: Carry Sparse-Tree.

In order to carry out the subtraction, a chain of XORs has been added between an input (B) and the carry-in.

Overflow Detection

The check on the presence or absence of the overflow is made on eight possible instructions: ADD, ADDI, ADDU, ADDUI, SUBS, SUBI, SUBU and SUBUI.
So we will have to analyze the cases of addition and subtraction, signed and unsigned.
The two cases must be distinguished since if we consider the signed they will use half of the maximum size for the data as it must be divided between positive and negative.

- The range that can be represented in the unsigned format is: between 4294967295 and 0.
- The range that can be represented in the signed format is: between +2147483647 and -2147483648.

The overflow is identified for signed in this way:

- ADD/ADDI : Cout XOR A(31) XOR B(31) XOR SUM(31)
- SUB/SUBI : NOT (Cout XOR A(31) XOR B(31) XOR SUM(31))

while for unsigned are:

- ADDU/ADDUI : Cout
- SUBU/SUBUI : NOT Cout

Logic

The Logic Unit derive from the UltraSPARC T2 that has two-level of combinational logic.
In this case, compared to the original of T2, only the AND, OR and XOR operations are acceptable.
For the reason described above, the logic has been made simpler.
Each bit of the input signals are input to 3 NAND gates with different combinations of that, each with a different additional signal (used to select the correct logic operation).
The second level performs a NAND between the outputs of the gates above, generating the output bits.

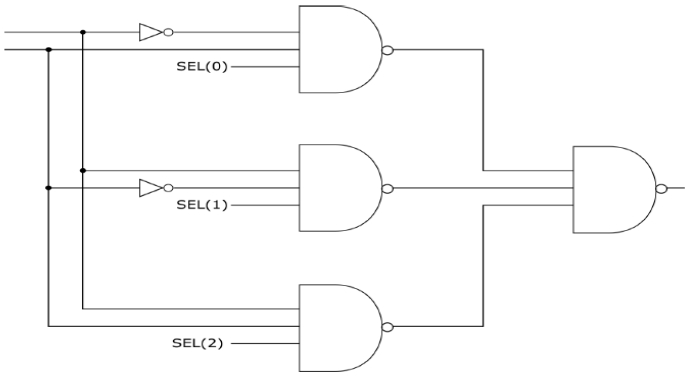

Figure 5: Schematic of 1 single bit in the Logic Unit.

Comparator

The comparison is performed after the subtraction of the two inputs, carried out by the adder P4.
The result of the subtraction and the carry-out are taken as input but to perform also signed operations then it is also necessary to have the msb value of the two inputs as input.
To check if the result is equal to zero, a first network of NOR gates is created and followed by an AND network but made with a tree diagram, thus obtaining a single bit that says whether or not it is equal to 0.

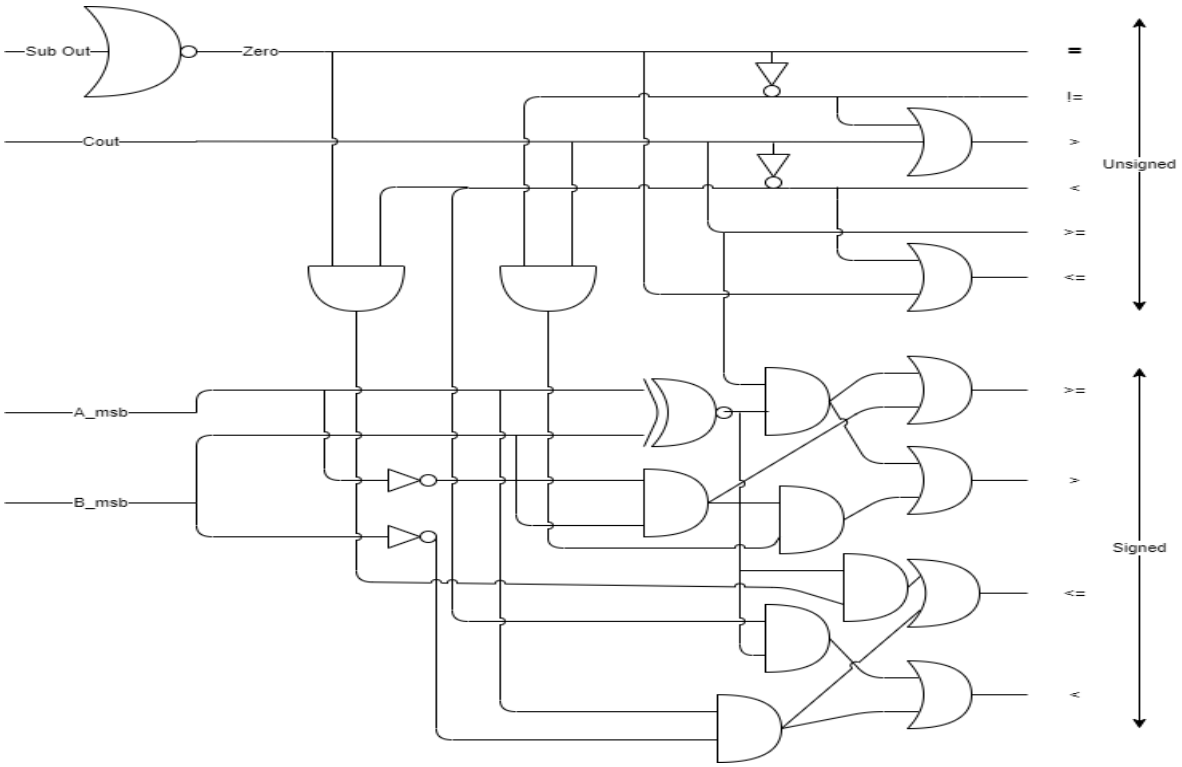

Figure 6: Schematic of the Comparator Unit.

Shifter

The Shifter is derived from the UltraSPARC T2 and is able to shift to the right or left or right arithmetic, based on the signal passed.
The shift operation is carried out following three successive phases.
The first phase generates 40-bit masks, shifting of multiples of 8 bits according to the type of shift (Left, Right and Right arithmetic).
The second phase acts as a coarse grain shift by choosing the right mask among those available, using as selector two bits of the second input of the unit.
At the end a fine grain shift translates back the operand to 32 bits using the last bits of the second input operand.

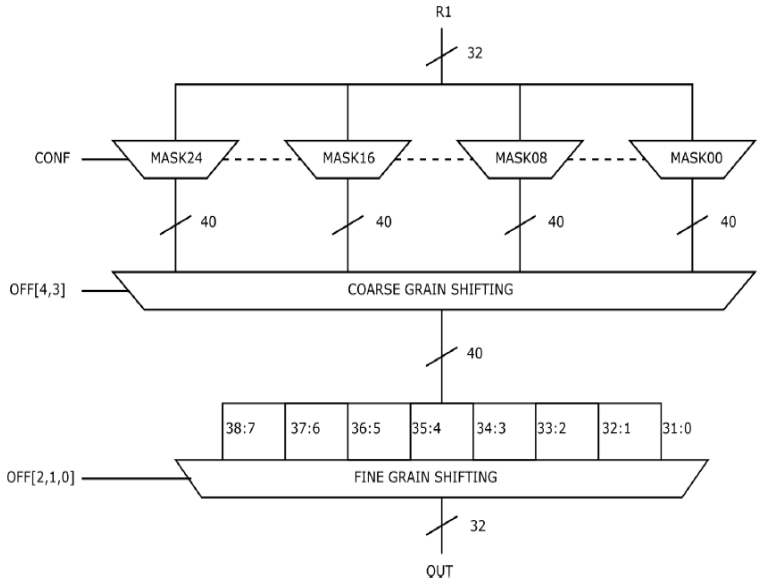

Figure 7: Schematic of the Shifter.