Experiment 3 – Function Generator

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***Abstract* – This document is Seyed Mohammad Amin Atyabi report on experiment 3 for Digital Logic Design Lab. In this experiment we are to create a function generator. Our Function Generator can create different waveforms with different frequencies and amplitude.**

***Keyword* – Function Generator, Frequency, Amplitude, Waveform, Rhomboid, Square, Triangle, Sine, Cosine, Reciprocal**

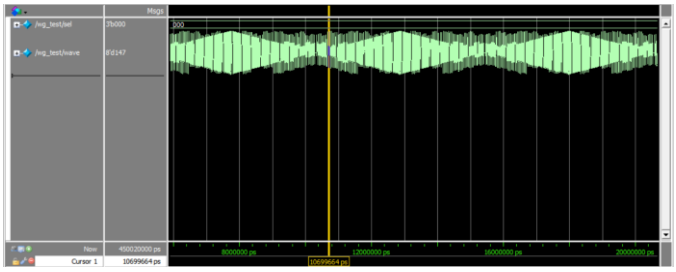
Introduction

A Function Generator is and electrical instrument that can create wide variety of waveforms with different frequencies and amplitude. In this experiment our Function Generator will create Square, Rhomboid, Reciprocal, Triangle, Full-wave rectified, Half-wave rectified, and Sinusoidally modulated square wave.

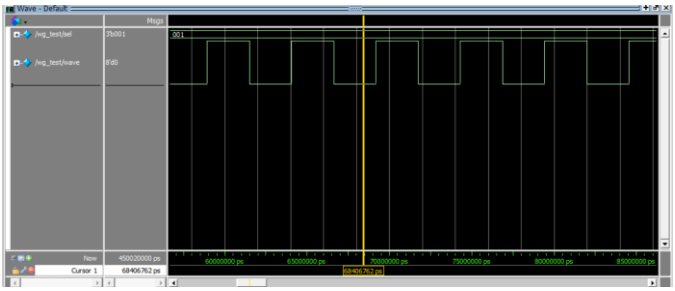
1. Waveform Generator

In this part we will create above mentioned waveforms with no frequency and amplitude adjustment. There is a counter attached to circuit in test bench to create a sequence of numbers for counter base waveforms and sine waveform. In next parts this counter will be inside circuit which will control frequency. Here are above mentioned waveforms simulated in ModelSim including DDS waveform.

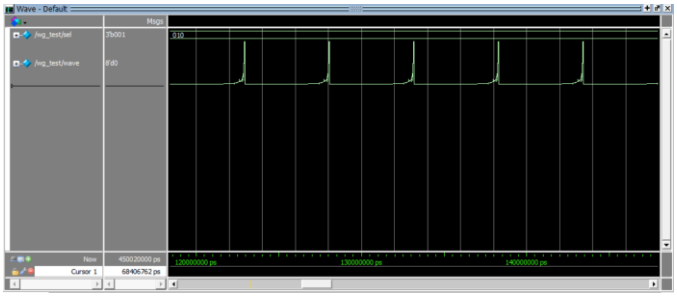
Rhomboid)



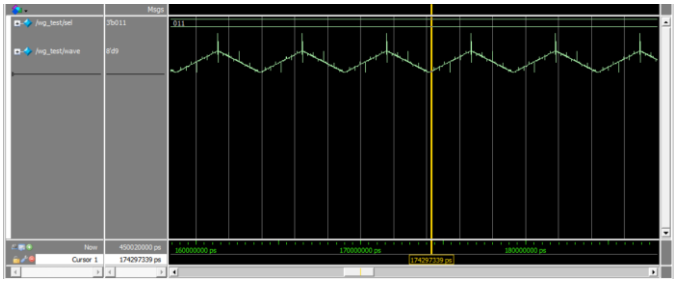
Square)



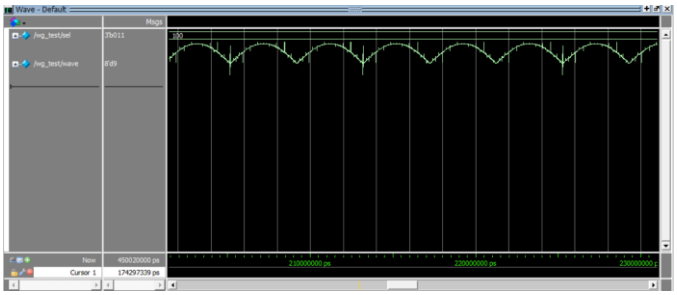
Reciprocal)



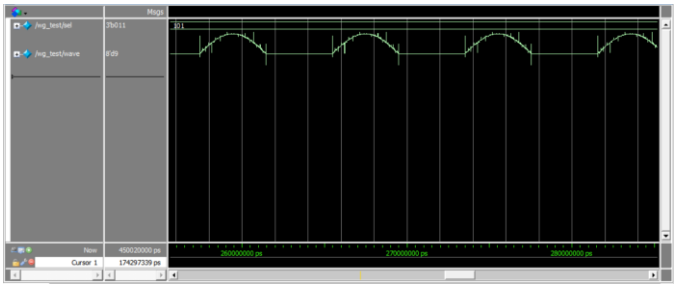
Triangle)



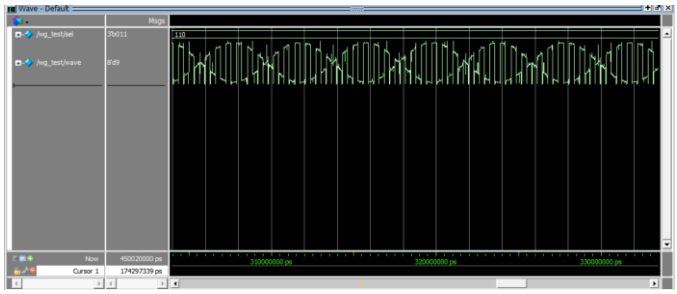
Full-wave rectified)



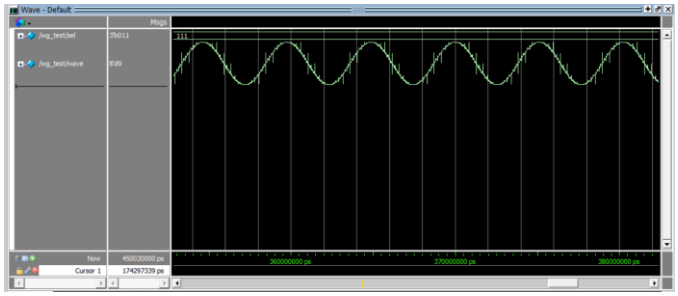
Half-wave rectified)



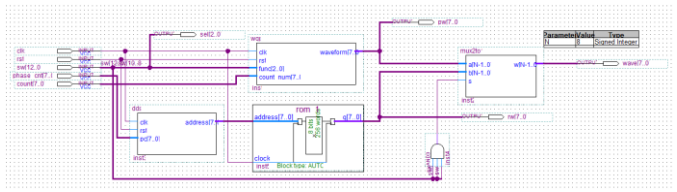
Sinusoidally modulated square wave)



DDS)



Final circuit)



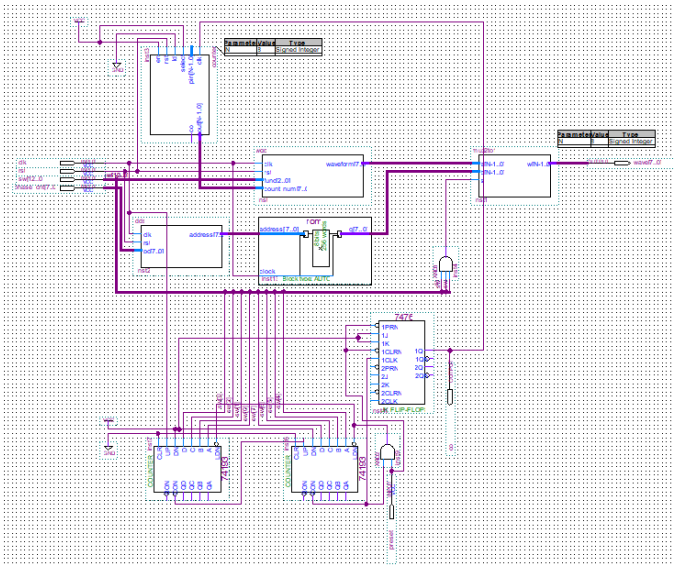
Synthesize summary)

Flow Summary	
Flow Status	Successful - Sat May 22 11:28:41 2021
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	wg
Top-level Entity Name	wg
Family	Cyclone IV E
Total logic elements	252 / 6,272 (4 %)
Total combinational functions	245 / 6,272 (4 %)
Dedicated logic registers	105 / 6,272 (2 %)
Total registers	105
Total pins	58 / 92 (63 %)
Total virtual pins	0
Total memory bits	2,048 / 276,480 (< 1 %)
Embedded Multiplier 9-bit elements	0 / 30 (0 %)
Total PLLs	0 / 2 (0 %)
Device	EP4CE6E22C6
Timing Models	Final

1. Frequency Selector

In this part we added frequency divider from experiment 1 to divide input clock frequency. So, the input clock of internal counter will have our desired frequency.

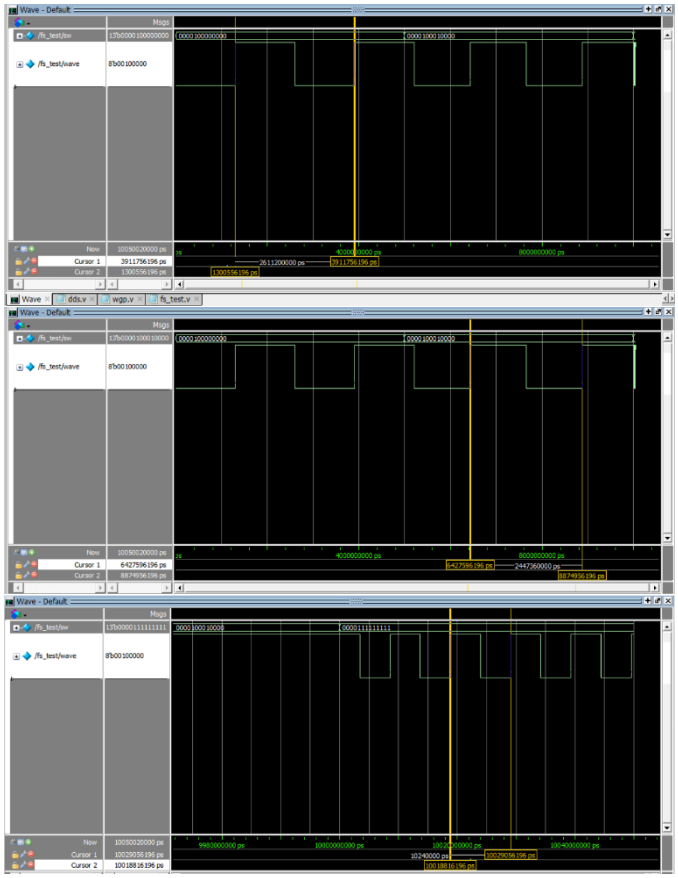
Final circuit)



Synthesize summary)

Flow Summary	
Flow Status	Successful - Sat May 22 13:41:49 2021
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	fs
Top-level Entity Name	fs
Family	Cyclone IV E
Total logic elements	292 / 6,272 (5 %)
Total combinational functions	291 / 6,272 (5 %)
Dedicated logic registers	114 / 6,272 (2 %)
Total registers	114
Total pins	33 / 92 (36 %)
Total virtual pins	0
Total memory bits	2,048 / 276,480 (< 1 %)
Embedded Multiplier 9-bit elements	0 / 30 (0 %)
Total PLLs	0 / 2 (0 %)
Device	EP4CE6E22C6
Timing Models	Final

SW[7:0] Frequency select on square waveform)



Phase_cntrl Frequency select for DDS waveform)