

Experiment 1 – Clock and Periodic Signal Generation

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Abstract— This document is Seyed Mohammad Amin Atyabi report on experiment 1 for digital logic design laboratory. In this experiment we will discuss about different method of clock generation (Ring Oscillator, LM555 Timer and Schmitt Trigger), Frequency divider and Baud Rate Generator for UART Serial Communication.

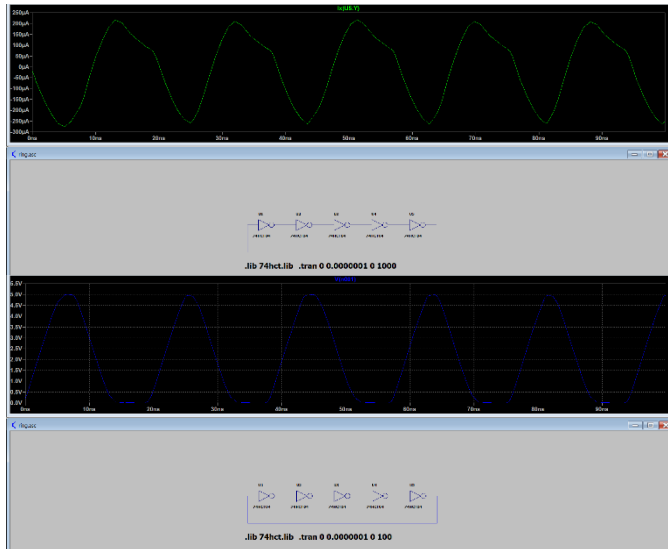
Keywords— Ring Oscillator, LM555, Schmitt Trigger, Frequency Divider, Baud Rate Generator for UART Serial Communication

INTRODUCTION

Most of digital circuits use a system called clock to work property and there are many methods to generate clock but we discuss about three of them in this experiment. Then we will design a Baud Rate Calculator for UART Serial Communication.

1. CLOCK GENERATION USING ICs AND ANALOG COMPONENTS

A. Ring Oscillator



By measuring two points time in wave form of ring oscillator we collect these data:

Time₁: 32 ns

Time₂: 51.3 ns

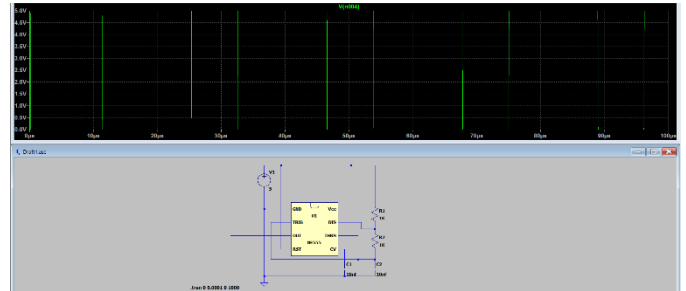
1. So, the time period of propagation delay of this chain will be 19.3 ns.
2. Using the delay formula:

$$2N \times Delay_{inv} = 19.3ns$$

$$Delay_{inv} = \frac{19.3ns}{2 \times 5}$$

$$Delay_{inv} = 1.93ns$$

B. LM555 Timer



In LTspice software LM555 IC named NE555.

R₂ = 1KΩ)

$$T = 0.693 \times 3 \times 10^3 \times 10 \times 10^{-9} = 20ns$$

$$F = 50KHz$$

$$Duty\ Cycle \cong 66\%$$

R₂ = 10KΩ)

$$T = 0.693 \times 21 \times 10^3 \times 10 \times 10^{-9} = 145ns$$

$$F = 6.9KHz$$

$$Duty\ Cycle \cong 52.38\%$$

R₂ = 100KΩ)

$$T = 0.693 \times 201 \times 10^3 \times 10 \times 10^{-9} = 1.4ms$$

$$F = 714Hz$$

$$Duty\ Cycle \cong 50.25\%$$

C. Schmitt Trigger Oscillator



For every resistor value we calculate time from wave form, then calculate frequency to find α value.

R = 470Ω)

$$Time_1: 22.7\mu s$$

$$Time_2: 26.3\mu s$$

$$T = 3.6\mu s$$

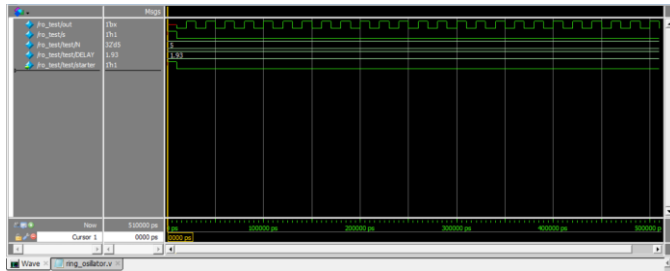
$$F = 278KHz$$

$$\alpha = 1.3$$

$R = 1K\Omega$
 $Time_1: 23.7\mu s$
 $Time_2: 30.9\mu s$
 $T = 7.2\mu s$ $F = 139KHz$
 $\alpha = 1.39$
 $R = 2.2K\Omega$
 $Time_1: 19.9\mu s$
 $Time_2: 35.2\mu s$
 $T = 15.2\mu s$ $F = 65.8KHz$
 $\alpha = 1.45$

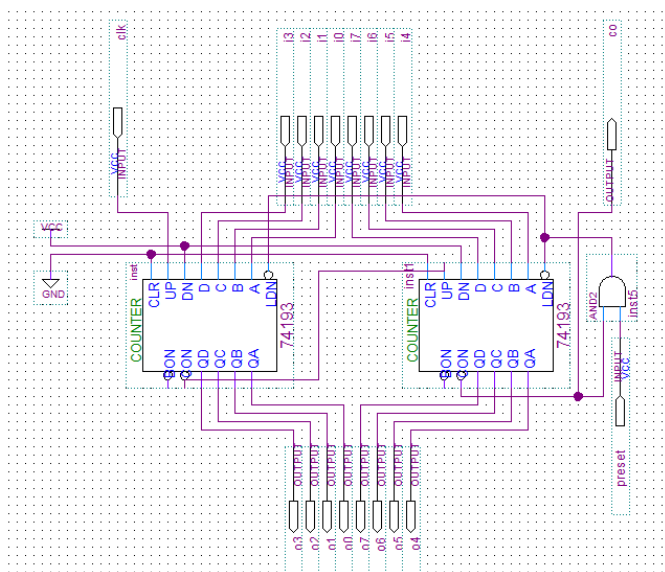
2. FPGA DESIGN

A. Ring Oscillator



We chose 5 as number of inverter gates and 1.93 as delay of each gate. Also, we generate a starter signal to initiate the chain, the time value of starter signal is $N \times \text{Delay}_{\text{inv}}$ witch in our case is 9.65ns.

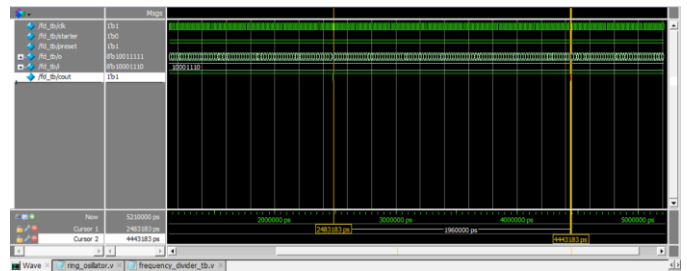
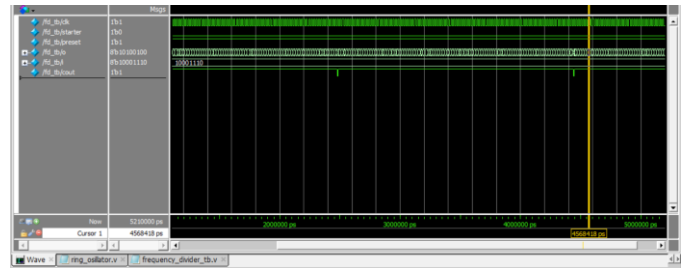
B. Synchronous Counter as a Frequency Divider



We designed the frequency divider using 74193 IC in Quartus program. Then synthesize the schematic to create Verilog description and timing files to simulate the circuit.

The preset mechanism helps us to indicate when do circuit starts to load our manual values to divide frequency.

By input value $(10001110)_2$ as input to circuit $(255_{10} - 113_{10} = 142_{10} = 10001110_2)$ we have a modulo 113 frequency divider.



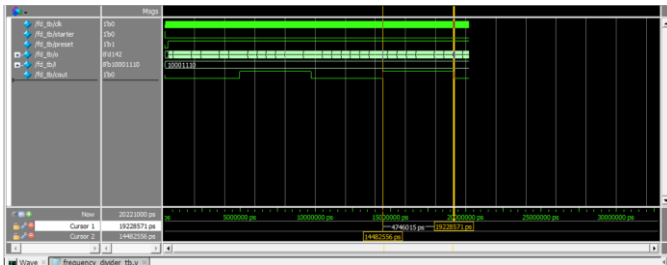
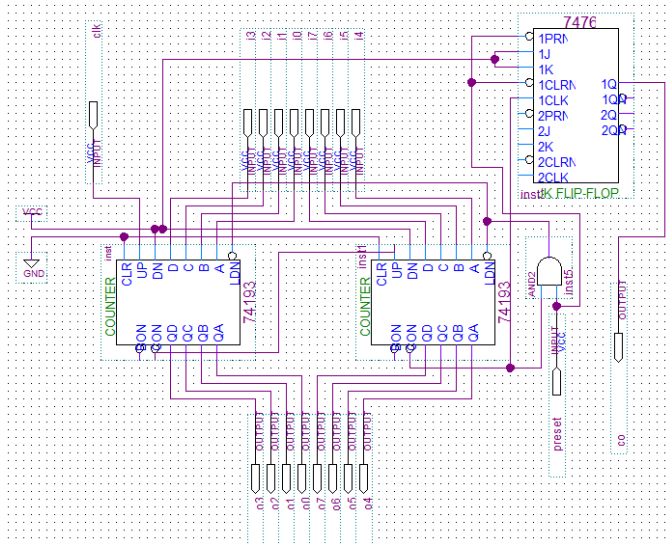
In simulation I find out the clock speed is too high for this circuit so I had to lower the frequency of clock by adding more not gate and increase time delay of each not gate. In this simulation I have 7 inverter gates with delay of 3ns, So the frequency of clock will be 23.8MHz.

By measuring two points of frequency divider where we have carry out, below data collected:

$Time_1: 4985355ps$
 $Time_2: 39731355ps$
 $T = 4746000ps$
 $F = 210.7KHz$

So, by dividing above frequencies $\left(\frac{23.8MHz}{210.7KHz}\right)$ we have $\cong 113$ ratio witch we expect.

C. T Flip-Flop



Then we create a T-Flip-Flop using a JK-Flip-Flop to make frequency divider duty cycle 50%.

2. BAUD RATE GENERATOR FOR UART SERIAL COMMUNICATION

A. Automatic Baud Rate Generator

