Experiment 2 – Clock Adjusting and Monitoring

Seyed Mohammad Amin Atyabi

810198559

***Abstract* – This document is Seyed Mohammad Amin Atyabi report on experiment 2 for Digital Logic Design Lab. In this experiment we want to validated, regulate and correct the clock of circuit. We will use Frequency Regulator module to regulate clock frequency, Clock Monitoring module to validate clock and Noise Eliminator module to correct clock.**

***Keywords* – Frequency Regulator, Nosie Eliminator, Clock Monitoring, Clock Adjusting, FPGA**

Introduction

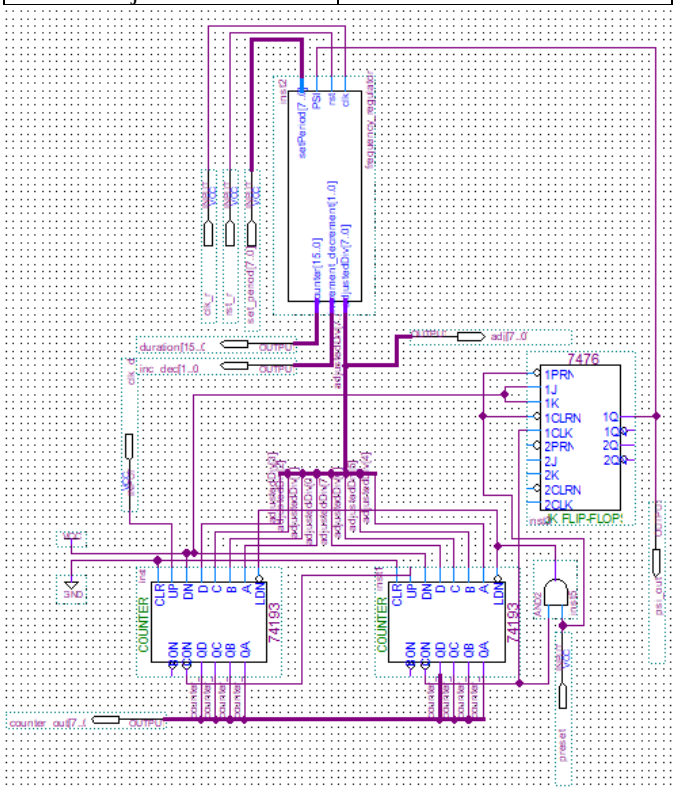
Most of digital circuits use clock to work properly. As we learned how to create the clock signal, we need to verify this signal and correct it in case of interruption to make sure our system works properly.

1. Clock Adjusting Unit

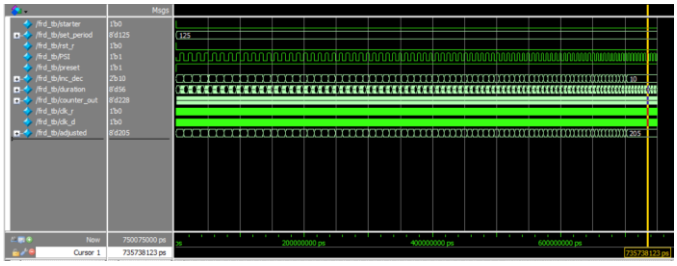
This module is responsible for dividing frequency in the way that meets our expectations.

After creating and synthesis the circuit we tested the circuit and fill the table below.

Final Frequency	200Khz
adjustedDiv	205



Flow Summary	
Flow Status	Successful - Tue May 04 14:40:34 2021
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	frequency_rd
Top-level Entity Name	frequency_rd
Family	Cyclone IV E
Total logic elements	117 / 6,272 (2 %)
Total combinational functions	117 / 6,272 (2 %)
Dedicated logic registers	34 / 6,272 (< 1 %)
Total registers	34
Total pins	47 / 92 (51 %)
Total virtual pins	0
Total memory bits	0 / 276,480 (0 %)
Embedded Multiplier 9-bit elements	0 / 30 (0 %)
Total PLLs	0 / 2 (0 %)
Device	EP4CE6E22C6
Timing Models	Final



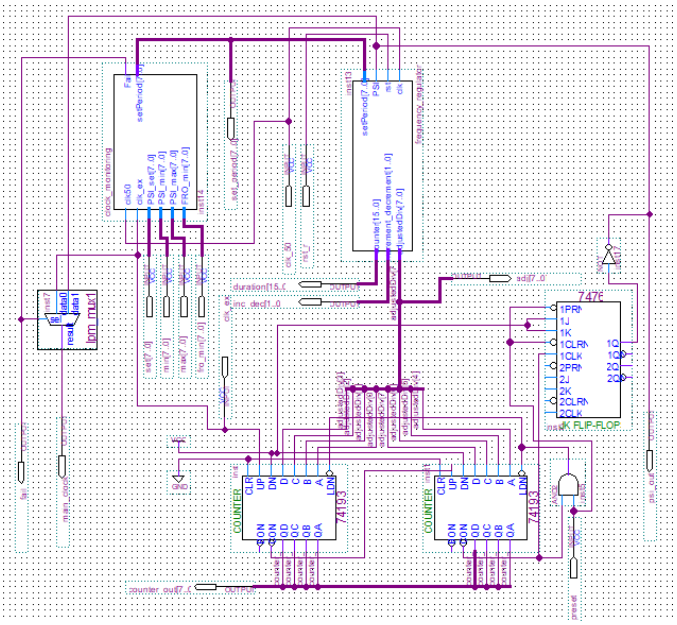
As we can see in the wave form, adjustedDiv signal keep changing until it reached setPeriod desired frequency.

2. Clock Monitoring Unit

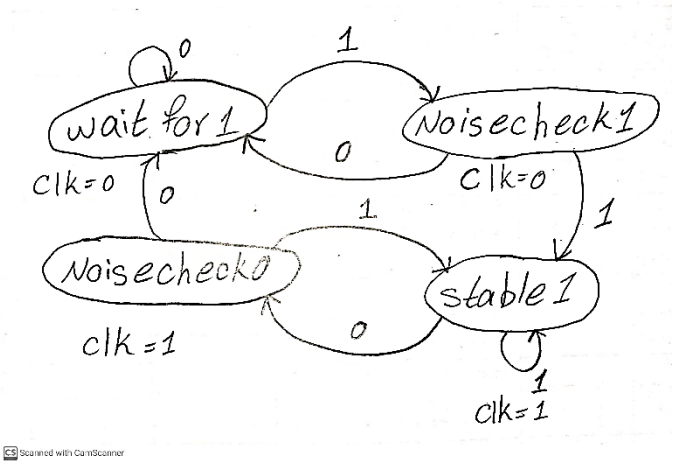
This module will keep the input setPSI in bounded range and validate the clock signal to check if it is proper for system or not.

To validate the clock signal, we use 50MHz and external clock ratio.

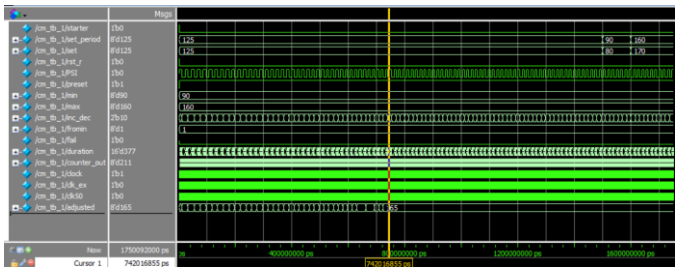
Flow Summary	
Flow Status	Successful - Tue May 04 15:35:53 2021
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	clock_monitoring
Top-level Entity Name	clock_monitoring
Family	Cyclone IV E
Total logic elements	97 / 6,272 (2 %)
Total combinational functions	96 / 6,272 (2 %)
Dedicated logic registers	18 / 6,272 (< 1 %)
Total registers	18
Total pins	43 / 92 (47 %)
Total virtual pins	0
Total memory bits	0 / 276,480 (0 %)
Embedded Multiplier 9-bit elements	0 / 30 (0 %)
Total PLLs	0 / 2 (0 %)
Device	EP4CE6E22C6
Timing Models	Final



3. Noise Eliminator Unit



Scenario 1)



Scenario 2)