# Experiment 4 – Integrated System

Seyed Mohammad Amin Atyabi

810198559

***Abstract*** **– This document is Seyed Mohammad Amin Atyabi report on experiment 3 for Digital Logic Design Lab. In this experiment we are to create a frequency multiplier and exponential accelerator and a wrapper for this module.**

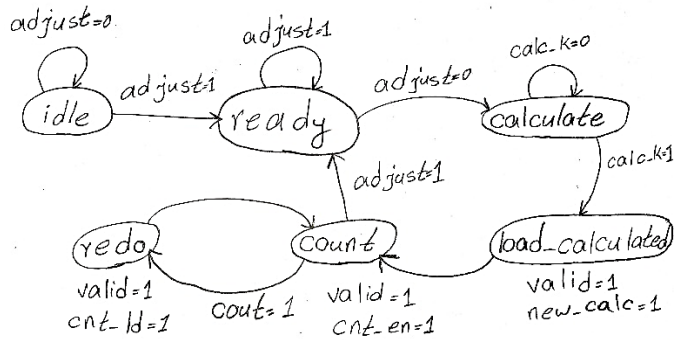
***Keyword*** **– Frequency Multiplier, Exponential Accelerator, SOC, Wrapper, Integrated Circuit**

## I. Introduction

System on Chip is an integrated circuit that integrates multiple components including digital, analog, hardware and software programs all in a single chip. The main core of SoC is a processor that handles different computational tasks within the system. In addition to the processor, the system includes a memory, Input/Output ports and accelerators. Because accelerators are responsible for a single job, they can work with higher frequency than main processor. In this experiment we are about to create an exponential accelerator and a frequency multiplier to boost the frequency for our accelerator.

## II. Frequency Multiplier

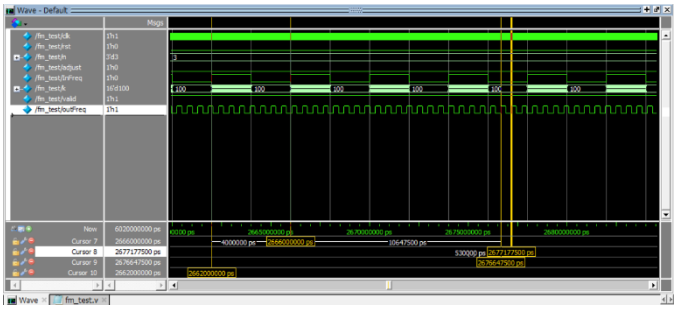
*State Diagram)*




*n = 1)*

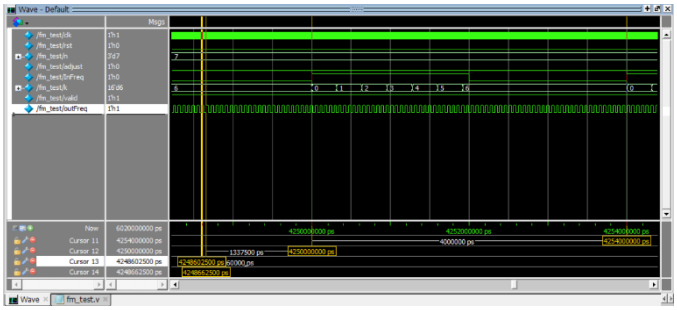
InFreq frequency = 250 KHz
outFreq frequency ≈ 492 KHz

*n = 3)*



InFreq frequency = 250 KHz
outFreq frequency ≈ 1.88 MHz

*n = 7)*

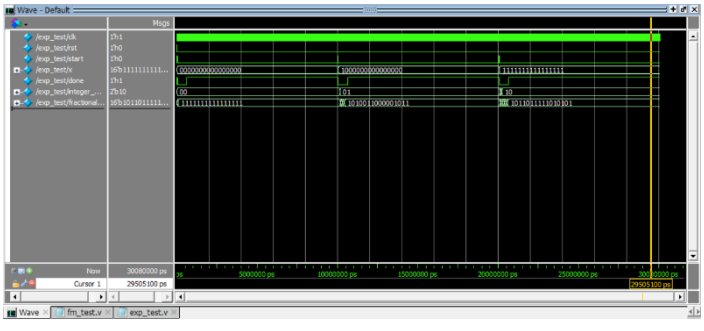


InFreq frequency = 250 KHz
outFreq frequency ≈ 16.6 MHz

## III. Exponential Accelerator

### 1. Exponential Engine

*Waveform)*



*Synthesize Report)*

| Flow Summary | |
|---|---|
| Flow Status | Successful - Fri Jun 18 17:42:43 2021 |
| Quartus II 64-Bit Version | 13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition |
| Revision Name | exponential |
| Top-level Entity Name | exponential |
| Family | Cyclone IV E |
| Total logic elements | 102 / 6,272 ( 2 % ) |
| Total combinational functions | 100 / 6,272 ( 2 % ) |
| Dedicated logic registers | 60 / 6,272 ( < 1 % ) |
| Total registers | 60 |
| Total pins | 38 / 92 ( 41 % ) |
| Total virtual pins | 0 |
| Total memory bits | 0 / 276,480 ( 0 % ) |
| Embedded Multiplier 9-bit elements | 2 / 30 ( 7 % ) |
| Total PLLs | 0 / 2 ( 0 % ) |
| Device | EP4CE6E22C6 |
| Timing Models | Final |

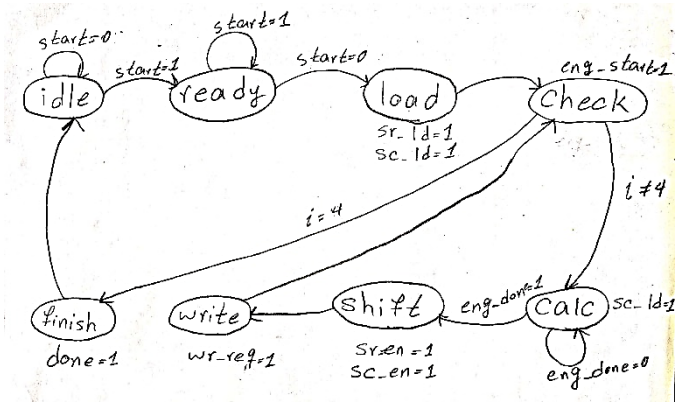
*Maximum Frequency)*

| Slow 1200mV 85C Model Fmax Summary | | | | |
|---|---|---|---|---|
| | Fmax | Restricted Fmax | Clock Name | Note |
| 1 | 162.95 MHz | 162.95 MHz | clk | |

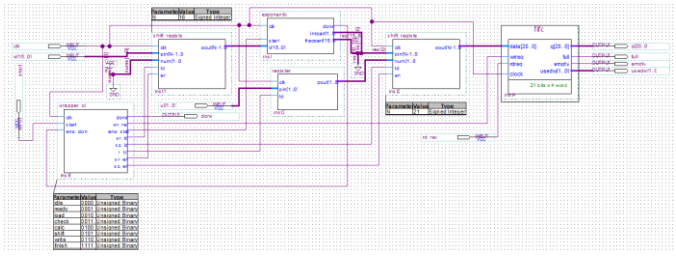
Maximum Frequency = 162.95 MHz

2. Exponential Accelerator Wrapper

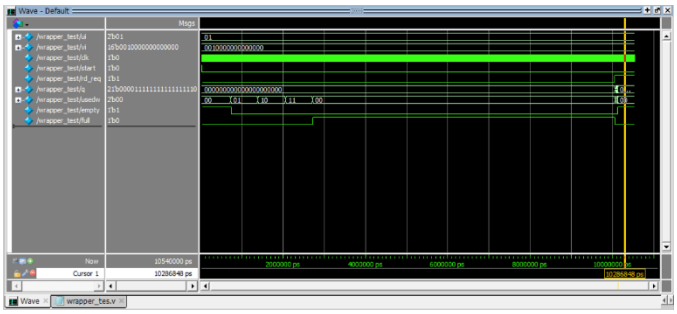
*State Diagram)*




*Final Circuit)*



*Wave form)*



*Synthesize Report)*

| Flow Summary | |
|---|---|
| Flow Status | Successful - Sat Jun 19 12:41:30 2021 |
| Quartus II 64-Bit Version | 13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition |
| Revision Name | wrapper |
| Top-level Entity Name | wrapper |
| Family | Cyclone IV E |
| Total logic elements | 194 / 6,272 ( 3 % ) |
| Total combinational functions | 186 / 6,272 ( 3 % ) |
| Dedicated logic registers | 118 / 6,272 ( 2 % ) |
| Total registers | 118 |
| Total pins | 47 / 92 ( 51 % ) |
| Total virtual pins | 0 |
| Total memory bits | 84 / 276,480 ( < 1 % ) |
| Embedded Multiplier 9-bit elements | 2 / 30 ( 7 % ) |
| Total PLLs | 0 / 2 ( 0 % ) |
| Device | EP4CE6E22C6 |
| Timing Models | Final |

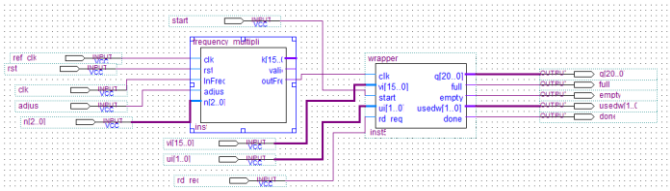
*Maximum Frequency)*

| Slow 1200mV 85C Model Fmax Summary | | | | |
|---|---|---|---|---|
| | Fmax | Restricted Fmax | Clock Name | Note |
| 1 | 160.72 MHz | 160.72 MHz | clk | |

Maximum Frequency = 160.72 MHz

## IV. Frequency Multiplier

*Final Circuit)*



*Synthesize Summary)*

| Flow Summary | |
|---|---|
| Flow Status | Successful - Sat Jun 19 15:20:52 2021 |
| Quartus II 64-Bit Version | 13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition |
| Revision Name | integrated |
| Top-level Entity Name | integrated |
| Family | Cyclone IV E |
| Total logic elements | 321 / 6,272 ( 5 % ) |
| Total combinational functions | 312 / 6,272 ( 5 % ) |
| Dedicated logic registers | 172 / 6,272 ( 3 % ) |
| Total registers | 172 |
| Total pins | 53 / 92 ( 58 % ) |
| Total virtual pins | 0 |
| Total memory bits | 84 / 276,480 ( < 1 % ) |
| Embedded Multiplier 9-bit elements | 2 / 30 ( 7 % ) |
| Total PLLs | 0 / 2 ( 0 % ) |
| Device | EP4CE6E22C6 |
| Timing Models | Final |

*Wave Form)*