Group 7 Wednesday 2nd progress

This Wednesday, we finalized our concept of the FSM that will drive the controller. We are working on programming the FSM in VHDL. We also made an overview of all the signals that are passed between different subsystems. The memory is finished and tested using a post simulation. We made various supporting functions such as `display` and `hex2bin`. Lastly, we are making progress on the datapath.