Instruction	Need	Give
mem ld:	address(8 downto 0) (c -> m)	data out(31 downto 0) (m -> d)
	rd = 1 (c -> m)	
	wr = 0 (c -> m)	
	b = 0 (c -> m)	
	%rd(31 downto 0) (c -> d)	
	Cmux = 1 (c -> d)	
	Amux = 0 (c -> d)	
st:	address (c -> m)	
	rd = 0 (c -> m)	
	wr = 1 (c -> m)	
	b = 0 (c -> m)	
	dataIn(31 downto 0) (d -> m)	
	Cmux = 0 (c -> d)	
	Amux = 1 (c -> d)	
	%rs(31 downto 0) (c -> d)	
ldb:	address(8 downto 0) (c -> m)	data out(31 downto 0) (m -> d)
	rd = 1 (c -> m)	
	wr = 0 (c -> m)	
	b = 1 (c -> m)	
	%rd(31 downto 0) (c -> d)	
	Cmux = 1 (c -> d)	
	Amux = 0 (c -> d)	
stb:	address (c -> m)	
	rd = 0 (c -> m)	
	wr = 1 (c -> m)	
	b = 1 (c -> m)	
	dataIn(31 downto 0) (d -> m)	
	Cmux = 0 (c -> d)	
	Amux = 1 (c -> d)	
	%rs(31 downto 0) (c -> d)	
arth r to num		
AND	ALU = 000 (c->d)	
	rr = 1 (d->c)	
	rs (c->d)	
	rd (c->d)	
OR	ALU = 001 (c->d)	
	rr = 1 (d->c)	
	rs (c->d)	
	rd (c->d)	
ADD	ALU = 010 (c->d)	
	rr = 1 (d->c)	
	rs (c->d)	
	rd (c->d)	
SHIFT	ALU = 011 (c->d)	
	rr = 1 (d->c)	
	rs (c->d)	
	rd (c->d)	
ANDcc	ALU = 100 (c->d)	

	rr = 1 (d->c)
	rs (c->d)
	rd (c->d)
ORcc	ALU = 101 (c->d)
	rr = 1 (d->c)
	rs (c->d)
	rd (c->d)
ADDcc	ALU = 110 (c->d)
	rr = 1(d->c)
	rs (c->d)
	rd (c->d)
AND	ALU = 000 (c->d)
	rr = 0 (d->c)
	SIMM10(c->d)
	rd (c->d)
OR	ALU = 001 (c->d)
	rr = 0 (d->c)
	SIMM10(c->d)
	rd (c->d)
ADD	ALU = 010 (c->d)
	rr = 0 (d->c)
	SIMM10(c->d)
	rd (c->d)
SHIFT	ALU = 011 (c->d)
	rr = 0 (d->c)
	SIMM10(c->d)
	rd (c->d)
ANDcc	ALU = 100 (c->d)
	rr = 0 (d->c)
	SIMM10(c->d)
	rd (c->d)
ORcc	ALU = 101 (c->d)
	rr = 0 (d->c)
	SIMM10(c->d)
	rd (c->d)
ADDcc	ALU = 110 (c->d)
	rr = 0 (d->c)
	SIMM10(c->d)
	rd (c->d)
display	rs (c->d)
	IO=01 (c->d)
readIO	rd (c->d)
	IO=10 (c->d)