CE-210 Digital Systems I
Solution of Assignment 3

1. Apply the combining theorem (T10-L) to

Y = A . B' . F' + A . B . F'

Let a = A . F' and b = B, therefore

Y = A . F'

2. Apply the covering theorem (T9-L) to

Y = A' . G' . H . E . C + G' . E

Let a = G' . E and b = A' . H . C, therefore

Y = G' . E

3. Apply the distributivity theorem (T8-L) to Y = A . C' . D . E . (B' + F' + G') to obtain a SOP expression for Y.

Y = A . C' . D . E . B' + A . C' . D . E. F' + A . C' . D . E . G'

4. Prove the **elimination** theorem shown below: (Use algebraic techniques)

X + X' . Y = X + Y

Apply T8-R: X + X' . Y = (X + X') . (X + Y)

Apply T5-L: (X + X') . (X + Y) = 1 . (X + Y)

Apply T1-R: 1 . (X + Y) = X + Y

5. Apply DeMorgan's theorem(s) to Y as many times as you need to remove all primed parentheses:

Y = ((A + B . C')' . ((A . D')'+ B))'

Let M = (A + B . C')' and N = (A . D')'+ B)

Y = (M . N)' = M' + N'

M' = ((A + B . C')')' = A + B . C'

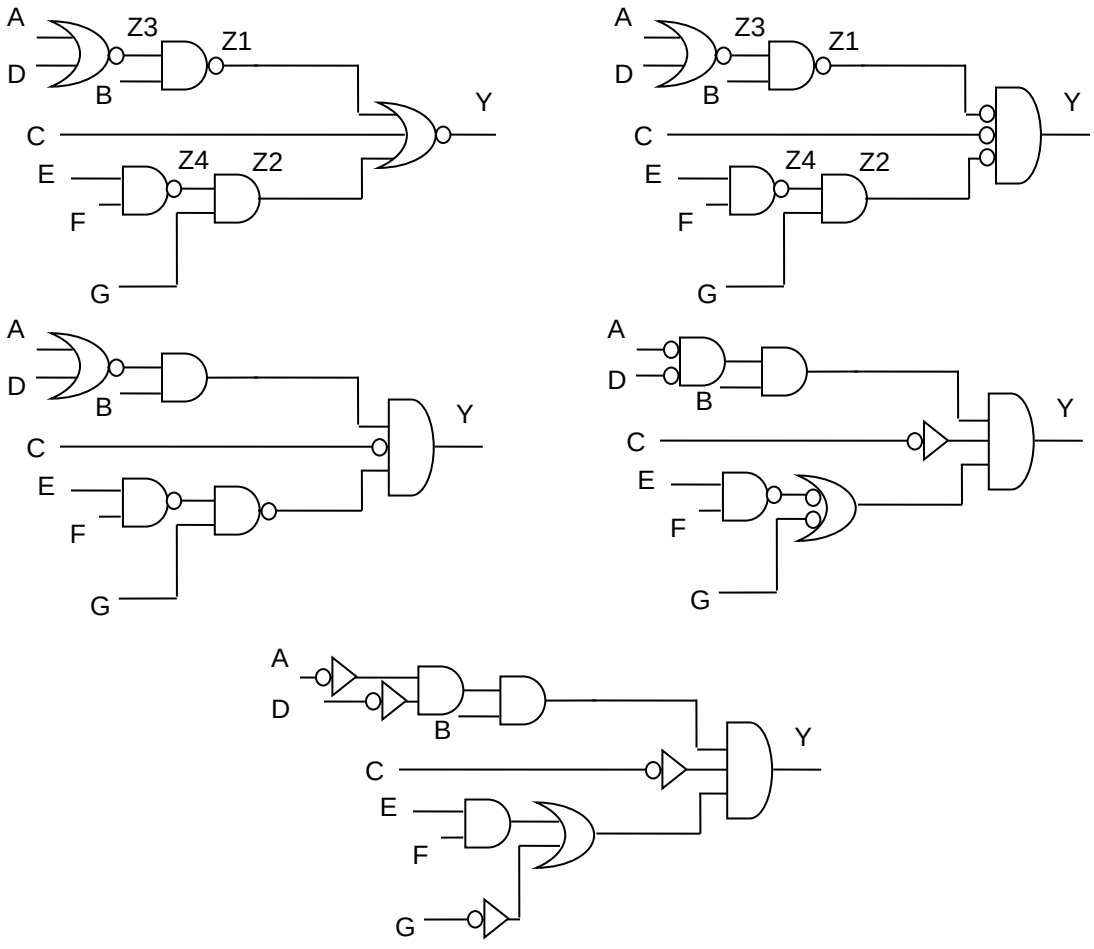
N' = ((A . D')'+ B))' = ((A . D')')' . B' = A . D' . B'

Y = M ' + N' = A + B . C' + A . D' . B'

According to T9-L: A + A . D' . B' = A

Therefore, Y = A + B . C'

6. Apply DeMorgan's theorem(s) to the following circuit to absorb all inversion bubbles at the output of gates, and eventually come up with a circuit with AND and OR gates only. Inverters are only allowed to complement the input variables, if needed. Do not simplify the circuit. Do not change the circuit topology either. Show your work.



7. Derive an exact logic expression for output Y of the above circuit **before** any changes are made to the circuit.

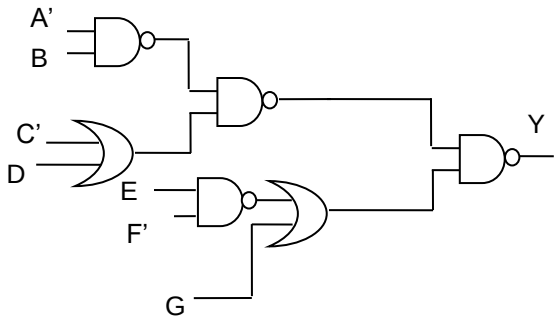
Y = (Z1 + C + Z2)' Z1 = (B . Z3)' Z3 = (A + D)' Z1 = (B . (A + D)')' Z2 = G . Z4 Z4 = (E . F)'

Z2 = G . (E . F)' Substitute for Z1and Z2:

Y = ((B . (A + D)')' + C + G . (E . F)')'

8. Obtain an exact logic circuit for Y shown below:

y = (((A' . B)' . (C' + D))' . ((E . F')' + G))'



9. Apply the principle of duality to:

X . Y + X' . Z + Y . Z = X . Y + X' . Z

(X + Y) . (X' + Z) . (Y + Z) = (X + Y) . (X' + Z)

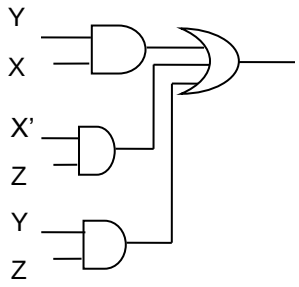
Determine the number of gates that we need to realize each side of the above expression. What is the type of each gate? How many inputs does each gate need?

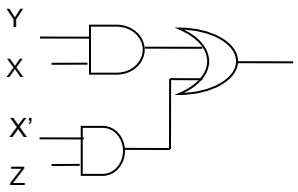
X . Y + X' . Z + Y . Z = X . Y + X' . Z

Left: Three 2-input AND + One 3-input OR

Right: Two 2-input AND + One 2-input OR

Draw two logic circuits to realize these two logic expressions.





Which side needs less hardware? **Right**

10. Use the theorems of switching algebra shown in Table 2 of Chapter 3 to prove the **consensus** theorem:

(A + B) . (A' + C) = (A + B) . (A' + C) . (B + C) (1)

T10 –R: B + C = (B + C + A) . (B + C + A')

Sub for (B + C) in (1):

Right side: (A + B) . (A' + C) . (A + B + C) . (A' + B + C) =

(A + B) . (A + B + C) . (A' + C) . (A' + B + C)

= A + B (Covering) = A' + C (Covering)

= (A + B) . (A' + C)

11. Obtain the truth table, the off-set maxterm list (shorthand notation) and the canonical POS of Y (A, B, C) = Σ (0, 4, 6).

Row	A B C	Y
0	0 0 0	1
1	0 0 1	0
2	0 1 0	0
3	0 1 1	0
4	1 0 0	1
5	1 0 1	0
6	1 1 0	1
7	1 1 1	0

$Y(A, B, C) = \prod (1, 2, 3, 5, 7)$

$Y = (A + B + C') \cdot (A + B' + C) \cdot (A + B' + C') \cdot (A' + B + C') \cdot (A' + B' + C')$

12. Obtain the truth table, the canonical SOP and the canonical POS of $Z(A, B, C) = A' \cdot C' + B' \cdot C'$

Row	A B C	Z
0	0 0 0	1
1	0 0 1	0
2	0 1 0	1
3	0 1 1	0
4	1 0 0	1
5	1 0 1	0
6	1 1 0	0
7	1 1 1	0

$A' \cdot C' = 1$ or $A' = 1, C' = 1$ or $A = 0, C = 0$ rows 0 & 2

$B' \cdot C' = 1$ or $B' = 1, C' = 1$ or $B = 0, C = 0$ rows 0 & 4

These rows each receive a 1.

$Z = A' \cdot B' \cdot C' + A' \cdot B \cdot C' + A \cdot B' \cdot C'$

$Z = (A + B + C') \cdot (A + B' + C') \cdot (A' + B + C') \cdot (A' + B' + C) \cdot (A' + B' + C')$

13. Obtain the truth table, the on-set minterm list (shorthand notation) and the canonical SOP of $Z(A, B, C) = \prod (0, 3, 4, 5, 6)$.

Row	A B C	Z
0	0 0 0	0
1	0 0 1	1
2	0 1 0	1
3	0 1 1	0
4	1 0 0	0
5	1 0 1	0
6	1 1 0	0
7	1 1 1	1

$Y(A, B, C) = \Sigma (1, 2, 7)$

$Z = A' \cdot B' \cdot C + A' \cdot B \cdot C' + A \cdot B \cdot C$