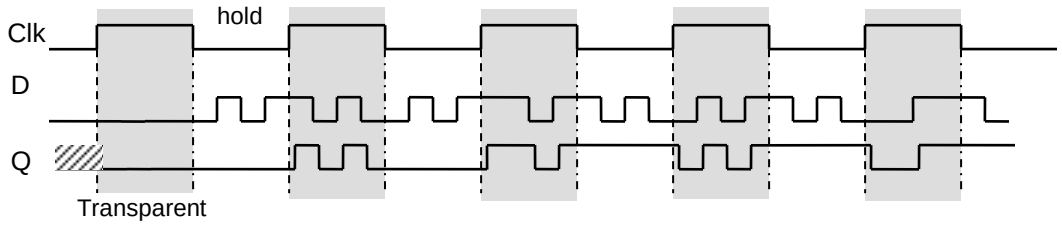
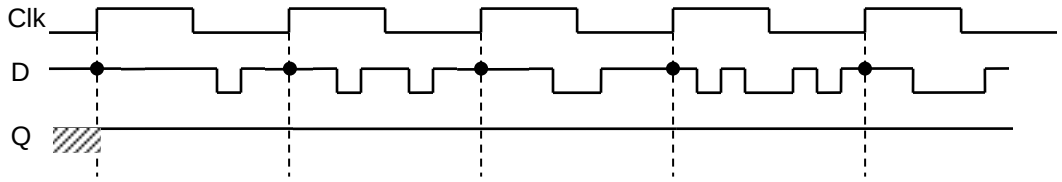
CE-210 Digital Systems I
Assignment # 7 – Chapter #7 - Solution

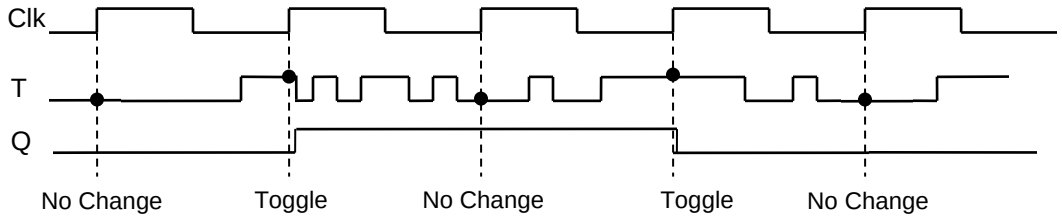
1- The D & Clk signals applied to a NOR-gate-based D-latch are shown below. Draw the output waveform of this latch.



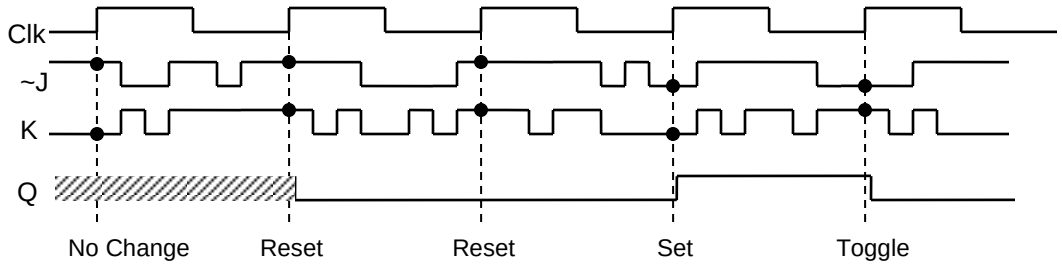
2- The D & Clk signals applied to a positive-edge-triggered D-FF are shown below. Draw the output waveform of this FF.



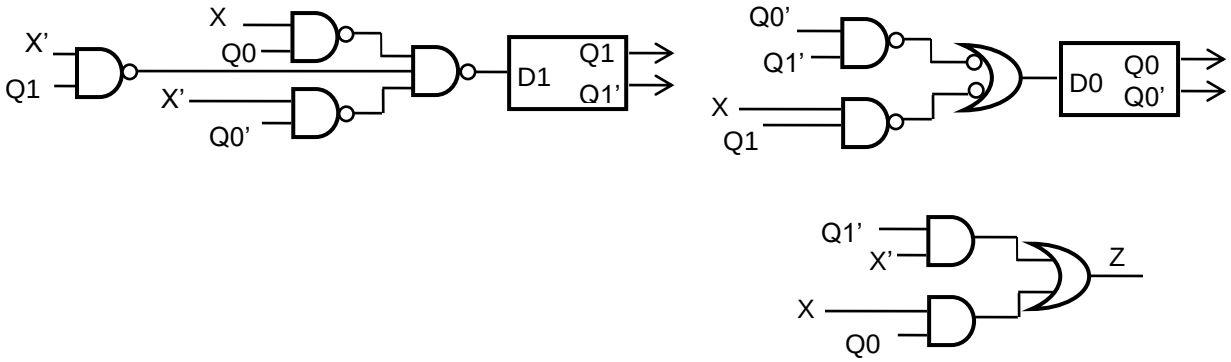
3- The T & Clk signals applied to a positive-edge-triggered T-FF are shown below. Draw the output waveform of this FF. Assume that the initial state of the FF is 0.



4- The J, K & Clk signals applied to a positive-edge-triggered JK-FF are shown below. Draw the output waveform of this FF.



5- Circuit analysis: Obtain a transition diagram and a state diagram for the circuit shown below. Z is the output. Show your work.



1- Excitation and output equations

D1 = ((X.Q0)'. (X'.Q1)'. (X'.Q0')')' = X . Q0 + X' . Q1 + X' . Q0'

D0 = Q1' . Q0' + X . Q1

Z = X . Q0 + X' . Q1'

2- Excitation and output maps

O1O0 \ X	0	1
00	1	0
01	0	1
11	1	1
10	1	0

D1

O1O0 \ X	0	1
00	1	1
01	0	0
11	0	1
10	0	1

D0

O1O0 \ X	0	1
00	1	0
01	1	1
11	0	1
10	0	0

Z

3- Partial Transition Tables

O1O0 \ X	0	1
00	1	0
01	0	1
11	1	1
10	1	0

$Q1^{n+1}$

O1O0 \ X	0	1
00	1	1
01	0	0
11	0	1
10	0	1

$Q0^{n+1}$

4,5- Transition Table, and State Table

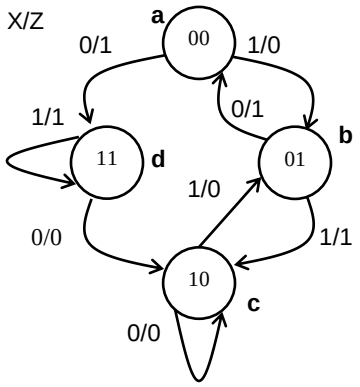
6- Transition Graph, and State Graph

Q1Q0 \ X	0	1
00	11, 1	01, 0
01	00, 1	10, 1
11	10, 0	11, 1
10	10, 0	01, 0

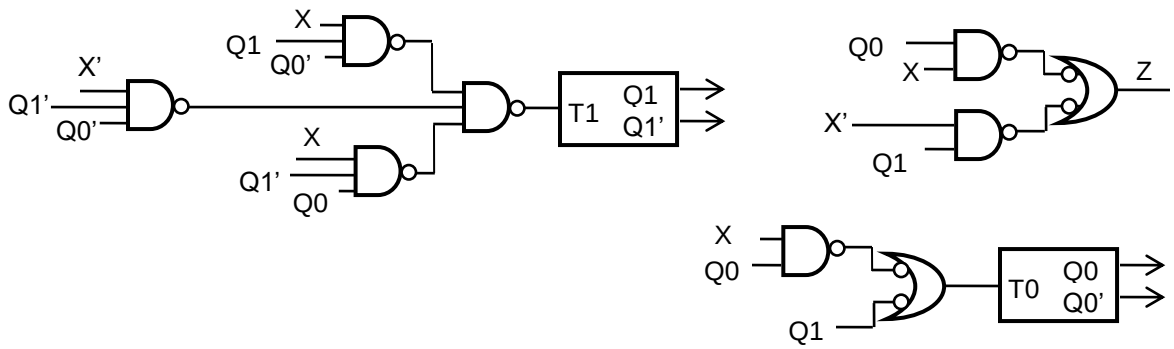
$Q1^{n+1}\,Q0^{n+1}$, Z

Q1Q0	Q \ X	0	1
00	a	d, 1	b, 0
01	b	a, 1	c, 1
11	d	c, 0	d, 1
10	c	c, 0	b, 0

Q^{n+1}, Z



6- Circuit analysis: Obtain a transition diagram and a state diagram for the circuit shown below. Z is the output. Show your work.



1- Excitation and output equations

T1 = ((X . Q1' . Q0)' . (X' . Q1' . Q0') . (X . Q1 . Q0'))' = X . Q1' . Q0 + X' . Q1' . Q0' + X . Q1 . Q0'

T0 = Q1' + X . Q0

Z = X . Q0 + X' . Q1

2- Excitation and output maps **3- Partial Transition Tables**

O1O0 \ X	0	1
00	1	0
01	0	1
11	0	0
10	0	1

T1

O1O0 \ X	0	1
00	1	1
01	1	1
11	0	1
10	0	0

T0

O1O0 \ X	0	1
00	0	0
01	0	1
11	1	1
10	1	0

Z

O1O0 \ X	0	1
00	1	0
01	0	1
11	1	1
10	1	0

$Q1^{n+1}$

O1O0 \ X	0	1
00	1	1
01	0	0
11	1	0
10	0	0

$Q0^{n+1}$

4,5- Transition Table and State Table

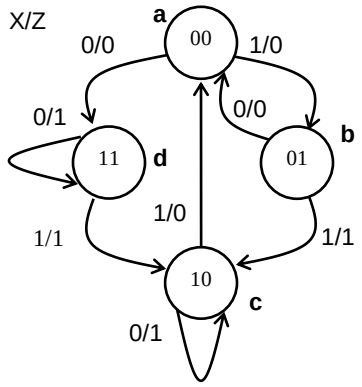
Q1Q0 \ X	0	1
00	11,0	01, 0
01	00, 0	10, 1
11	11, 1	10, 1
10	10, 1	00, 0

$Q1^{n+1}\,Q0^{n+1}$, Z

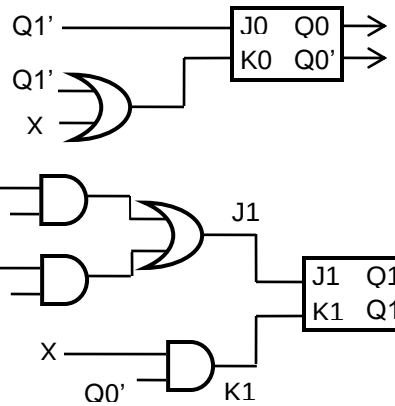
Q1Q0	Q \ X	0	1
00	a	d, 0	b, 0
01	b	a, 0	c, 1
11	d	d, 1	c, 1
10	c	c, 1	a, 0

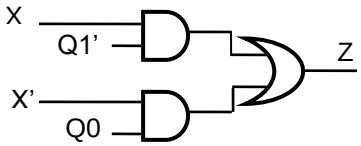
Q^{n+1}, Z

6- Transition Graph and State Graph



7- Circuit analysis: Obtain a transition diagram and a state diagram for the circuit shown below. Z is the output. Show your work.





1) Excitation & output equations

J1 = X . Q0 + X' . Q0'
K1 = X . Q0'
J0 = Q1'
K0 = Q1' + X
Z = X' . Q0 + X . Q1'

2) Excitation and output maps

O1O0 \ X	0	1
00	1	0
01	0	1
11	0	1
10	1	0

J1

O1O0 \ X	0	1
00	0	1
01	0	0
11	0	0
10	0	1

K1

O1O0 \ X	0	1
00	1	1
01	1	1
11	0	0
10	0	0

J0

O1O0 \ X	0	1
00	1	1
01	1	1
11	0	1
10	0	1

K0

O1O0 \ X	0	1
00	0	1
01	1	1
11	1	0
10	0	0

Z

3- Partial Transition Tables

O1O0 \ X	0	1
00	1	0
01	0	1
11	1	1
10	1	0

$Q1^{n+1}$

O1O0 \ X	0	1
00	1	1
01	0	0
11	1	0
10	0	0

$Q0^{n+1}$

4,5- Transition Table and State Table

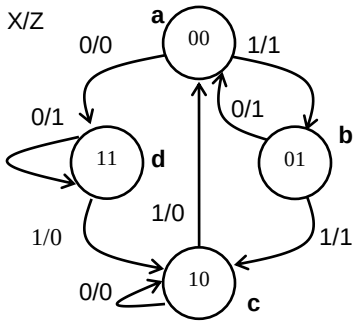
Q1Q0 \ X	0	1
00	11, 0	01, 1
01	00, 1	10, 1
11	11, 1	10, 0
10	10, 0	00, 0

$Q1^{n+1}$ $Q0^{n+1}$, Z

Q1Q0	Q	X=0	X=1
00	a	d, 0	b, 1
01	b	a, 1	c, 1
11	d	d, 1	c, 0
10	c	c, 0	a, 0

Q^{n+1}, Z

6- Transition Graph and State Graph


X/Z
a
00
0/0
1/1
0/1
0/1
b
11
d
01
1/0
1/0
1/1
10
0/0
c