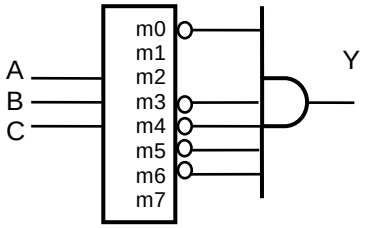
CE-210 Digital Systems I
Solution of Assignment # 6 – Chapter 6

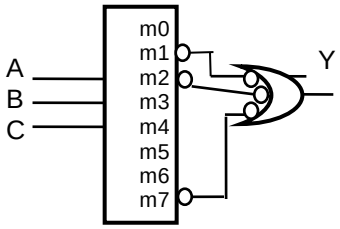
1- Realize $Y = \prod_{A, B, C} (0, 3, 4, 5, 6)$ with a minimum-size **active-low** binary decoder. Show two different circuits:

$Y = \prod_{A, B, C} (0, 3, 4, 5, 6)$ $\quad\quad$ $Y' = \prod_{A, B, C} (1, 2, 7)$

Active-low DCD



Active-low DCD



2- Put two 74x138 chips together and draw a schematic diagram to obtain a 4-to-16 binary decoder. How many outputs does the resulting decoder have?

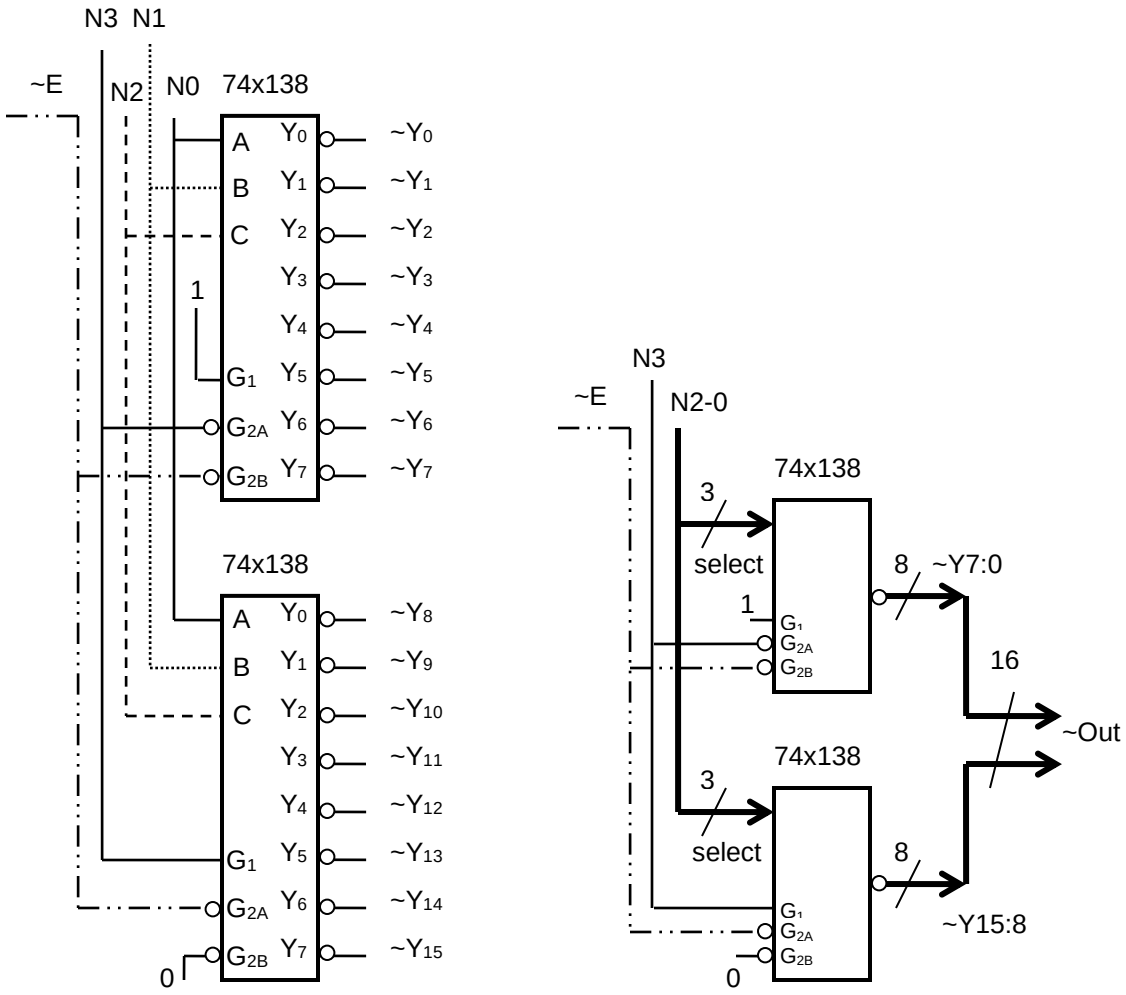
16

Now apply N3 N2 N1 N0 = 10**1**1 to the resulting decoder and suppose the whole decoder is enabled (~E = 0).

Which chip is enabled? The bottom one

Obtain the output of the 4-to-16 decoder for this input bit pattern (1011).

Output = 1111 0111 1111 1111



Logic diagram

Shorthand notation

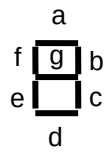
3- Draw a compressed truth table for an 8-input priority encoder (with no enable input). Suppose that the inputs are active low and outputs are active high. Determine the encoder's output if the input pattern is 0011 0011. Assume that the LSB has the highest priority.

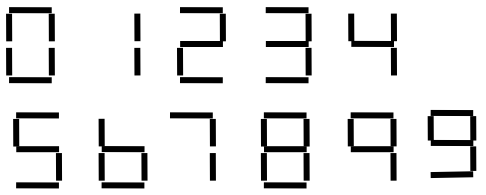
~I7	~I6	~I5	~I4	~I3	~I2	~I1	~I0	A2	A1	A0
x	**x**	**x**	**x**	**x**	**x**	**x**	**0**	**0**	**0**	**0**
x	x	x	x	x	x	0	1	0	0	1
x	x	x	x	x	0	1	1	0	1	0
x	x	x	x	0	1	1	1	0	1	1
x	x	x	0	1	1	1	1	1	0	0
x	x	0	1	1	1	1	1	1	0	1
x	0	1	1	1	1	1	1	1	1	0
0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	x	x	x

A2A1A0 = 010

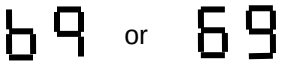
4- Draw a truth table for segment d of an active-low BCD-to-7-segment decoder. Let's assume that a segment turns on with a 0. Can you put an X (don't care) in one of the first ten rows of this table?

Decimal	D	C	B	A	d
0	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	0
3	0	0	1	1	0
4	0	1	0	0	1
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	1
8	1	0	0	0	0
9	1	0	0	1	X
10-15					X





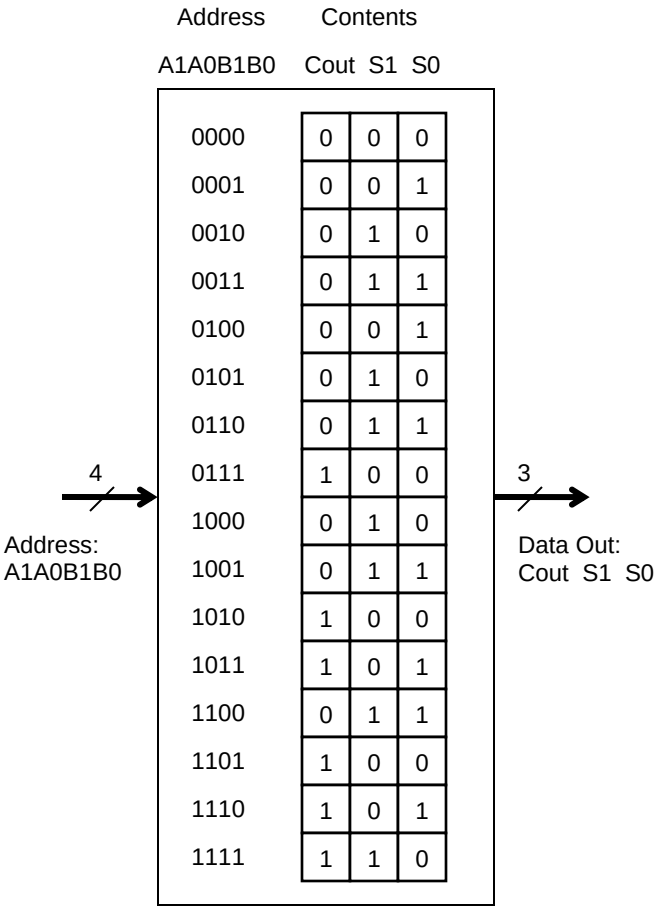
But notice that we normally prefer to have either



or

5- Determine the right size of a ROM that you need to realize a 2-bit adder (each operand is two bits wide) and then program the ROM to obtain this adder.

We need three columns to realize Cout, S1 and S0. On the other hand we need 16 rows, because a two bit adder has 2 x 2-bit operands (four variables).



6- Convert a 6-bit adder/subtractor to an **unsigned** full comparator with one output, A = B, where A and B are the two 6-bit operands.