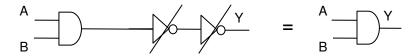
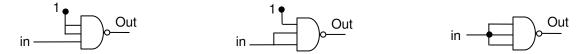
CE-210 Digital Systems I Solution of Assignment 2

Summer - 2016

- **1.** The output of a 4-input NAND gate is 1. What can you tell about the inputs of this gate? At least one of the inputs is low or zero.
- **2.** Simplify the following logic circuit:



3. Convert a 3-input NAND gate to an inverter. Show all the possible circuits.



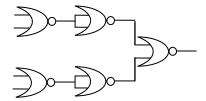
4. Convert a 4-input NOR gate to a 3-input NOR gate. Show all the possible circuits.



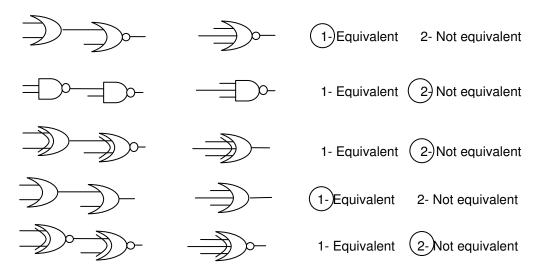
5. How does the compressed truth table shown below read? Draw a logic circuit to realize this table.

| AB | Υ | If $B = 0$, then $Y = A$ | в Y |
|-----|---|---|------------|
| x 0 | Α | If $B = 1$, then $Y = 1$ (no matter what A is) | , <u>B</u> |
| x 1 | 1 | | A 2 |

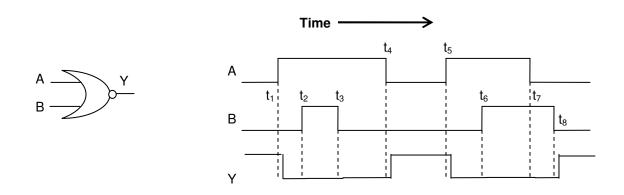
6. Use only 2-input NOR gates to design a 4-input NOR gate. Show one circuit.



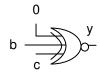
7. For each row in the following figure determine whether or not the two circuits are functionally equivalent. Circle the right choice.



8. The two time-varying signals (A and B) shown below are applied to a real two-input NOR gate. Assume that $t_1 = 0$, $t_2 = 1000$ ps, and the gate delay is 250 ps. Obtain the output waveform (Y).



9. Convert a 3-input XNOR gate to a 2-input XNOR gate.



| Row | abc | у | |
|-----------------------|--------|-----|---|
| 0 | 0¦0¯0¯ | -ī¦ | i |
| 1 | 0¦0 1 | 0¦ | 1 |
| 2 | 0 1 0 | 0 | 1 |
| 2 3 4 5 6 | 0 1 1 | 1 | ! |
| 4 | 100 | Ø | |
| 5 | 1 0 1/ | 1 | |
| 6 | 11/0\ | 1 | |
| 7 | 1/11 | Ø | |

10. Draw a switch diagram for a three-input CMOS NAND gate when the inputs are A1 A2 A3 = 1 0 1.

