## Digital Systems I lab

## **Lab06 Lecture Exercise**

Look at the following VHDL code:

```
"1111"
                       EN = '0'
L <=
               WHEN
                                   ELSE
                                   ELSE
       "1110"
               WHEN
                       S = "00"
       "1101"
               WHEN S = "01"
                                   ELSE
       "1011"
               WHEN S = "10"
                                   ELSE
       "0111";
```

Which frequently used digital circuit is described by this code?

Are the outputs active-high or active-low? Circle the correct answer:

active-high active-low

Is the Enable input (EN) active-high or active-low? Circle the correct answer:

active-high active-low

We will get the following code if the first two lines of the above code are swapped:

```
L <=
       "1110"
               WHEN
                       S = "00"
                                   ELSE
       "1111"
                       EN = '0'
                                   ELSE
               WHEN
       "1101"
               WHEN S = "01"
                                   ELSE
               WHEN S = "10"
       "1011"
                                   ELSE
       "0111";
```

Give a counterexample to show that the above two codes are not equivalent: In your example, the two codes receive the same value for EN and same value for S, but generate two different values for L. Fill in the blanks:

EN = S = First code: L = Second code: L =

Fill in the blank:

In this example, the order of WHEN ELSE lines is ... Circle the correct answer:

Important Unimportant

Write an input value that generates the same output for both codes:

EN = S =

If the last 2 WHEN ELSE lines are swapped, will the meaning of the code change? Circle the correct answer:

Yes No