## CE-210 Digital Systems I Fall 2021

## 120 Minutes

**Final Exam** 

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## Notes:

Show all your work.
Write clearly, neatly, and concisely.
Do not spend too much time on one single question, otherwise you may run out of time.
The Kettering University Code of Academic Integrity will be strictly enforced.

| 1- | Realize Y = $\prod_{A, B, C}$ (1, 3, 4) with a minimum-size <b>active-lov</b> | <b>v</b> binary | decoder. | Show two | different |
|----|---|-----------------|----------|----------|-----------|
|    | circuits.   |                 |          |          |           |

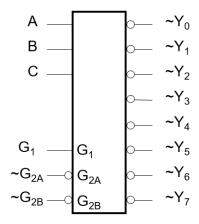
2- Put two **74x138** chips together and draw a schematic diagram to obtain a 4-to-16 binary decoder. How many outputs does the resulting decoder have?

Now apply N3 N2 N1 N0 = 0101 to the resulting decoder and suppose the whole decoder is enabled ( $\sim E = 0$ ).

Which chip is enabled?

Obtain the output of the 4-to-16 decoder for this input bit pattern (0101).

Output =



74x138: 3-8 active-low output

3- A compressed truth table for an 8-input priority encoder is given below. Determine the encoder's output if the input pattern is 0011 0111. Assume that the LSB has the highest priority.

| ~EI | ~10 | ~I1 | ~l2 | ~l3 | ~ 4 | ~I5 | ~l6 | ~17 | ~A2 | ~A1 | ~A0 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1   | х   | х   | х   | х   | х   | х   | х   | х   | 1   | 1   | 1   |
| 0   | х   | х   | х   | х   | х   | х   | х   | 0   | 0   | 0   | 0   |
| 0   | х   | х   | х   | х   | х   | х   | 0   | 1   | 0   | 0   | 1   |
| 0   | х   | х   | х   | х   | х   | 0   | 1   | 1   | 0   | 1   | 0   |
| 0   | х   | х   | х   | х   | 0   | 1   | 1   | 1   | 0   | 1   | 1   |
| 0   | х   | х   | х   | 0   | 1   | 1   | 1   | 1   | 1   | 0   | 0   |
| 0   | х   | х   | 0   | 1   | 1   | 1   | 1   | 1   | 1   | 0   | 1   |
| 0   | х   | 0   | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 0   |
| 0   | 0   | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   |
| 0   | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   |

An 8-input priority encoder

| 4- | Use K-maps to obtain a minimal SOP and a minim | al POS for the | e following function | Which realization, |
|----|--|----------------|----------------------|--------------------|
|    | SOP or POS, is more cost-effective?            |                |                      |                    |

$$Y = \prod A, B, C(2, 3, 6)$$

## 5- For the following function obtain:

all on-set prime implicants and all off-set prime implicants,

all distinguished 1-cells and all distinguished 0-cells,

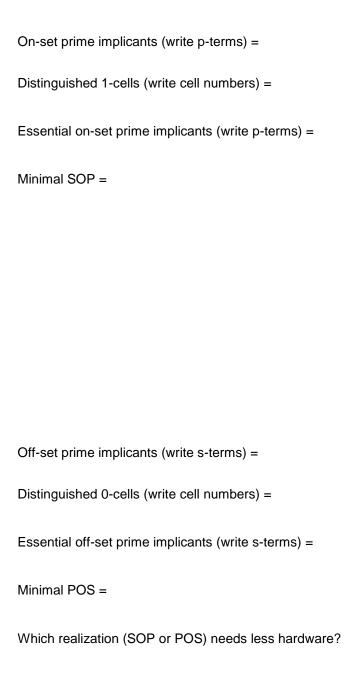
all essential on-set prime implicants and all essential off-set prime implicants,

a minimal SOP and a minimal POS.

Also determine which realization, SOP or POS, needs less hardware.

**Note:** For this function, draw a K-map to show all the on-set prime implicants and another K-map to show the minimal SOP. If these two K-maps are identical, then one K-map is sufficient. Similarly, draw a K-map to show all the off-set prime implicants and another K-map to show the minimal POS. Again, if these two K-maps are identical, then one K-map is sufficient.

$$Y = \Sigma_{A,B,C,D}$$
 (0, 1, 2, 3, 4, 5, 6, 7, 14, 15)



6- Perform the following additions in the four-bit unsigned system. Use the paper-and-pencil algorithm. For each addition determine whether or not a carry is generated.

| o Carry | Yes No |
|---------|--------|
| 1       | 011+   |
| 1       | 011    |
|         | 1      |

7- Apply the covering theorem (T9-L) to

$$Y = A' . G' . H . E . C + G' . E$$

8- Draw a switch diagram for a three-input CMOS NAND gate when the inputs are A1 A2 A3 = 0.11.

$$A2 \frac{A1}{A3} \bigcirc Z$$

9- Convert a 3-input XNOR gate to a 2-input XNOR gate.

- Circuit analysis: Obtain a transition diagram and a state diagram for the circuit shown below. Z is the output. Show your work.

