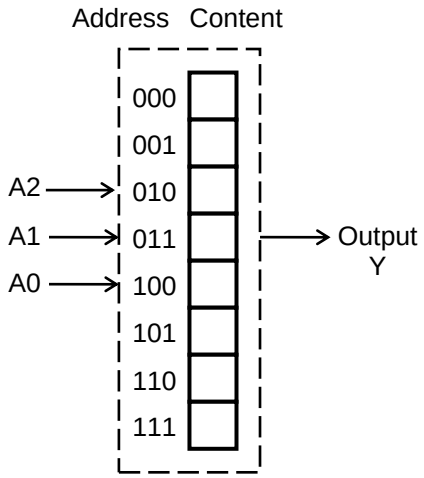
Lab03 Lecture Exercise

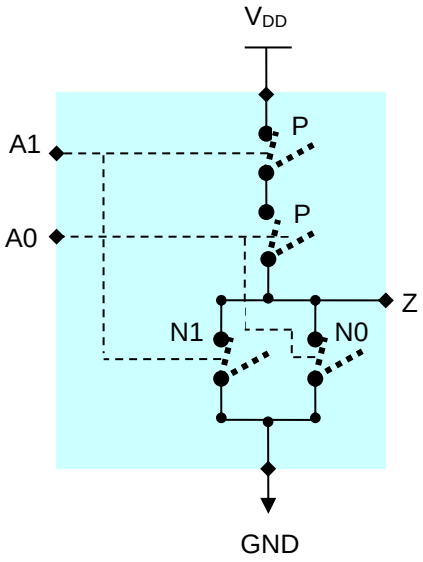
1. Different FPGAs may have different-size **L**ook**u**p **T**ables (LUTs). Let us suppose that an FPGA has 3-variable LUTs such as the one shown below. *Program* this LUT to get a 3-input XOR ate.

By LUT *programming* we mean placing right logic values in the memory cells of the LUT. LUTs can be *reprogrammed*.



2. How many functions can we create using the above LUT? What is the maximum number of inputs of the functions?

3. Which technology is more expensive in terms of number of transistors? Standard CMOS (shown below) or LUT-based?



4. What is the point in using the more expensive technology?

5. What type of information does an ENTITY provide about the underlying circuit? Circle all the correct answers, if any.

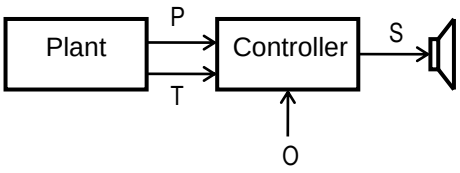
☐ It describes the inputs/outputs of the circuit.

☐ It explains how the circuit is built or behaves.

☐ Both of the them.

☐ None of them.

6. A hypothetical chemical plant has two binary output variables, T and P. T is pulled up (T = 1) when the temperature rises beyond a threshold, and so is P, when the pressure goes above normal. In this question, **you will write ONLY an ENTITY for an alarm control system (called Controller) for the plant** in the space provided below. The controller has one output variable (S) and three input variables, T, P and O. Inputs T and P come from the plant. O stands for operator. **Input O will be at logic 0 whenever the plant is supervised** by an operator. Otherwise, O will be pulled up. Output S drives the alarm. See the following figure. Let us assume that **the alarm goes off with a 0,** i.e., when S = 0**.** A 1 will shut off the alarm. When the temperature or the pressure or both go up, the alarm must sound provided that the plant is unattended. The alarm must shut off otherwise.



To write the ENTITY, did you need/use ALL the information that exists in the word description of the problem?

Remember: A VHDL code can be synthesized in different technologies, such as FPGAs or semicustom chips.

Remember: A VHDL code for a digital circuit needs one ENTITY and an ARCHITECTURE.

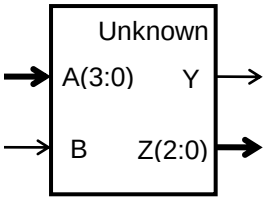
7. Write an ARCHITECTURE for the following two functions:

Y = A . B
Z = A + B

Call the ARCHITECTURE LogicFunction. The ENTITY is shown below:

```
ENTITY andor IS
PORT (   A, B : IN  STD_LOGIC;
         Y, Z : OUT     STD_LOGIC
       );
END andor;
```

8. Write an ENTITY for the following logic symbol:



9. Consider the following VHDL code:

```
ENTITY vector_operation IS
PORT (A, B    : IN      STD_LOGIC_VECTOR (2 DOWNTO 0);     -- Each input is 3 bits wide
            Y   : OUT     STD_LOGIC_VECTOR (7 DOWNTO 5)      -- Output is also 3 bits wide
        );
END vector_operation;

ARCHITECTURE algebraic OF vector_operation IS
BEGIN
    Y <=  A XOR B;
END algebraic;
```

Split the following simple vector assignment into three simple single-bit assignments in VHDL:

Y <= A XOR B;