Digital Systems I

CE 210 - 02L

Course Syllabus

Fall 2022

Welcome Back to School!

Instructor: Nozar Tabrizi, Associate Professor of Computer Engineering

Contact Information: Email (preferred): ntabrizi@kettering.edu, Tel: (810) 762 7826

Office: AB 2-703-G

Office Hours: MR 3:45 - 5:15 pm or by Appointment

Lab Sec. 02: W 1:20 3:25 pm AB 2-821

Contact Hours: 3 (lecture) + 2 (lab)

Prerequisite: ECE-101, CS-101 or IME-211

Grading

Lab Test 5 Points Week 8: This is a VHDL/FPGA-based test, which will be given *right at the beginning* of the lab time of Week 8, and will cover Parts II of Chapters 3, 4, and 5, and the associated Lab Exercises. The Lab Test will be closed book. You may use one double-sided cheat sheet. These chapters will be posted on Blackboard.

Lab Exercises 20 Points

Please note

1. **You are encouraged** to stop by my office and let us talk about your lab/lecture questions. ***Remember, your success is my first goal; I will do my best to reach this goal☺***
2. VHDL modeling and FPGA synthesis of digital circuits will be covered in the lab.
3. "Out-of-class weekly time commitment" expected of students is *approximately* 8 hours (lecture and lab combined). **Remember, you may need to read a paragraph a few times to thoroughly understand it.**
4. To enhance your performance you are urged to
   Go over the lab handouts beforehand (advance reading)
   Work together, but do NOT copy from each other!
5. Regular lab attendance is required. An attentive lab participant will not miss class unless there is an acceptable excuse such as a job interview. You may get extra credit for your *active* lab participation and attentiveness. *Non-attentive students will not receive any extra credit or be considered for grade curving, if any.*
6. If you miss a lab, you will lose its whole credit unless you provide a document showing an acceptable excuse for your absence. I will then give you either a makeup lab or a grade based on your other grades at my discretion.
7. No make-up lab will be allowed if you leave the lab early while the lab exercise is incomplete.
8. For your lab assignments, you will work in groups of two. You will do some intense teamwork over the term. You will be notified of pre-labs, if any, in due course.
9. Due dates for each pre-lab and lab report are shown in the lab handout. Late pre-labs will not be accepted. Late lab reports may or may not be accepted; if they are, they will not get full credit. You should show your lab work *individually* and before you submit the report. Lab reports and pre-labs should be submitted *electronically*.
10. You are expected to be an active lab participant. As part of the lab presentation, you should *individually* demonstrate a solid understating of your work and results in each lab. If you do not *show* your lab work *individually* or *successfully*, you will not get credit for that lab.
11. If you are also in my (lecture) class, then to pass Digital Systems I class, and in addition to the minimum grade requirement, you need to *individually* and *successfully* present at least 6 lab works.
12. You are expected to check your Bb email at least once a day.
13. Your grades (pre-labs, lab reports, etc.) will be posted in Bb. Then you will have two days to let me know if you have any objections. No grades may change after this period.
14. And here is a helpful tip to assess your competency in a topic: ***see if you can teach the topic!***

Common Statement on Students with Documented Disabilities

The University will make reasonable accommodations for persons with documented disabilities. Students need to register with the Wellness Center every term they are enrolled in classes. To be assured of having services when they are needed, students should contact the Wellness Center during the first week of each term. Note that it is the student's responsibility to arrange accommodations with each professor. For more information on "Disability Services," refer to the Student Life section of the current Undergraduate Catalog. This information is also noted in the Student Handbook.

Common Statement on Ethics in the University and Academic Integrity

Kettering University values academic honesty and integrity. Cheating, collusion, misconduct, fabrication, and plagiarism are serious offenses. Each student has a responsibility to understand, accept, and comply with the University's standards of academic conduct as set forth in our statement, "Ethics in the University," and "Academic Integrity" as well as policies established by individual professors. For more information, refer to the Student Life section of the current Undergraduate Catalog. This information is also noted in the Student Handbook.

Academic Assistance

In addition to your professors, academic assistance with class work and writing is available from the Academic Success Center (ASC) at (810) 762-7995 or academicsuccess@kettering.edu .

The Undergraduate Catalog is located at
http://catalog.kettering.edu/undergrad/student-life/

Link to University Policy Syllabus:
https://drive.google.com/file/d/1WpFfPZqt0GYaPEtoV5QhCeOL0j5WHkD9/view

Why is "Digital Systems I" Important?

What you learn in this course is the first step toward the hardware design of revolutionizing microprocessors, which are increasingly and inevitably entering our daily lives.

Brief Course Description

Design and analysis techniques for combinational and sequential logic circuits are studied. Topics include binary number systems and binary addition/subtraction, combination logic minimization, frequently used combinational logic circuits, finite state machines, shift registers and counters. VHDL will be used for description, simulation and FPGA synthesis of digital circuits.

Lab Schedule

Week 1:

Lab01 (virtual)
Download, Install and Test Quartus

Getting Started
Intel Quartus Prime and DE10-Lite FPGA Board

Week 2:

Lab02
Intel Quartus Schematic Capture

Gates
Basic Building Blocks of Digital Circuits

Week 3:

Lab03
ENTITY, ARCHITECTURE, and
Simple Signal Assignments in VHDL

Switching Algebra

Week 4:

Lab04
Concurrency in VHDL

Design and Empirical Analysis of Digital Circuits

Week 5:

Lab05
Structural Modeling and Hierarchical Designs

Four-bit Full Comparator

Logic Minimization using Karnaugh Maps

Week 6:

Lab06
Behavioral Modeling of Digital Circuits
Conditional Signal Assignments

Decoders, Encoders, Multiplexers, and Comparators
Two Textbooks and Eight Students

Week 7:

Lab07
Behavioral Modeling of Digital Circuits
Selected Signal Assignments

Basic Arithmetic and Logic Unit (ALU)

Week 8:

Lab Test
Will cover Parts II of Chapters 3, 4, and 5, and the associated Lab Exercises

VHDL Lecture: Latches and FFs
and
Introduction to Sequential Circuits in VHDL

Week 9:

Lab08
Behavioral Modeling of Digital Circuits

Process Constructs
"If Then Else" Statements

Simulation of Digital Circuits
Using Intel ModelSim

D-latches and D-FFs
and
Empirical Analysis of Finite-State Machines

Week 10:

Lab08 (Cont'd)

Optional Lab09, should you complete lab08 in Week 9:

Behavioral Modeling of Digital Circuits

Process Constructs
"Case" Statements

Design of State Machines

Good luck!
Nozar Tabrizi