

Kettering University

Digital Systems I

Lab Exercise 1

Download, Install and Test Quartus

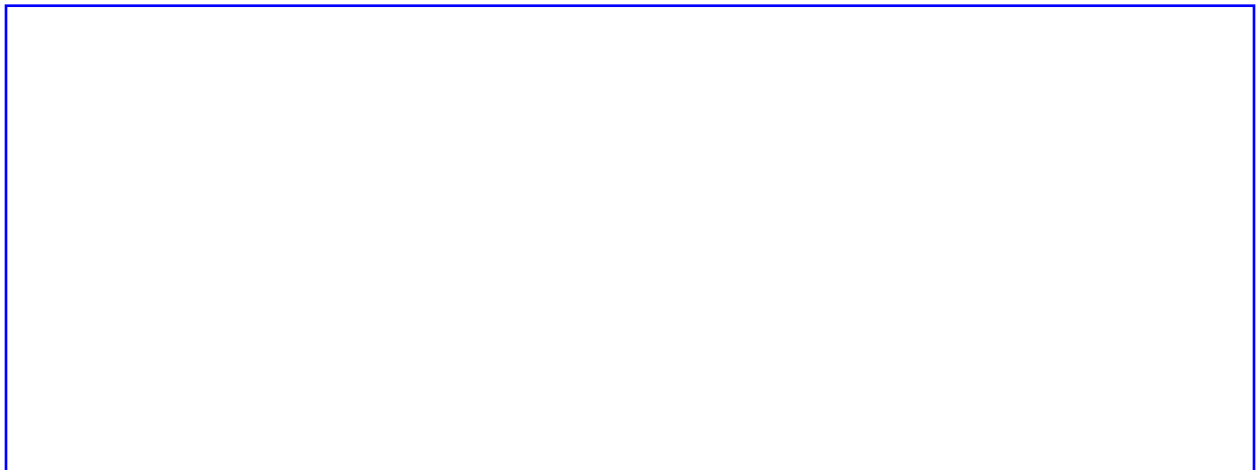
Getting Started

Intel Quartus Prime and DE10-Lite FPGA Board

Fall 2022

We will meet virtually in week 1.

Purpose of this lab experiment:



Objectives

Install and test Quartus software, learn how to create a project, and become familiar with the DE10-Lite FPGA board.

What to Hand In

- There is no lab report for this week. Show your functional circuit in Assignment **3** to the lab instructor *individually*. You may show your work **virtually** during lab time in week 1, or as soon as you walk into the lab in week 2.

Assignments

Please do Assignments 1 and 2 before our lab starts in Week01. Note that download time and also installation time should be lengthy.

1. Download and install Intel Quartus Prime 18.1 Lite Edition

2. Download the tar file [Quartus-lite-18.1.0.625-windows.tar](#)

3. Use 7-zip to untar the tar file. You will get two files and one folder, including a "setup" file.

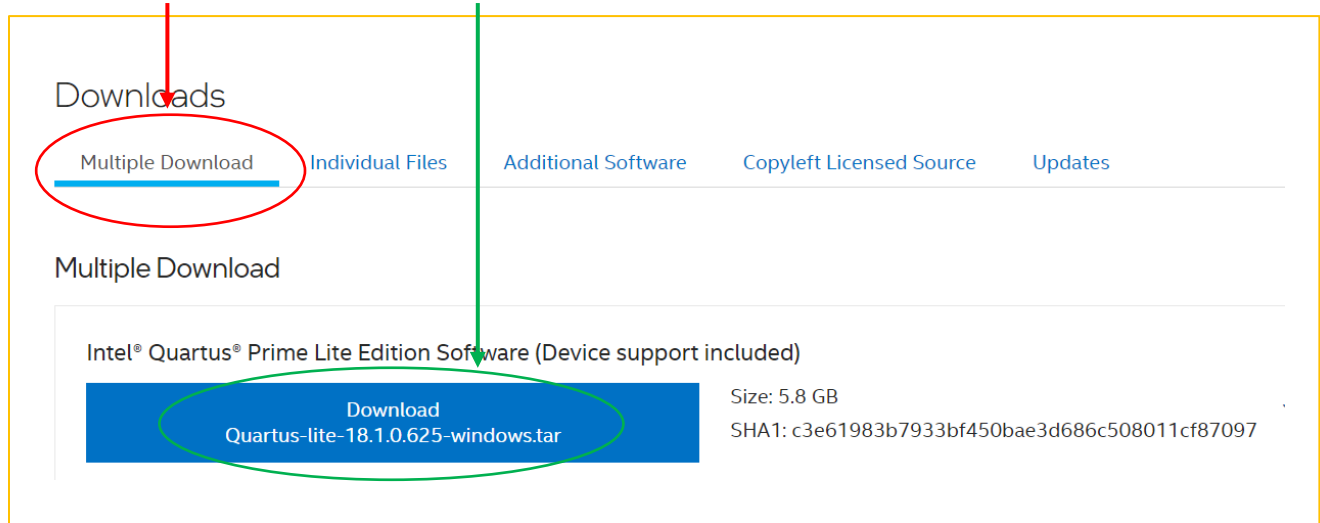
4. Double-click on the setup file to start installation ...

The details of the above steps are as follows:

Go to this webpage:

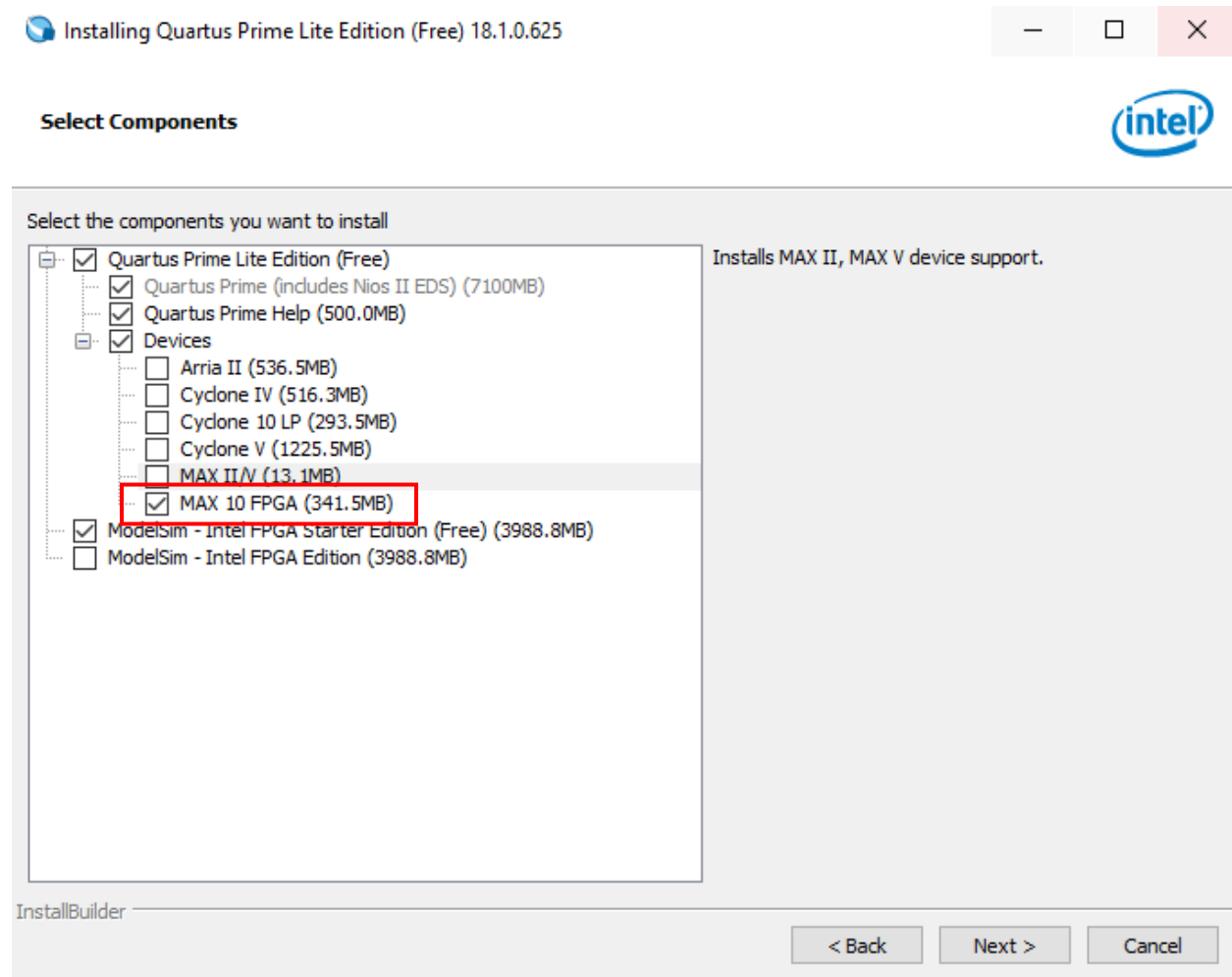
<https://www.intel.com/content/www/us/en/software-kit/665990/intel-quartus-prime-lite-edition-design-software-version-18-1-for-windows.html>

Choose **Multiple Download**. Click on the **Download** button.



Note: Download time and also installation time should be lengthy. **So, you are encouraged to download and install the software ASAP. We need the software before lab time.**

Put the tar file in a folder, and then use 7-zip to untar it. You will get one folder and two files including the "setup" file. Double-click on this file to begin the installation. Follow the instructions. **Not the installation path on a piece of paper.** You will need it in Assignment 2. At some stage, you are given the following option table to select components. To save time and space, deselect all the components except MAX10 FPGA as shown in the following screenshot. This is the FPGA family used on the DE10-Lite, our lab board:



2. USB Blaster Driver Installation

Go to the following site:

http://www.terasic.com.tw/wiki/Altera_USB_Blaster_Driver_Installation_Instructions#For_Windows_10_2C_do_the_following

Connect your DE10-Lite FPGA board to your laptop, and then follow the instructions to install the Intel USB Blaster Driver.

Note: If you chose the default installation path, the following should be the path of the USB blaster driver that you would need in this installation:

c:/intelfpga_lite/18.1/quartus/drivers

3. Test the software and the DE10-Lite FPGA board

Create a folder called Digitals.1 on your desktop, make folder lab01 inside Digitals.1, and download files tb.vhd and DE10_LITE.qsf from Bb (Week 01), and place them in lab01 folder.

To build your circuit in the FPGA chip, you need to take the following three steps:

Step I: Create a project or use a project that has already been created. We learn how to create a project in this lab exercise.

Step II: Describe your circuit using a hardware description language or as a schematic.

We will learn how to take this step in the coming weeks. For today's lab, the description file, tb.vhd, is provided; it is in your lab01 folder!

Step III: Attach your description file(s) from Step II to the project (that you created in Step I), compile the description, and then map it into the FPGA chip. We learn how to take this step in today's lab.

Note: The largest chip on the DE10-Lite board is the FPGA chip. To do Lab Exercise 1, we do not have to know how FPGAs work. We will learn it in the upcoming weeks.

Step I: Create a project

Double-click on the Quartus icon to run the tool. Take the following sub-steps to create a project (called tb) in the lab01 folder:

In Quartus window:

File > New Project Wizard ...

The "Introduction" window pops up: Click on Next:

The "Directory, Name, Top-Level Entity" window appears:

In the first field called "what is the working directory for this project?" browse and select your lab01 directory.

In the second field called "what is the name of this project?" type: tb

Note that the same name, tb, will automatically be typed in the third (last) field, "... the name of the top-level design entity ..." as well. It means that the project name and the top-level design entity (or top-level module) name should be the same. (You will see what we mean by the *top-level* module in the coming weeks.) Click on Next:

The "Project Type" window appears. Select "Empty project". Click on Next:

The "Add Files" window will open up. Let us add (attach) the description file(s) later. Click on Next:

The “Family, Device & Board Settings” window appears. Select the “Device” tab. In the “Family” drop-down list choose MAX 10(DA/DF/DC/SA/SC). It should be your only choice based on the devices you installed. In the “Available devices” table select: **10M50DAF484C6GES**.

Hint: Copy and paste this number in the “Name filter” field to get to the right chip straightaway.

Family, Device & Board Settings

Device Board

Select the family and device you want to target for compilation.
You can install additional device support with the Install Devices command on the Tools menu.

To determine the version of the Quartus Prime software in which your target device is supported, refer to the [Device Support List](#) webpage.

Device family

Family: MAX 10 (DA/DF/DC/SA/SC)

Device: All

Target device

☐ Auto device selected by the Fitter

☒ Specific device selected in 'Available devices' list

☐ Other: n/a

Available devices:

Name	Core Voltage	LEs	Total I/Os	GPIOs	Memory Bits	Embedded multiplier 9-bit elem
10M50DAF484C6GES	1.2V	49760	360	360	1677312	288

< Back Next > Finish Cancel Help

Click on Next.

The “EDA Tool Settings” window will appear. We are not going to use other EDA tools. Click on Next:

The “Summary” window pops up. Check the information and make sure it is correct.

Question: Based on the information on this page, how much is the core Vcc?

Click on Finish. Project tb is created 😊

To see what you did, open your lab01 folder; you will see the following three new items:

Folder db; File tb.qpf; File tb.qsf.

Do NOT add anything to folder db.

tb.qpf (**Q**uartus **P**roject **F**ile) is your project file. If you come back later, open this file to open your project: File > Open project ... (ctrl + J)

Step II: Describe your circuit

For today’s lab, the circuit has already been described in file tb.vhd, which you placed in your lab01 folder. In the coming weeks, you will learn how to describe digital circuits in VHDL.

Step III: Attach your description file(s) to the project, compile the description (source code), and then map it into the FPGA chip

- If you closed the project, open it:

File > Open Project ...

Select tb.qpf and click Open.

- If you opened a closed project, you need to change the default Device Number to our Device Number:

Assignments > Device ...

The “Device” window pops up.

Similar to what you did above when you created project tb, in the “Family” drop-down list choose MAX 10(DA/DF/DC/SA/SC). It should be your only choice based on the devices you installed. In the “Available devices” table, select **10M50DAF484C6GES**, then click OK.

Hint: Copy and paste this number in the “Name filter” to get to the right chip immediately. Select the right chip, and click on OK.

- Add (attach) the .vhd file(s) to your project:

Project > Add/Remove Files in Project ...

Browse and select tb.vhd (which is in the lab01 folder); click on Open, then OK.

Note: In today’s lab, we have/need only one .vhd file. In general, we may have/need more files all of which should be added to the project and compiled.

- Import the pin assignment file, DE10_LITE.qsf, into your project:

Assignments > Import Assignments ...

Browse and select DE10_LITE.qsf (which is in your lab01 folder); click on Open, and then OK.

- Click on the triangle on the toolbar to compile tb.vhd. See Figure 1. There is no syntax error in this file! In general, if you get syntax error messages (in red), double-click on the *first* one; the problematic line of code will be highlighted. See if you can resolve the error; if not, ask your lab instructor for help.
- Once you get the successful compilation message, connect the FPGA board to your laptop if it is disconnected. Click on the “programmer” button on the toolbar. See Figure 1. The “programmer” window appears. **Now your physical circuit is only one click away!** Click on the “Start” button to map your code into the FPGA chip. Test your circuit: *The slide switches should be able to turn ON/OFF the LEDs! Show your functional circuit to the lab instructor.*

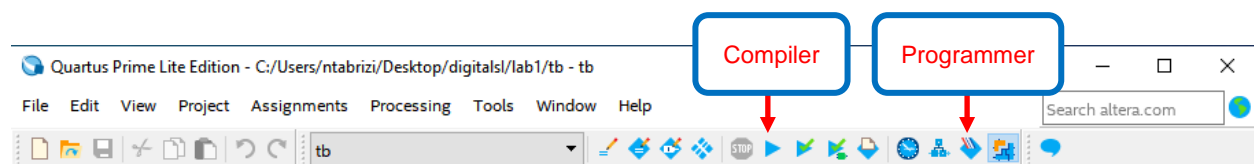


Figure 1. Quartus toolbar

When you compile the source code, a folder called output_files is created in your lab01 directory. This new folder contains some files including tb.sof, which is the file that “Programmer” uses to map your code into the FPGA chip. See Figure 2.

Troubleshooting tip: When you click on “Programmer”, what should you do if the “Start” button was grayed out as shown in Figure 2?

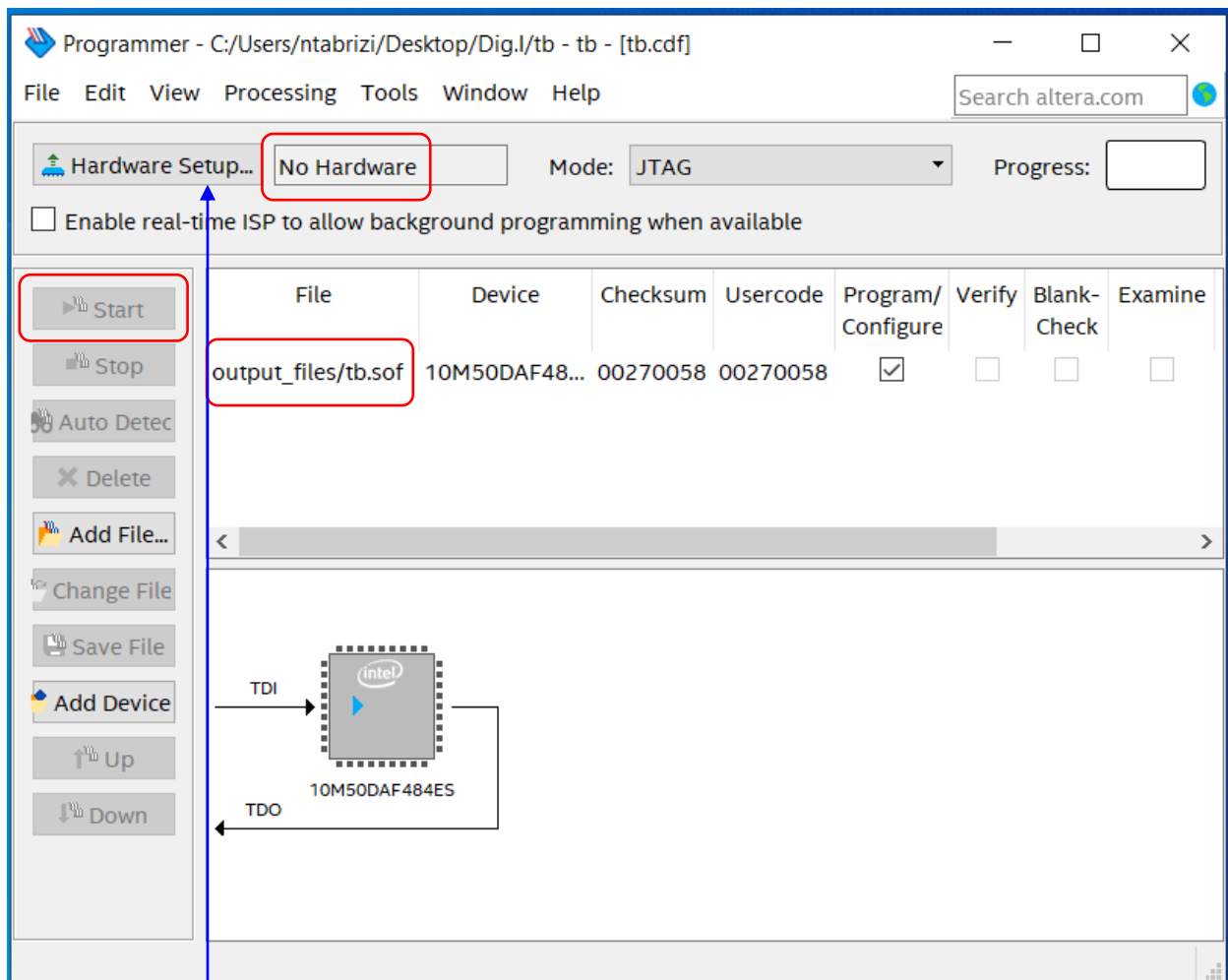


Figure 2. Programmer window: .sof file; start button grayed out

The reason is that the USB Blaster has not been selected. To resolve the issue, take these steps:

- Click on the “**Hardware Setup**” button to open the “Hardware Setup” window shown in Figure 3:

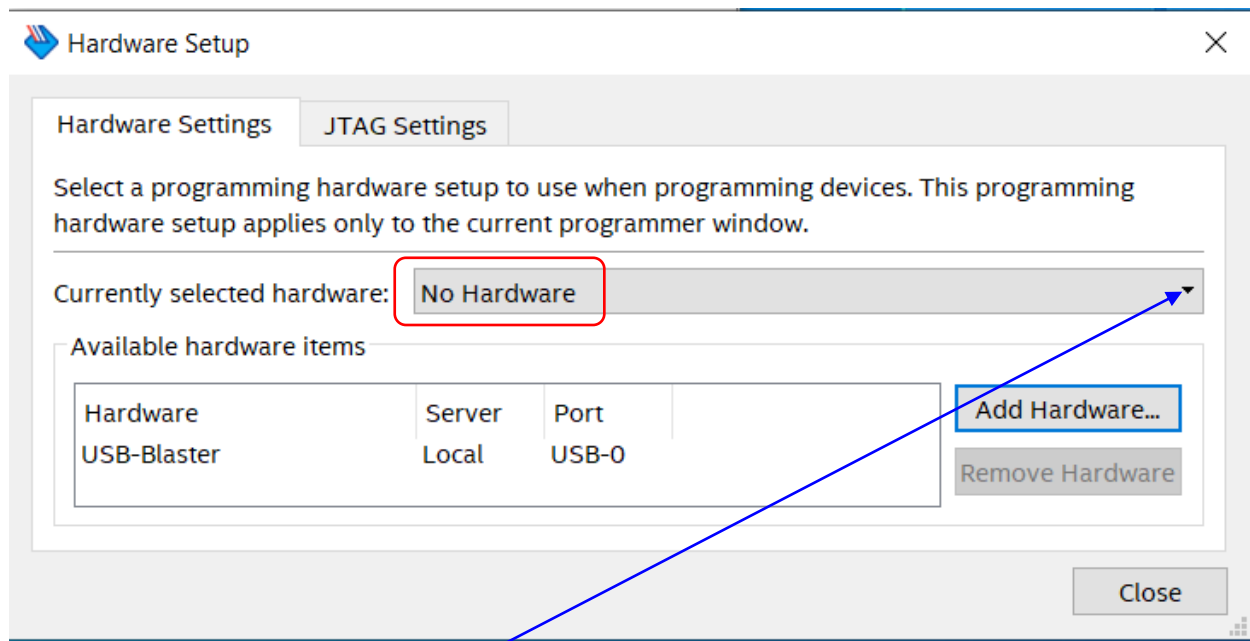


Figure 3. Hardware Setup window

- Open the **drop-down menu** and select USB-Blaster [USB-0]. The “Hardware Setup” window will change to what you see in Figure 4. Click on Close. Now the Start button should be clickable.

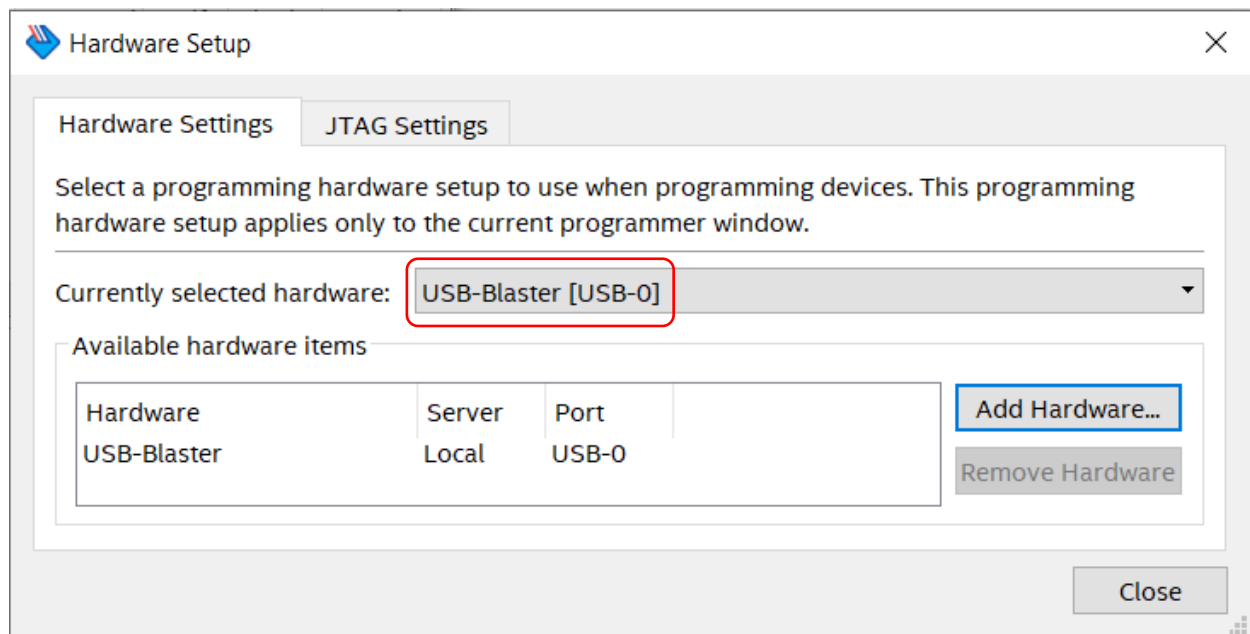


Figure 4. Hardware Setup window when USB-Blaster [USB-0] is selected