October 11, 2022

ECE 6240

Lab#4+5 NAND gate Schematic + Test Bench + Simulation (DC + VTC) + Layout

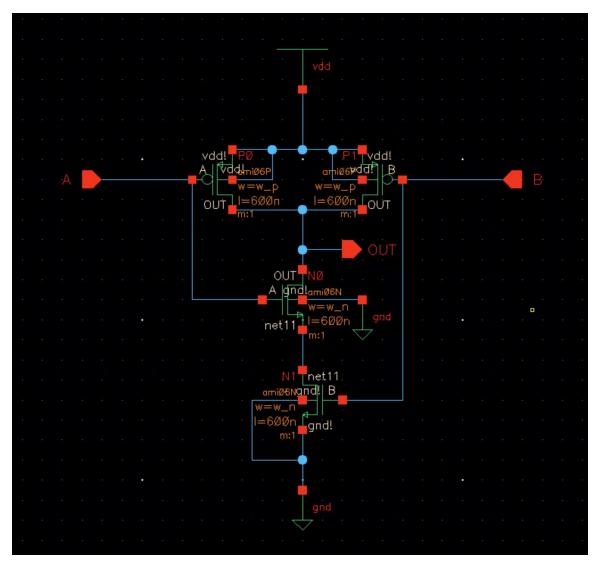


Figure 1 Schematic

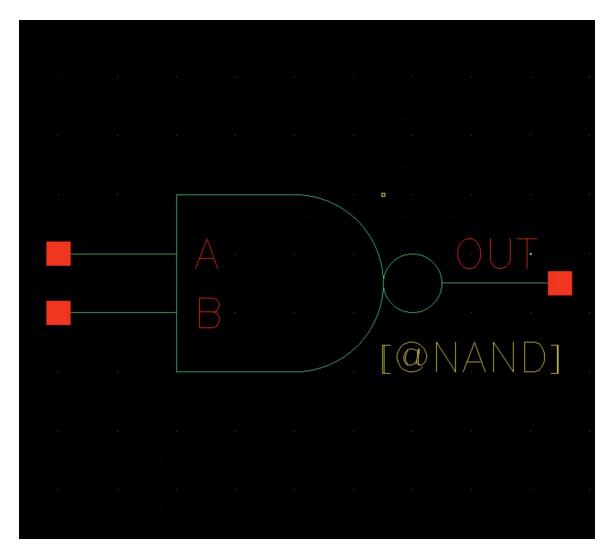


Figure 2 Symbol

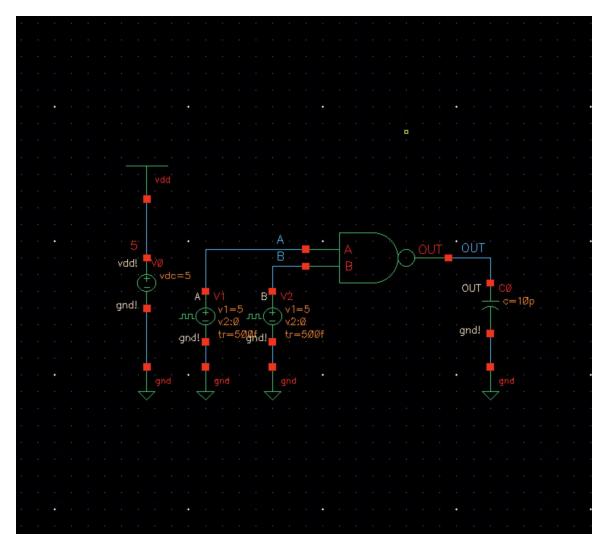


Figure 3 Testbench schematic

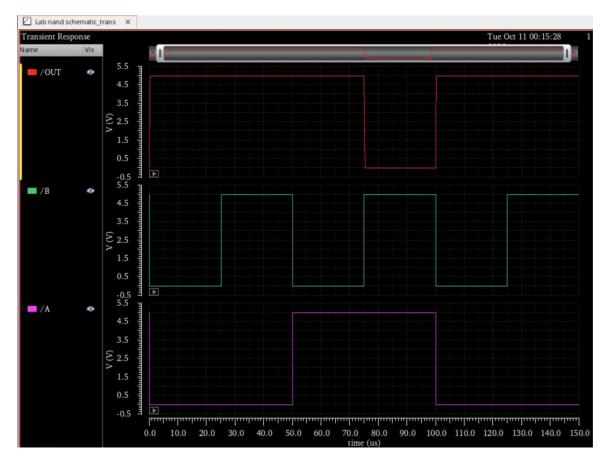


Figure 4 Transient Simulation

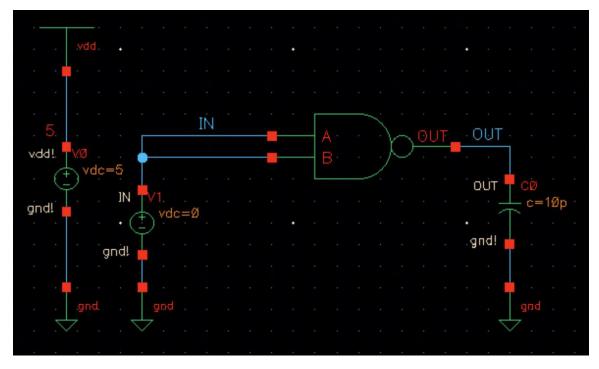


Figure 5 VTC Testbench Schematic

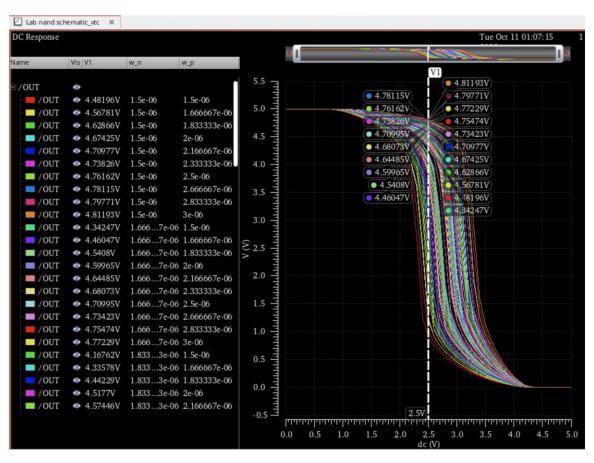


Figure 6 VTC DC Sweep, both transistors varied

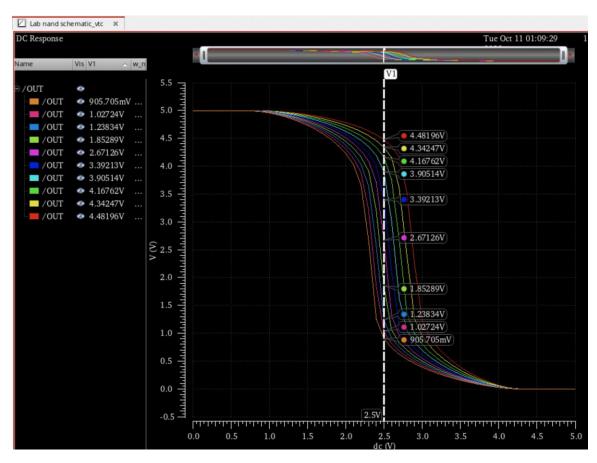


Figure 7 VTC DC Sweep, w_n varied

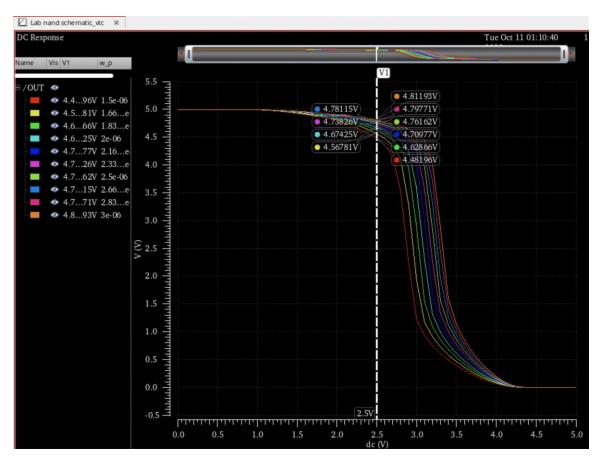


Figure 8 VTC DC Sweep, w_p varied

With w_p=1.5u and w_n=2.3u, we can get 2.5v-2.67v.

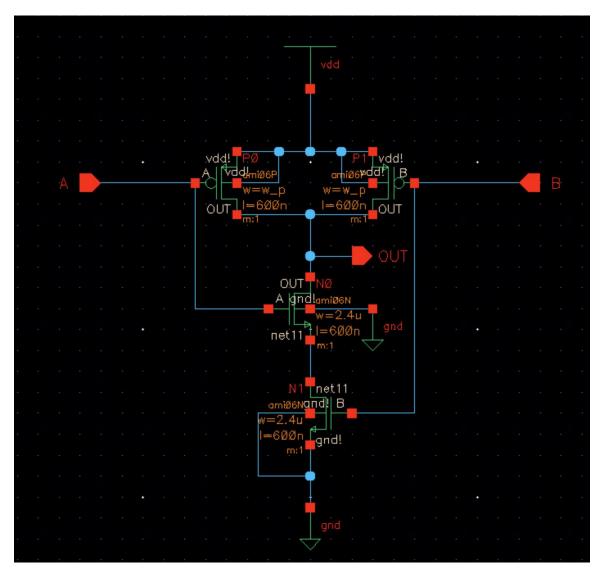


Figure 9 Schematic with new width

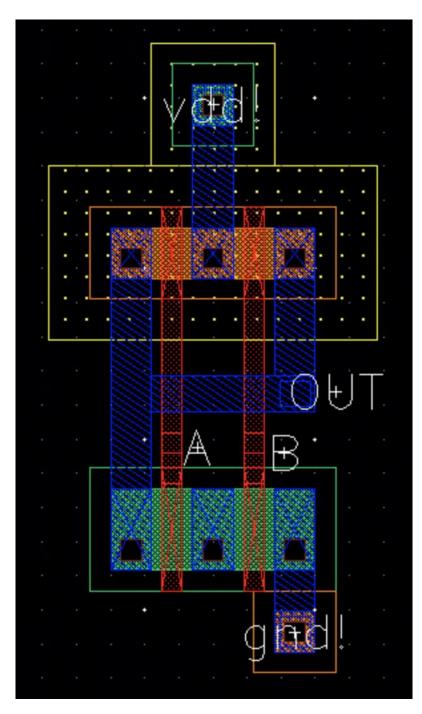


Figure 10 Layout

```
Virtuoso® 6.1.7-64b - Log: /home/ead/yihui/CDS.log.1 x

File Tools Options IBM_PDK Help Cadence

drc(elecHighresEdge (notch < (lambda * 7.0)) errMesg)
executing: drc(highresEdge elecHighresEdge (enc < (lambda * 2.0)) errMesg)

DRC started......Tue Oct 11 01:20:07 2022
completed ....Tue Oct 11 01:20:07 2022
CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
*************** Summary of rule violations for cell "nand layout" *********

Total errors found: 0

M: ibmPdkHiSetRefPoint() R: ibmPdkcycleSelSet()
```

Figure 11 DRC Result

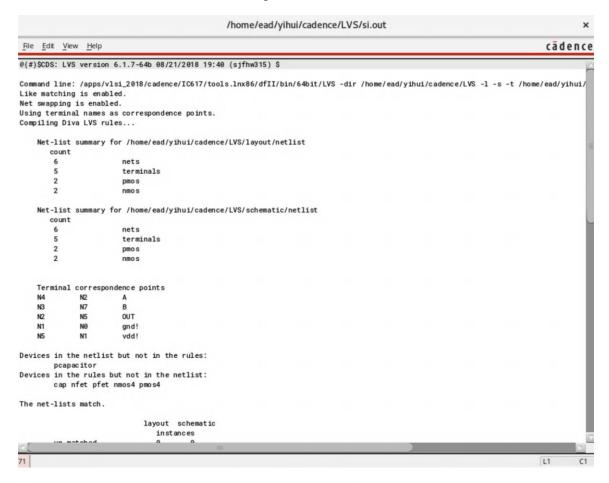


Figure 12 LVS Match

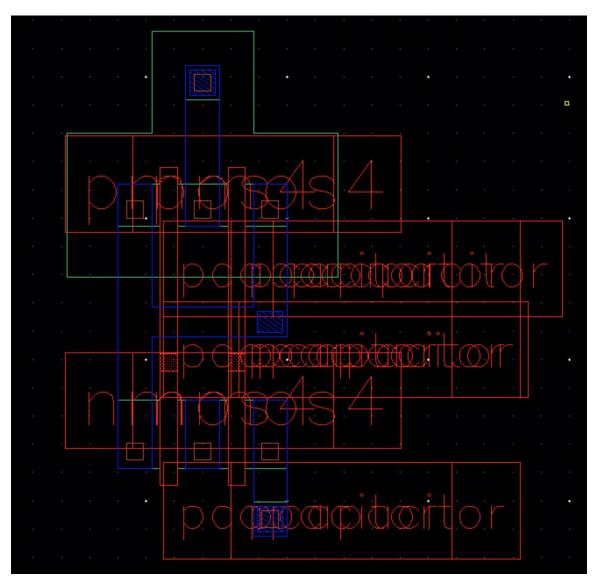


Figure 13 Extracted Layout