Yihui Wang

September 27, 2022

ECE 6240

Lab#3 Inverter Layout, DRC, Extraction, & LVS

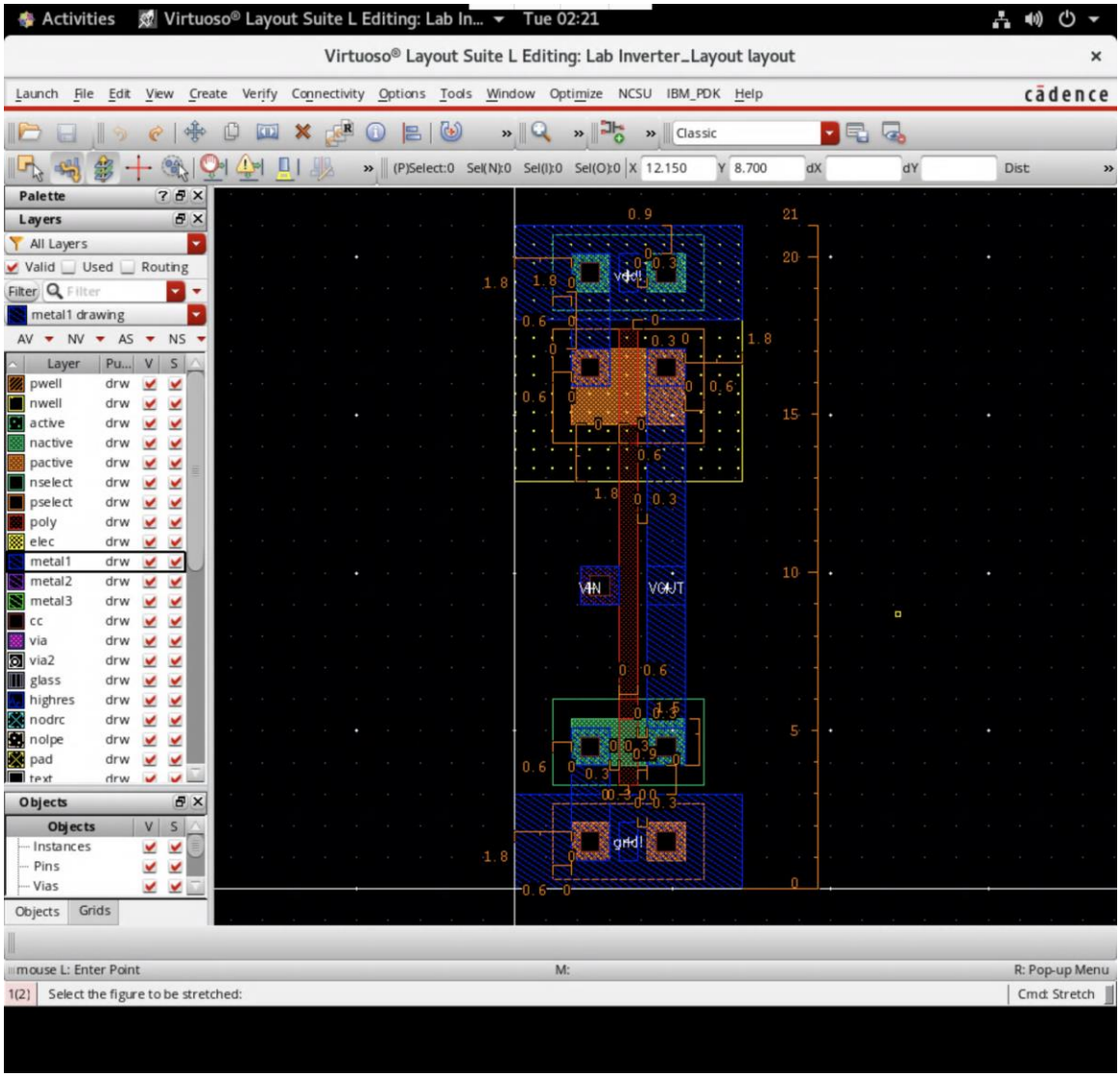

Figure 1 Overall completed layout

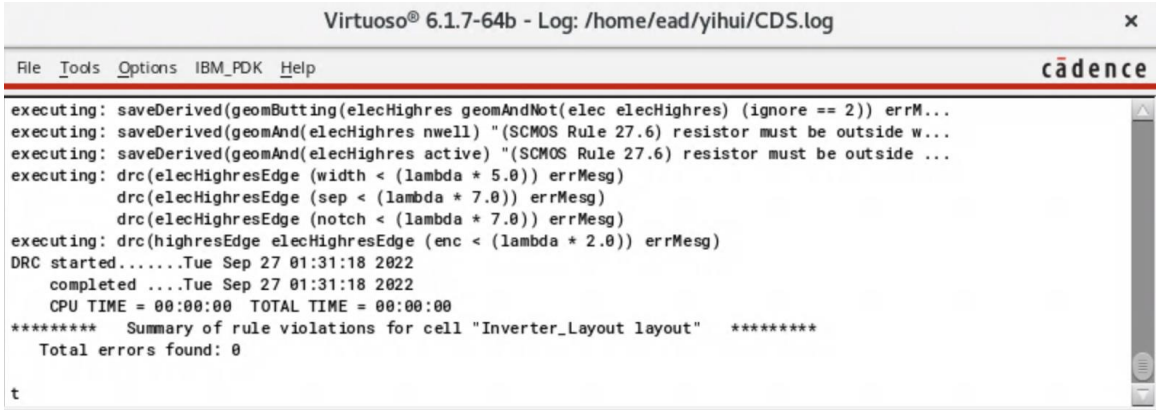

Figure 2 "DRC Errors: 0" Window

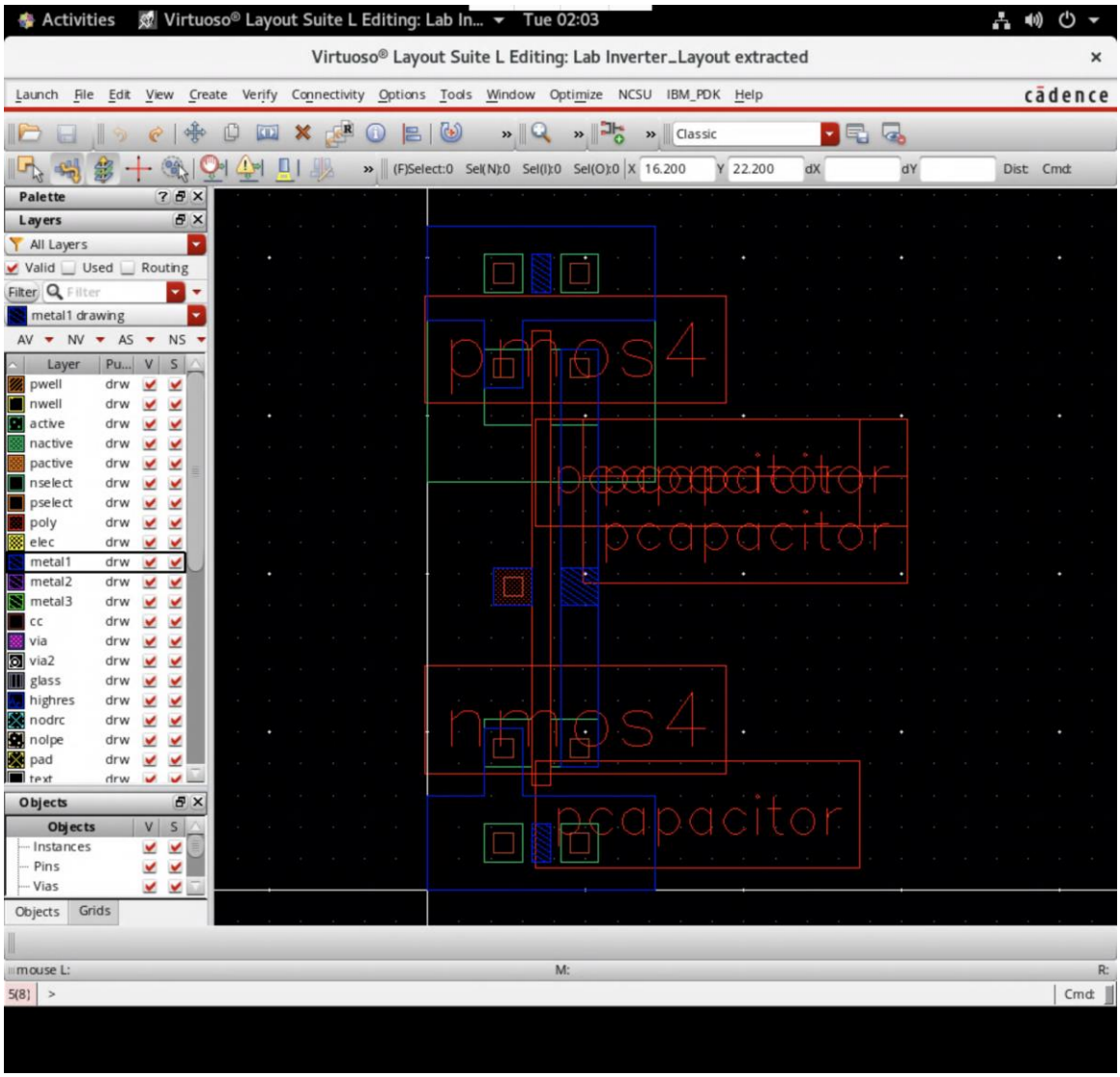

Figure 3 Extracted block layout

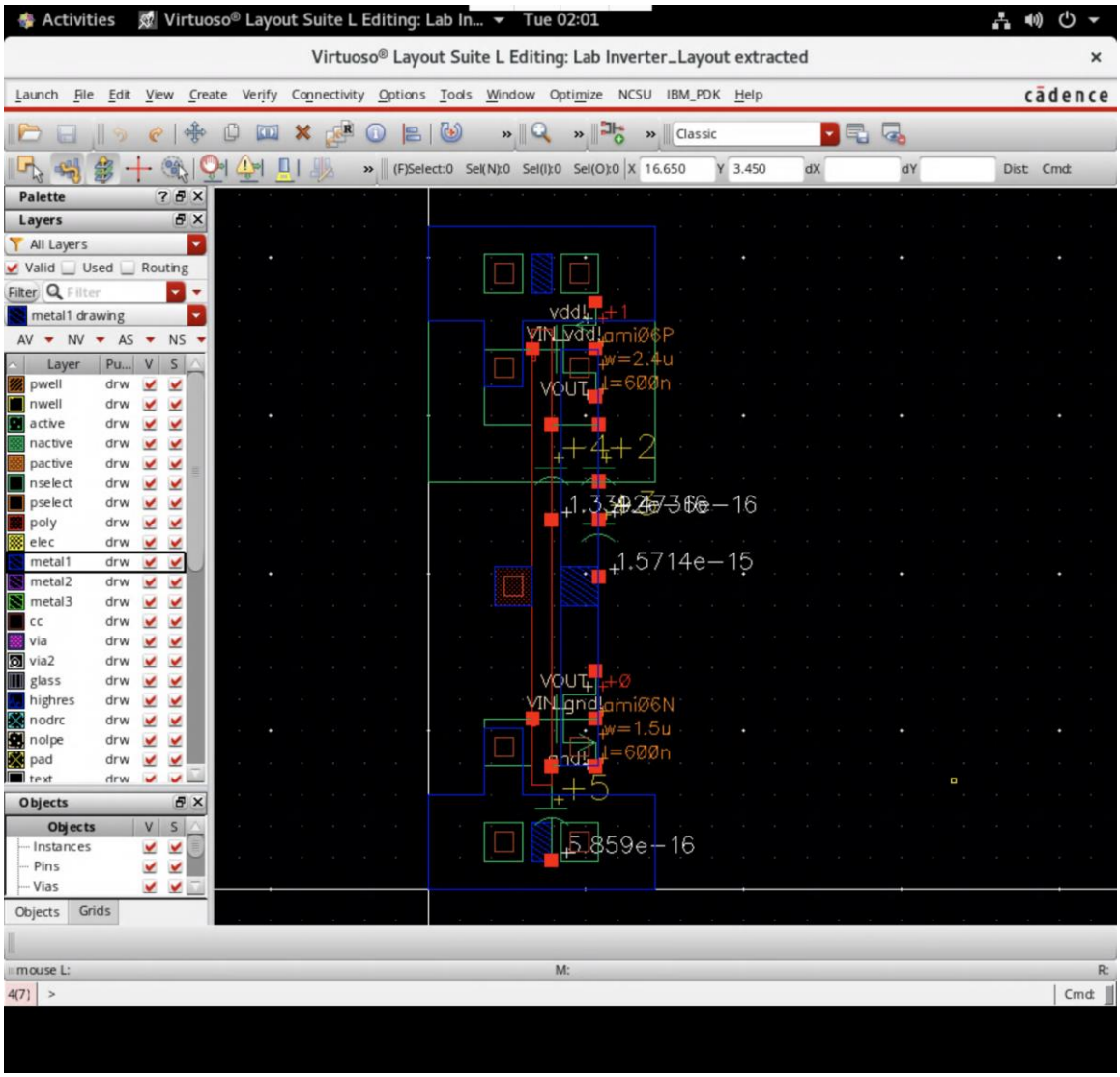

Figure 4 Extracted parasitic layout

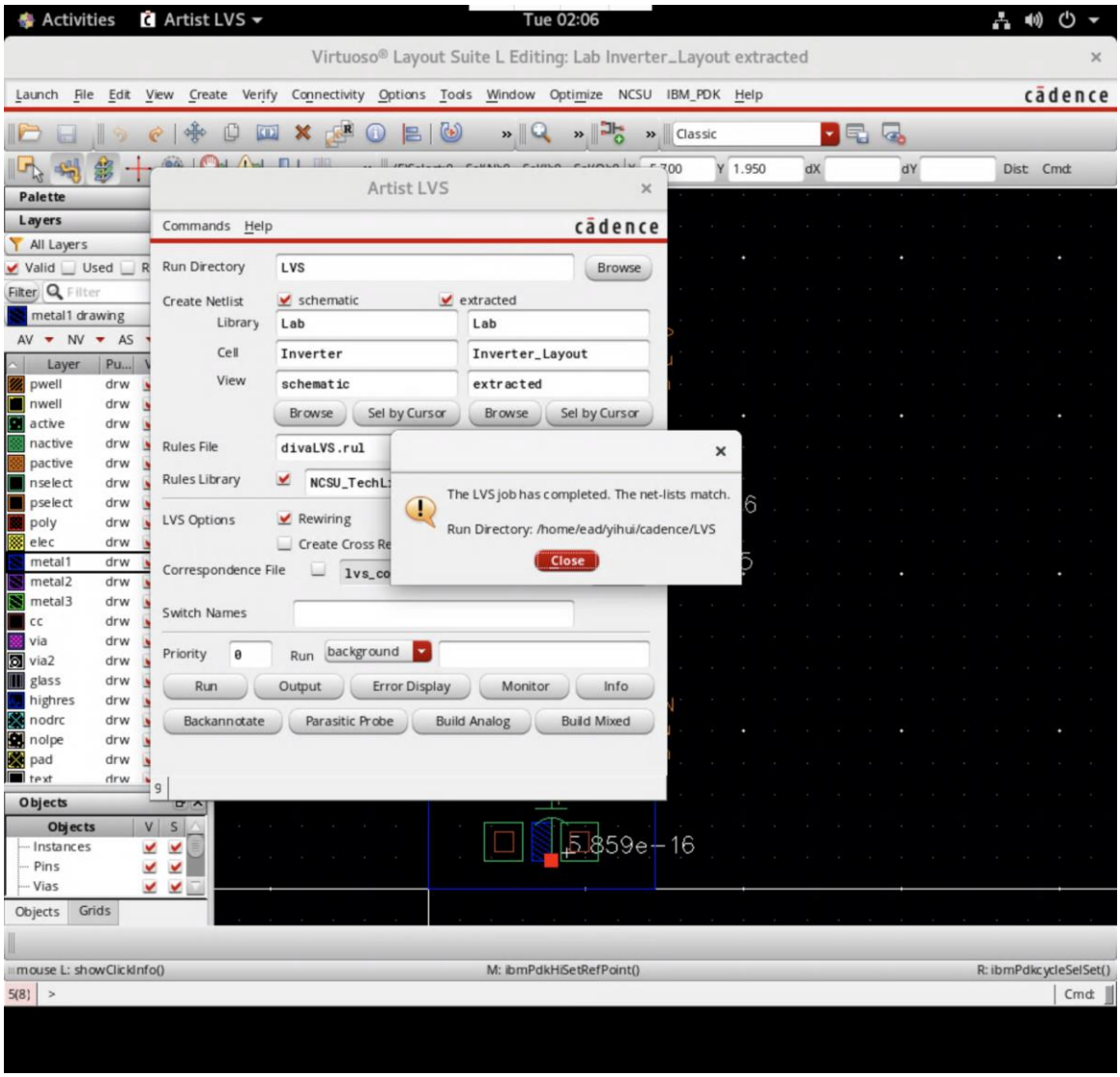

Figure 5 LVS Match Window