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ECE 6240

Lab#3 Inverter Layout, DRC, Extraction, & LVS

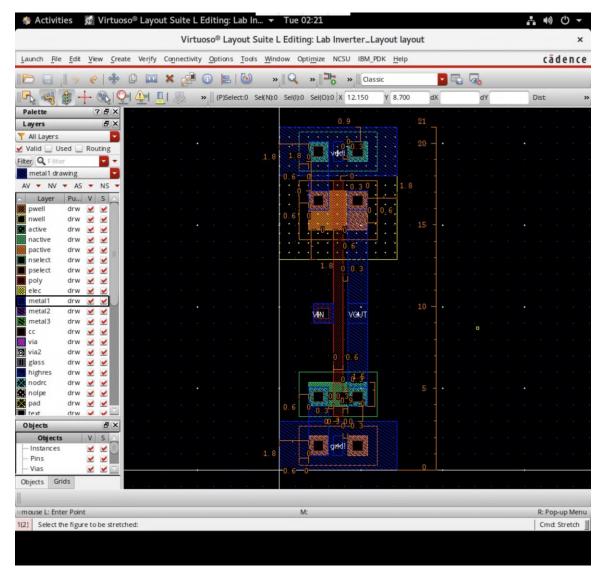


Figure 1 Overall completed layout

```
Virtuoso® 6.1.7-64b - Log: /home/ead/yihui/CDS.log

x

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cadence

executing: saveDerived(geomButting(elecHighres geomAndNot(elec elecHighres) (ignore == 2)) errM...

executing: saveDerived(geomAnd(elecHighres nwell) "(SCMOS Rule 27.6) resistor must be outside w...

executing: saveDerived(geomAnd(elecHighres active) "(SCMOS Rule 27.6) resistor must be outside ...

executing: drc(elecHighresEdge (width < (lambda * 5.0)) errMesg)

drc(elecHighresEdge (sep < (lambda * 7.0)) errMesg)

executing: drc(highresEdge (notch < (lambda * 7.0)) errMesg)

executing: drc(highresEdge elecHighresEdge (enc < (lambda * 2.0)) errMesg)

DRC started......Tue Sep 27 01:31:18 2022

CPU TIME = 00:00:00 TOTAL TIME = 00:00:00

************ Summary of rule violations for cell "Inverter_Layout layout" **********

Total errors found: 0
```

Figure 2 "DRC Errors: 0" Window

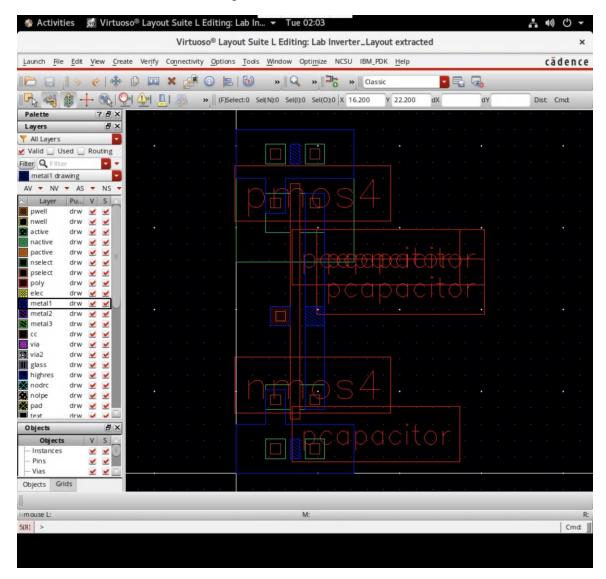


Figure 3 Extracted block layout

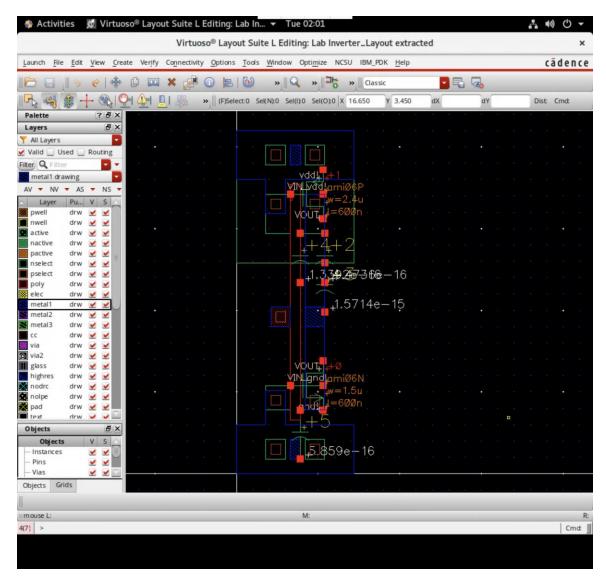


Figure 4 Extracted parasitic layout

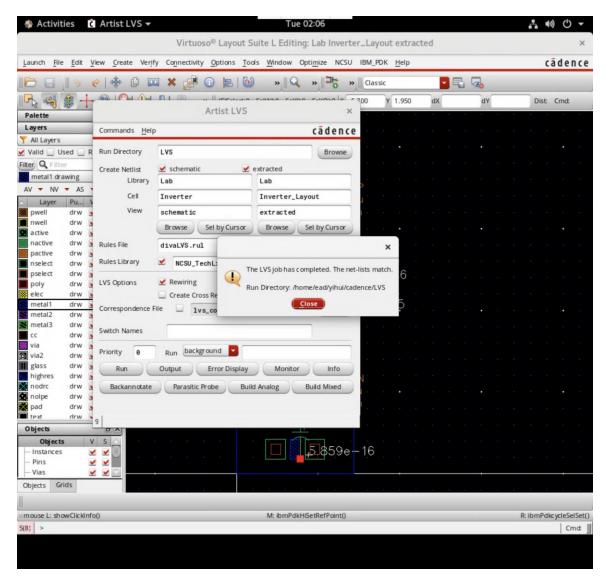


Figure 5 LVS Match Window