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October 11, 2022

ECE 6240

Lab#4+5 NAND gate Schematic + Test Bench + Simulation (DC + VTC) + Layout

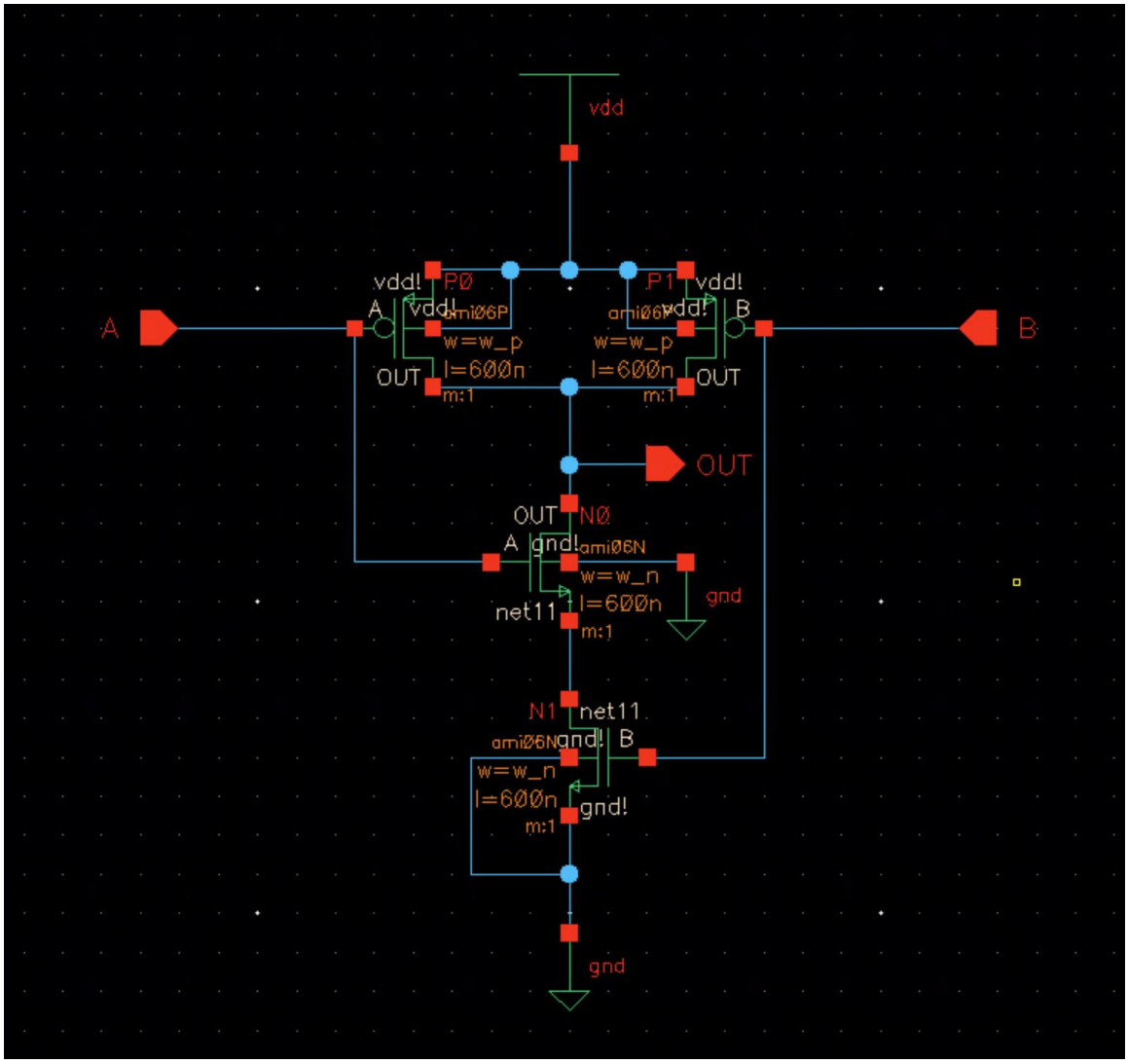

Figure 1 Schematic

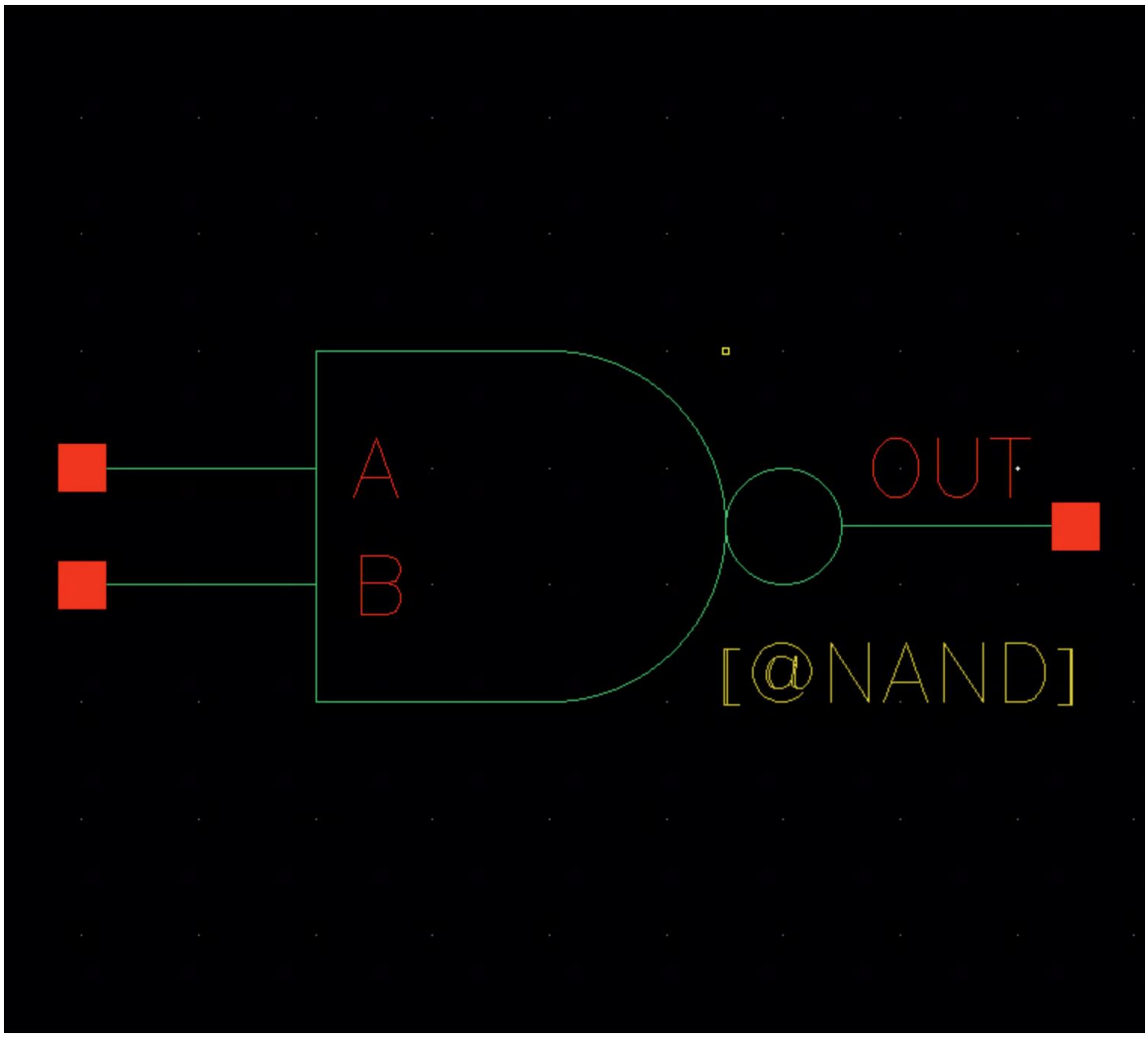

Figure 2 Symbol

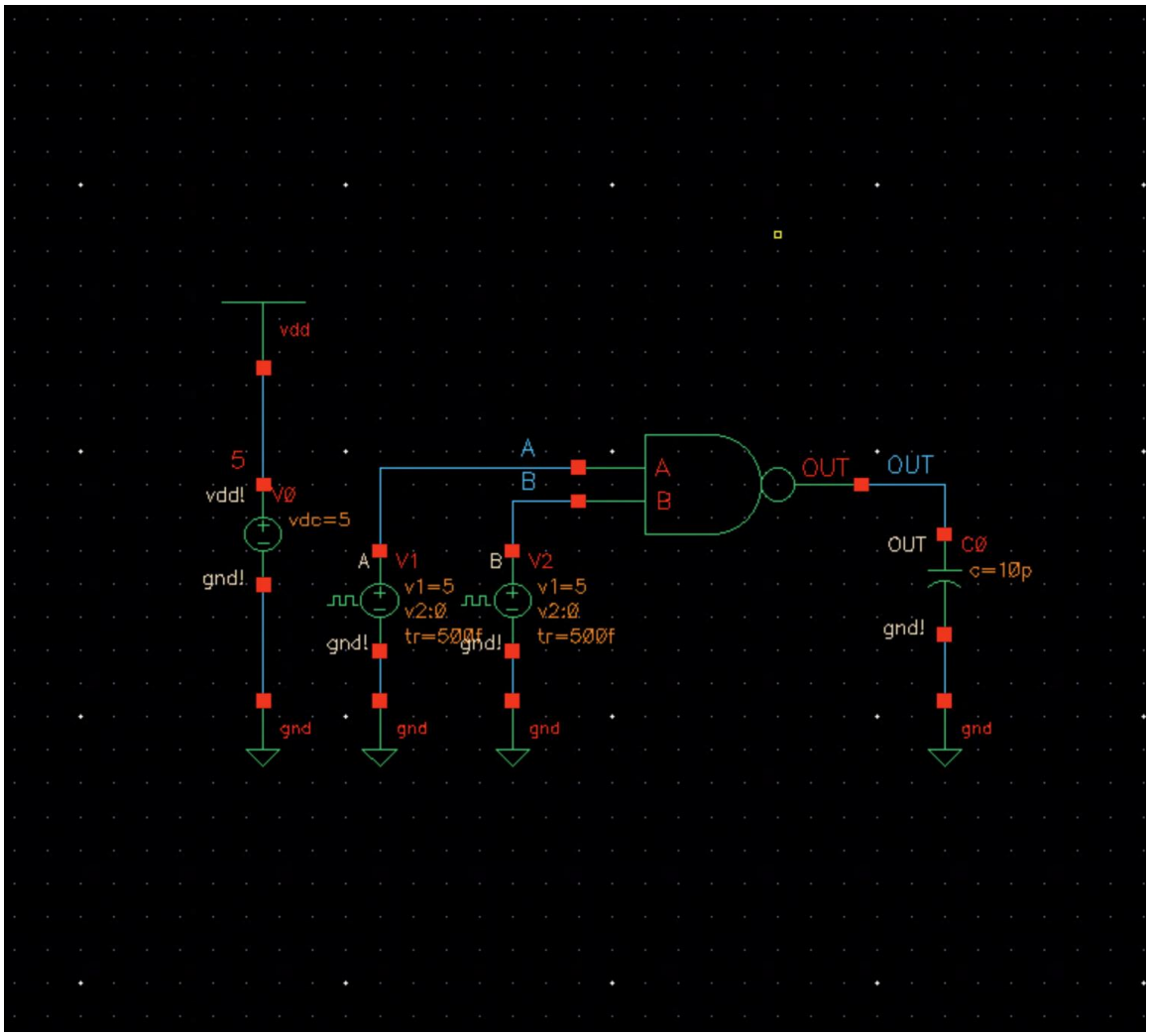

Figure 3 Testbench schematic

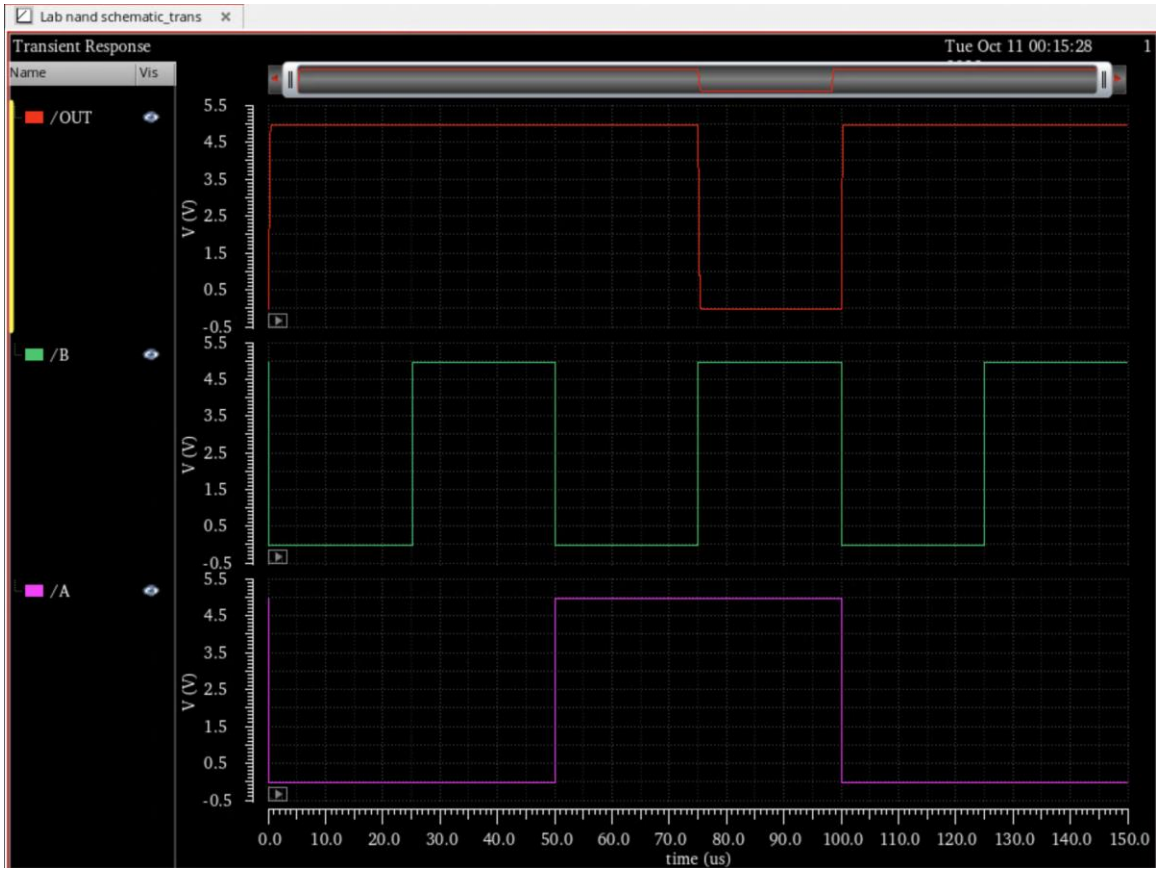

Figure 4 Transient Simulation

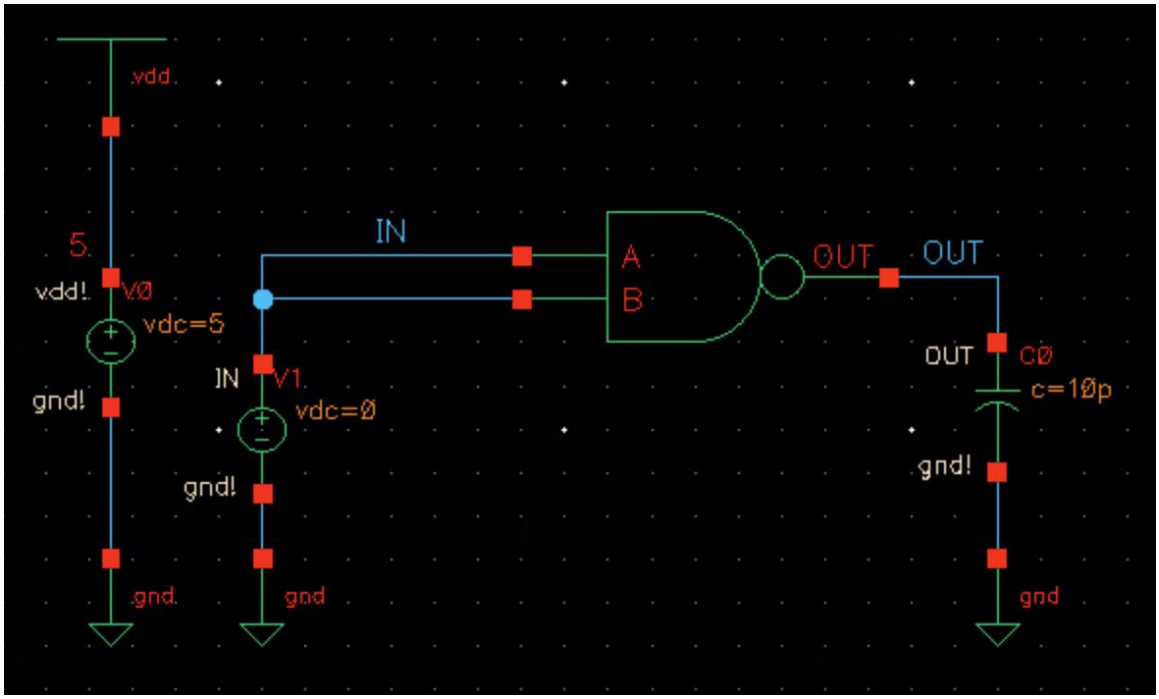

Figure 5 VTC Testbench Schematic

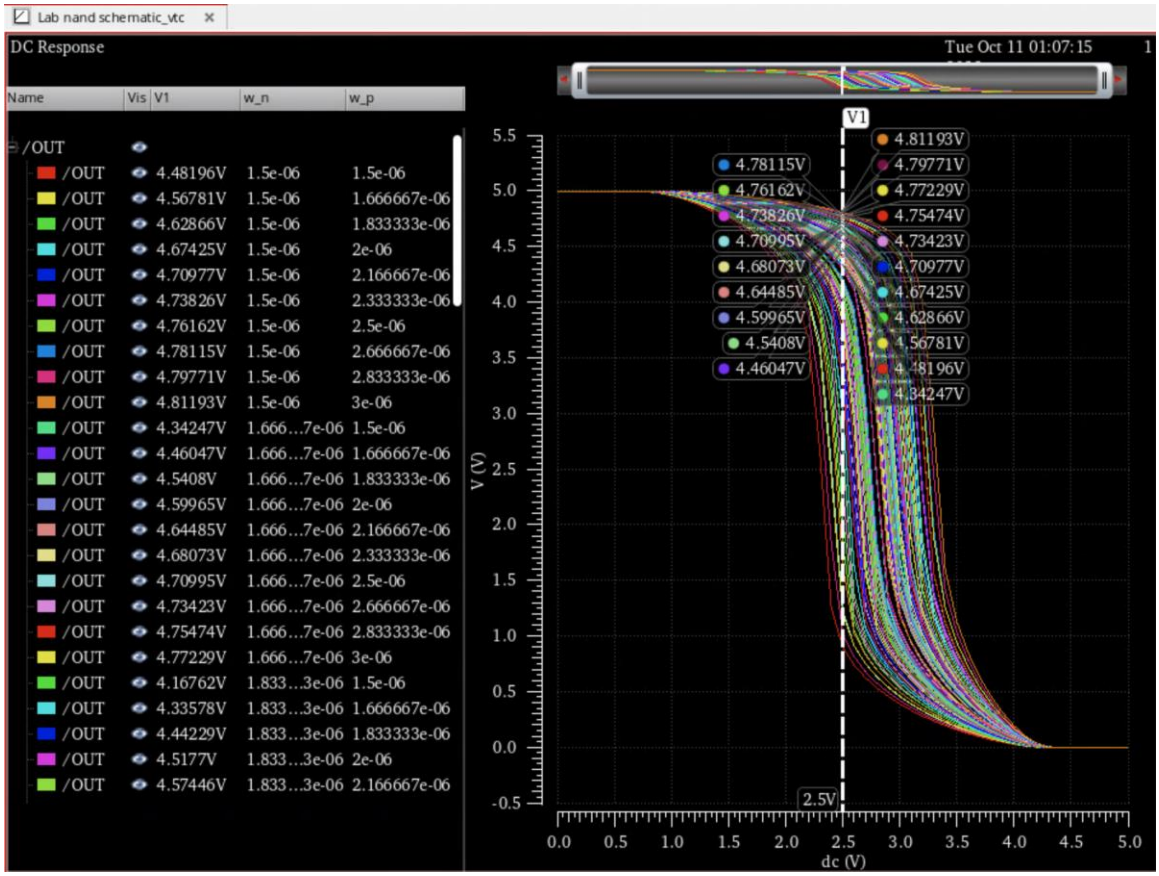

Figure 6 VTC DC Sweep, both transistors varied

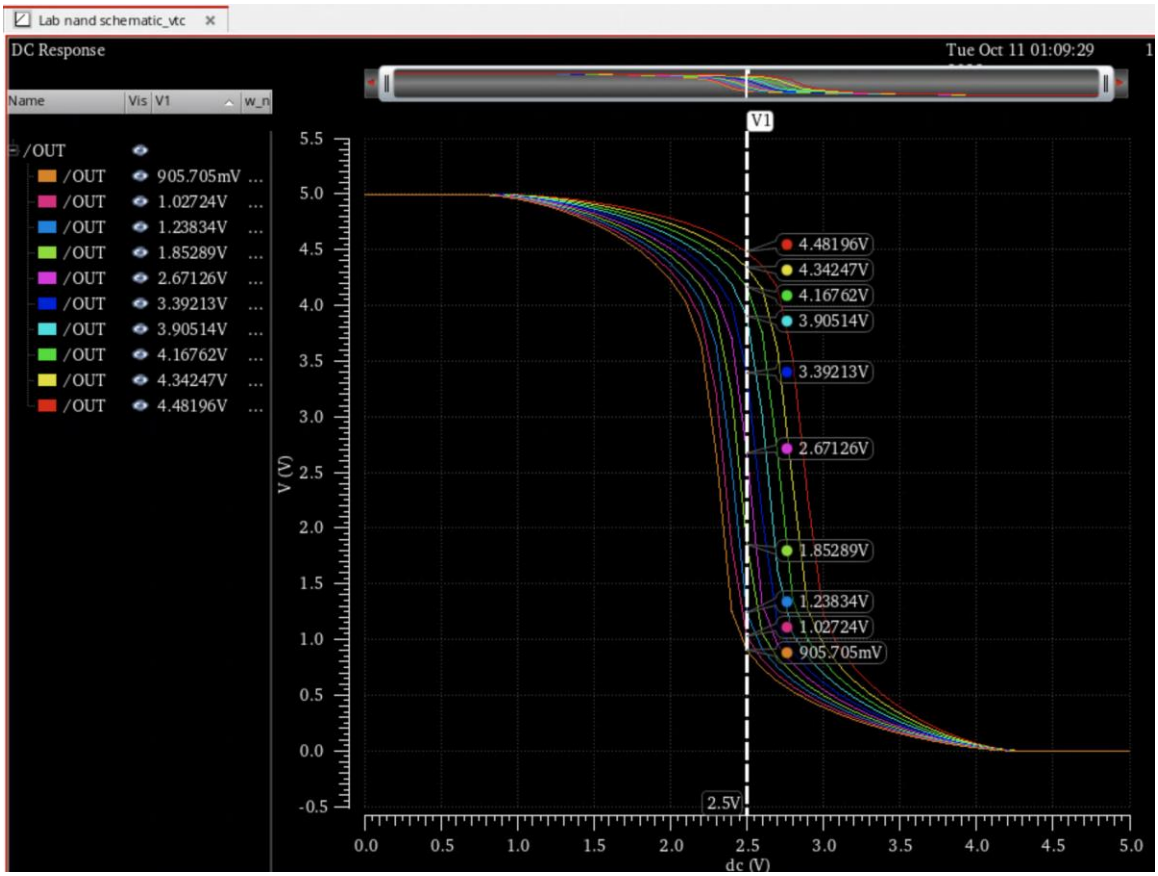

Figure 7 VTC DC Sweep, w_n varied

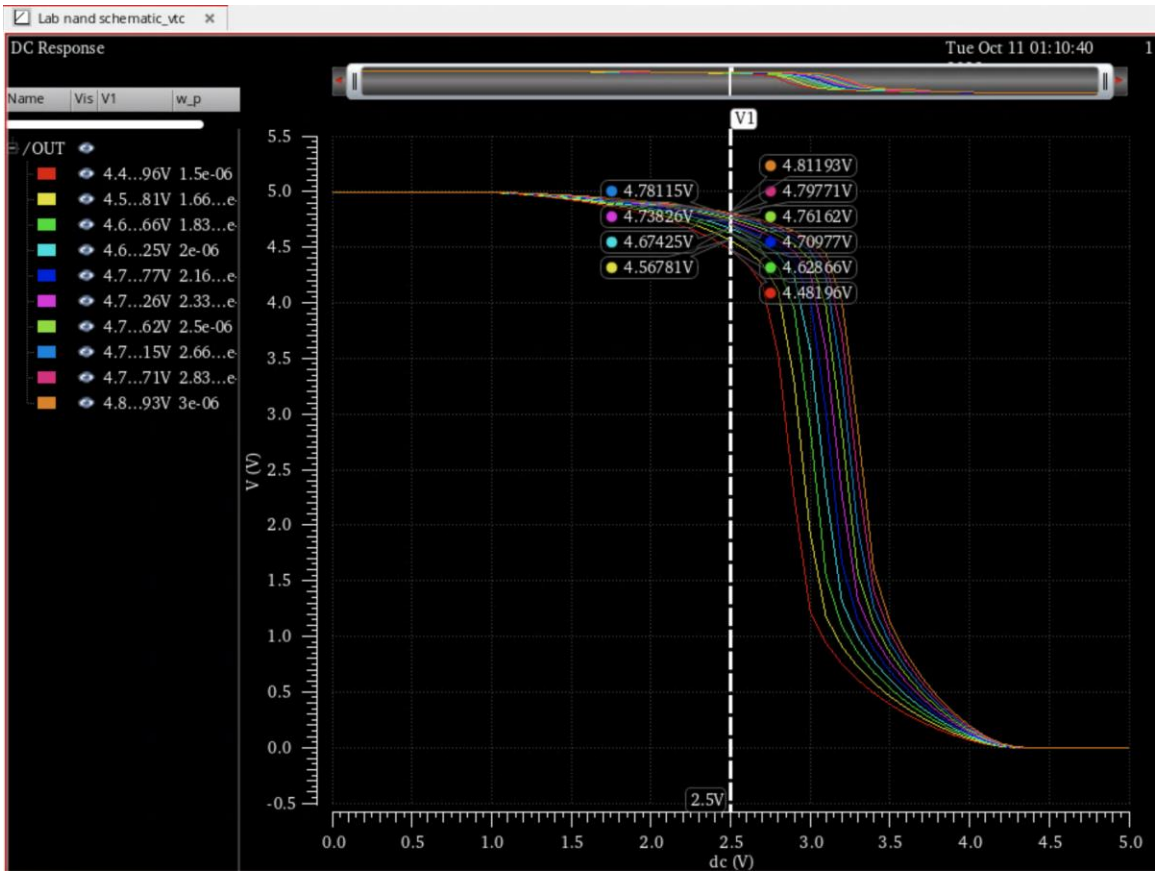

Figure 8 VTC DC Sweep, w_p varied

With w_p=1.5u and w_n=2.3u, we can get 2.5v-2.67v.

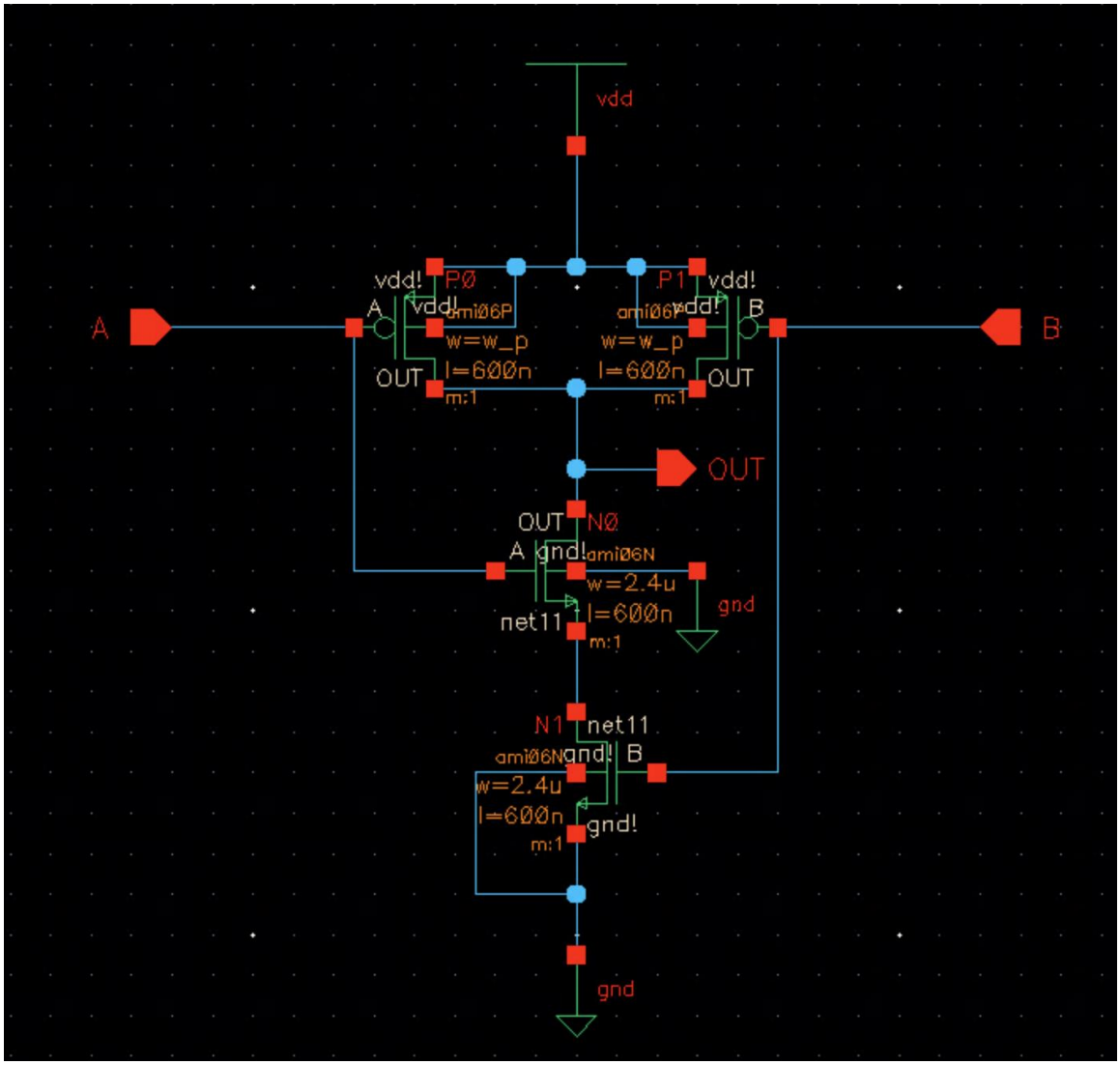

Figure 9 Schematic with new width

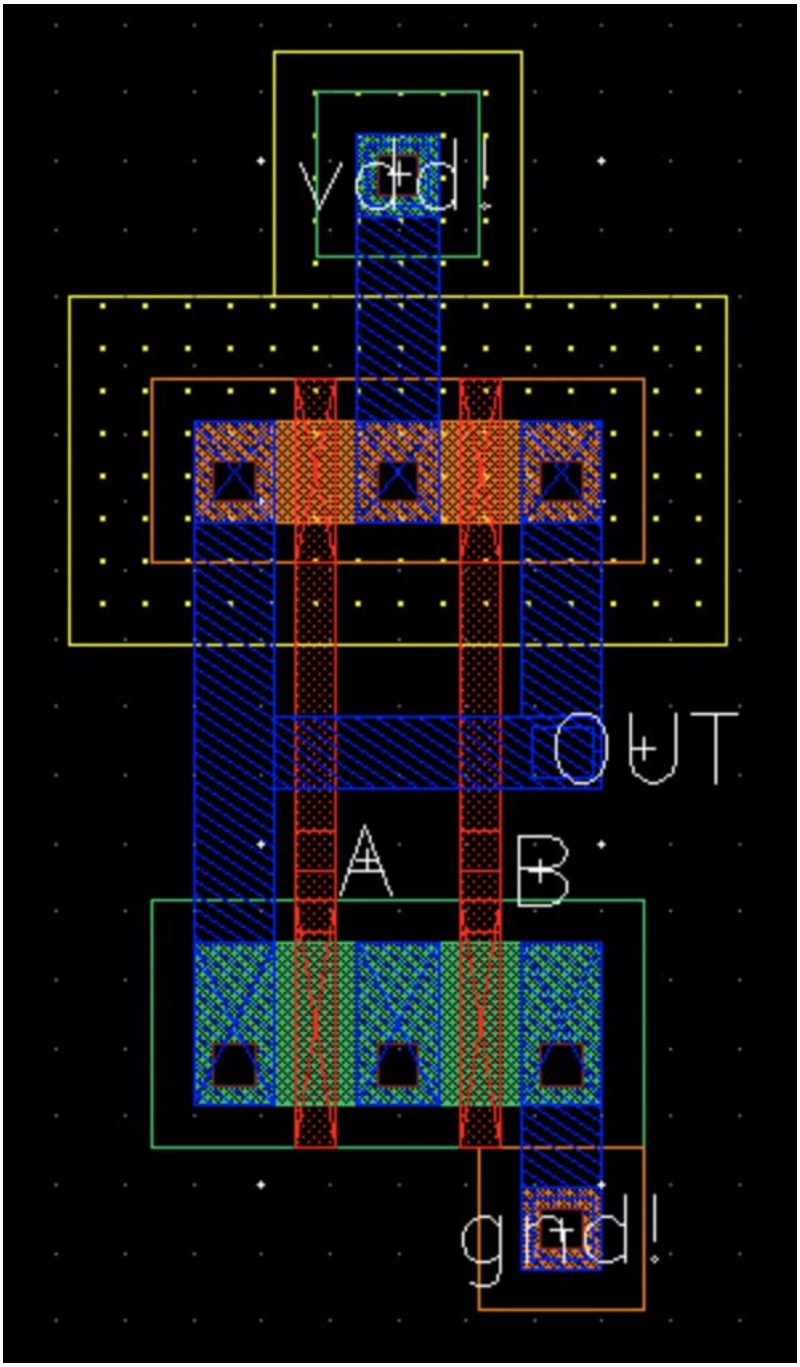

Figure 10 Layout

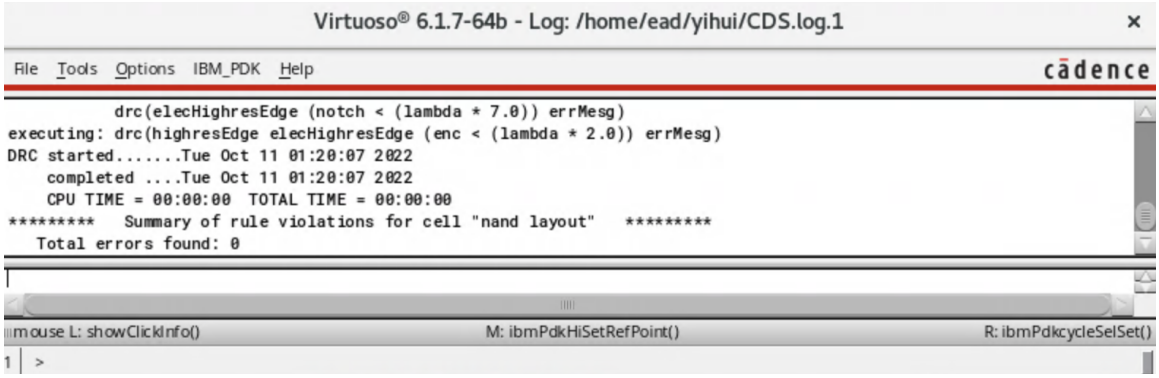

Figure 11 DRC Result

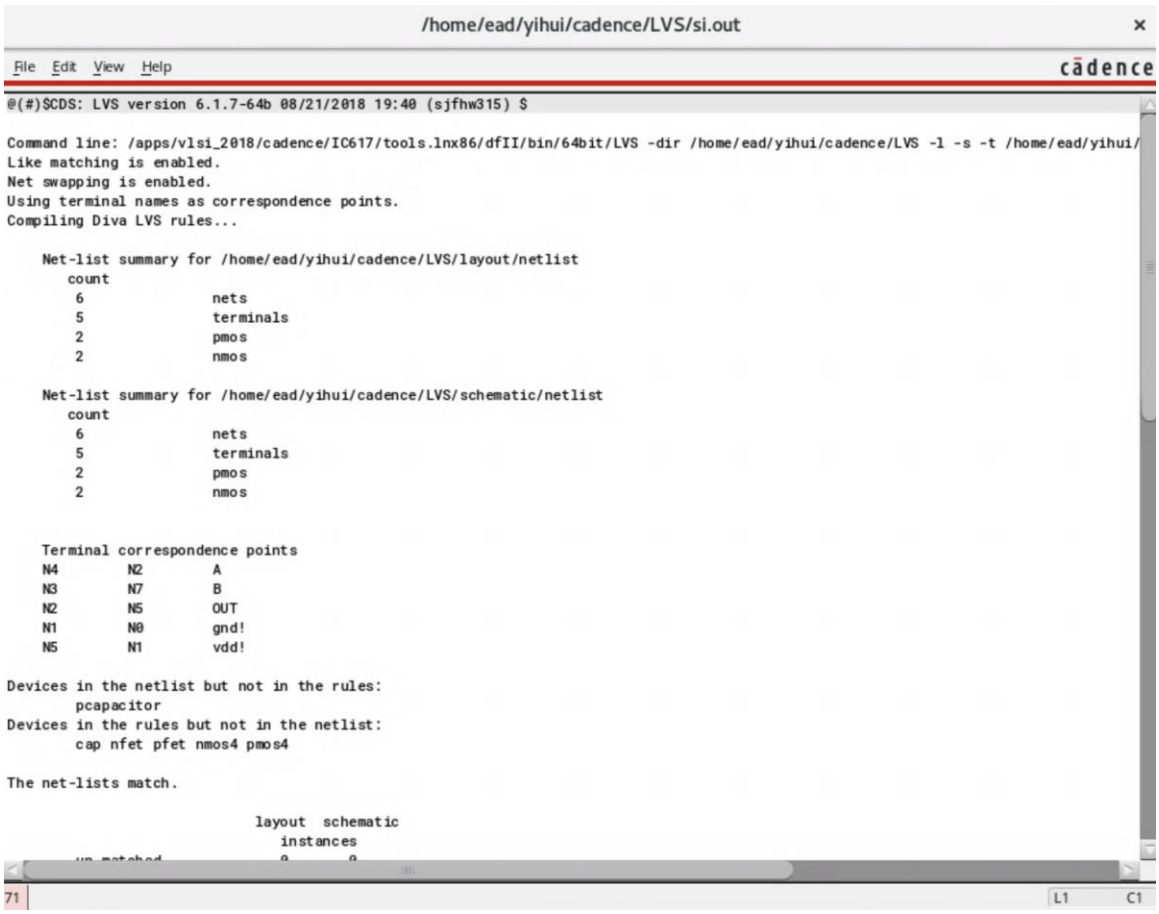

Figure 12 LVS Match

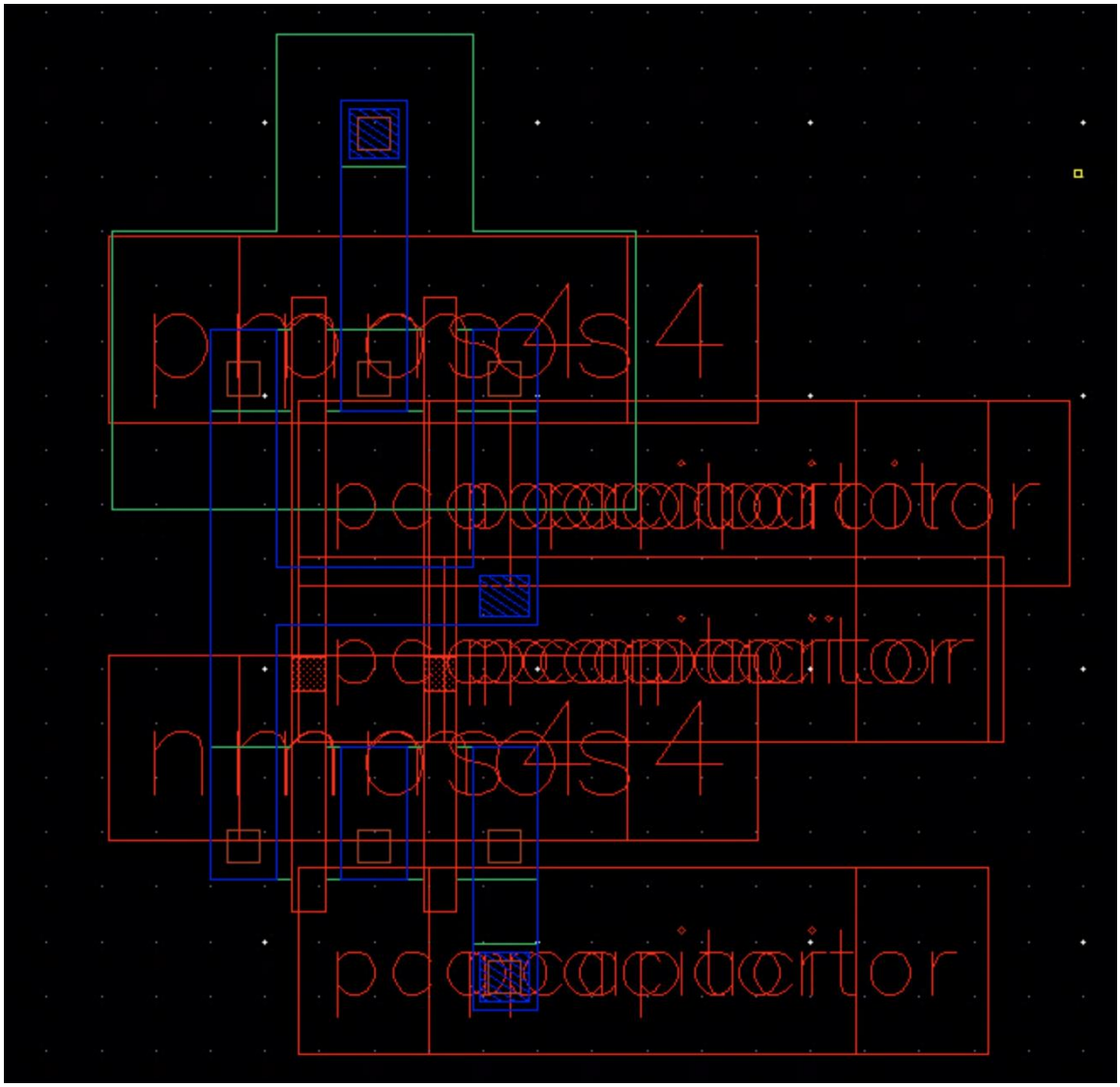

Figure 13 Extracted Layout