Yihui Wang

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ECE 6240

Lab#8 Interconnect Delay Optimization

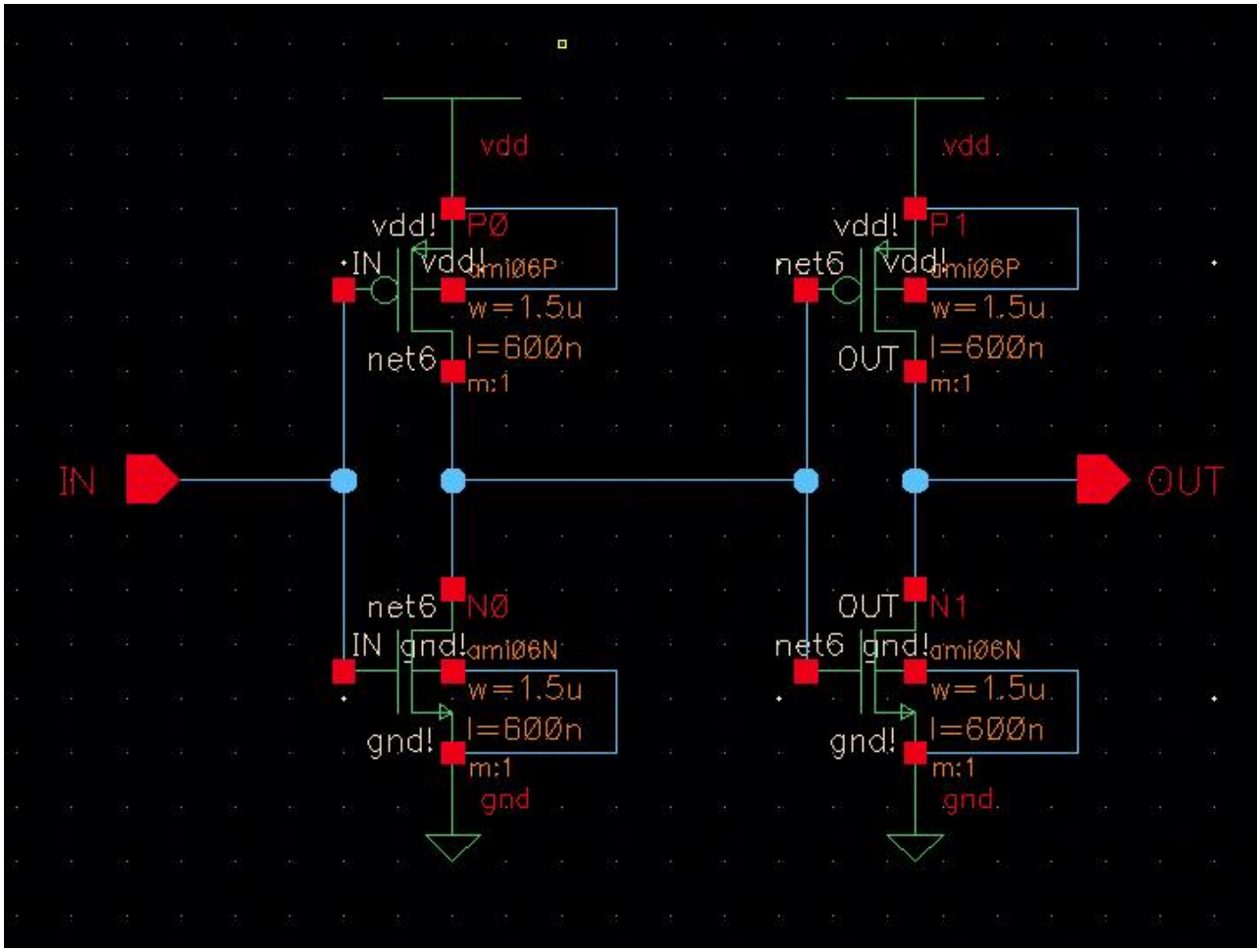

Figure 1 Schematic of Buffer

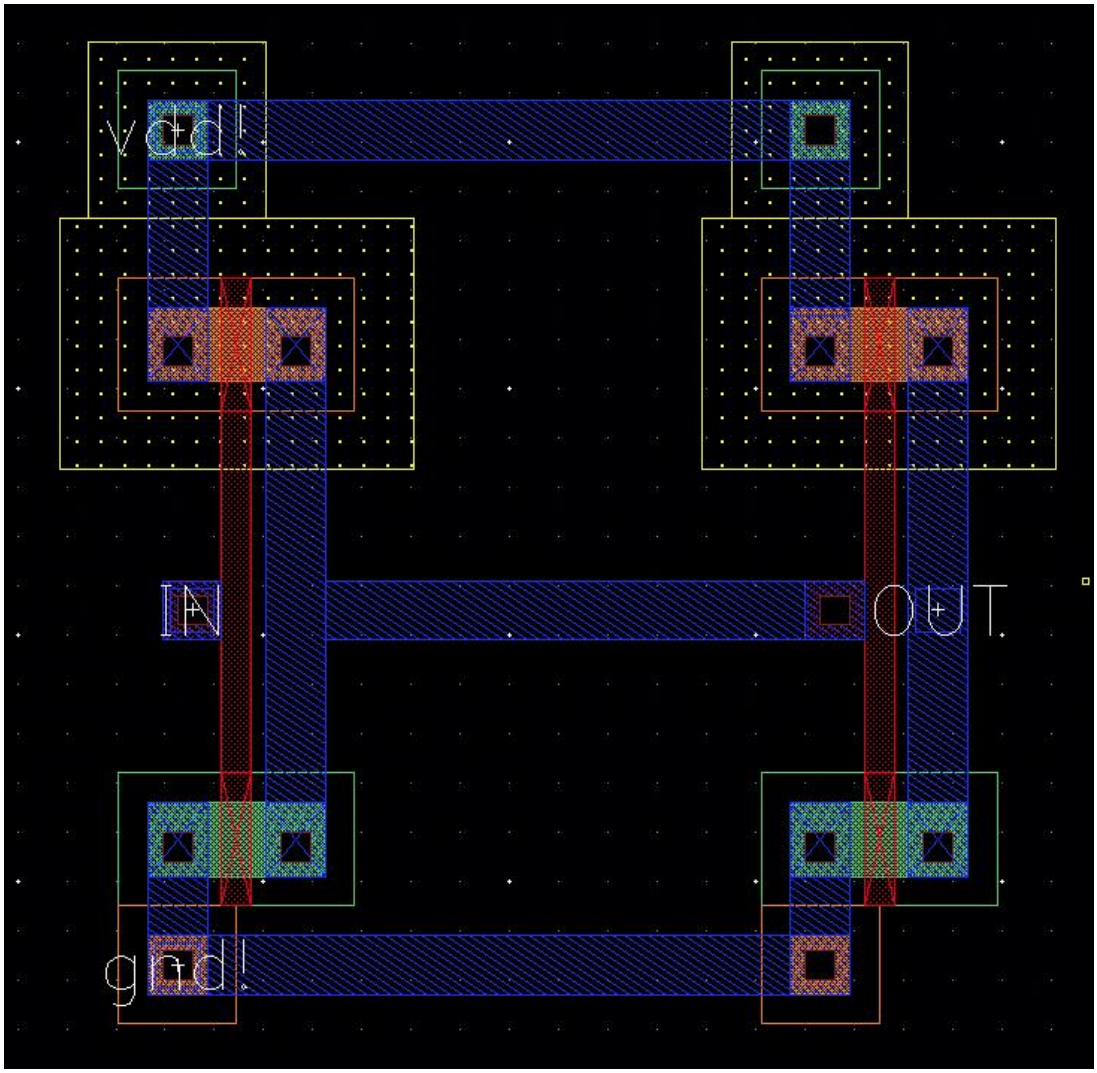

Figure 2 Layout of Buffer

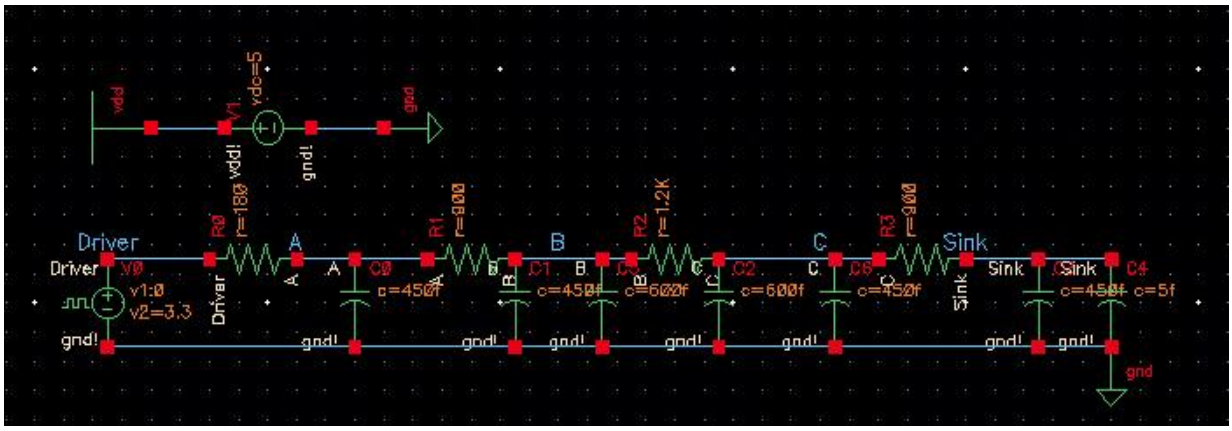

Figure 3 Schematic of Testbench

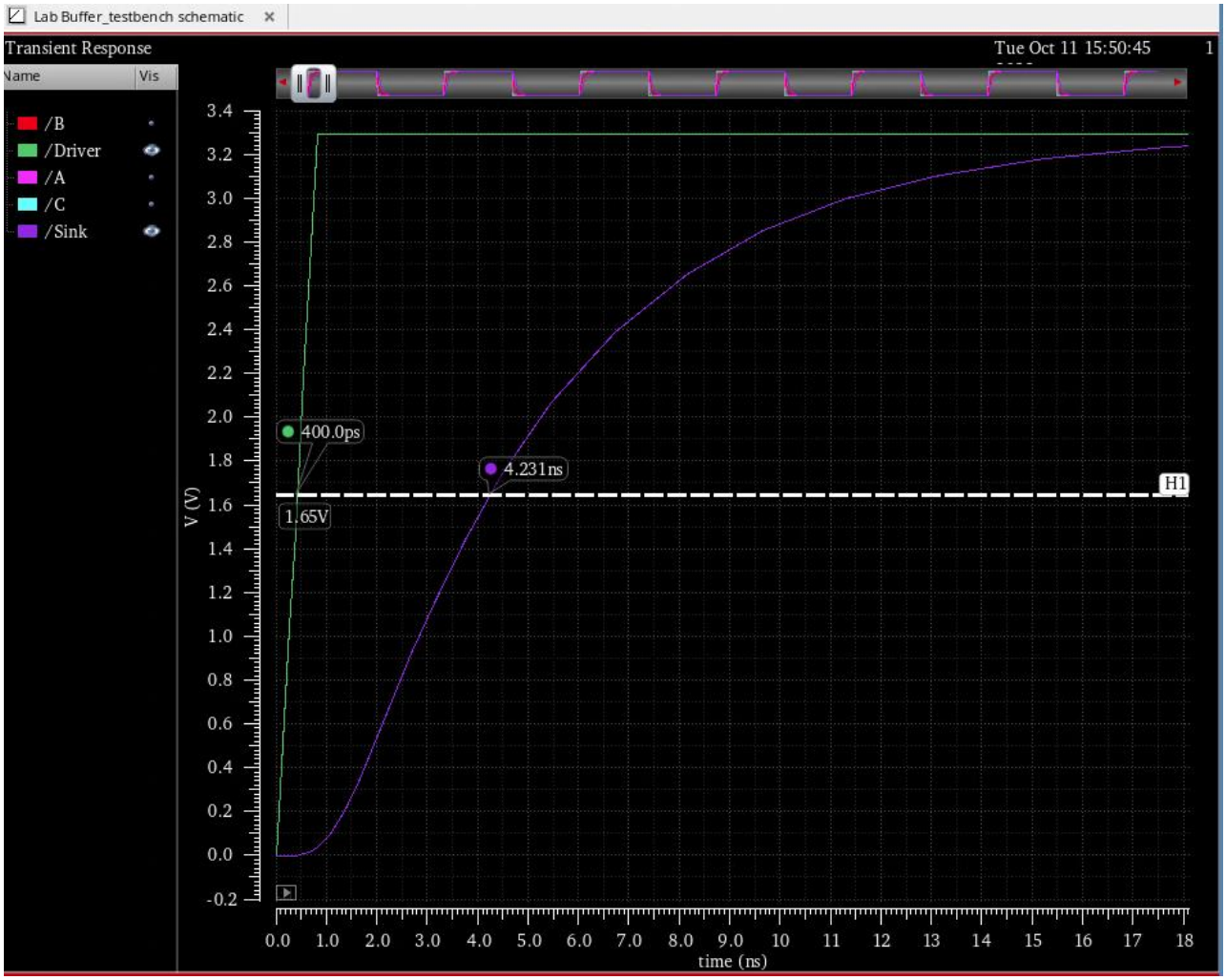

Figure 4 Without Buffer delay is 4.231ns – 400ps=3.832ns

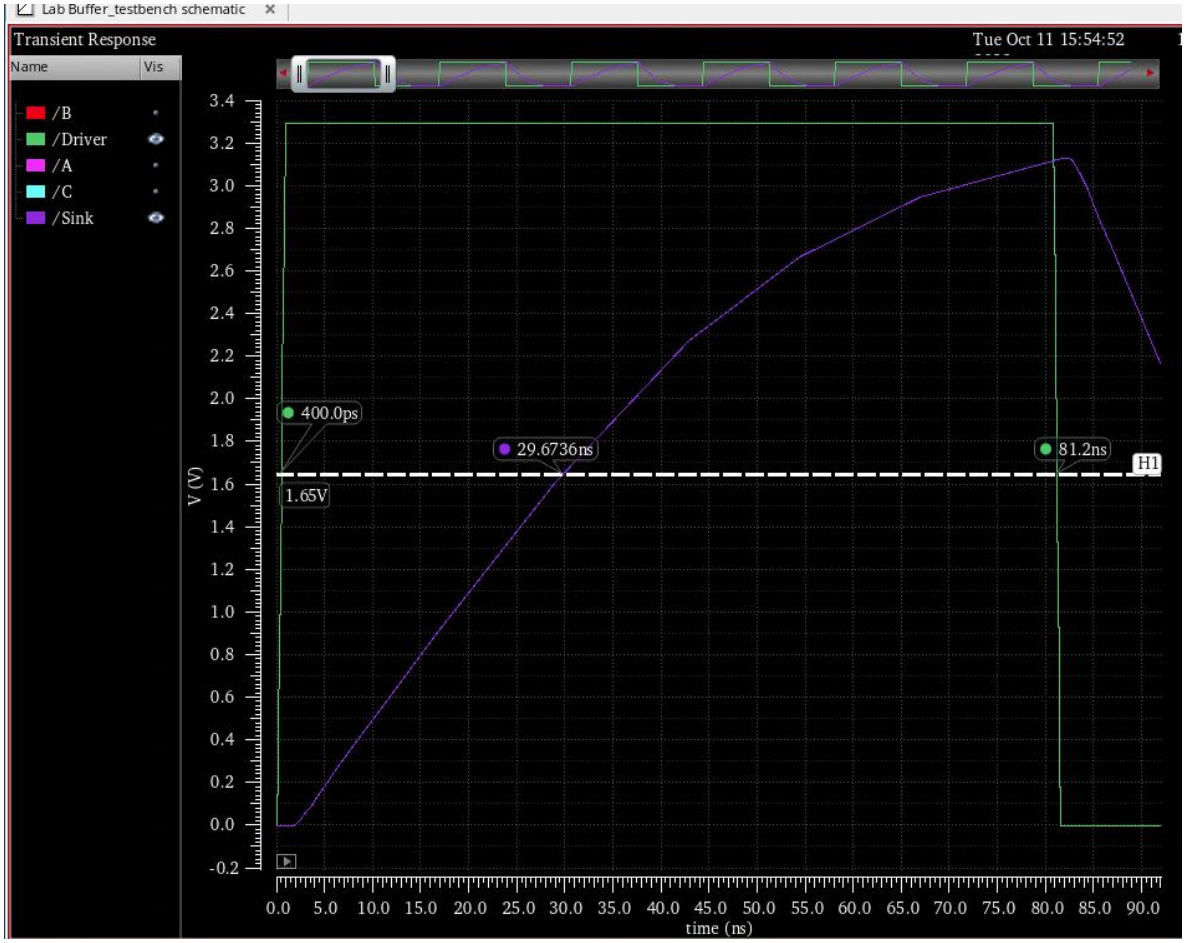

Figure 5 With Buffer Inserted in B the delay is 29.6736ns-400ps=29.2736ns

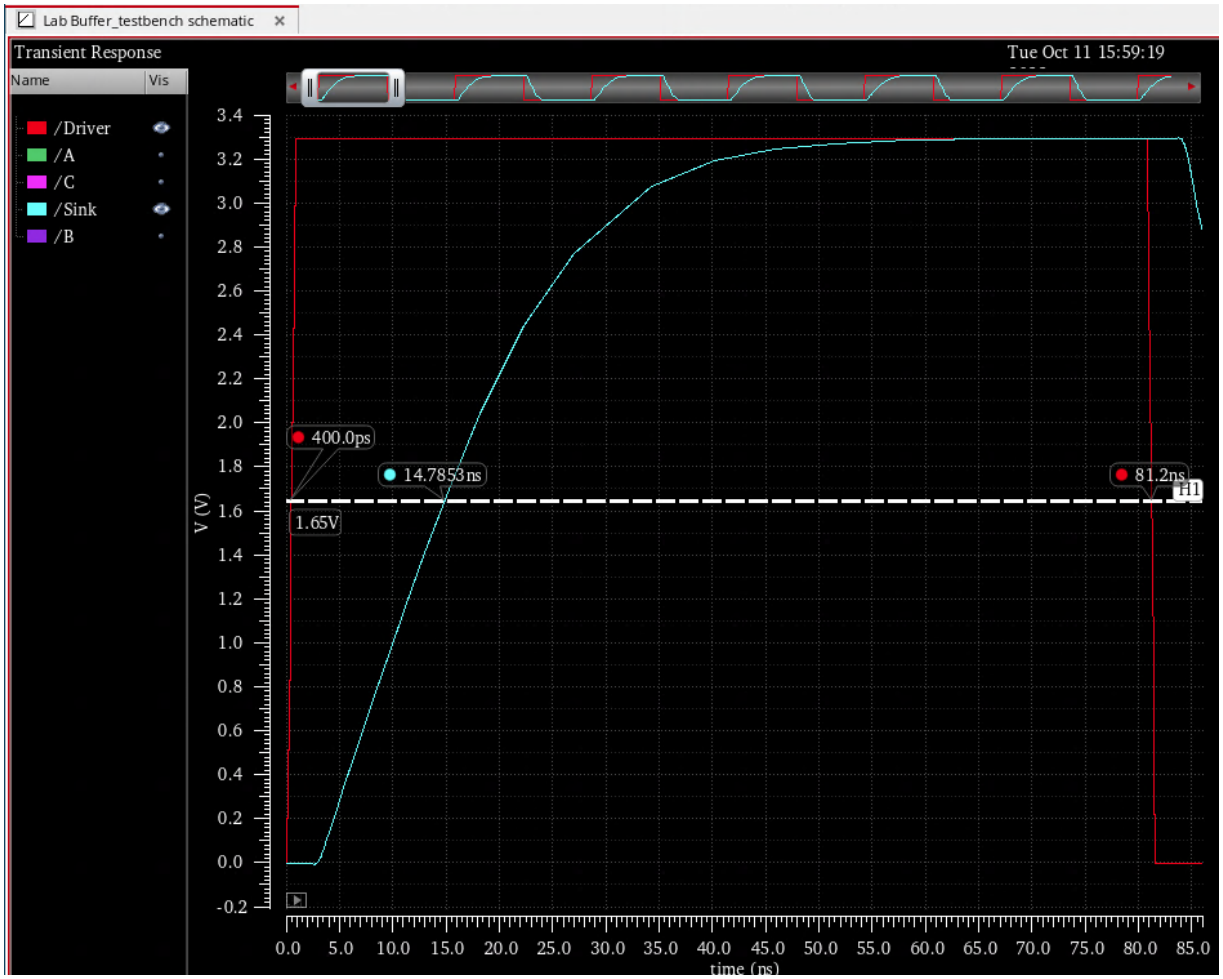

Figure 6 With Buffer Inserted in C the delay is 14.7853ns-400ps=14.3853ns

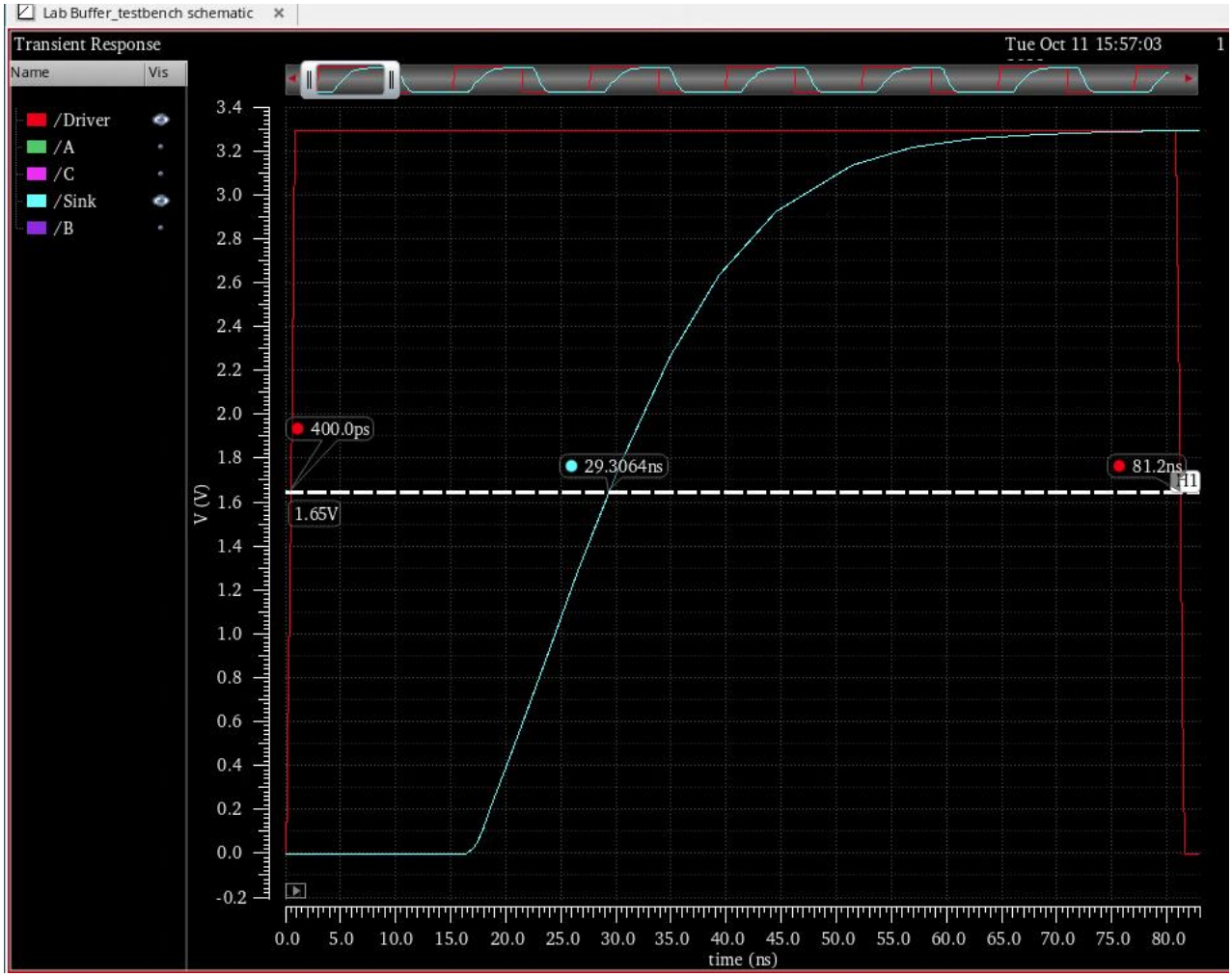

Figure 7 With Buffer Inserted in both B and C the delay is 29.3064ns-400ps=28.9064ns