# ALD Process for Top-Gating 2D Materials

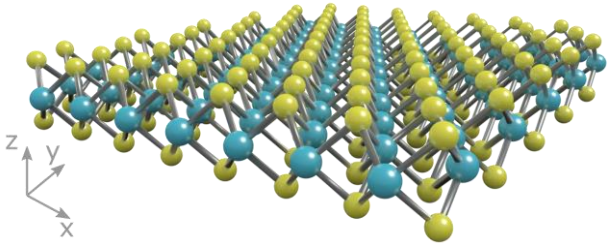
## ENGR241 Project Proposal

Project Members: Akash Levy, Jung-Soo Ko

Mentor: Michelle Rincon, Vijay Narasimhan, J Provine

# Motivation

- Many research groups are studying 2D materials at Stanford
  - Poplab (EE)
  - Evan Reed group (MATSCI)
  - Saraswat group (EE)
  - More…

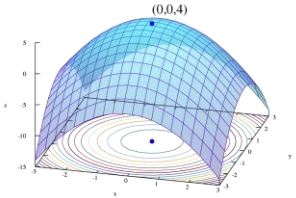



- For 2D FET devices, ALD is needed to produce high-quality gate dielectrics for CMOS integration which groups in Stanford want to develop
- Process flow involves metal buffer layer for adhesion and other tricks (plasma-enhanced) that are not currently documented anywhere for SNF members
- No optimization of the processes for high-quality TMD gate dielectrics that is essential in today's devices

# Aim & Goals

- To develop and document process flow for ALD top-gating on *transition metal dichalchogenides (TMDs), e.g.* $MoS_2$, $WSe_2$
- Aiming for reliable and controlled growth of high-k materials
- Optimization of process parameters/conditions for best film quality/electrical properties
- Will make data available to lab members via wiki page

Process Flow Development




Parameter Optimization

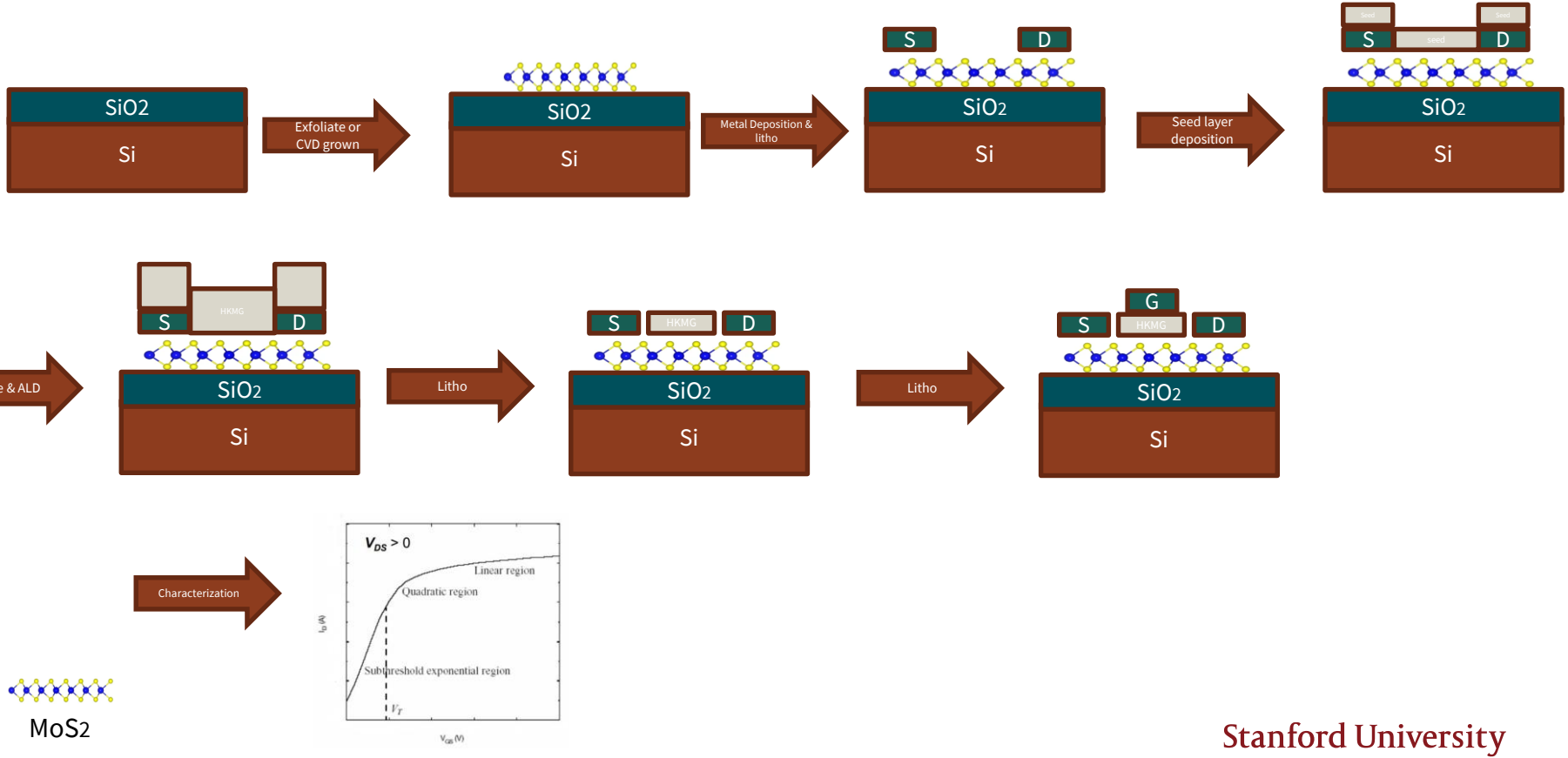
Comprehensive Documentation

SNF Database

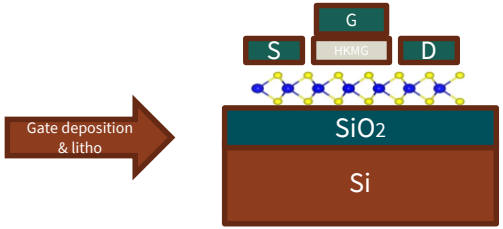
# Process Flow

- Start with $MoS_2$ thin film wafers (pre-grown or exfoliated)
- Perform e-beam evaporation to deposit metal buffer layer
- ALD for high-k gate oxide
  - E-beam evaporation to deposit metal seed layer, then ALD (or)
  - ALD through Plasma-enhanced
- Patterning via photolithography
- Perform e-beam evaporation for metal top-gate contact

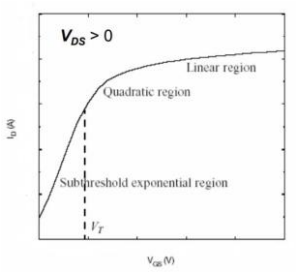
# Sample Preparation (Seed Layer)



# Sample Preparation (Thermal or Plasma)





# Parameters to Optimize

- **High-k metal oxide for buffer:** Al, Zr, Hf, (Y, Ta = Q2 stretch goal)
- **Buffer layer thickness**
- **Growth temperature**
- **Plasma-enhancement:** yes or no

- Still need to determine exact wafer splits…
  - Will be based on initial testing and feedback from people in Poplab with tribal knowledge of the currently-used recipe

- Start with standard recipe then make modification

# Characterization

- Autumn
  - AFM images for surface roughness after seeding
  - XPS for surface coverage after seeding
  - Auger Electron Spectroscopy
  - C-V Measurement with MOSCAP
- Winter
  - Typical MOSFET characterizations
  - I-V curves
  - Gate breakdown voltages
  - Other materials (if time permits)

- Will use micromanipulator for characterization (which Akash is trained on)
- Imaging will be done with help of Jung-Soo's colleagues (TEM)
- More measurements can be done to examine the film quality through Raman, SEM, PL with help of Jung-Soo's colleagues

# Tentative Timeline

| Week | Description of Activities |
|---|---|
| 2 | Jung-Soo: finishing up lab membership training<br>Akash: tool shadowing/training for Fiji, AJA, spectrometry |
| 3 | Both: tool shadowing/training for AFM, Auger, Fiji, AJA, spectrometry |
| 4 | Both: tool shadowing/training for AFM, Auger, Fiji, AJA, spectrometry |
| 5 | Finish up training, run initial experiments to determine wafer splits |
| 6 | ALD/e-beam deposition under various settings |
| 7 | Photolithographic patterning of microstructures, more ALD deposition |
| 8 | Electrical characterization and imaging |
| 9 | Adjust and continue |
| 10 | Wrap up, documentation, database compilation, planning for next quarter |

# Training Required

- Akash is a lab member and is qualified (through EE 312) on:
  - All photolithography equipment
  - Wet benches
  - Furnaces
  - Micromanipulator6000
- Jung-Soo will be a new lab member
- Both Akash and Jung-Soo need training on:
  - ALD equipment (Fiji)
  - E-beam evaporation (AJA)
  - AFM
  - XPS
  - Heidelberg
  - Auger Spectroscopy

# Tentative Budget

| Equipment Name | Training | Usage | Total $ |
|---|---|---|---|
| Fiji | 3h→ 80X3X2=$480 | $50/hX30h=$1500 | $1980 |
| SEM | 6h→ 80X6X2=$960 | $45X5h=$225 | $1185 |
| AFM | 4h→ 80X4X2=$640 | $20X5h=$100 | $640 |
| Si wafers | - | $14X10 = $140 | $140 |
| AJA e-beam | 1h→ 80X1X2=$160 | $35X10 = $350 | $510 |
| Heidelberg | 2h→ 80X2X2=$320 | $35X2 = $70 | $390 |
| | | | $4890 |

# Recap of Deliverables

- Wiki page on optimized process flow for top-gating 2D materials
  - Best conditions for each top-gate material will be specified
  - Optimal seed layer thickness for thin gate will be specified
  - Optimal thickness to protect TMDs from plasma will be specified
  - Recipes will be made available to lab members on the equipment
- Electrical characterization data (raw and summarized) will be made available to lab members via database
  - I-V curves
  - C-V curves
  - Gate breakdown voltage
- All imaging data taken will be made available to lab members in raw and summarized form
  - AFM
  - XPS
  - Auger Spectroscopy

# Thank you!

QUESTIONS?