Spring 2017
CSE334 Microprocessors Quiz 1

Below are the values of some timer registers in the MC9S12:

TIOS	TSCR1	TCTL1	TCTL2	TCTL3	TCTL4	TIE	TSCR2	TFLG1	TFLG2
32	80	A4	C2	5F	76	2C	84	52	00

(a) Which timer channels are being used for output compare?

ch1,ch4,ch5

(b) Which timer channel interrupts are enabled?

ch5,ch3,ch2

(c) What action is timer channel 2 set to perform? (i.e., if it is set up as input capture, which edge will it capture; if it is set up as output compare what action will occur when TCNT equals TC2?)

TCTL4- 11 -> Input capture both edges

(d) What action is timer channel 3 set to perform?

TCTL4 -> 01 -> Input capture in rising edge

(e) What action is timer channel 4 set to perform?

TCTL1 -> 00 -> Not used.

(f) What action is timer channel 5 set to perform?

TCTL1 -> 01 -> Reverse the bits in TC5

(g) Which timer flags are set? What are they mean?

Flag bit 1, 6, 4. These flags being set when tcnt = tcx. For example, flag bit 6 has been set, so TCNT = TC6 AT LEAST ONE TIME. Flag should've been clear, so we can capture tcnt=tc6 again.

(h) What is the timer prescaler set at – i.e., by what factor will the processor clock be divided before driving the TCNT register?

2^4 = 16 . When driving processor, oscillator speed reduce 2 times, after that main speed reduce 16 times because of prescaler. 32 times slower.

(i) How long (in seconds) will it take for the TCNT register to overflow?

Let's say microp. has 24 mhz speed.
24 / 32 = 0.75 mhz
0.75 (1/sec) * 10^6 cycle = 750000 cycle/sec
1 sec-> 750000cycle, 65536 cycle = x sec
x= 0.08738 sec

(j) What is the maximum frequency for a square wave so that you can detect it using input capture and this timer settings?

Text

3.3.6 TSCR1 — Timer System Control Register 1

Register offset: $_06

	BIT7	6	5	4	3	2	1	BIT0
R	TEN	TSWAI	TSFRZ	TFFCA	0	0	0	0
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-6 Timer System Control Register 1 (TSCR1)

3.3.13 TFLG2 — Main Timer Interrupt Flag 2

Register offset: $_0F

	BIT7	6	5	4	3	2	1	BIT0
R	TOF	0	0	0	0	0	0	0
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-13 Main Timer Interrupt Flag 2 (TFLG2)

TFLG2 indicates when interrupt conditions have occurred. To clear a bit in the flag register, write the bit

3.3.10 TIE — Timer Interrupt Enable Register

Register offset: $_0C

	BIT7	6	5	4	3	2	1	BIT0
R	C7I	C6I	C5I	C4I	C3I	C2I	C1I	C0I
W								
RESET:	0	0	0	0	0	0	0	0

Figure 3-10 Timer Interrupt Enable Register (TIE)

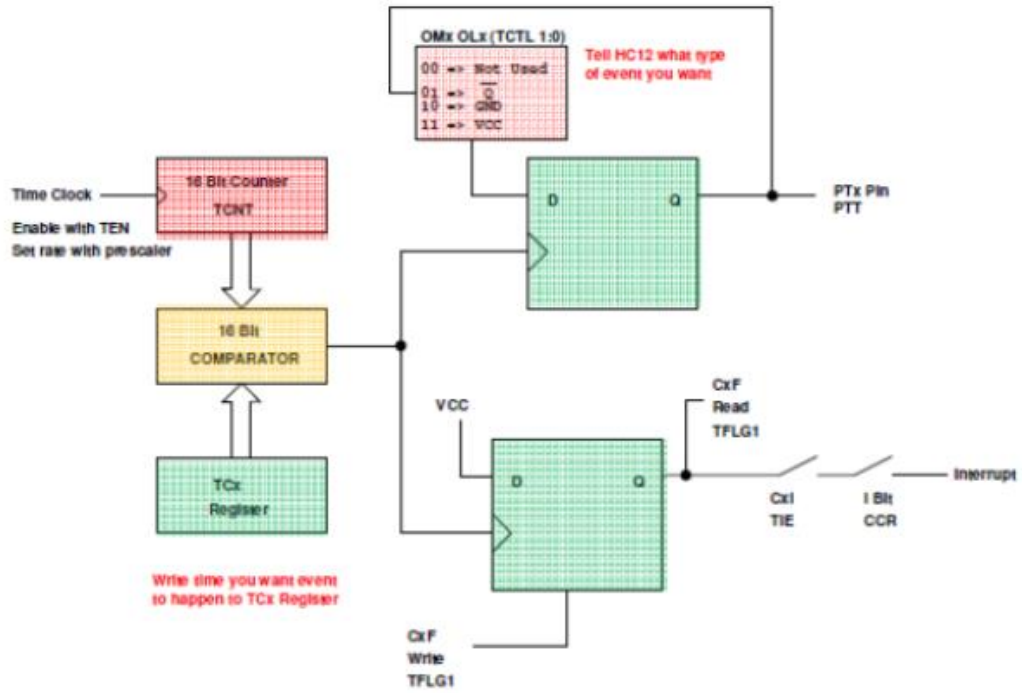
3.3.11 TSCR2 — Timer System Control Register 2

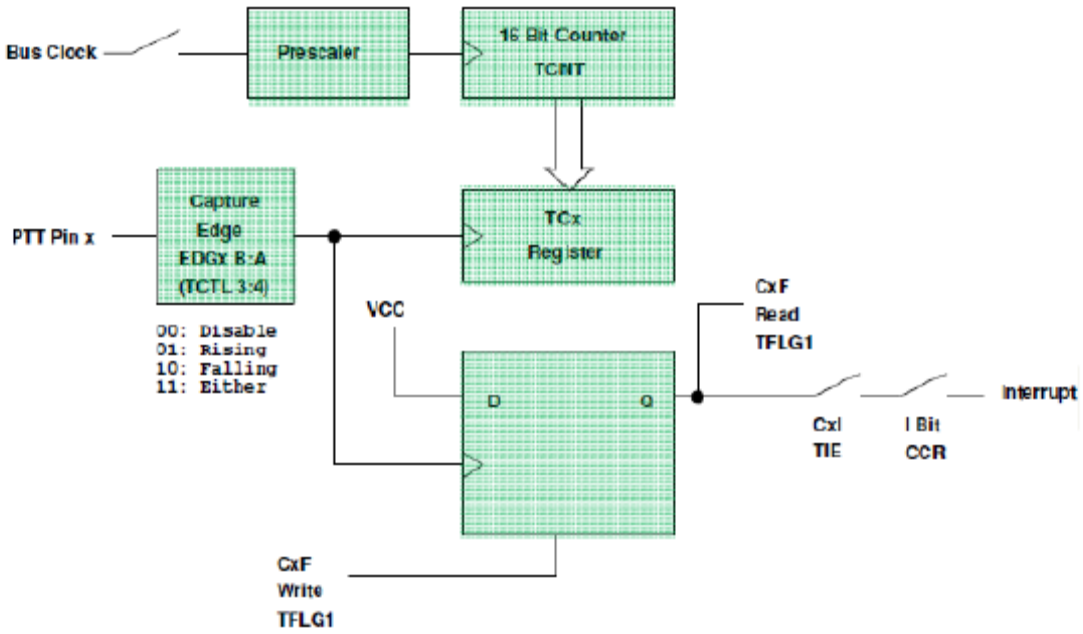
Register offset: $_0D

	BIT7	6	5	4	3	2	1	BIT0
R	TOI	0	0	0	TCRE	PR2	PR1	PR0
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-11 Timer System Control Register 2 (TSCR2)


OMx OLx (TCTL 1:0)
00 => Not Used
01 => Toggle
10 => GND
11 => VCC
Tell HC12 what type of event you want
Time Clock
16 Bit Counter TCNT
Enable with TEN
Set rate with prescaler
D
Q
PTx Pin PTT
16 Bit COMPARATOR
TCx Register
Write time you want event to happen to TCx Register
VCC
CxF Read TFLG1
Cxl TIE
I Bit CCR
Interrupt
CxF Write TFLG1


Bus Clock
Prescaler
16 Bit Counter TCNT
PTT Pin x
Capture Edge EDGx B:A (TCTL 3:4)
00: Disable
01: Rising
10: Falling
11: Either
TCx Register
VCC
D
Q
CxF Read TFLG1
Cxl TIE
I Bit CCR
Interrupt
CxF Write TFLG1

3.3.12 TFLG1 — Main Timer Interrupt Flag 1

Register offset: $_0E

	BIT7	6	5	4	3	2	1	BIT0
R W	C7F	C6F	C5F	C4F	C3F	C2F	C1F	C0F
RESET:	0	0	0	0	0	0	0	0

Figure 3-12 Main Timer Interrupt Flag 1 (TFLG1)

IOS7	IOS6	IOS5	IOS4	IOS3	IOS2	IOS1	IOS0	0x0080	TIOS

OM7	OL7	OM6	OL6	OM5	OL5	OM4	OL4	0x0048	TCTL1
OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0	0x0049	TCTL2

EDG7B	EDG7A	EDG6B	EDG6A	EDG5B	EDG5A	EDG4B	EDG4A	0x004A	TCTL3
EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG0A	0x004B	TCTL4

C7I	C6I	C5I	C4I	C3I	C2I	C1I	C0I	0x004C	TIE