Amitabh **Yadav**

Electronics Engineer | Digital Design, Computer Architecture and Computer Security

D.O.B. March 27, 1995 | Nationality: INDIAN | Current Residence: Geneva, Switzerland

+41 766 241 471 | amitabhydv@gmail.com | amitabhyadav.com | amitabhyadav | amitabhydv

Summary

I'm an Electronics Engineer and a researcher - a cheerful nerd who loves Vim, Linux, Mathematics, Physics and Problem solving. Experienced (2+ years) in designing complex systems for critical applications in Experimental Physics, Space and Safety critical electronics systems. I'm also interested in select topics in Parallel Computing, Quantum Information Theory, and Computer Security.

Education

TU Delft (Delft University of Technology)

Delft, Netherlands

M.Sc. Computer Engineering (spl. Quantum Computing) (Overall GPA: 8.2/10.0) *September 2017 - August 2019*

- Master Thesis: **'Micro-architecture Design for control of Spin Qubit Quantum Processor'**. Thesis Grade: 9/10. (1 year)
- Teaching Assistant: (i) 'The Building Blocks of a Quantum Computer: Part 1 and Part 2' MOOC on edx.org (12+ weeks); (ii) 'EE1D11 Digital Systems A: Programming in C' Undergraduate Course. (8 weeks)
- Stratos-III Sounding Rocket Firmware Engineer at **Delft Aerospace Rocket Engineering (DARE)** (5 months)
- Research Affiliate: Department of Physics, **University of California Berkeley**. (Nov 2019 - present).

UPES (University of Petroleum and Energy Studies)

Dehradun, India

B.Tech. Electronics Engineering (Overall GPA: 3.1/4.0) *August 2013 - June 2017*

- Final Project: "Design & Simulation of 16-bit microcontroller". Thesis Grade: 4/4. (8 months)
- Research Assistant at Embedded Systems Lab, UPES

Research Experience

CERN (Conseil Européen pour la Recherche Nucléaire)

Geneva, Switzerland

Research Fellow (Digital Design and Verification) *November 2020 - present*

- Digital Design, verification and embedded software development for CERN's safety-critical (SIL2) Radiation Monitoring Electronics devices running on **Zynq-7000 SoCs and communication** framework development for the TCP/IP network.

LBNL (Lawrence Berkeley National Laboratory)

Berkeley, California, U.S.A.

Research Associate, Physics Division *November 2019 - November 2020*

- Developed **Quantum Hough Transform** algorithm using HHL, Quantum Phase Estimation and Grovers-Long Algorithm for ATLAS/CERN Track Reconstruction.

QuTech/TU Delft

Delft, Netherlands

Research Assistant, Quantum & Computer Engineering Lab *August 2018 - September 2019*

- Developed the **CC Spin Micro-architecture Design** targeting high qubit count control for Spin Qubit Quantum Processor.
- Implemented the design on a Cyclone-V SoC-FPGA dedicated for translating the Instruction Set (QISA) to sequences of arbitrary I/Q and DC Pulses. The micro-architecture is interfaced with a FPGA controlled Direct Digital Synthesis (DDS) h/w communicating via high-speed LVDS signals for multi-channel synchronous waveform generation. It comprises of a Quantum Pipeline, a Microcode Unit, Timing Control Unit and SPI Master (DDS controller) to perform Qubit operations.

CERN (Conseil Européen pour la Recherche Nucléaire)

Geneva, Switzerland

Summer Student (ATLAS Pixel Group, EP-ADE-ID) *June 2017 - August 2017*

- Developed a **front-end DAQ firmware for ATLAS Inner Detector's FEI-4 Silicon Pixel Chip** on Xilinx Kintex KC705.
- Integrated the IPBus (UDP/IP) protocol (front-end monitoring) and 8b/10b encoded Rx/Tx Core to communicate with back-end Gigabit Transceiver (GBT) protocol. Further, developed a data_routing entity called 'E_Link Bank'.

BARC (Bhabha Atomic Research Center)

Mumbai, India

Project Trainee (Data Acquisition & Processing Systems (DA&PS) Group) *June 2016 - August 2016*

- Developed **Compression and De-Noising library** for A, B and C Scan Ultrasonic Scan Data for application in NDT of Materials.
- Achieved loss-less data compression up to 75.37% in C-Scan data using standard information coding algorithms. (**Report**)
- Analyzed compression ratios & noise in Lossy compression algorithms including 1-D & 2-D DCT, DFT and Wavelet Transform.

Technical Skills

Programming C (Expert), C++, VHDL (Expert), CUDA (Basic), SystemVerilog (Basic), Tcl, Shell, Makefile, Python

Software Tools Matlab, Altium Designer, Xilinx Vivado, Petalinux, Yocto, Altera Quartus, QuestaSim, Cadence Spectre, LaTeX, Anaconda, IBM-QISKIT.

Academic Projects

- Running **Shor's Algorithm on IBM Quantum Experience** using IBM-Q QISKit. (Report)
- **BICMOS5 Fabrication & Measurement** of IC parameters in Else Kooi IC fabrication Cleanroom, TU Delft. (16 hours)
- OpenCL implementation of Smith-Waterman Algorithm for **Protein/DNA Sequencing**. (CUDA provided)
- Performance improvement of **Plasma processor core (opencores.org)** in VHDL. (Processor Design Project)
- **Parallel Poisson Solver** on Distributed Memory HPC cluster using MPI. (High Performance Computing)
- Design and Jitter Analysis of **Quadrature Phase By-6 frequency divider** in Cadence Spectre. (Digital IC Design)
- Development of Classic Snake Game using **Software Design Patterns in Java**. [ATHENS Programme 2017]
- Modelling and Simulation of a **16-bit Microcontroller in Xilinx/VHDL**. [Bachelors Thesis Project]
- Embedded Hardware development of AVR-MCU based **Audio-Signal Morse Code Encoding/Decoding**.
- **Wireless Sensor Network** system for: (i) Landslide Forecasting and, (ii)Patient Monitoring and Tracking System.
  Funded research projects (INR 45,000) [UPES Best Research Award 2017]

National & International Competitions

Lockheed Martin Roll-On/Roll-Off Design Challenge — *New Delhi*

Electronics Engineer (Phase II) — *August 2015 - May 2017*

- Developed the detailed technical design of Aerial Surveillance System, Payload Control and Communication System.
- **Excelled with National Rank 1** in the Critical Design Phase (Phase-II).
- Secured a research grant by the Aerospace and Defense giant, **Lockheed Martin** (USD 25,000 + USD 40,000) to manufacture the prototype payload structure for C-130J Super Hercules Military Aircraft.

Intercollegiate Rocket Engineering Competition (IREC) 2017 — *Spaceport America, U.S.A.*

Avionics and Payload Engineer — *August 2016 - May 2017*

- Developed the avionics and telemetry systems in the Sounding Rocket 'Kalam' for Team Garud (Rocketry Division of UPES).
- Lead the development of a Cansat payload performing stable decent using triple-modular redundancy electronics.

Cansat Competition 2015, '16 & '17 — *Texas, U.S.A.*

Technical Advisor 2017, Team Leader (Electronics) 2016, Team Member 2015 — *August 2015 - June 2017*

- Lead the development & integration of Sensor Subsystem, Telemetry System and real-time decent monitoring system by Ground Station for the rocket payloads weighing under 500g. [News1] [News2]

Certifications & Summer Schools

- 'The Quantum Wave in Computing' (Jan - May, 2020) at **Simons Institute for the Theory of Computing, UC Berkeley**.
- 'Quantum Information for Developers 2018' Summer School at **Institute for Theoretical Physics, ETH Zurich**.
- 'TUD15 Software Design Patterns' 2018 at **ATHENS Programme**

MOOCs: Particle Physics: An Introduction (University of Geneva, Coursera) - 2017; Quantum Cryptography (TU Delft & Caltech, EDX) - 2018; Quantum Machine Learning (University of Toronto, EDX) - 2019

Selected Publications

- ROMULUSLib: An Autonomous, TCP/IP-Based, Multi-Architecture C Networking Library for DAQ & Control (2022)
- Quantum Pattern Recognition for Tracking in High Energy Physics (2021)
- CC-Spin: A Micro-architecture design for scalable control of Spin-Qubit Quantum Processor. (2020)
- Quantum Computer Architecture: Towards Full-Stack Quantum Accelerators, Design, Automation Test in Europe Conference Exhibition (DATE), 2020. (2019)

All hyperlinks to talks, publications, presentations etc. are available at amitabhyadav.com/links