

ET4icp IC-Technology Lab

REPORT

Simulation, Processing and Measurements

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Submitted By:

GROUP - 9

Amitabh Yadav, Student No. 4715020
Pinakin Padalia, Student No. 4743644

DELFT UNIVERSITY OF TECHNOLOGY
Delft, Netherlands

1 Introduction

As a part of requirements for ‘ET4icp IC-Technology Lab’ course, this report summarizes our (Group 9’s) findings during different stages, as we proceed through simulating, processing and performing measurements on the MOS transistors according to the BICMOS5 process.

1.1 Fabrication Process

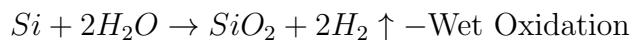
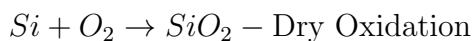
The fabrication process involves series of steps to print a given circuit on silicon substrate. A lot of the major steps are common in the process. It starts with doping the substrate and ends with a full circuit laid out on the chip with bonding pads to the outside world. Later on, it can be packaged to individual ICs. The key steps involved in the process are as under -

- Oxidation - wet and dry
- Doping - diffusion and ion implantation
- Lithography
- Deposition - PVD, CVD, ALD
- Etching - chemical, plasma

The actual fabrication process may involve using these steps multiple times.

1.1.1 Oxidation

Oxidation involves growing silicon dioxide on the wafer. It consumes the silicon in the process. But, it will have excellent adhering capability as compared to deposited oxide. The oxidation can be dry - where oxygen is used as an ambient under high temperatures ($900^{\circ}C$ to $1000^{\circ}C$) or it can wet, where water is used under relatively low temperatures. The oxide grown at high temperatures is generally more pure and takes more time growing the same thickness of oxide as compared to wet oxidation. The equations involved are as under -



Roughly 45% of silicon is consumed for a given amount of oxide growth.

1.1.2 Doping

Doping means to add desired substances (p/n type dopants) to silicon to change its properties locally. By adding p-type dopants such as Boron, one increases the number of holes in the silicon substrate. Similarly, by adding n-type dopants such as Arsenic, Phosphorous and Antimony,

the concentration of electrons is increased. However, the law of mass action is followed for the equilibrium case -

$$(n_i)^2 = n.p$$

Where n is the concentration of electrons and p is concentration of holes. While n_i represents the intrinsic concentration of charge carriers. Doping can be done in two major ways - ion implantation and diffusion. However, a lot of times diffusion can also be a second step in doping after ion implantation.

- Ion implantation - The dopant atoms are ionized and accelerated in an electric field. Mass spectrometry is performed on these accelerated ions to separate the pure dopant atoms from their isotopes. The resulting high energy ions are then bombarded on the silicon substrate where they penetrate it depending on their ionization energy and the crystal orientation. The doping profile can be approximated to first order as Gaussian -

$$N(x) = N_p \cdot e^{-\frac{(x-R_p)^2}{2\Delta R_p^2}}$$

Where R_p is the projected depth of the ions and ΔR_p is the standard deviation or the straggle. N is the doping concentration.

However, one should also take into account the effect of channeling. Depending on the crystal orientation, dopant size and the angle of tilt, the bombarded atoms can channel into the substrate further than expected causing a tail. Which would mean that the junctions are less abrupt. Hence, one has to prevent such channeling effect. There are at least 3 ways in which one can reduce the tailing effect. More of it would be described in the simulation section, where one can see the tail effect and the ways adopted to reduce it.

- Diffusion - Diffusion is straight forward in terms of implementation. One has to have a source of dopant atoms near/on the silicon substrate and the atoms will diffuse inside the substrate based on the Fick's laws -

$$J = -D \frac{\partial C}{\partial x}$$

$$\frac{\partial C}{\partial t} = D \frac{\partial^2 C}{\partial x^2}$$

Here, J is the flux, C is the concentration of the dopant, D is the diffusion coefficient, x is the position and t is time.

Further, the kind of source for diffusion can be limited or constant. Both cases will result into different doping profiles. Under limited source diffusion, the amount of dopant atoms remain the same and the profile is gaussian. However, if left long enough, the dopant would diffuse completely inside the substrate and the concentration would go to minimum 0. The doping profile would follow the following equation -

$$C(x, t) = \frac{Q_o}{\sqrt{\pi D t}} \cdot e^{-\frac{x^2}{4Dt}}$$

The symbols carry the same meaning and Q_o represents the initial concentration per unit area.

Under constant source diffusion the concentration of the dopant on the surface remains constant. This can be achieved by depositing a layer of doped oxide on the substrate. The profile can be approximated using an error function. If left long enough, the substrate would contain the same doping concentration as at the surface. The error function of the profile can be given as under -

$$C(x, t) = C_s \cdot \text{erfc} \left(\frac{x}{2\sqrt{Dt}} \right)$$

Here, erfc is the complimentary error function and C_s is the surface concentration of the dopant atoms. The simulations will talk more about the diffusion process.

1.1.3 Lithography

“Lithography” is a Greek word, which literally means - “to write on stone”. To make devices on substrate, one requires a certain mask, which has the required pattern and a process to transfer that pattern on silicon for realization of the device. Lithography is the process of transferring these patterns onto the silicon.

During the process, the wafer is coated with a photoresist. This is a light sensitive layer whose chemical reactivity is altered by the presence or absence of light of a certain wavelength. The photoresist is generally a liquid which is coated over the wafer and spun at high speed for uniform layer formation. The wafer is then exposed to UV light via mask, to selectively change the reactivity of the exposed photoresist. Upon chemical treatment, the exposed photoresist (If positive photoresist is used) dissolves. The remaining resist acts as protection layer for further processing steps, such as - ion implantation, diffusion, etching, etc.

1.1.4 Deposition

Deposition allows for the formation of a thin layer of required material onto the silicon. This can be polysilicon on dielectric, metals such as aluminum, etc. Depending on the type of substance and environment, various methods are adopted which include - Chemical Vapour Deposition (CVD), Physical Vapour Deposition (PVD), Plasma Enhanced Chemical Vapour Deposition (PECVD), Low Pressure Chemical Vapour Deposition (LPCVD), Atomic Layer Deposition (ALD), etc.

CVD uses chemical compositions of substances to be deposited on substrate. Normally the residues that are formed should be easily removable. PECVD, uses plasma to generate the required radicals, whereas LPCVD uses low pressure to increase the deposition rates. ALD deposits layers which can be single atom thick.

1.1.5 Etching

Etching is selective to the type of material to be etched away. Different chemicals such as KOH and others can be used to selectively etch away the photoresist, oxides or metal, depending on

the application. This kind of etching with chemicals is highly selective but has an isotropic profile. This can be a problem if the etching is done for a long time as it may undercut the structures. This may lead to no structures at all or short circuits in some cases.

On the other end, plasma can be used for directive etching. It allows for anisotropic etching but can be less selective as compared to chemical etching.

1.2 BICMOS5 - processing steps

The technology allows for the fabrication of 3 main devices - NPN bipolartransistors, NMOS and PMOS FETs. The process takes in 5 mask steps -

- N-Well (NW) - Allows formation of n-well in PMOS devices and collector well for BJTs
- Shallow-N (SN) - Allows the formation of source and drain junction in NMOS, emitter area for BJTs,Collector contact for BJTs and guard ring formation
- Shallow-P (SP) - Allows the formation of source and drain junctions for PMOS, base area for BJTs, and p-type guard rings.
- Contact Openings (CO) - Allows the formation of contact openings for interconnecting devices.
- Interconnect (IC) - Allows for the formation of interconnections

Apart from the standard steps listed above, there is an additional mask step for adjusting the threshold of the devices - V_T adjust implantation. Moreover, additional processing steps could also be added to improve the devices with desirable characteristics.

The whole process begins with monocrystalline silicon wafer. The wafer is p-type with doping in the range of $7 - 3 * 10^{15} cm^{-3}$ for the wafers that are with EKL. Next, the alignment markers are first placed at the corners of the wafer to allow for good alignment of different masks used in the process. After placing the alignment markers, one can start with the first step towards fabrication - mainly doping for well formation (NW). However, to prevent the channeling effect, amorphous SiO_2 of roughly 20nm thickness is grown over the Silicon wafer. The oxide also helps in preventing contamination as it will act as a barrier.

Doping in specific regions is done with the use of different masks. First the N-Well doping is done using an n-type dopant such as phosphorous. The ion implantation of phosphorous will be followed by diffusion (1150°C) with nitrogen as ambient. This will allow for the formation of correct junction depth, depending on the time of diffusion. The protective and overgrown oxide layer is later removed via etching in HF solution. Similar steps are followed for SN and SP implantation. First, a protective layer is formed (20nm) of oxide, followed by masking and application of photoresist. The dopants are implanted via ion implantation (n-type Arsenic and p-type Boron) followed by diffusion. Later on the photoresist and the protective layer is removed via etching. Both, the SN and SP processes are done one at a time.

At this time one can do additional implantation step for threshold adjustment with Boron. After the implant stage, the wafer is oxidized and annealed at $1000^{\circ}C$ to repair the crystal for any damage done during ion implantation. Moreover, a layer of SiO_2 is formed during oxidation which acts as isolation for the metalization steps to follow after this. It also defines the gate oxide thickness in this case.

The next mask layer is for creating contact openings (CO). Again the photoresist is applied and subsequently etched after masking to make the contact openings. A layer of Aluminum (0.2um) is coated with 1% of silicon to prevent spiking. Now the IC mask is applied with a coating of photoresist to define the interconnections and also the connections to outside with bonding pads. Etching step in phosphoric acid solution at $35^{\circ}C$ or plasma etching removes the unwanted metal. Now the processing steps are completed and one can check the various properties of the devices to monitor the processing steps. In general, further processing steps can be done for depositing additional metal layers. Eventually the different chips are diced and packaged individually.

2 Technology Assignment

The section compiles the calculations done before the simulation and actual processing in BICMOS5 process.

2.1 Assignment 1 - Marker oxidation

The assignment calculates the step height during the formation of markers. It involves double oxidation and relies on the fact that rate of oxidation depends on the layer of oxide already present at the interface. The Deal-Grove model gives the oxidation rate and its relation with time and previous oxide layer. The equations involved are as under -

$$\frac{dx}{dt} = \frac{B}{2x + A}$$

$$t = \frac{(x^2 - x_o^2) + A(x - x_o)}{B}$$

Where t is time and x is the oxide thickness.

1. The equation above is a second order equation in x. The solution is given as -

$$x = \frac{\sqrt{\left(\frac{A}{B}\right)^2 + \frac{4}{B}(t + \frac{x_o^2}{B} + \frac{Ax_o}{B})} - \frac{A}{B}}{\frac{2}{B}}$$

For t=0, the feasible solution is $x = x_o$. This can be easily seen by substituting t=0 in the above equation and solving.

2. Now, t=38.5 minutes = 38.5/60 hours. Substituting t and having $B = 0.553 \text{ um}^2/\text{hr}$ and $A/B = 3.1695 \text{ um}/\text{hr}$, the thickness of the oxide layer comes out to be -

$$x = 0.513326 \text{ um}$$

3. Now a window is etched on the oxide, such that the height some of silicon is exposed. With the next oxidation step, the one which already has the oxide layer will grow slowly as compared to the one without the oxide layer. Hence, one can see the difference in the silicon consumption as well. This creates the required notch for alignment. Now, the etched area will grow the oxide same as the previous calculation. Hence -

$$d_1 = 0.513326 \text{ um} - \text{Etched area}$$

For the non-etched side, the same equation can be used but with $x_o = 0.513326 \text{ um}$ - as obtained in previous calculation. Substituting in the equation, the total height of the oxide is obtained as under -

$$d_2 = 0.754135 \text{ um} - \text{Non-etched area}$$

4. The amount of silicon consumed for is $0.455d_{ox}$. Where d_{ox} is the thickness of the oxide formed. To calculate the height of the step, one has to find the amount of silicon consumed in the etched area and the amount of silicon consumed in the non etched area in the second processing step. The amount of silicon consumed in etched area is = $0.455d_1$ and the amount of silicon consumed in non etched area is = $0.455(d_2 - d_1)$. Hence the height of the step formed is given as under -

$$h = 0.455d_1 - 0.455(d_2 - d_1)$$

$$h = 123.99 \text{ nm}$$

2.2 Assignment 2 - Gate Oxidation

Dry oxidation - The oxide layer produced via dry oxidation is of higher quality and has been normally used for making gate oxides. Whereas the oxides formed with wet oxidation are generally thick oxides used for insulation and passivation. They also exhibit lower dielectric strength as compared to dry oxides and have more porosity to impurities penetrating inside the wafer. Hence, dry oxidation is preferred in this case. Wet oxides should be preferred where the electrical and chemical properties of the oxide are not critical.

2.3 Assignment 3 - Implantation and diffusion

1. N-Well implantation - Upon ignoring the implantation depth, the subsequent diffusion step can be approximated as limited source diffusion. This is because, after the implantation step, the amount of dopant atoms remains the same. Gradually they start diffusing inside and create a exponential like profile. Here, the diffusion constant of phosphorous is given as - $D = 8.86 * 10^{-13} \text{ cm}^2/\text{s}$. Total time for diffusion, $t = 4 \text{ hours} = 14400 \text{ s}$. Upon ignoring the implantation depth, the peak concentration appears at the surface, hence setting $x = 0$, in the below equation -

$$C(x = 0, t = 4 \text{ hours}) = \frac{Q_o}{\sqrt{\pi D t}} e^{-\frac{x^2}{4Dt}}$$

One can get the peak concentration, C_p as -

$$C_p = \frac{Q_o}{\sqrt{\pi D t}}$$

With $Q_o = 6 * 10^{12} \text{ cm}^{-2}$ as the initial dosage, the peak concentration at the end of 4 hours is -

$$C_p = 2.9969 * 10^{16} \text{ cm}^{-3}$$

The junction depth is the distance x where the concentration of the phosphorous dopant and the background doping of Boron becomes equal. The boron doping is 10^{16} cm^{-3} . Substituting $C(x,t)$ as this concentration and evaluating for x gives -

$$x = \sqrt{4Dt * \ln\left(\frac{C_p}{C(x,t)}\right)} = 2.367 \mu\text{m}$$

2. SN implantation - Here, the background doping of boron is 10^{16} cm^{-3} . Moreover, the implantation profile is gaussian with the projected range, $R_p = 0.0314 \text{ um}$ and the straggle $\Delta R_p = 0.0114 \text{ um}$. Again, the junction depth is given when the dopant concentration becomes equal to the background doping concentration. Hence, substituting $N(x) = 10^{16} \text{ cm}^{-3}$ in the below equation, and all other parameters given, one can calculate the junction depth as below -

$$x = \sqrt{2\Delta R_p * \ln\left(\frac{N_p}{N(x)}\right)} + R_p \text{ um}$$

and with -

$$N_p = \frac{Q}{\sqrt{2\pi}\Delta R_p} \text{ cm}^{-3}$$

Where, Q is the initial dosage = $5 * 10^{15} \text{ cm}^{-2}$. The junction depth obtained in calculation is -

$$x_j = 0.0874 \text{ um}$$

3. SP implantation - Here, the background doping of phosphorous (from N-Well) is $2 * 10^{16} \text{ cm}^{-3}$. Moreover, the implantation profile is gaussian with the projected range, $R_p = 0.0685 \text{ um}$ and the straggle $\Delta R_p = 0.0296 \text{ um}$. Again, the junction depth is given when the dopant concentration becomes equal to the background doping concentration. Hence, substituting $N(x) = 2 * 10^{16} \text{ cm}^{-3}$ in the below equation, and all other parameters given, one can calculate the junction depth as below -

$$x = \sqrt{2\Delta R_p * \ln\left(\frac{N_p}{N(x)}\right)} + R_p \text{ um}$$

and with -

$$N_p = \frac{Q}{\sqrt{2\pi}\Delta R_p} \text{ cm}^{-3}$$

Where, Q is the initial dosage = $4 * 10^{14} \text{ cm}^{-2}$. The junction depth obtained in calculation is -

$$x_j = 0.1865 \text{ um}$$

2.4 Assignment 4 - BICMOS process flow

The correct order for the masks is as follows -

1. Mask 3 - N-Well (NW)
2. Mask 5 - Shallow N (SN)
3. Mask 4 - Shallow P (SP)
4. Mask 2 - Contact opening (CO)
5. Mask 1 - Interconnect (IC)

2.5 V_T - Adjust

The expression for threshold voltage can be given as under -

$$V_T = V_{fb} + \frac{|Q|}{C_{ox}} + \frac{2kT}{q} \ln\left(\frac{N_d}{n_i}\right)$$

Here, V_{fb} represents the flat band voltage which takes into account the fixed charges in the oxide and also the work function difference between the gate and silicon. $|Q|$ represents the total depletion charge under the gate including the charge added during the threshold adjustment. k represents the Boltzmann's constant, T as temperature and q as electric charge. N_d represents the doping concentration and n_i as the intrinsic concentration.

Threshold voltage indicates the amount of gate voltage required to form a channel in either NMOS or PMOS. The threshold voltage magnitude depends on the doping concentration. Now, the PMOS already has a higher background doping than NMOS as it is fabricated in N-Well. Hence, the threshold voltage will be always higher(in magnitude) than that of NMOS. The additional doping of boron is done so that one can keep the threshold voltages same for both NMOS and PMOS devices. By adding boron dopants at the gate, the thershold voltage for NMOS increases and that of PMOS reduces. Hence, ultimately equating the threshold voltages for both.

3 Process Simulation

The process simulations are done to estimate the doping profiles of various dopants used in the fabrication process. This determines the device performance and hence it is crucial to estimate these process parameters before jumping to fabrication. Only when the desired performance is met, one can start with the actual fabrication process.

Ques. 3 Implantation profiles

The doping profiles obtained for Arsenic, Boron and Antimony can be seen below -

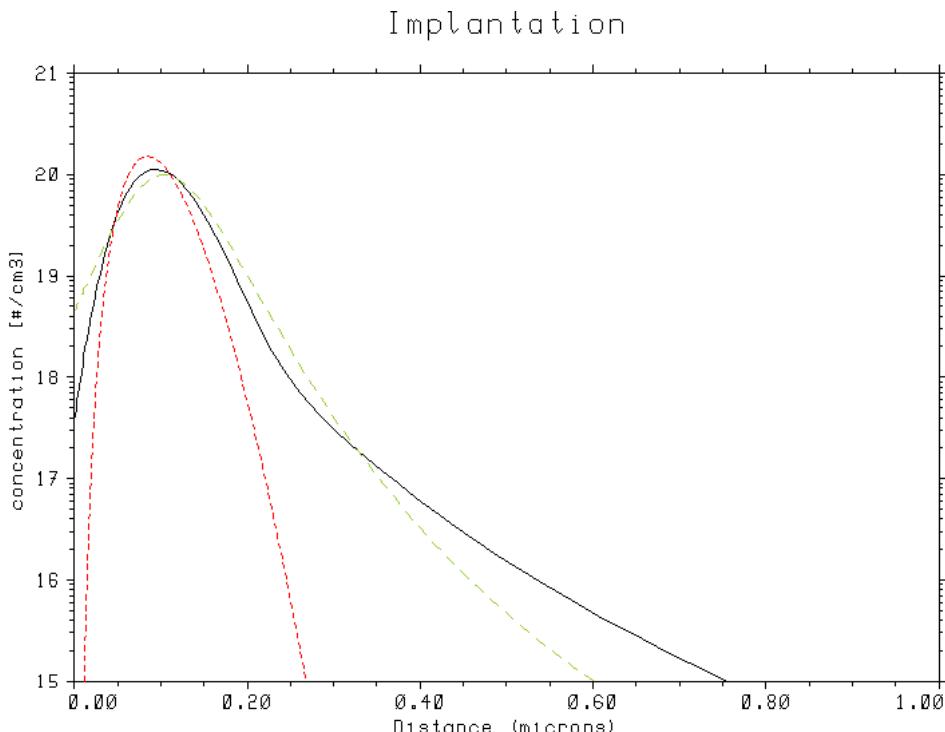


Figure 1: Implantation of Arsenic (black), Antimony (red) and Boron (green)

As one can see, the dopants have lengths of the tails. They do not exhibit an ideal gaussian behavior. The gaussian behavior should look like a parabola in the log scale. The tail indicates that the dopants have diffused even further than their estimated depth using the gaussian approximation. Generally more channeling is observed with lighter dopants such as Boron (-ve misfit factors). However, in case of Arsenic the ion steering effect dominates and one can see that it forms the longest tail. The next longest is Boron, being a lighter element. The shortest tail is of arsenic, being bigger than silicon atoms. The order of the dopants from shortest to longest tail is given below -

$$\text{Antimony (Sb)} < \text{Boron (B)} < \text{Arsenic (As)}$$

Ques. 4 Now, phosphorous is to be implanted to the same depth as other dopants. One can see that the energy required for a dopant is directly proportional to its atomic mass. Hence, one can estimate the required amount of energy by looking at the relation between mass and energy for other dopant atoms. It follows approximately $y = mx + c$ relation. From equating the slopes, the required energy comes out to be $\sim 50.12\text{keV}$. However, the

approximation is not totally valid as there is some sort of curvature involved. On doing 3rd order fit with the 3 points, one could estimate the required energy to be $\sim 71.78\text{keV}$. The table below shows the atomic masses and the respective energy used for a specific depth. The energy for phosphorous is averaged from linear and polynomial approximation $\sim 61\text{keV}$.

Dopant atom	Atomic mass (gm/mol)	Energy required (keV)
Boron (B)	11	28
Phosphorous (P)	31	61
Arsenic (As)	75	148
Antimony (Sb)	122	200

The image shown below shows the polynomial approximation of the same.

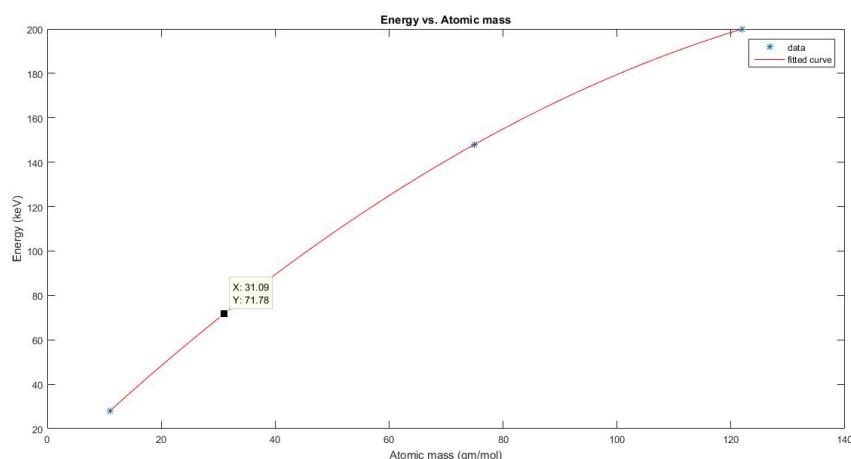


Figure 2: Energy vs. Atomic masses

The figure now shows all the dopant atoms with their respective color coding.

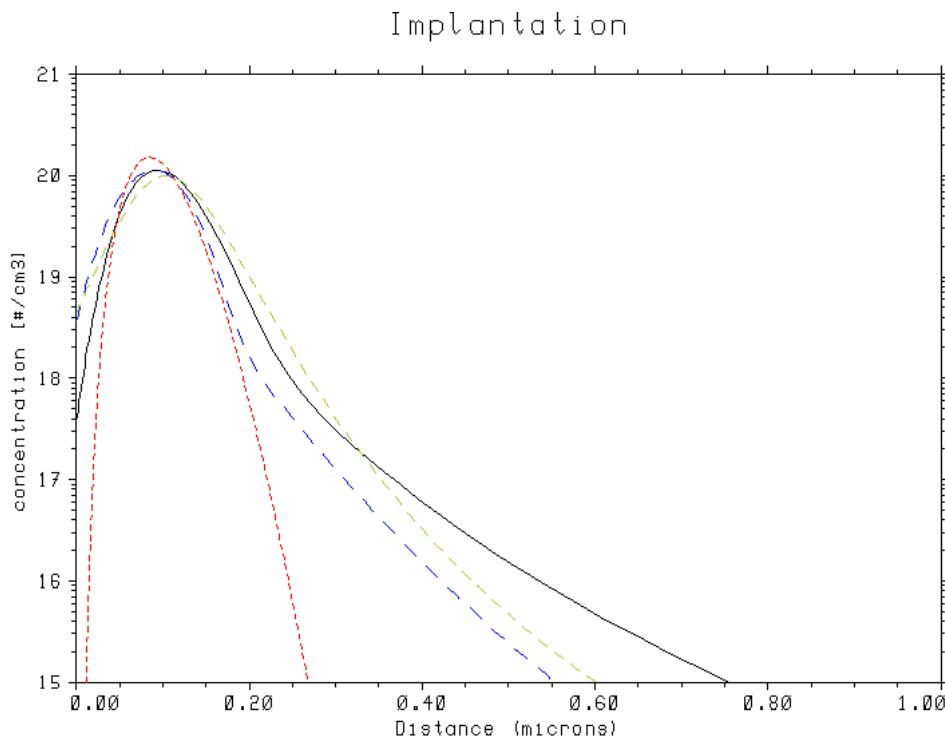


Figure 3: Implantation of Arsenic (black), Antimony (red), Boron (green) and Phosphorus (blue)

Ques. 5 One of the ways to decrease the effect of channeling is to place a layer of amorphous silicon over crystalline silicon. This increases the scattering of the incoming dopant ions and reduces channeling. When amorphous silicon is used instead of crystalline silicon, the dopant ions are greatly scattered and there is virtually no net channeling effect. To simulate that, one has to run several Monte Carlo runs. The figure below shows the obtained profile of the dopants in an amorphous silicon. One can clearly see that the channeling is significantly reduced (almost no channeling) as compared to crystalline silicon shown earlier.

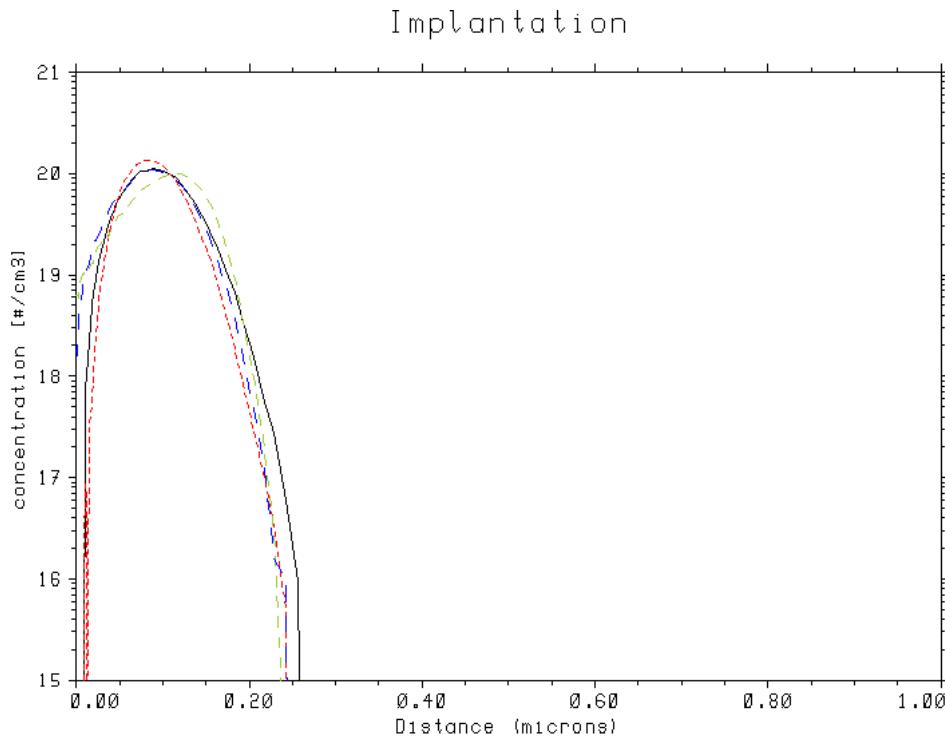
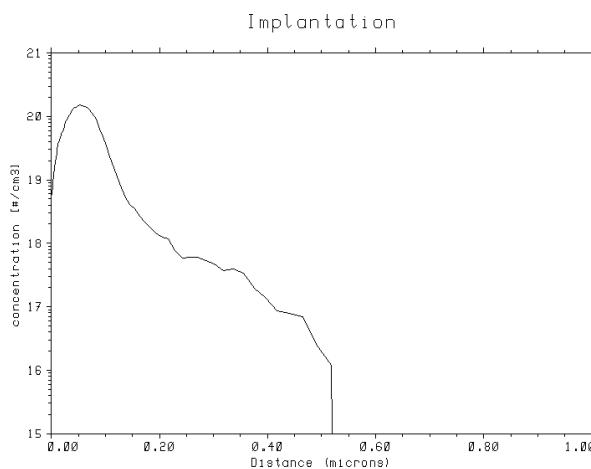


Figure 4: Implantation of Arsenic (black), Antimony (red), Boron (green) and Phosphorus (blue) on Amorphous Silicon

Ques. 6 Second way to reduce the channeling is to change the tilt angle of the silicon substrate. Upon causing a tilt, the incoming dopant atoms see a different density of silicon atoms. Hence, with a different tilt angle, the amount of channeling will differ. Generally, the channeling is minimum when the dopant atoms see the structure as close as possible to an amorphous silicon. Due to the crystal struc of the silicon, it is possible to see such a profile depending on the tilt and rotation of the wafer. The figures below show the different doping profiles for a tilt angle of 0° , 3° and 8° . For all the tilts, the rotation is kept as 0° . The dopant used is Phosphorous with an energy of 40keV.



Ques. 7 It is clearly seen from the plots that as one increases the tilt angle, the tail length reduces. However, one does not see a significant different in the tail going from 0° to 3° . But, one can still see more narrowing of the channel for tilt angle of 3° . For 8° of tilt angle, the

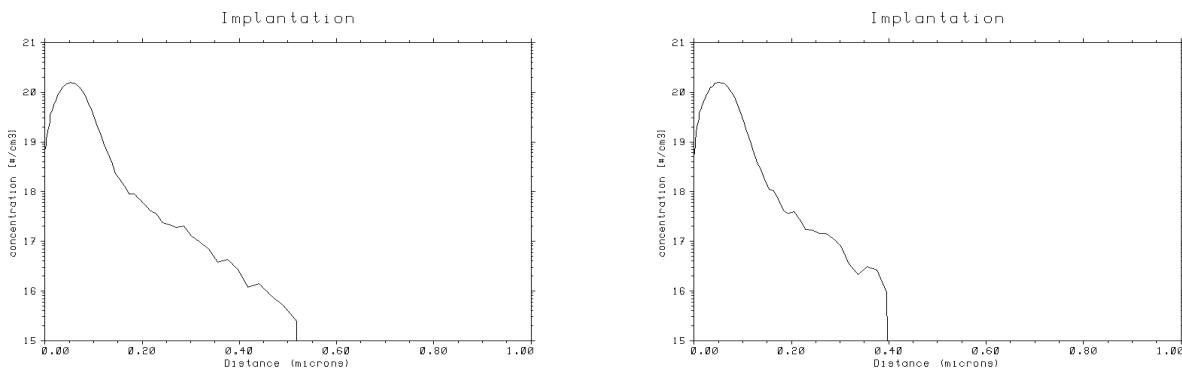


Figure 5: Implantation when $\text{Tilt} = 0^\circ$ (top), $\text{Tilt} = 3^\circ$ (bottom-left), $\text{Tilt} = 8^\circ$ (bottom-right)

channel length is reduced to 0.4 microns.

Ques. 8 For simulating diffusion, ion implantation on amorphous silicon is allowed to diffuse for 5 hours at 1000°C . The figure below shows the diffusion profiles of different dopants. One can see that phosphorous has diffused the most followed by Boron. The next is Antimony and the last is Arsenic, with the solid black curve as reference. Generally, the smaller the misfit factor, the higher the diffusion. In case of Phosphorous and Boron, the misfit factor are negative (-0.068 and -0.254 respectively). This factor estimates the size of dopant as compared to that of silicon, normalized to the size of silicon. Hence, a negative factor means that the dopant ion is smaller as compared to silicon and faces the least resistance while diffusing. In case of Arsenic, the misfit factor is 0 and in case of Anitmony it is 0.153. Hence, both of them will face resistance while diffusing. Of course, other factors like the energy required for diffusing will also affect the depth of diffusion. Hence, we do see that even with smaller misfit factor for Boron, Phosphorous has the maximum diffusion.

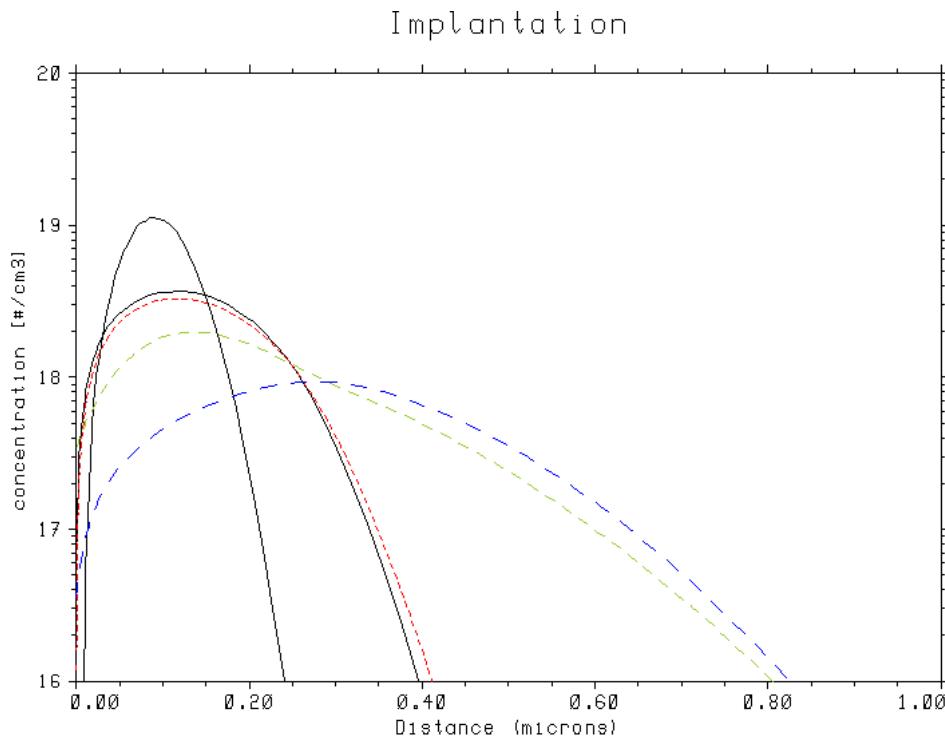


Figure 6: Diffusion in Amorphous Silicon are diffused at 1000°C for 5 hours

Ques. 9 This simulation was done to see the effect of solubility limit. The table below shows the solubility limits for different dopants. Here, the diffusion is run for 60 minutes and at

Dopant atom	Solubility Limit
Boron (B)	$4 * 10^{20}$
Phosphorous (P)	$1.5 * 10^{21}$
Arsenic (As)	$2 * 10^{21}$
Antimony (Sb)	$1 * 10^{20}$

$1000^{\circ}C$ for antimony. In the first case, the doping concentration is $10^{20} \text{ atoms/cm}^2$. While in the second case, the doping is $10^{19} \text{ atoms/cm}^2$. One can see a kink in the first case as the solubility of Arsenic is reached and it can no longer become fully electrically active. The atoms remain interstitial positions and cluster at the surface.

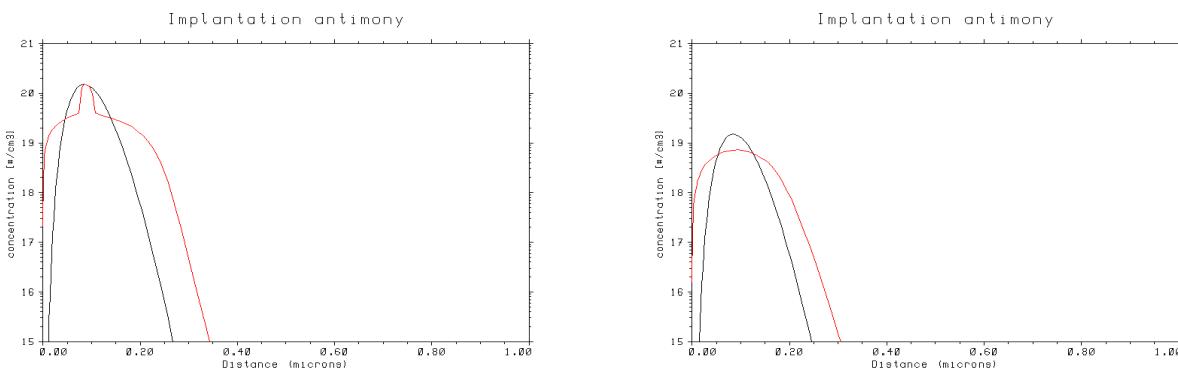


Figure 7: Diffusion of Antimony (Sb) at solubility limit (left) and under solubility limit - by lowering the dose factor of 10 (right)

Ques. 10 The various dopants are ranked below based on the different criteria.

Dopant	Doping Type	Short Channel Tail	Narrow Diffusion	Solid Solubility
Sb	N	1 (Shortest)	2	1 (Least)
As	N	4	1 (Narrowest)	4
P	N	2	4	3
B	P	3	3	2

Table 1: Dopant ranking based on criteria of Doping Type, Short Channel Tail, Narrow Diffusion, Solid Solubility - 1st being ‘best’ up to 4th as the ‘worst’

Ques. 11 For a drain of NMOS one needs high concentration (Which means highest solid solubility) and a sharp profile (Which means narrow diffusion and lowest straggle) which is given by Arsenic. On the other hand, for N Well, one requires a long tail (Which translates to highest diffusion) and high concentration (Which translates to higher solid solubility) which is given by Phosphorous.

Ques. 12 Different masks are used while doing implantation at specific cites. A good mask should block the implantation where it is not required. It should also be easy to remove without affecting the substrate. Generally, one can make a thicker mask and prevent the ion from being implanted in the unwanted regions. But, this would be a waste of resource. Hence, one can evaluate the quality of a mask by looking at the blocking capacity of the substance

for a given ion implantation and a given thickness of the mask. The plots below compare 3 different masks with a thickness of 0.4 micrometers. These are the photoresist, oxide and nitride masks. One can see that the nitride mask allows for maximum blocking of the ions (in this case, phosphorous).

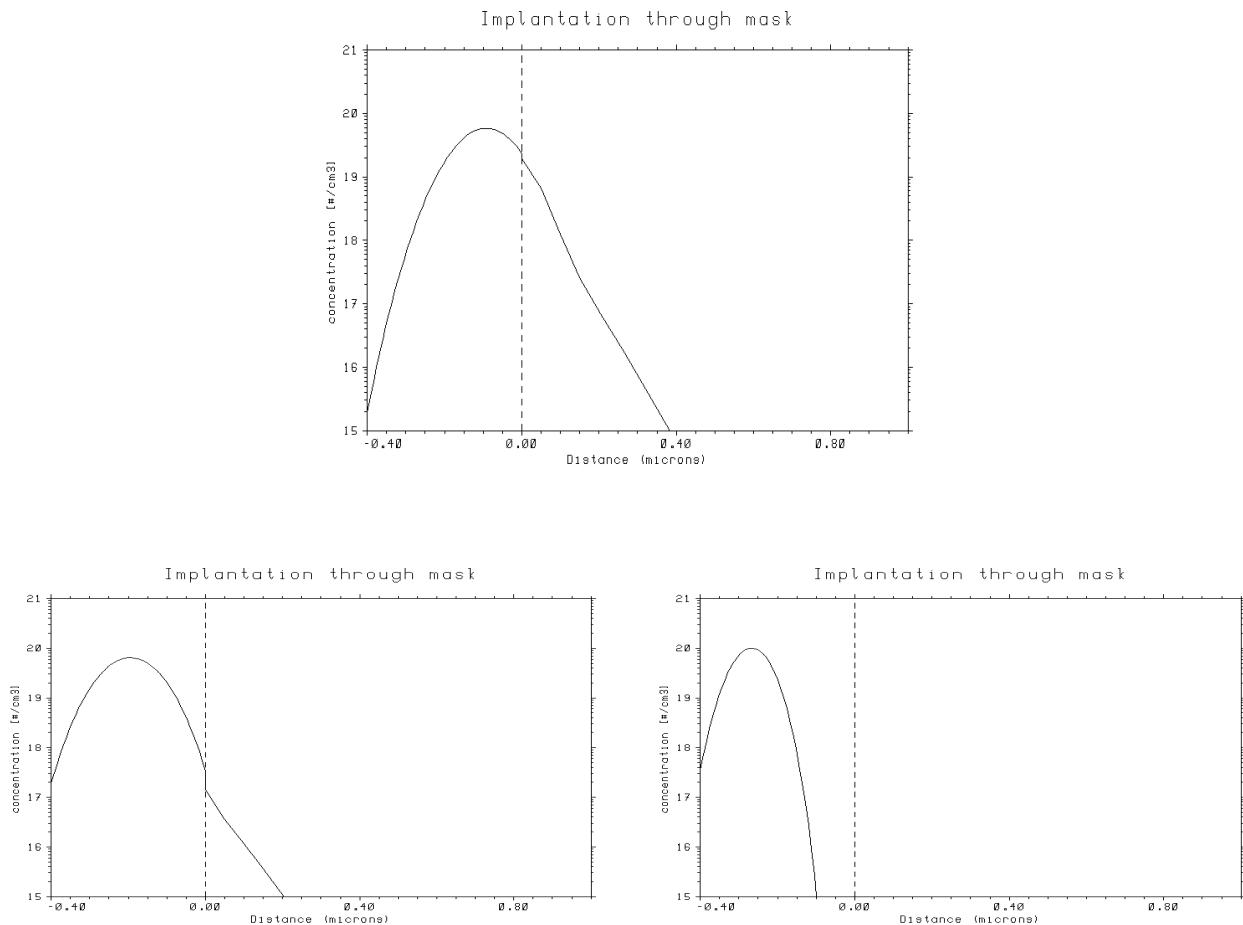


Figure 8: Resist (top), Oxide(bottom-left) and Nitride(bottom-right) masking (at 0.4 micron) with phosphorus implant

Ques. 13 Now, one can see the effect of increasing the thickness of the mask layer. With the thickness of 1 micrometer, all the masks can block the ions completely. The figure 8 shows the effect.

Ques. 14 One can clearly see that Silicon nitride can serve as the best mask as it can stop the ion implantation with minimum possible thickness as compared to the oxide and the photoresist. However, generally the nitride mask is least used as it is difficult to process as compared to the other two. Moreover, it also introduces high thermal stress on the silicon substrate. Normally, for lower steps in fabrication process, the oxide mask can be easily grown and has least stress on the silicon, but it consumes silicon in the process. On the other hand, resist mask can be easily used has similar results without consuming the silicon in the process.

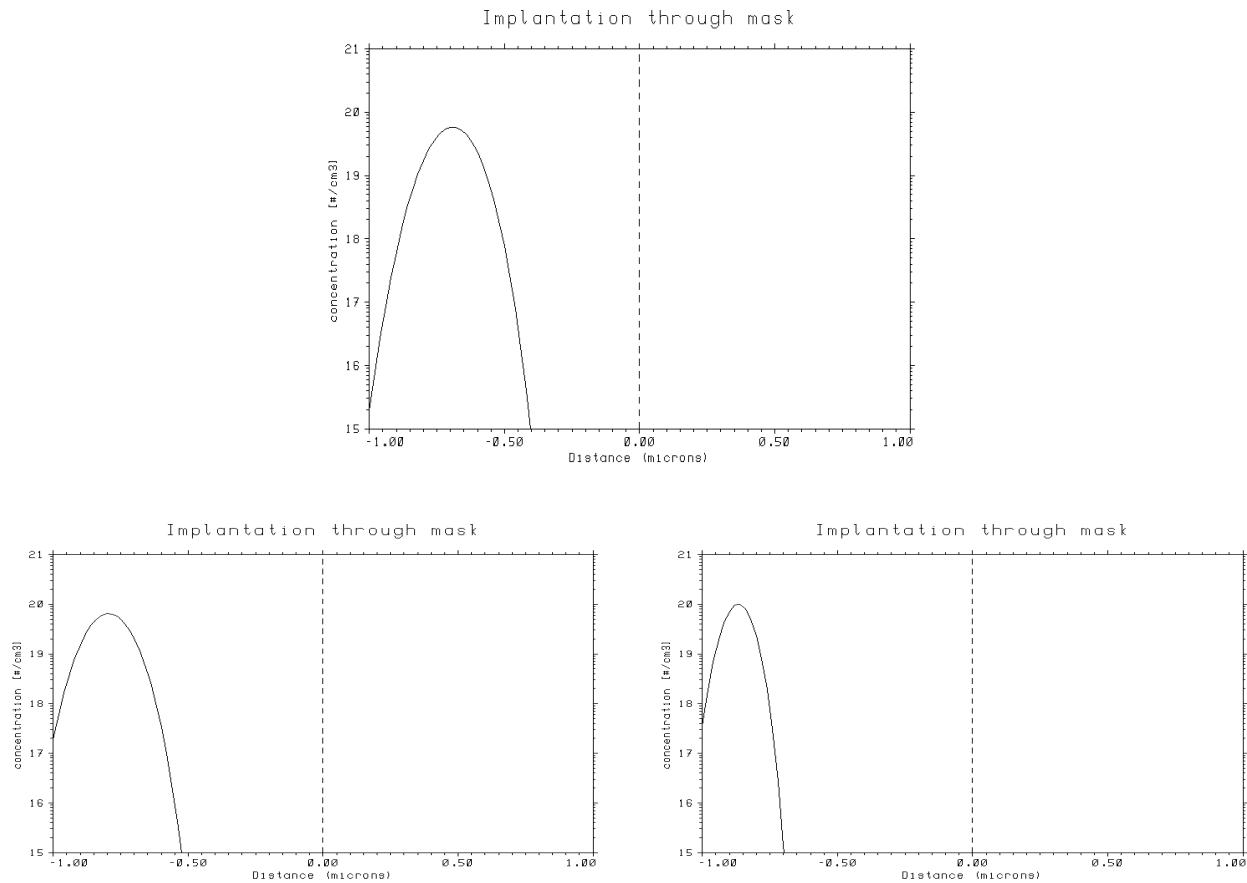


Figure 9: After making Resist (top), Oxide(bottom-left) and Nitride(bottom-right) masking thicker (at 1 micron) with phosphorus implant

4 Device Simulation

The device simulations estimate the device performance based on the doping concentration and the profiles obtained from the process simulations. MEDICI software is used to calculate the electrical characteristic of the device. It uses the doping concentration and the device dimensions to generate a proper mesh for calculating the electron and hole concentration for estimating the electrical potential. From electrical potential, one can easily calculate the electron and hole current density.

We would first look at the NMOS and the PMOS devices individually and then compile the results for the junction depths and the threshold voltages obtained for different threshold adjustment implants at the end.

NMOS Device

Ques. 1 Here the NMOS device structure is shown along with the depletion region and the equipotential lines.

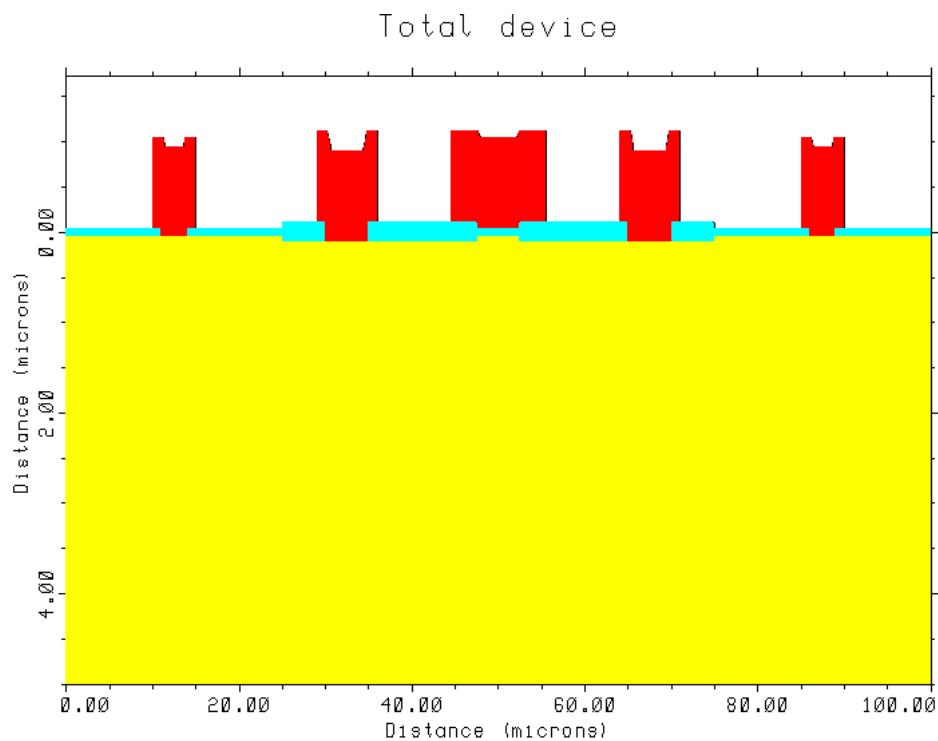


Figure 10: NMOS device structure

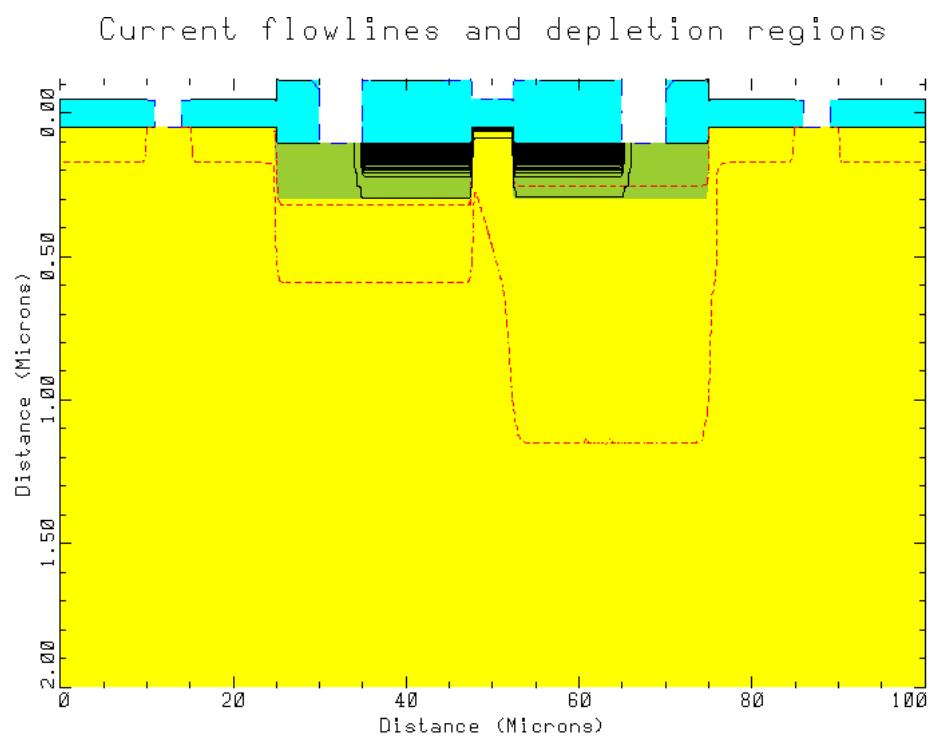


Figure 11: NMOS device current flowlines and depletion regions

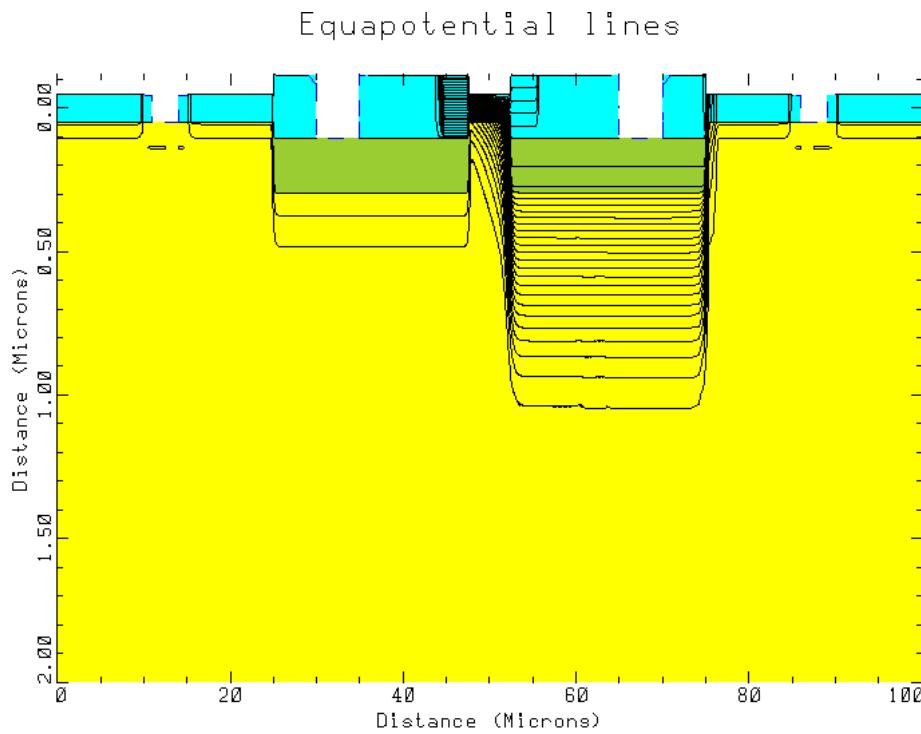


Figure 12: NMOS device equipotential lines

Ques. 2 The substrate of the NMOS can act as the fourth terminal for controlling the device behavior apart from the gate. The drain and source terminals allow for the current flow. Figure 13 shows the I_d vs. V_{gs} plots for different substrate bias voltages in NMOS with a doping of $9 * 10^{11}$ for V_T adjust implant. One can see that the threshold voltage increases with decrease in substrate bias voltage. This is because the width of the depletion region under the gate changes with the substrate voltage and hence affects amount of voltage needed on the gate for forming the inversion layer.

Id vs Vg Characteristics --Substrate bias = -2V

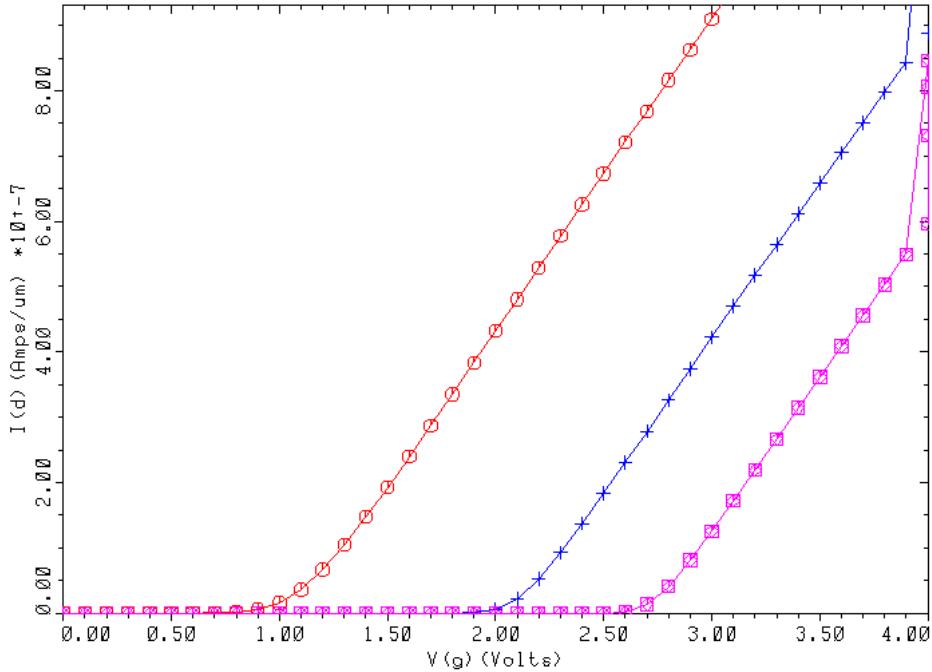


Figure 13: I_D vs V_G plot for NMOS. The substrate bias voltage (V_{sub}) are 0V (red), -1V(blue) and -2V(pink), respectively.

Ques. 3 Now, the drain to source voltage is swept for the same device for different gate voltages. This kind of plot is called the output characteristics of the device. One can see that for small drain voltages the I_D is linearly proportional to V_{ds} . Hence, it forms the linear region of operation. For higher values of V_{ds} , the current is saturated as indicated by the horizontal lines. This indicates the saturation behavior of the device. The boundary condition can be given as under -

$$V_{ds} > V_{gs} - V_{th} \text{ - Saturation region}$$

$$V_{ds} < V_{gs} - V_{th} \text{ - Linear region}$$

$$V_{gs} < V_{th} \text{ - Cut-off region}$$

The gate voltage changes from 0 to 7V going from bottom to top.

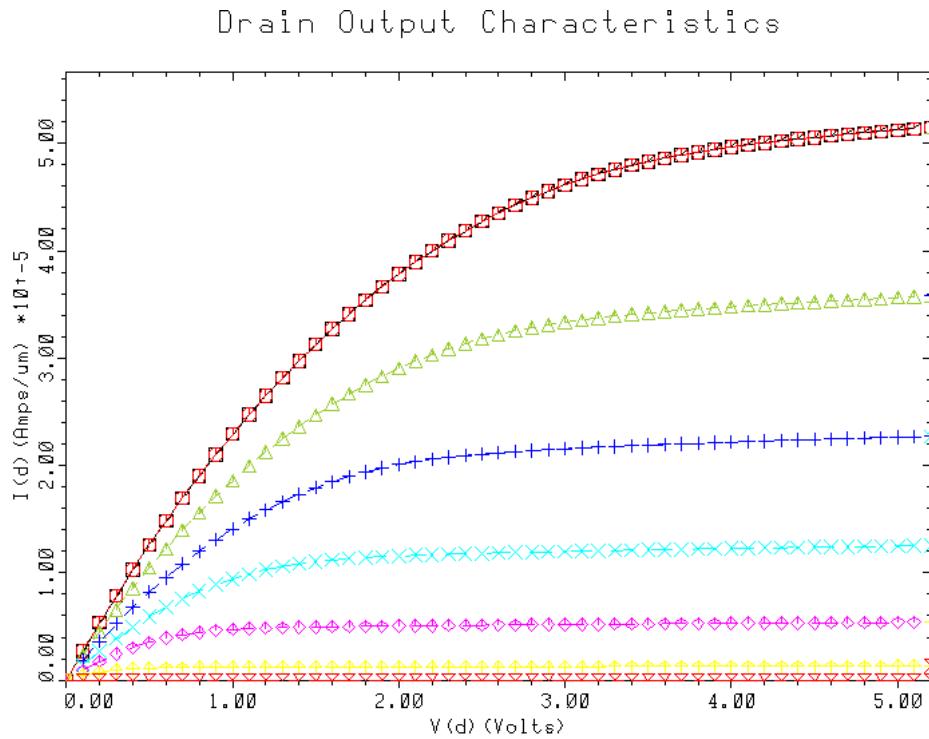
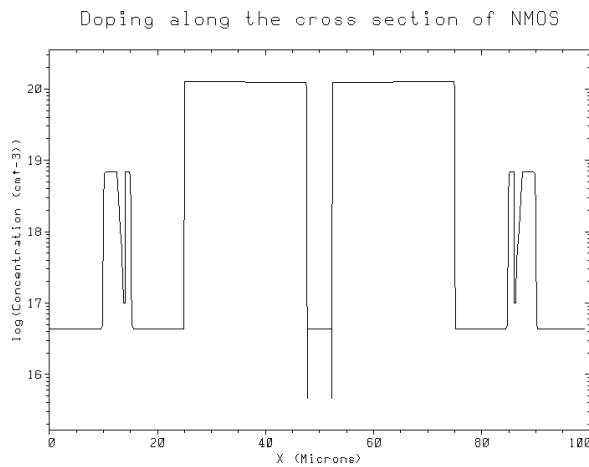


Figure 14: I_D vs V_{DS} plot for NMOS at $V_{sub} = 0V$ when V_G is swept from 0V to 7V with steps of 1V.

Ques. 4 Figure 15 shows the horizontal cross section of the NMOS device along with the doping profiles across the channel and the source. One can estimate the source/drain junction depth of the SN implant from the doping profile across the source. It is 0.3 micrometer as seen from the simulation.



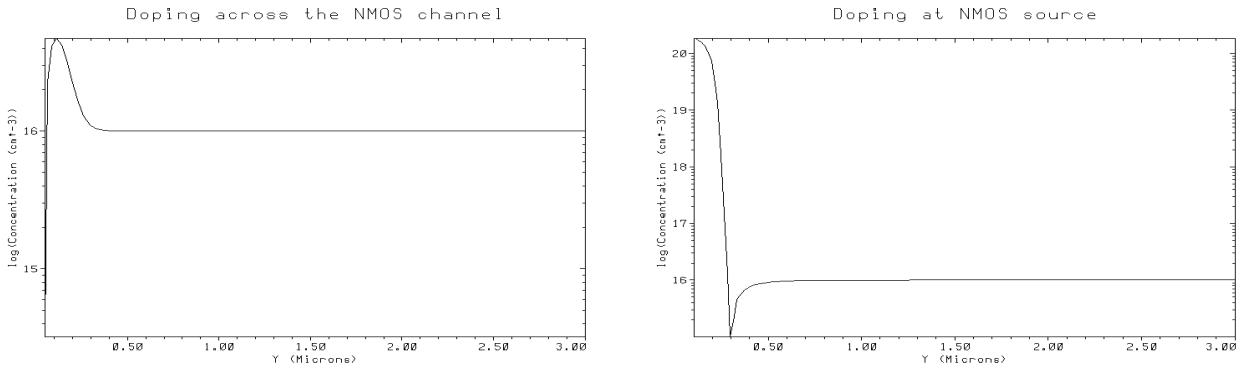


Figure 15: Doping profile of NMOS device along horizontal cross-section (top), vertical across channel (bottom-left), and vertical across Source(bottom-right)

Ques. 7 The graphs below show the effect of different threshold adjust implant. As the implantation is more, the threshold voltage increases. The 3 different doping concentration used are - $3 * 10^{11}$, $6 * 10^{11}$, $9 * 10^{11}$

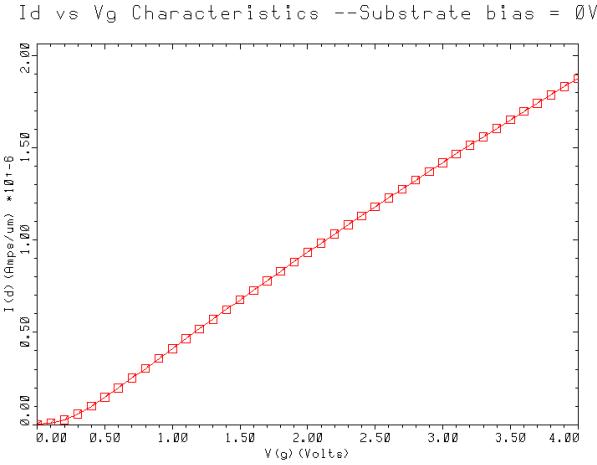
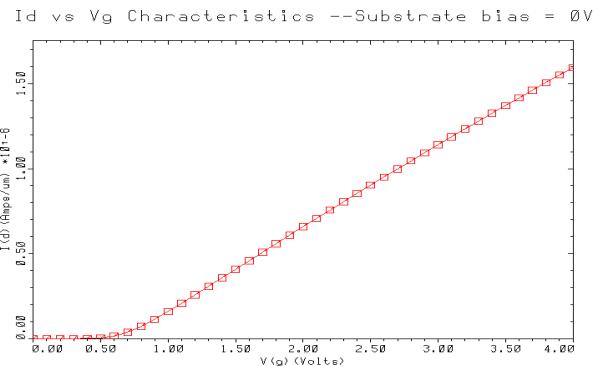
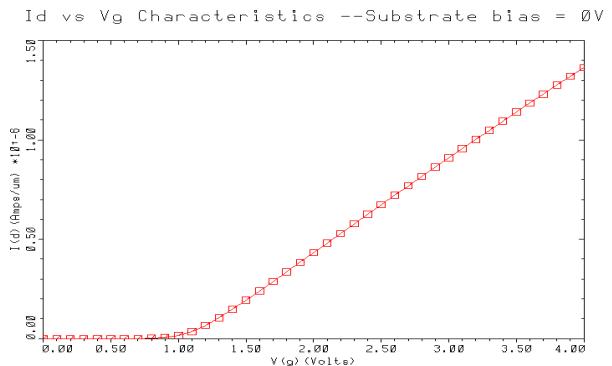


Figure 16: I_D vs V_G plot for NMOS at $V_T = 3e11$



(a) I_D vs V_G plot for NMOS at $V_T = 6e11$



(b) I_D vs V_G plot for NMOS at $V_T = 9e11$

Figure 17: I_D vs V_G plot for NMOS at $V_T = 3e11, 6e11$ and $9e11$

PMOS Device

Ques. 1 Here the PMOS device structure is shown along with the depletion region and the equipotential lines.

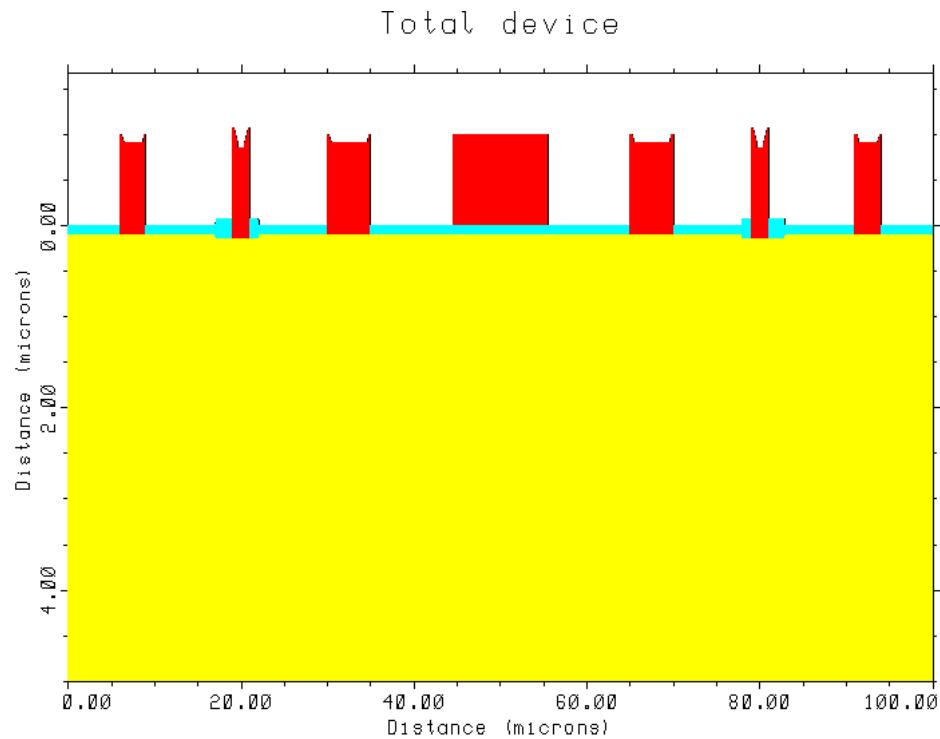


Figure 18: PMOS device structure

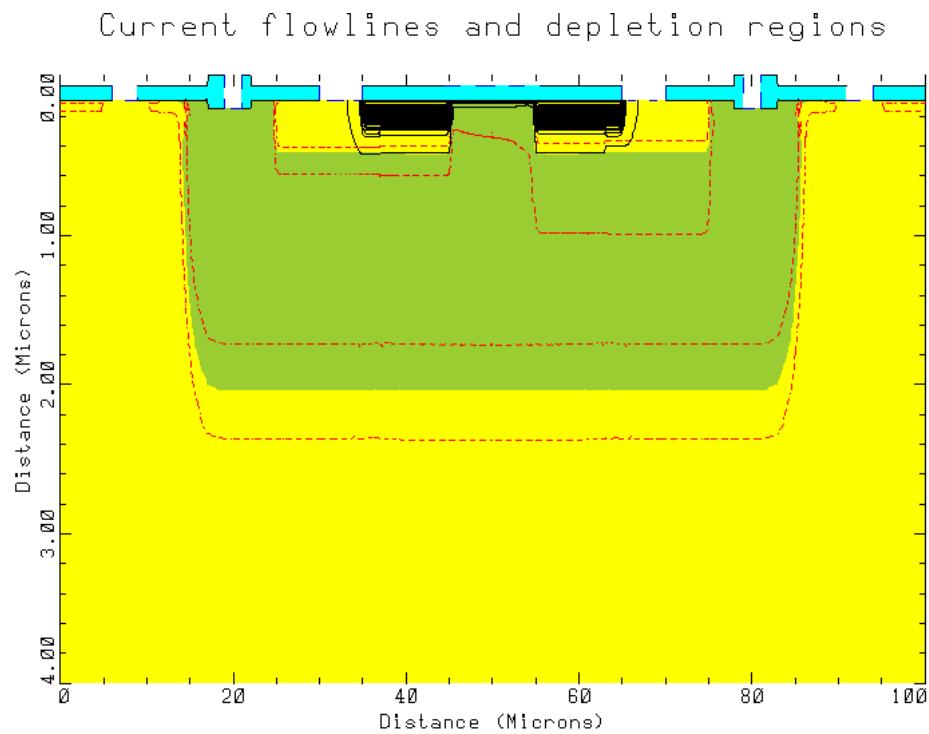


Figure 19: PMOS device current flowlines and depletion regions

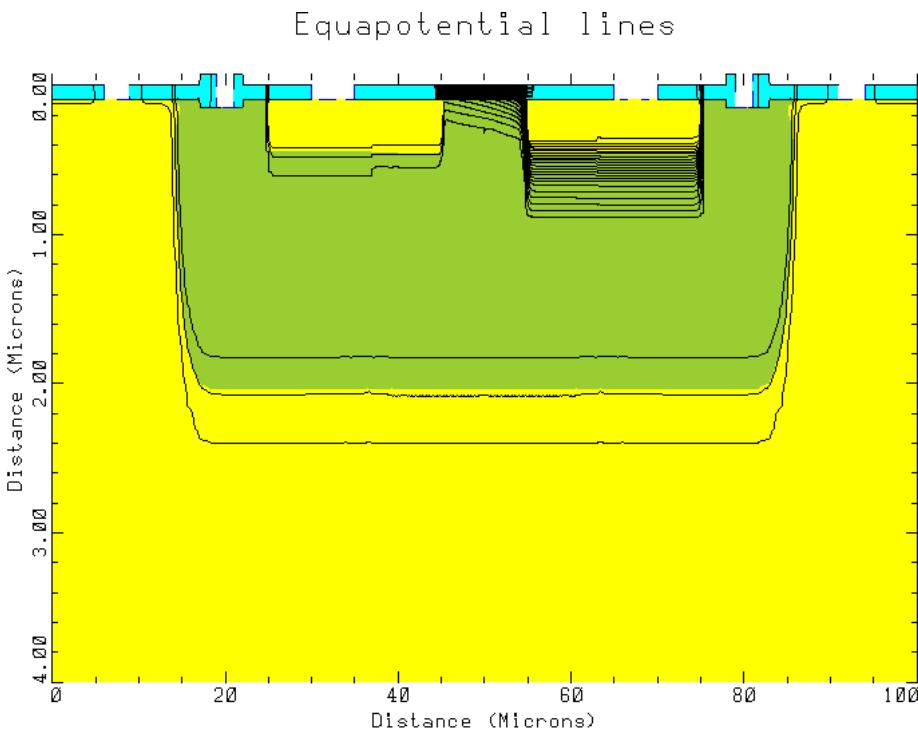


Figure 20: PMOS device equipotential lines

Ques. 2 Now, the I_d vs V_{gs} is plotted for the PMOS device with the substrate bias kept at 0V. Such a characteristic plot is also called the transfer characteristics of the device. One can calculate the threshold voltage from the plot which is around -2.8V. The threshold adjust implant is $9 * 10^{11}$.

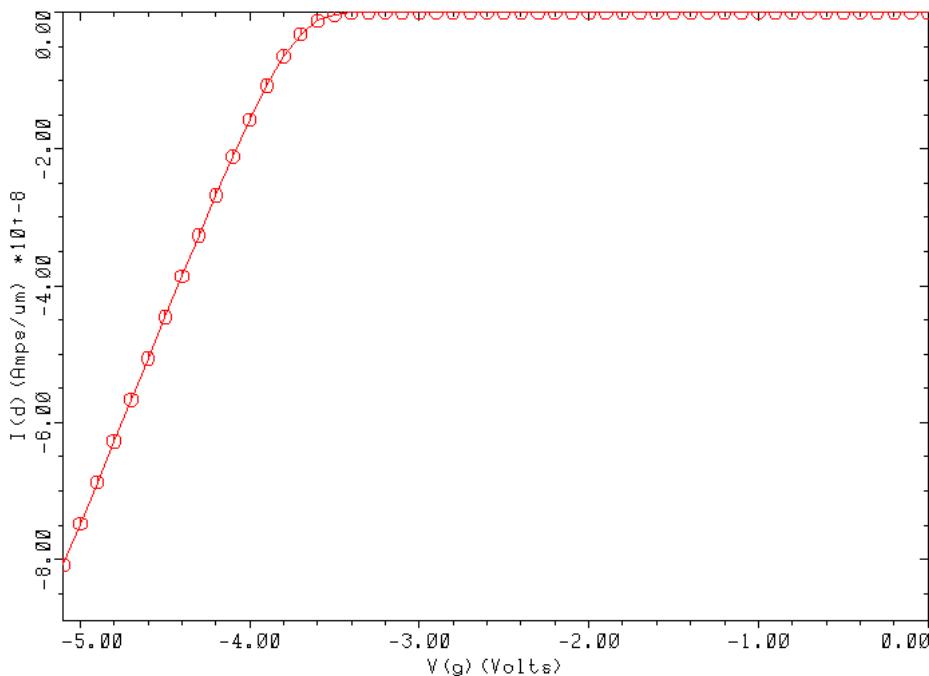


Figure 21: I_D vs V_G plot for PMOS. The substrate bias voltage (V_{sub}) is 0V (red).

Ques. 3 Now, the drain to source voltage is swept for the same device for different gate voltages. This kind of plot is called the output characteristics of the device. One can see that for small V_{ds} (near 0V) the I_d is linearly proportional to V_{ds} . Hence, it forms the linear region of operation. For higher values of V_{ds} (near -5V), the current is saturated as indicated by the horizontal lines. This indicates the saturation behavior of the device. The boundary condition can be given as under -

$$V_{sd} < V_{sg} - V_{th} \text{ - Saturation region}$$

$$V_{sd} < V_{sg} - V_{th} \text{ - Linear region}$$

$$V_{sg} < V_{th} \text{ - Cut-off region}$$

The gate voltage changes from 0 to -7V going from top to bottom.

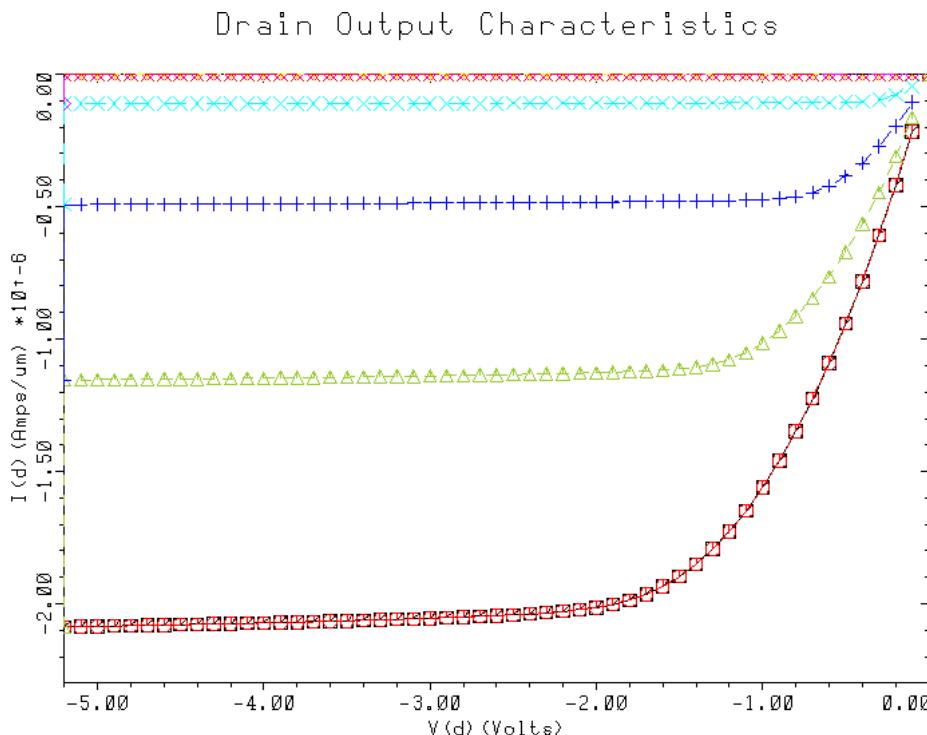


Figure 22: I_D vs V_{DS} plot for PMOS at $V_{sub} = 0V$ when V_G is swept from 0V to 7V with steps of 1V.

Ques. 4 Figure 23 shows the horizontal cross section of the PMOS device along with the doping profiles across the channel and the source. One can estimate the source/drain junction depth of the SP implant and the N-Well implantation from the doping profile across the source. It is 2 micrometers for N-Well and 0.4 micrometers for SP as seen from the simulation.

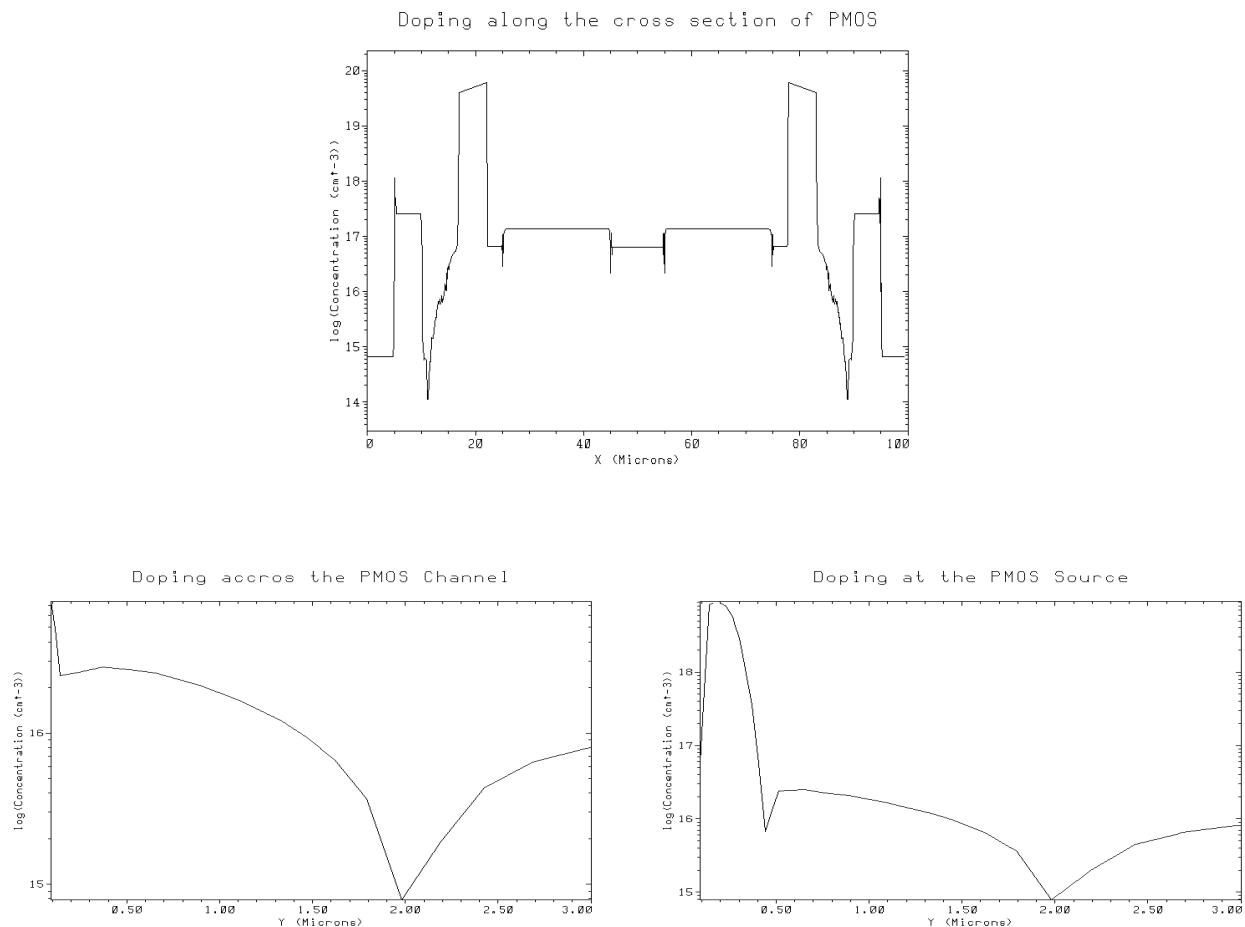
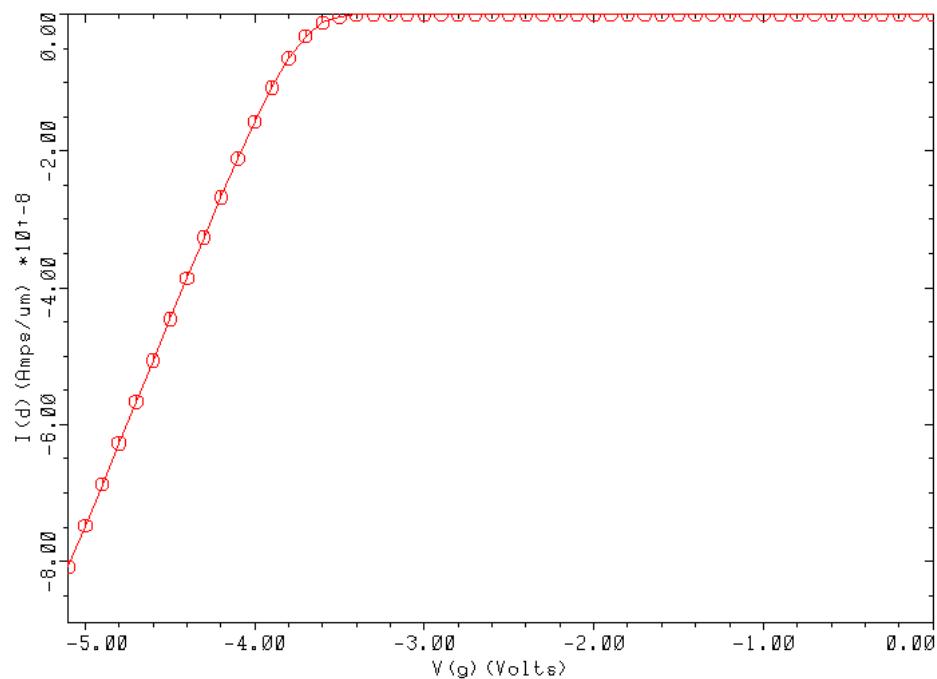
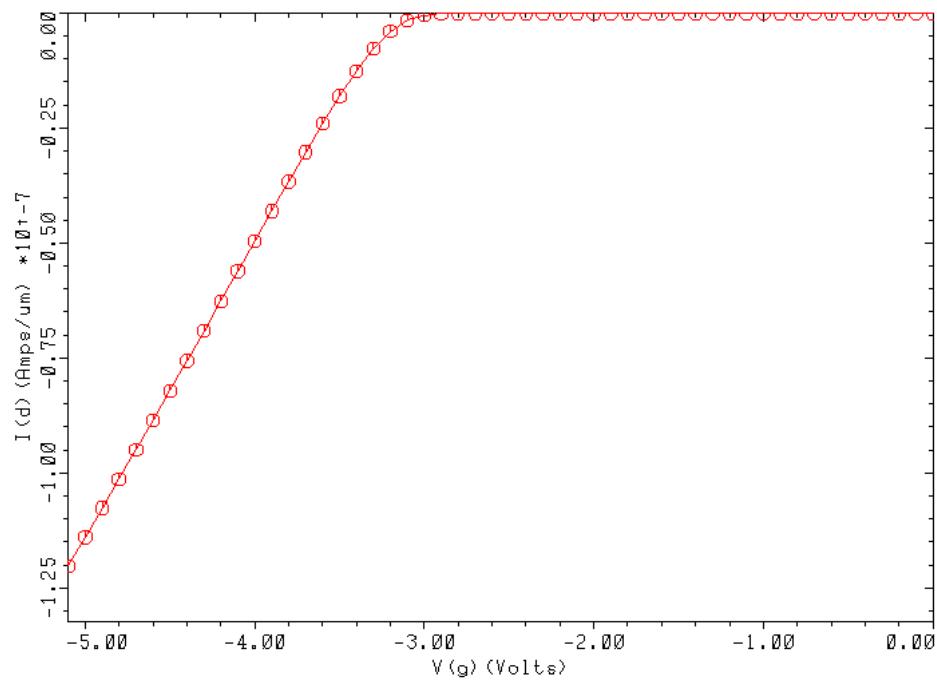
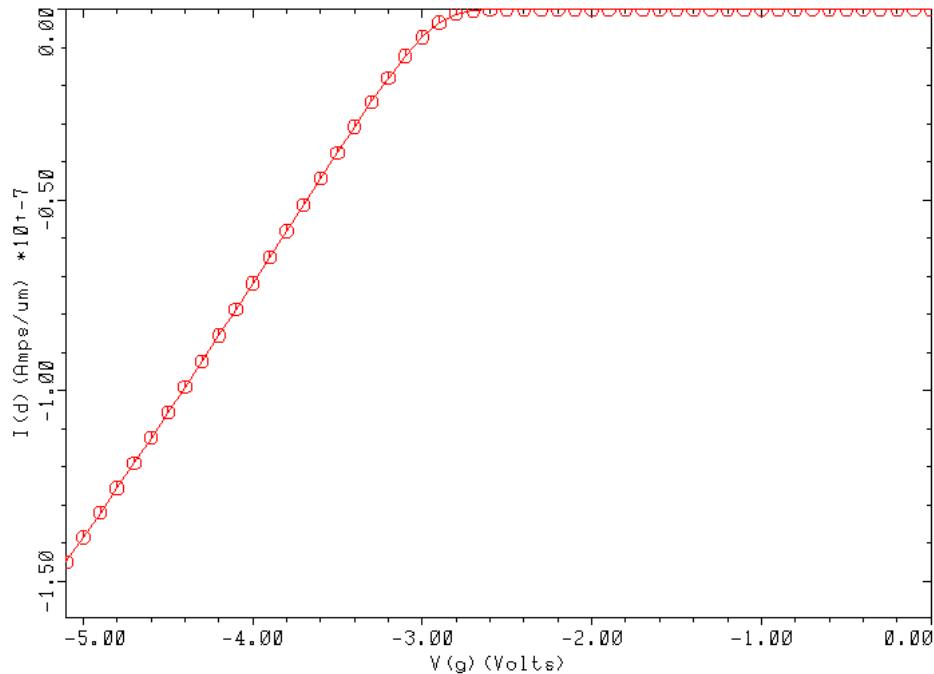


Figure 23: Doping profile of PMOS device along horizontal cross-section (top), vertical across channel (bottom-left), and vertical across Source(bottom-right)

Ques. 7 The graphs below show the effect of different threshold adjust implant. As the implantation is more, the threshold voltage increases. This means it becomes more positive with increase in the threshold adjust implant. The 3 different doping concentration used are - $3 * 10^{11}$, $6 * 10^{11}$, $9 * 10^{11}$

Figure 24: I_D vs V_G plot for PMOS at $V_T = 3e11$ Figure 25: I_D vs V_G plot for PMOS at $V_T = 6e11$

Figure 26: I_D vs V_G plot for PMOS at $V_T = 9e11$

Ques. 4 The table below compares the junction depths of SN,SP and N-Well as calculated in the assignment and the values as obtained from the simulations -

Implantation	Calculated Junction Depth (um)	Simulated Junction Depth (um)
SN	0.0875	0.3
N-Well	2.367	2
SP	0.1865	0.4

Ques. 7 The table below shows the threshold voltages for different threshold adjust implants for NMOS and PMOS device. As mentioned before, with higher dosage of threshold adjust implant, the threshold voltage becomes more positive for both NMOS and PMOS.

VT-Adjust dose	VT(V) for 3E11	VT(V) for 6E11	VT(V) for 9E11
NMOS, V _{sub} = 0V	0.2 V	0.7 V	1.1 V
NMOS, V _{sub} = -1V	X	X	2.1 V
NMOS, V _{sub} = -2V	X	X	2.6 V
PMOS, V _{sub} = 0V	-3.6 V	-3.2 V	-2.8 V

5 Processing

The processing step of the IC-Technology Lab was performed on May 13th, 2019 under assistance of Hande Aydogmus, PhD Researcher at Department of Microelectronics. The complete process is described in following steps:

Step 1: OXIDATION

Oxidation step is performed in a Temprus Furnace. It can also be used for implantation. We use the online tool Oxide Growth Calculator to calculate the time required by the Temprus furnace to grow an Oxide layer of desired thickness viz. 300 nm at 1000°C. For low temperature CVD, we use temperatures 500 - 900 °C.

Calculated time for Oxide layer growth are as follows:

Dry Oxidation: 15 hours 21minutes 13 seconds

Wet Oxidation: 41 minutes 21 seconds

Dummy Wafers are placed at the start and end of the batch in the furnace. The rack is made of Silicon Carbide (SiC) and place holders are made of Quartz. The Wafers used in our experiment are p-type, (100) and are 500 μ m thick.

We have placed the wafer inside the furnace for 41 minutes 21 seconds and we proceed to the next step.

Step 2: ETCHING

In this step, we proceed with a different wafer. To remove organic impurities from the wafer we use highly concentrated 99% HNO₃ acid. Green Metals such as, Al, Al/Si, Ti, Mo, Zr, Ge can be removed using 99% HNO₃.

Here, we remove Al from the Si wafer. So, we dip the wafer in HNO₃ for 10 minutes.

The etching process involves use of concentrated acids and high care must be taken care during this processing step. In order to ensure safe chemical handling, Else Kooi Lab recommends ‘buddy system’ to ensure proper safety measures. Timer should be used to accurately time the process to prevent over-etching and remove the wafer when done.

Other Deposition Techniques :

1. Atomic layer deposition (ALD) is a thin-film deposition technique based on the sequential use of a gas phase chemical process; it is a subclass of chemical vapour deposition. The majority of ALD reactions use two chemicals called precursors. These precursors react with the surface of a material one at a time in a sequential, self-limiting, manner. Through the repeated exposure to separate precursors, a thin film is slowly deposited.

Tetraethyl orthosilicate (TEOS) is mainly used as a precursor to silicon dioxide in the semiconductor industry.

2. Electron-beam Physical Vapour Deposition (EBPVD) is a form of physical vapor deposition in which a target anode is bombarded with an electron beam given off by a charged tungsten filament under high vacuum. The electron beam causes atoms from the target to transform into the gaseous phase. These atoms then precipitate into solid form, coating everything in the vacuum chamber with a thin layer of the anode material.

Step 3: CLEANING

After 10 minutes in conc. HNO₃, we take the wafer out and clean it with demineralized water for 5 minutes. Notes that we can associate this time with the resistivity of the wafer 5 minutes \sim 5 M Ω . After this, we place the wafer in N₂ dryer and Spinner to dry off the wafer.

Step 4: PECVD for Deposition and Plasma Etching

This steps involves deposition of photoresist on the wafer. For this, Syringe EVG120 resist processing system is used. We first align our wafers and do coating of HMDS on place on hotplate. Then photoresist is applied. The thickness of photoresist layer is at $1.4\mu\text{m}$.

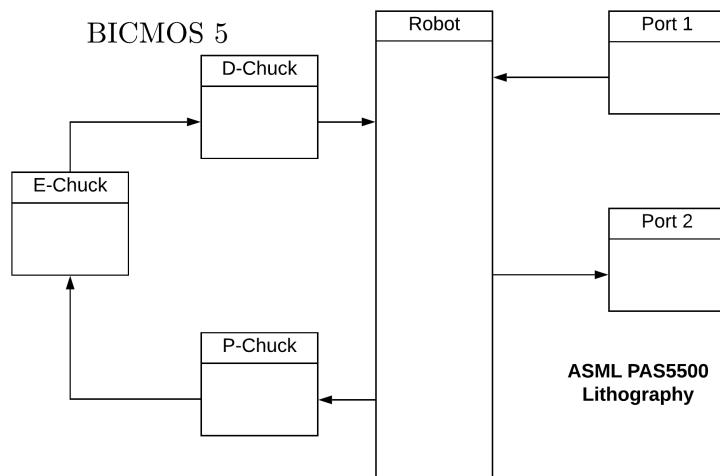
Step 5: Lithography

We apply use the IC mask for patterning on the chip by lithography. We can either use, Wafer Stepper (automatic operation) or Contact Aligner (manual operation).

In this step, we are going to use the Wafer Stepper. The machine used at this step is ASML PAS5500 and it does one image at a time.

The details related to the Mask are:

Glass & Chrome - Box 411	Layer Name: IC(8)
Size: $6 \times 6 \text{ cm}$	Exposure: 140mJ/cm^2



After the exposure, we perform the post exposure bake (PEB). We align the wafers again before placing it in the EVG120 coaten resist processing system. PDMS is the commonly used polymer.

Step 6: Measurement using 4-point probe (for green metals)

n-well (Dopant: Phosphorus):

$R_s\text{-avg.} = 1497 \text{ Ohm/sq}$

Standard Deviation = $7.394 \quad 0.494\%$

shallow-n (Dopant: Boron):

$R_s\text{-avg.} = 57.33 \text{ Ohm/sq}$

Standard Deviation = $0.978 \quad 1.707\%$

shallow-p: (Dopant: Arsenic)

$R_s\text{-avg.} = 494.8 \text{ Ohm/sq}$

Standard Deviation = $6.921 \quad 1.399\%$

We cannot judge from $R_s\text{-avg.}$ without knowing dopant concentration.

Sheet Resistivity:

.	Dopant Conc.	Junction Depth
n-well	$\rightarrow 1.61e+16$	$2.0\mu\text{m}$
shallow-p	$\rightarrow 8.24e+18$	$0.2\mu\text{m}$
shallow-n	$\rightarrow 5.17e+19$	$0.3\mu\text{m}$

Resistivity $\rho(\Omega - cm)$:

n-well $\rightarrow 0.2994$

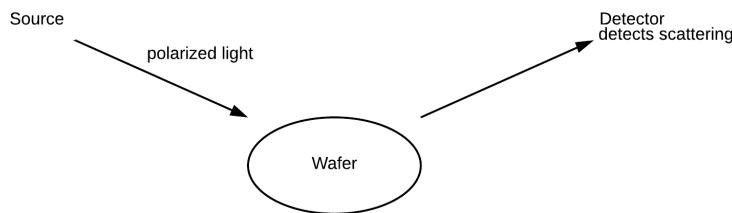
shallow-p $\rightarrow 0.00114$

shallow-n $\rightarrow 0.0148$

Step 7: Measurement of Thickness of Wafer

We take out the wafer that was kept in the furnace for Oxidation. We note a difference that the PECVD process oxidises the wafer only on one side, while in the furnace, both sides of the wafer gets oxidised.

To measure the thickness, we use the Woolam M-2000 Ellipsometer which checks the thickness at 5 points.



Furnace Oxidised Wafer:

Thickness = 296.32 nm Standard Deviation = 0.69072

Confidence = 0.03 MSE = 9.3960 n = 1.457

PECVD Oxidised Wafer:

Thickness = 305.87 nm Standard Deviation = 0.13418

Confidence = 0.07 MSE = 18.576 n = 1.457

Step 8: Wet Etching:

We do wet etching for 30 seconds in Buffered HF 1:7, then put in the demineralized water for 5 minutes ($\sim 5 \text{ M}\Omega$ resistivity). We then Nitrogen spray dry the wafer and perform Spinning to dry the wafer.

Wet Etching is more selective than dry etching.

Step 9: Measurement of Thickness after Etching

Furnace Oxidised Wafer:

Thickness = 244.88 nm Standard Deviation = 3.110

PECVD Oxidised Wafer:

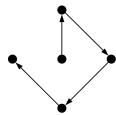
Thickness = 136.98 nm Standard Deviation = 7.1369

Etch Rate (note that the wet etching performed in this step is done for 30 seconds.):

Furnace Oxidised Wafer: 1.714 nm/sec

PECVD Oxidised Wafer: 5.629 nm/sec

We used the same Woolam M-2000 Ellipsometer. It takes 5 measurements in the following manner:



Step 10: Dry Etching We do Reactive Ion Etching with plasma for Dry Etching. The Trikon Omega 201 Etch machine is used.

The steps to operate are: change the temperature to $T = 25^{\circ}\text{C}$, Load the wafer and Sequence AC06_350, and Run.

Step 11: Laser microscope measurement after Plasma Etching

The images and the measured lengths are tabulated below:

Van der Pauw Structures:

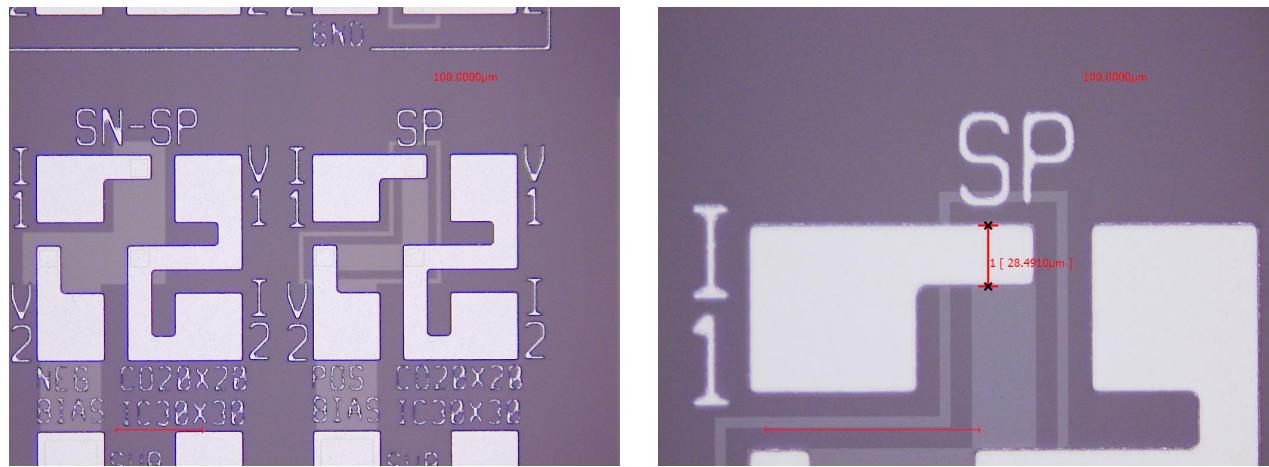


Figure 27: Van Der Pauw Structures under microscope after Dry Etching

NMOS Structures:

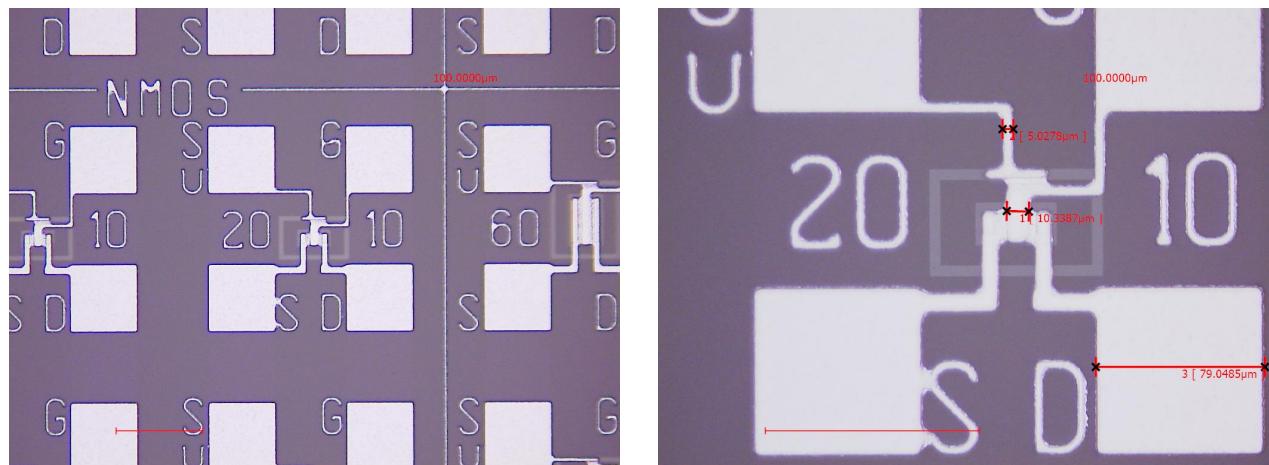


Figure 28: NMOS Structures under microscope after Dry Etching

PMOS Structures:

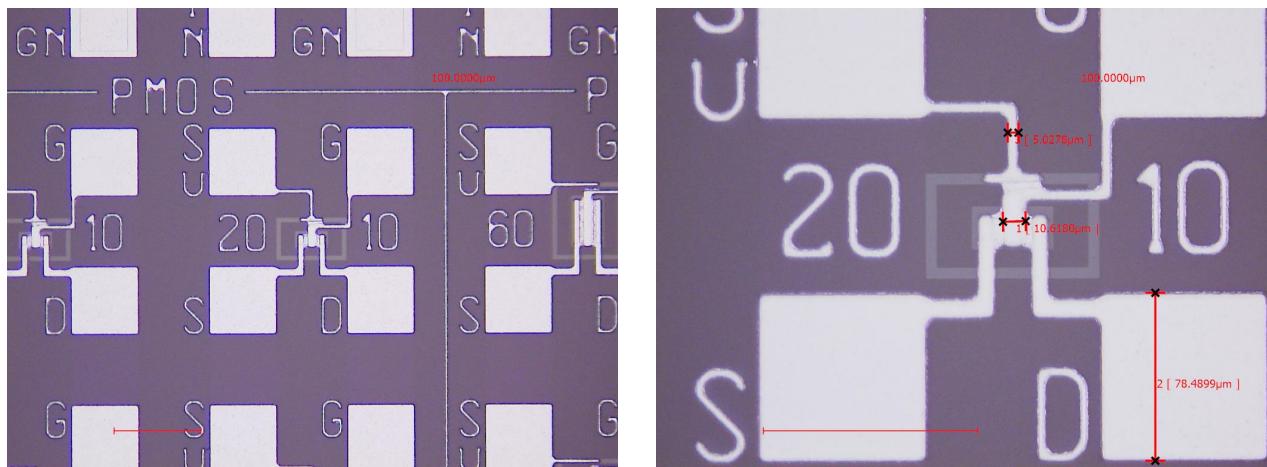


Figure 29: PMOS Structures under microscope after Dry Etching

	Source (μm)	Gate (μm)	Drain (μm)
PMOS	5.02	10.61	78.48
NMOS	5.02	10.33	79.04

Table 2: Dimensions of NMOS and PMOS after Dry Etching

Step 12: Wet Etching of Patterned Wafer (using Phosphoric Acid)

Triton X - 100 (48 sec) → Al Etch 35C (PES 77-19-04) (4 mins + 30 sec of overetching)
→ Demineralized Water (4 mins)

Step 13: Measure:

The images and the measured lengths are tabulated below:
Van der Pauw Structures:

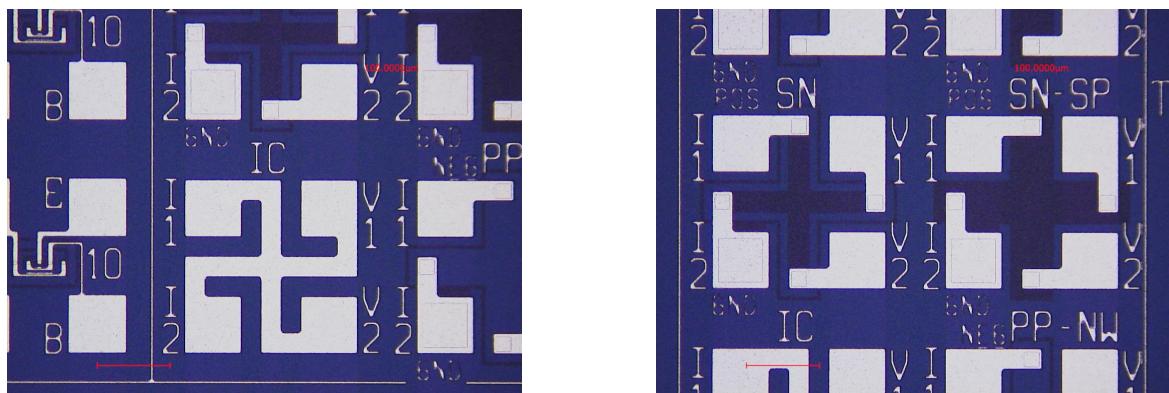


Figure 30: Van Der Pauw Structures under microscope after Wet Etching

NMOS Structures:

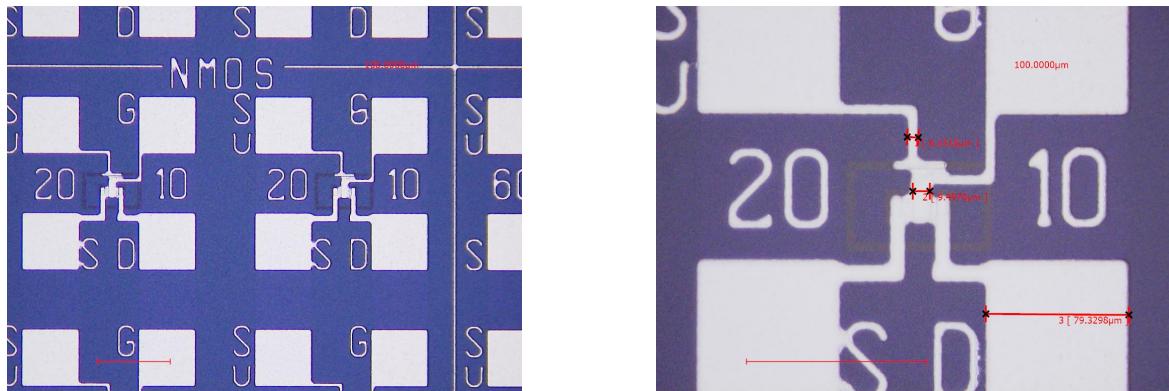


Figure 31: NMOS Structures under microscope after Wet Etching

PMOS Structures:

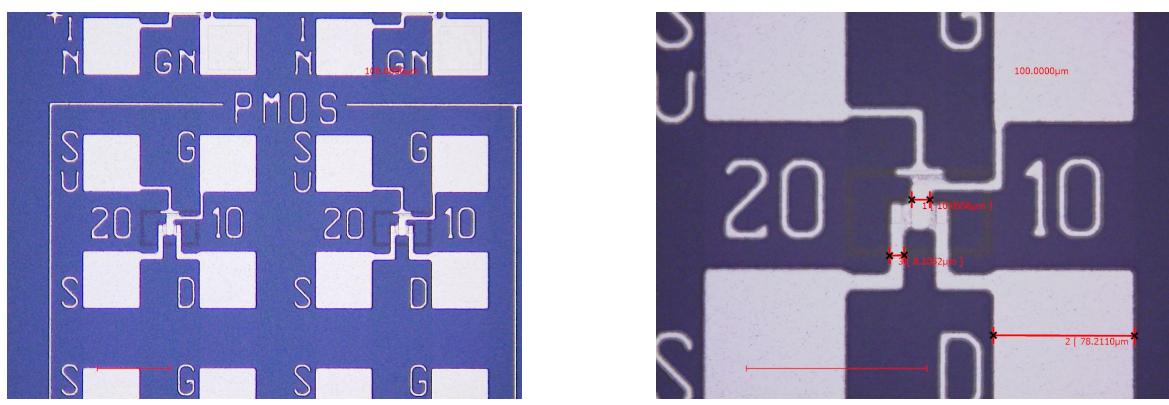


Figure 32: PMOS Structures under microscope after Wet Etching

	Source (μm)	Gate (μm)	Drain (μm)
PMOS	8.10	10.05	78.21
NMOS	6.15	9.49	79.32

Table 3: Dimensions of NMOS and PMOS after Wet Etching

Dry Etching vs. Wet Etching

Wet etching is highly selective and has high etching rate. Chemicals used in Wet etching generally remove the substrate material under the masking material. Dry etching does not etch in one direction and can enter from beneath the masking material.

We measure after Wet Etching. Wet etching is very selective but we have 99% Al and 1% Si. See images below.

So we have traces of Si and photoresist (PR) left even after wet etching. This is depicted by the Blue Surface.

Therefore, we do Si-Wet etching to get 1% Si out.

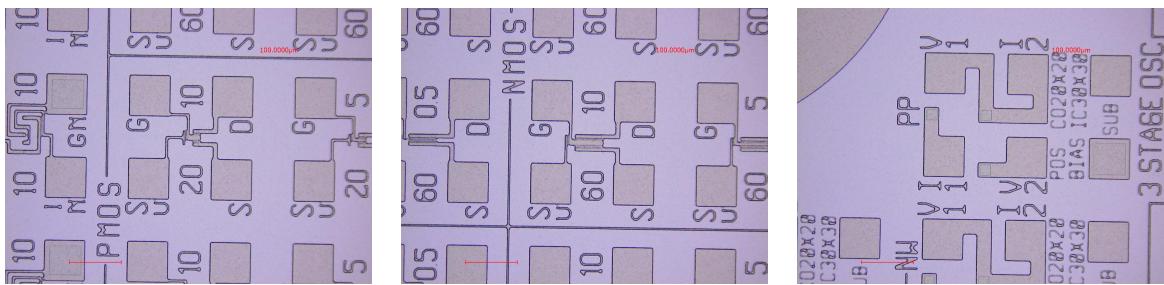


Figure 33: Images when PR is not etched. After this, we do the next step: Si Wet Etching

Step 14: Si Wet Etching:

Poly-Si Etch is done using HNO_3/HF (40%) for 15 seconds.

+ Acetone after wet etching to remove the PR

+ Oxygen Plasma after dry Etching to remove the PR

Note: In this step, we had to etch again for another 15 seconds.

Images after Poly-Si Etch are shown below:

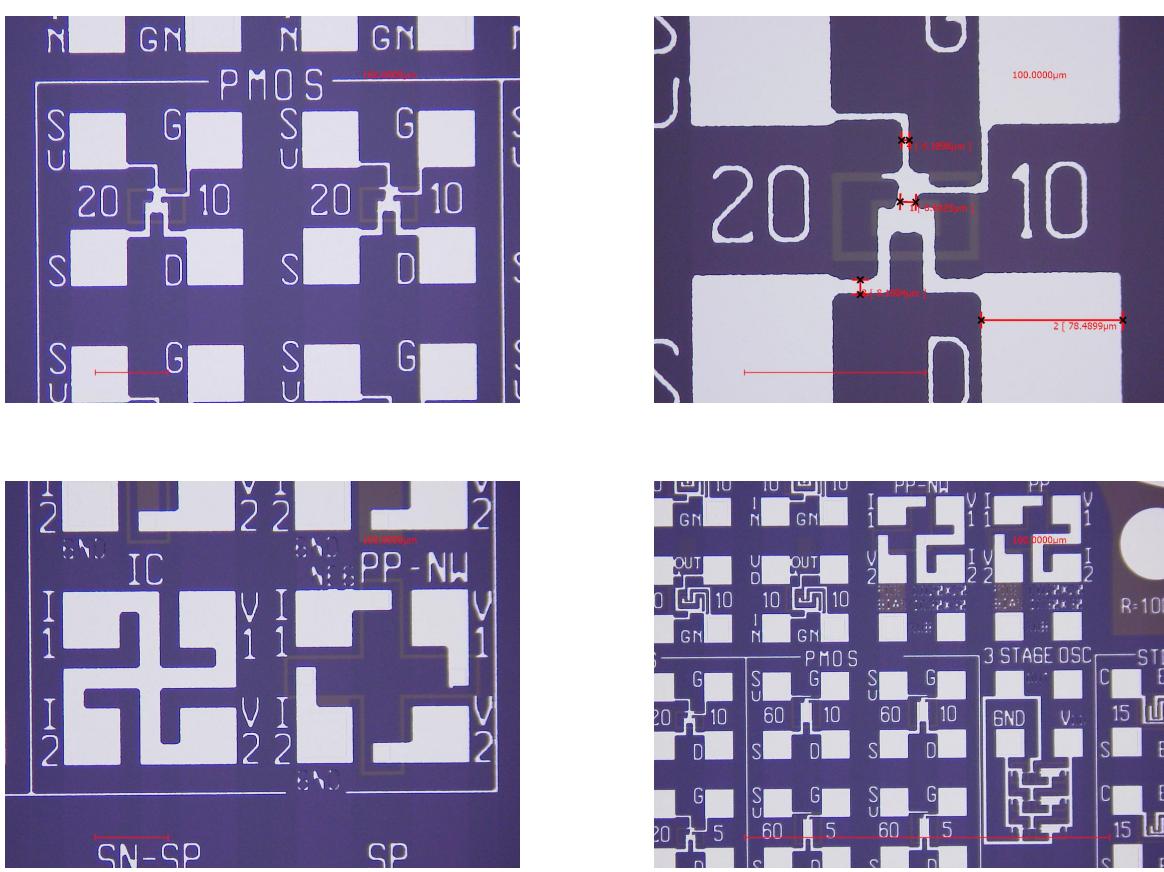


Figure 35: Wet Poly-Si Etch Structures

6 Measurements

In this chapter, we summarise our finding from performing measurements on PMOS, NMOS and resistance structures on the Silicon Wafer. These measurements helps determine device performance and in calculation of mobility of transistor. We used the Four-probe station to apply voltage and current to the different structures on the chip and record the result parameters. All plots are created in MATLAB R2017B.

We first perform resistance measurements. These can be done by two methods: Van der Pauw (VdP) method or using electrical linewidth (ELM) structures. The formulae used for calculations are:

$$R = \rho \cdot \frac{L}{W \times d} = R_{\square} \cdot \frac{L}{W}$$

by knowing sheet resistance and junction depth, we can calculate doping concentration by calculating resistivity first and then using Irving curves.

6.1 Using VdP Model

In this method, the resistivity of the layers is to be checked. A diagram of the four probe method is shown in figure 36.

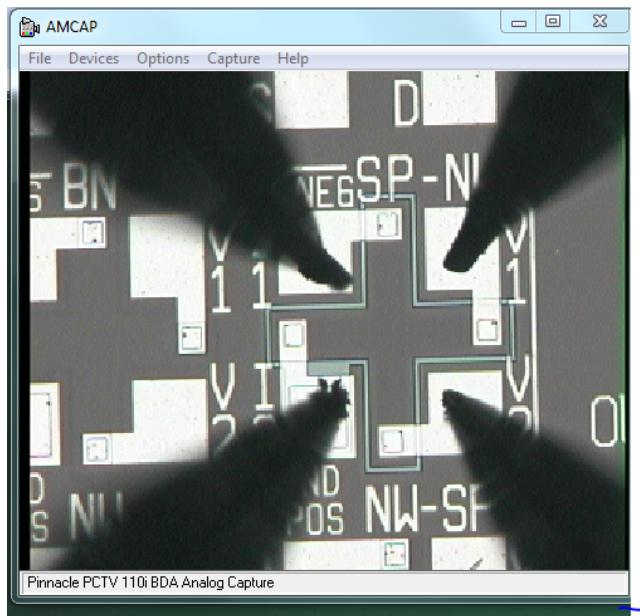


Figure 36: Four Probe Station

The calculation of the sheet resistance is done as follows:

$$R_{\square} = \frac{\pi}{\ln 2} R_{AB,CD}$$

$R_{AB,CD}$ is the measured resistance from the station.

By having sheet resistance, we can calculate resistivity and dopant concentration (using Irving curves).

Assignment :

1. We measure the Van der Pauw structures to determine sheet resistance of different types of implants. Since the pn junction has a threshold voltage of about 0.7V, an input voltage of $-0.2 < V_{in} < 0.2$ would hold the reverse bias condition towards the substrate.
2. Measured Sheet Resistance (using Van der Pauw Structures) of N Well (NW), Shallow n (SN), Shallow p (SP-NW) and IC layer.

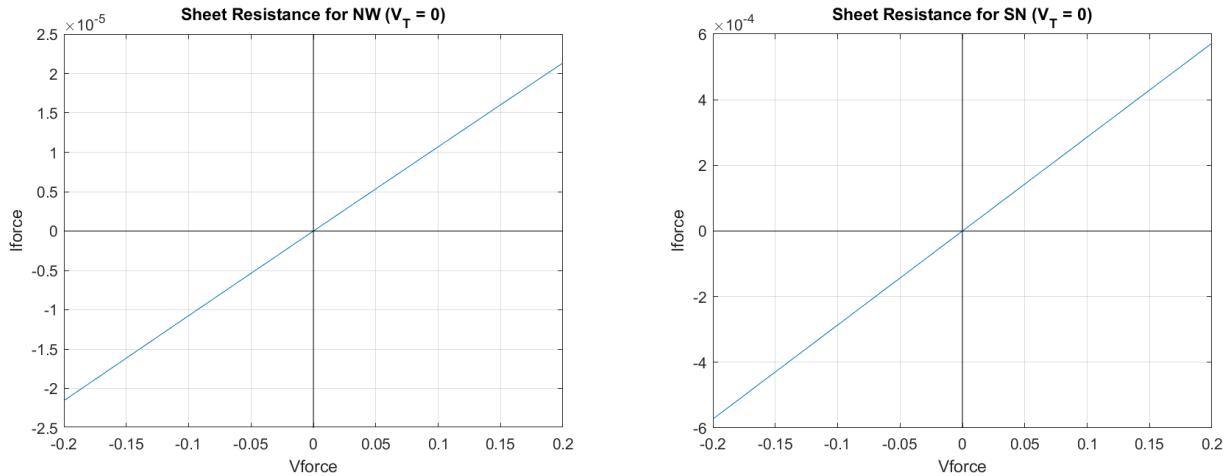


Figure 37: Sheet Resistance of NW and SN

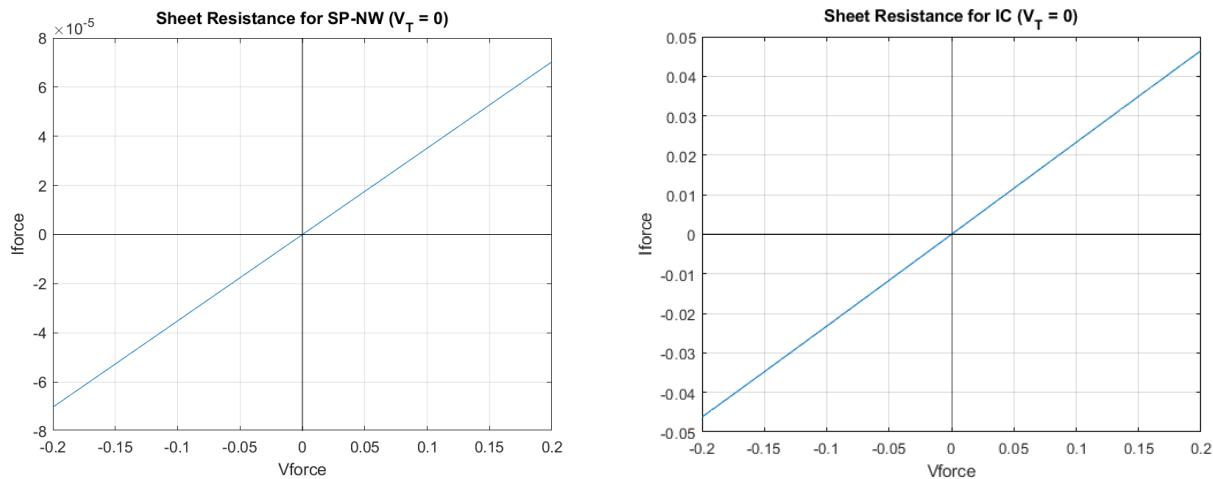


Figure 38: Sheet Resistance of SP-NW and IC layer

The Resistance and Sheet Resistance is calculated and tabulated below:

	$R_{AB,CD}(\Omega)$	$R_{\square}(\Omega)$	$\rho(\Omega - cm)$	Dopant Conc. (per cm^3)
NW	9765	44.25×10^3	8.8500	3.47×10^{17}
SN	374	1695	0.05085	1.36×10^{18}
SP-NW	3044	13.797×10^3	0.5518	2.356×10^{18}
IC	4.6	20		

Table 4: Resistance measurements using VdP method

3. Compare the sheet resistance between implantation and the metal, and explain the difference in magnitude.

6.2 Using ELM Model

In ELM measurements the structure width is comparable to the lateral out-diffusion. Using this we can investigate the effects of lateral out-diffusion.

1. Measure the Resistance of NW with electrical linewidth measurement structures of width $2\mu\text{m}$, $5\mu\text{m}$ and $10\mu\text{m}$.

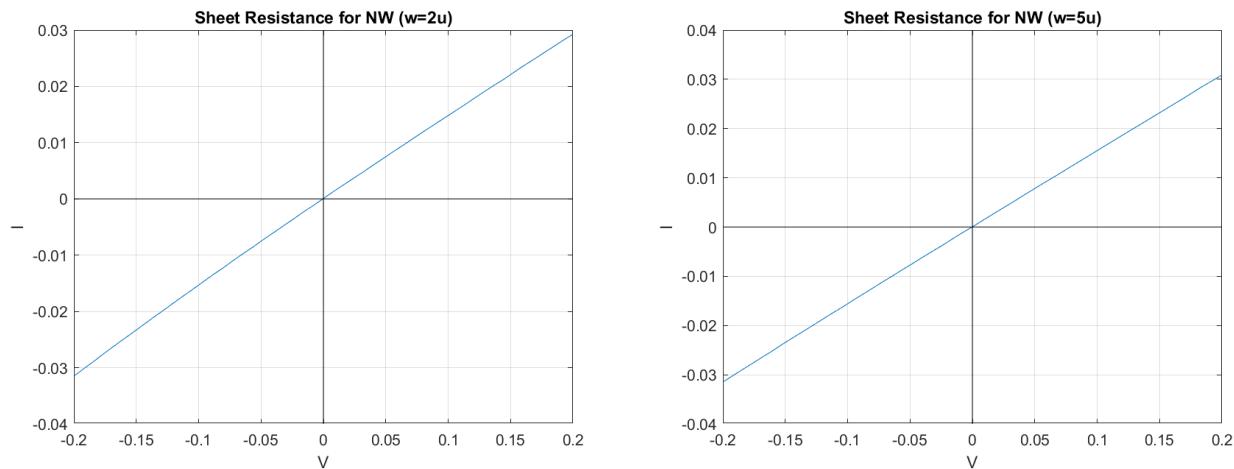


Figure 39: Resistance of NW at Structure width = $2\mu\text{m}$ and $5\mu\text{m}$

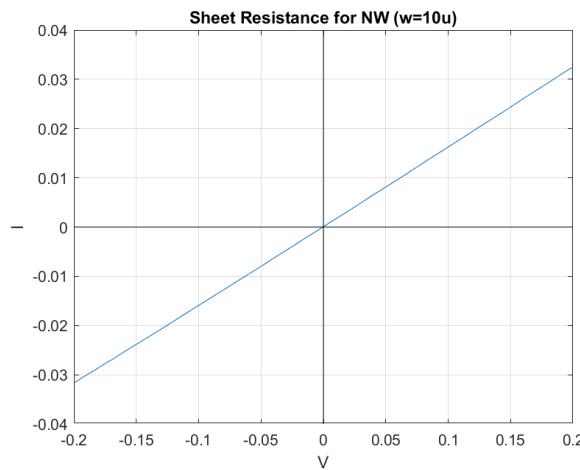


Figure 40: Resistance of NW at Structure width = $10\mu\text{m}$

2. Measure the Resistance of SN with electrical linewidth measurement structures of width $2\mu\text{m}$, $5\mu\text{m}$ and $10\mu\text{m}$.

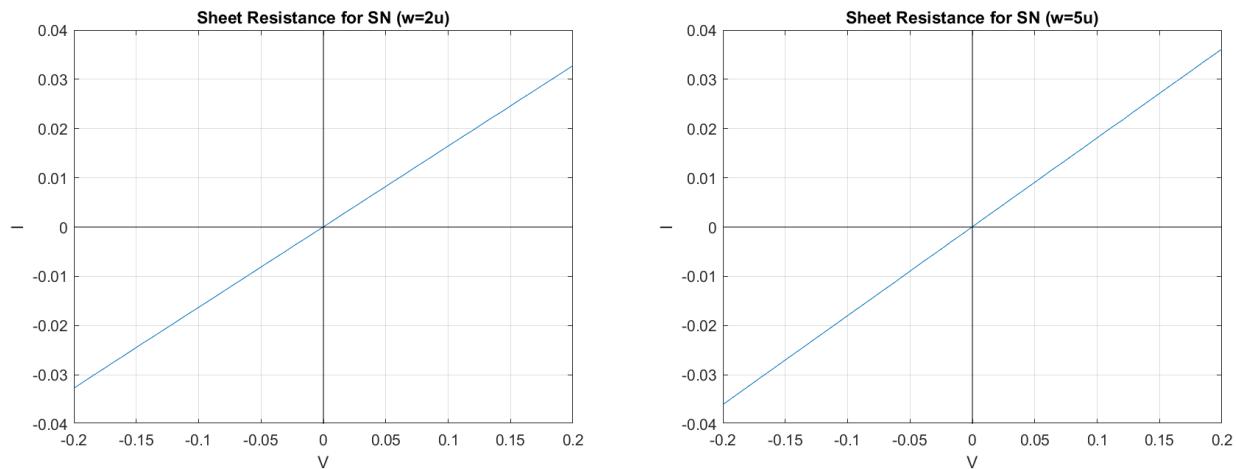


Figure 41: Resistance of SN at Structure width = $2\mu\text{m}$ and $5\mu\text{m}$

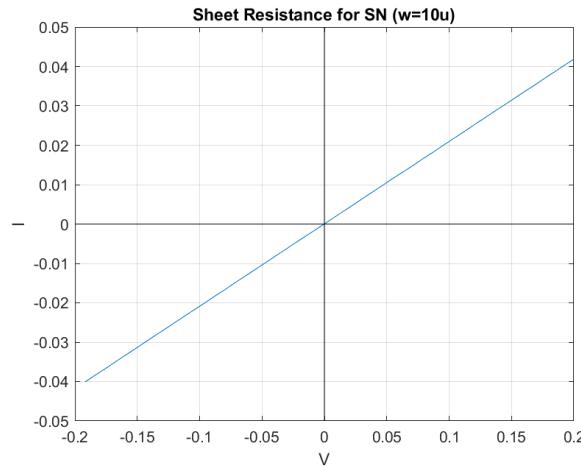


Figure 42: Resistance of SN at Structure width = $10\mu\text{m}$

The Resistance measurements are summarized in the table below:

	$R_{measured}$	R_{\square}
NW $2\mu\text{m}$	$256 \text{ k}\Omega$	$2.49 \text{ k}\Omega$
NW $5\mu\text{m}$	$103 \text{ k}\Omega$	$2.5 \text{ k}\Omega$
NW $10\mu\text{m}$	$43 \text{ k}\Omega$	$2 \text{ k}\Omega$
SN $2\mu\text{m}$	$8.767 \text{ k}\Omega$	85.1Ω
SN $5\mu\text{m}$	$3.582 \text{ k}\Omega$	86Ω
SN $10\mu\text{m}$	$47 \text{ k}\Omega$	$2.28 \text{ k}\Omega$

Table 5: ELM Resistance Measurement

3. The plot for Sheet Resistance as a function of Width is shown below:

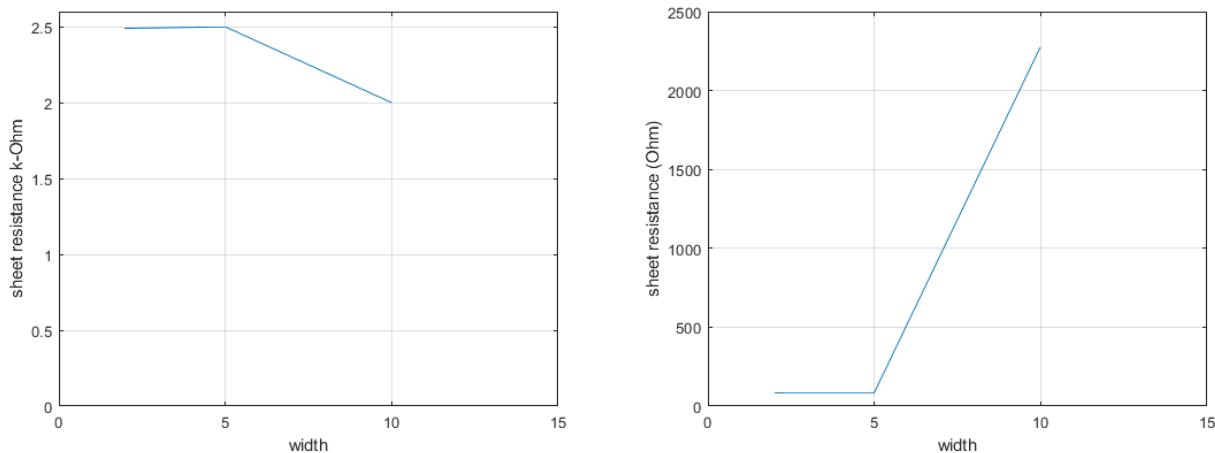


Figure 43: sheet Resistance vs width graph (NW on left and SN on right)

The sheet resistance is calculated shown the table above. The lateral out-diffusion can be observed from the the sheet resistance as it is different for structures with different width.

For NW, the sheet resistance decreases with the increase in width of structure whereas for SN, the sheet resistance increases with increase in width of structure.

Note: Minor difference observed with lights on and off on the probe station. Though it happens rarely, it is recommended to keep the light off while running measurements.

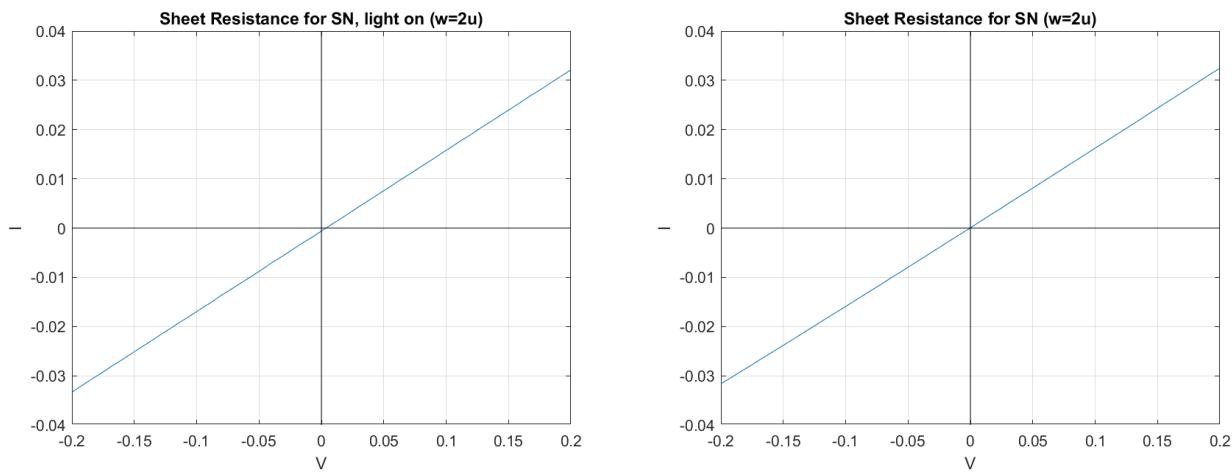


Figure 44: Difference in measurements while keeping the light on and off on the probe station. A difference is observed in the measurements (near origin).

6.3 MOSFET Measurements

6.3.1 PMOS Measurements

I_D vs V_G graphs in V_T -adjust of $9E11$ ions/cm 2 doping quadrant is shown below.

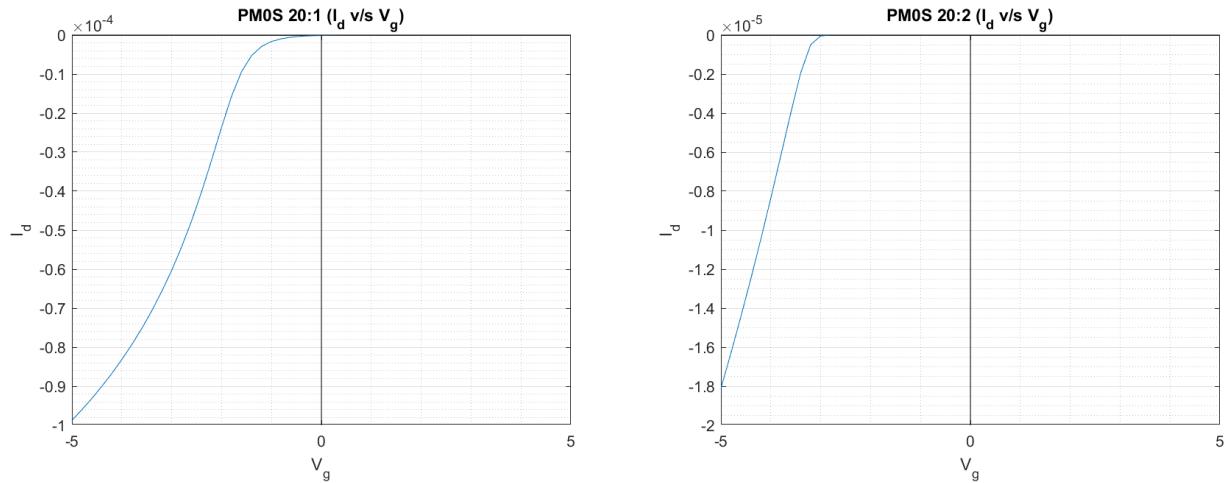


Figure 45: I_D vs V_G for transistor dimensions 20:1 and 20:2 (width:length) in V_T -adjust of 9E11 ions/cm² doping quadrant

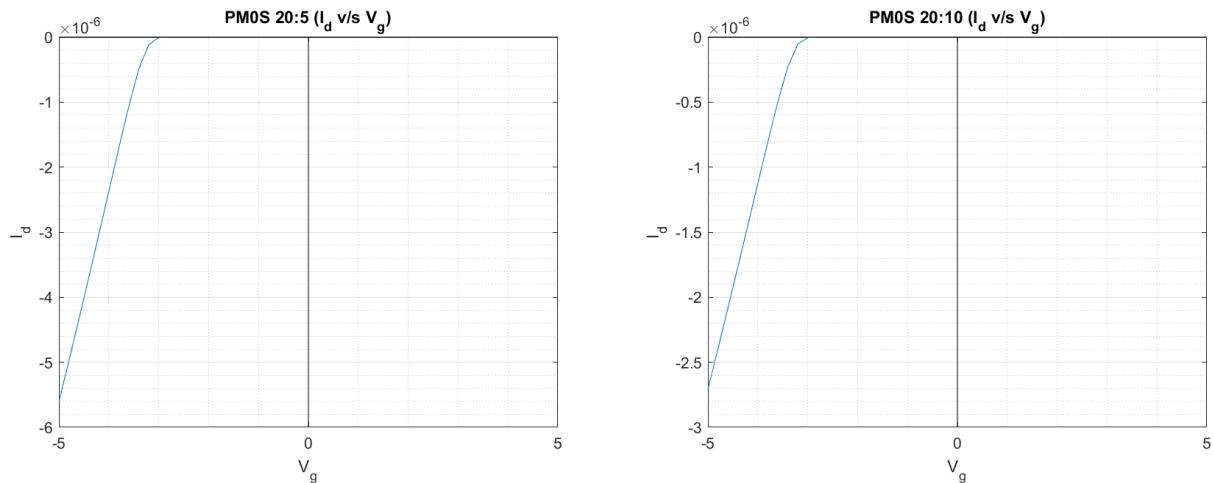


Figure 46: I_D vs V_G for transistor dimensions 20:5 and 20:10 (width:length) in V_T -adjust of 9E11 ions/cm² doping quadrant

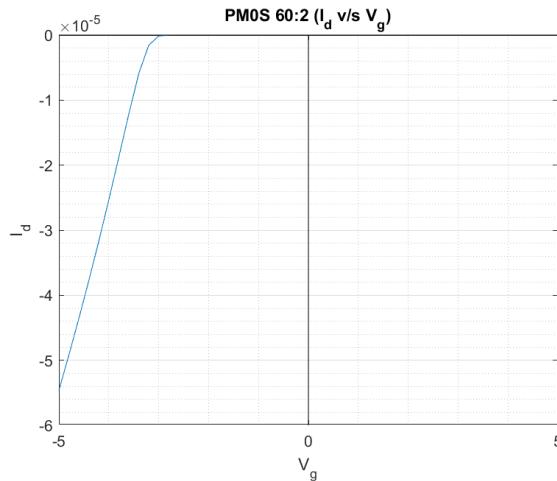


Figure 47: I_D vs V_G for transistor dimensions 60:2 (width:length) in V_T -adjust of 9E11 ions/cm² doping quadrant

Influence of W/L: W/L ratio directly affects the drain current I_D .

PMOS transistor W/L ratio	V_{th} (V)
20:1	-0.2
20:2	-3
20:5	-3
20:10	-3
60:2	-3

Table 6: V_{th} for different PMOS transistor sizes

The calculated hole mobilities for different W/L dimensions of PMOS transistors are given in the table below for 9E11 ions/cm³ doping:

PMOS W/L	Hole Mobility (μ_p)
20:2	289
20:5	231
20:10	231
60:2	182

Table 7: Hole Mobility for different PMOS W/L size transistor sizes

From the table it is clear that V_{th} does not depend on geometry of the transistor.

I_D vs V_G in V_T -adjust of 0 ions/cm² doping quadrant

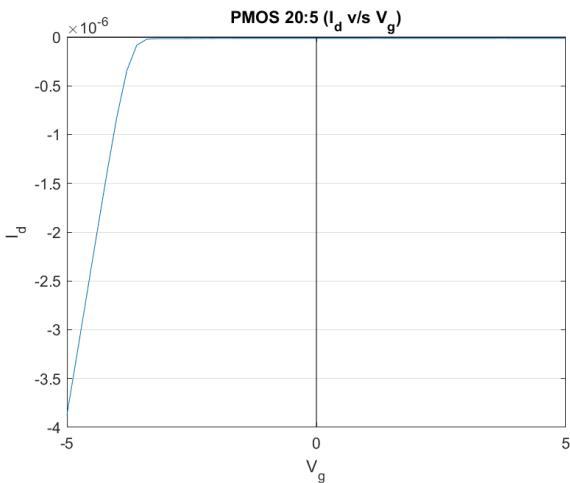


Figure 48: I_D vs V_G for transistor dimensions 20:5 (width:length) in V_T -adjust of 0 ions/cm² doping quadrant

I_D vs V_G in V_T -adjust of 3E11 ions/cm² doping quadrant

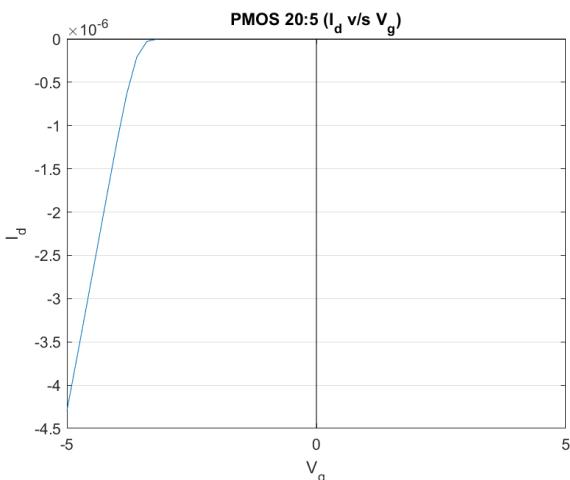


Figure 49: I_D vs V_G for transistor dimensions 20:5 (width:length) in V_T -adjust of 3E11 ions/cm² doping quadrant

I_D vs V_G in V_T -adjust of 6E11 ions/cm² doping quadrant

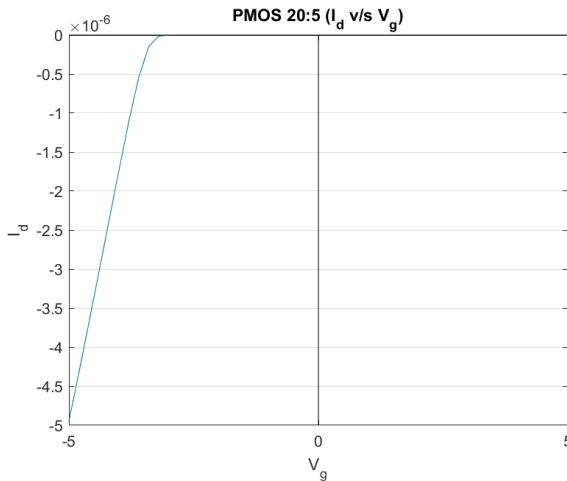


Figure 50: I_D vs V_G for transistor dimensions 20:5 (width:length) in V_T -adjust of $6\text{E}11 \text{ ions/cm}^2$ doping quadrant

PMOS Doping (ions/cm ²)	V_{th} (V)
0e11	-3.5
3e11	-3.4
6e11	-3.2
9e11	-3

Table 8: V_{th} for different PMOS doping levels for 20:5 W/L

The calculated hole mobilities for different doping levels of PMOS transistors are given in the table below:

PMOS Doping (ions/cm ³)	Hole Mobility (μ_p)
0E11	172
3E11	224
6E11	231
9E11	231

Table 9: Hole Mobility for different PMOS doping levels at 20:5 transistor size

I_D vs V_{DS} in V_T -adjust of $9\text{E}11 \text{ ions/cm}^2$ doping quadrant

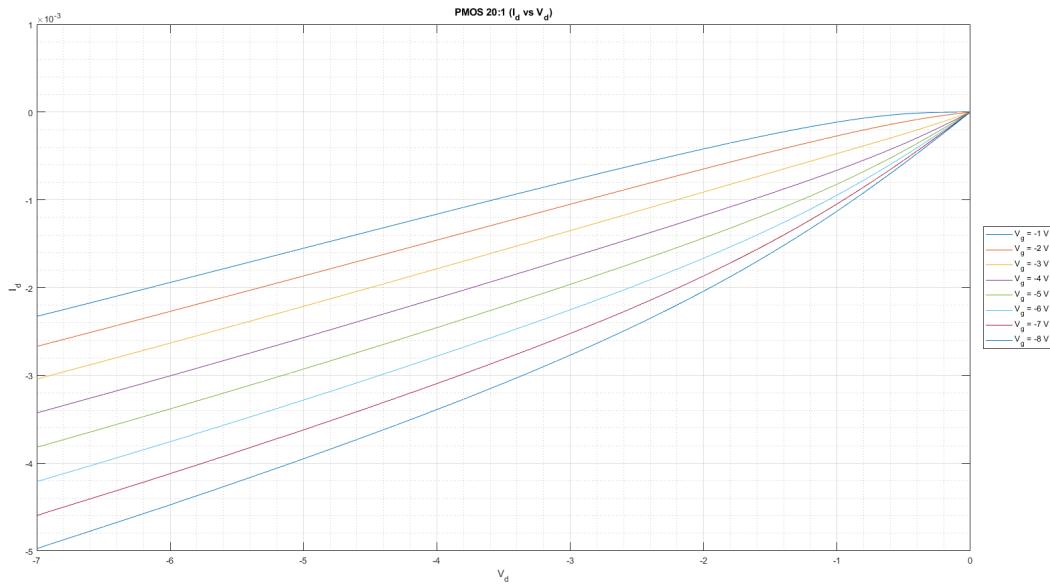


Figure 51: I_D vs V_{DS} for different gate voltages (-1V to -8V) for transistor dimension 20:1 (width:length) in V_T -adjust of 9E11 ions/cm² doping quadrant

I_D vs V_{DS} in V_T -adjust of 9E11 ions/cm² doping quadrant

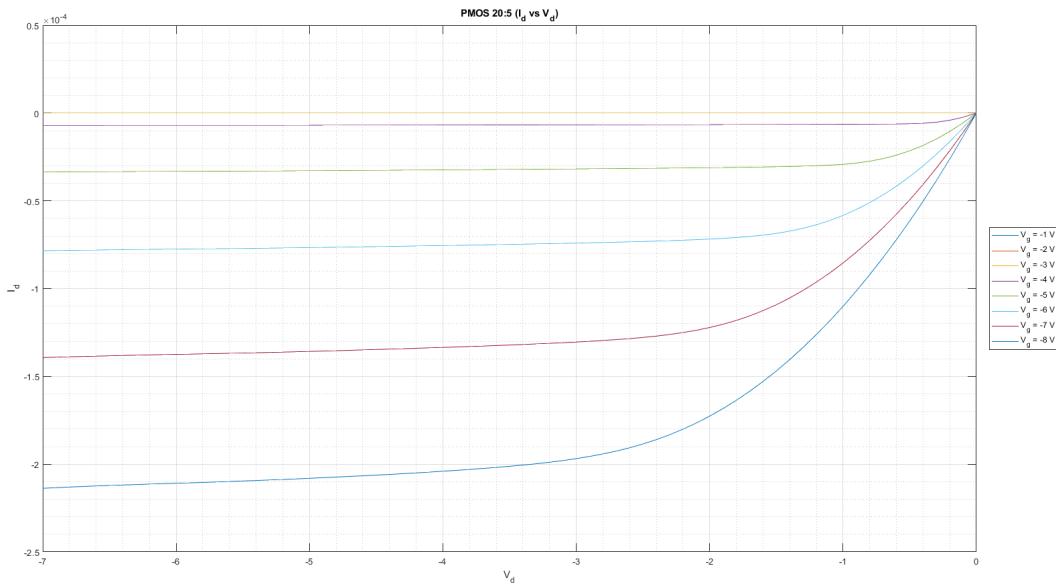


Figure 52: I_D vs V_{DS} for different gate voltages (-1V to -8V) for transistor dimension 20:5 (width:length) in V_T -adjust of 9E11 ions/cm² doping quadrant

The plot curves for 20:1 and 20:5 are different because the W/L of the transistors are different and the drain current is directly proportional to the W/L ratio.

6.3.2 NMOS Measurements

I_D vs V_G in V_T -adjust of $9E11$ ions/ cm^2 doping quadrant

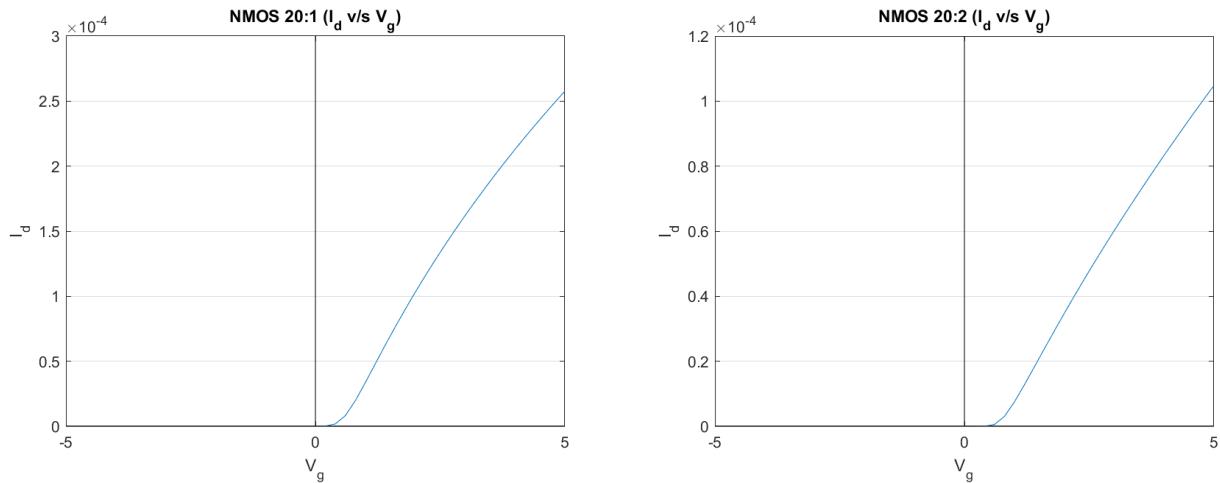


Figure 53: I_D vs V_G for transistor dimensions 20:1 and 20:2 (width:length) in V_T -adjust of $9E11$ ions/ cm^2 doping quadrant

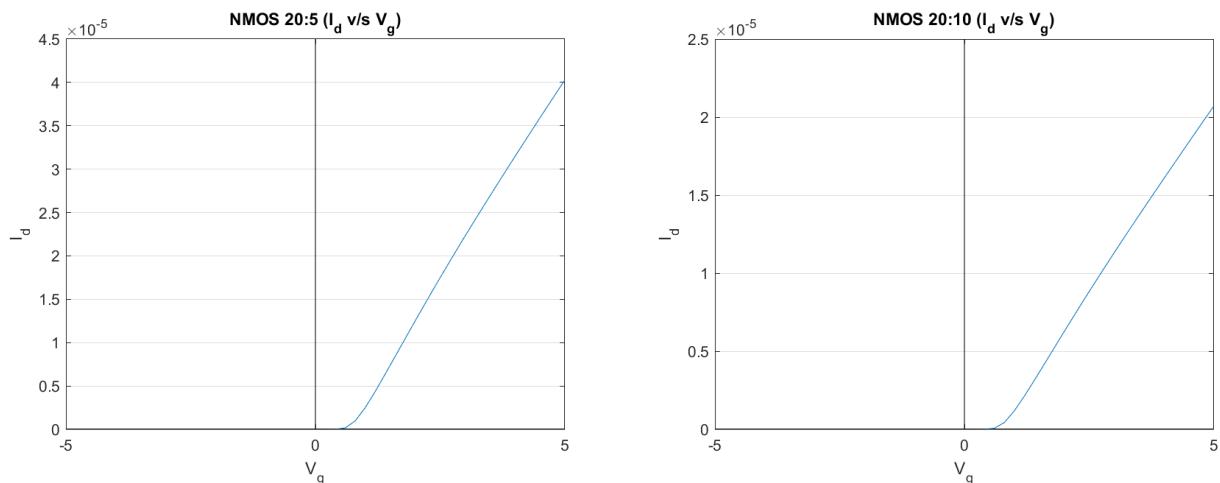


Figure 54: I_D vs V_G for transistor dimensions 20:5 and 20:10 (width:length) in V_T -adjust of $9E11$ ions/ cm^2 doping quadrant

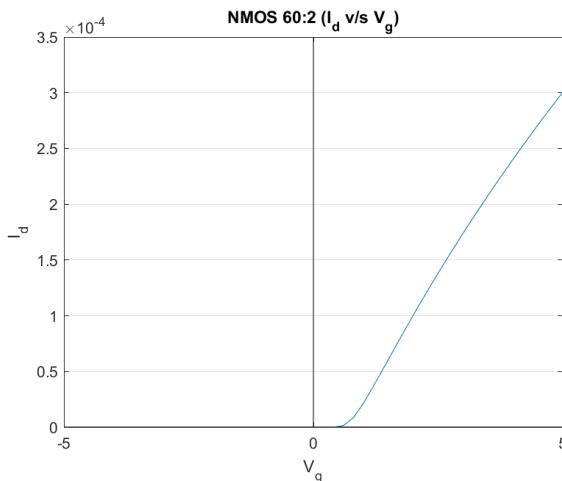


Figure 55: I_D vs V_G for transistor dimensions 60:2 (width:length) in V_T -adjust of 9E11 ions/cm² doping quadrant

W/L ratio directly affects the drain current I_D .

NMOS transistor W/L ratio	V_{th} (V)
20:1	0.2
20:2	0.8
20:5	0.8
20:10	0.8
60:2	0.8

Table 10: V_{th} for different NMOS transistor sizes

The threshold voltages for different NMOS transistor dimension is show in table 10.

I_D vs V_G in V_T -adjust of 0 ions/cm² doping quadrant

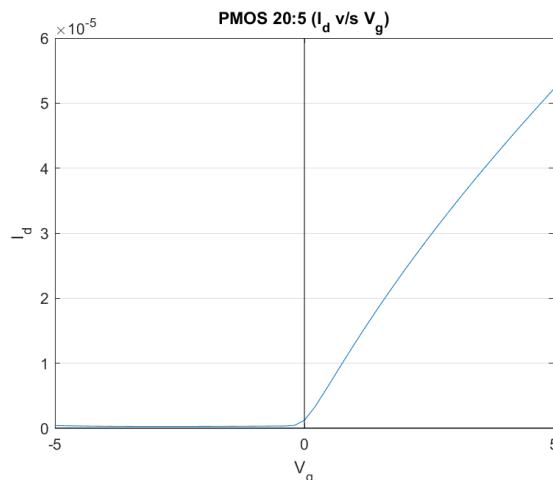


Figure 56: I_D vs V_G for transistor dimensions 20:5 (width:length) in V_T -adjust of 0 ions/cm² doping quadrant

I_D vs V_G in V_T-adjust of 3E11 ions/cm² doping quadrant

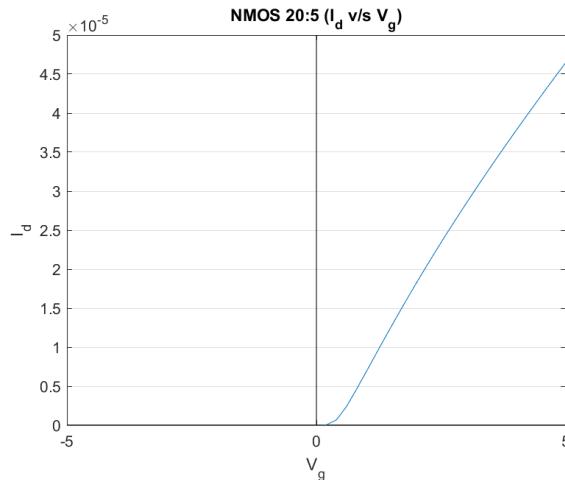


Figure 57: I_D vs V_G for transistor dimensions 20:5 (width:length) in V_T-adjust of 3E11 ions/cm² doping quadrant

I_D vs V_G in V_T-adjust of 6E11 ions/cm² doping quadrant

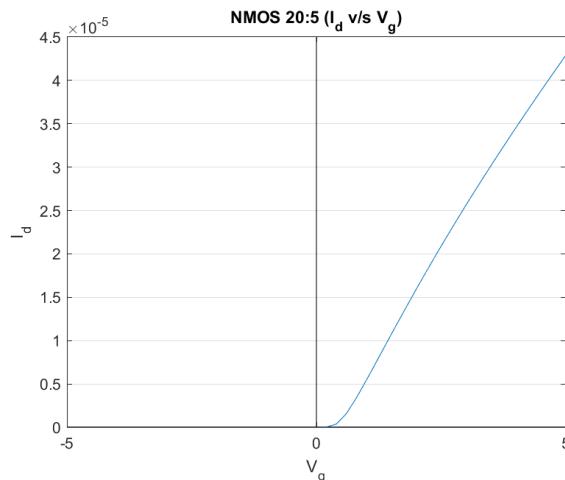


Figure 58: I_D vs V_G for transistor dimensions 20:5 (width:length) in V_T-adjust of 6E11 ions/cm² doping quadrant

NMOS Doping (ions/cm ²)	V _{th} (V)
0e11	-0.2
3e11	0.2
6e11	0.4
9e11	0.8

Table 11: V_{th} for different NMOS doping levels for 20:5 W/L

I_D vs V_{DS} in V_T-adjust of 9E11 ions/cm² doping quadrant

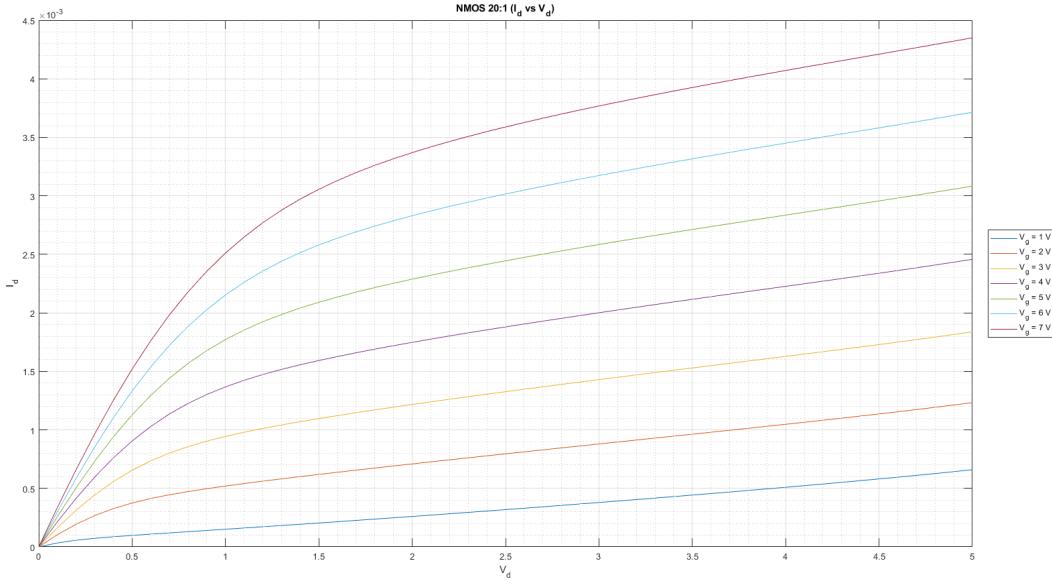


Figure 59: I_D vs V_{DS} for different gate voltages (1V to 7V) for transistor dimension 20:1 (width:length) in V_T -adjust of 9E11 ions/cm² doping quadrant

I_D vs V_{DS} in V_T -adjust of 9E11 ions/cm² doping quadrant

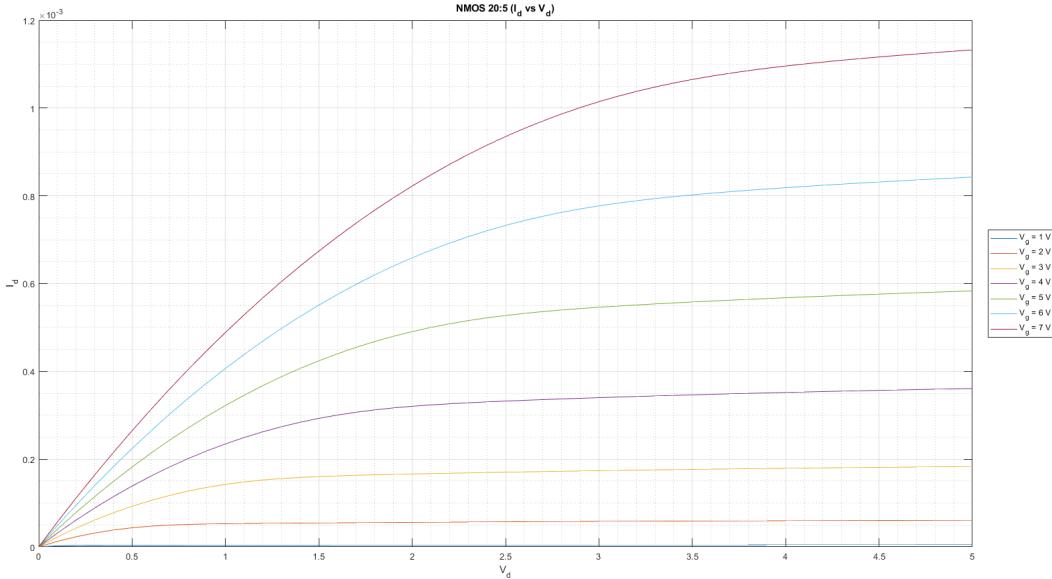


Figure 60: I_D vs V_{DS} for different gate voltages (1V to 7V) for transistor dimension 20:5 (width:length) in V_T -adjust of 9E11 ions/cm² doping quadrant

If we compare the I_d - V_{ds} characteristics of NMOS and PMOS, we observe that PMOS lines are more flat. Furthermore, since the mobility of PMOS is less, less current I_d will flow for the same sizes compared to NMOS.