MikroLeo Instruction Set

Instruction Hex Code	Encoding of MikroLeo Instruction Word (16-bits)						Mnemonic	Instructions with all possibilities	Operation	Affected Flags
	ROMH (8-bit)				ROML (8-bit)					
	High Nibble (HiNB)			Decoder Address	MAddr	Operand/LAddr				
ROM (16-bit)	MICRO2_IN	AMODE	MOD	MICRO						
	b15	b14	b13:b12	b11:b8	b7:b4	b3:b0				
00Xn	0	X	0	0	X	n	LDI	LDI ACC,n	ACC ← n	ZF
10Xn			1					LDI RA,n	RA ← n	-
20Xn			2					LDI RB,n	RB ← n	
30Xn			3					LDI RC,n	RC ← n	
01Xn			0	1	X	n	NAND	NAND ACC,n	ACC ← ACC NAND n	ZF
11XX			1			X		NAND ACC,RA	ACC ← ACC NAND RA	
21XX			2					NAND ACC,RB	ACC ← ACC NAND RB	
31mn		0	3		MAddr	LAddr		NAND ACC,RAM[Addr]	ACC ← ACC NAND RAM[RC:MAddr:LAddr]	
71XX		1			X	X			ACC ← ACC NAND RAM[RC:RB:RA]	
02mn		0	0	2	MAddr	LAddr	LDW	LDW ACC,RAM[Addr]	ACC ← RAM[RC:MAddr:LAddr]	ZF
42XX		1			X	X			ACC ← RAM[RC:RB:RA]	
13XX		X	1	3	X	X	LDA	LDA RA	ACC ← RA	ZF
23XX			2					LDA RB	ACC ← RB	
33XX			3					LDA RC	ACC ← RC	
04Xn			0	4	X	n	OUTA	OUTA n	OUTA ← n	-
14XX			1			X		OUTA ACC	OUTA ← ACC	
24XX			2					OUTA RA	OUTA ← RA	
34mn		0	3		MAddr	LAddr		OUTA RAM[Addr]	OUTA ← RAM[RC:MAddr:LAddr]	
74XX		1			X	X			OUTA ← RAM[RC:RB:RA]	
05Xn		X	0	5	X	n	OUTB	OUTB n	OUTB ← n	-
15XX			1			X		OUTB ACC	OUTB ← ACC	
25XX			2					OUTB RA	OUTB ← RA	
35mn		0	3		MAddr	LAddr		OUTB RAM[Addr]	OUTB ← RAM[RC:MAddr:LAddr]	
75XX		1			X	X			OUTB ← RAM[RC:RB:RA]	
06Xn		X	0	6	X	n	OUTC	OUTC n	OUTC ← n	-
16XX			1			X		OUTC ACC	OUTC ← ACC	
26XX			2					OUTC RA	OUTC ← RA	
36mn		0	3		MAddr	LAddr		OUTC RAM[Addr]	OUTC ← RAM[RC:MAddr:LAddr]	
76XX		1			X	X			OUTC ← RAM[RC:RB:RA]	
07XX		X	0	7	X	X	NOP	NOP	No Operation	-
17XX			1		X	X	LDR	LDR RA	RA ← ACC	-
27XX			2					LDR RB	RB ← ACC	
37XX			3					LDR RC	RC ← ACC	
08Xn			0	8	X	n	CMP	CMP ACC,n	ACC - n	CF, ZF
18XX			1			X		CMP ACC,RA	ACC - RA	
28XX			2					CMP ACC,RB	ACC - RB	
38mn		0	3		MAddr	LAddr		CMP ACC,RAM[Addr]	ACC - RAM[RC:MAddr:LAddr]	
78XX		1			X	X			ACC - RAM[RC:RB:RA]	
09Xn		X	0	9	X	n	OUTD	OUTD n	OUTD ← n	-
19XX			1			X		OUTD ACC	OUTD ← ACC	
29XX			2					OUTD RA	OUTD ← RA	
39mn		0	3		MAddr	LAddr		OUTD RAM[Addr]	OUTD ← RAM[RC:MAddr:LAddr]	
79XX		1							OUTD ← RAM[RC:RB:RA]	
0Amn		0	0	Ah	MAddr	LAddr	STW	STW RAM[Addr],ACC	RAM[RC:MAddr:LAddr] ← ACC	-
4AXX		1			X	X			RAM[RC:RB:RA] ← ACC	
0BXn		X	0	Bh	X	n	SUB	SUB ACC,n	ACC ← ACC - n	CF, ZF
1BXX			1			X		SUB ACC,RA	ACC ← ACC - RA	
2BXX			2					SUB ACC,RB	ACC ← ACC - RB	
3Bmn		0	3		MAddr	LAddr		SUB ACC,RAM[Addr]	ACC ← ACC - RAM[RC:MAddr:LAddr]	
7BXX		1			X	X			ACC ← ACC - RAM[RC:RB:RA]	
0Cmn		0	0	Ch	MAddr	LAddr	JPI	JPI RC:MA[7:4]:LA[3:0]	PC ← [RC:MAddr:LAddr]	-
4CXX		1			X	X			PC ← [RC:RB:RA]	
0Dmn		0	0	Dh	MAddr	LAddr	JPC	JPC MA[7:4]:LA[3:0]	If CF=1, PC ← [PCH:MAddr:LAddr]	
4DXX		1			X	X			If CF=1, PC ← [PCH:RB:RA]	
0Emn		0	0	Eh	MAddr	LAddr	JPZ	JPZ MA[7:4]:LA[3:0]	If ZF=1, PC ← [PCH:MAddr:LAddr]	
4EXX		1			X	X			If ZF=1, PC ← [PCH:RB:RA]	
0FXn		X	0	Fh	X	n	ADD	ADD ACC,n	ACC ← ACC + n	CF, ZF
1FXX			1			X		ADD ACC,RA	ACC ← ACC + RA	
2FXX			2					ADD ACC,RB	ACC ← ACC + RB	
3Fmn		0	3		MAddr	LAddr		ADD ACC,RAM[Addr]	ACC ← ACC + RAM[RC:MAddr:LAddr]	
7FXX		1			X	X			ACC ← ACC + RAM[RC:RB:RA]	
8XXX	1	X	0	X			INA	INA	ACC ← INA	ZF
9XXX			1				INB	INB	ACC ← INB	
AXXX			2				INC	INC	ACC ← INC	
BXXX			3				IND	IND	ACC ← IND	

LA[3:0] => can be RA or Operand (LAddr), depends on the AMODE bit.
MA[7:4] => can be RB or MAddr, depends on the AMODE bit.
Address = Addr => RC:MA[7:4]:LA[3:0]
If AMODE=0, Addr=RC:Maddr:LAddr
If AMODE=1, Addr=RC:RB:RA
X = don't care
MAddr = m, so the names are interchangeable
Operand = n, so the names are interchangeable

AMODE = Addresing mode (b14)
MOD = Modifier bits (b13:b12)
MAddr = Medium Address (b7:b4)
LAddr = Low Address (b3:b0)
MICRO = Instruction (b11:b8)
OPCODE = AMODE:MOD:MICRO
ZF = Zero Flag
CF = Carry Flag