

RTL design using Verilog with SKY130 Technology Workshop Certificate

{26-30 May 2021}

Hríshíkesh Prabhu

has successfully completed

an online cloud based 5 day workshop conducted on $\mathcal{VSD} ext{-}\mathit{IAT}$

| Lab Skills Activities | 115/116 |
|-----------------------|------------------------------|
| Github Repo Link | https://github.com/embedded- |
| | explorer/Open-Source-RTL- |
| | Design |
| % of Completion | 100 |

Hofred.

Kunal Ghosh

(Design & Sign-off Expertise, Founder VLSI System Design)