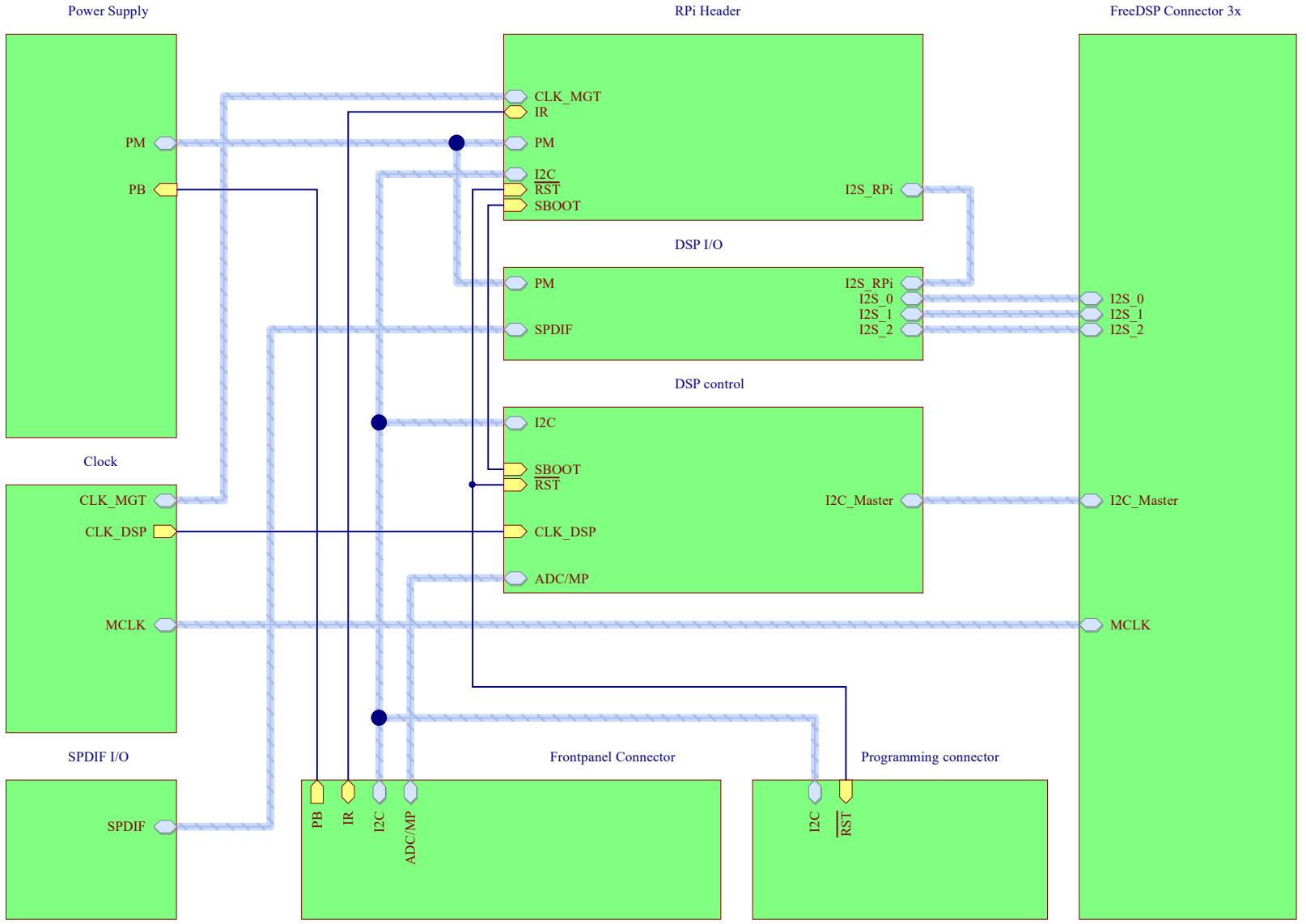

Sheet Title: Top Sheet	**Board Revision:** B2
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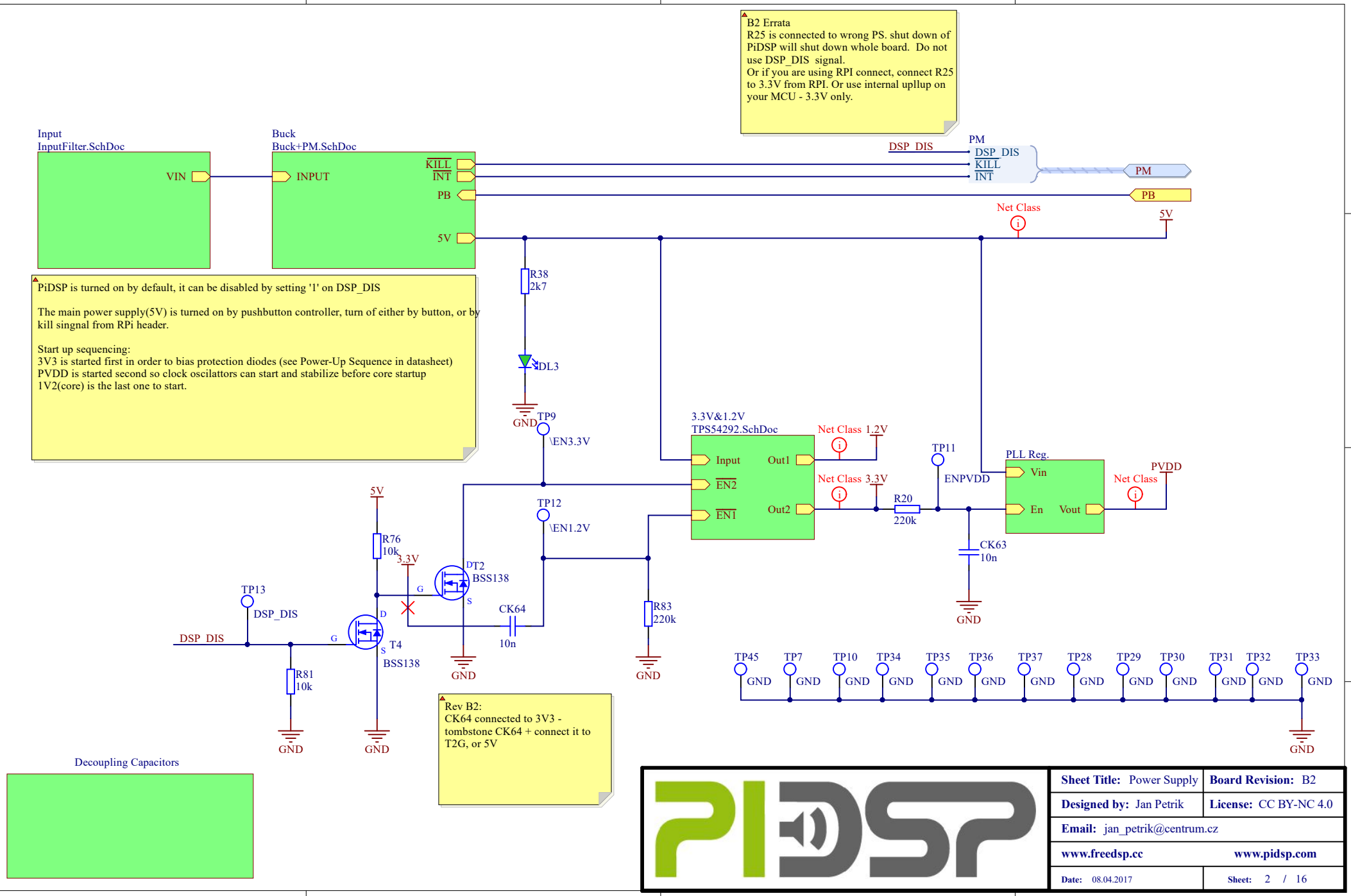
Date: 08.04.2017	**Sheet:** 1 / 16


B2 Errata
R25 is connected to wrong PS. shut down of PiDSP will shut down whole board. Do not use DSP_DIS signal.
Or if you are using RPI connect, connect R25 to 3.3V from RPI. Or use internal upllup on your MCU - 3.3V only.
Input
InputFilter.SchDoc
VIN
Buck
Buck+PM.SchDoc
INPUT
KILL
INT
PB
5V
DSP_DIS
PM
DSP_DIS
KILL
INT
PM
PB
Net Class
5V
PiDSP is turned on by default, it can be disabled by setting '1' on DSP_DIS
The main power supply(5V) is turned on by pushbutton controller, turn of either by button, or by kill singnal from RPi header.
Start up sequencing:
3V3 is started first in order to bias protection diodes (see Power-Up Sequence in datasheet)
PVDD is started second so clock oscilattors can start and stabilize before core startup
1V2(core) is the last one to start.
R38
2k7
DL3
GND
TP9
\EN3.3V
3.3V&1.2V
TPS54292.SchDoc
Input
Out1
EN2
EN1
Out2
Net Class 1.2V
Net Class 3.3V
TP11
ENPVDD
R20
220k
PLL Reg.
Vin
En
Vout
Net Class
PVDD
CK63
10n
GND
5V
R76
10k
3.3V
TP12
\EN1.2V
DT2
BSS138
G
S
D
TP13
DSP_DIS
DSP_DIS
G
T4
BSS138
S
CK64
10n
R83
220k
R81
10k
GND
GND
GND
TP45
TP7
TP10
TP34
TP35
TP36
TP37
TP28
TP29
TP30
TP31
TP32
TP33
Rev B2:
CK64 connected to 3V3 - tombstone CK64 + connect it to T2G, or 5V
Decoupling Capacitors
Sheet Title: Power Supply
Board Revision: B2
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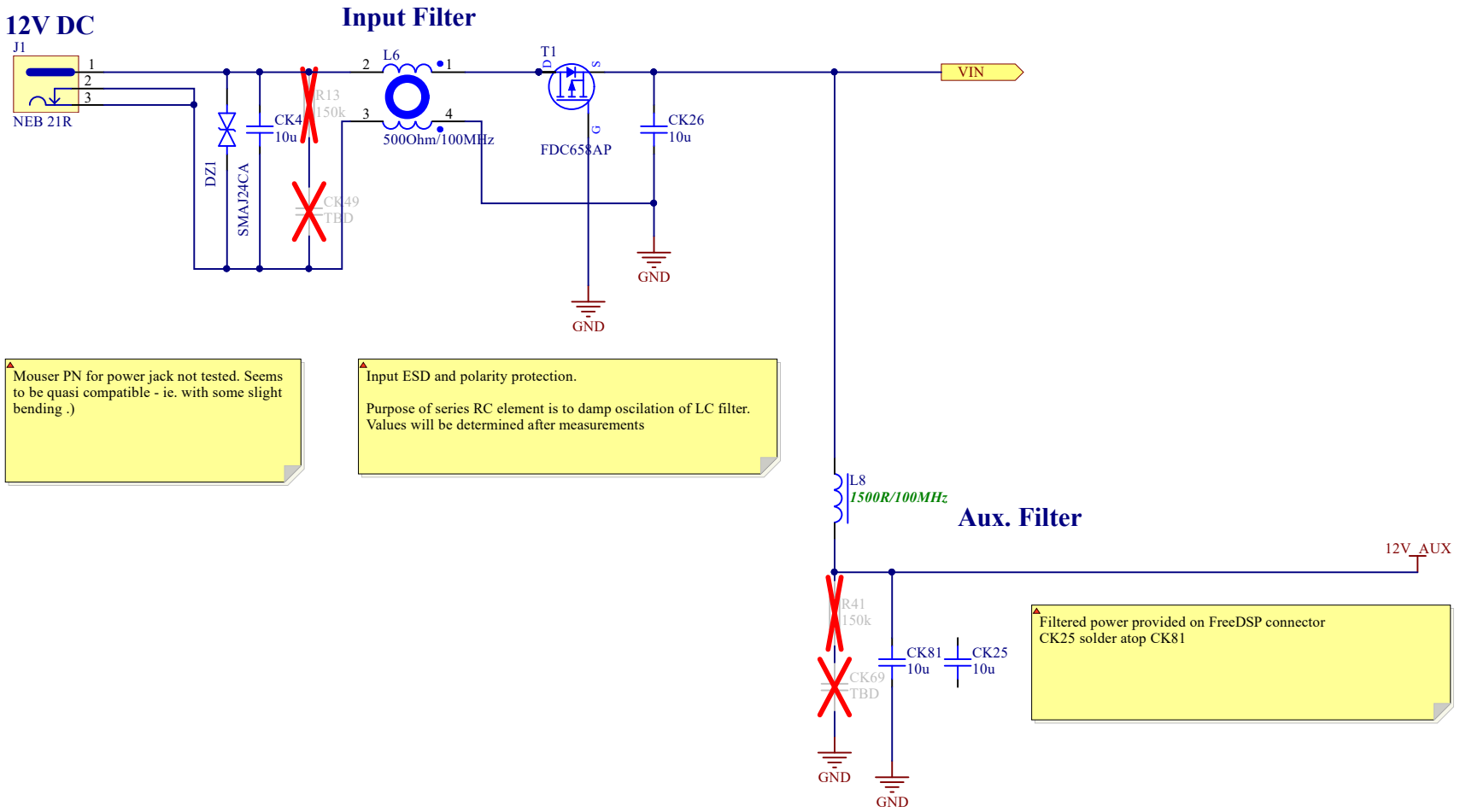

Sheet Title: Input Filter	**Board Revision:** B2
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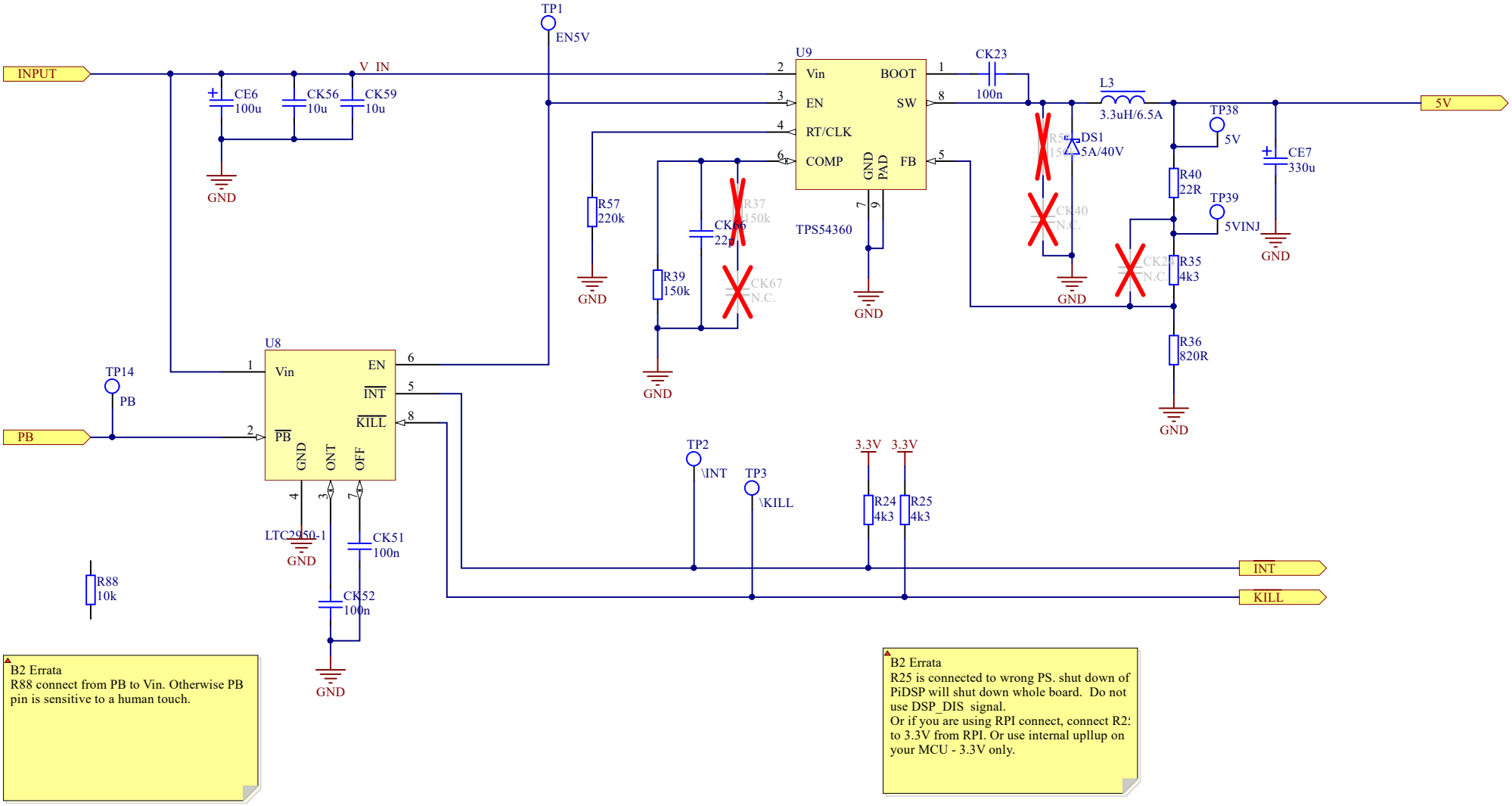

Sheet Title: 5V Regulator	**Board Revision:** B2
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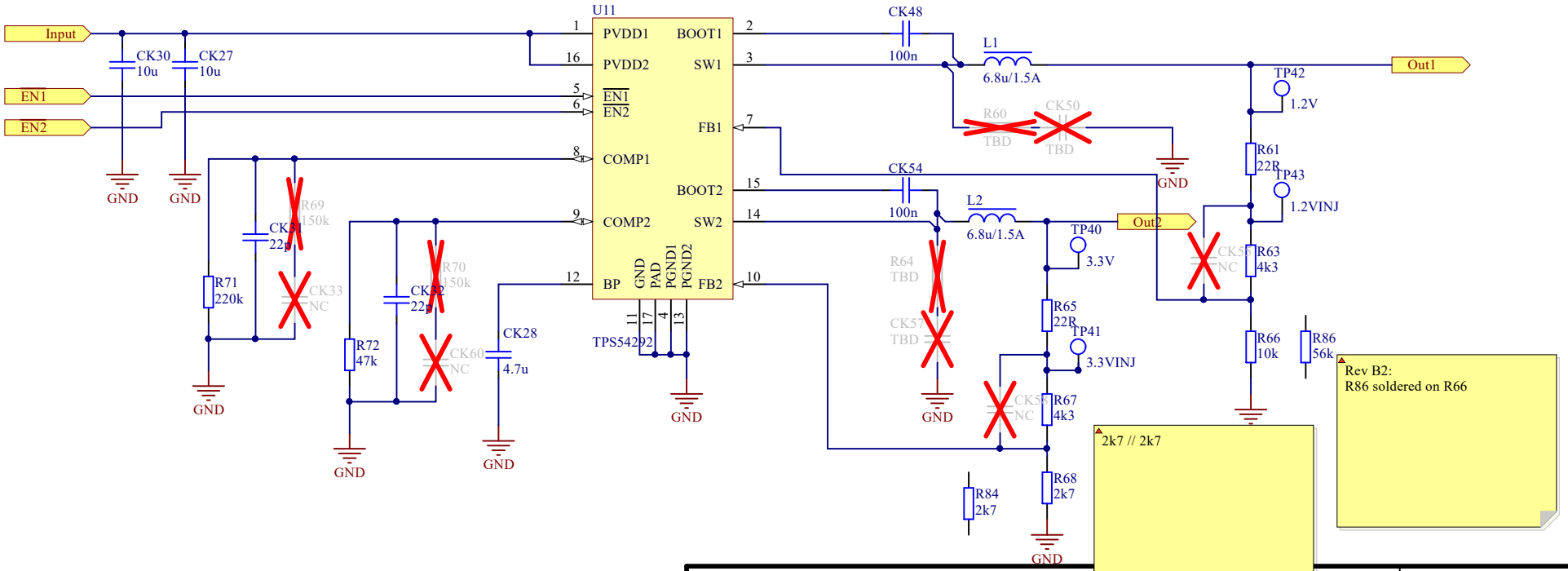
3.3V and 1.2V Regulator

3.3V - IOVDD + general use. Output is aviable on front panel connector.
1.2V - ADAU core
Powered from 5V



3V+1.2V	**Board Revision:** B2
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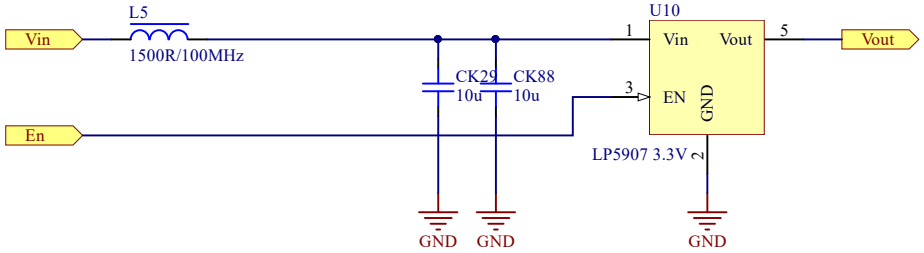
3.3V PVDD Regulator

Low noise regulator provides 3.3V for oscillators and AVDD and PVDD of ADAU1452.
Powered from 5V rail.



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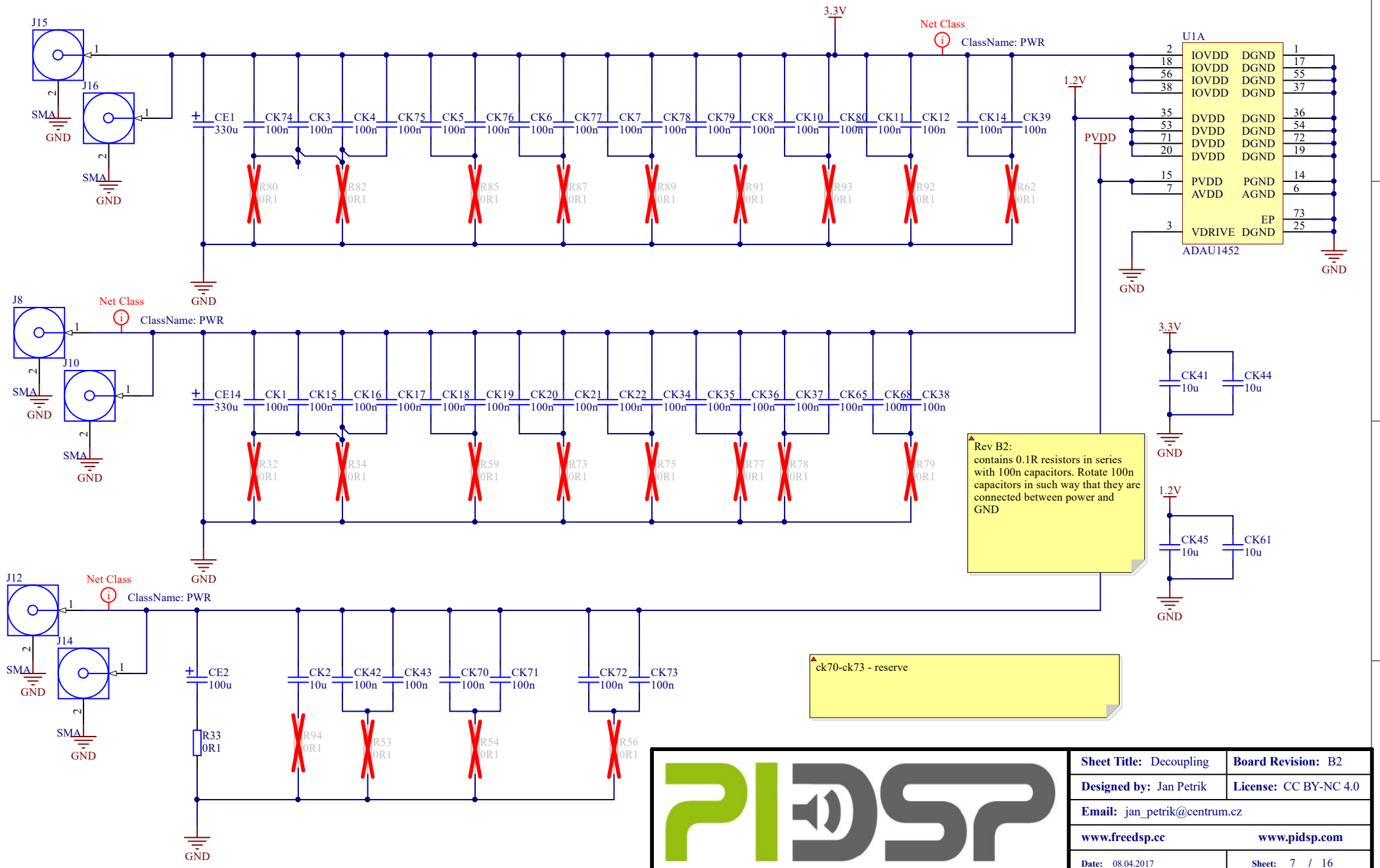
J15
J16
SMA
GND
CE1
330u
CK74
CK3
CK4
CK75
CK5
CK76
CK6
CK77
CK7
CK78
CK79
CK8
CK10
CK80
CK11
CK12
CK14
CK39
100n
R80
R82
R85
R87
R89
R91
R93
R92
R62
0R1
3.3V
Net Class
ClassName: PWR
1.2V
PVDD
U1A
IOVDD
DVDD
PVDD
AVDD
DGND
PGND
AGND
EP
VDRIVE
ADAU1452
J8
J10
CE14
CK1
CK15
CK16
CK17
CK18
CK19
CK20
CK21
CK22
CK34
CK35
CK36
CK37
CK65
CK68
CK38
R32
R34
R59
R73
R75
R77
R78
R79
CK41
CK44
10u
CK45
CK61
Rev B2:
contains 0.1R resistors in series with 100n capacitors. Rotate 100n capacitors in such way that they are connected between power and GND
J12
J14
CE2
100u
CK2
CK42
CK43
CK70
CK71
CK72
CK73
R33
R94
R53
R54
R56
ck70-ck73 - reserve
PIDSP
Sheet Title: Decoupling
Board Revision: B2
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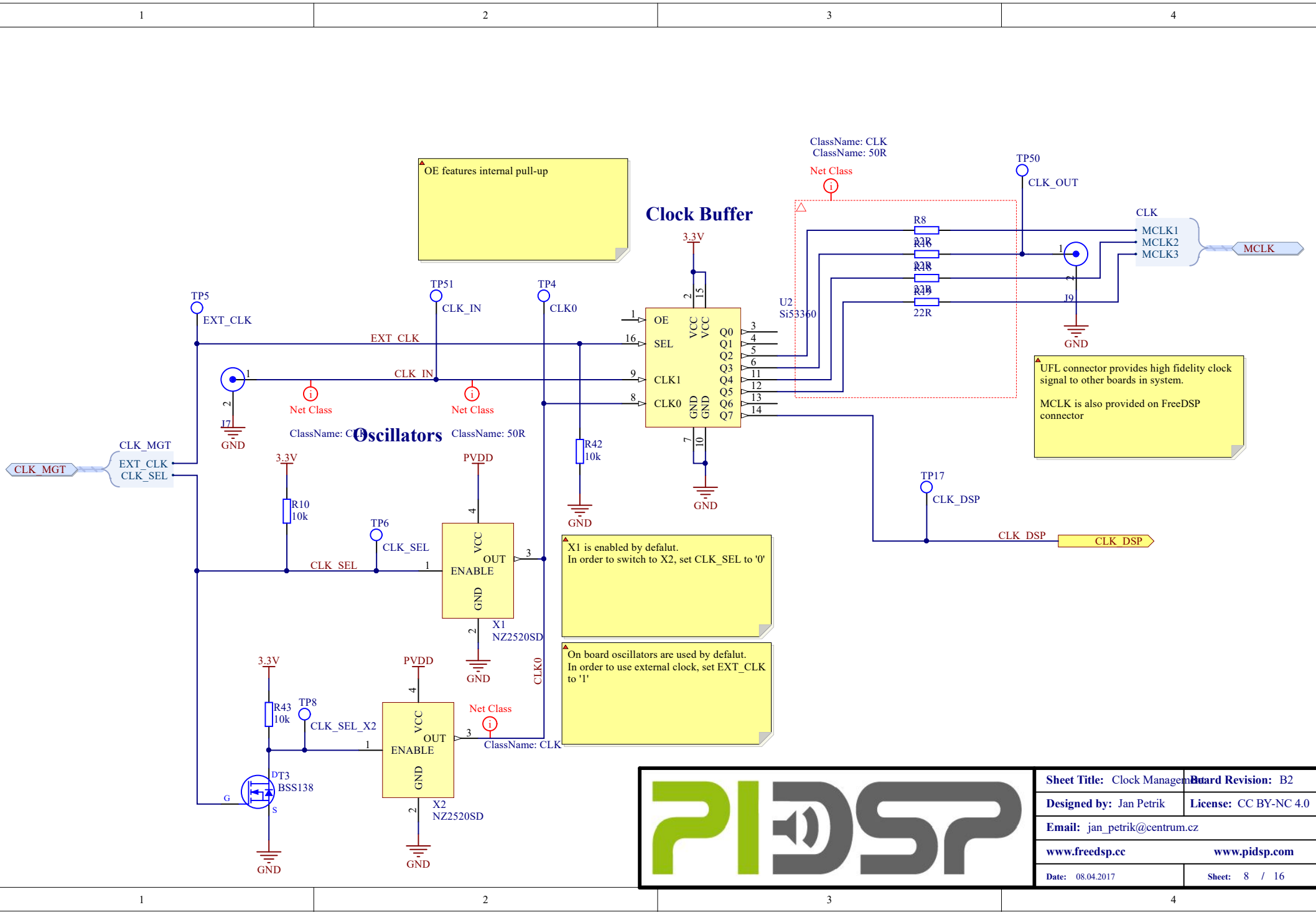
Clock Buffer
Oscillators
OE features internal pull-up
ClassName: CLK
ClassName: 50R
Net Class
TP50
CLK_OUT
CLK
MCLK1
MCLK2
MCLK3
MCLK
R8
22R
R16
22R
R18
22R
R19
22R
U2
Si53360
OE
SEL
CLK1
CLK0
VCC
GND
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
J9
GND
UFL connector provides high fidelity clock signal to other boards in system.
MCLK is also provided on FreeDSP connector
TP5
EXT_CLK
TP51
CLK_IN
TP4
CLK0
J7
Net Class
ClassName: CLK
ClassName: 50R
3.3V
R42
10k
CLK_MGT
EXT_CLK
CLK_SEL
R10
10k
PVDD
TP6
CLK_SEL
TP17
CLK_DSP
X1 is enabled by defalut.
In order to switch to X2, set CLK_SEL to '0'
X1
NZ2520SD
On board oscillators are used by defalut.
In order to use external clock, set EXT_CLK to '1'
R43
10k
TP8
CLK_SEL_X2
DT3
BSS138
G
S
X2
NZ2520SD
Sheet Title: Clock Management
Board Revision: B2
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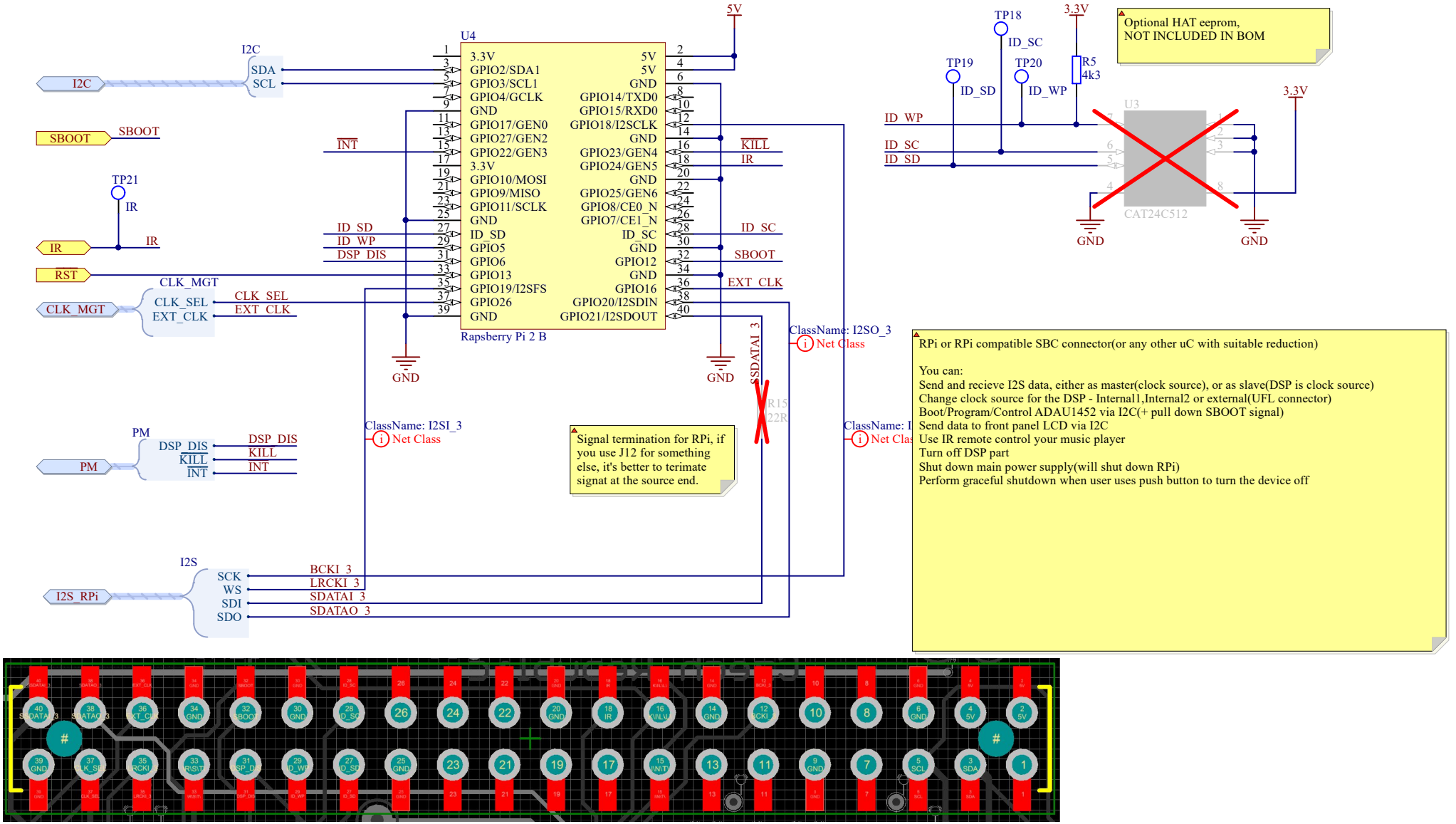

Sheet Title: RPi	**Board Revision:** B2
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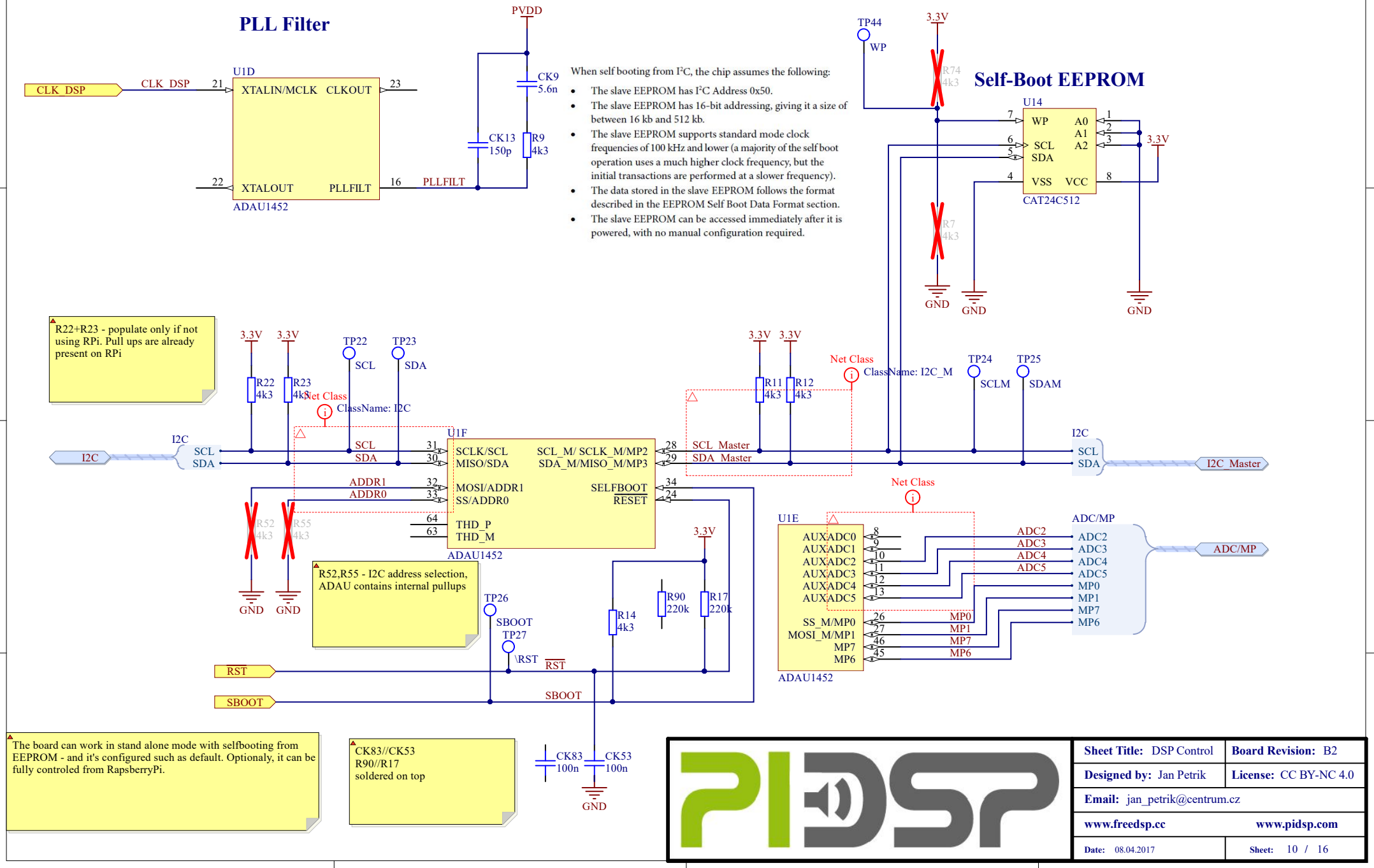
PLL Filter
PVDD
CLK_DSP
CLK_DSP
U1D
XTALIN/MCLK
CLKOUT
XTALOUT
PLLFILT
ADAU1452
CK9
5.6n
CK13
150p
R9
4k3
PLLFILT
When self booting from I²C, the chip assumes the following:
The slave EEPROM has I²C Address 0x50.
The slave EEPROM has 16-bit addressing, giving it a size of between 16 kb and 512 kb.
The slave EEPROM supports standard mode clock frequencies of 100 kHz and lower (a majority of the self boot operation uses a much higher clock frequency, but the initial transactions are performed at a slower frequency).
The data stored in the slave EEPROM follows the format described in the EEPROM Self Boot Data Format section.
The slave EEPROM can be accessed immediately after it is powered, with no manual configuration required.
Self-Boot EEPROM
TP44
WP
3.3V
R74
4k3
U14
WP
SCL
SDA
VSS
A0
A1
A2
VCC
CAT24C512
R7
4k3
GND
R22+R23 - populate only if not using RPi. Pull ups are already present on RPi
R22
4k3
R23
4k3
TP22
SCL
TP23
SDA
Net Class
ClassName: I2C
I2C
U1F
SCLK/SCL
MISO/SDA
MOSI/ADDR1
SS/ADDR0
THD_P
THD_M
SCL_M/ SCLK_M/MP2
SDA_M/MISO_M/MP3
SELFBOOT
RESET
ADDR1
ADDR0
SCL_Master
SDA_Master
R11
4k3
R12
4k3
Net Class
ClassName: I2C_M
TP24
SCLM
TP25
SDAM
I2C_Master
R52
4k3
R55
4k3
R52,R55 - I2C address selection, ADAU contains internal pullups
TP26
SBOOT
TP27
\RST
R14
4k3
R90
220k
R17
220k
RST
SBOOT
U1E
AUXADC0
AUXADC1
AUXADC2
AUXADC3
AUXADC4
AUXADC5
SS_M/MP0
MOSI_M/MP1
MP7
MP6
ADAU1452
ADC2
ADC3
ADC4
ADC5
MP0
MP1
MP7
MP6
ADC/MP
The board can work in stand alone mode with selfbooting from EEPROM - and it's configured such as default. Optionaly, it can be fully controled from RapsberryPi.
CK83//CK53
R90//R17
soldered on top
CK83
100n
CK53
100n
PIDSP
Sheet Title: DSP Control
Board Revision: B2
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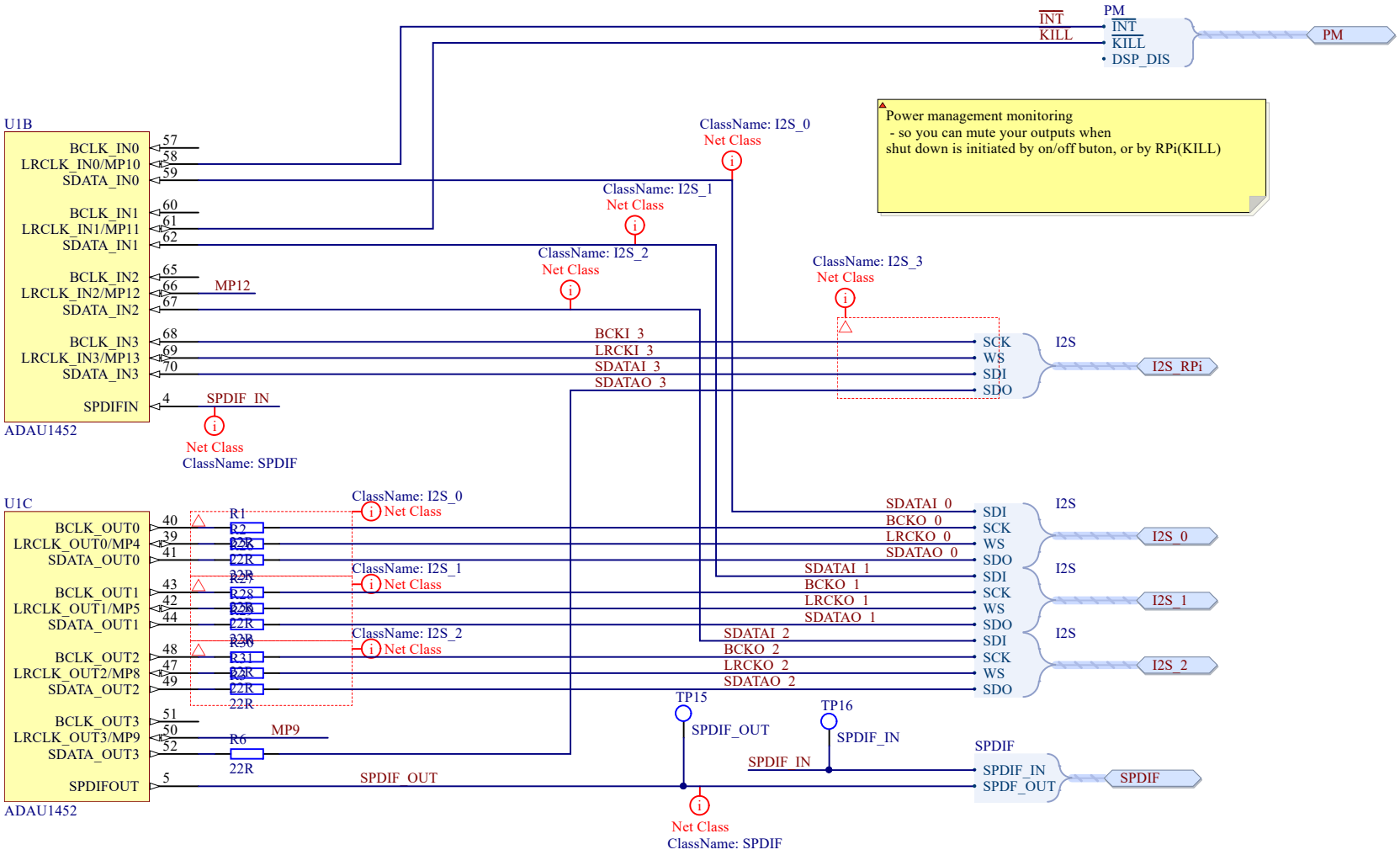

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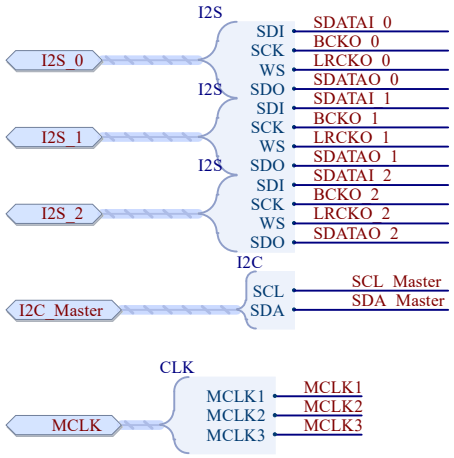
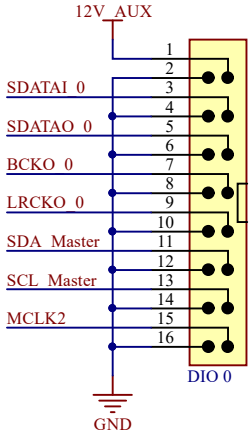
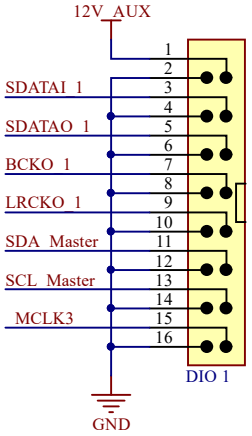


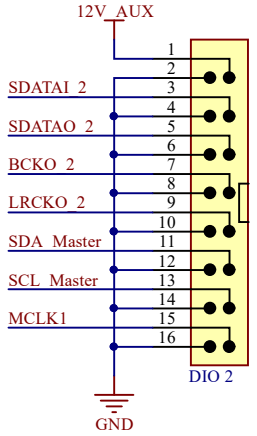
FreeDSP Connector 0



FreeDSP Connector 1



FreeDSP Connector 2



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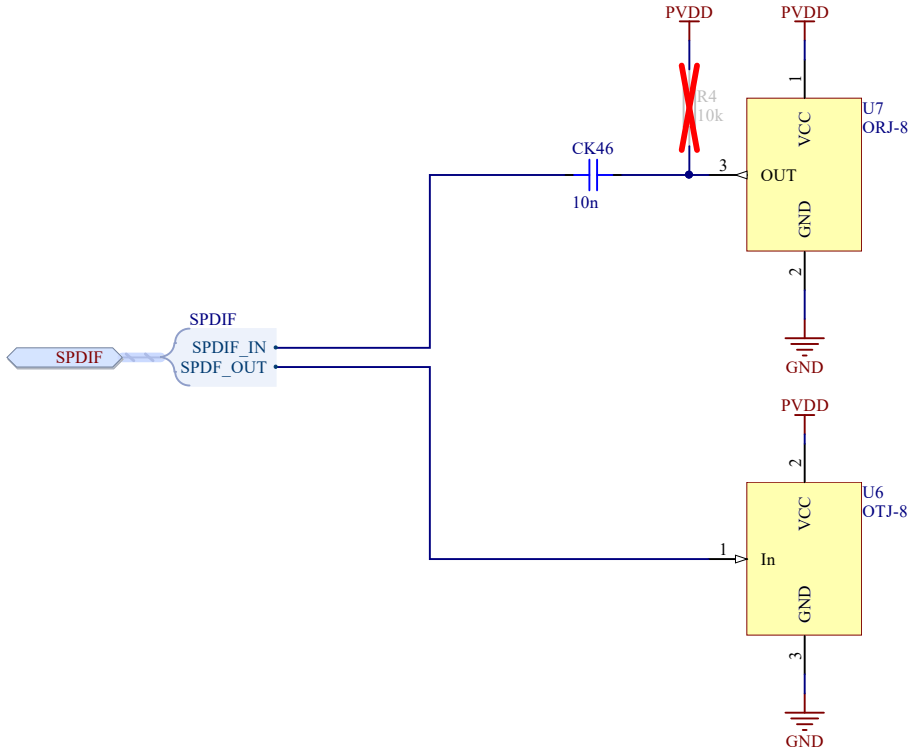
SPDIF I/O



SPDIF IN & OUT

Toslink optical connector - SPDIF input for PC,TV, gaming console etc. Stereo only. Input is fed through ASRC in ADAU.

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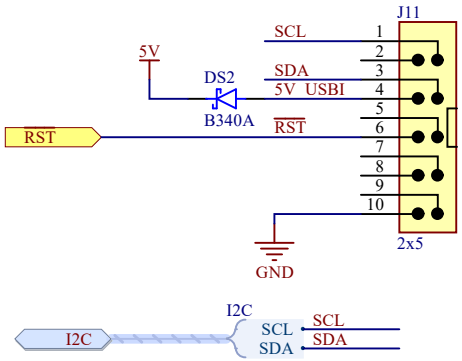
USBi connector



Programing connector for USBi

Use it to program your DSP. PiDSP can be powered from USBi.
Power is NOT provided to other modules connected via FreeDSP connector

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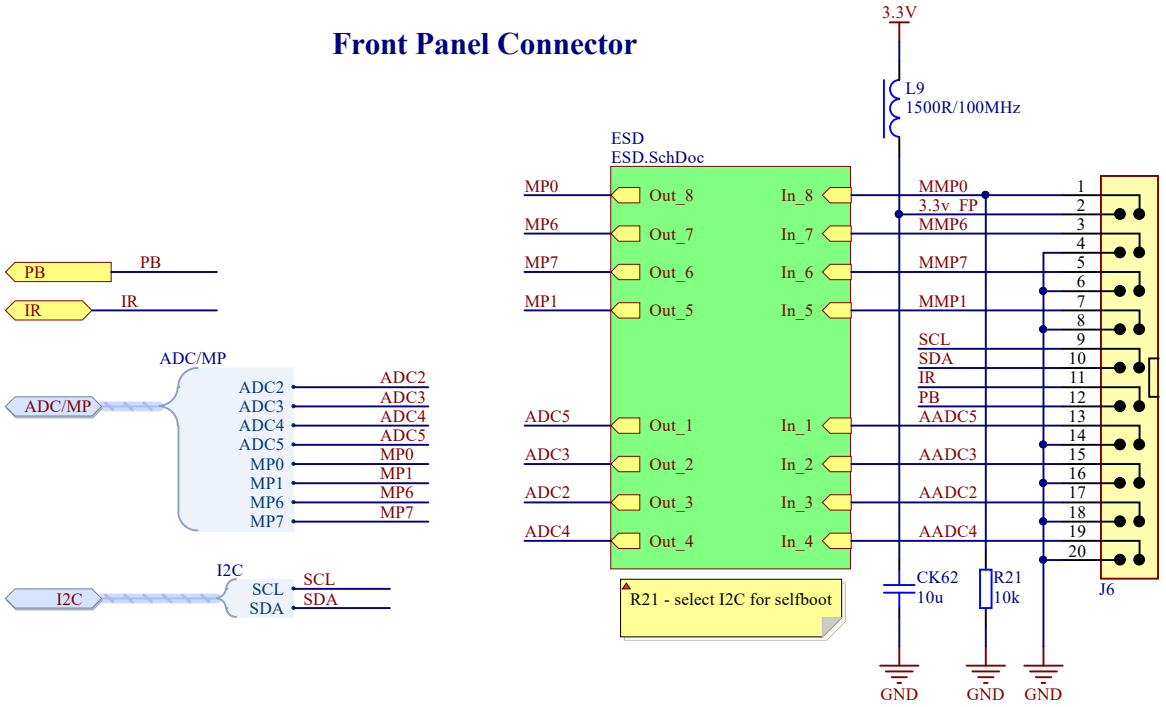
Front Panel Connector



Front Panel Connector

The connector contains:
4x GPIO from DSP - input selection, mute, general control
4x ADC from DSP - volume control, balance etc.
- both GPIO and ADC inputs are ESD protected, pcb footprint is extended so you can connect potentiometer directly into 3pin header. Push buttons can be connected directly aswell - you just need to enable pull-ups. With exception of MP0 - there is a pulldown for selfboot and pushbutton is connected 3.3V

1x On/Off pushbutton - connected to power management
1x GPIO from RPi - for IR control
1x I2C from RPi - front panel LCD/control of RPi

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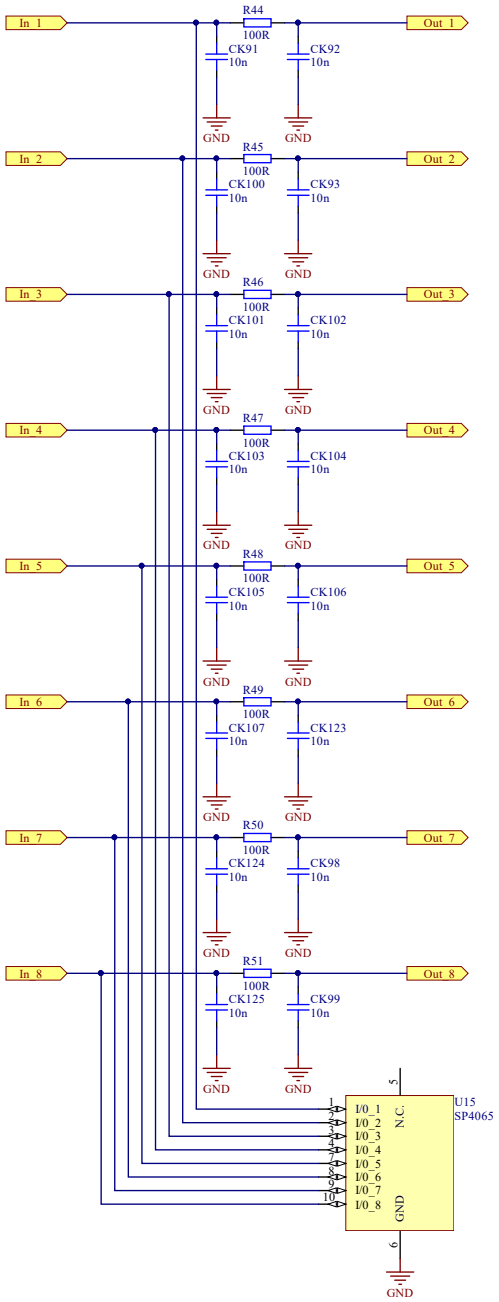
GPIO/ADC ESD Protection



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