2M ×8 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

• **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
KM48V2104A/AL/ALL/ASL-6	60ns	15ns	110ns	24ns
KM48V2104A/AL/ALL/ASL-7	70ns	20ns	130ns	29ns
KM48V2104A/AL/ALL/ASL-8	80ns	20ns	150ns	34ns

- **Fast Page Mode with Extended data out**
- **Self Refresh operation (LL-ver. only)**
- **Byte Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **LVTTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Single+3.3V ±0.3V power supply**
- **2048 cycles/32ms refresh (Normal)**
- **2048 cycles/128ms refresh (Low power & Self Ref.)**
- **2048 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II)**

GENERAL DESCRIPTION

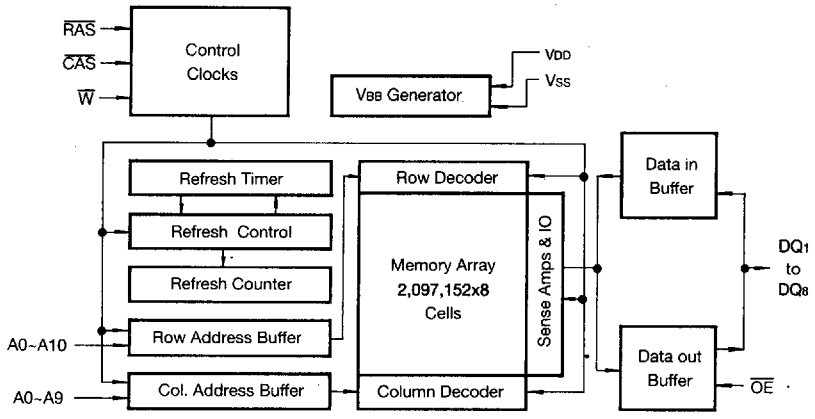
The Samsung KM48V2104A/AL/ALL/ASL is a high speed CMOS 2,097,152 bit × 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM48V2104A/AL/ALL/ASL features EDO Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM48V2104A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



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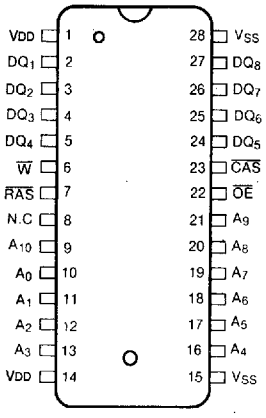
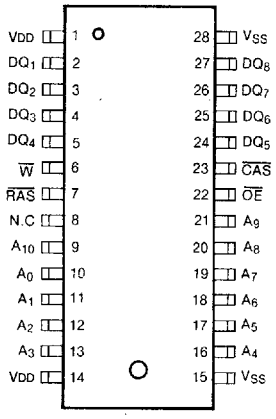
PIN CONFIGURATION (Top Views)

• KM48V2104 AJ/ALJ/ALLJ/ASLJ



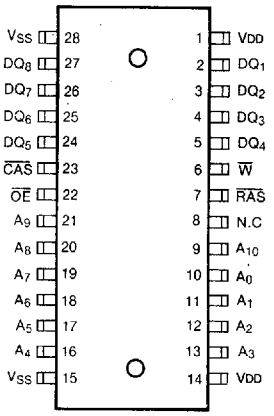
J : 400MIL

• KM48V2104 AT/ALT/ALLT/ASLT



T : 400MIL(Forward)

• KM48V2104 ATR/ALTR/ALLTR/ASLTR



TR : 400MIL(Reverse)

Pin Name	Pin Function
A0-A10	Address Inputs
DQ1~8	Data In/Out
VSS	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
VDD	Power(+3.3V)
N.C	No Connection

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5~ 4.6	V
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.5~ 4.6	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM48V2104A/AL/ALL/ASL-6	I_{CC1}	-	100	mA
	KM48V2104A/AL/ALL/ASL-7			90	mA
	KM48V2104A/AL/ALL/ASL-8			80	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM48V2104A	I_{CC2}	-	2	mA
	KM48V2104AL			1	mA
	KM48V2104ALL			1	mA
	KM48V2104ASL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM48V2104A/AL/ALL/ASL-6	I_{CC3}	-	100	mA
	KM48V2104A/AL/ALL/ASL-7			90	mA
	KM48V2104A/AL/ALL/ASL-8			80	mA
Hyper Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM48V2104A/AL/ALL/ASL-6	I_{CC4}	-	100	mA
	KM48V2104A/AL/ALL/ASL-7			90	mA
	KM48V2104A/AL/ALL/ASL-8			80	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{DD}-0.2V)	KM48V2104A	I_{CC5}	-	1	mA
	KM48V2104AL			300	μA
	KM48V2104ALL			200	μA
	KM48V2104ASL			200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM48V2104A/AL/ALL/ASL-6	I_{CC6}	-	100	mA
	KM48V2104A/AL/ALL/ASL-7			90	mA
	KM48V2104A/AL/ALL/ASL-8			80	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V_{IH})=V_{DD}-0.2V, Input Low Voltage (V_{IL})=0.2V, $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V, DQ_1~DQ_8=Don't Care, t_{RC}=62.5μs(L-Ver.) 125μs(SL-Ver.), t_{RAS}=t_{RAS} min.~300ns	KM48V2104AL	I_{CC7}	-	400	μA
	KM48V2104ASL			300	μA
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_{10}=V_{DD}-0.2V or 0.2V DQ_1~DQ_8=V_{DD}-0.2V, 0.2V or Open	KM48V2104ALL	I_{CC8}	-	250	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD}+0.3V$, all other pins not under test=0 volts.)	$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one Hyper Page cycle.

CAPACITANCE (T_A=25°C, V_{DD}=3.3V, f=1MHz))

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_{10})	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Output Capacitance (DQ_1~DQ_8)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{DD}=3.3V±0.3V, See notes 1,2)

Test Condition : V_{ih}/V_{il}=2.0V/0.8V, V_{oh}/V_{ol}=2.0V/0.8V, Output Loading C_L=100pF

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		ns	3
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{OEZ}	3	15	3	20	3	20	ns	7,14
Transition time (rise and fall)	t_T	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	45		50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	10,000	15	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	4
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	11

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	45		55		60		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	6
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		15		15		ns	9
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	
Write command pulse width	t_{WP}	10		15		15		ns	6
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	10		15		20		ns	
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	45		55		60		ns	6
Refresh period (Normal)	t_{REF}		32		32		32	ms	
Refresh period (Low power & Self Ref.)	t_{REF}		128		128		128	ms	
Refresh period (Super Low power)	t_{REF}		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	55		65		70		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	60		70		75		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Hyper Page cycle time	t_{HPC}	24		29		34		ns	17
Hyper Page read-modify-write cycle time	t_{HPRWC}	71		86		96		ns	17
$\overline{CAS}$ precharge time (Hyper Page cycle)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ pulse width (Hyper Page cycle)	t_{RASP}	60	200,000	70	200,000	80	200,000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Output buffer turn off delay time from $\overline{OE}$	tOEZ	3	15	3	20	3	20	ns	7,14
$\overline{OE}$ commend hold time	tOEH	15		20		20		ns	
Write command set-up time (Test mode in)	tWTS	10		10		10		ns	
Write command hold time (Test mode in)	tWTH	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		ns	
Output data hold time	tDOH	5		5		5		ns	7,15
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		ns	
$\overline{W}$ pulse width (Hyper Page Cycle)	tWPE	5		5		5		ns	
Output buffer turn off delay from $\overline{RAs}$	tREZ	3	15	3	20	3	20	ns	7,14
Output buffer turn off delay from $\overline{W}$	tWEZ	3	15	3	20	3	20	ns	7,14
$\overline{W}$ to data delay	tWED	15		20		20		ns	
$\overline{RAS}$ pulse width (LL-ver)	tRASS	100		100		100		μs	16
$\overline{RAS}$ precharge time (LL-ver)	tRPS	110		130		150		ns	16
$\overline{CAS}$ hold time (LL-ver)	tCHS	-50		-50		-50		ns	16

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	115		135		155		ns	
Read-modify-write cycle time	tRWC	160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		20		25		25	ns	3,4,5
Access time from column address	tAA		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	15	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	50		55		65		ns	
Column address to $\overline{RAS}$ lead time	tRAL	35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	60		70		75		ns	8
Hyper Page cycle time	tHPC	29		34		39		ns	
Hyper Page read-modify-write cycle time	tHPRWC	76		91		101		ns	
$\overline{RAS}$ pulse width (Hyper Page Cycle)	tRASP	65	200,000	75	200,000	85	200,000	ns	

TEST MODE CYCLE (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{CAS}$ precharge	tCPA		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	20		25		25		ns	

TEST MODE DESCRIPTION

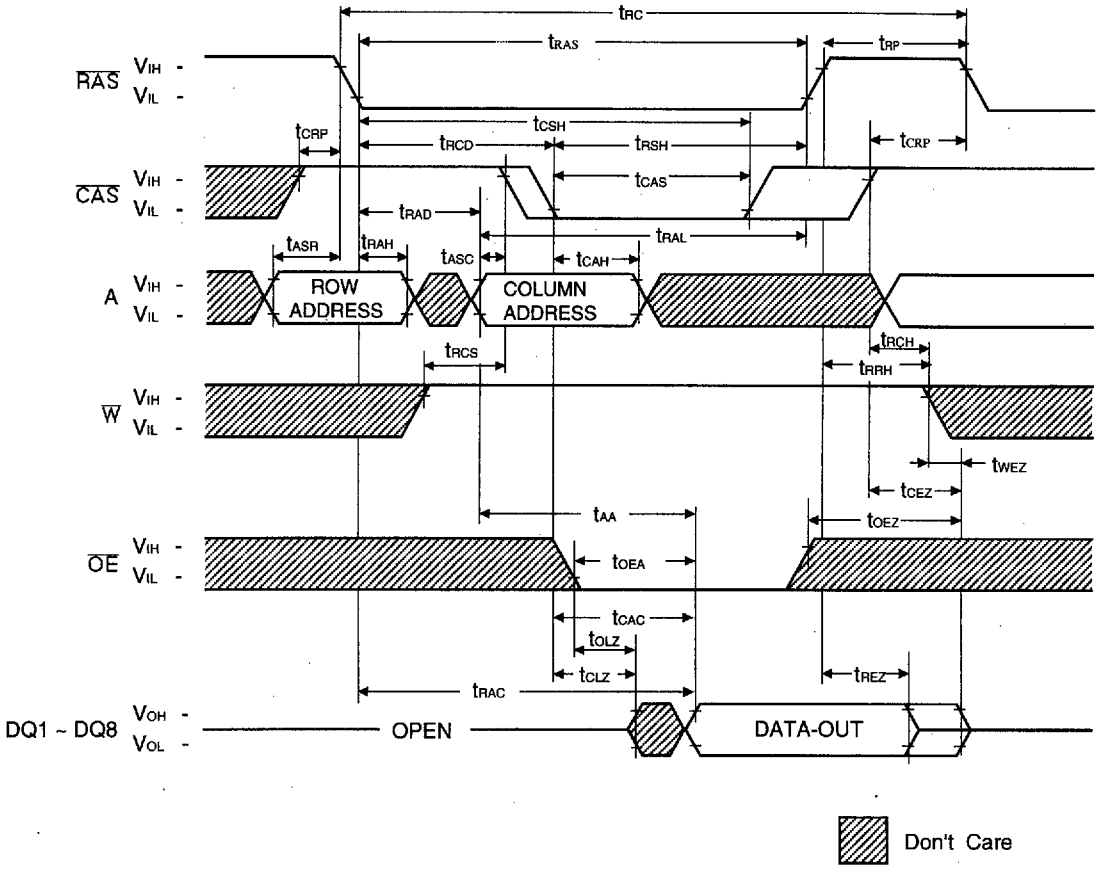
The KM48V2104A/AL/ALL/ASL is the CMOS DRAM organized 2,097,152 words by 8 bit internally organized 1,048,576 words by 16 bits. In " Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A0 is not used. If upon reading, two bits on one I/O pin are equal (all "1" or "0"s) the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In Test Mode", the 2Mx8 DRAM can be tested as if it were a 1Mx8 DRAM. $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ Cycle (WCBR, Test Mode In Cycle) puts the device into "Test Mode", And "$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle" or "RAS Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle" peforms the refresh operation with internal CBR refresh address counter. "Test Mode" function reduces test time (1/2 in cases of N test pattern).

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs, without t_{HPC} and t_{HPRWC}.
3. Measured with a load equivalent to 1TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{REZ}(max), t_{CEZ}(max), t_{WEZ}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 2048 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
16. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going
17. $t_{ASC} \geq t_{CP}$min, Assumn t_T=2.0ns

TIMING DIAGRAM

READ CYCLE



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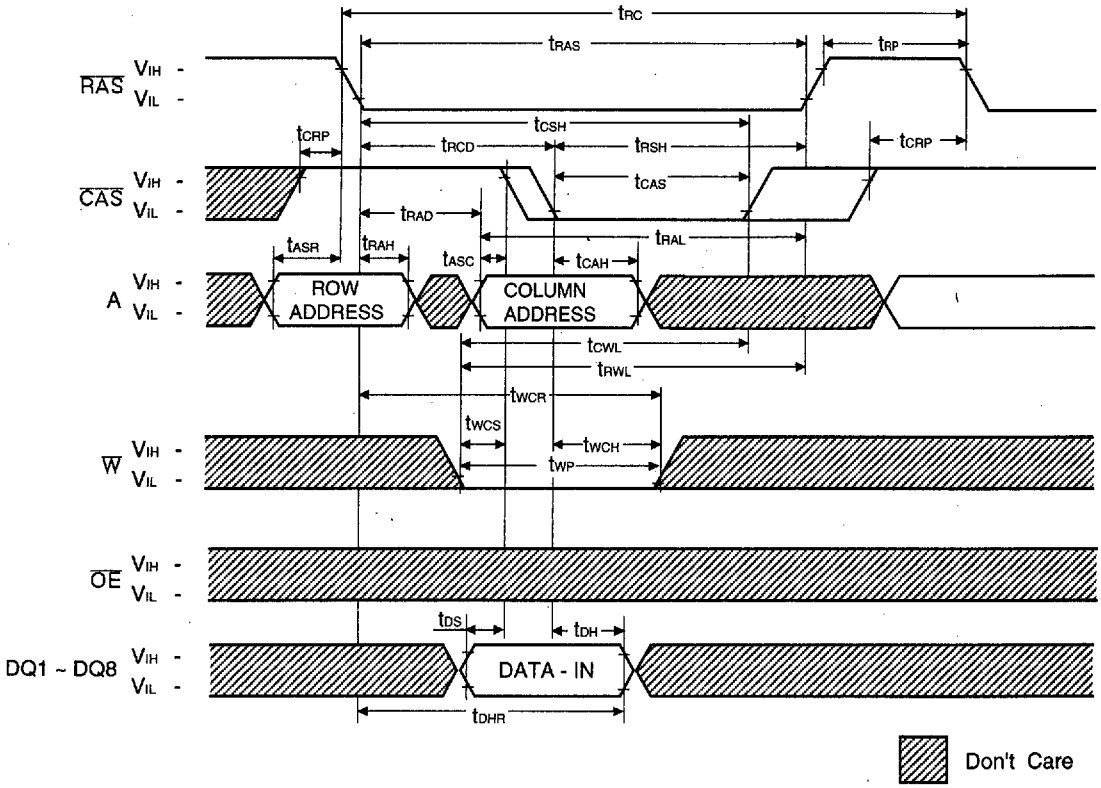
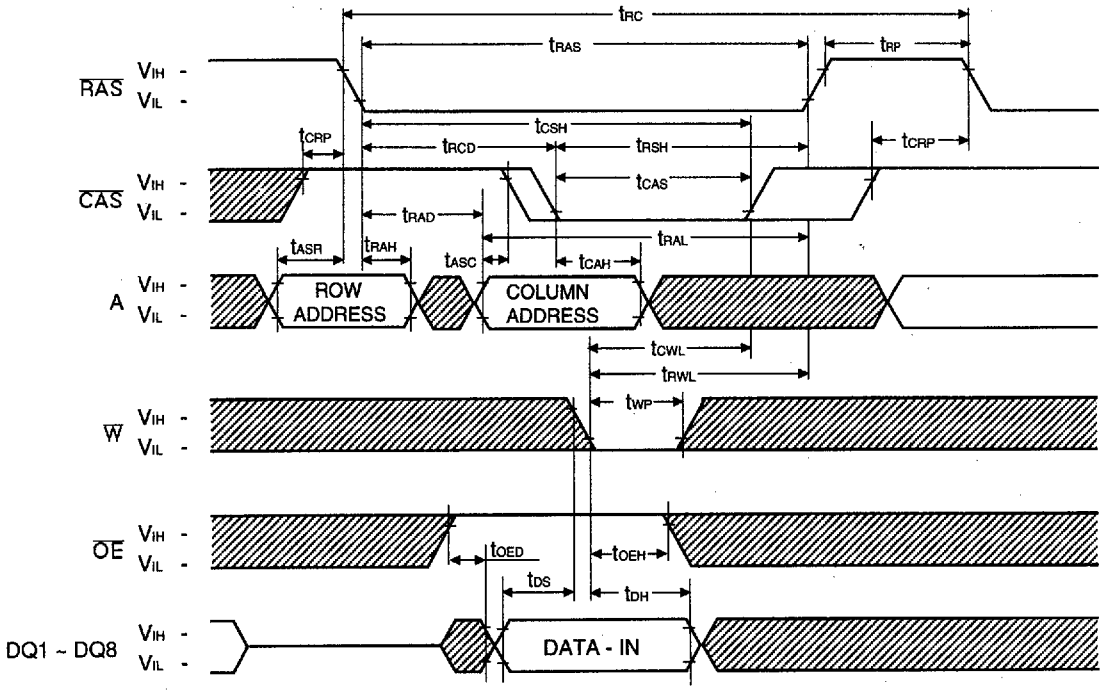
WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN



Don't Care

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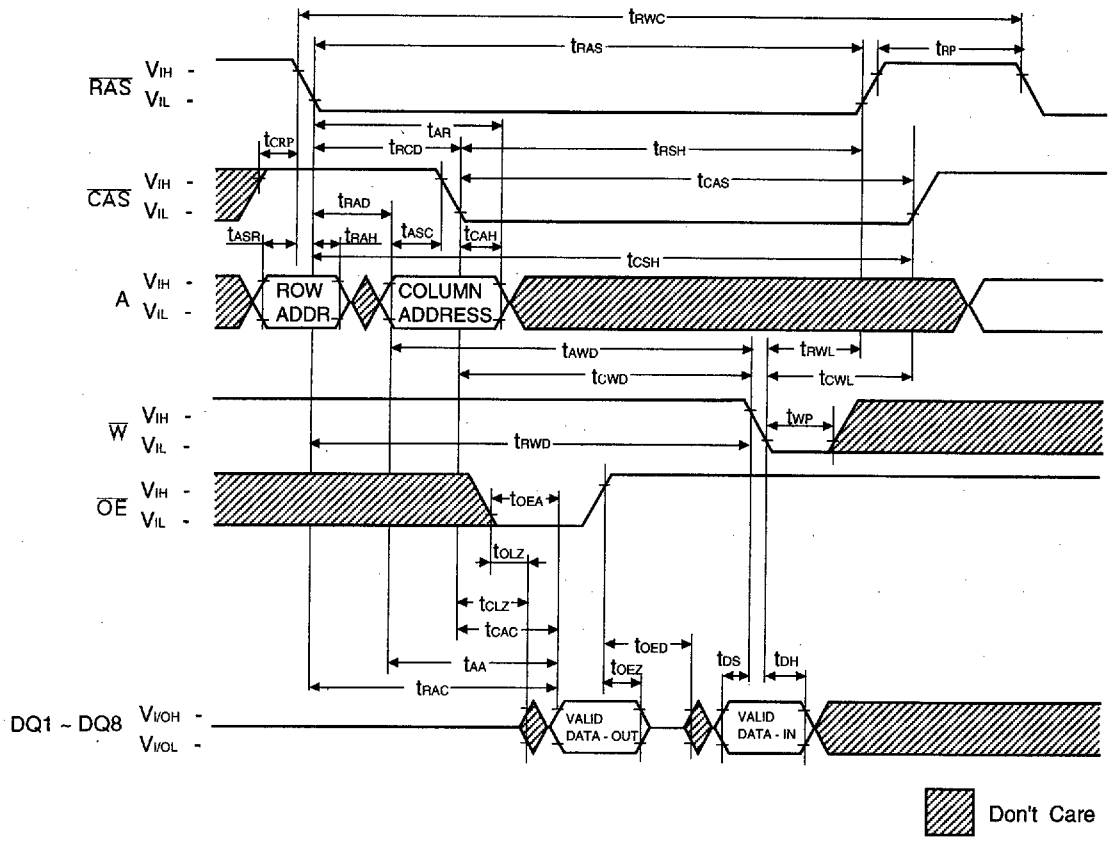
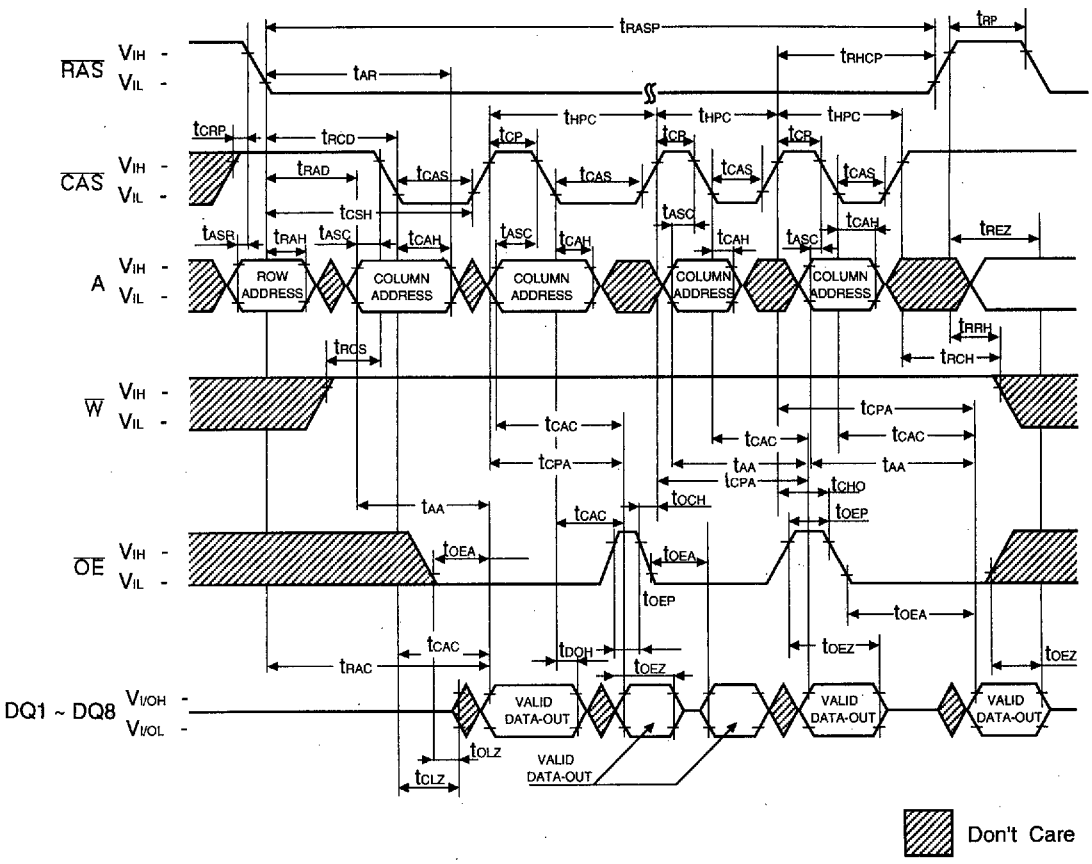
READ - MODIFY - WRITE CYCLE

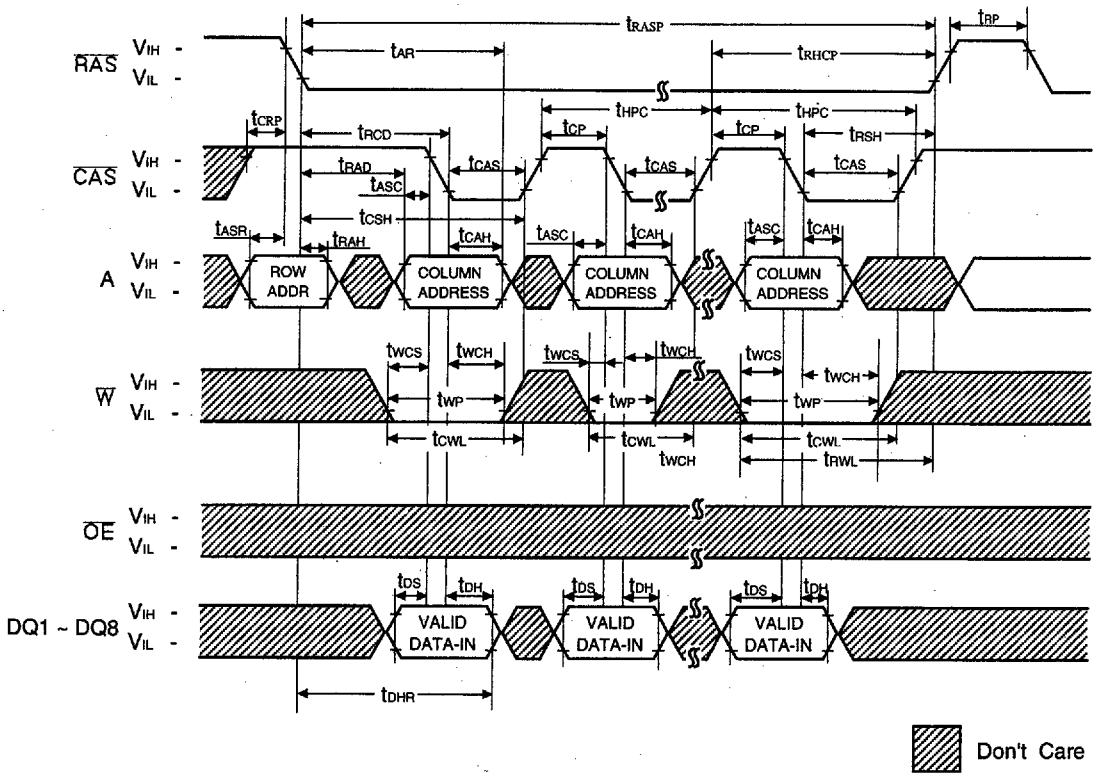


HYPER PAGE READ CYCLE

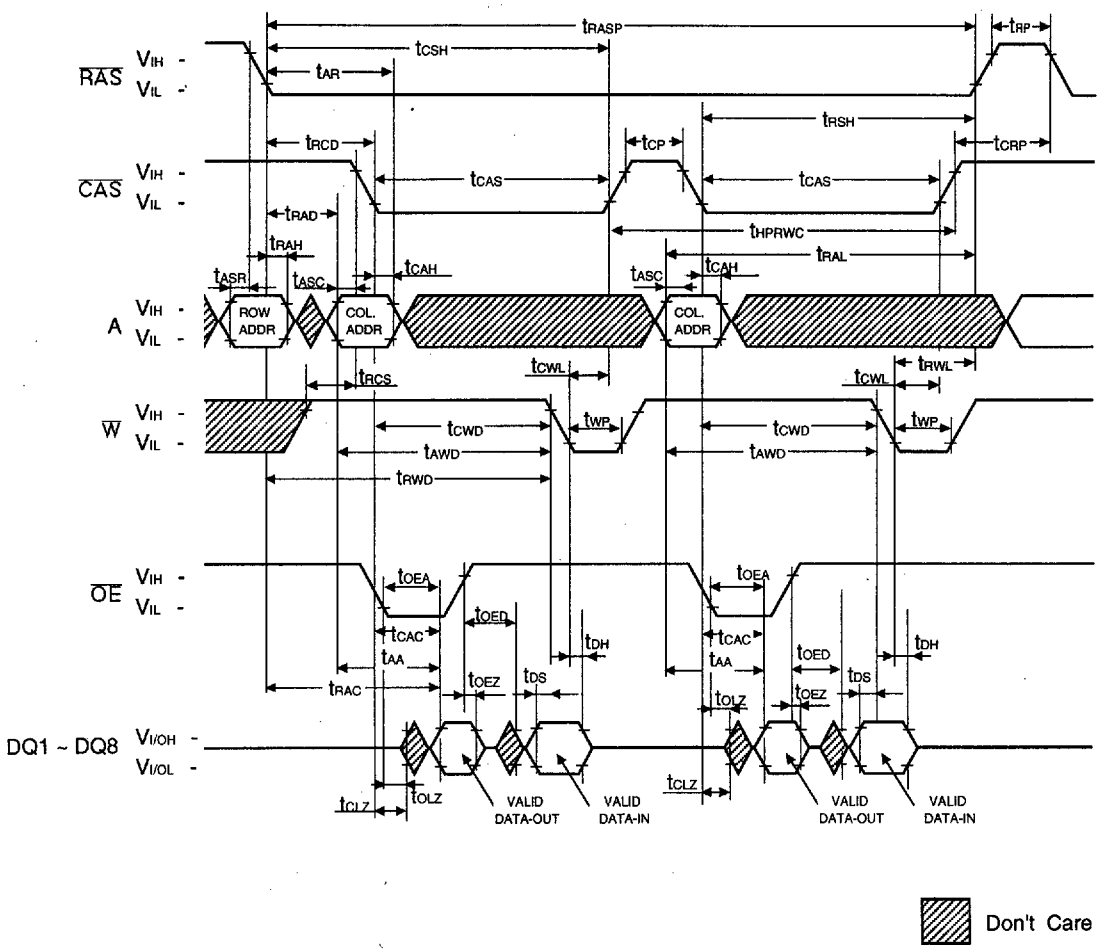


HYPER PAGE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open

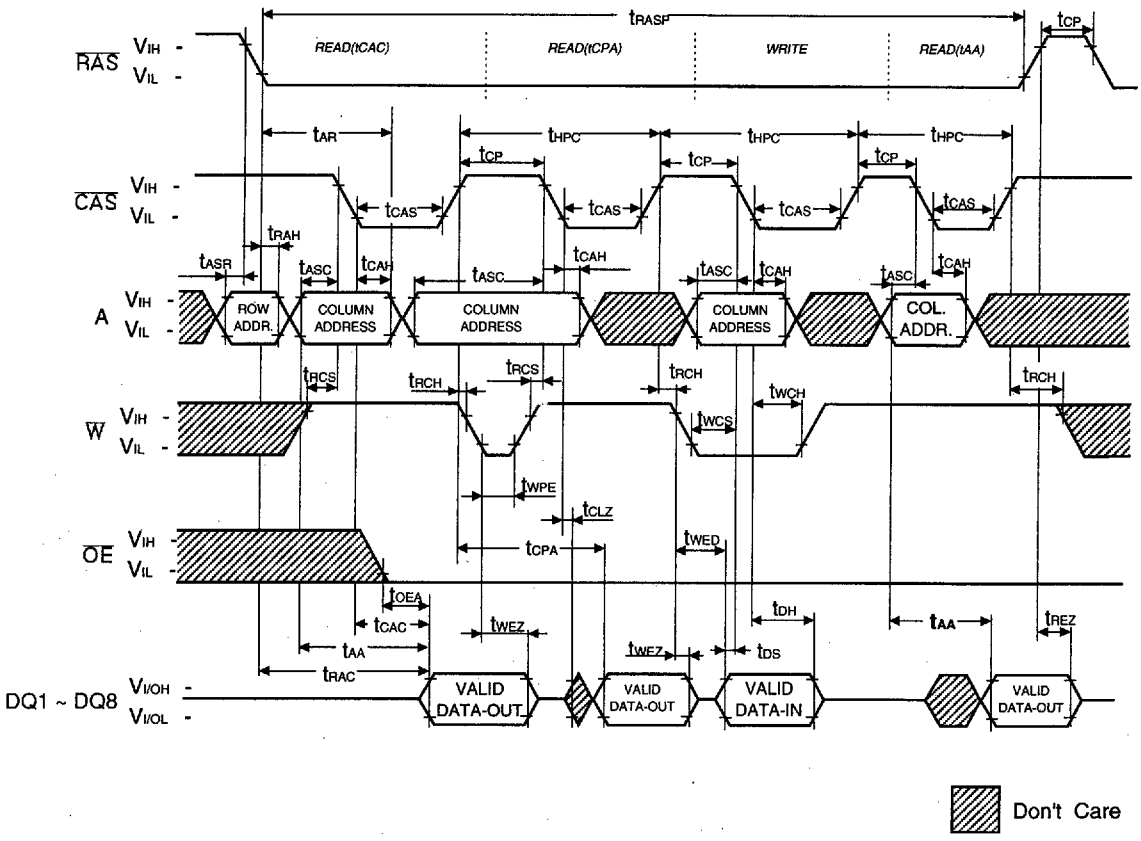


HYPER PAGE READ-MODIFY-WRITE CYCLE



6

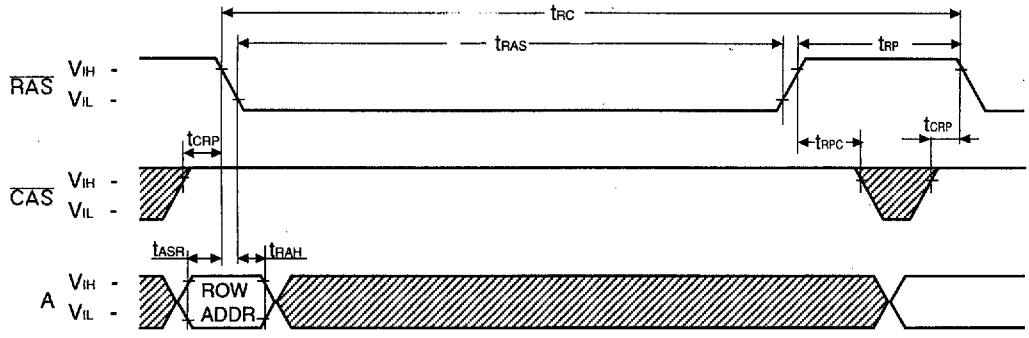
HYPER PAGE READ AND WRITE MIXED CYCLE



SAMSUNG ELECTRONICS

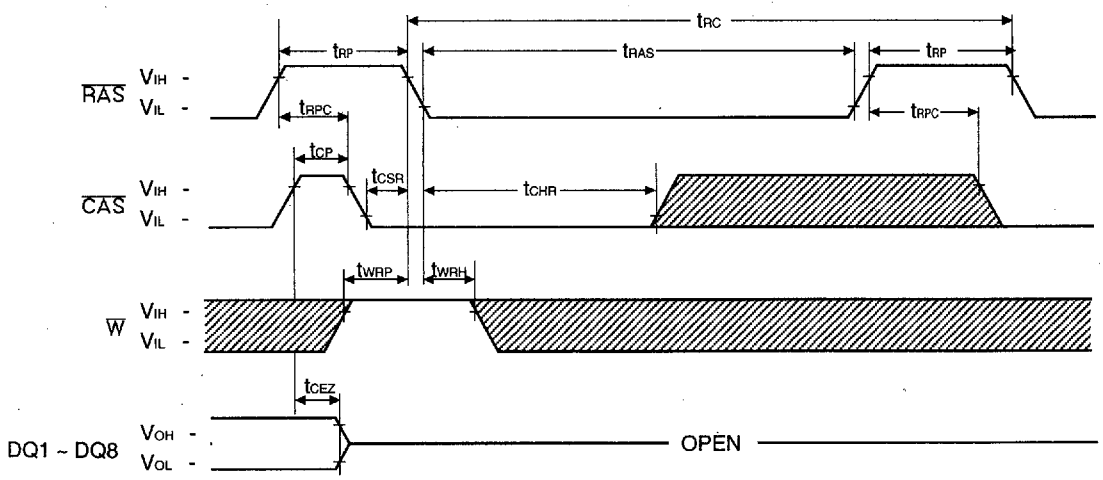
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care
D_{OUT} = Open



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care

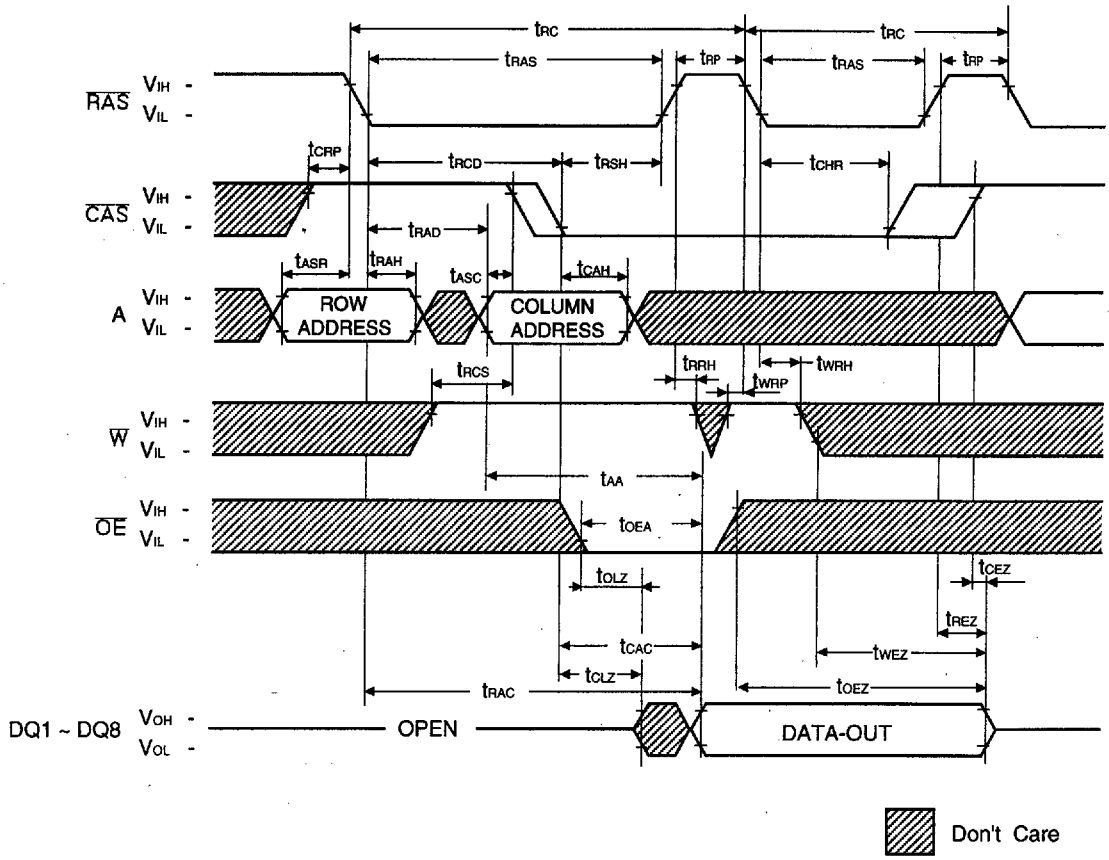


Don't Care

6

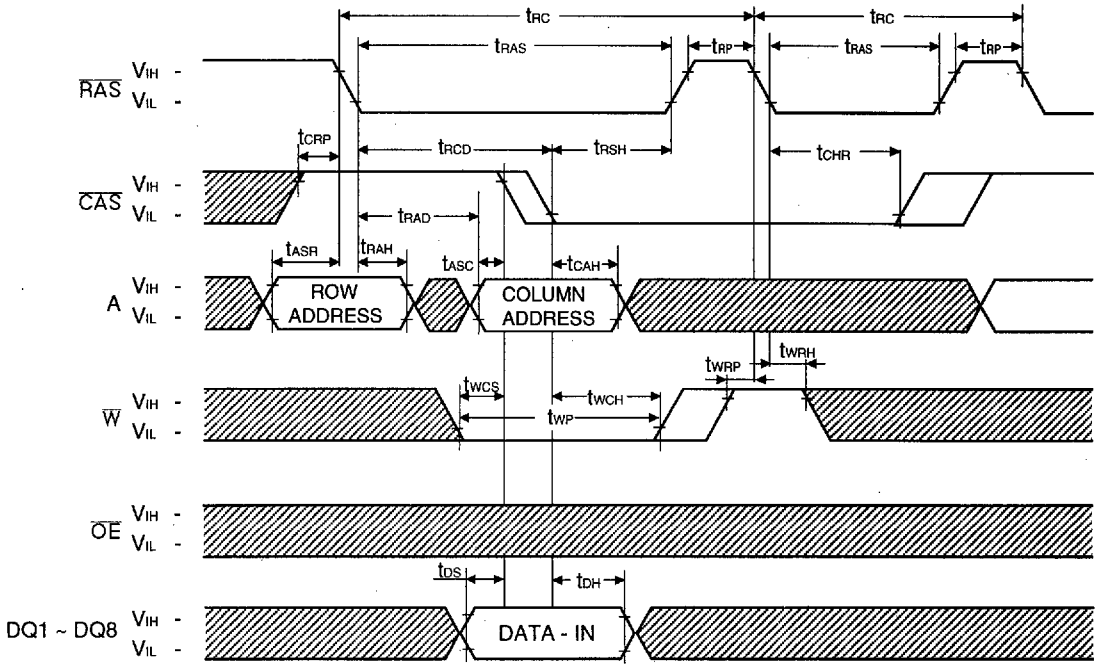
SAMSUNG ELECTRONICS

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN

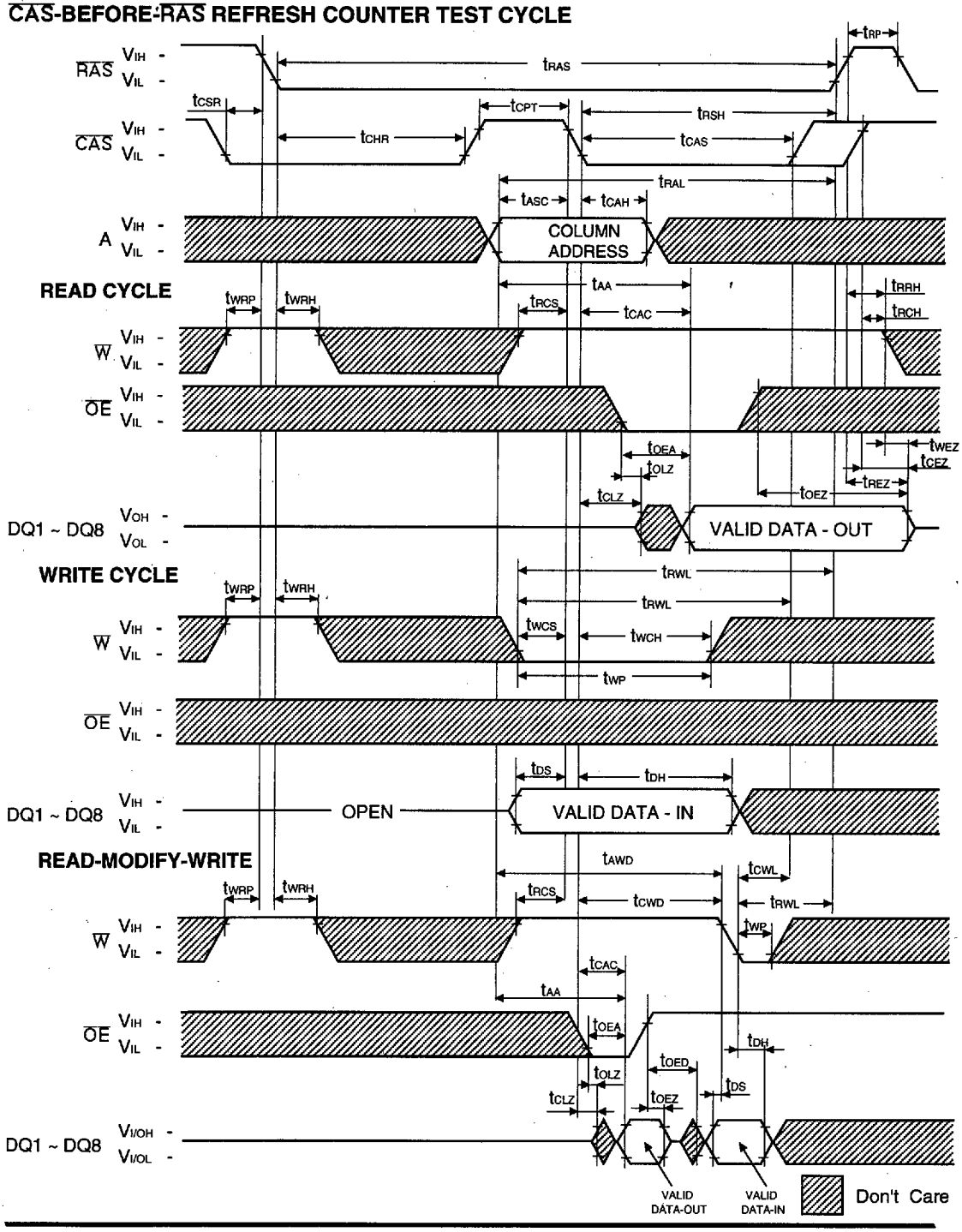


Don't Care

6

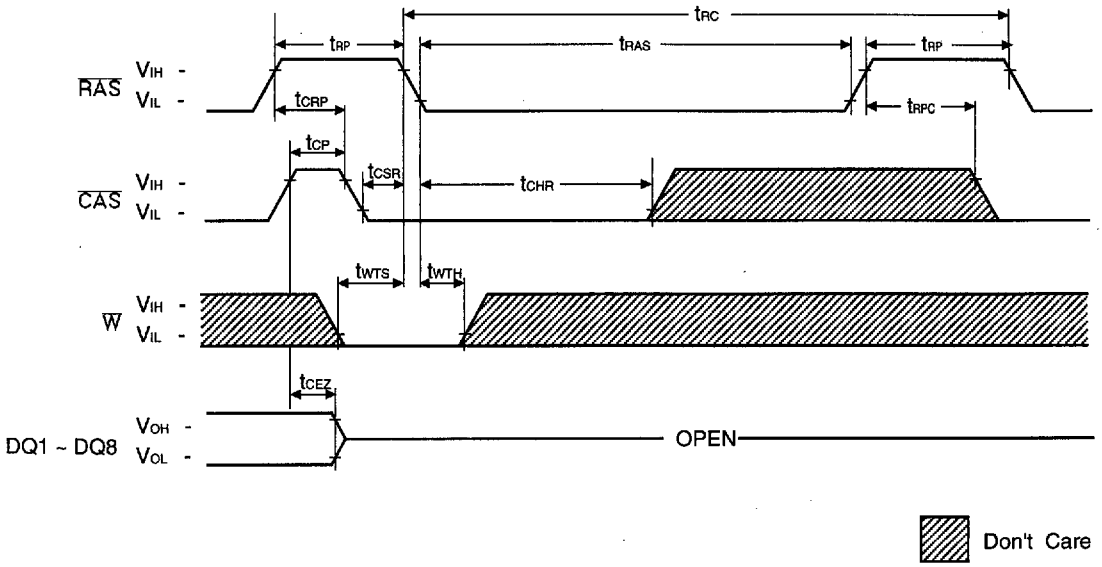
SAMSUNG ELECTRONICS

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TEST MODE IN CYCLE

NOTE : $\overline{OE}$, A = Don't Care

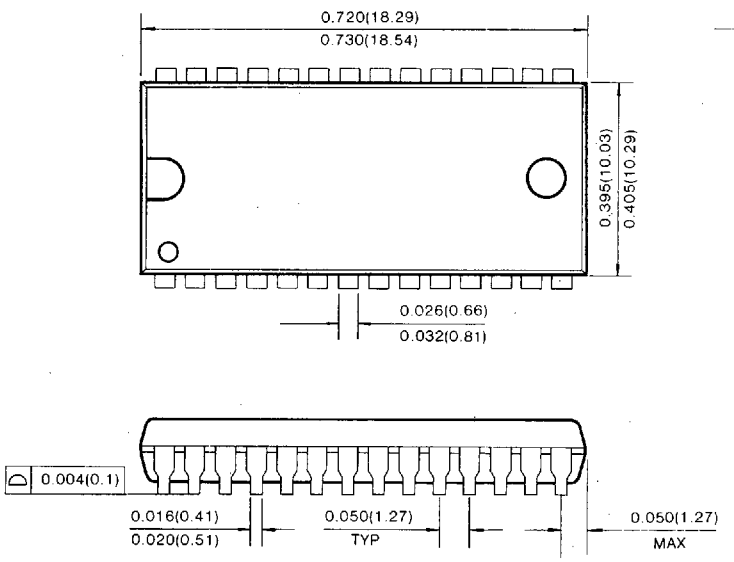


6

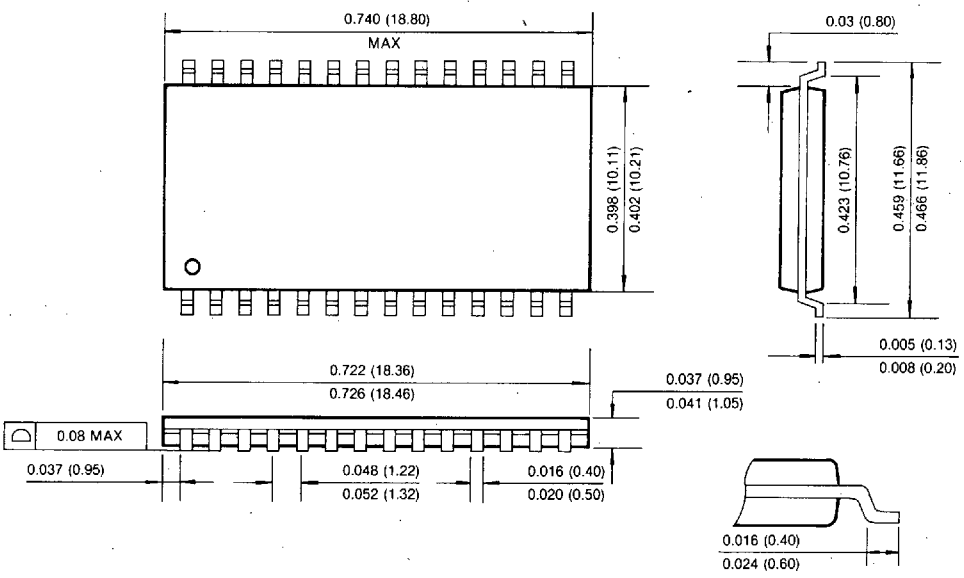
PACKAGE DIMENSION

28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



SAMSUNG ELECTRONICS