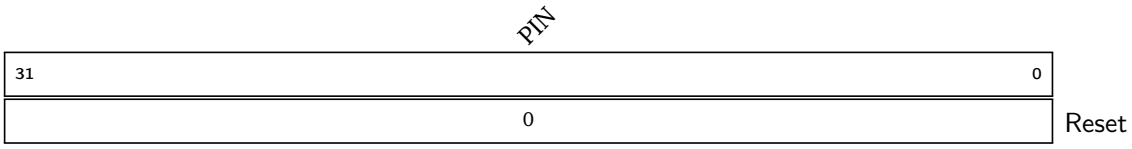
1 I/O registers

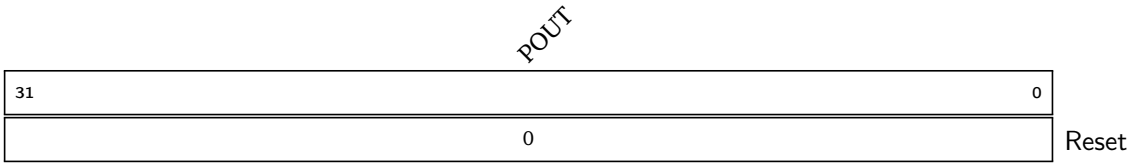
This is a list of currently supported I/O addresses. The default start address is 0xF0000000. The offset is given in bytes. Note that the I/O can only be accesses on 4-byte boundaries and on word size accesses.

1.1 GPIOA – General Purpose I/O



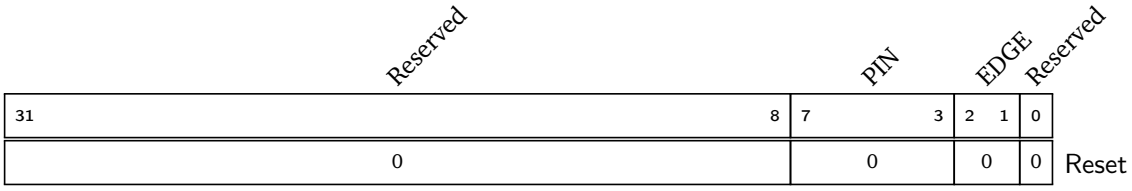
Register 1.1: PORT A INPUT REGISTER GPIOA_PIN *(0x00)*

Note: This I/O register can only be read. Writes are ignored.



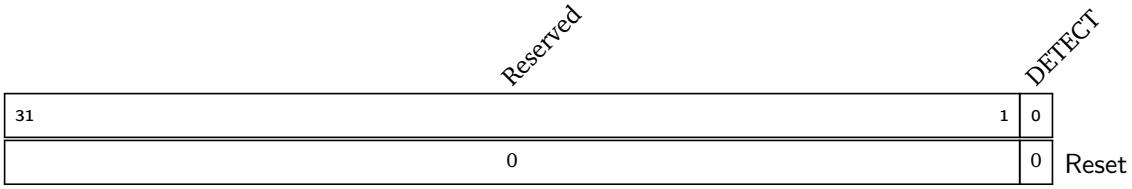
Register 1.2: PORT A OUTPUT REGISTER GPIOA_POUT *(0x04)*

Write The data is written to the output pins.
Read The last entered data is read back.



Register 1.3: EXTERNAL INPUT INTERRUPT CONTROL REGISTER GPIOA_EXTC *(0x18)*

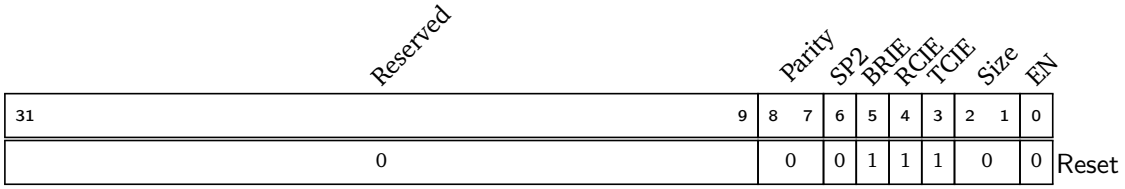
PIN Port pin number as input source.
EDGE Edge selection: 00 = off, 01 = rising, 10 = falling, 11 = both.



Register 1.4: EXTERNAL INPUT INTERRUPT STATUS REGISTER GPIOA_EXTS *(0x1c)*

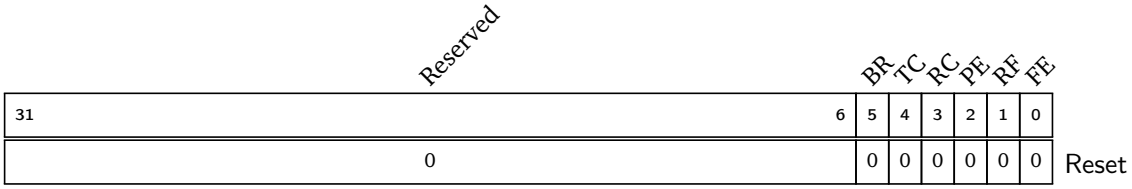
DETECT Edge detected. Must be cleared to reset the pending interrupt.

1.2 UART1 – Universal Asynchronous Receiver/Transmitter



Register 1.5: UART1 CONTROL REGISTER UART1_CTRL *(0x20)*

Parity 00: none, 10: even, 11: odd.
SP2 0: one stop bit, 1: two stop bits.
BRIE BREAK received interrupt enable.
TCIE Transmit character interrupt enable.
RCIE Receive character interrupt enable.
Size 00: 8 bits, 10: 9 bits, 11: 7 bits, excluding the parity.
EN Enable UART1 (both receiver and transmitter)



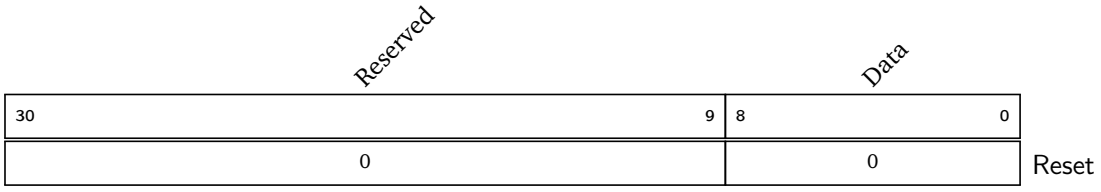
Register 1.6: UART1 STATUS REGISTER UART1_STAT *(0x24)*

BR BREAK condition detected. A BREAK is a stream of null bits for the duration of 1 start bit + number of data bits + 1 stop bit.
TC Transmit completed. Set directly to 1 when a character was transmitted. Automatically cleared when writing new character to the data register or when writing 0 in the TC bit in UART1_STAT.
RC Receive completed. Set to 1 when a character was received. Automatically cleared when data register is read or when writing 0 in the RC bit in UART1_STAT.

PE Parity error. Set to 1 if parity is enabled and there is a parity error while receiving. Automatically cleared when data register is read or when writing 0 in the PE bit in UART1_STAT.

RF Receive failed. Set to 1 when failed receiving (invalid start bit). Automatically cleared when data register is read or when writing 0 in the RF bit in UART1_STAT.

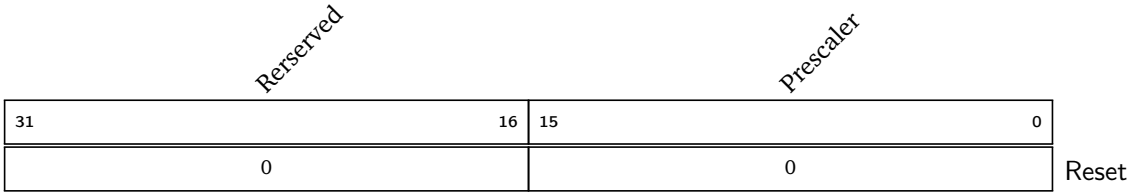
FE Frame error. Set to 1 when a low is detected at the position of the (first) stop bit. Automatically cleared when data register is read or writing a 0 in the FE bit in UART1_STAT.



Register 1.7: UART1 DATA REGISTER UART1_DATA *(0x28)*

Write	The data is written to an internal buffer and transmitted.
Read	The last received data is read.

Size depends on the Size field in the UART1 Control Register.

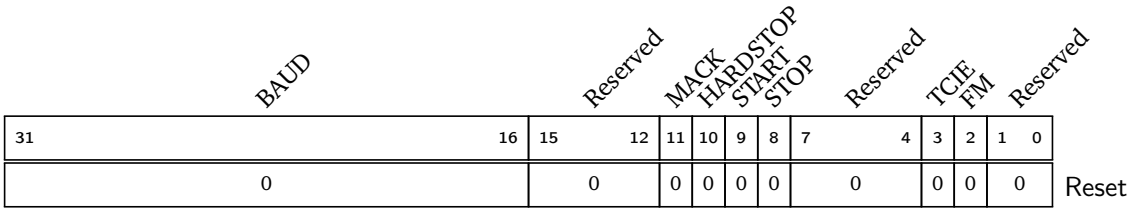


Register 1.8: UART1 BAUD RATE REGISTER UART1_BAUD *(0x2c)*

Prescaler $\text{Baud rate} = \dfrac{f_{system}}{\text{prescaler} + 1}$

1.3 I2C1 – Inter-Integrated Circuit master-only controller

General purpose I^2C peripheral, with programmable baud rate prescaler, start- and stop-bit generation, no clock stretching, no arbitration, Standard mode (Sm) and Fast mode (Fm) only.



Register 1.9: I2C1 CONTROL REGISTER I2C1_CTRL *(0x40)*

BAUD Baud rate prescaler. Number of system clock pulses minus 1 for **one-half** bit time (Sm) or **one-third** bit time (Fm). Note: because of the 50 MHz system frequency, the lowest I^2C clock frequency is 763 Hz.

MACK Set to 1 to acknowledge a reception by the master. Must only be used when receiving.

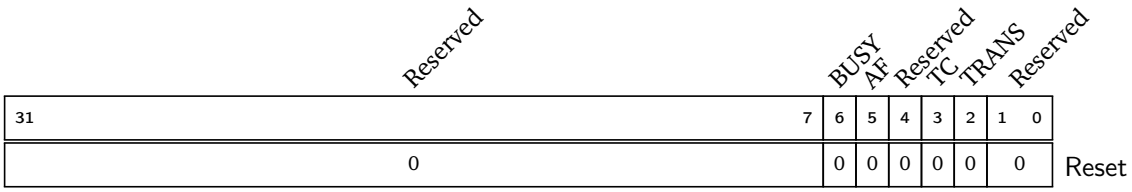
HARDSTOP Set to 1 to just generate a STOP condition. Useful after addressing a target that didn't respond. Cleared by hardware.

START Send a START before next byte send. Cleared by hardware when transmission ends.

STOP Send a STOP after next byte send or received. Cleared by hardware when transmission ends.

TCIE Transmission Complete interrupt enable.

FM 0: Standard mode 1:1 (SCL 1/2 low, 1/2 high)
1: Fast mode 2:1 (SCL 2/3 low, 1/3 high)



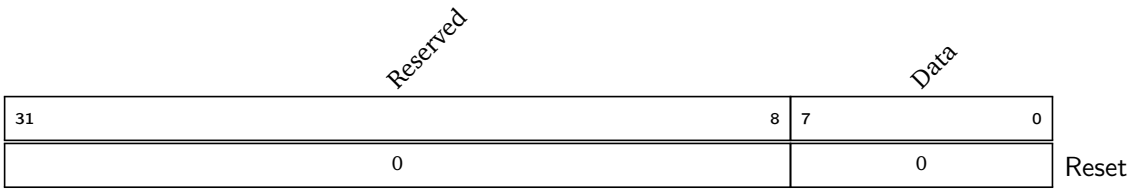
Register 1.10: I2C1 STATUS REGISTER I2C1_STAT *(0x44)*

BUSY Set to 1 when SDA or SCL is low, set to 0 when STOP condition is detected, independent of the I2C1 device.

AF Acknowledge Fail, set when no target responded. Cleared by hardware when `I2C1_DATA` is accessed.

TC Transmission Complete, including START or STOP, if any. Cleared by hardware when `I2C1_DATA` is accessed.

TRANS Indicates transmitting (1) or not (0) by this controller.

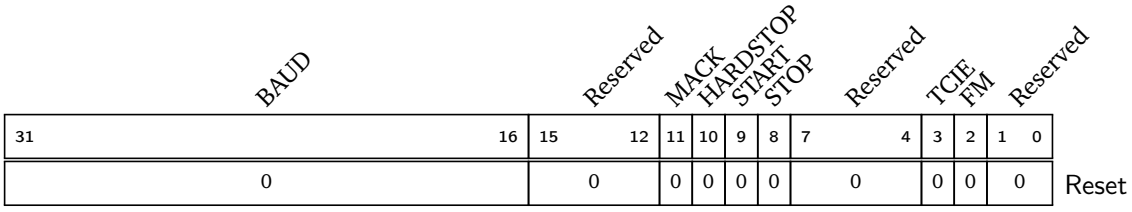


Register 1.11: I2C1 DATA REGISTER I2C1_DATA *(0x48)*

Write	The data is written to an internal buffer and transmitted.
Read	The last received data is read.

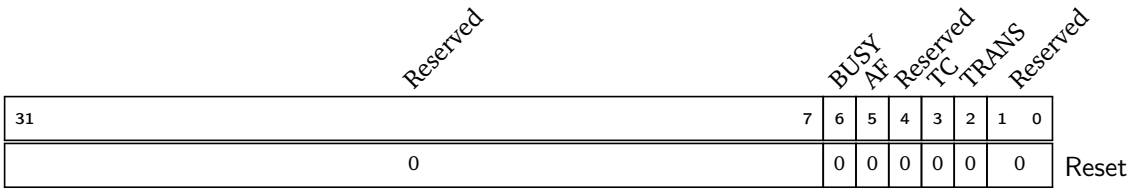
1.4 I2C2 – Inter-Integrated Circuit master-only controller

General purpose I^2C peripheral, with programmable baud rate prescaler, start- and stop-bit generation, no clock stretching, no arbitration, Standard mode (Sm) and Fast mode (Fm) only.



Register 1.12: I2C2 CONTROL REGISTER I2C2_CTRL *(0x50)*

BAUD	Baud rate prescaler. Number of system clock pulses minus 1 for **one-half** bit time (Sm) or **one-third** bit time (Fm). Note: because of the 50 MHz system frequency, the lowest I^2C clock frequency is 763 Hz.
MACK	Set to 1 to acknowledge a reception by the master. Must only be used when receiving.
HARDSTOP	Set to 1 to just generate a STOP condition. Useful after addressing a target that didn't respond. Cleared by hardware.
START	Send a START before next byte send. Cleared by hardware when transmission ends.
STOP	Send a STOP after next byte send or received. Cleared by hardware when transmission ends.
TCIE	Transmission Complete interrupt enable.
FM	0: Standard mode 1:1 (SCL 1/2 low, 1/2 high) 1: Fast mode 2:1 (SCL 2/3 low, 1/3 high)



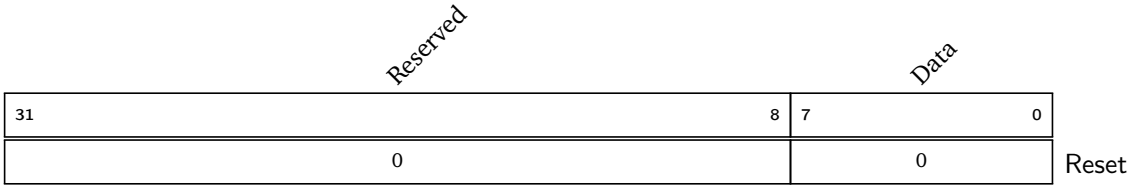
Register 1.13: I2C2 STATUS REGISTER I2C2_STAT *(0x54)*

BUSY Set to 1 when SDA or SCL is low, set to 0 when STOP condition is detected, independent of the I2C1 device.

AF Acknowledge Fail, set when no target responded. Cleared by hardware when `I2C2_DATA` is accessed.

TC Transmission Complete, including START or STOP, if any. Cleared by hardware when `I2C2_DATA` is accessed.

TRANS Indicates transmitting (1) or not (0) by this controller.



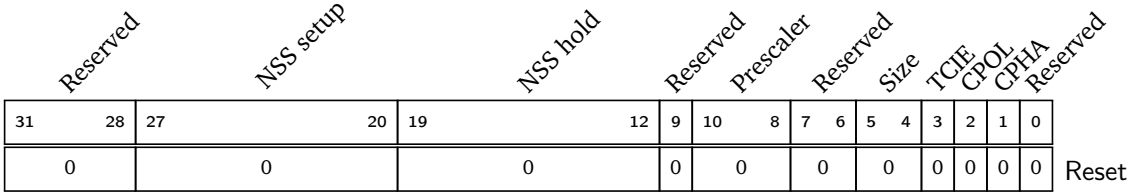
Register 1.14: I2C2 DATA REGISTER I2C2_DATA *(0x58)*

Write The data is written to an internal buffer and transmitted.

Read The last received data is read.

1.5 SPI1 – Serial Peripheral Interface

General purpose SPI master peripheral, with prescaler, 8/16/24/32 bits data exchange, hardware NSS and interrupt.



Register 1.15: SPI1 CONTROL REGISTER SPI1_CTRL *(0x60)*

NSS setup Number of system clock pulses after NSS active before transfer starts

NSS hold Number of system clock pulses before NSS inactive after transfer ends

Prescaler
000 /2
001 /4
010 /8
011 /16
100 /32
101 /64
110 /128
111 /256

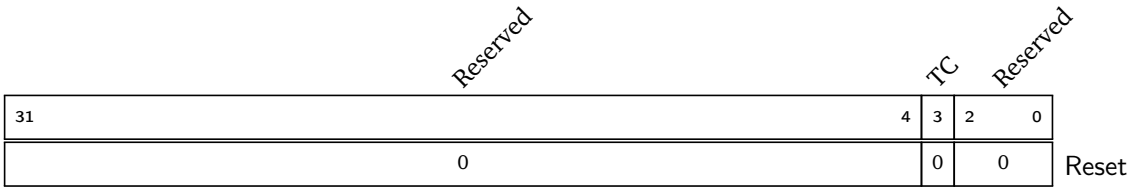
Note: because of the 50 MHz system frequency, the lowest SPI clock frequency is 195.3125 kHz.

Size
00 8 bits
01 16 bits
10 24 bits
11 32 bits

TCIE Transfer complete interrupt enable

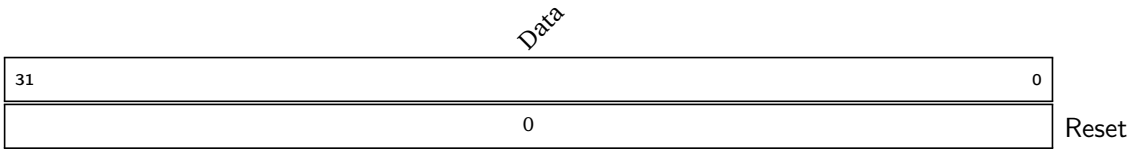
CPOL Clock polarity

CPHA Transfer phase



Register 1.16: SPI1 STATUS REGISTER SPI1_STAT *(0x64)*

TC Transfer complete



Register 1.17: SPI1 DATA REGISTER SPI1_DATA *(0x68)*

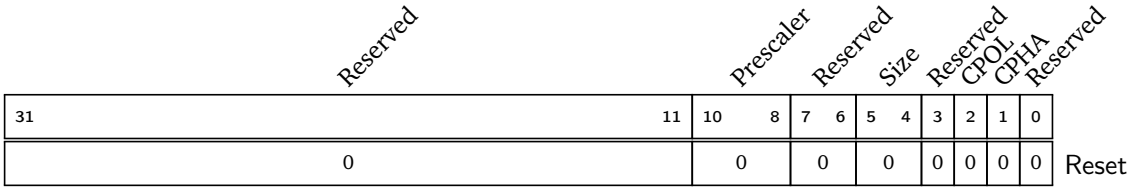
Write The data is written to an internal buffer and transmitted.

Read The last received data is read.

Data size depends on the Size field in the SPI1 Control Register. Data is right aligned.

1.6 SPI2 – Serial Peripheral Interface

SPI master peripheral dedicated for SD card access, with prescaler and 8/16/24/32 bits data exchange. This device has no interrupt available.



Register 1.18: SPI2 CONTROL REGISTER SPI2_CTRL *(0x70)*

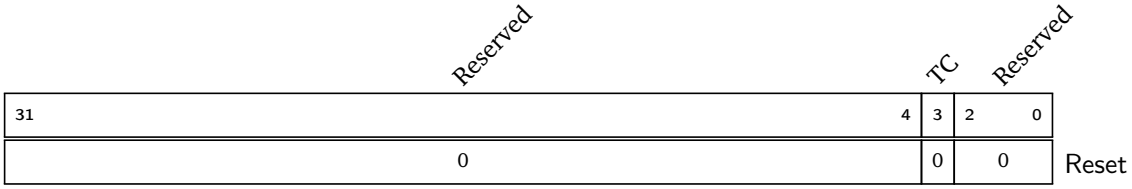
Prescaler
000 /2
001 /4
010 /8
011 /16
100 /32
101 /64
110 /128
111 /256

Note: because of the 50 MHz system frequency, the lowest SPI clock frequency is 195.3125 kHz.

Size
00 8 bits
01 16 bits
10 24 bits
11 32 bits

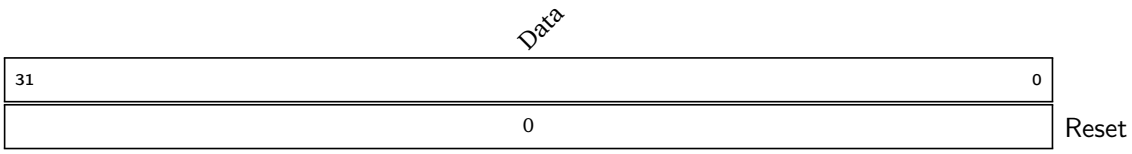
CPOL Clock polarity

CPHA Transfer phase



Register 1.19: SPI2 STATUS REGISTER SPI2_STAT *(0x74)*

TC Transfer complete



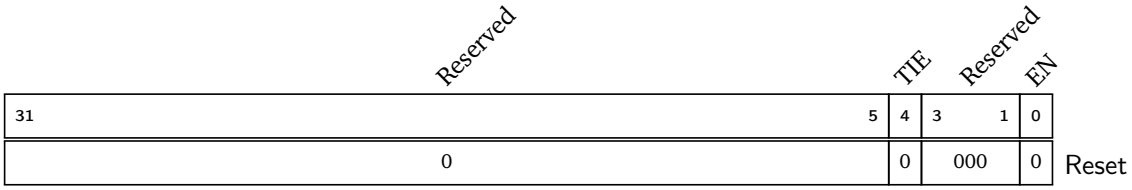
Register 1.20: SPI2 DATA REGISTER SPI2_DATA *(0x78)*

Write	The data is written to an internal buffer and transmitted.
Read	The last received data is read.

Data size depends on the Size field in the SPI2 Control Register. Data is right aligned.

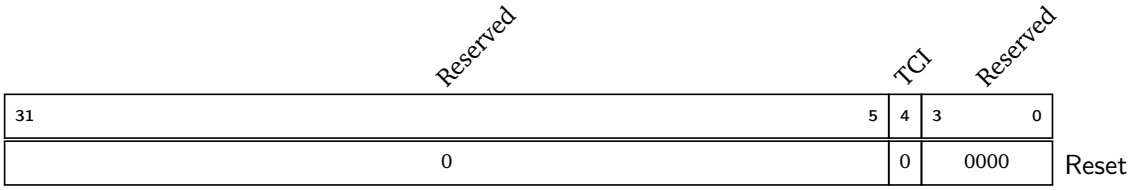
1.7 TIMER1 – a simple timer

Simple 32-bit timer peripheral for time base generation, with interrupt.



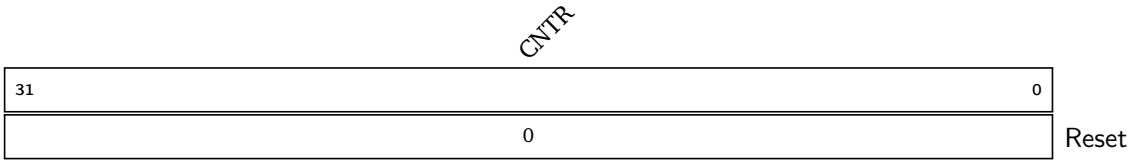
Register 1.21: TIMER1 CONTROL REGISTER TIMER1_CTRL *(0x80)*

EN	Enable the timer
TIE	Timer compare match interrupt enable



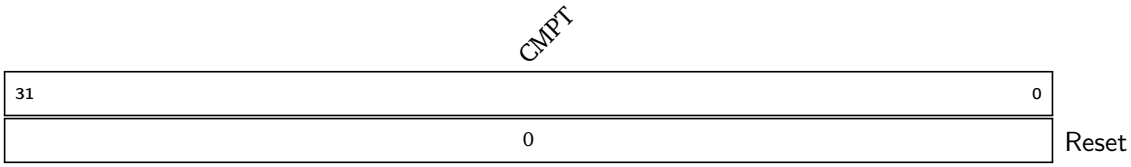
Register 1.22: TIMER1 STATUS REGISTER TIMER1_STAT *(0x84)*

TCI	Timer compare match interrupt. Set to 1 on compare match between the timer Count register and the Compare Match register. Must be cleared by software by writing a 0.



Register 1.23: TIMER1 COUNT REGISTER TIMER1_CNTR *(0x88)*

CNTR This register holds the counted clock pulses on the timer. This register may be written by software.

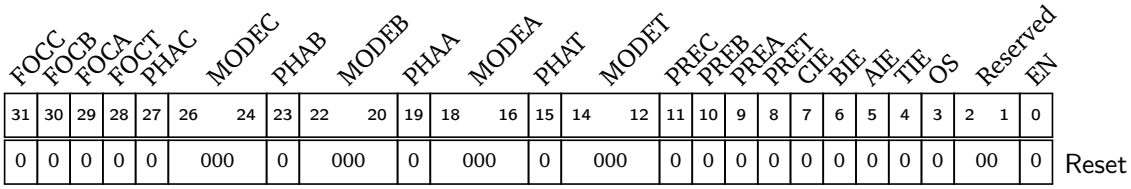


Register 1.24: TIMER1 COMPARE TIMER T REGISTER TIMER1_CMPT *(0x8c)*

CMPT This register holds the value at which the counter register is compared. On CNTR compares to greater than or equal to CMPT, the counter register will be cleared and the TCI flag will be set (both in the next clock cycle).

1.8 TIMER2 – a more elaborate timer

General purpose 16-bit timer with Output Compare, PWM generation and Input Capture capabilities, preload and interrupts.



Register 1.25: TIMER2 CONTROL REGISTER TIMER2_CTRL *(0x90)*

FOCC Force Output Compare match C.
FOCB Force Output Compare match B.
FOCA Force Output Compare match A.
FOCT Force Output Compare match T.
PHAC Register C start phase.
MODEC Register C mode.
PHAB Register B start phase.
MODEB Register B mode.
PHAA Register A start phase.
MODEA Register A mode.
PHAT Register T start phase.
MODET Register T mode.
PREC Enable compare register C preload.
PREB Enable compare register B preload.
PREA Enable compare register A preload.
PRET Enable compare register T preload.
CIE Timer compare match/input capture C interrupt enable
BIE Timer compare match/input capture B interrupt enable

AIE Timer compare match/input capture A interrupt enable
TIE Timer compare match T interrupt enable
OS One-shot mode
EN Enable the timer

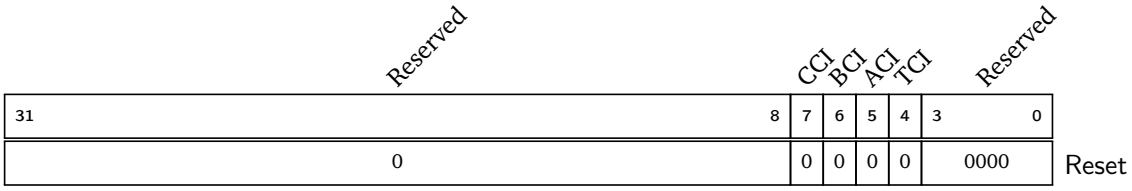
If none of the FOC*x* bits are 1, MODET and MODEA/B/C have the following meaning:

000 Output off
001 Toggle on compare match
010 Set high on compare match
011 Set low on compare match
100 Edge-aligned PWM (only A/B/C, for T not allowed)
101 Reserved
110 Input capture positive edge (only A/B/C, for T not allowed)
111 Input capture negative edge (only A/B/C, for T not allowed)

If at least one of the FOC*x* bits is 1, MODET and MODEA/B/C have the following meaning:

000 Not used
001 Toggle output compare
010 Set high output compare
011 Set low output compare
100 not allowed
101 not allowed
110 not allowed
111 not allowed

In this case, the CTRL register is not written and keeps its original setting.

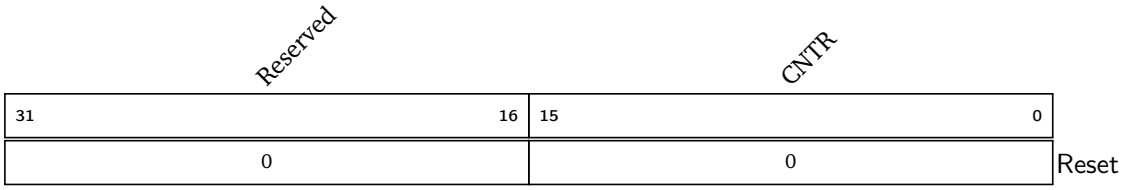


Register 1.26: TIMER2 STATUS REGISTER TIMER2_STAT *(0x94)*

CCI Timer compare match A interrupt. Set to 1 on compare match between the timer Count register and the Compare Match C register. Set on input capture on detecting selected edge. Must be cleared by software by writing a 0.
BCI Timer compare match A interrupt. Set to 1 on compare match between the timer Count register and the Compare Match B register. Set on input capture on detecting selected edge. Must be cleared by software by writing a 0.

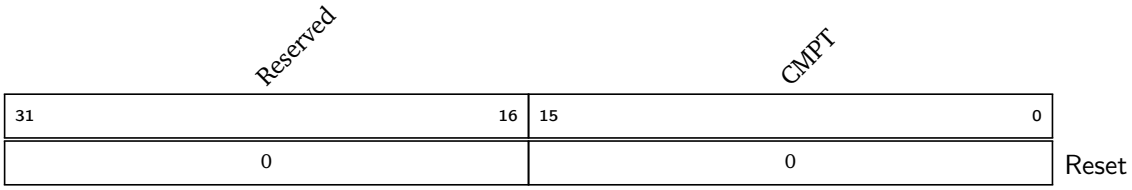
ACI Timer compare match A interrupt. Set to 1 on compare match between the timer Count register and the Compare Match A register. Set on input capture on detecting selected edge. Must be cleared by software by writing a 0.

TCI Timer compare match T interrupt. Set to 1 on compare match between the timer Count register and the Compare Match T register. Must be cleared by software by writing a 0.



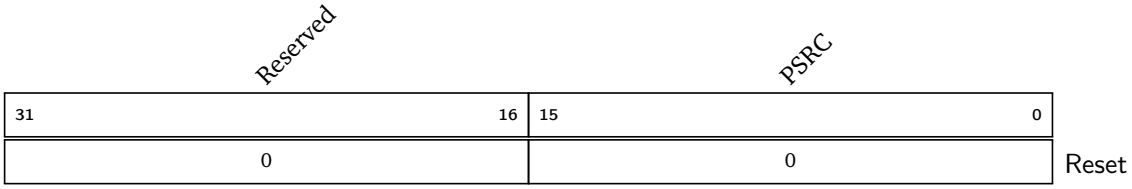
Register 1.27: TIMER2 COUNT REGISTER TIMER2_CNTR *(0x98)*

CNTR This register holds the counted clock pulses on the timer. This register may be written by software. Rolls over when CNTR compare greater than or equal to CMPT on the next clock cycle.



Register 1.28: TIMER2 COMPARE TIMER T REGISTER TIMER2_CMPT *(0x9c)*

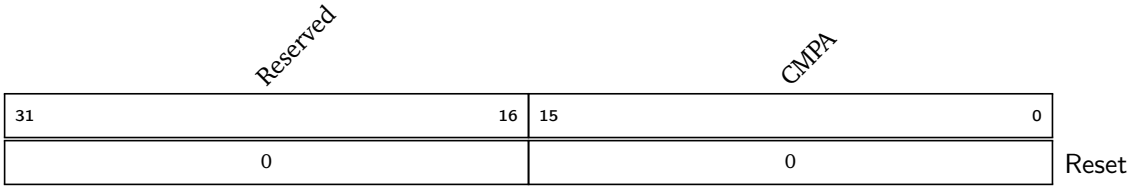
CMPT This register holds the value at which the Count register is compared. On CNTR compares to greater than or equal to CMPT, the Count register will be cleared and the TCI flag will be set (both in the next clock cycle).



Register 1.29: TIMER2 PRESCALER REGISTER TIMER2_PRSC *(0xa0)*

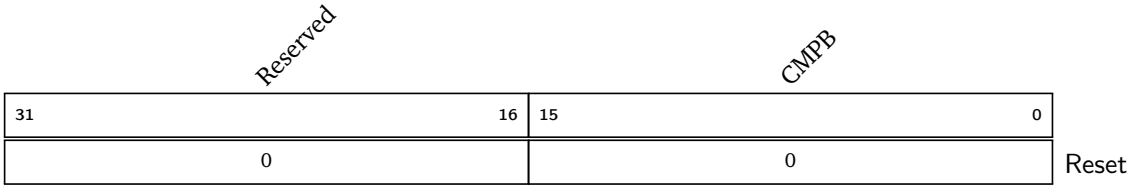
PRSC This register holds the prescaler of the timer. This register may be written by software. Whenever the internal prescaler is equal to or greater than this register, the internal prescaler

is reset. This register should only be written when the timer is stopped. Writing this register resets the internal prescaler.



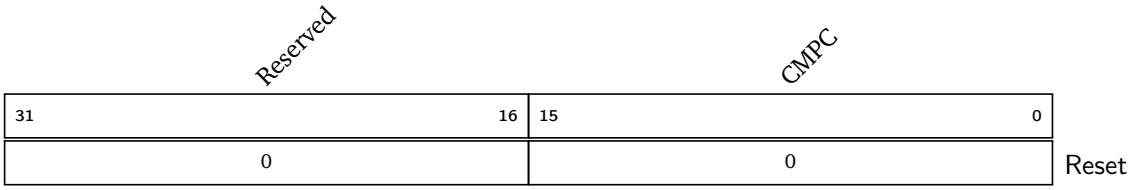
Register 1.30: TIMER2 COMPARE TIMER A REGISTER TIMER2_CMPA *(0xa4)*

CMPA For Output Compare: This register holds the value at which the Count register is compared. On CNTR compares to greater than or equal to CMPA, the ACI flag will be set in the next clock cycle. For Input Capture: The value of CNTR is copied to CMPA on detecting the selected edge, and the ACI flag is set.



Register 1.31: TIMER2 COMPARE TIMER B REGISTER TIMER2_CMPB *(0xa8)*

CMPB For Output Compare: This register holds the value at which the Count register is compared. On CNTR compares to greater than or equal to CMPB, the BCI flag will be set in the next clock cycle. For Input Capture: The value of CNTR is copied to CMPB on detecting the selected edge, and the BCI flag is set.

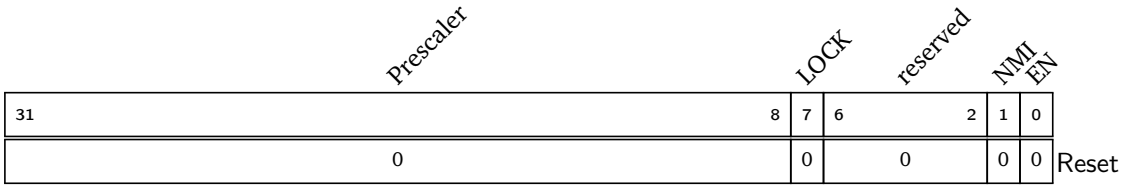


Register 1.32: TIMER2 COMPARE TIMER C REGISTER TIMER2_CMPC *(0xac)*

CMPC For Output Compare: This register holds the value at which the Count register is compared. On CNTR compares to greater than or equal to CMPC, the CCI flag will be set in the next clock cycle. For Input Capture: The value of CNTR is copied

to CMPC on detecting the selected edge, and the CCI flag is set.

1.9 WDT – Watchdog Timer



Register 1.33: WATCHDOG CONTROL REGISTER WDT_CTRL *(0xe0)*

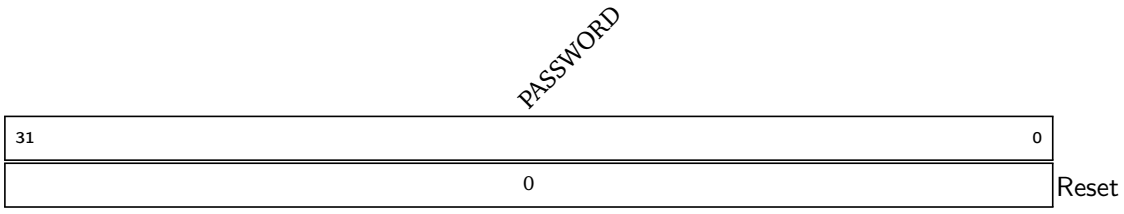
Prescaler 24-bit prescaler. The timeout time is computed with

$$t = \frac{Prescaler \cdot 256}{f_{cpu}}$$

LOCK If set to 1, the control register is locked. Watchdog write accesses trigger a system reset or NMI.

NMI If set to 1, the watchdog triggers an NMI on timeout, otherswise the watchdog triggers a system reset on timeout.

EN If set to 1, the WDT starts counting.

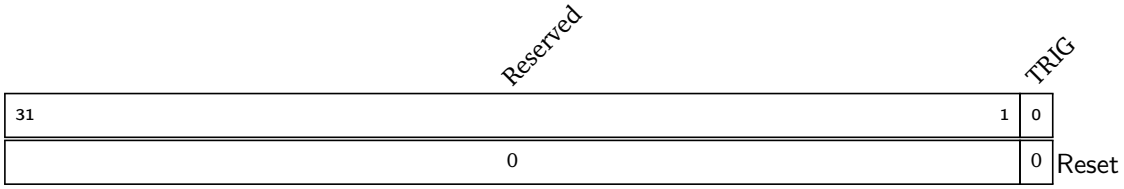


Register 1.34: WATCHDOG TRIGGER REGISTER WDT_TRIG *(0xe4)*

Note: this register must be written with the WDT password to reset the watchdog. No actual value is written in this register. Reads return all zero bits.

1.10 MSI – Machine Software Interrupt

Note: MSI has to be enabled by writing a 1 to `mie.MSIE`.

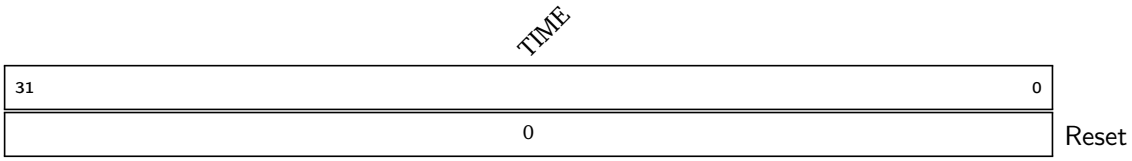


Register 1.35: MSI TRIGGER REGISTER MSI_TRIG *(0xec)*

TRIG Writing a 1 to this field will trigger an MSI. Writing a 0 will disarm the trigger.

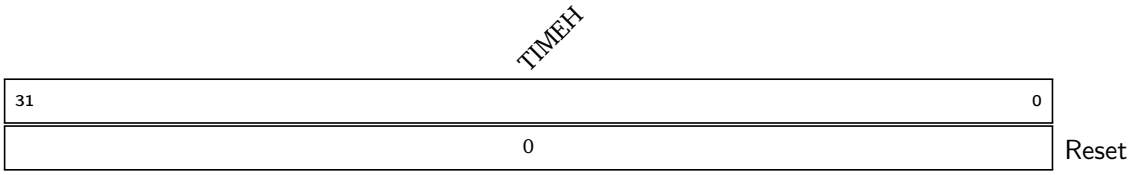
1.11 MTIME – RISC-V system timer

Note: the external timer interrupt has to be enabled by writing a 1 to `mie.MTIE`. Note: the external timer will assert a pending interrupt if TIMEH:TIME (viewed as a 64-bit register) is greater than or equal to TIMECMPH:TIMECPM (viewed as a 64-bit register). To negate the pending interrupt, set TIMECMPH:TIMECMP to a higher value than TIMEH:TIME. The TIMEH:TIME registers count the number of micro seconds since last reset. As such, the system clock frequency must be a integer multiple of 1 MHz.



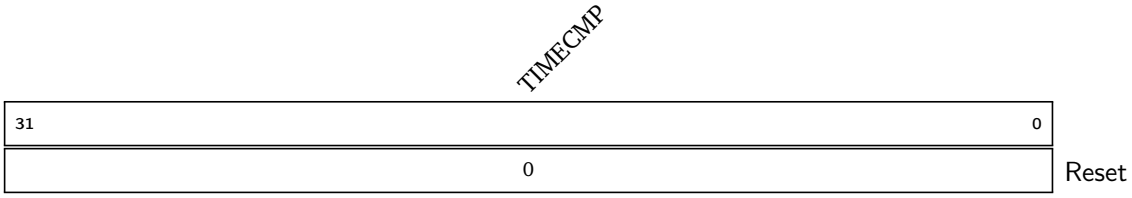
Register 1.36: TIME EXTERNAL TIMER REGISTER TIME *(0xf0)*

TIME This register holds the low 32 bits of the external timer. Currently read-only.



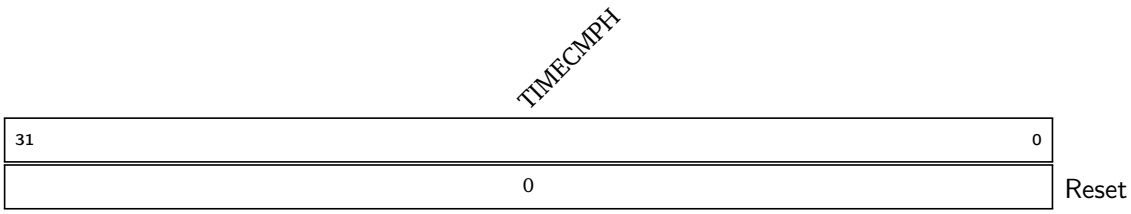
Register 1.37: TIMEH EXTERNAL TIMER REGISTER TIME *(0xf4)*

TIMEH This register holds the upper 32 bits of the external timer. Currently read-only.



Register 1.38: TIMECMP EXTERNAL TIMER COMPARE REGISTER TIMECMP *(0xf8)*

TIMECMP This register holds the low 32 bits of the external timer compare register.



Register 1.39: TIMECMPH EXTERNAL TIMER COMPARE REGISTER TIMECMP *(0xfc)*

TIMECMPH This register holds the upper 32 bits of the external timer compare register.