Digital Communications Lab

Laboratory report submitted for the partial fulfillment of the requirements for the degree of

Bachelor of Technology in Electronics and Communication Engineering

by

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Chapter 1

Experiment - 08

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Experiment No.: 08

1 Aim

1. Implement BPSK Modulation and carrier recovery using square-loop method.

2 Apparatus Used

1. ICs: LM741 5. 7476 (J-K Flip Flop IC) 8. 565 (PLL) 11. BJT [BC547, BC557]

2. Diode 6. Resistance 9. Capacitor 12. Breadboard

3. DC power supply 7. Connecting wires 10. DSO Probe 13. Function Generator

4. Digital signal oscilloscope

3 Theory

3.1 Connection Diagram

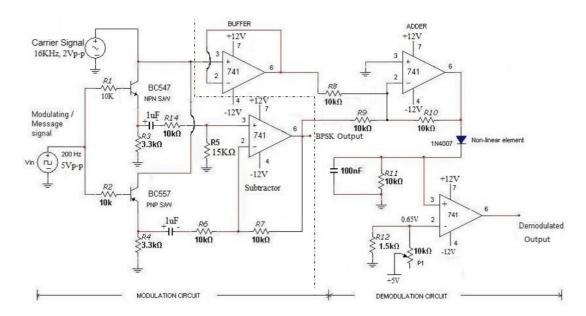


Figure 1: BPSK Modulation and Demodulation

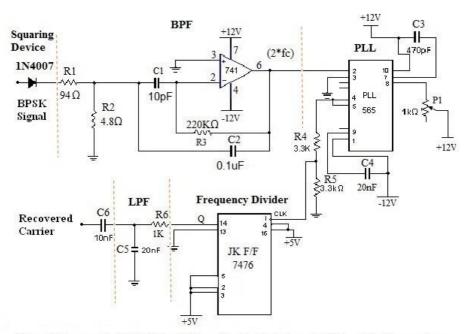
4 Procedure

- 1. Connect the circuit as given in Figure 1.
- 2. Give Square wave as a message signal of $5V_{pp}$ and 200Hz at the base of NPN and PNP BJT switches as shown in Figure 1. Give sinusoidal carrier signal of 16KHz and $2V_{pp}$ at the collector of NPN BJT switch.
- 3. Observe BPSK Modulated output after Subtractor. Draw it on your copy.
- 4. Observe BPSK Demodulated output and draw it in your copy, compare it with message signal.
- 5. Now connect circuit as shown in Fig. 2.



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Note:- First connection LM565 circuit. Now adjust the Potentiometer P1 to get the free running frequency 32 KHz. Then you will complete remaining circuit.

Figure 2: Carrier Recovery

- 6. Give BPSK Modulated signal at the input of diode (Fig 2). Observe output after each stage of Figure 2 and compare recovered carrier with original carrier signal. Draw it in your copy with proper specification.
- 7. Now disconnect carrier input at demodulator circuit (Fig 1) and connect recovered carrier signal.
- 8. Observe demodulated output and draw it.

5 Analysis of Results

6 Conclusions

Precautions

- 1. Check the connections before switching on the kit.
- 2. Connections should be done properly.
- 3. Observation should be taken properly.

1.1 Observations

1.1.1 Result Screenshots

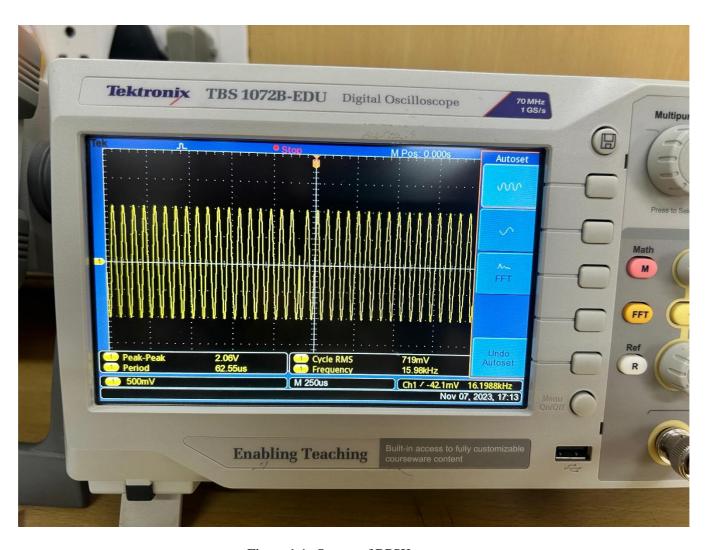


Figure 1.1: Output of BPSK

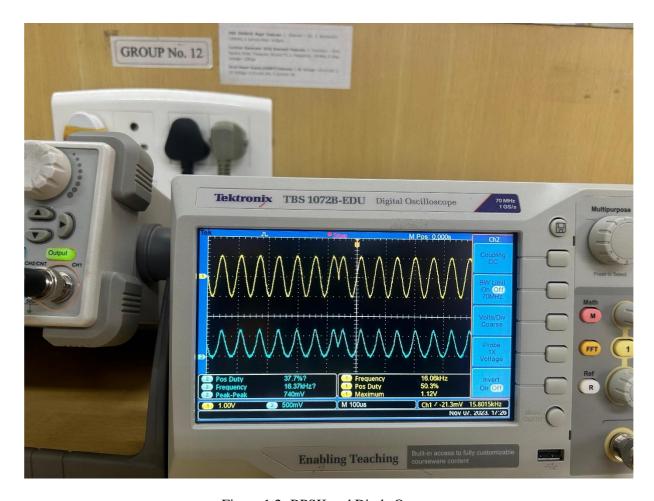


Figure 1.2: BPSK and Diode Output

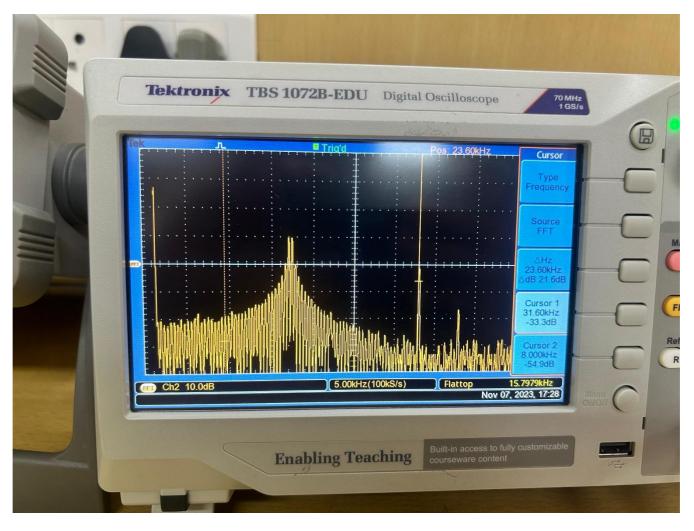


Figure 1.3: FFT of Diode with Center at 32kHz.

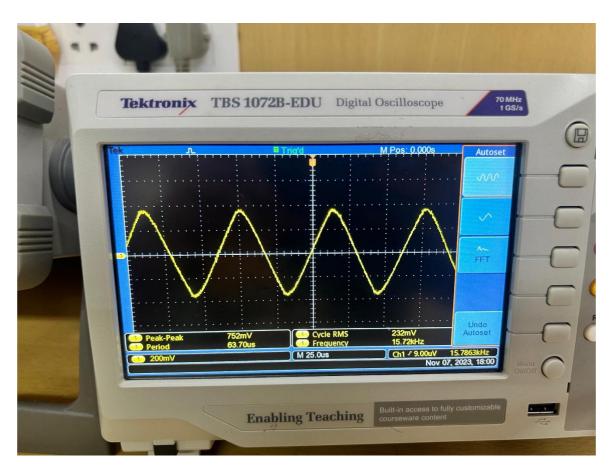


Figure 1.4: BPF Output at Pin 6

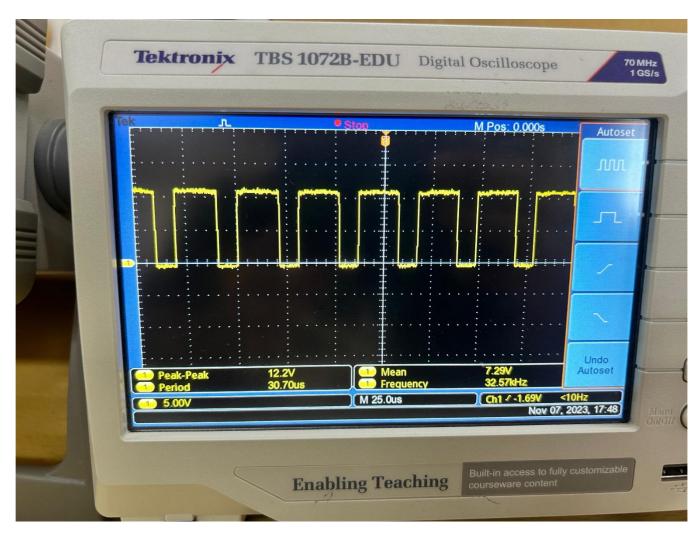


Figure 1.5: PLL Free Running Frequency at 32kHz.

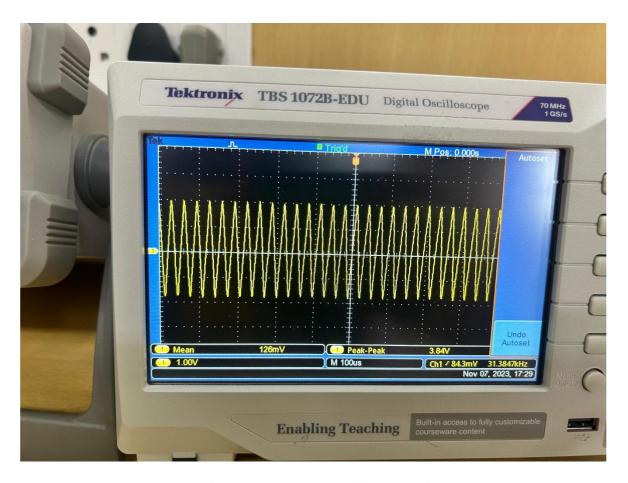


Figure 1.6: PLL output with Input at pin 2

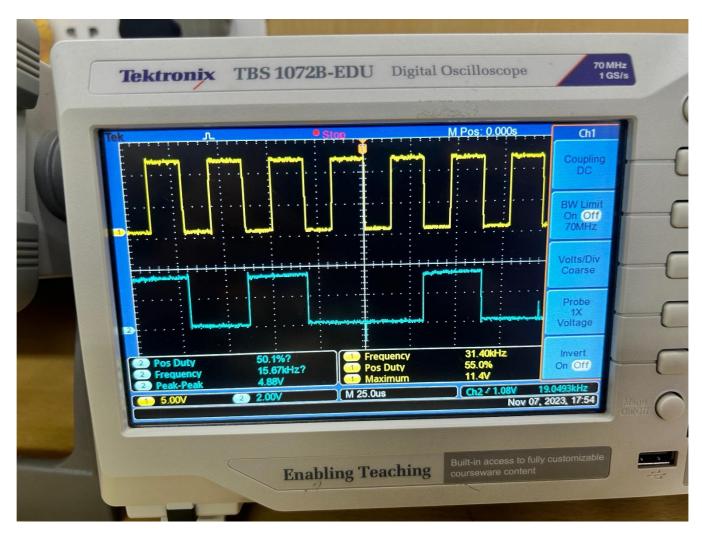


Figure 1.7: Frequency Divider

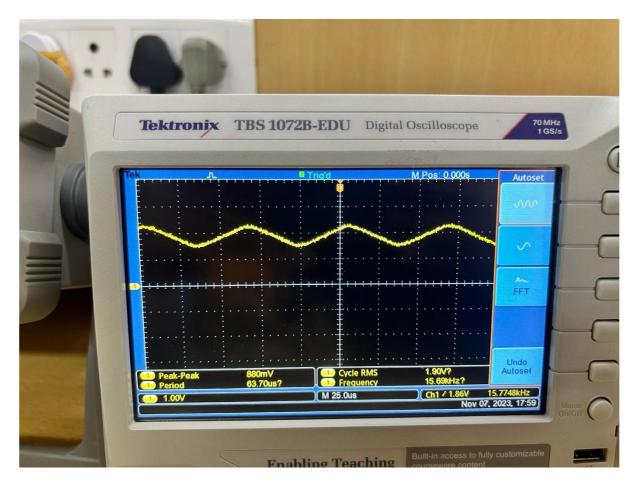


Figure 1.8: Output of 2nd order LPF

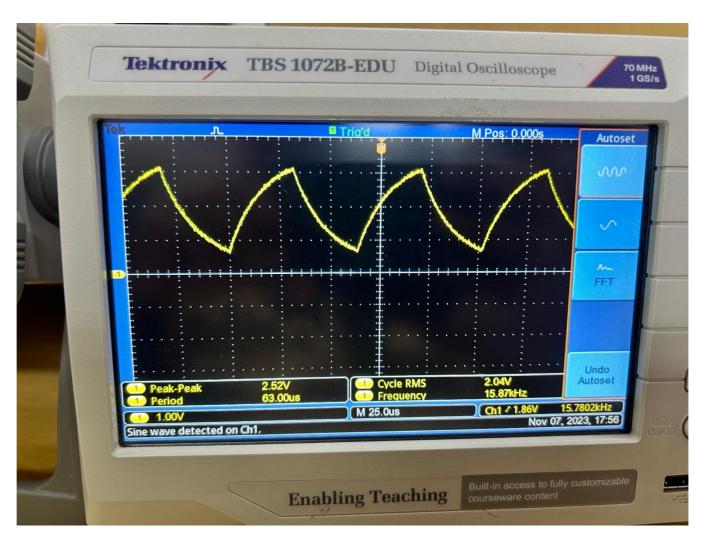


Figure 1.9: Recovered Carrier

1.2 Precautions

- 1. Check the connections before switching on the kit.
- 2. Connections should be done properly.
- 3. Observation should be taken properly.