



DesignWare DW_apb_i2c Databook

DW_apb_i2c – **Product Code**

Copyright Notice and Proprietary Information Notice

© 2015 Synopsys, Inc. All rights reserved. This software and documentation contain confidential and proprietary information that is the property of Synopsys, Inc. The software and documentation are furnished under a license agreement and may be used or copied only in accordance with the terms of the license agreement. No part of the software and documentation may be reproduced, transmitted, or translated, in any form or by any means, electronic, mechanical, manual, optical, or otherwise, without prior written permission of Synopsys, Inc., or as expressly provided by the license agreement.

Destination Control Statement

All technical data contained in this publication is subject to the export control laws of the United States of America. Disclosure to nationals of other countries contrary to United States law is prohibited. It is the reader's responsibility to determine the applicable regulations and to comply with them.

Disclaimer

SYNOPSYS, INC., AND ITS LICENSORS MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

Trademarks

Synopsis and certain Synopsis product names are trademarks of Synopsis, as set forth at <http://www.synopsys.com/Company/Pages/Trademarks.aspx>.

All other product or company names may be trademarks of their respective owners.

Synopsis, Inc.
690 E. Middlefield Road
Mountain View, CA 94043
www.synopsys.com

Contents

Preface	9
Revision History	13
Chapter 1	
Product Overview	17
1.1 DesignWare System Overview	17
1.2 General Product Description	19
1.2.1 DW_apb_i2c Block Diagram	19
1.3 Features	20
1.3.1 I ² C Features	20
1.3.2 DesignWare APB Slave Interface	21
1.4 Standards Compliance	21
1.5 Verification Environment Overview	21
1.6 Licenses	21
Chapter 2	
Building and Verifying a Component or Subsystem	23
2.1 Setting up Your Environment	23
2.2 Overview of the coreConsultant Configuration and Integration Process	24
2.2.1 coreConsultant Usage	24
2.2.2 Configuring the DW_apb_i2c within coreConsultant	26
2.2.3 Creating Gate-Level Netlists within coreConsultant	26
2.2.4 Verifying the DW_apb_i2c within coreConsultant	26
2.2.5 Running Leda on Generated Code with coreConsultant	26
2.2.6 Running SpyGlass® Lint and SpyGlass® CDC	26
2.3 Overview of the coreAssembler Configuration and Integration Process	30
2.3.1 coreAssembler Usage	30
2.3.2 Configuring the DW_apb_i2c within a Subsystem	33
2.3.3 Creating Gate-Level Netlists within coreAssembler	34
2.3.4 Verifying the DW_apb_i2c within coreAssembler	34
2.3.5 Running Leda on Generated Code with coreAssembler	34
2.3.6 Running Spyglass on Generated Code with coreAssembler	34
2.4 Database Files	34
2.4.1 Design/HDL Files	34
2.4.2 Synthesis Files	36
2.4.3 Verification Reference Files	36
Chapter 3	
Functional Description	37

3.1 Overview	37
3.2 I ² C Terminology	40
3.2.1 I ² C Bus Terms	40
3.2.2 Bus Transfer Terms	41
3.3 I ² C Behavior	41
3.3.1 START and STOP Generation	42
3.3.2 Combined Formats	42
3.4 I ² C Protocols	43
3.4.1 START and STOP Conditions	43
3.4.2 Addressing Slave Protocol	44
3.4.3 Transmitting and Receiving Protocol	45
3.4.4 START BYTE Transfer Protocol	47
3.5 Tx FIFO Management and START, STOP and RESTART Generation	48
3.5.1 Tx FIFO Management When IC_EMPTYFIFO_HOLD_MASTER_EN = 0	48
3.5.2 Tx FIFO Management When IC_EMPTYFIFO_HOLD_MASTER_EN = 1	49
3.6 Multiple Master Arbitration	53
3.7 Clock Synchronization	55
3.8 Operation Modes	56
3.8.1 Slave Mode Operation	56
3.8.2 Master Mode Operation	60
3.8.3 Disabling DW_apb_i2c	62
3.8.4 Aborting I2C Transfers	63
3.9 Spike Suppression	64
3.10 Fast Mode Plus Operation	65
3.11 Bus Clear Feature	66
3.11.1 SDA Line Stuck at LOW Recovery	66
3.11.2 SCL Line is Stuck at LOW	67
3.12 Device ID	67
3.13 Ultra-Fast Speed Mode	68
3.14 SMBus/PMBus	69
3.14.1 tTimeout,MIN Parameter	69
3.14.2 Master Device Clock Extension	69
3.14.3 Slave Device Clock Extension	70
3.14.4 SMBDAT Low Timeout	70
3.14.5 Bus Protocols	70
3.14.6 SMBUS Address Resolution Protocol	72
3.14.7 SMBUS Additional Slave Address	77
3.14.8 SMBUS Optional Signals	78
3.15 IC_CLK Frequency Configuration	79
3.15.1 Minimum High and Low Counts in SS, FS, FM+ and HS Modes With IC_CLK_FREQ_OPTIMIZATION = 0	80
3.15.2 Minimum High and Low Counts in SS, FS, FM+ and HS Modes With IC_CLK_FREQ_OPTIMIZATION = 1	82
3.15.3 Minimum High and Low counts in Ultra-Fast mode (IC_ULTRA_FAST_MODE = 1)	82
3.15.4 Minimum IC_CLK Frequency	82
3.16 SDA Hold Time	90
3.16.1 SDA Hold Timings in Receiver	91
3.16.2 SDA Hold Timings in Transmitter	92
3.17 DMA Controller Interface	93

3.17.1 Enabling the DMA Controller Interface	94
3.17.2 Overview of Operation	94
3.17.3 Transmit Watermark Level and Transmit FIFO Underflow	96
3.17.4 Choosing the Transmit Watermark Level	96
3.17.5 Selecting DEST_MSIZE and Transmit FIFO Overflow	98
3.17.6 Receive Watermark Level and Receive FIFO Overflow	98
3.17.7 Choosing the Receive Watermark level	99
3.17.8 Selecting SRC_MSIZE and Receive FIFO Underflow	99
3.17.9 Handshaking Interface Operation	99
3.18 APB Interface	103
Chapter 4	
Parameters	105
4.1 Parameter Descriptions	105
4.2 Configuration Parameters	105
Chapter 5	
Signal Descriptions	125
Chapter 6	
Registers	153
6.1 Register Memory Map	153
6.2 Operation of Interrupt Registers	160
6.3 Registers and Field Descriptions	161
6.3.1 IC_CON	161
6.3.2 IC_TAR	168
6.3.3 IC_SAR	171
6.3.4 IC_HS_MADDR	171
6.3.5 IC_DATA_CMD	173
6.3.6 IC_SS_SCL_HCNT	175
6.3.7 IC_SS_SCL_LCNT	176
6.3.8 IC_FS_SCL_HCNT	177
6.3.9 IC_FS_SCL_LCNT	178
6.3.10 IC_HS_SCL_HCNT	179
6.3.11 IC_HS_SCL_LCNT	180
6.3.12 IC_INTR_STAT	182
6.3.13 IC_INTR_MASK	183
6.3.14 IC_RAW_INTR_STAT	186
6.3.15 IC_RX_TL	190
6.3.16 IC_TX_TL	191
6.3.17 IC_CLR_INTR	192
6.3.18 IC_CLR_RX_UNDER	192
6.3.19 IC_CLR_RX_OVER	193
6.3.20 IC_CLR_TX_OVER	193
6.3.21 IC_CLR_RD_REQ	194
6.3.22 IC_CLR_TX_ABRT	194
6.3.23 IC_CLR_RX_DONE	195
6.3.24 IC_CLR_ACTIVITY	195
6.3.25 IC_CLR_STOP_DET	196
6.3.26 IC_CLR_START_DET	196

6.3.27 IC_CLR_GEN_CALL	197
6.3.28 IC_ENABLE	198
6.3.29 IC_STATUS	201
6.3.30 IC_TXFLR	205
6.3.31 IC_RXFLR	206
6.3.32 IC_SDA_HOLD	207
6.3.33 IC_TX_ABRT_SOURCE	208
6.3.34 IC_SLV_DATA_NACK_ONLY	214
6.3.35 IC_DMA_CR	215
6.3.36 IC_DMA_TDLR	216
6.3.37 IC_DMA_RDLR	217
6.3.38 IC_SDA_SETUP	218
6.3.39 IC_ACK_GENERAL_CALL	219
6.3.40 IC_ENABLE_STATUS	220
6.3.41 IC_FS_SPKLEN	222
6.3.42 IC_HS_SPKLEN	223
6.3.43 IC_CLR_RESTART_DET	224
6.3.44 IC_COMP_PARAM_1	225
6.3.45 IC_COMP_VERSION	227
6.3.46 IC_COMP_TYPE	227
6.3.47 IC_SCL_STUCK_AT_LOW_TIMEOUT	228
6.3.48 IC_SDA_STUCK_AT_LOW_TIMEOUT	228
6.3.49 IC_CLR_SCL_STUCK_DET	229
6.3.50 IC_DEVICE_ID	230
6.3.51 IC_UFM_SCL_HCNT	231
6.3.52 IC_UFM_SCL_LCNT	232
6.3.53 IC_UFM_SPKLEN	232
6.3.54 IC_UFM_TBUF_CNT	234
6.3.55 IC_SMBUS_CLOCK_LOW_SEXT	235
6.3.56 IC_SMBUS_CLOCK_LOW_MEXT	235
6.3.57 IC_SMBUS_THIGH_MAX_IDLE_COUNT	236
6.3.58 IC_SMBUS_INTR_STAT	237
6.3.59 IC_SMBUS_INTR_MASK	239
6.3.60 IC_SMBUS_INTR_RAW_STATUS	241
6.3.61 IC_CLR_SMBUS_INTR	243
6.3.62 IC_OPTIONAL_SAR	244
6.3.63 IC_SMBUS_UDID_LSB	245
 Chapter 7 Internal Parameter Descriptions	247
 Chapter 8 Programming the DW_apb_i2c	249
8.1 Software Registers	249
8.2 Software Drivers	249
8.3 Programming Example	250
8.4 Programming Flow for SCL and SDA Bus Recovery	256
8.5 Programming Flow for Reading the Device ID	257
8.6 Programming Flow for SMBUS Timeout in Master Mode	258

8.7 Programming Flow for SMBUS Timeout in Slave Mode	259
8.8 ARP Master Programming Flow	260
8.9 ARP Slave Programming Flow	260
8.10 SMBus SUSPEND Programming Flow in Host Mode	263
8.11 SMBus SUSPEND Programming Flow in Device Mode	264
8.12 SMBus ALERT Programming Flow in Host Mode	265
8.13 SMBus ALERT Programming Flow in Device Mode	266
8.14 Programming Flow Of DW_apb_i2c in Ultra-Fast Mode	267
8.14.1 DW_apb_i2c Master Mode	267
8.14.2 DW_apb_i2c Slave Mode	268
Chapter 9	
Verification	269
9.1 Overview of Vera Tests	269
9.1.1 APB Slave Interface	269
9.1.2 DW_apb_i2c Master Operation	270
9.1.3 DW_apb_i2c Slave Operation	270
9.1.4 DW_apb_i2c Interrupts	271
9.1.5 DMA Handshaking Interface	271
9.1.6 DW_apb_i2c Dynamic IC_TAR and IC_10BITADDR_MASTER Update	271
9.1.7 Generate NACK as a Slave-Receiver	271
9.1.8 SCL Held Low for Duration Specified in IC_SDA_SETUP	271
9.1.9 Generate ACK/NACK for General Call	271
9.2 Overview of DW_apb_i2c Testbench	272
Chapter 10	
Integration Considerations	275
10.1 Accessing Top-level Constraints	275
10.1.1 Area	275
10.1.2 Power Consumption	276
Appendix A	
Synchronizer Methods	279
A.1 Synchronizers Used in DW_apb_i2c	280
A.2 Synchronizer 1: Simple Double Register Synchronizer	281
A.3 Synchronizer 2: Simple Double Register Synchronizer with Configurable Polarity Reset	281
Appendix B	
Glossary	283
Index	287

Preface

This databook provides information that you need to interface the DW_apb_i2c to the Advanced Peripheral Bus (APB). The DW_apb_i2c conforms to the [AMBA Specification, Revision 2.0](#) from ARM.

The information in this databook includes an overview, pin and parameter descriptions, a memory map, and functional behavior of the component. An overview of the testbench, a description of the tests that are run to verify the coreKit, and synthesis information for the component are also provided.

Organization

The chapters of this databook are organized as follows:

- Chapter 1, “[Product Overview](#)” provides a system overview, a component block diagram, basic features, and an overview of the verification environment.
- Chapter 2, “[Building and Verifying a Component or Subsystem](#)” introduces you to using the DW_apb_i2c within the coreAssembler and coreConsultant tools.
- Chapter 3, “[Functional Description](#)” describes the functional operation of the DW_apb_i2c.
- Chapter 4, “[Parameters](#)” identifies the configurable parameters supported by the DW_apb_i2c.
- Chapter 5, “[Signal Descriptions](#)” provides a list and description of the DW_apb_i2c signals.
- Chapter 6, “[Registers](#)” describes the programmable registers of the DW_apb_i2c.
- Chapter 7, “[Internal Parameter Descriptions](#)” provides a list of internal parameter descriptions that might be indirectly referenced in expressions in the Signals chapter.
- Chapter 8, “[Programming the DW_apb_i2c](#)” provides information needed to program the configured DW_apb_i2c.
- Chapter 9, “[Verification](#)” provides information on verifying the configured DW_apb_i2c.
- Chapter 10, “[Integration Considerations](#)” includes information you need to integrate the configured DW_apb_i2c into your design.
- Chapter A, “[Synchronizer Methods](#)” documents the synchronizer methods (blocks of synchronizer functionality) used in DW_apb_i2c to cross clock boundaries.
- Appendix B, “[Glossary](#)” provides a glossary of general terms.

Related Documentation

- [DW_apb_i2c Driver Kit User Guide](#) – Contains information on the Driver Kit for the DW_apb_i2c; requires source code license (DWC-APB-Periph-Source)
- [Using DesignWare Library IP in coreAssembler](#) – Contains information on getting started with using DesignWare SIP components for AMBA 2 and AMBA 3 AXI components within coreTools
- [coreAssembler User Guide](#) – Contains information on using coreAssembler
- [coreConsultant User Guide](#) – Contains information on using coreConsultant

To see a complete listing of documentation within the DesignWare Synthesizable Components for AMBA 3 AXI, refer to the [Guide to Documentation for DesignWare Synthesizable Components for AMBA 2 and AMBA 3 AXI](#).

Web Resources

- DesignWare IP product information: <http://www.designware.com>
- Your custom DesignWare IP page: <http://www.mydesignware.com>
- Documentation through SolvNet: <http://solvnet.synopsys.com> (Synopsys password required)
- Synopsys Common Licensing (SCL): <http://www.synopsys.com/keys>

Customer Support

To obtain support for your product:

- First, prepare the following debug information, if applicable:
 - For environment setup problems or failures with configuration, simulation, or synthesis that occur within coreConsultant or coreAssembler, use the following menu entry:

File > Build Debug Tar-file

Check all the boxes in the dialog box that apply to your issue. This menu entry gathers all the Synopsys product data needed to begin debugging an issue and writes it to the file `<core tool startup directory>/debug.tar.gz`.
 - For simulation issues outside of coreConsultant or coreAssembler:
 - Create a waveforms file (such as VPD or VCD)
 - Identify the hierarchy path to the DesignWare instance
 - Identify the timestamp of any signals or locations in the waveforms that are not understood
- Then, contact Support Center, with a description of your question and supplying the above information, using one of the following methods:
 - *For fastest response*, use the SolvNet website. If you fill in your information as explained below, your issue is automatically routed to a support engineer who is experienced with your product. The **Sub Product** entry is critical for correct routing.

Go to <http://solvnet.synopsys.com/EnterACall> and click on the link to enter a call. Provide the requested information, including:

- **Product:** DesignWare Library IP
- **Sub Product:** AMBA
- **Tool Version:** <product version number>
- **Problem Type:**
- **Priority:**
- **Title:** DW_apb_i2c
- **Description:** For simulation issues, include the timestamp of any signals or locations in waveforms that are not understood

After creating the case, attach any debug files you created in the previous step.

- Or, send an e-mail message to support_center@synopsys.com (your email will be queued and then, on a first-come, first-served basis, manually routed to the correct support engineer):
 - Include the Product name, Sub Product name, and Tool Version number in your e-mail (as identified above) so it can be routed correctly.
 - For simulation issues, include the timestamp of any signals or locations in waveforms that are not understood
 - Attach any debug files you created in the previous step.
- Or, telephone your local support center:
 - North America:
Call 1-800-245-8005 from 7 AM to 5:30 PM Pacific time, Monday through Friday.
 - All other countries:
<http://www.synopsys.com/Support/GlobalSupportCenters>

Product Code

Table 1-1 lists all the components associated with the product code for DesignWare APB Advanced Peripherals.

Table 1-1 DesignWare APB Advanced Peripherals – Product Code: 3772-0

Component Name	Description
DW_apb_i2c	A highly configurable, programmable master or slave i2c device with an APB slave interface
DW_apb_i2s	A configurable master or slave device for the three-wire interface (I2S) for streaming stereo audio between devices
DW_apb_ssi	A configurable, programmable, full-duplex, master or slave synchronous serial interface
DW_apb_uart	A programmable and configurable Universal Asynchronous Receiver/Transmitter (UART) for the AMBA 2 APB bus

Revision History

This table shows the revision history for the databook from release to release. This is being tracked from version 1.08a onward.

Version	Date	Description
2.00a	June 2015	<p>Added:</p> <ul style="list-style-type: none"> ■ “Running SpyGlass® Lint and SpyGlass® CDC” on page 26 ■ “Running Spyglass on Generated Code with coreAssembler” on page 34 ■ “Internal Parameter Descriptions” on page 247 ■ New features: <ul style="list-style-type: none"> - “Bus Clear Feature” on page 66 - “Device ID” on page 67 - “SMBus/PMBus” on page 69 - “Ultra-Fast Speed Mode” on page 68 - New parameter “IC_CLK_FREQ_OPTIMIZATION” - Synchronizer Methods ■ Included a note regarding tBUF timing and setup/hold time. <p>Updated:</p> <ul style="list-style-type: none"> - “IC_CLK Frequency Configuration” on page 79 updated for IC_CLK_FREQ_OPTIMIZATION and IC_ULTRA_FAST_MODE Configurations - “Signal Descriptions” on page 125 auto-extracted from the RTL
1.22a	June 2014	<p>Added:</p> <ul style="list-style-type: none"> ■ New features: <ul style="list-style-type: none"> - Blocking the Tx FIFO commands using IC_TX_CMD_BLOCK field in IC_ENABLE register - Indication for first data byte received after the address in IC_DATA_CMD register - Detection of STOP interrupt only if master is active ■ coreConsultant parameter (IC_AVOID_RX_FIFO_FLUSH_ON_TX_ABRT) introduced to avoid flushing of RX FIFO during TX Abort ■ New bits in IC_STATUS register for Indicating a reason for bus holding ■ Performance section in Integration considerations <p>Updated:</p> <ul style="list-style-type: none"> ■ Width of TX_FLUSH_CNT field in the IC_TX_ABRT_SOURCE register ■ Default Input/Output Delays in Signals chapter

(Continued)

Version	Date	Description
1.21a	May 2013	<p>Added:</p> <ul style="list-style-type: none"> ■ Section on Fast Mode Plus ■ Configuration Parameters: <ul style="list-style-type: none"> - IC_RX_FULL_HLD_BUS_EN - IC_SLV_RESTART_DET_EN ■ Signals: <ul style="list-style-type: none"> - ic_restart_det_intr(_n) signal to enable restart detect in slave mode ■ Registers <ul style="list-style-type: none"> - RESTART_DET bit of IC_INTR_STAT, IC_INTR_MASK and IC_RAW_INTR_STAT registers Bit detects a repeated start when the DW_apb_i2c is the addressed slave - IC_CLR_RESTART_DET to clear the RESTART_DET interrupt - MST_ON_HOLD bit to the IC_INTR_STAT, IC_INTR_MASK and IC_RAW_INTR_STAT registers. This bit indicates whether a master is holding the bus and the Tx FIFO is empty. Added the signal ic_mst_on_hold_intr(_n) ■ Programming flow for DW_apb_i2c master with TAR update
1.21a <i>Cont'd</i>	May 2013 <i>Cont'd</i>	<p><i>Continued</i></p> <p>Updated:</p> <ul style="list-style-type: none"> ■ References to Fast Mode Plus ■ Registers: <ul style="list-style-type: none"> - TX_FLUSH_CNT field of the IC_TX_ABRT_SOURCE register - TX_ABRT field of the IC_RAW_INTR_STAT register - IC_CON - IC_RAW_INTR_STAT - IC_SDA_HOLD Signals: <ul style="list-style-type: none"> ■ Active state of the ic_current_src_en signal ■ Programming flow for DW_apb_i2c as master in standard or fast mode ■ Method for deriving ic_clk values in high-speed modes ■ Documentation template Removed: <ul style="list-style-type: none"> ■ Text stating that Fast Mode Plus is not supported ■ Note in the IC_TX_ABRT_SOURCE register description stating DW_apb_i2c can be a master and slave at the same time
1.20a	Oct 2012	Added the product code on the cover and in Table 1-1.
1.20a	June 2012	Edited calculations for driving SDA in "High-Speed Modes" section; updated IC_ENABLE and IC_TX_ABRT_SOURCE registers.
1.17a	Mar 2012	Enhanced DW_ahb_dmac and DW_apb_i2c programming example; updated definition of IC_FS_SPKLEN and IC_HS_SPKLEN register descriptions; corrected programming values for dma_tx_req and dma_rx_req signals.

(Continued)

Version	Date	Description
1.16b	Dec 2011	Enhanced description of IC_ADD_ENCODED_PARAMS parameter.
1.16b	Nov 2011	Version change for 2011.11a release.
1.16a	Oct 2011	Version change for 2011.10a release.
1.15a	14 June 2011	Removed “Digital/Analog Domain Functional Partitioning” section (9.1) – irrelevant now with Spike Suppression functionality.
1.15a	June 2011	Updated system diagram in Figure 1-1; enhanced description of ic_rst_n signal; enhanced “Related Documents” section in Preface.
1.15a	21 Apr 2011	Clarified description of C_DEFAULT_SDA_HOLD parameter.
1.15a	12 Apr 2011	Corrected IC_DEFAULT_FS_SPKLEN and IC_DEFAULT_HS_SPKLEN default values.
1.15a	Apr 2011	Added spike suppression material; corrected R/W locations in timing diagrams in “Tx FIFO Management and START, STOP and RESTART Generation” section
1.14a	Dec 2010	Corrected subsection numbering in Registers chapter.
1.13a	Oct 2010	Added information on calculating maximum value for IC_DEFAULT_SDA_HOLD parameter and IC_SDA_HOLD register; “SDA Hold Time” section, description of IC_DEFAULT_SDA_HOLD parameter, and IC_SDA_HOLD register updated
1.12a	7 Sep 2010	Corrected DW_ahb_dmac response in “Receive Watermark Level and Receive FIFO Overflow” section
1.12a	Sep 2010	Corrected names of include files and vcs command used for simulation
1.11a	Mar 2010	Corrected information regarding how DW_apb_i2c communicates with slaves when operating in master mode; corrected default value for IC_DEFAULT_SDA_SETUP parameter; added SDA hold time information; added IC_SDA_HOLD register description; removed references to 300ns hold time in integration considerations; removed DW_apb_i2c Application Notes appendix.
1.10a	Jan 2010	Removed reference to I2C protocol created by Philips (NXP).
1.10a	Dec 2009	Corrected dependencies for IC_SS_SCL_HIGH_COUNT, IC_SS_SCL_LOW_COUNT, IC_FS_SCL_HIGH_COUNT, and IC_FS_SCL_LOW_COUNT parameters; corrected IC_RESTART_EN parameter description; modified description of IC_SDA_SETUP register; updated databook to new template for consistency with other IIP/VIP/PHY databooks.
1.10a	Jul 2009	Corrected equations for avoiding underflow when programming a source burst transaction.
1.10a	Jun 2009	Corrected name of IC_10BITADDR_SLAVE parameter in “Parameters” chapter.
1.10a	May 2009	Removed references to QuickStarts, as they are no longer supported.
1.10a	24 Apr 2009	Enhanced IC_CON description with table for IC_SLAVE_DISABLE and MASTER_MODE combinations that result in configuration errors.

(Continued)

Version	Date	Description
1.10a	23 Apr 2009	Enhanced “Master Transmit and Master Receive” subsection to clarify reads for multiple bytes.
1.10a	Oct 2008	IC_RX_FULL_GEN_NACK parameter removed; IC_INTR_MASK is active low; dependency changed for IC_HS_MASTER_CODE parameter; IC_SLAVE_DISABLE default changed to 1; values for HS mode corrected in Table 8; debug_* signal default values corrected; version change for 2008.10a release.
1.09a	Jul 2008	Removed IC_RX_FULL_GEN_NACK configuration parameter and its conditional text. Changed reference to non-existent table for IC_*S_SCL_*CNT registers to link to “IC_CLK Frequency Configuration” section. Removed USE_FOUNDATION parameter.
1.09a	Jun 2008	Removed Synchronous value from IC_CLK_TYPE parameter; clarified that putting data into the FIFO generates a START and emptying the FIFO generates a STOP; clarified description of I2C_DYNAMIC_TAR_UPDATE parameter; clarification of IC_TAR description.
1.08b	11 Feb 2008	Modified note on restriction; page 47.

Product Overview

This chapter describes the DesignWare APB I²C Interface Peripheral, referred to as DW_apb_i2c. The DW_apb_i2c component is an AMBA 2.0-compliant Advanced Peripheral Bus (APB) slave device and is part of the family of DesignWare Synthesizable Components.

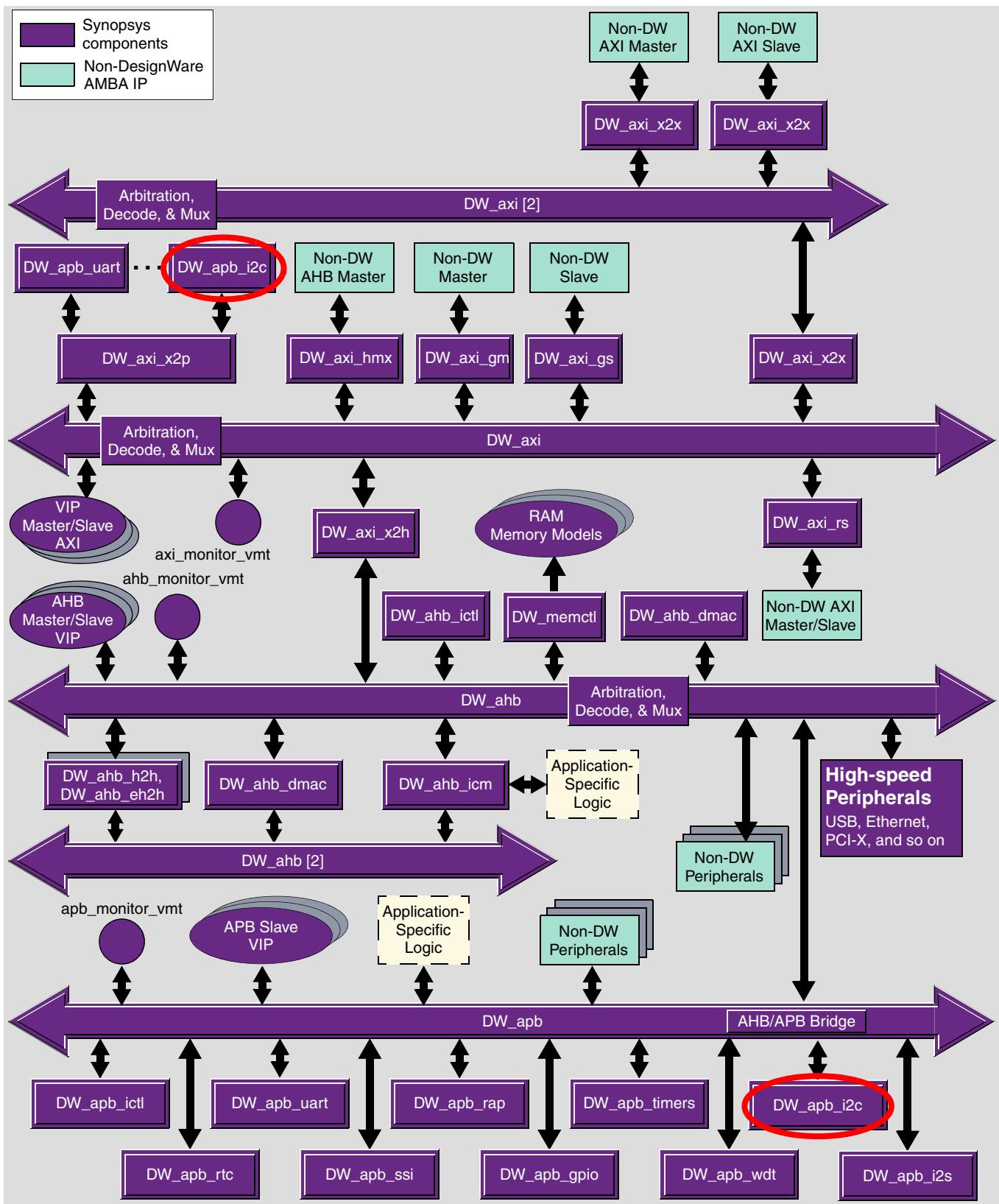
1.1 DesignWare System Overview

The Synopsys DesignWare Synthesizable Components environment is a parameterizable bus system containing AMBA version 2.0-compliant AHB (Advanced High-performance Bus) and APB (Advanced Peripheral Bus) components, and AMBA version 3.0-compliant AXI (Advanced eXtensible Interface) components.

[Figure 1-1](#) illustrates one example of this environment, including the AXI bus, the AHB bus, and the APB bus. Included in this subsystem are synthesizable IP for AXI/AHB/APB peripherals, bus bridges, and an AXI interconnect and AHB bus fabric. Also included are verification IP for AXI/AHB/APB master/slave models and bus monitors. In order to display the databook for a DW_* component, click on the corresponding component object in the illustration.



Links resolve only if you are viewing this databook from your \$DESIGNWARE_HOME tree, and to only those components that are installed in the tree.

Figure 1-1 Example of DW_apb_i2c in a Complete System

You can connect, configure, synthesize, and verify the DW_apb_i2c within a DesignWare subsystem using coreAssembler, documentation for which is available on the web in the [coreAssembler User Guide](#).

If you want to configure, synthesize, and verify a single component such as the DW_apb_i2c component, you might prefer to use coreConsultant, documentation for which is available in the [coreConsultant User Guide](#).

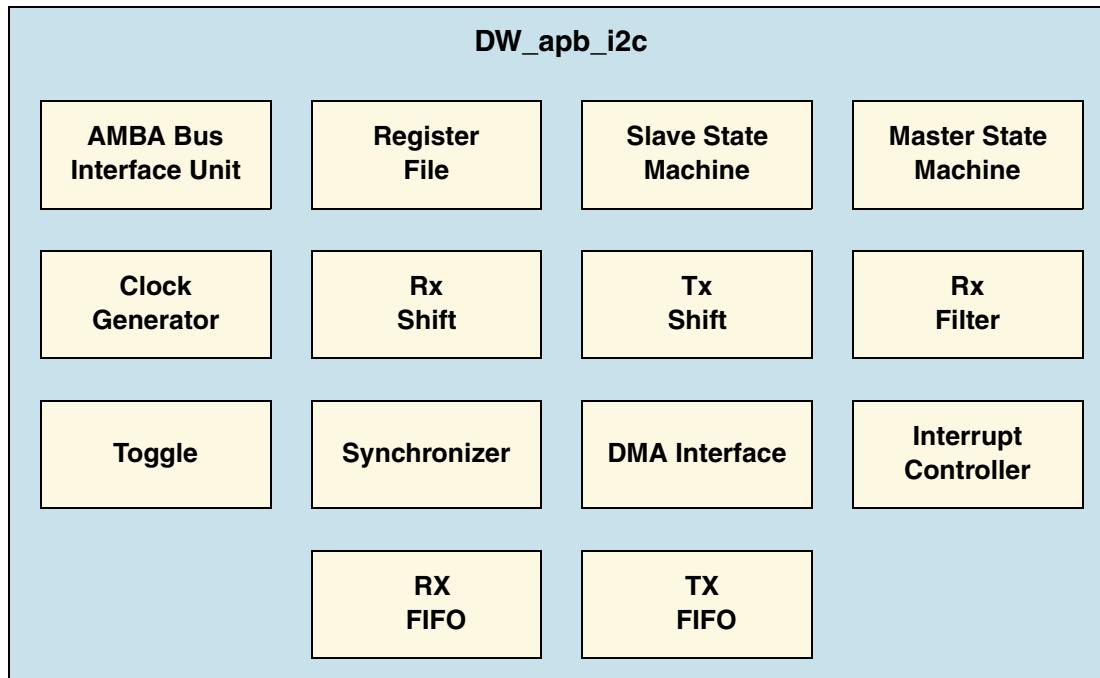
1.2 General Product Description

The DW_apb_i2c is a configurable, synthesizable, and programmable control bus that provides support for the communications link between integrated circuits in a system. It is a simple two-wire bus with a software-defined protocol for system control, which is used in temperature sensors and voltage level translators to EEPROMs, general-purpose I/O, A/D and D/A converters, CODECs, and many types of microprocessors.

1.2.1 DW_apb_i2c Block Diagram

Figure 1-2 illustrates a simple block diagram of DW_apb_i2c. For a more detailed block diagram and description of the component, refer to “Functional Description” on page 37.

Figure 1-2 Block Diagram of DW_apb_i2c



1.3 Features

DW_apb_i2c has the following features:

1.3.1 I²C Features

- Two-wire I²C serial interface – consists of a serial data line (SDA) and a serial clock (SCL)
- Three speeds:
 - Standard mode (0 to 100 Kb/s)
 - Fast mode (\leq 400 Kb/s) or fast mode plus (\leq 1000 Kb/s)¹
 - High-speed mode (\leq 3.4 Mb/s)
- Clock synchronization
- Master OR slave I²C operation
- 7- or 10-bit addressing
- 7- or 10-bit combined format transfers
- Bulk transmit mode
- Ignores CBUS addresses (an older ancestor of I²C that used to share the I²C bus)
- Transmit and receive buffers
- Interrupt or polled-mode operation
- Handles Bit and Byte waiting at all bus speeds
- Simple software interface consistent with DesignWare APB peripherals
- Component parameters for configurable software driver support
- DMA handshaking interface compatible with the DW_ahb_dmac handshaking interface
- Programmable SDA hold time (tHD;DAT)
- Bus clear feature
- Device ID feature
- SMBus/PMBus Support
- SMBus Slave detects and responds to ARP commands.
- Ultra-Fast mode support

The DW_apb_i2c requires external hardware components as support in order to be compliant in an I²C system. The descriptions are detailed later in this document.

It must also be noted that the DW_apb_i2c should only be operated either as (but not both):

- A master in an I²C system and programmed only as a Master; OR
- A slave in an I²C system and programmed only as a Slave.

1. In this document, references to fast mode also apply to fast mode plus, unless specifically stated otherwise.

1.3.2 DesignWare APB Slave Interface

- Support for APB data bus widths of 8, 16, and 32 bits
- Source code for this component is available on a per-project basis as a DesignWare Core; contact your local sales office for the details.

1.4 Standards Compliance

The DW_apb_i2c component conforms to the [AMBA Specification, Revision 2.0](#) from ARM. Readers are assumed to be familiar with this specification.

The DW_apb_i2c was designed for the following specifications:

- *I2C Bus Specification, Version 6.0*, dated April 2014
- *SMBus specification Version 3.0*, dated January 2015
- *PMBus Specification Version 1.2*, dated September 2010

1.5 Verification Environment Overview

The DW_apb_i2c includes an extensive verification environment, which sets up and invokes your selected simulation tool to execute tests that verify the functionality of the configured component. You can then analyze the results of the simulation.

The “[Verification](#)” on page [269](#) chapter discusses the specific procedures for verifying the DW_apb_i2c.

1.6 Licenses

Before you begin using the DW_apb_i2c, you must have a valid license. For more information, refer to the [DesignWare Synthesizable Components for AMBA 2/AMBA 3 AXI Installation Guide](#).

2

Building and Verifying a Component or Subsystem

DesignWare Synthesizable IP (SIP) components for AMBA 2 and AMBA 3 AXI are packaged using Synopsys coreTools, which enable the user to configure, synthesize, and run simulations on a single SIP title, or to build a configured AMBA subsystem. You do this by generating a workspace view using one of the following coreTools applications:

- coreConsultant – Used for configuration, RTL generation, synthesis, and execution of packaged verification for a single SIP title. The [coreConsultant User Guide](#) provides complete information on using coreConsultant.
- coreAssembler – Used for building and configuration of a subsystem that connects multiple SIP titles, RTL generation, synthesis, and creation of a template subsystem testbench. The [coreAssembler User Guide](#) provides complete information on using coreAssembler.

A workspace is your working version of a DesignWare SIP component or subsystem. In fact, you can create several workspaces to experiment with different design alternatives.



Hint If you are unfamiliar with coreTools—which is comprised of the coreAssembler, coreConsultant, and coreBuilder tools—you can go to [Using DesignWare Library IP in coreAssembler](#) to “get started” learning how to work with DesignWare SIP components.

2.1 Setting up Your Environment

The DW_apb_i2c is included in a release of DesignWare SIP components. It is assumed that you have already downloaded and installed the release. If you have not, you can download and install the latest versions of required tools using the [DesignWare Synthesizable Components for AMBA 2/AMBA 3 AXI Installation Guide](#).

You also need to set up your environment correctly using specific environment variables, such as DESIGNWARE_HOME, VERA_HOME, PATH, and SYNOPSYS. If you are not familiar with these requirements and the necessary licenses, refer to the [DesignWare Synthesizable Components for AMBA 2/AMBA 3 AXI Installation Guide](#).

2.2 Overview of the coreConsultant Configuration and Integration Process

Once you have correctly downloaded and installed a release of DesignWare SIP components and then set up your environment, you can begin work on the DW_apb_i2c using coreConsultant.

2.2.1 coreConsultant Usage

Figure 2-1 illustrates some general directories and files in a coreConsultant workspace.

Figure 2-1 coreConsultant Usage Flow

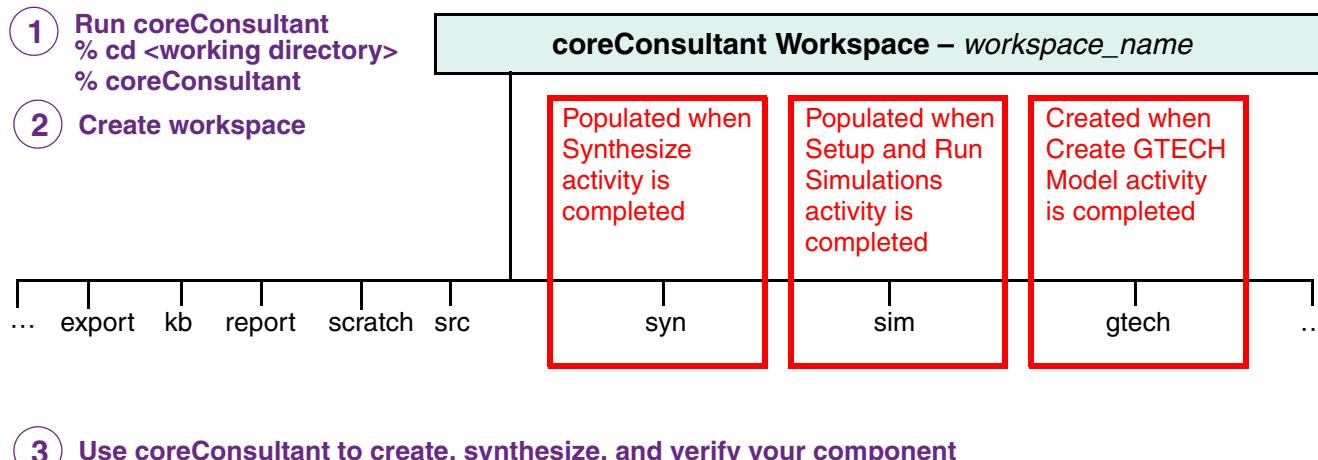


Table 2-1 provides a description of the implementation workspace directory and subdirectories.

Table 2-1 coreConsultant Implementation Workspace Directory Contents

Directory/Subdirectory	Description
auxiliary	Scripts and text files used by coreConsultant. Generated upon first creating workspace.
custom	Contains RTL preprocessor scripts. Generated during Specify Configuration activity.
doc	Contains local copies of component-specific databooks. Generated upon first creating workspace.
export	Contains files used to integrate results from the completed source configuration and synthesis activities into your design (outside coreConsultant). Generated upon first creating workspace; populated during Specify Configuration activity.
gtech	Contains synthesis scripts and output netlists from gtech generation; also used for RTL simulation of encrypted source code. Generated during Generate GTECH Model activity.

Table 2-1 coreConsultant Implementation Workspace Directory Contents (Continued)

Directory/Subdirectory	Description
kb	Contains knowledge base information used by coreConsultant. These are binary files containing the state of the design. Generated upon first creating workspace; populated and updated throughout activities.
leda	Contains Leda configuration files for the component. Generated upon first creating workspace; updated during Run Leda Coding Checker activity.
report	Contains all of the reports created by coreConsultant during build, configuration, test and synthesis phases. An index.html file in this directory links to many of these generated reports. Generated upon first creating workspace; populated and updated throughout activities.
scratch	Contains temp files used during the coreConsultant processes. Generated upon first creating workspace; populated and updated throughout activities.
sim	Contains test stimulus and output files. Generated upon first creating workspace; updated during Setup and Run Simulations activity.
spyglass	Contains SpyGlass Lint and CDC configuration files for the component. Generated upon first SpyGlass run; updated during Run Spyglass RTL Checker activity.
src	Includes the top-level RTL file, <i>design_name.v</i> . If you have a source license, this will contain plain-text RTL; if you only have a designware license, this will contain encrypted RTL. Generated upon first creating workspace; populated during Specify Configuration activity.
syn	Contains synthesis files for the component. Generated upon first creating workspace; updated during Synthesis activity and Formal Verification activity.
tcl	Contains synthesis intent scripts. Generated upon first creating workspace.

For details on some key files created during coreConsultant activities, refer to “[Database Files](#)” on page [34](#).

For information on using coreConsultant, refer to the [coreConsultant User Guide](#).

2.2.2 Configuring the DW_apb_i2c within coreConsultant

The “Parameters” chapter on [page 105](#) describes the DW_apb_i2c hardware configuration parameters that you configure using the coreConsultant GUI.

The “Creating the RTL View of a Core” chapter in the [coreConsultant User Guide](#) discusses how to specify a configuration for an individual component like the DW_apb_i2c.

2.2.3 Creating Gate-Level Netlists within coreConsultant

The “Creating the Gate-Level Netlist for a Core” chapter in the [coreConsultant User Guide](#) discusses how to create a translation of the RTL view into a technology-specific netlist for an individual component like the DW_apb_i2c.

2.2.4 Verifying the DW_apb_i2c within coreConsultant

The “Verification” chapter on [page 269](#) provides an overview of the testbench available for DW_apb_i2c verification using the coreConsultant GUI.

The “Verifying Your Implementation” chapter in the [coreConsultant User Guide](#) discusses how to simulate an individual component like the DW_apb_i2c.

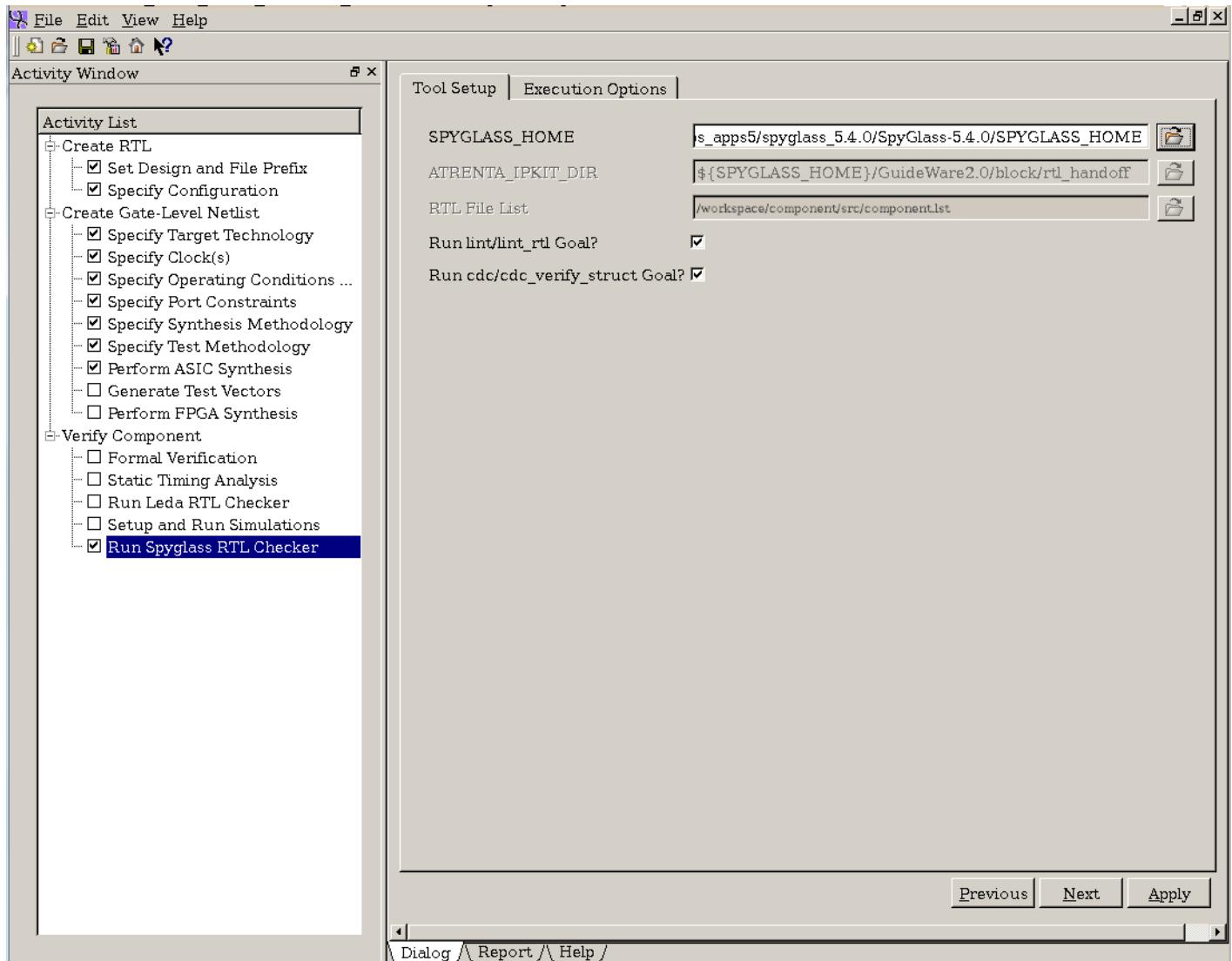
2.2.5 Running Leda on Generated Code with coreConsultant

When you select **Verify Component > Run Leda Coding Checker** from the Activity List, the corresponding Activity View appears. In this Activity View you select rules configuration file and define Leda command line switches.

2.2.6 Running SpyGlass® Lint and SpyGlass® CDC

This section discusses the procedure to run SpyGlass Lint and SpyGlass CDC.

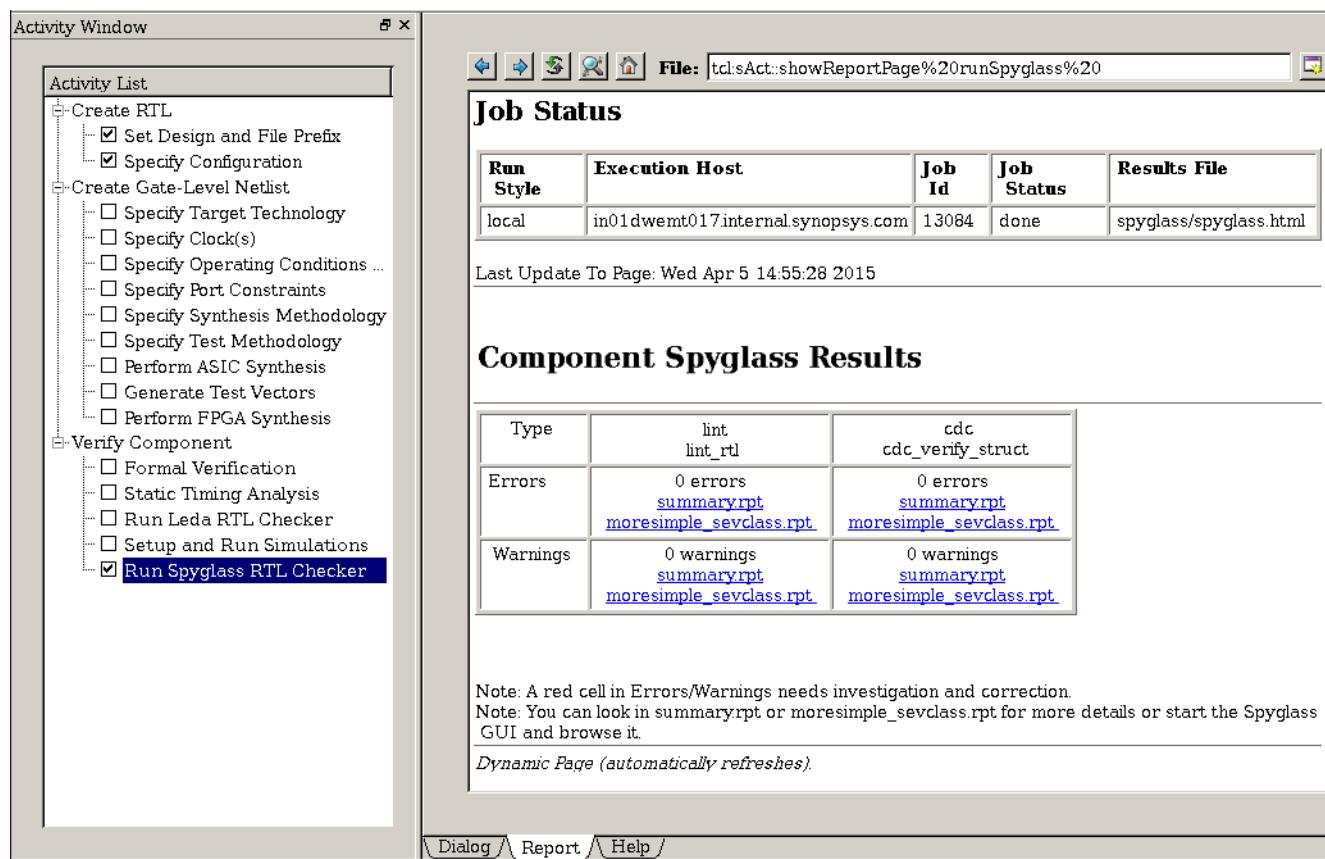
[Figure 2-2](#) shows the coreConsultant GUI in which you run Lint and CDC goals.

Figure 2-2 SpyGlass Options in coreConsultant

The SpyGlass flow in coreConsultant runs Guideware 2.0 rules for block/rtl_handoff. Within the block/rtl_handoff, only lint/lint_rtl and cdc/cdc_verify_struct goals are run.

In [Figure 2-2](#), select the type of run goals. You can select either Lint run goal or CDC run goal, or both Lint and CDC run goals. By default, both Lint and CDC are selected.

When the Lint and/or CDC is run, the results are available in the Report tab. Errors (if any) are displayed with a red colored cell and warnings (if any) are displayed in yellow colored cell, as shown in [Figure 2-3](#).

Figure 2-3 coreConsultant SpyGlass Report Summary

2.2.6.1 Fixed Settings

The settings are fixed (hardcoded) when you run SpyGlass in coreConsultant.

2.2.6.2 SpyGlass Lint

Table 2-2 lists the SpyGlass Link waiver files that are used by the coreConsultant tool.

Table 2-2 Waiver Files for Sypglass Lint

File Name	Description
<code><configured_workspace>/spyglass/spyglass_design_specific_waivers.swl</code>	These are DW_apb_i2c design-specific rule waivers. This file contains Lint waivers for DW_apb_i2c (if applicable). The reason for each of the waivers (if any) are included as comments in the file.
<code><configured_workspace>/spyglass/spyglass_engineering_council_waivers.swl</code>	This file contains rules that Synopsys waives for its IPs.

2.2.6.3 SpyGlass CDC

To define the SpyGlass CDC constraints, it is important to understand the reset and clock logic used in DW_apb_i2c. For information on reset and clock logic, refer “[Functional Description](#)” on page [37](#) and “[Signal Descriptions](#)” on page [125](#).

2.2.6.3.1 CDC Files

[Table 2-3](#) summarizes files for SpyGlass CDC used by coreConsultant.

Table 2-3 Waiver Files for Spyglass CDC

File Name	Description
<code><configured_workspace>/spyglass/manual.sgd</code>	These are the constraints pertaining to a given mode.
<code><configured_workspace>/spyglass/ports.sgdc</code>	These are the list of I/O signals and their respective clocks.
<code><configured_workspace>/spyglass/spyglass_design_specific_waivers.swl</code>	These are DW_apb_i2c design-specific rule waivers. This file contains CDC waivers for DW_apb_i2c (if applicable). The reason for each of the waivers (if any) are included as comments in the file.
<code><configured_workspace>/spyglass/spyglass_engineering_council_waivers.swl</code>	These are rules that Synopsys waives for its IPs.

2.2.6.3.2 CDC Path Debug Using the SpyGlass GUI

For debugging the CDC path, it is necessary to run SpyGlass in interactive mode in the configured workspace. To invoke the SpyGlass GUI and to run CDC, complete the following steps:

1. Go to the `<configured_workspace>/spyglass` directory.
2. Issue `./sh.spyglass` to start the SpyGlass GUI or issue `./sh.spyglass -batch` to start the SpyGlass in batch mode.
3. In the SpyGlass GUI, the Goal Setup window opens by default.
4. Uncheck the `lint rtl` option and click the **Selected Goal (s)** button.
5. After the CDC run is complete, the Analyze Results window displays the results.

Navigate to and select the relevant errors to open a schematic for analysis.

2.3 Overview of the coreAssembler Configuration and Integration Process

Once you have correctly downloaded and installed a release of DesignWare SIP components and then set up your environment, you can begin work on your DesignWare subsystem with coreAssembler.

2.3.1 coreAssembler Usage

Figure 2-4 illustrates some general directories and files in a coreAssembler workspace.

Figure 2-4 coreAssembler Usage Flow

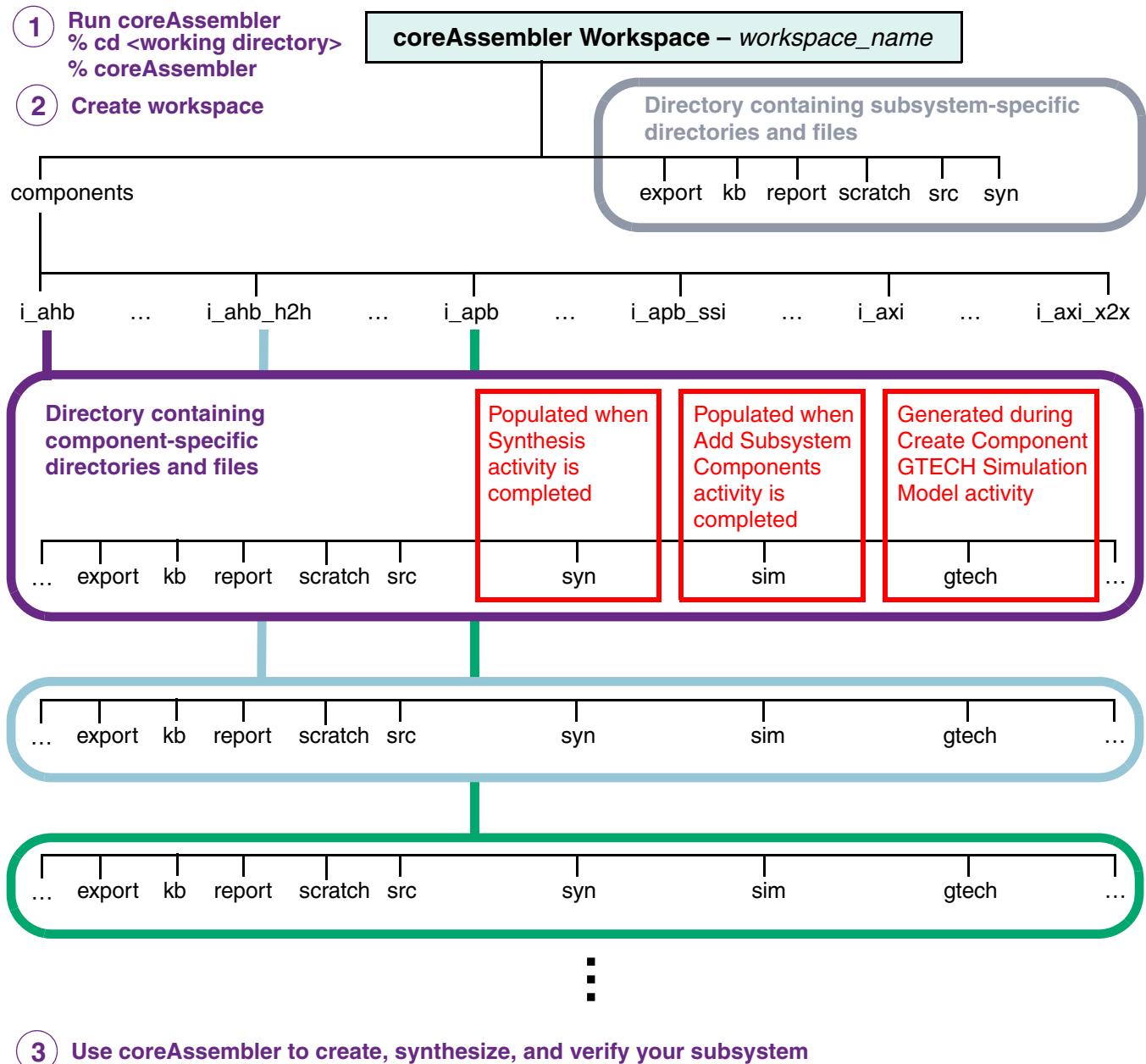


Table 2-4 provides a description of the implementation workspace directory and subdirectories.

Table 2-4 coreAssembler Implementation Workspace Directory Contents

Directory/Subdirectory	Description
components	Contains a directory for each IP component instance connected in the subsystem. Generated and populated with separate component directories upon first adding components; populated and updated throughout activities.
i_component/auxiliary	Scripts and text files used by coreAssembler. Generated during Add Subsystem Components activity.
i_component/custom	Contains RTL preprocessor scripts. Generated during Configure Components activity.
i_component/doc	Contains local copies of component-specific databooks. Generated during Add Subsystem Components activity.
i_component/export	Contains files used to integrate results from the completed source configuration and synthesis activities into your design (outside coreAssembler). Generated during Add Subsystem Components activity; populated during Configure Components activity.
i_component/gtech	Contains synthesis scripts and output netlists from gtech generation; also used for RTL simulation of encrypted source code. Generated during Create Component GTECH Simulation Model activity.
i_component/kb	Contains knowledge base information used by coreAssembler. These are binary files containing the state of the design. Generated during Add Subsystem Components activity; populated and updated throughout activities.
i_component/leda	Contains Leda configuration files for the component. Generated during Add Subsystem Components activity; populated during Run Leda Coding Checker (for /i_component) activity.
i_component/report	Contains all of the reports created by coreAssembler during build, configuration, test and synthesis phases. An index.html file in this directory links to many of these generated reports. Generated during Add Subsystem Components activity; populated and updated throughout activities.
i_component/scratch	Contains temp files used during the coreAssembler processes. Generated during Add Subsystem Components activity; populated and updated throughout activities.
i_component/sim	Contains test stimulus and output files. Generated during Add Subsystem Components activity; updated during Setup and Run Simulations (for /i_component) activity.

Table 2-4 coreAssembler Implementation Workspace Directory Contents (Continued)

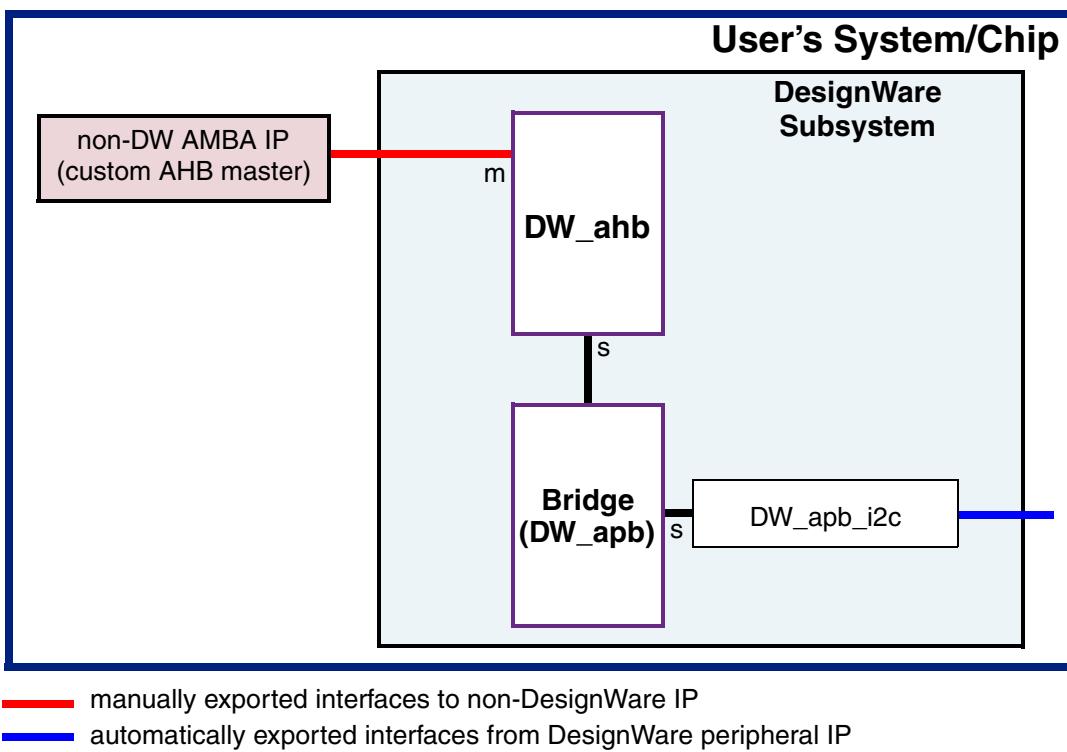
Directory/Subdirectory	Description
i_component/spyglass	Contains SpyGlass Lint and CDC configuration files for the component. Generated upon first SpyGlass run; updated during Run Spyglass RTL Checker activity.
i_component/src	Includes the top-level RTL file, <i>design_name.v</i> . If you have a source license, this will contain plain-text RTL; if you only have a designware license, this will contain encrypted RTL.
	Generated during Add Subsystem Components activity; populated during Specify Configuration activity.
i_component/syn	Contains synthesis files for the component. Generated during Add Subsystem Components activity; updated during Synthesis activity.
i_component/tcl	Contains synthesis intent scripts. Generated during Add Subsystem Components activity.
export	Contains subsystem files used to integrate the results from the completed source configuration and synthesis activities into your design (outside coreAssembler). Generated upon first creating workspace; populated starting with Memory Map Specification activity.
kb	Contains subsystem knowledge base information used by coreAssembler. These are binary files containing the state of the design. Generated upon first creating workspace; populated and updated throughout activities.
report	Contains subsystem reports created by coreAssembler during build, configuration, test and synthesis phases. An index.html file in this directory links to many of these generated reports. Generated upon first creating workspace; populated and updated throughout activities.
scratch	Contains subsystem temp files used during the coreAssembler processes. Generated upon first creating workspace; populated and updated throughout activities.
src	Includes the RTL related to the subsystem. If you have a source license, this will contain plain-text RTL; if you only have a designware license, this will contain encrypted RTL. Generated upon first creating workspace; populated starting with Generate Subsystem RTL activity.
syn	Contains synthesis files for the subsystem. Generated upon first creating workspace; updated during Synthesize activity and Formal Verification activity.

For details on some key files created during coreAssembler activities, refer to “[Database Files](#)” on page [34](#).

For information on using coreAssembler, refer to the [coreAssembler User Guide](#). For information on getting started with using DesignWare SIP components for AMBA 2 and AMBA 3 AXI components within coreTools, refer to [Using DesignWare Library IP in coreAssembler](#).

Figure 2-5 illustrates the DW_apb_i2c in a simple subsystem.

Figure 2-5 DW_apb_i2c in Simple Subsystem



The subsystem in [Figure 2-5](#) contains the following components that you may want to use as you learn to use coreAssembler:

- DW_apb_i2c
- DW_ahb
- DW_apb
- AHB Master

The AHB Master is meant to be exported out of the design and then replaced by a real AHB Master—such as a CPU—later in the design process; at least one exported AHB master is required in a subsystem if you intend to do a basic simulation that tests connections.

2.3.2 Configuring the DW_apb_i2c within a Subsystem

The “Parameters” chapter on [page 105](#) describes the DW_apb_i2c hardware configuration parameters that you configure using the coreAssembler GUI. Corresponding databooks for the other components in a subsystem contain “Parameters” chapters that describe their respective configuration parameters.

The “Creating the RTL View of a Subsystem” chapter in the [coreAssembler User Guide](#) discusses how to configure subsystem components and automatically connect them using the coreAssembler GUI.

2.3.3 Creating Gate-Level Netlists within coreAssembler

The “Creating the Gate-Level Netlist for a Subsystem” chapter in the [coreAssembler User Guide](#) discusses how to create a translation of the RTL view into a technology-specific netlist for a subsystem.

2.3.4 Verifying the DW_apb_i2c within coreAssembler

The “Verification” chapter on [page 269](#) provides an overview of the testbench available for DW_apb_i2c verification using the coreAssembler GUI.

The “Verifying Subsystems and Components” chapter in the [coreAssembler User Guide](#) discusses how to simulate a subsystem.

2.3.5 Running Leda on Generated Code with coreAssembler

When you select **Verify Component > Run Leda Coding Checker for/i_component** from the Activity List, the corresponding Activity View appears. In this Activity View you select rules configuration file and define Leda command line switches.

2.3.6 Running Spyglass on Generated Code with coreAssembler

When you select **Verify Component > Run Spyglass RTL Checker for/i_component** from the Activity List, the corresponding Activity View appears. In this Activity View, you can select to run Spyglass Lint and Spyglass CDC.

2.4 Database Files

The following subsections describe some key files created in coreConsultant and coreAssembler activities.

2.4.1 Design/HDL Files

The following sections describe the design and HDL files that are produced by coreConsultant and coreAssembler when configuring and verifying a DesignWare Synthesizable Component. The following files are created in different directories by coreConsultant and coreAssembler:

- coreConsultant – *workspace/* directory
- coreAssembler – *workspace/components/i_component/* directory

2.4.1.1 RTL-Level Files

The following table describes the RTL files that are generated by the Create RTL activity. They are encrypted except where otherwise noted. Any Synopsys synthesis tool or simulator can read encrypted RTL files.

Table 2-5 RTL-Level Files

Files	Encrypted?	Purpose
<code>./src/component_cc_constants.v</code>	No	Includes definitions and values of all configuration parameters that you have specified for the component.
<code>./src/component.v</code>	No	Top-level HDL file. Include the DesignWare libraries by using the following options in your simulator invocation: <code>+libext+.v+.V -y \${SYNOPSYS}/packages/gtech/src_ver -y \${SYNOPSYS}/dw/sim_ver</code>
<code>./src/component_submodule.v</code>	Yes	Sub-modules of component
<code>./src/component_constants.v</code>	No	Includes the constants used internally in the design.
<code>./src/component_undef.v</code>		Includes an undef for each of the definitions found in the <code>component_cc_constants.v</code> file; compiled in after the last file listed in <code>./src/components.lst</code> when compiling multiple instances of the same IP.
<code>./src/component.lst</code>	No	Lists the order in which the RTL files should be read into tools, such as simulators or dc_shell. For example, use the following option to read the design into VCS: <code>vcs +v2k -f component.lst</code>

2.4.1.2 Simulation Model Files

The following table includes files generated for the component during the Generate GTECH Simulation activity. These files are needed when you are using a non-Synopsys simulator (when you can not use the encrypted RTL).

Table 2-6 Simulation Model Files

Files	Encrypted?	Purpose
<code>./gtech/final/db/component.v</code>	No	Simulation model of the component for use with non-Synopsys simulators. A technology-independent, gate-level netlist; VHDL and Verilog versions are generated. Include the DesignWare libraries by using the following options in your simulator invocation: <code>+libext+.v+.V -y \${SYNOPSYS}/packages/gtech/src_ver -y \${SYNOPSYS}/dw/sim_ver</code>

2.4.2 Synthesis Files

The following table includes files generated after the Create Gate-Level Netlist activity is performed on a component.

Table 2-7 Synthesis Files

Files	Encrypted?	Purpose
./syn/auxScripts	No	Auxiliary files for synthesis.
./syn/final/db/ <i>component</i> .db	Binary format	Synopsys .db files (gate level) that can be read into dc_shell for further synthesis, if desired.
./syn/final/db/ <i>component</i> .v	No	Gate-level netlist that is mapped to technology libraries that you specify.
./syn/constrain/script/*.*	No	Constraint files for the components.
./syn/final/report/*.*	No	Synthesis result files.

2.4.3 Verification Reference Files

Files described in the following table include information pertaining to the component's operation so that you can verify installation and configuration of the component has been successful. These files are not for re-use during system-level verification.

Table 2-8 Verification Reference Files

Files	Encrypted?	Purpose
./sim/runttest	No	Perl script that runs the Setup and Run Simulations activity from the command line.
./sim/runttest.log	No	The overall result of simulation, including pass/fail results.
./sim/test_ <i>testname</i> /test.result	No	Pass/fail of individual test.
./sim/test_ <i>testname</i> /test.log	No	Log file for individual test.

3

Functional Description

This chapter describes the functional behavior of DW_apb_i2c in more detail.

3.1 Overview

The I²C bus is a two-wire serial interface, consisting of a serial data line (SDA) and a serial clock (SCL). These wires carry information between the devices connected to the bus. Each device is recognized by a unique address and can operate as either a “transmitter” or “receiver,” depending on the function of the device. Devices can also be considered as masters or slaves when performing data transfers. A master is a device that initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.



Note The DW_apb_i2c must only be programmed to operate in either master OR slave mode only. Operating as a master and slave simultaneously is not supported.

The DW_apb_i2c module can operate in standard mode (with data rates 0 to 100 Kb/s), fast mode (with data rates less than or equal to 400 Kb/s), fast mode plus (with data rates less than or equal to 1000 Kb/s), high-speed mode (with data rates less than or equal to 3.4 Mb/s), and Ultra-Fast Speed Mode (with data rates less than or equal to 5 Mb/s).



Note In this document, references to fast mode also apply to fast mode plus, unless specifically stated otherwise.

The DW_apb_i2c can communicate with devices only of these modes as long as they are attached to the bus. Additionally, high-speed mode and fast mode devices are downward compatible. For instance, high-speed mode devices can communicate with fast mode and standard mode devices in a mixed-speed bus system; fast mode devices can communicate with standard mode devices in 0 to 100 Kb/s I²C bus system. However:

1. Standard mode devices are not upward compatible and should not be incorporated in a fast-mode I²C bus system as they cannot follow the higher transfer rate and unpredictable states would occur.
2. Ultra-Fast mode devices are not downward compatible and should not be incorporated in traditional I²C speeds (High speed, Fast/Fast Mode Plus speed, Standard mode speed) as Ultra-Fast mode

follows the higher transfer rate (up to 5Mb/s) with only write transfers and there is no acknowledgment from the slave.

An example of high-speed mode devices are LCD displays, high-bit count ADCs, and high capacity EEPROMs. These devices typically need to transfer large amounts of data. Most maintenance and control applications, the common use for the I²C bus, typically operate at 100 kHz (in standard and fast modes).

An example of Ultra-Fast speed mode devices are LED controllers and other devices that do not need feedback. These devices typically need to transfer large amounts of data greater than 1Mhz.

Any DW_apb_i2c device can be attached to an I²C-bus and every device can talk with any master, passing information back and forth. There needs to be at least one master (such as a microcontroller or DSP) on the bus but there can be multiple masters, which require them to arbitrate for ownership. Multiple masters and arbitration are explained later in this chapter.

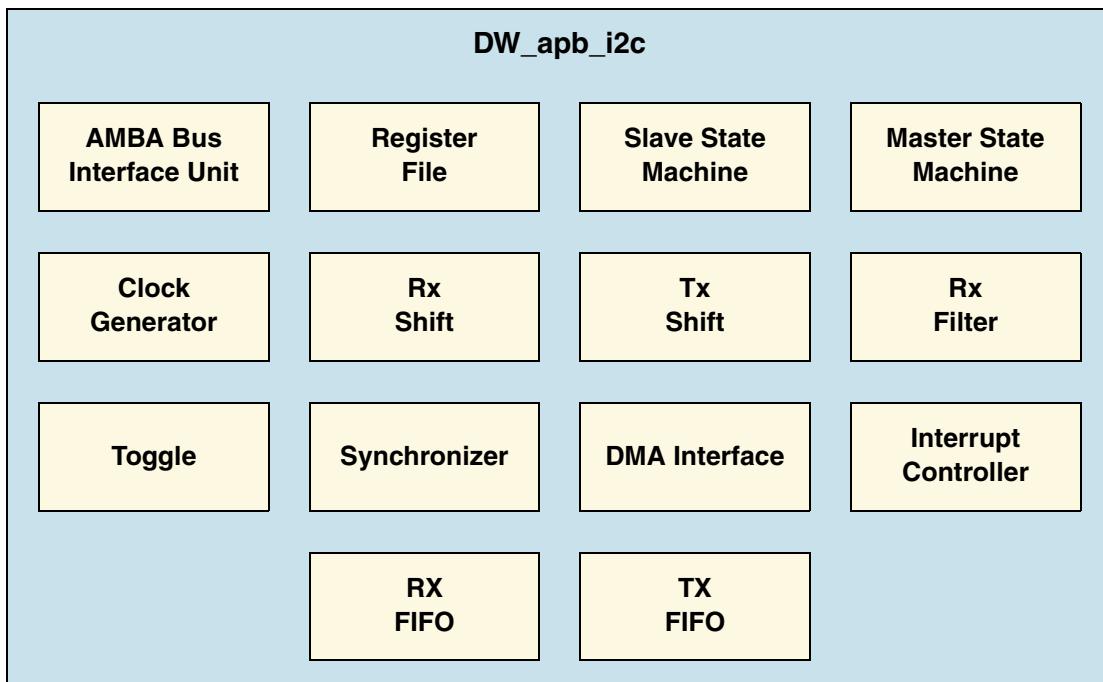
The DW_apb_i2c also supports SMBus and PMBus protocols for System Management and Power management.



In this databook, any reference to SMBus implicitly refers to PMBus also and vice versa.

The DW_apb_i2c is made up of an AMBA APB slave interface, an I²C interface, and FIFO logic to maintain coherency between the two interfaces. A simplified block diagram of the component is illustrated in [Figure 3-1](#).

Figure 3-1 DW_apb_i2c Block Diagram



The following define the file names and functions of the blocks in [Figure 3-1](#):

- AMBA Bus Interface Unit—DW_apb_i2c_biu.v—Takes the APB interface signals and translates them into a common generic interface that allows the register file to be bus protocol-agnostic.
- Register File—DW_apb_i2c_Regfile—Contains configuration registers and is the interface with software.
- Slave State Machine—DW_apb_i2c_slvfsm—Follows the protocol for a slave and monitors bus for address match.
- Master State Machine—DW_apb_i2c_mstfsm—Generates the I²C protocol for the master transfers.
- Clock Generator—DW_apb_i2c_clk_gen.v—Calculates the required timing to do the following:
 - Generate the SCL clock when configured as a master
 - Check for bus idle
 - Generate a START and a STOP
 - Setup the data and hold the data
- Rx Shift—DW_apb_i2c_rx_shift—Takes data into the design and extracts it in byte format.
- Tx Shift—DW_apb_i2c_tx_shift—Presents data supplied by CPU for transfer on the I²C bus.
- Rx Filter—DW_apb_i2c_rx_filter—Detects the events in the bus; for example, start, stop and arbitration lost.
- Toggle—DW_apb_i2c_toggle—Generates pulses on both sides and toggles to transfer signals across clock domains.
- Synchronizer—DW_apb_i2c_sync—Transfers signals from one clock domain to another.
- DMA Interface—DW_apb_i2c_dma—Generates the handshaking signals to the central DMA controller in order to automate the data transfer without CPU intervention.
- Interrupt Controller—DW_apb_i2c_intctl—Generates the raw interrupt and interrupt flags, allowing them to be set and cleared.
- RX FIFO/TX FIFO—DW_apb_i2c_fifo—Holds the RX FIFO and TX FIFO register banks and controllers, along with their status levels.



Note The ic_clk frequency must be greater than or equal to the pclk frequency. This restriction occurs because the clock domain-crossing scheme within the DW_apb_i2c does not support pclk faster than ic_clk.

3.2 I²C Terminology

The following terms are used throughout this manual and are defined as follows:

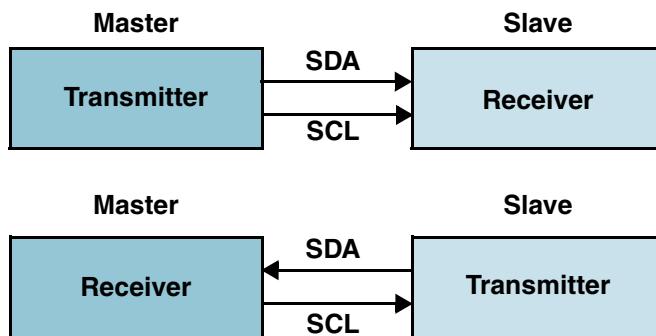
3.2.1 I²C Bus Terms

The following terms relate to how the role of the I²C device and how it interacts with other I²C devices on the bus.

- **Transmitter** – the device that sends data to the bus. A transmitter can either be a device that initiates the data transmission to the bus (a *master-transmitter*) or responds to a request from the master to send data to the bus (a *slave-transmitter*).
- **Receiver** – the device that receives data from the bus. A receiver can either be a device that receives data on its own request (a *master-receiver*) or in response to a request from the master (a *slave-receiver*).
- **Master** -- the component that initializes a transfer (START command), generates the clock (SCL) signal and terminates the transfer (STOP command). A master can be either a transmitter or a receiver.
- **Slave** – the device addressed by the master. A slave can be either receiver or transmitter.

These concepts are illustrated in [Figure 3-2](#).

Figure 3-2 Master/Slave and Transmitter/Receiver Relationships



- **Multi-master** – the ability for more than one master to co-exist on the bus at the same time without collision or data loss.
- **Arbitration** – the predefined procedure that authorizes only one master at a time to take control of the bus. For more information about this behavior, refer to “[Multiple Master Arbitration](#)” on page [53](#).
- **Synchronization** – the predefined procedure that synchronizes the clock signals provided by two or more masters. For more information about this feature, refer to “[Clock Synchronization](#)” on page [55](#).
- **SDA** – data signal line (Serial DAta)
- **SCL** – clock signal line (Serial CLock)

3.2.2 Bus Transfer Terms

The following terms are specific to data transfers that occur to/from the I²C bus.

- **START (RESTART)** – data transfer begins with a START or RESTART condition. The level of the SDA data line changes from high to low, while the SCL clock line remains high. When this occurs, the bus becomes busy.



Note START and RESTART conditions are functionally identical.

-
- **STOP** – data transfer is terminated by a STOP condition. This occurs when the level on the SDA data line passes from the low state to the high state, while the SCL clock line remains high. When the data transfer has been terminated, the bus is free or idle once again. The bus stays busy if a RESTART is generated instead of a STOP condition.

3.3 I²C Behavior

The DW_apb_i2c can be controlled via software to be either:

- An I²C master only, communicating with other I²C slaves; OR
- An I²C slave only, communicating with one more I²C masters.

The master is responsible for generating the clock and controlling the transfer of data. The slave is responsible for either transmitting or receiving data to/from the master. The acknowledgement of data is sent by the device that is receiving data, which can be either a master or a slave. As mentioned previously, the I²C protocol also allows multiple masters to reside on the I²C bus and uses an arbitration procedure to determine bus ownership.

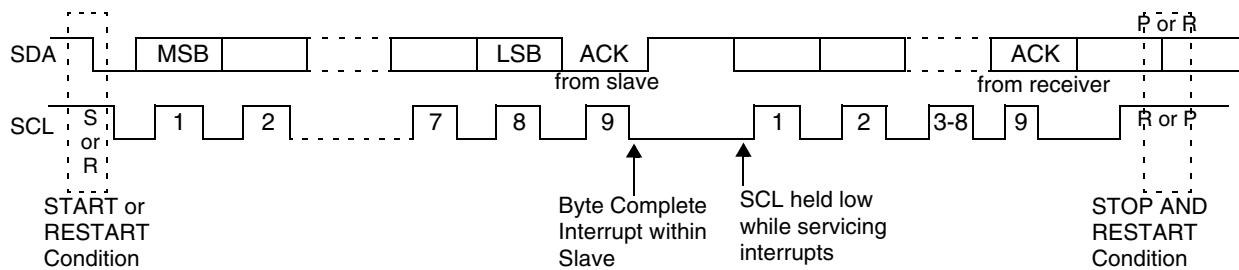
Each slave has a unique address that is determined by the system designer. When a master wants to communicate with a slave, the master transmits a START/RESTART condition that is then followed by the slave's address and a control bit (R/W) to determine if the master wants to transmit data or receive data from the slave. The slave then sends an acknowledge (ACK) pulse after the address.

If the master (master-transmitter) is writing to the slave (slave-receiver), the receiver gets one byte of data. This transaction continues until the master terminates the transmission with a STOP condition. If the master is reading from a slave (master-receiver), the slave transmits (slave-transmitter) a byte of data to the master, and the master then acknowledges the transaction with the ACK pulse. This transaction continues until the master terminates the transmission by not acknowledging (NACK) the transaction after the last byte is

received, and then the master issues a STOP condition or addresses another slave after issuing a RESTART condition. This behavior is illustrated in [Figure 3-3](#).

In Ultra-Fast Speed Mode, the master can issue only the write transfers to the slaves with always not acknowledging (NACK) from the slaves. Read transfers are not allowed in this mode.

Figure 3-3 Data transfer on the I2C Bus



The DW_apb_i2c is a synchronous serial interface. The SDA line is a bidirectional signal and changes only while the SCL line is low, except for STOP, START, and RESTART conditions. The output drivers are open-drain or open-collector to perform wire-AND functions on the bus. The maximum number of devices on the bus is limited by only the maximum capacitance specification of 400 pF. Data is transmitted in byte packages.

The I²C protocols implemented in DW_apb_i2c are described in more details in [“I²C Protocols”](#) on page [43](#).

3.3.1 START and STOP Generation

When operating as an I²C master, putting data into the transmit FIFO causes the DW_apb_i2c to generate a START condition on the I²C bus. If the IC_EMPTYFIFO_HOLD_MASTER_EN parameter is set to 0, allowing the transmit FIFO to empty causes the DW_apb_i2c to generate a STOP condition on the I²C bus. If IC_EMPTYFIFO_HOLD_MASTER_EN is set to 1, then writing a 1 to IC_DATA_CMD[9] causes the DW_apb_i2c to generate a STOP condition on the I²C bus; a STOP condition is not issued if this bit is not set, even if the transmit FIFO is empty.

When operating as a slave, the DW_apb_i2c does not generate START and STOP conditions, as per the protocol. However, if a read request is made to the DW_apb_i2c, it holds the SCL line low until read data has been supplied to it. This stalls the I²C bus until read data is provided to the slave DW_apb_i2c, or the DW_apb_i2c slave is disabled by writing a 0 to bit 0 of the [IC_ENABLE](#) register.

3.3.2 Combined Formats

The DW_apb_i2c supports mixed read and write combined format transactions in both 7-bit and 10-bit addressing modes.

The DW_apb_i2c does not support mixed address and mixed address format—that is, a 7-bit address transaction followed by a 10-bit address transaction or vice versa—combined format transactions.

To initiate combined format transfers, IC_CON.IC_RESTART_EN should be set to 1. With this value set and operating as a master, when the DW_apb_i2c completes an I²C transfer, it checks the transmit FIFO and executes the next transfer. If the direction of this transfer differs from the previous transfer, the combined

format is used to issue the transfer. If the transmit FIFO is empty when the current I²C transfer completes – depending on the value of IC_EMPTYFIFO_HOLD_MASTER_EN:

- Either a STOP is issued or,
- IC_DATA_CMD[9] is checked *and*:
 - If set to 1, a STOP bit is issued.
 - If set to 0, the SCL is held low until the next command is written to the transmit FIFO.

For more details, refer to “[Tx FIFO Management and START, STOP and RESTART Generation](#)” on page [48](#).



Note Mixed write and read transactions in both 7-bit and 10-bit addressing modes are not applicable for Ultra-Fast Mode (IC_ULTRA_FAST_MODE=1) as read transfers are not supported in Ultra-Fast Mode.

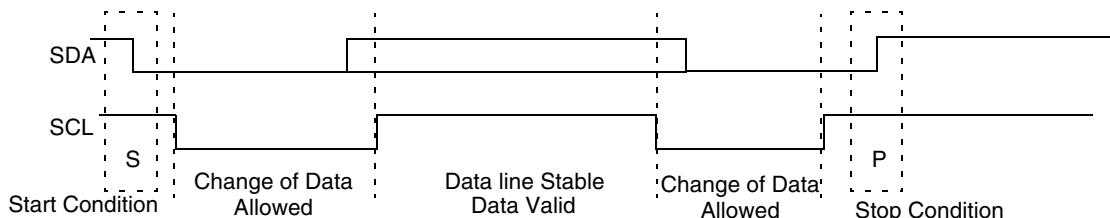
3.4 I²C Protocols

The DW_apb_i2c has the protocols discussed in this section.

3.4.1 START and STOP Conditions

When the bus is idle, both the SCL and SDA signals are pulled high through external pull-up resistors on the bus. When the master wants to start a transmission on the bus, the master issues a START condition. This is defined to be a high-to-low transition of the SDA signal while SCL is 1. When the master wants to terminate the transmission, the master issues a STOP condition. This is defined to be a low-to-high transition of the SDA line while SCL is 1. [Figure 3-4](#) shows the timing of the START and STOP conditions. When data is being transmitted on the bus, the SDA line must be stable when SCL is 1.

Figure 3-4 START and STOP Condition



Note The signal transitions for the START/STOP conditions, as depicted in [Figure 3-4](#), reflect those observed at the output signals of the Master driving the I²C bus. Care should be taken when observing the SDA/SCL signals at the input signals of the Slave(s), because unequal line delays may result in an incorrect SDA/SCL timing relationship.

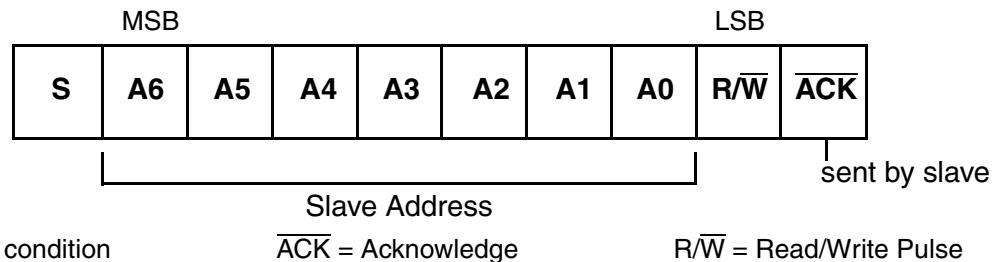
3.4.2 Addressing Slave Protocol

There are two address formats: the 7-bit address format and the 10-bit address format.

3.4.2.1 7-bit Address Format

During the 7-bit address format, the first seven bits (bits 7:1) of the first byte set the slave address and the LSB bit (bit 0) is the R/W bit as shown in [Figure 3-5](#). When bit 0 (R/W) is set to 0, the master writes to the slave. When bit 0 (R/W) is set to 1, the master reads from the slave.

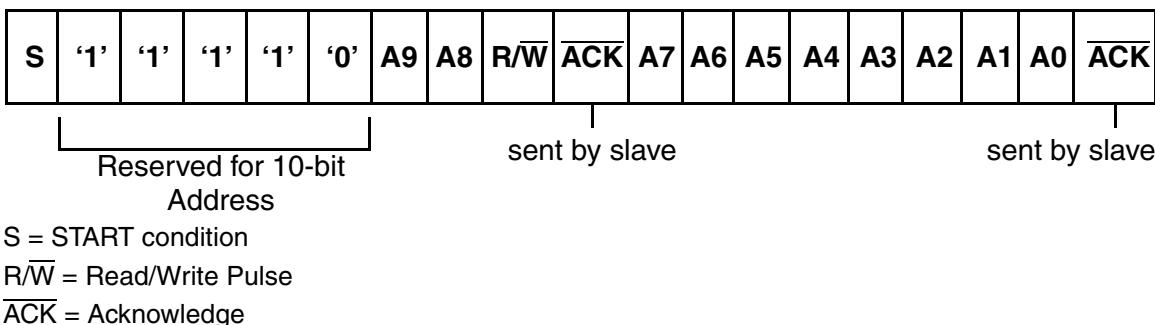
Figure 3-5 7-bit Address Format



3.4.2.2 10-bit Address Format

During 10-bit addressing, two bytes are transferred to set the 10-bit address. The transfer of the first byte contains the following bit definition. The first five bits (bits 7:3) notify the slaves that this is a 10-bit transfer followed by the next two bits (bits 2:1), which set the slaves address bits 9:8, and the LSB bit (bit 0) is the R/W bit. The second byte transferred sets bits 7:0 of the slave address. [Figure 3-6](#) shows the 10-bit address format.

Figure 3-6 10-bit Address Format



[Table 3-1](#) on page [44](#) defines the special purpose and reserved first byte addresses.

Table 3-1 I²C/SMBus Definition of Bits in First Byte

Slave Address	R/W Bit	Description
0000 000	0	General Call Address. DW_apb_i2c places the data in the receive buffer and issues a General Call interrupt.
0000 000	1	START byte. For more details, refer to " START BYTE Transfer Protocol " on page 47 .
0000 001	X	CBUS address. DW_apb_i2c ignores these accesses.

Table 3-1 I²C/SMBus Definition of Bits in First Byte (Continued)

Slave Address	R/W Bit	Description
0000 010	X	Reserved.
0000 011	X	Reserved.
0000 1XX	X	High-speed master code (for more information, refer to “ Multiple Master Arbitration ” on page 53).
1111 1XX	X	Reserved.
1111 0XX	X	10-bit slave addressing.
0001 000	X	SMBus Host
0001 100	X	SMBus Alert Response Address
1100 001	X	SMBus Device Default Address

DW_apb_i2c does not restrict you from using these reserved addresses. However, if you use these reserved addresses, you may run into incompatibilities with other I²C components.

3.4.3 Transmitting and Receiving Protocol

The master can initiate data transmission and reception to/from the bus, acting as either a master-transmitter or master-receiver. A slave responds to requests from the master to either transmit data or receive data to/from the bus, acting as either a slave-transmitter or slave-receiver, respectively.

3.4.3.1 Master-Transmitter and Slave-Receiver

All data is transmitted in byte format, with no limit on the number of bytes transferred per data transfer. After the master sends the address and R/W bit or the master transmits a byte of data to the slave, the slave-receiver must respond with the acknowledge signal (ACK). When a slave-receiver does not respond with an ACK pulse, the master aborts the transfer by issuing a STOP condition. The slave must leave the SDA line high so that the master can abort the transfer.

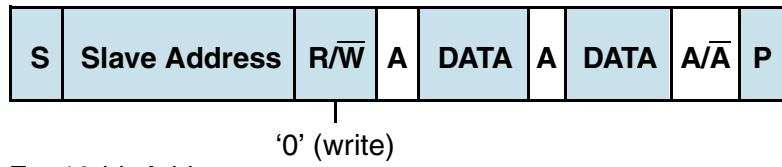
If the master-transmitter is transmitting data as shown in [Figure 3-7](#), then the slave-receiver responds to the master-transmitter with an acknowledge pulse after every byte of data is received.



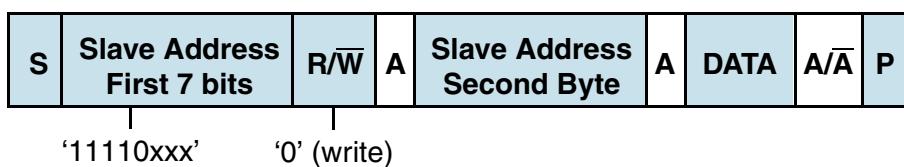
Note In Ultra-Fast Mode, the slave-receiver always responds with the No Acknowledge signal (NACK) for the Address and the write data from the Master.

Figure 3-7 Master-Transmitter Protocol

For 7-bit Address



For 10-bit Address



From Master to Slave

A = Acknowledge (SDA low)

From Slave to Master

A = No Acknowledge (SDA high)

S = START Condition

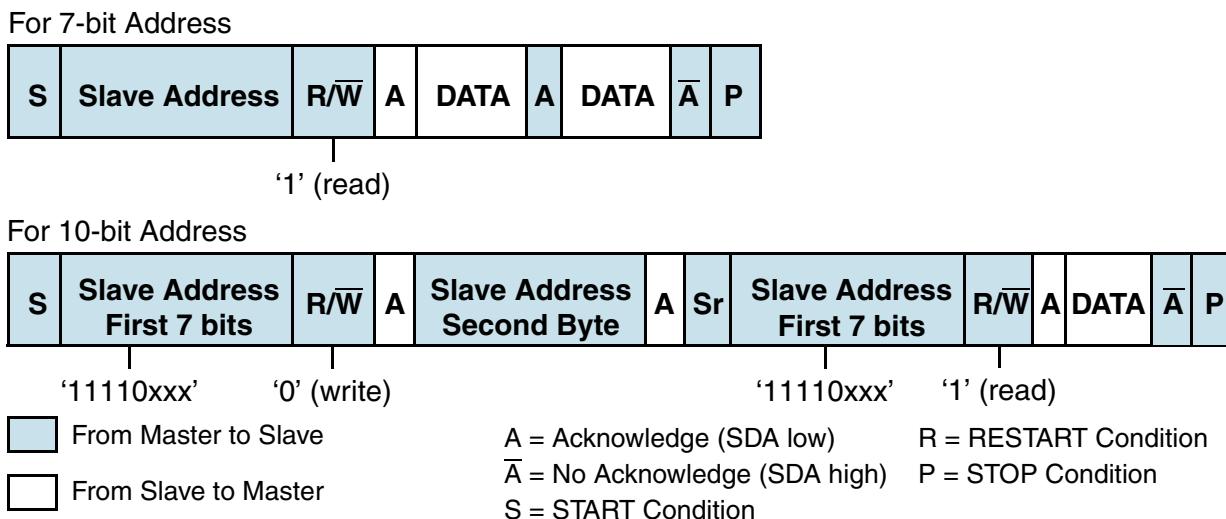
P = STOP Condition

3.4.3.2 Master-Receiver and Slave-Transmitter

If the master is receiving data as shown in [Figure 3-8](#), then the master responds to the slave-transmitter with an acknowledge pulse after a byte of data has been received, except for the last byte. This is the way the

master-receiver notifies the slave-transmitter that this is the last byte. The slave-transmitter relinquishes the SDA line after detecting the No Acknowledge (NACK) so that the master can issue a STOP condition.

Figure 3-8 Master-Receiver Protocol



When a master does not want to relinquish the bus with a STOP condition, the master can issue a RESTART condition. This is identical to a START condition except it occurs after the ACK pulse. Operating in master mode, the DW_apb_i2c can then communicate with the same slave using a transfer of a different direction. For a description of the combined format transactions that the DW_apb_i2c supports, refer to “[Combined Formats](#)” on page [42](#).



The DW_apb_i2c must be completely disabled—if I2C_DYNAMIC_TAR_UPDATE = 0—or inactive on the serial port—if I2C_DYNAMIC_TAR_UPDATE = 1—before the target slave address register (IC_TAR) can be reprogrammed.



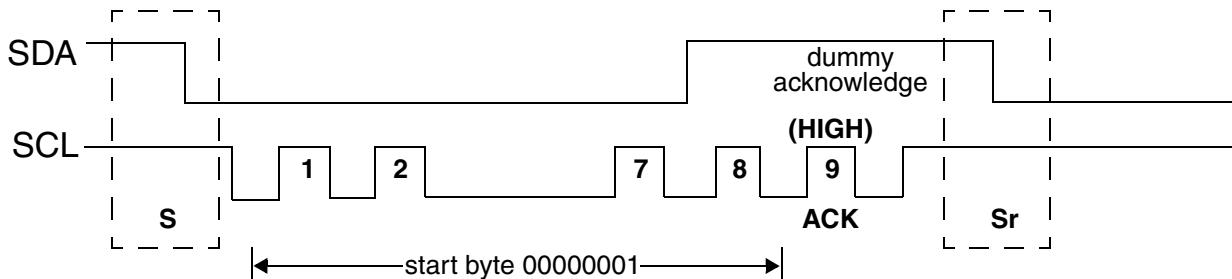
In Ultra-Fast mode, the Master receiver and Slave Transmitter is not applicable, as read transfers are not supported.

3.4.4 START BYTE Transfer Protocol

The START BYTE transfer protocol is set up for systems that do not have an on-board dedicated I²C hardware module. When the DW_apb_i2c is addressed as a slave, it always samples the I²C bus at the highest speed supported so that it never requires a START BYTE transfer. However, when DW_apb_i2c is a master, it supports the generation of START BYTE transfers at the beginning of every transfer in case a slave device requires it.

This protocol consists of seven zeros being transmitted followed by a 1, as illustrated in [Figure 3-9](#). This allows the processor that is polling the bus to under-sample the address phase until 0 is detected. Once the microcontroller detects a 0, it switches from the under sampling rate to the correct rate of the master.

Figure 3-9 START BYTE Transfer



The START BYTES procedure is as follows:

1. Master generates a START condition.
2. Master transmits the START byte (0000 0001).
3. Master transmits the ACK clock pulse. (Present only to conform with the byte handling format used on the bus)
4. No slave sets the ACK signal to 0.
5. Master generates a RESTART (R) condition.

A hardware receiver does not respond to the START BYTES because it is a reserved address and resets after the RESTART condition is generated.

3.5 Tx FIFO Management and START, STOP and RESTART Generation

When operating as a master, the DW_apb_i2c component supports two modes of Tx FIFO management. You use the IC_EMPTYFIFO_HOLD_MASTER_EN parameter to select between these two modes:

- IC_EMPTYFIFO_HOLD_MASTER_EN equals 0, illustrated in [Figure 3-10](#)
- IC_EMPTYFIFO_HOLD_MASTER_EN equals 1, illustrated in [Figure 3-13](#) on page 50

3.5.1 Tx FIFO Management When IC_EMPTYFIFO_HOLD_MASTER_EN = 0

When the value of IC_EMPTYFIFO_HOLD_MASTER_EN is 0, the component generates a STOP on the bus whenever the Tx FIFO becomes empty. If RESTART generation capability is enabled, the component generates a RESTART when the direction of the transfer in the Tx FIFO commands changes from Read to Write or vice-versa; if RESTART is not enabled, a STOP followed by a START is generated in this situation.

Figure 3-10 shows the bits in the IC_DATA_CMD register if IC_EMPTYFIFO_HOLD_MASTER_EN = 0.

Figure 3-10 IC_DATA_CMD Register if IC_EMPTYFIFO_HOLD_MASTER_EN = 0

IC_DATA_CMD	CMD	DATA
	8 7	0

DATA –Read/Write field; data retrieved from slave is read from this field; data to be sent to slave is written to this field.

CMD –Write-only field; this bit determines whether transfer to be carried out is Read (CMD=1) or Write (CMD=0)

Figure 3-11 shows a timing diagram that illustrates the behavior of the DW_apb_i2c when Tx FIFO becomes empty while operating as a master transmitter when IC_EMPTYFIFO_HOLD_MASTER_EN=0.

Figure 3-11 Master Transmitter — Tx FIFO Becomes Empty If IC_EMPTYFIFO_HOLD_MASTER_EN = 0

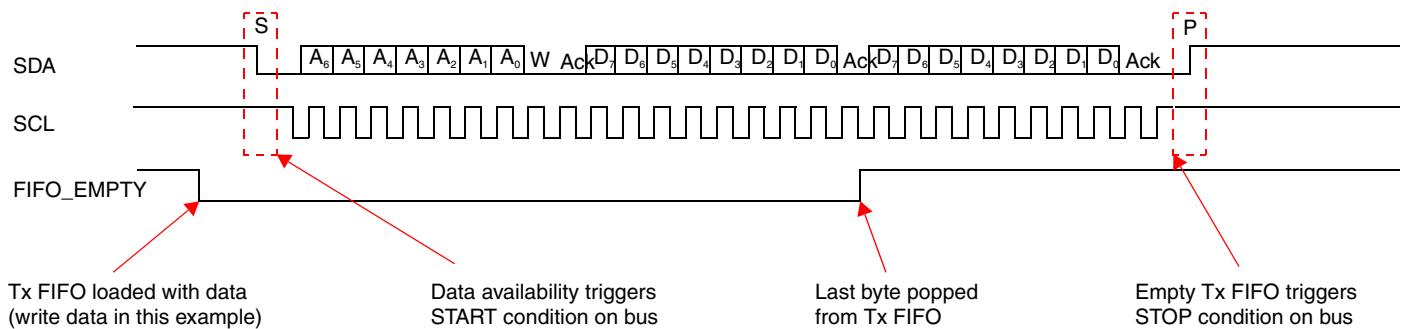
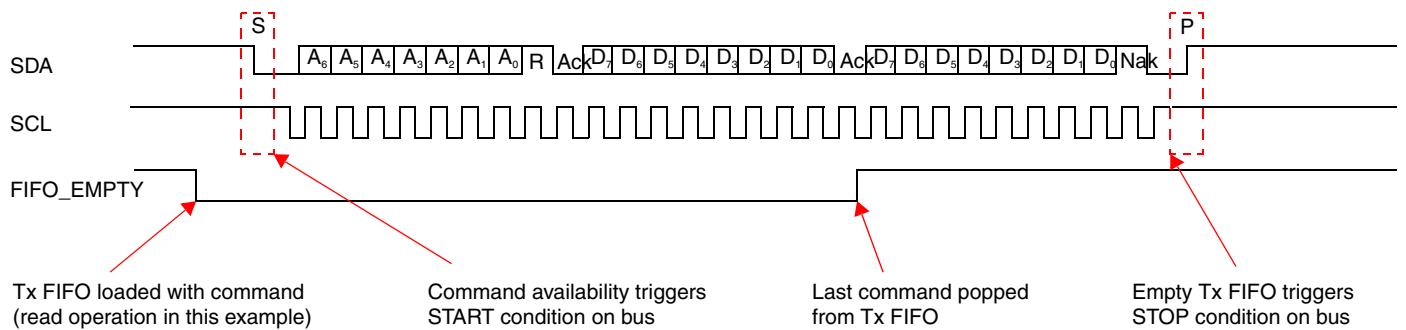


Figure 3-12 shows a timing diagram that illustrates the behavior of the DW_apb_i2c when Tx FIFO becomes empty while operating as a master receiver when IC_EMPTYFIFO_HOLD_MASTER_EN=0.

Figure 3-12 Master Receiver — Tx FIFO Becomes Empty If IC_EMPTYFIFO_HOLD_MASTER_EN = 0



3.5.2 Tx FIFO Management When IC_EMPTYFIFO_HOLD_MASTER_EN = 1

When the value of IC_EMPTYFIFO_HOLD_MASTER_EN is 1, the component does not generate a STOP if the Tx FIFO becomes empty; in this situation the component holds the SCL line low, stalling the bus until a new entry is available in the Tx FIFO. A STOP condition is generated only when the user specifically requests it by setting bit 9 (Stop bit) of the command written to IC_DATA_CMD register.

Figure 3-13 shows the bits in the IC_DATA_CMD register if IC_EMPTYFIFO_HOLD_MASTER_EN = 1.

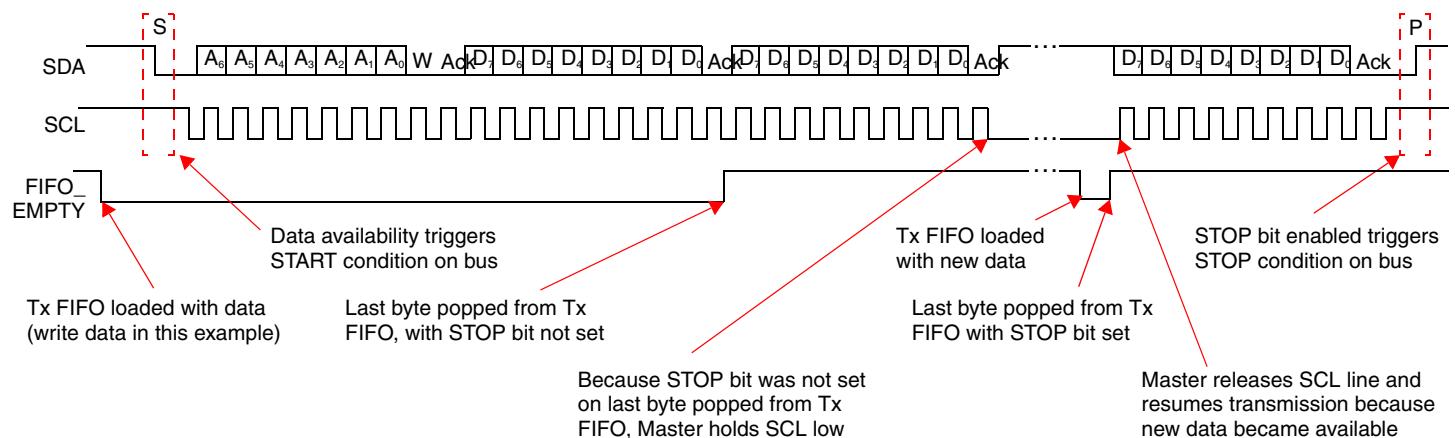
Figure 3-13 IC_DATA_CMD Register if IC_EMPTYFIFO_HOLD_MASTER_EN = 1

IC_DATA_CMD	Restart	Stop	CMD	DATA	0
	10	9	8	7	

DATA –Read/Write field; data retrieved from slave is read from this field; data to be sent to slave is written to this field
CMD –Write-only field; this bit determines whether transfer to be carried out is Read (CMD=1) or Write (CMD=0)
Stop –Write-only field; this bit determines whether STOP is generated after data byte is sent or received
Restart – Write-only field; this bit determines whether RESTART (or STOP followed by START in case of restart capability is not enabled) is generated before data byte is sent or received

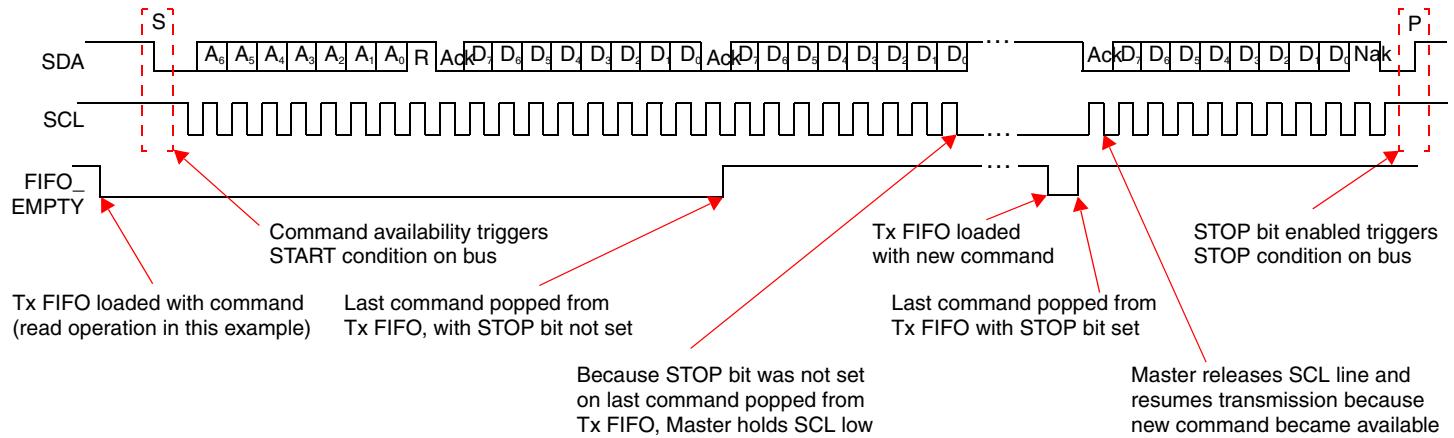
Figure 3-14 illustrates the behavior of the DW_apb_i2c when the Tx FIFO becomes empty while operating as a master transmitter, as well as showing the generation of a STOP condition when IC_EMPTYFIFO_HOLD_MASTER_EN=1.

Figure 3-14 Master Transmitter — Tx FIFO Empties/STOP Generation If IC_EMPTYFIFO_HOLD_MASTER_EN = 1



[Figure 3-15](#) illustrates the behavior of the DW_apb_i2c when the Tx FIFO becomes empty while operating as a master receiver, as well as showing the generation of a STOP condition when IC_EMPTYFIFO_HOLD_MASTER_EN=1.

Figure 3-15 Master Receiver — Tx FIFO Empties/STOP Generation If IC_EMPTYFIFO_HOLD_MASTER_EN = 1



[Figure 3-16](#) and [Figure 3-17](#) illustrate configurations where the user can control the generation of RESTART conditions on the I2C bus. If bit 10 (Restart) of the IC_DATA_CMD register is set and the restart capability is enabled (IC_RESTART_EN=1), a RESTART is generated before the data byte is written to or read from the slave. If the restart capability is not enabled a STOP followed by a START is generated in place of the RESTART. [Figure 3-16](#) illustrates this situation during operation as a master transmitter.

Figure 3-16 Master Transmitter — Restart Bit of IC_DATA_CMD Is Set (IC_EMPTYFIFO_HOLD_MASTER_EN = 1)

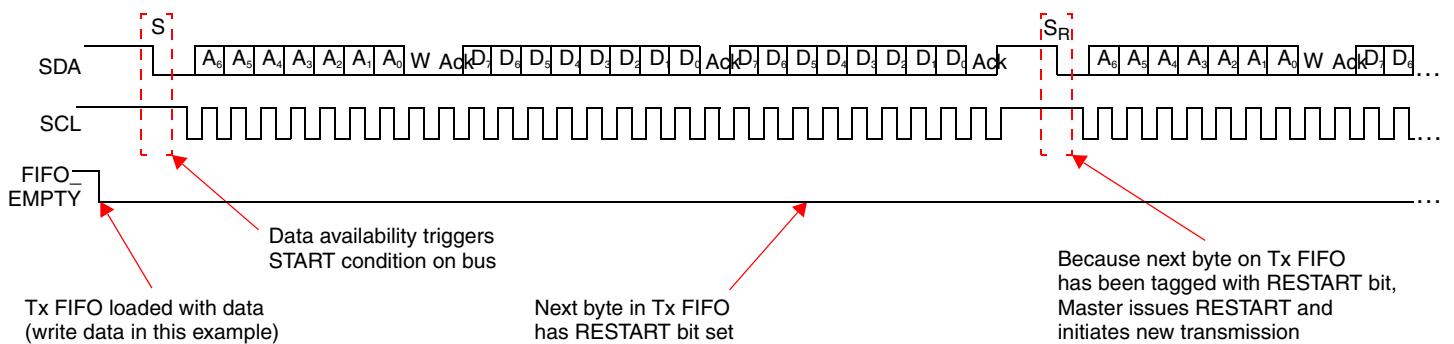


Figure 3-17 illustrates the same situation, but during operation as a master receiver.

Figure 3-17 Master Receiver — Restart Bit of IC_DATA_CMD Is Set (IC_EMPTYFIFO_HOLD_MASTER_EN = 1)

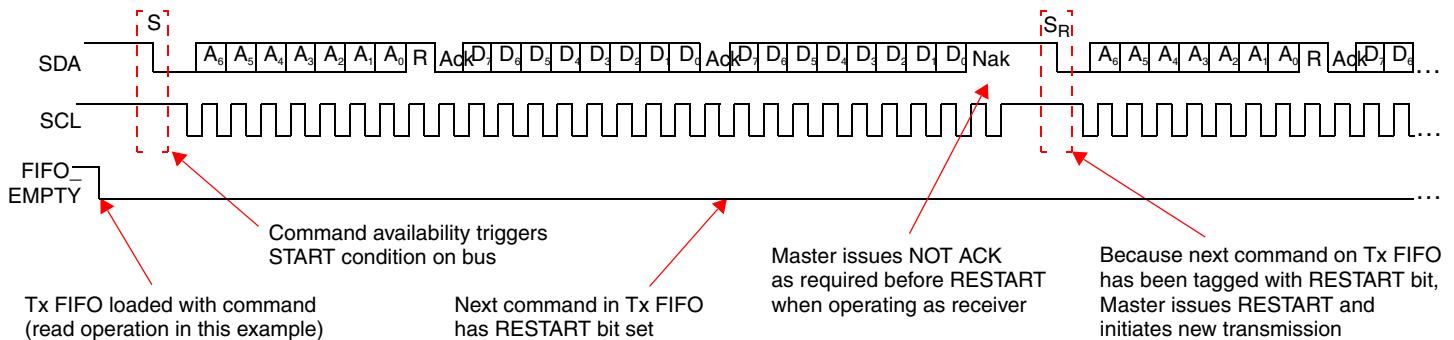


Figure 3-18 illustrates operation as a master transmitter where the Stop bit of the IC_DATA_CMD register is set and the Tx FIFO is not empty (IC_EMPTYFIFO_HOLD_MASTER_EN=1).

Figure 3-18 Master Transmitter — Stop Bit of IC_DATA_CMD Set/Tx FIFO Not Empty (IC_EMPTYFIFO_HOLD_MASTER_EN=1)

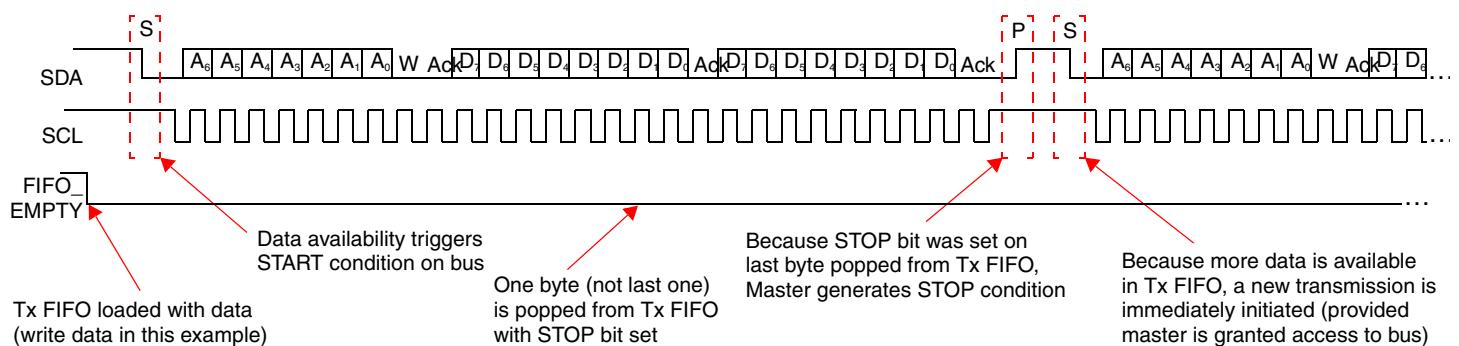


Figure 3-19 illustrates operation as a master transmitter where the first byte loaded into the Tx FIFO is allowed to go empty with the Restart bit set (IC_EMPTYFIFO_HOLD_MASTER_EN=1).

Figure 3-19 Master Transmitter — First Byte Loaded Into Tx FIFO Allowed to Empty, Restart Bit Set (IC_EMPTYFIFO_HOLD_MASTER_EN=1)

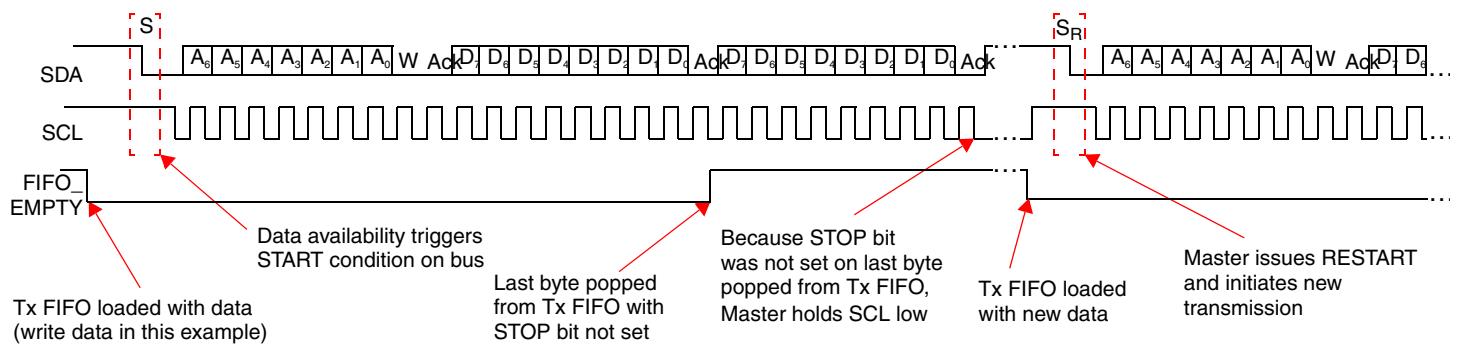


Figure 3-20 illustrates operation as a master receiver where the Stop bit of the IC_DATA_CMD register is set and the Tx FIFO is not empty (IC_EMPTYFIFO_HOLD_MASTER_EN=1).

Figure 3-20 Master Receiver — Stop Bit of IC_DATA_CMD Set/Tx FIFO Not Empty (IC_EMPTYFIFO_HOLD_MASTER_EN=1 and IC_ULTRA_FAST_MODE=0)

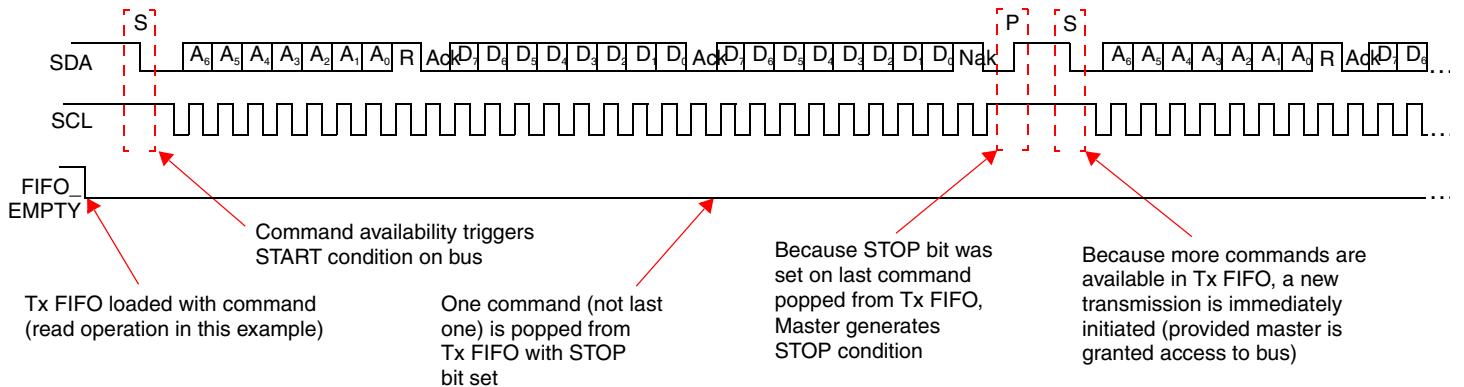
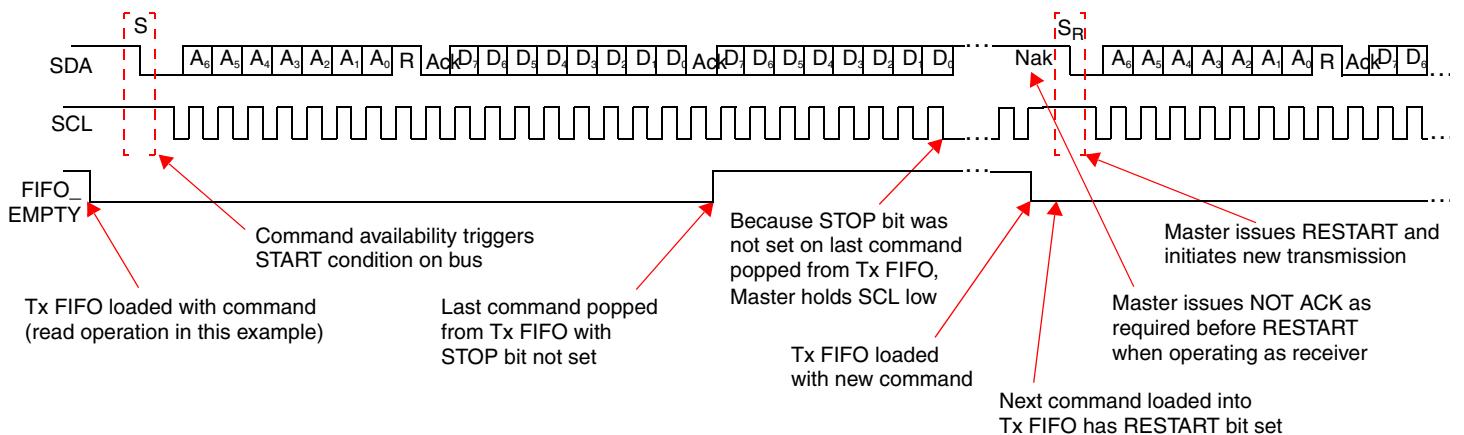


Figure 3-21 illustrates operation as a master receiver where the first command loaded after the Tx FIFO is allowed to empty and the Restart bit is set (IC_EMPTYFIFO_HOLD_MASTER_EN=1).

Figure 3-21 Master Receiver — First Command Loaded After Tx FIFO Allowed to Empty/Restart Bit Set (IC_EMPTYFIFO_HOLD_MASTER_EN=1 and IC_ULTRA_FAST_MODE=0)



3.6 Multiple Master Arbitration

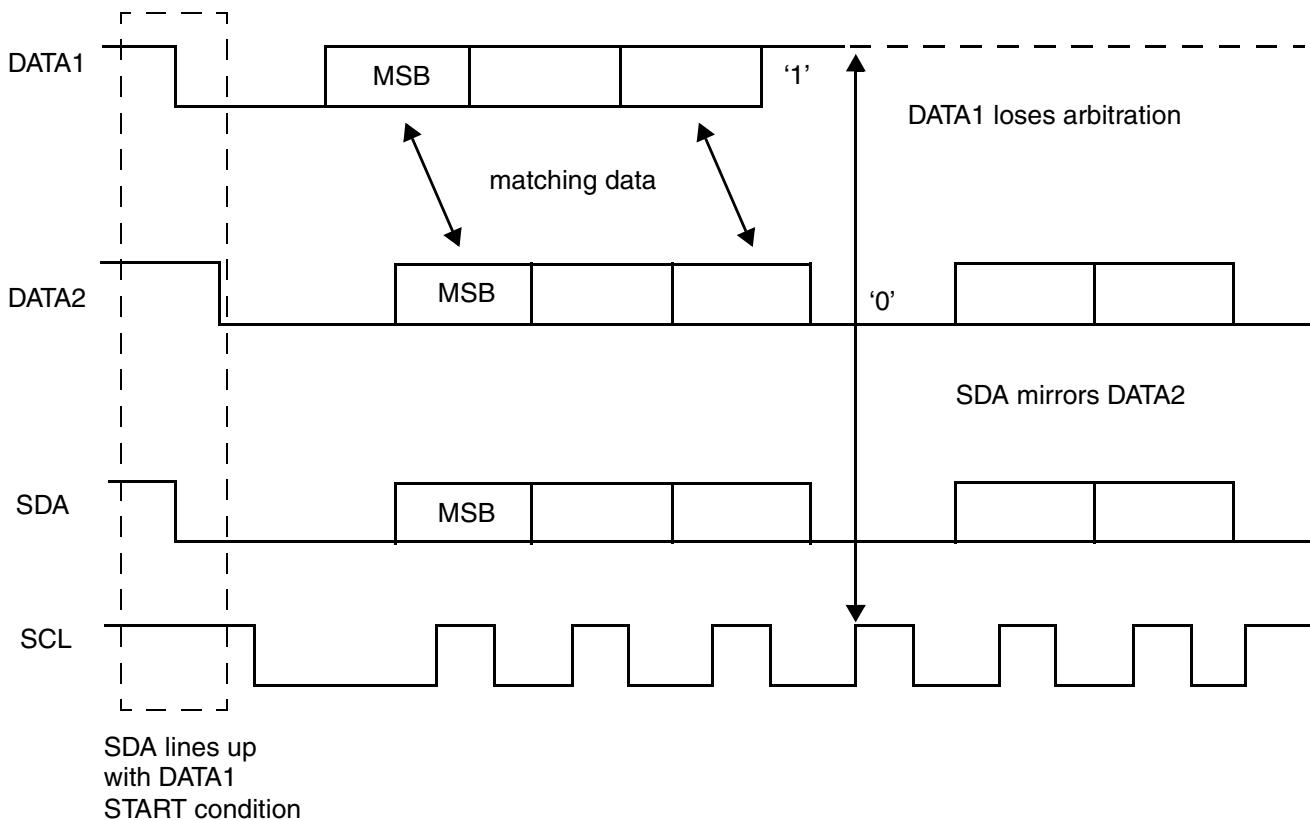
The DW_apb_i2c bus protocol allows multiple masters to reside on the same bus. If there are two masters on the same I²C-bus, there is an arbitration procedure if both try to take control of the bus at the same time by generating a START condition at the same time. Once a master (for example, a microcontroller) has control of the bus, no other master can take control until the first master sends a STOP condition and places the bus in an idle state.

Arbitration takes place on the SDA line, while the SCL line is 1. The master, which transmits a 1 while the other master transmits 0, loses arbitration and turns off its data output stage. The master that lost arbitration can continue to generate clocks until the end of the byte transfer. If both masters are addressing the same slave device, the arbitration could go into the data phase.

Upon detecting that it has lost arbitration to another master, the DW_apb_i2c will stop generating SCL (ic_clk_oe).

[Figure 3-22](#) illustrates the timing of when two masters are arbitrating on the bus.

Figure 3-22 Multiple Master Arbitration



For high-speed mode, the arbitration cannot go into the data phase because each master is programmed with a unique high-speed master code. This 8-bitcode is defined by the system designer and is set by writing to the High Speed Master Mode Code Address Register, [IC_HS_MADDR](#). Because the codes are unique, only one master can win arbitration, which occurs by the end of the transmission of the high-speed master code.

Control of the bus is determined by address or master code and data sent by competing masters, so there is no central master nor any order of priority on the bus.

Arbitration is not allowed between the following conditions:

- A RESTART condition and a data bit
- A STOP condition and a data bit
- A RESTART condition and a STOP condition

Slaves are not involved in the arbitration process.



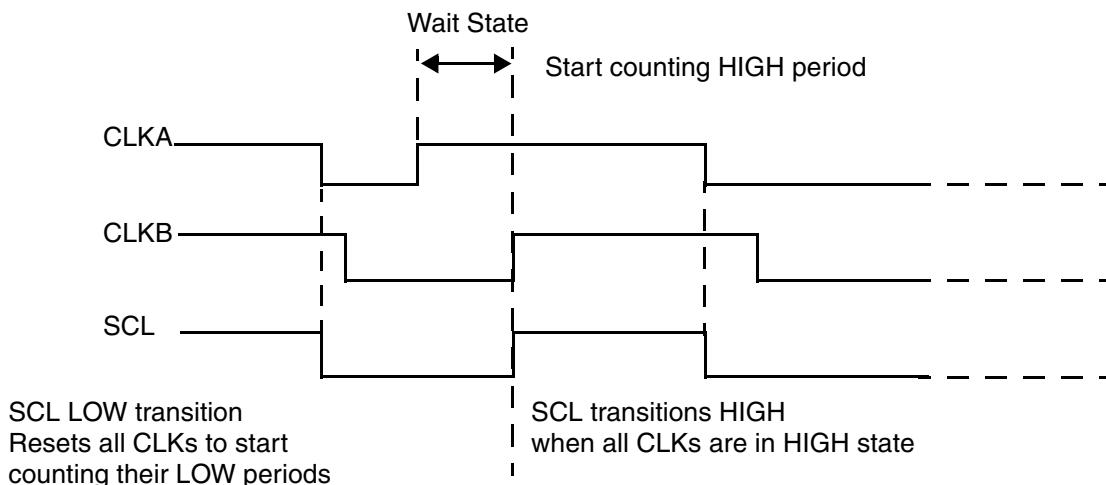
Note Multi-master arbitration is not applicable in Ultra-Fast Mode (IC_ULTRA_FAST_MODE=1) as single Master is present.

3.7 Clock Synchronization

When two or more masters try to transfer information on the bus at the same time, they must arbitrate and synchronize the SCL clock. All masters generate their own clock to transfer messages. Data is valid only during the high period of SCL clock. Clock synchronization is performed using the wired-AND connection to the SCL signal. When the master transitions the SCL clock to 0, the master starts counting the low time of the SCL clock and transitions the SCL clock signal to 1 at the beginning of the next clock period. However, if another master is holding the SCL line to 0, then the master goes into a HIGH wait state until the SCL clock line transitions to 1.

All masters then count off their high time, and the master with the shortest high time transitions the SCL line to 0. The masters then counts out their low time and the one with the longest low time forces the other master into a HIGH wait state. Therefore, a synchronized SCL clock is generated, which is illustrated in [Figure 3-23](#). Optionally, slaves may hold the SCL line low to slow down the timing on the I²C bus.

Figure 3-23 Multi-Master Clock Synchronization





Clock Synchronization is not supported in Ultra-Fast Mode (IC_ULTRA_FAST_MODE=1) as single master is present in the Ultra-Fast Mode system.

3.8 Operation Modes

This section provides information on operation modes.



It is important to note that the DW_apb_i2c should only be set to operate as an I²C Master, or I²C Slave, but not both simultaneously. This is achieved by ensuring that bit 6 (IC_SLAVE_DISABLE) and 0 (IC_MASTER_MODE) of the IC_CON register are never set to 0 and 1, respectively.

3.8.1 Slave Mode Operation

This section discusses slave mode procedures.

3.8.1.1 Initial Configuration

To use the DW_apb_i2c as a slave, perform the following steps:

1. Disable the DW_apb_i2c by writing a '0' to bit 0 of the IC_ENABLE register.
2. Write to the IC_SAR register (bits 9:0) to set the slave address. This is the address to which the DW_apb_i2c responds.
3. Write to the IC_CON register to specify which type of addressing is supported (7- or 10-bit by setting bit 3). Enable the DW_apb_i2c in slave-only mode by writing a '0' into bit 6 (IC_SLAVE_DISABLE) and a '0' to bit 0 (MASTER_MODE).



Slaves and masters do not have to be programmed with the same type of addressing 7- or 10-bit address. For instance, a slave can be programmed with 7-bit addressing and a master with 10-bit addressing, and vice versa.

4. Enable the DW_apb_i2c by writing a '1' in bit 0 of the IC_ENABLE register.



Depending on the reset values chosen, steps 2 and 3 may not be necessary because the reset values can be configured. For instance, if the device is only going to be a master, there would be no need to set the slave address because you can configure DW_apb_i2c to have the slave disabled after reset and to enable the master after reset. The values stored are static and do not need to be reprogrammed if the DW_apb_i2c is disabled.

Attention

It is recommended that the DW_apb_i2c Slave be brought out of reset only when the I²C bus is IDLE. De-asserting the reset when a transfer is ongoing on the bus causes internal synchronization flip-flops used to synchronize SDA and SCL to toggle from a reset value of 1 to the actual value on the bus. This can result in SDA toggling from 1 to 0 while SCL is 1, thereby causing a false START condition to be detected by the DW_apb_i2c Slave. This scenario can also be avoided by configuring the DW_apb_i2c with IC_SLAVE_DISABLE = 1 and IC_MASTER_MODE = 1 so that the Slave interface is disabled after reset. It can then be enabled by programming IC_CON[0] = 0 and IC_CON[6] = 0 after the internal SDA and SCL have synchronized to the value on the bus; this takes approximately 6 ic_clk cycles after reset de-assertion.

3.8.1.2 Slave-Transmitter Operation for a Single Byte

When another I²C master device on the bus addresses the DW_apb_i2c and requests data, the DW_apb_i2c acts as a slave-transmitter and the following steps occur:

1. The other I²C master device initiates an I²C transfer with an address that matches the slave address in the [IC_SAR](#) register of the DW_apb_i2c.
2. The DW_apb_i2c acknowledges the sent address and recognizes the direction of the transfer to indicate that it is acting as a slave-transmitter.
3. The DW_apb_i2c asserts the RD_REQ interrupt (bit 5 of the [IC_RAW_INTR_STAT](#) register) and holds the SCL line low. It is in a wait state until software responds.

If the RD_REQ interrupt has been masked, due to [IC_INTR_MASK\[5\]](#) register (M_RD_REQ bit field) being set to 0, then it is recommended that a hardware and/or software timing routine be used to instruct the CPU to perform periodic reads of the [IC_RAW_INTR_STAT](#) register.

- a. Reads that indicate [IC_RAW_INTR_STAT\[5\]](#) (R_RD_REQ bit field) being set to 1 must be treated as the equivalent of the RD_REQ interrupt being asserted.
- b. Software must then act to satisfy the I²C transfer.
- c. The timing interval used should be in the order of 10 times the fastest SCL clock period the DW_apb_i2c can handle. For example, for 400 kb/s, the timing interval is 25us.

Note

The value of 10 is recommended here because this is approximately the amount of time required for a single byte of data transferred on the I²C bus.

4. If there is any data remaining in the Tx FIFO before receiving the read request, then the DW_apb_i2c asserts a TX_ABRT interrupt (bit 6 of the [IC_RAW_INTR_STAT](#) register) to flush the old data from the TX FIFO.

Note

Because the DW_apb_i2c's Tx FIFO is forced into a flushed/reset state whenever a TX_ABRT event occurs, it is necessary for software to release the DW_apb_i2c from this state by reading the IC_CLR_TX_ABRT register before attempting to write into the Tx FIFO. See register [IC_RAW_INTR_STAT](#) for more details.

If the TX_ABRT interrupt has been masked, due to of [IC_INTR_MASK\[6\]](#) register (M_TX_ABRT bit field) being set to 0, then it is recommended that re-using the timing routine (described in the previous step), or a similar one, be used to read the [IC_RAW_INTR_STAT](#) register.

- a. Reads that indicate bit 6 (R_TX_ABRT) being set to 1 must be treated as the equivalent of the TX_ABRT interrupt being asserted.
 - b. There is no further action required from software.
 - c. The timing interval used should be similar to that described in the previous step for the [IC_RAW_INTR_STAT\[5\]](#) register.
 5. Software writes to the [IC_DATA_CMD](#) register with the data to be written (by writing a '0' in bit 8).
 6. Software must clear the RD_REQ and TX_ABRT interrupts (bits 5 and 6, respectively) of the [IC_RAW_INTR_STAT](#) register before proceeding.
- If the RD_REQ and/or TX_ABRT interrupts have been masked, then clearing of the [IC_RAW_INTR_STAT](#) register will have already been performed when either the R_RD_REQ or R_TX_ABRT bit has been read as 1.
7. The DW_apb_i2c releases the SCL and transmits the byte.
 8. The master may hold the I²C bus by issuing a RESTART condition or release the bus by issuing a STOP condition.



Note Slave-Transmitter Operation for a Single Byte is not applicable in Ultra-Fast Mode as Read transfers are not supported.

3.8.1.3 Slave-Receiver Operation for a Single Byte

When another I²C master device on the bus addresses the DW_apb_i2c and is sending data, the DW_apb_i2c acts as a slave-receiver and the following steps occur:

1. The other I²C master device initiates an I²C transfer with an address that matches the DW_apb_i2c's slave address in the [IC_SAR](#) register.
2. The DW_apb_i2c acknowledges the sent address and recognizes the direction of the transfer to indicate that the DW_apb_i2c is acting as a slave-receiver.
3. DW_apb_i2c receives the transmitted byte and places it in the receive buffer.



If the Rx FIFO is completely filled with data when a byte is pushed, and [IC_RX_FULL_HLD_BUS_EN](#) = 0, then an overflow occurs and the DW_apb_i2c continues with subsequent I²C transfers. Because a NACK is not generated, software must recognize the overflow when indicated by the DW_apb_i2c (by the R_RX_OVER bit in the [IC_INTR_STAT](#) register) and take appropriate actions to recover from lost data. Hence, there is a real time constraint on software to service the Rx FIFO before the latter overflows, as there is no way to re-apply pressure to the remote transmitting master. You must select a deep enough Rx FIFO depth to satisfy the interrupt service interval of the system.

If the Rx FIFO is completely filled with data when a byte is pushed, and [IC_RX_FULL_HLD_BUS_EN](#) = 1, then the DW_apb_i2c slave holds the I²C SCL line low until the Rx FIFO has some space, and then continues with the next read request.

4. DW_apb_i2c asserts the RX_FULL interrupt ([IC_RAW_INTR_STAT\[2\]](#) register).

If the RX_FULL interrupt has been masked, due to setting [IC_INTR_MASK\[2\]](#) register to 0 or setting [IC_TX_TL](#) to a value larger than 0, then it is recommended that a timing routine (described in “Slave-Transmitter Operation for a Single Byte” on page 57) be implemented for periodic reads of the [IC_STATUS](#) register. Reads of the IC_STATUS register, with bit 3 (RFNE) set at 1, must then be treated by software as the equivalent of the RX_FULL interrupt being asserted.

5. Software may read the byte from the [IC_DATA_CMD](#) register (bits 7:0).
6. The other master device may hold the I²C bus by issuing a RESTART condition, or release the bus by issuing a STOP condition.

3.8.1.4 Slave-Transfer Operation For Bulk Transfers

In the standard I²C protocol, all transactions are single byte transactions and the programmer responds to a remote master read request by writing one byte into the slave’s TX FIFO. When a slave (slave-transmitter) is issued with a read request (RD_REQ) from the remote master (master-receiver), at a minimum there should be at least one entry placed into the slave-transmitter’s TX FIFO. DW_apb_i2c is designed to handle more data in the TX FIFO so that subsequent read requests can take that data without raising an interrupt to get more data. Ultimately, this eliminates the possibility of significant latencies being incurred between raising the interrupt for data each time had there been a restriction of having only one entry placed in the TX FIFO.

This mode only occurs when DW_apb_i2c is acting as a slave-transmitter. If the remote master acknowledges the data sent by the slave-transmitter and there is no data in the slave’s TX FIFO, the DW_apb_i2c holds the I²C SCL line low while it raises the read request interrupt (RD_REQ) and waits for data to be written into the TX FIFO before it can be sent to the remote master.

If the RD_REQ interrupt is masked, due to bit 5 (M_RD_REQ) of the [IC_INTR_STAT](#) register being set to 0, then it is recommended that a timing routine be used to activate periodic reads of the [IC_RAW_INTR_STAT](#) register. Reads of [IC_RAW_INTR_STAT](#) that return bit 5 (R_RD_REQ) set to 1 must be treated as the equivalent of the RD_REQ interrupt referred to in this section. This timing routine is similar to that described in “Slave-Transmitter Operation for a Single Byte” on page 57.

The RD_REQ interrupt is raised upon a read request, and like interrupts, must be cleared when exiting the interrupt service handling routine (ISR). The ISR allows you to either write 1 byte or more than 1 byte into the Tx FIFO. During the transmission of these bytes to the master, if the master acknowledges the last byte, then the slave must raise the RD_REQ again because the master is requesting for more data.

If the programmer knows in advance that the remote master is requesting a packet of n bytes, then when another master addresses DW_apb_i2c and requests data, the Tx FIFO could be written with n number bytes and the remote master receives it as a continuous stream of data. For example, the DW_apb_i2c slave continues to send data to the remote master as long as the remote master is acknowledging the data sent and there is data available in the Tx FIFO. There is no need to hold the SCL line low or to issue RD_REQ again.

If the remote master is to receive n bytes from the DW_apb_i2c but the programmer wrote a number of bytes larger than n to the Tx FIFO, then when the slave finishes sending the requested n bytes, it clears the Tx FIFO and ignores any excess bytes.

The DW_apb_i2c generates a transmit abort (TX_ABRT) event to indicate the clearing of the Tx FIFO in this example. At the time an ACK/NACK is expected, if a NACK is received, then the remote master has all the data it wants. At this time, a flag is raised within the slave’s state machine to clear the leftover data in the

Tx FIFO. This flag is transferred to the processor bus clock domain where the FIFO exists and the contents of the Tx FIFO is cleared at that time.



Note Slave Transmitter Operation for Bulk Transfers is not applicable in Ultra-Fast Mode (IC_ULTRA_FAST_MODE=1) as Master Read Transfers are not supported.

3.8.2 Master Mode Operation

This section discusses master mode procedures.

3.8.2.1 Initial Configuration

The initial configuration procedure for Master Mode Operation depends on the configuration parameter I2C_DYNAMIC_TAR_UPDATE. When set to “Yes” (1), the target address and address format can be changed dynamically without having to disable DW_apb_i2c. This parameter only applies to when DW_apb_i2c is acting as a master because the slave requires the component to be disabled before any changes can be made to the address. For more information about this parameter, see [page 114](#). For more information about how this parameter affects the IC_TAR register, see [page 154](#).

The procedures are very similar and are only different with regard to where the IC_10BITADDR_MASTER bit is set (either bit 4 of IC_CON register or bit 12 of IC_TAR register).

3.8.2.1.1 I2C_DYNAMIC_TAR_UPDATE = 0

To use the DW_apb_i2c as a master when the I2C_DYNAMIC_TAR_UPDATE configuration parameter is set to “No” (0), perform the following steps:

1. Disable the DW_apb_i2c by writing 0 to bit 0 of the [IC_ENABLE](#) register.
2. Write to the [IC_CON](#) register to set the maximum speed mode supported (bits 2:1) and the desired speed of the DW_apb_i2c master-initiated transfers, either 7-bit or 10-bit addressing (bit 4). Ensure that bit 6 (IC_SLAVE_DISABLE) is written with a ‘1’ and bit 0 (MASTER_MODE) is written with a ‘1’.



Note Slaves and masters do not have to be programmed with the same type of addressing 7- or 10-bit address. For instance, a slave can be programmed with 7-bit addressing and a master with 10-bit addressing, and vice versa.

3. Write to the [IC_TAR](#) register the address of the I²C device to be addressed (bits 9:0). This register also indicates whether a General Call or a START BYTE command is going to be performed by I²C.
4. *Only applicable for high-speed mode transfers.* Write to the [IC_HS_MADDR](#) register the desired master code for the DW_apb_i2c. The master code is programmer-defined.
5. Enable the DW_apb_i2c by writing a 1 to bit 0 of the [IC_ENABLE](#) register.
6. Now write transfer direction and data to be sent to the [IC_DATA_CMD](#) register. If the [IC_DATA_CMD](#) register is written before the DW_apb_i2c is enabled, the data and commands are lost as the buffers are kept cleared when DW_apb_i2c is disabled.

This step generates the START condition and the address byte on the DW_apb_i2c. Once DW_apb_i2c is enabled and there is data in the TX FIFO, DW_apb_i2c starts reading the data.



Note Depending on the reset values chosen, steps 2, 3, 4, and 5 may not be necessary because the reset values can be configured. The values stored are static and do not need to be reprogrammed if the DW_apb_i2c is disabled, with the exception of the transfer direction and data.

3.8.2.1.2 I2C_DYNAMIC_TAR_UPDATE = 1

To use the DW_apb_i2c as a master when the I2C_DYNAMIC_TAR_UPDATE configuration parameter is set to "Yes" (1), perform the following steps:

1. Disable the DW_apb_i2c by writing 0 to bit 0 of the **IC_ENABLE** register.
2. Write to the **IC_CON** register to set the maximum speed mode supported for slave operation (bits 2:1) and to specify whether the DW_apb_i2c starts its transfers in 7/10 bit addressing mode when the device is a slave (bit 3).
3. Write to the **IC_TAR** register the address of the I²C device to be addressed. It also indicates whether a General Call or a START BYTE command is going to be performed by I²C. The desired speed of the DW_apb_i2c master-initiated transfers, either 7-bit or 10-bit addressing, is controlled by the **IC_10BITADDR_MASTER** bit field (bit 12).
4. *Only applicable for high-speed mode transfers.* Write to the **IC_HS_MADDR** register the desired master code for the DW_apb_i2c. The master code is programmer-defined.
5. Enable the DW_apb_i2c by writing a 1 to bit 0 of the **IC_ENABLE** register.
6. Now write the transfer direction and data to be sent to the **IC_DATA_CMD** register. If the **IC_DATA_CMD** register is written before the DW_apb_i2c is enabled, the data and commands are lost as the buffers are kept cleared when DW_apb_i2c is not enabled.



Note When a DW_apb_i2c Master is configured with **IC_EMPTYFIFO_HOLD_MASTER_EN** = 0, then for multiple I²C transfers, perform additional writes to the Tx FIFO such that the Tx FIFO does not become empty during the I²C transaction. If the Tx FIFO is completely emptied at any stage, then further writes to the Tx FIFO results in an independent I²C transaction.

3.8.2.2 Dynamic IC_TAR or IC_10BITADDR_MASTER Update

The DW_apb_i2c supports dynamic updating of the **IC_TAR** (bits 9:0) and **IC_10BITADDR_MASTER** (bit 12) bit fields of the **IC_TAR** register. In order to perform a dynamic update of the **IC_TAR** register, the **I2C_DYNAMIC_TAR_UPDATE** configuration parameter must be set to Yes (1). You can dynamically write to the **IC_TAR** register provided the software ensures that there are no other commands in the Tx FIFO that use the existing TAR address. If the software does not ensure this, then **IC_TAR** should be re-programmed only if the following conditions are met:

- DW_apb_i2c is not enabled (**IC_ENABLE[0]**=0);

OR

DW_apb_i2c is enabled (**IC_ENABLE[0]**=1); AND
 DW_apb_i2c is NOT engaged in any Master (tx, rx) operation (**IC_STATUS[5]**=0); AND
 DW_apb_i2c is enabled to operate in Master mode (**IC_CON[0]**=1); AND
 there are NO entries in the Tx FIFO (**IC_STATUS[2]**=1);¹

You can change the TAR address dynamically without losing the bus, only if the following conditions are met.

- DW_apb_i2c is enabled (**IC_ENABLE[0]**=1); AND
IC_EMPTYFIFO_HOLD_MASTER_EN configuration parameter is set to 1; AND
 DW_apb_i2c is enabled to operate in Master mode (**IC_CON[0]**=1); AND
 there are NO entries in the Tx FIFO and the master is in HOLD state (**IC_INTR_STAT[13]**=1);¹



Note DW_apb_i2c uses the TAR address if either of the following conditions is true:

- The command has either RESTART or STOP bit set.
- The direction is changed in commands with a read command following a write command or vice versa

The updated TAR address comes into effect only when the next START or RESTART occurs on the bus.

3.8.2.3 Master Transmit and Master Receive

The DW_apb_i2c supports switching back and forth between reading and writing dynamically. To transmit data, write the data to be written to the lower byte of the I²C Rx/Tx Data Buffer and Command Register (**IC_DATA_CMD**). The **CMD** bit [8] should be written to 0 for I²C write operations. Subsequently, a read command may be issued by writing “don’t cares” to the lower byte of the **IC_DATA_CMD** register, and a 1 should be written to the **CMD** bit. The DW_apb_i2c master continues to initiate transfers as long as there are commands present in the transmit FIFO. If the transmit FIFO becomes empty – depending on the value of **IC_EMPTYFIFO_HOLD_MASTER_EN**, the master either inserts a STOP condition after completing the current transfers, or it checks to see if **IC_DATA_CMD[9]** is set to 1.

- If set to 1, it issues a STOP condition after completing the current transfer.
- If set to 0, it holds SCL low until next command is written to the transmit FIFO.

For more details, refer to “[Tx FIFO Management and START, STOP and RESTART Generation](#)” on page 48.



Note Master Receiver Mode is not supported in Ultra-Fast Mode (**IC_ULTRA_FAST_MODE**=1) as Master Read transfers are not supported.

3.8.3 Disabling DW_apb_i2c

The register **IC_ENABLE_STATUS** is added to allow software to unambiguously determine when the hardware has completely shutdown in response to bit 0 of the **IC_ENABLE** register being set from 1 to 0.

1. If the software or application is aware the the DW_apb_i2c is not using the TAR address for the pending commands in the Tx FIFO, then it is possible to update the TAR address even while the Tx FIFO has entries (**IC_STATUS[2]**=0).

Only one register is required to be monitored, as opposed to monitoring two registers (IC_STATUS and IC_RAW_INTR_STAT) which is a requirement for DW_apb_i2c versions 1.05a or earlier.



Note When IC_EMPTYFIFO_HOLD_MASTER_EN = 1, the DW_apb_i2c Master can be disabled only if the current command being processed—when the ic_enable de-assertion occurs—has the STOP bit set to 1.

When an attempt is made to disable the DW_apb_i2c Master while processing a command without the STOP bit set, the DW_apb_i2c Master continues to remain active, holding the SCL line low until a new command is received in the Tx FIFO.

3.8.3.1 Procedure

1. Define a timer interval (t_{i2c_poll}) equal to the 10 times the signaling period for the highest I²C transfer speed used in the system and supported by DW_apb_i2c. For example, if the highest I²C transfer mode is 400 kb/s, then this t_{i2c_poll} is 25us.
2. Define a maximum time-out parameter, MAX_T_POLL_COUNT, such that if any repeated polling operation exceeds this maximum value, an error is reported.
3. Execute a blocking thread/process/function that prevents any further I²C master transactions to be started by software, but allows any pending transfers to be completed.



This step can be ignored if DW_apb_i2c is programmed to operate as an I²C slave only.

4. The variable POLL_COUNT is initialized to zero.
5. Set bit 0 of the **IC_ENABLE** register to 0.
6. Read the IC_ENABLE_STATUS register and test the IC_EN bit (bit 0). Increment POLL_COUNT by one. If POLL_COUNT >= MAX_T_POLL_COUNT, exit with the relevant error code.
7. If IC_ENABLE_STATUS[0] is 1, then sleep for t_{i2c_poll} and proceed to the previous step. Otherwise, exit with a relevant success code.

3.8.4 Aborting I2C Transfers

The ABORT control bit of the IC_ENABLE register allows the software to relinquish the I2C bus before completing the issued transfer commands from the Tx FIFO. In response to an ABORT request, the controller issues the STOP condition over the I2C bus, followed by Tx FIFO flush. Aborting the transfer is allowed only in master mode of operation.

3.8.4.1 Procedure

1. Stop filling the Tx FIFO (IC_DATA_CMD) with new commands.
2. When operating in DMA mode, disable the transmit DMA by setting TDMAE to 0.
3. Set bit 1 of the **IC_ENABLE** register (ABORT) to 1.
4. Wait for the M_TX_ABRT interrupt.

5. Read the IC_TX_ABRT_SOURCE register to identify the source as ABRT_USER_ABRT.

3.9 Spike Suppression

The DW_apb_i2c contains programmable spike suppression logic that match requirements imposed by the *I²C Bus Specification* for SS/FS (tSP, Table 9), HS (tSP, Table 11), and UFm (tSP, Table 13) modes.

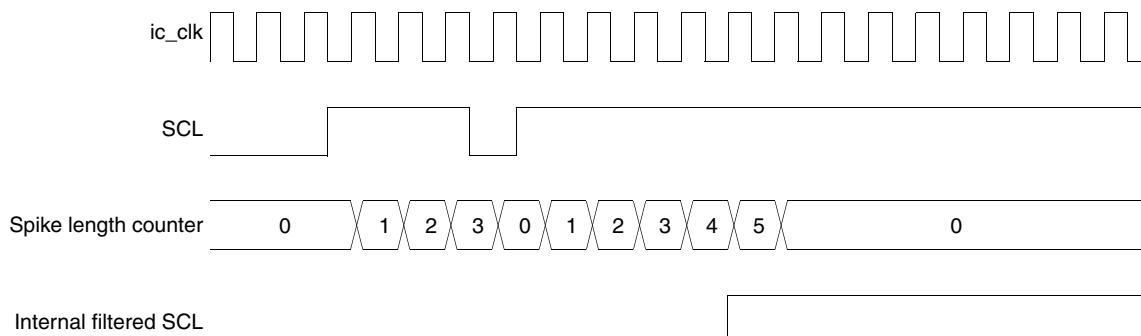
This logic is based on counters that monitor the input signals (SCL and SDA), checking if they remain stable for a predetermined amount of ic_clk cycles before they are sampled internally. There is one separate counter for each signal (SCL and SDA). The number of ic_clk cycles can be programmed by the user and should be calculated taking into account the frequency of ic_clk and the relevant spike length specification.

Each counter is started whenever its input signal changes its value. Depending on the behavior of the input signal, one of the following scenarios occurs:

- The input signal remains unchanged until the counter reaches its count limit value. When this happens, the internal version of the signal is updated with the input value, and the counter is reset and stopped. The counter is not restarted until a new change on the input signal is detected.
- The input signal changes again before the counter reaches its count limit value. When this happens, the counter is reset and stopped, but the internal version of the signal is not updated. The counter remains stopped until a new change on the input signal is detected.

The timing diagram in [Figure 3-24](#) illustrates the behavior described above.

Figure 3-24 Spike Suppression Example



The count limit value used in this example is 5 and was calculated for a 10 ns ic_clk period and for SS/FS operation (50 ns spike suppression).



Note There is a 2-stage synchronizer on the SCL input, but for the sake of simplicity this synchronization delay was not included in the timing diagram in [Figure 3-24](#).

The *I²C Bus Specification* calls for different maximum spike lengths according to the operating mode—50 ns for SS and FS; 10 ns for HS, 10 ns for UFm, so three registers are required to store the values needed for each case:

- Register IC_FS_SPKLEN holds the maximum spike length for SS and FS modes
- Register IC_HS_SPKLEN holds the maximum spike value for HS mode.

- Register IC_UFM_SPKLEN holds the maximum spike value for UFm.



- IC_HS_SPKLEN is implemented only if the component is configured for HS operation; that is, (IC_MAX_SPEED = High).
- IC_UFM_SPKLEN is implemented only if the component is configured for Ultra-Fast mode; that is, (IC_ULTRA_FAST_MODE=1).
- IC_FS_SPKLEN and IC_HS_SPKLEN are not implemented when configured for Ultra-Fast mode; that is, (IC_ULTRA_FAST_MODE=1).

These registers are 8 bits wide and accessible through the APB interface for read and write purposes; however, they can be written to only when the DW_apb_i2c is disabled. The minimum value that can be programmed into these registers is 1; attempting to program a value smaller than 1 results in the value 1 being written.

The default value for these registers is automatically calculated in coreConsultant based on the value of ic_clk period, but this value can be overridden by the user when configuring the component.



- Because the minimum value that can be programmed into the IC_FS_SPKLEN, IC_HS_SPKLEN, and IC_UFM_SPKLEN registers is 1, the spike length specification can be exceeded for low frequencies of ic_clk. Consider the simple example of a 10 MHz (100 ns period) ic_clk; in this case, the minimum spike length that can be programmed is 100 ns, which means that spikes up to this length are suppressed.
 - Standard synchronization logic (two flip-flops in series) is implemented upstream of the spike suppression logic and is not affected in any way by the contents of the spike length registers or the operation of the spike suppression logic; the two operations (synchronization and spike suppression) are completely independent.
- Because the SCL and SDA inputs are asynchronous to ic_clk, there is one ic_clk cycle uncertainty in the sampling of these signals; that is, depending on when they occur relative to the rising edge of ic_clk, spikes of the same original length might show a difference of one ic_clk cycle after being sampled.
- Spike suppression is symmetrical; that is, the behavior is exactly the same for transitions from 0 to 1 and from 1 to 0.

3.10 Fast Mode Plus Operation

In fast mode plus, the DW_apb_i2c allows the fast mode operation to be extended to support speeds up to 1000 Kb/s. To enable the DW_apb_i2c for fast mode plus operation, perform the following steps before initiating any data transfer:

1. Configure the Maximum Speed mode of DW_apb_i2c Master or Slave to Fast Mode or High Speed mode (IC_MAX_SPEED_MODE > 2).
2. Set ic_clk frequency greater than or equal to 32 MHz (refer to “[Standard Mode \(SM\), Fast Mode \(FM\), and Fast Mode Plus \(FM+\) with IC_CLK_FREQ_OPTIMIZATION = 0](#)” on page 82).
3. Program the IC_CON register [2:1] = 2'b10 for fast mode or fast mode plus.
4. Program IC_FS_SCL_LCNT and IC_FS_SCL_HCNT registers to meet the fast mode plus SCL (refer to “[IC_CLK Frequency Configuration](#)” on page 79).

5. Program the [IC_FS_SPKLEN](#) register to suppress the maximum spike of 50ns.
6. Program the [IC_SDA_SETUP](#) register to meet the minimum data setup time (t_{SU} ; DAT).

3.11 Bus Clear Feature

DWC_apb_i2c supports the bus clear feature that provides graceful recovery of data (SDA) and clock (SCL) lines during unlikely events in which either the clock or data line is stuck at LOW.

The following sections describes the SDA and SCL lines stuck at LOW recovery mechanisms:

- “[SDA Line Stuck at LOW Recovery](#)” on page [66](#)
- “[SCL Line is Stuck at LOW](#)” on page [67](#)

3.11.1 SDA Line Stuck at LOW Recovery

In case of SDA line stuck at LOW, the master performs the following actions to recover as shown in [Figure 3-25](#) and [Figure 3-26](#):

1. Master sends a maximum of 9 clock pulses to recover the bus LOW within those 9 clocks.
 - The number of clock pulses will vary with the number of bits that remain to be sent by the slave. As the maximum number of bits is 9, master sends up to 9 clock pluses and allows the slave to recover it.
 - The master attempts to assert a Logic 1 on the SDA line and check whether SDA is recovered. If the SDA is not recovered, it will continue to send a maximum of 9 SCL clocks.
2. If SDA line is recovered within 9 clock pulses then the master will send the STOP to release the bus.
3. If SDA line is not recovered even after the 9th clock pulse then system needs a hardware reset.

The detailed flow to recover the SDA stuck at LOW is explained in the section “[Programming Flow for SCL and SDA Bus Recovery](#)” on page [256](#).

Figure 3-25 SDA Recovery with 9 SCL Clocks

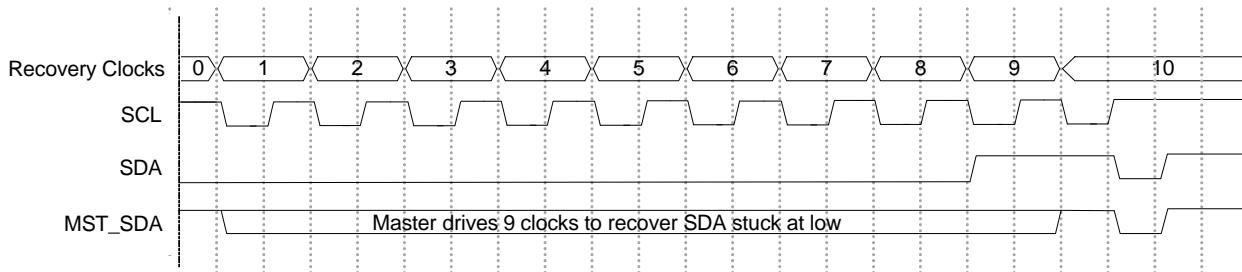
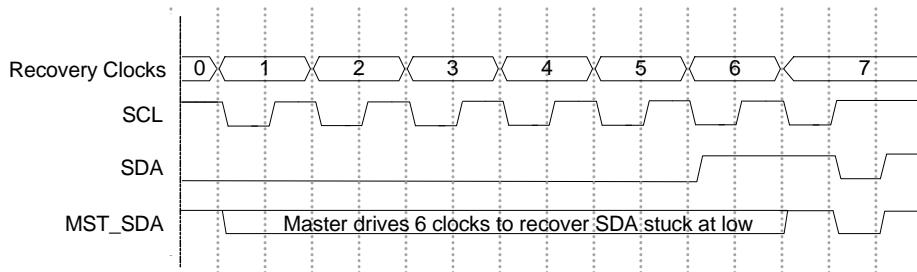


Figure 3-26 SDA Recovery with 6 SCL Clocks

3.11.2 SCL Line is Stuck at LOW

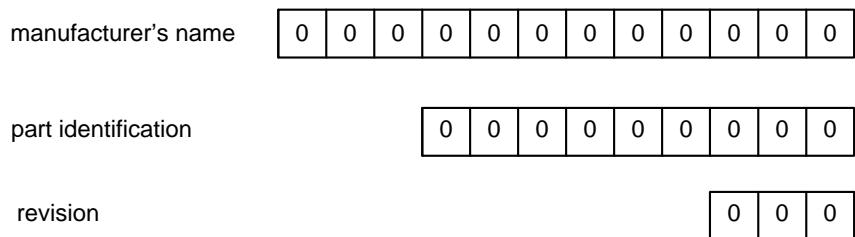
In the unlikely event (due to an electric failure of a circuit) where the clock (SCL) is stuck to LOW, there is no effective method to overcome this problem but to reset the bus using the hardware reset signal. The detailed flow to recover the SCL stuck at LOW is explained in “[Programming Flow for SCL and SDA Bus Recovery](#)” on page [256](#).

3.12 Device ID

A Device ID field is an optional 3-byte read-only (24 bits) word, which provides the following information:

- Twelve bits with the manufacturer’s name, which is unique for every manufacturer.
- Nine bits with the part identification, which is assigned by the manufacturer.
- Three bits with the die revision, which is assigned by the manufacturer.

[Figure 3-27](#) shows the Device ID field structure.

Figure 3-27 Device ID Field Structure

For reading the Device ID of a particular slave, the master can follow the procedure in “[Programming Flow for Reading the Device ID](#)” on page [257](#). The Device ID that is read will be available in RX FIFO, which can be read using IC_DATA_CMD register.

In case of a slave, the user has to configure the Device ID using the IC_DEVICE_ID_VALUE coreConsultant parameter and user can read the Device ID of the slave using IC_DEVICE_ID register.



Note Device ID is not supported for 10-bit addressing and High Speed transfers (HS mode).

3.13 Ultra-Fast Speed Mode

The Ultra-Fast Speed mode is a variant of I2C Bus Speed mode that operates from DC (0) to 5 MHz transmitting data in one direction. It is useful for speeds greater than 1 MHz to drive LED controllers and other gaming systems that do not need feedback.

Ultra-Fast speed mode is based on the standard I2C Protocol, which consists of START, slave address, command bit, ninth clock (ACK cycle) and a STOP bit. The command bit should be always 'write' (0) only since it is a unidirectional bus (except for the START byte). The data bit on the ninth (ACK) cycle is driven high by the master, ignoring the ACK cycle due to unidirectional nature of bus. The driver used for Ultra-Fast Mode is push-pull driver.

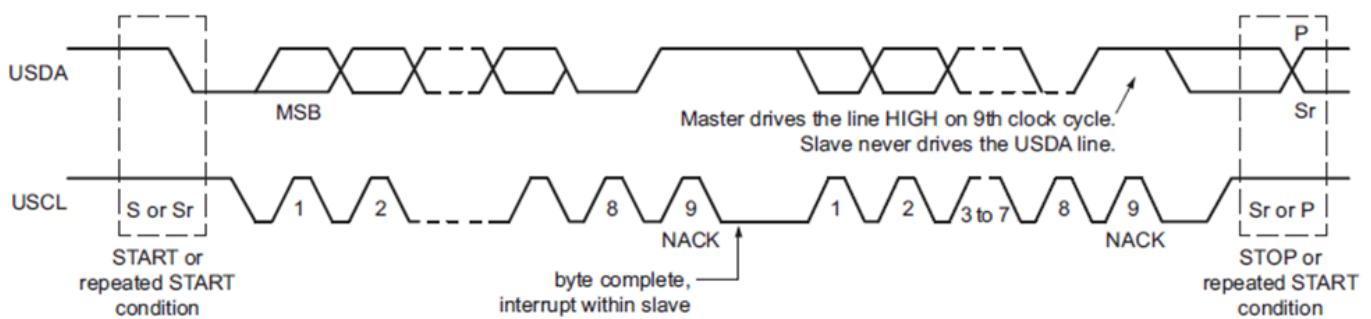
The Master consists of serial clock (ic_clk_oe, USCL) and a serial data (ic_data_oe, USDA) output signals. The Output signals are Active-Low in nature.

The Slave consists of serial clock (ic_clk_in_a, USCL) and serial data (ic_data_in_a, USDA) input signals. The input signals are Active-High in nature.

The UFm I2C-bus does not have the multi-master capability and hence, it does not consist of wired-AND open-drain driver. In the UFm I2C bus, the master is the only device that initiates a data transfer (write transfer) on the bus and provides the clock signals to support that transfer. All other devices are considered as slaves. Because of single master support, the arbitration, synchronization, clock stretching mechanisms are not applicable.

The Byte format, START and STOP generation are same as in other modes of the I2C Protocol except for the ignorance of ACK cycle. The Slave never drives anything on the bus hence, the master always drives NACK during the ninth cycle of the transfer as shown in [Figure 3-28](#).

Figure 3-28 UFm-I2C Byte Transfer

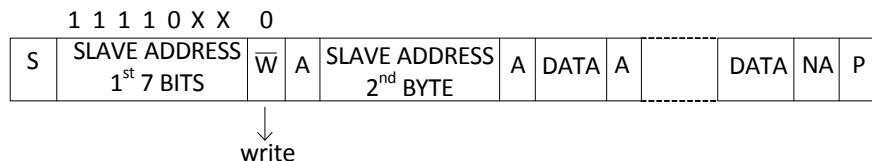


In UFm-I2C mode, the slave is not allowed to hold the clock LOW if it cannot receive another complete byte of data or while it is performing some other function, for example, servicing an internal interrupt. The ninth clock cycle that represents ACK/NACK of the byte is not applicable as slave will not respond and it is preserved in UFm to be compatible with the I2C Protocol. The 8th bit of the address that represents Read or

write transfer should be always set to write (0), since Read is not supported in UFm (except for the START Byte).

The Combined format of I2C Protocol is not supported in UFm-I2C mode. The 10-bit addressing that expands the number of possible devices is supported in UFm-I2C mode and it behaves similar to other modes as shown in [Figure 3-29](#) (Only write transfer is supported).

Figure 3-29 10-bit addressing write transfer



The UFm-I2C mode supports START byte and general call features similar to other I2C modes. If the slave is not responsive (determined through external feedback and not through UFm I2C-bus), then the slave can reset through software reset or external hardware reset.

3.14 SMBus/PMBus

The SMBus is designed to provide a predictable communication line between a system and its devices. It describes the Device timeout definitions and their conditions.

3.14.1 t_{Timeout,MIN} Parameter

This Parameter allows a master or slave to conclude that a defective device is holding the clock low indefinitely or a master is intentionally trying to drive devices off the bus. It is highly recommended that a slave device release the bus (stop driving the bus and let SMBCLK and SMBDAT float high) when it detects any single clock held low longer than tTIMEOUT,MIN. Devices that have detected this condition must reset their communication interface and be able to receive a new START condition in no later than tTIMEOUT,MAX.

The DW_apb_i2c enables the Bus clear feature in SMBus mode and the user can use the IC_SCL_STUCK_TIMEOUT Register to program the tTIMEOUT,MIN Value to detect the SMBCLK low timeout.

The DW_apb_i2c slave device will reset its communication interface and release both SCL and SDA lines after detecting the SCL_STUCK_TIMEOUT interrupt.

The DW_apb_i2c master has a provision to generate the Abort which completes the current transfer and generate STOP condition on the bus through programming the IC_ENABLE[1] register bit.

3.14.2 Master Device Clock Extension

The interval tLOW: MEXT is defined as the cumulative time a master device is allowed to extend its clock cycles within one byte in a message as measured from:

- START to ACK
- ACK to ACK

- ACK to STOP.

The DW_apb_i2c Master uses the IC_SMBUS_CLOCK_LOW_MEXT register to detect the Master device clock extension timeout and generates SMBUS_CLK_LOW_MEXT interrupt.

3.14.3 Slave Device Clock Extension

The interval tLOW:SEXT is the cumulative time a given slave device is allowed to extend the clock cycles in one message from the initial START to the STOP.

The DW_apb_i2c Master uses the IC_SMBUS_CLOCK_LOW_SEXT register to detect the Slave device clock extension timeout and generates SMBUS_CLK_LOW_SEXT interrupt.

A Master is allowed to abort the transaction in progress to any slave that violates the tLOW:SEXT or tTIMEOUT,MIN specifications through the enabling the user abort (IC_ENABLE[1]).

3.14.4 SMBDAT Low Timeout

A malfunctioning device holds the SMBDAT line low indefinitely. This would prevent the master from issuing a STOP condition and ending a transaction. If SMBDAT is still low tTIMEOUT,MAX after SMBCLK has gone high at the end of a transaction the master should hold SMBCLK low for at least tTIMEOUT,MAX in an attempt to reset the SMBus interface of all of the devices on the bus.

The DW_apb_i2c enables the Bus clear feature in SMBus mode and the user can use the IC_SDA_STUCK_TIMEOUT Register to program the SMBDAT timeout value to detect the SMBDAT low timeout. If SMBDAT line is stuck at low, the SDA_STUCK_TIMEOUT abort is generated and software can enable the SMBUS_CLK_RESET register bit of IC_ENABLE register to hold the SCL low for IC_SCL_STUCK_TIMEOUT which in turn resets the SMBus interface of all devices on the bus.

3.14.5 Bus Protocols

A typical SMBus device will have a set of commands by which data can be read and written. All commands are one byte long while their arguments and return values can vary in length. In accordance with the SMBus specification, the most significant bit (MSB) is transferred first. There are eleven possible command protocols for any given device. These commands are Quick Command, Send Byte, Receive Byte, Write Byte, Write Word, Read Byte, Read Word, Process Call, Block Read, Block Write, and Block Write-Block Read Process Call.

SMBus protocols for message transactions are generally different from I2C data transfer commands. It is still possible to program an SMBus master to deliver I2C data transfer commands. The following table describes the derivation of SMBus Bus Protocols through Tx-FIFO commands in DW_apb_i2c.

In the SMBus Master mode, all the receive data bytes will be available in Rx-FIFO. In the SMBus Slave mode, all the bus protocol command codes and data bytes will received in the Rx-FIFO and read request data bytes must be sent using Tx-FIFO, similar to the I2C mode.

Table 3-2 SMBus Bus Protocols Usage in DW_apb_i2c

Protocol	Required TxFIFO Commands	Command/Data (IC_DATA_CMD[7:0])	CMD bit (IC_DATA_CMD[8])	STOP bit (IC_DATA_CMD[9])	Remarks
Quick Command	1	Not Applicable	Set the command [R/W]	Set to 1	Set IC_TAR[11] and IC_TAR[16] to 1
Send Byte	1	Data Byte	Set to 0	Set to 1	
Receive Byte	1	Not Applicable	Set to 1	Set to 1	
Write Byte	2	Command Code	Set to 0	Set to 0	
		Data Byte	Set to 0	Set to 1	
Write Word	3	Command Code	Set to 0	Set to 0	
		Data Byte Low	Set to 0	Set to 0	
		Data Byte High	Set to 0	Set to 1	
Read Byte	2	Command Code	Set to 0	Set to 0	
		Not Applicable	Set to 1	Set to 1	
Read Word	3	Command Code	Set to 0	Set to 0	
		Not Applicable	Set to 1	Set to 0	
		Not Applicable	Set to 1	Set to 1	
Process Call	5	Command Code	Set to 0	Set to 0	
		Data Byte Low	Set to 0	Set to 0	
		Data Byte High	Set to 0	Set to 0	
		Not Applicable	Set to 1	Set to 0	
		Not Applicable	Set to 1	Set to 1	
Block Write	N+1	Command Code	Set to 0	Set to 0	
		Data Byte	Set to 0	Set to 0	
		N+1) Data Byte N	Set to 0	Set to 1	
Block Read	N+1	Command Code	Set to 0	Set to 0	
		Not Applicable	Set to 0	Set to 0	
		N+1) Not Applicable	Set to 0	Set to 1	

Table 3-2 SMBus Bus Protocols Usage in DW_apb_i2c

Protocol	Required TxFIFO Commands	Command/Data (IC_DATA_CMD[7:0])	CMD bit (IC_DATA_CMD[8])	STOP bit (IC_DATA_CMD[9])	Remarks
Block Write-Block Read Process Call	M+N+1	Command Code	Set to 0	Set to 0	
		Data Byte 1	Set to 0	Set to 0	
		M+1) Data Byte M	Set to 0	Set to 0	
		M+2) Not Applicable	Set to 1	Set to 0	
		M+3) Not Applicable	Set to 1	Set to 0	
		M+N+1) Not Applicable	Set to 1	Set to 1	
SMBUS Host Notify Protocol	3	Data Byte Low	Set to 0	Set to 0	Set IC_TAR[6:0] to SMB Host Address (0001 000)
		Data Byte High	Set to 0	Set to 1	

DW_apb_i2c Slave can be enabled to receive only Quick command through enabling the SLAVE_QUICK_CMD_EN bit in the IC_CON Register. Whenever this bit is selected the slave only receives quick commands and will not accept other Bus Protocols. The DW_apb_i2c slave issues the SMBUS_QUICK_DET interrupt upon receiving the QUICK command.

SMBus introduces a Packet Error checking Mechanism through appending PEC Byte at the end of the Bus Protocol. This can be achieved through adding an extra command (PEC byte) while transferring and decoding it while receiving by the software.

3.14.6 SMBUS Address Resolution Protocol

SMBus slave address conflicts can be resolved by dynamically assigning a new unique address to each slave device by the Host. This feature allows the devices to be 'hot-plugged' in to the system.

SMBus introduces a 128-bit Unique Device ID (UDID) for each device in the system to isolate each device for the purpose of address assignment. DW_apb_i2c uses the IC_SMBUS_UDID_MSB parameter for upper constant 96 bits and 'IC_SMBUS_ARP_UDID_LSB' register for lower variable 32 bits of the UDID.

DW_apb_i2c uses the PERSISTANT_SLV_ADDR_EN register bit in IC_CON register to indicate whether the DW_apb_i2c supports persistent slave address.

DW_apb_i2c master can issue general and directed Address Resolution Protocol (ARP) commands to assign the dynamic address for the slaves in the SMBus system.

Table 3-3 describes the derivation of SMBus ARP commands through Tx-FIFO commands in DW_apb_i2c.

Table 3-3 Derivation of SMBus ARP Command Through TxFIFO Commands in DW_apb_i2c

ARP Command	Required Tx_FIFO Commands	Command/Data (IC_DATA_CMD[7:0])	CMD Bit (IC_DATA_CMD[8])	STOP bit (IC_DATA_CMD[9])	Remarks
Prepare for ARP	2	Command = '0000 0001'	Set to 0	Set to 0	Set IC_TAR[6:0] to SMB Default Address (1100 001)
		PEC Byte	Set to 0	Set to 1	
Reset Device (General)	2	Command = '0000 0010'	Set to 0	Set to 0	Set IC_TAR[6:0] to SMB Default Address (1100 001)
		PEC Byte	Set to 0	Set to 1	
Get UDID (General)	20	Command = '0000 0011'	Set to 0	Set to 0	1. Set IC_TAR[6:0] to SMB Default Address (1100 001). 2. 16 Reads to be performed for the 128 UDID bytes. 3. Last read command for the slave address.
		Not Applicable	Set to 1	Set to 0	
		Not Applicable	Set to 1	Set to 0	
		Not Applicable	Set to 1	Set to 0	
		PEC Byte	Set to 1	Set to 1	
Assign Address	20	Command = '0000 0011'	Set to 0	Set to 0	1. Set IC_TAR[6:0] to SMB Default Address (1100 001). 2. 16 Writes to be performed for the 128 UDID byte. 3. Last Write command for the Assigned slave address.
		Byte Count = 17	Set to 0	Set to 0	
		UDID Byte 15	Set to 0	Set to 0	
		UDID Byte 14	Set to 0	Set to 0	
		Assigned Address	Set to 0	Set to 0	
		PEC Byte	Set to 01	Set to 1	
Get UDID (Directed)	19	Command = '0000 0011'	Set to 0	Set to 0	1. Set IC_TAR[6:0] to SMB Default Address (1100 001). 2. 16 Reads to be performed for the 128 UDID byte. 3. Last Read command for the slave address.
		Slave address[6:0],1}	Set to 1	Set to 0	
		Not Applicable	Set to 1	Set to 0	
		Not Applicable	Set to 1	Set to 0	
		PEC Byte	Set to 1	Set to 1	

Table 3-3 Derivation of SMBus ARP Command Through TxFIFO Commands in DW_apb_i2c

ARP Command	Required Tx_FIFO Commands	Command/Data (IC_DATA_CMD[7:0])	CMD Bit (IC_DATA_CMD[8])	STOP bit (IC_DATA_CMD[9])	Remarks
Reset Device (Directed)	2	command = {slave address[6:0],0}	Set to 0	Set to 0	Set IC_TAR[6:0] to SMB Default Address (1100 001)
		PEC byte	Set to 0	Set to 1	
Notify ARP Master	3	Device Address = '1100 0010'	Set to 0	Set to 0	Set IC_TAR[6:0] to SMB Host Address (0001 000)
		Data Byte Low = '0000 0000'	Set to 0	Set to 0	
		Data Byte High = '0000 0000'	Set to 0	Set to 1	



- DW_apb_i2c slave hardware:
 - Handles the generation, detection, and NACKing of the wrong PEC (CRC8 C(X)=X8+X2+X1+1) for the ARP Commands.
 - Does not handle the PEC for Non-ARP commands.
- DW_apb_i2c master hardware does not handle PEC for both APR and non-ARP commands.

3.14.6.1 Procedure to Perform ARP in Master Mode

To use the DW_apb_i2c as a SMBus Master/Host for assigning the unique address to each slave device to resolve the slave address conflicts, perform the following steps:

1. After a reset or a cold power up, the SMBus host or master issues a "Prepare to ARP" command to indicate that the master is carrying an ARP to assign dynamic addresses to all devices. Slave must flush any pending host notify commands.
2. An acknowledgement received for the "Prepare to ARP" command indicates that ARP-capable devices exist in the system and the "Get UDID" command must be issued. A NACK indicates that ARP-capable devices do not exist or currently all slaves have their addresses resolved. In this case, the master must complete steps outlined from Step 8 onwards. The DW_apb_i2c master indicates NACK reception through 'ABRT_7B_ADDR_NOACK' and 'ABRT_TXDATA_NOACK' bits of the IC_TX_ABRT_SOURCE register.
3. DW_apb_i2c Master issues 'Get UDID' to receive the UDID information of the slave for assigning the dynamic address.
4. If the first three bytes of the "Get UDID" command are ACK'ed and the receive byte count is 0x11, then the master issues the "Assign Address" command. Else, the master must complete steps outlined in step 8 onwards to indicate that the ARP is complete. DW_apb_i2c Master indicates NACK reception through ABRT_7B_ADDR_NOACK and ABRT_TXDATA_NOACK bits of the IC_TX_ABRT_SOURCE register.

5. The Master issues the "Assign Address" command to assign the Dynamic address to the slave whose UDID is received through "Get UDID command".
6. If the assigned address packet is ACK'ed, then Master removes the assigned address from the address pool and moves to Step 3 to get UDID of another slave. If the packet is not ACK'ed, then master will not remove the address from the address pool and moves to Step 3 to get UDID of same slave or another slave.
7. If the Assign Address is ACK'ed, then Master stores the assigned address in the used address pool with the UDID characteristics of the device.
8. The Master moves to Step 3 to issue a 'Get UDID' command again to receive the UDID of another slave. If it receives NACK for 'Get UDID', the Master moves to Step 9.
9. The DW_apb_i2c can be switched to Slave mode to detect device requests for Host Notify Protocol.
10. If the DW_apb_i2c switched to slave mode and DW_apb_i2c detects the Host Notify Protocol, then this indicates that a slave is requesting for the dynamic address and the Master has to undergo the ARP as outlined in Step 11.
11. If the DW_apb_i2c is in Master mode, then move to Step 3 for performing ARP procedure, otherwise move to Step 12.
12. The DW_apb_i2c is switched to Master Mode and moves to Step 3 to perform ARP procedure.

The detailed flow diagram is explained in [Figure 8-10](#) on page [260](#).

3.14.6.2 Procedure to Perform ARP in Slave Mode

The DW_apb_i2c as a SMBus Slave performs the following tasks:

- Decodes the ARP commands and responds based on internal state flags 'SMBUS_SLAVE_ADDR_VALID' and 'SMBUS_SLAVE_ADDR_RESOLVED' of the IC_STATUS register.
- Generates and Validates the PEC byte of ARP commands
- Generates ACK for the PEC byte only if it matches the CRC value calculated on data it received. If not, NACK the PEC byte.

When another SMBus Master/Host device on the bus generates the ARP commands and requests to participate in the ARP, the DW_apb_i2c acts as a SMBus slave and performs the following steps:

1. After a reset or a cold power up, the DW_apb_i2c slave device checks whether it supports a persistent slave address.
2. If DW_apb_i2c has a persistent slave address (PSA), which is indicated by the Address Valid flag being set, then PSA is set in the Slave Address Register (IC_SAR) register. If the flag is not set, then proceed to Step 4.
3. DW_apb_i2c persistent slave stores the persistent address in IC_SAR and sets Address Valid flag to 1 and Address Resolved Flag to 0.
4. DW_apb_i2c Non Persistent slave (non-PSA) clears both Address Valid and Address Resolved Flags.

5. DW_apb_i2c Checks whether any Packet received has ARP Default address in the slave address field of the packet to decide on ARP command or normal command. If there is a match then DW_apb_i2c slave proceeds to Step 6, otherwise to Step 25.
6. If DW_apb_i2c detects a packet addressed to the SMBus Device Default Address, it checks the command field to determine if this is the "Prepare to ARP" command. If so, then it proceeds to Step 7, otherwise it proceeds to Step 8.
7. Upon receipt of the "Prepare to ARP" command, the DW_apb_i2c acknowledges the packet and clears the Address Resolved flag in order to participate in the ARP Process. DW_apb_i2c proceeds to Step 5 and waits for another SMBus Packet.
8. The DW_apb_i2c checks the command field to verify if the "Reset Device" command was issued. If yes, the DW_apb_i2c proceeds to Step 9, otherwise it proceeds to Step 10.
9. Upon receipt of the "Reset Device" command, the DW_apb_i2c acknowledges the packet and clears the Address Resolved and Address Valid (If non-PSA and ic_con[19]=0) flags. DW_apb_i2c proceeds to Step 5 and waits for another SMBus Packet.
10. The device checks the command to verify if the "Assign Address" command was issued. If yes, then it proceeds to Step 11, otherwise proceeds to Step 13.
11. Upon receipt of the "Assign Address" command, the DW_apb_i2c compares its UDID with one its received bytes. If any byte does not match, then DW_apb_i2c will not acknowledge that byte and subsequent bytes also. If all bytes in the UDID matches, then the DEVICE proceeds to Step 12, otherwise it proceeds to Step 5 and waits for another SMBus packet.
12. After the UDID is matched in Step 11, the DW_apb_i2c will receive the slave address and sets the IC_SAR register with this slave address. The DW-apb_i2c sets its Address Valid and Address Resolved flags, which means it has received the dynamic address and will no longer respond to the "Get UDID" command unless it receives the "Prepare to ARP" or "Reset Device" commands. DW_apb_i2c now proceeds to Step 5 and waits for another SMBus packet.
13. The DW_apb_i2c checks the command field to verify if the "Get UDID" command was issued. If yes, then it proceeds to Step 14, otherwise to Step 19.
14. Upon receipt of the "Get UDID" command, the DW_apb_i2c checks its Address Resolved flag to determine whether it must participate in an ARP process. If set, then its address has already been resolved by the ARP Master, so the device proceeds to Step 5 and waits for another SMBus packet. If the ARP Flag is cleared, then it proceeds to Step 15.
15. The DW_apb_i2c returns its UDID and monitors the SMBus data line for collisions. If a collision is detected at any time, DW_apb_i2c generates the SLV_ARB_LOST bit and stops transmitting. Further, it proceeds to Step 5 and waits for another SMBus packet. If collisions are not detected, then DW_apb_i2c proceeds to Step 16.
16. The DW_apb_i2c check its Address Valid (AV) flag to determine the value to return for the Device Slave Address field. If the AV flag is set, then it proceeds to Step 17, otherwise it proceeds to Step 18.
17. When the AV flag is set, the current IC_SAR is valid, therefore the device returns this for the Device Slave Address field (with bit 0 set) and monitors the SMBus data line for collisions. DW_apb_i2c proceeds to Step 5 and waits for another SMBus Packet.
18. When the AV flag is not set, the current slave address (IC_SAR) is invalid. Therefore, the DW_apb_i2c returns a value of FFh and monitors the SMBus data line for collisions. The device

requires an address assignment if the ARP master receives the FFH value. DW_apb_i2c proceeds to Step 5 and waits for another SMBus packet.

19. The DW_apb_i2c may be receiving a directed command. If the Address Valid flag is set and address is the same as in IC_SAR, then proceed to Step 20 otherwise, proceed to Step 5 to wait for another SMBus packet.
20. If the Address Valid flag is set, check if the command is a directed "Reset Device" command. If yes, then proceed to Step 21, otherwise proceed to Step 22.
21. Upon receipt of the "Reset Device" command, the DW_apb_i2c acknowledges the packet and clears the Address Resolved and Address Valid (If non-PSA and ic_con[19]=0) flags. DW_apb_i2c proceeds to Step 5 and waits for another SMBus Packet.
22. DW_apb_i2c checks whether the received command is a "Directed Get UDID" command. If yes, then proceed to Step 23 and return the UDID information. If not, then proceed to Step 24.
23. If the received command is a "Directed Get UDID" command, then return the UDID information and current slave address, proceed to Step 5 and wait for another SMBus Packet.
24. If the received command is a "Directed Get UDID" command, the DW_apb_i2c has not received a valid ARP command and hence DW_apb_i2c NACKs the command and proceeds to Step 5 and wait for another SMBus Packet.
25. If the Address Valid bit is set then it proceeds to Step 26, otherwise it proceeds to Step 5 and waits for another SMBus Packet. The received address is not the SMBus Device Default Address and the packet may be addressed to the DW_apb_i2c's core function. The device checks its Address Valid bit to determine whether to respond.
26. When the address valid bit is set, DW_apb_i2c has a valid slave address. It compares the received slave address to its slave address, and if there is a match, DW_apb_i2c proceeds to Step 27, otherwise it proceeds to Step 5 and waits for another SMBus Packet.
27. The Dw_apb_i2c receives a packet addresses to its core function and hence it acknowledges the packet and processes it accordingly. DW_apb_i2c proceeds to step 5 and waits for another SMBus Packet.

The detailed flow diagram is explained in [Figure 8-11](#) on page [261](#).

3.14.7 SMBUS Additional Slave Address

DW_apb_i2c supports second optional slave address decode capability. It can be configured to contain an extra slave address register IC_OPTIONAL_SAR. If configured with this additional register, user can write any valid slave address to this register which will be matched against an incoming slave address on SMBus. A match of incoming address with either IC_SAR register or IC_OPTIONAL_SAR register will cause DW_apb_i2c to acknowledge the transaction and respond to it accordingly. Use of this additional slave address register is controlled by OPTIONAL_SAR_CTRL (IC_CON[17]) bit. If OPTIONAL_SAR_CTRL bit is programmed to be 1, then IC_OPTIONAL_SAR register will be used to match the incoming address. All restrictions of IC_SAR register applies to IC_OPTIONAL_SAR register as well.

The default value that IC_OPTIONAL_SAR register obtains after reset can be configured by the IC_OPTIONAL_SAR_DEFAULT parameter.

3.14.8 SMBUS Optional Signals

The SMBus standard supports these optional signals:

- SMBus Suspend Signal
- SMBus Alert Signal

As these signals are optional, DW_apb_i2c can be configured to include these signals through IC_SMBUS_SUSPEND_ALERT parameter.

3.14.8.1 SMBus Suspend Signal

The SMBus suspend signal (SMBSUS#) is an optional signal which is asserted by the system controller (mostly the Host) to indicate that the system should enter in low power suspend mode. It is output from the system controller and input to all other devices. This signal is an active low signal. DW_apb_i2c implements this functionality using following signals:

- ic_smbsus_in_n
- ic_smbsus_out_n

Output signal ic_smbsus_out_n is controlled directly by the SMBUS_SUS_CTRL bit (IC_ENABLE[17]). If this bit is programmed to 1, ic_smbsus_out_n signal goes to 0 as soon as master finishes any ongoing transfer. For coming out of the suspend mode, user needs to clear this bit, which deasserts the ic_smbus_out_n signal.

Input signal ic_smbsus_in_n generates interrupt ic_smbsus_det_intr (or ic_smbsus_det_intr_n) on the falling edge. This interrupt can be used by the software to enter the Low Power Mode. Current status of this ic_smbsus_in_n can be read from SMBUS_SUSPEND_STATUS bit of IC_STATUS (19) register.

3.14.8.2 SMBus Alert Signal

The SMBus alter signal (SMBALERT#) is other optional signal specified by the SMBus standard. It can be used by simple devices to request the attention of the host. Devices can use the SMBALERT# signal to request the attention of the host with master functionality. This active low signal is input to host device and output from all other devices. Since multiple devices may implement SMBALERT#, it is required to be a wired-AND signal. Upon detecting a SMBALERT# signal, a host must send an alert response address which is acknowledge by alerting the device and it sends the address to the host and deasserts the alert signal. If host still detects an asserted alert signal, it repeats sending alert response address. DW_apb_i2c implements this functionality using following signals:

- ic_smbalert_in_n
- ic_smbalert_oe

Output signal ic_smbalert_oe is open drain/open collector pull down driver and should be used similar to ic_clk_oe and ic_data_oe on a system implementation. Assertion of ic_smbalert_oe is controlled by SMBUS_ALERT_CTRL bit (IC_ENABLE[18]). Once asserted by user, DW_apb_i2c waits for alert response address to be sent by master. Upon receiving it, contents of IC_SAR[7:0] register are sent to the master. When successful, DW_apb_i2c clears the SMBUS_ALERT_CTRL bit and deasserts the ic_smbalert_oe signal.

Input signal ic_smbalert_in_n generates interrupt ic_smbalert_det_intr (or ic_smbalert_det_intr_n) on falling edge. If working as host, user needs to service this interrupt by sending read byte command with Alert Response Address. Current status of ic_smbalert_in_n can be read from SMBUS_ALERT_STATUS bit (IC_STATUS[20])

3.15 IC_CLK Frequency Configuration

When the DW_apb_i2c is configured as a Standard (SS), Fast (FS)/Fast-Mode Plus (FM+), or High Speed (HS) master, the *CNT registers must be set before any I²C bus transaction can take place in order to ensure proper I/O timing. The *CNT registers are:

- [IC_SS_SCL_HCNT](#)
- [IC_SS_SCL_LCNT](#)
- [IC_FS_SCL_HCNT](#)
- [IC_FS_SCL_LCNT](#)
- [IC_HS_SCL_HCNT](#)
- [IC_HS_SCL_LCNT](#)

When the DW_apb_i2c is configured as a Ultra-Fast Mode master, the *CNT registers must be set before any I²C bus transaction can take place in order to ensure proper I/O timing. The *CNT registers for this mode are:

- [IC_UFM_SCL_HCNT](#)
- [IC_UFM_SCL_LCNT](#)



Note The tBUF timing and setup/hold time of START, STOP and RESTART registers uses *HCNT/*LCNT register settings for the corresponding speed mode.



Note It is not necessary to program any of the *CNT registers if the DW_apb_i2c is enabled to operate only as an I²C slave, since these registers are used only to determine the SCL timing requirements for operation as an I²C master.

Table 3-4 lists the derivation of I²C timing parameters from the *CNT programming registers.

Table 3-4 Derivation of I²C Timing Parameters from *CNT Registers

Timing Parameter	Symbol	Standard Speed	Fast Speed / Fast Speed Plus	High Speed (100 pf)	High Speed (400 pf)
LOW period of the SCL clock	tLOW	IC_SS_SCL_LCNT	IC_FS_SCL_LCNT	IC_HS_SCL_LCNT	IC_HS_SCL_LCNT
HIGH period of the SCL clock	tHIGH	IC_SS_SCL_HCNT	IC_FS_SCL_HCNT	IC_HS_SCL_HCNT	IC_HS_SCL_HCNT

Table 3-4 Derivation of I²C Timing Parameters from *CNT Registers

Timing Parameter	Symbol	Standard Speed	Fast Speed / Fast Speed Plus	High Speed (100 pf)	High Speed (400 pf)
Setup time for a repeated START condition	tSU;STA	IC_SS_SCL_LCNT	IC_FS_SCL_HCNT	IC_HS_SCL_LCNT	(IC_HS_SCL_LCNT)/2
Hold time (repeated) START condition*	tHD;STA	IC_SS_SCL_HCNT	IC_FS_SCL_HCNT	IC_HS_SCL_LCNT	(IC_HS_SCL_LCNT)/2
Setup time for STOP condition	tSU;STO	IC_SS_SCL_HCNT	IC_FS_SCL_HCNT	IC_HS_SCL_LCNT	(IC_HS_SCL_LCNT)/2
Bus free time between a STOP and a START condition	tBUF	IC_SS_SCL_LCNT	IC_FS_SCL_LCNT	NA	NA
Spike length	tSP	IC_FS_SPKLEN	IC_FS_SPKLEN	IC_HS_SPKLEN	IC_HS_SPKLEN
Data hold time	tHD;DAT	IC_SDA_HOLD	IC_SDA_HOLD	IC_SDA_HOLD	IC_SDA_HOLD
Data setup time	tSU;DAT	IC_SDA_SETUP	IC_SDA_SETUP	IC_SDA_SETUP	IC_SDA_SETUP

3.15.1 Minimum High and Low Counts in SS, FS, FM+ and HS Modes With IC_CLK_FREQ_OPTIMIZATION = 0.

When the DW_apb_i2c operates as an I2C master, in both transmit and receive transfers:

- IC_SS_SCL_LCNT and IC_FS_SCL_LCNT register values must be larger than IC_FS_SPKLEN + 7.
- IC_SS_SCL_HCNT and IC_FS_SCL_HCNT register values must be larger than IC_FS_SPKLEN + 5.
- If the component is programmed to support HS, IC_HS_SCL_LCNT register value must be larger than IC_HS_SPKLEN + 7.
- If the component is programmed to support HS, IC_HS_SCL_HCNT register value must be larger than IC_HS_SPKLEN + 5.

Details regarding the DW_apb_i2c high and low counts are as follows:

- The minimum value of IC_*_SPKLEN + 7 for the *_LCNT registers is due to the time required for the DW_apb_i2c to drive SDA after a negative edge of SCL.
- The minimum value of IC_*_SPKLEN + 5 for the *_HCNT registers is due to the time required for the DW_apb_i2c to sample SDA during the high period of SCL.
- The DW_apb_i2c adds one cycle to the programmed *_LCNT value in order to generate the low period of the SCL clock; this is due to the counting logic for SCL low counting to (*_LCNT + 1).

- The DW_apb_i2c adds $IC_SPKLEN + 7$ cycles to the programmed $*_HCNT$ value in order to generate the high period of the SCL clock; this is due to the following factors:
 - The counting logic for SCL high counts to $(*_HCNT+1)$.
 - The digital filtering applied to the SCL line incurs a delay of $SPKLEN + 2$ ic_clk cycles, where SPKLEN is:
 - IC_FS_SPKLEN if the component is operating in SS or FS
 - IC_HS_SPKLEN if the component is operating in HS.
- This filtering includes metastability removal and the programmable spike suppression on SDA and SCL edges.
- Whenever SCL is driven 1 to 0 by the DW_apb_i2c—that is, completing the SCL high time—an internal logic latency of three ic_clk cycles is incurred. Consequently, the minimum SCL low time of which the DW_apb_i2c is capable is nine (9) ic_clk periods ($7 + 1 + 1$), while the minimum SCL high time is thirteen (13) ic_clk periods ($6 + 1 + 3 + 3$).

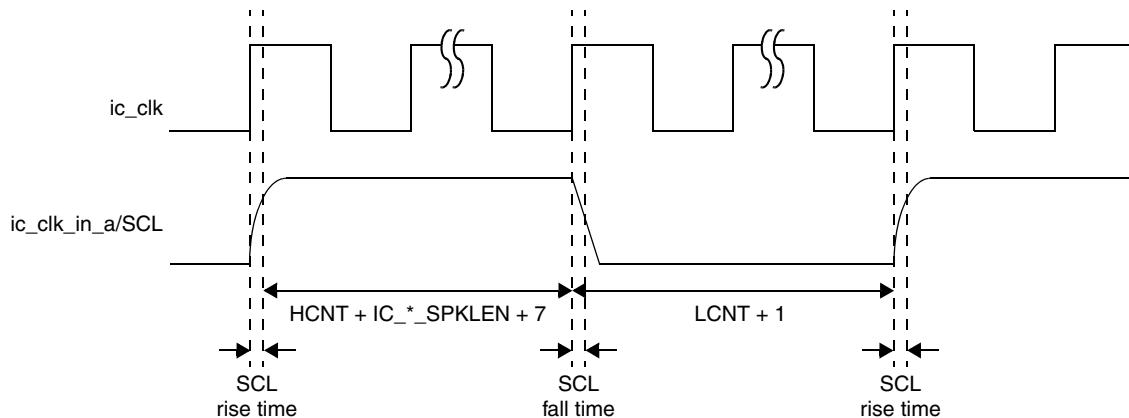


Note The total high time and low time of SCL generated by the DW_apb_i2c master is also influenced by the rise time and fall time of the SCL line, as shown in the illustration and equations in [Figure 3-30 on page 81](#). It should be noted that the SCL rise and fall time parameters vary, depending on external factors such as:

- Characteristics of IO driver
- Pull-up resistor value
- Total capacitance on SCL line, and so on

These characteristics are beyond the control of the DW_apb_i2c.

Figure 3-30 Impact of SCL Rise Time and Fall Time on Generated SCL



$$\begin{aligned} SCL_High_time &= [(HCNT + IC_SPKLEN + 7) * ic_clk] + SCL_Fall_time \\ SCL_Low_time &= [(LCNT + 1) * ic_clk] - SCL_Fall_time + SCL_Rise_time \end{aligned}$$

3.15.2 Minimum High and Low Counts in SS, FS, FM+ and HS Modes With IC_CLK_FREQ_OPTIMIZATION = 1

The minimum high and low counts in SS, FS, FM+ and HS Modes with the IC_CLK_FREQ_OPTIMIZATION parameter set to one is such that:

- The total SCL LOW period is driven by DW_apb_i2c will be IC_*_LCNT register value. The hardware does not support a value less than 6 to be written to the IC_*_LCNT register. Additionally, the minimum SCL low time of which the DW_apb_i2c is capable is 6 ic_clk periods.
- The total SCL HIGH period driven by DW_apb_i2c will be IC_*_HCNT register value + SPKLEN + 3. Additionally, the minimum SCL high time of which the DW_apb_i2c is capable is 5 ic_clk periods [1+1+3].

The total high time and low time of SCL generated by the DW_apb_i2c master is also influenced by the rise time and fall time of the SCL line. The SCL rise and fall time parameters vary depending on external factors such as:

- Characteristics of IO driver
- Pull-up resistor value
- Total capacitance on SCL line, and so on

These characteristics are beyond the control of the DW_apb_i2c.

3.15.3 Minimum High and Low counts in Ultra-Fast mode (IC_ULTRA_FAST_MODE = 1)

When the DW_apb_i2c operates as an I2C master:

- The IC_UFM_SCL_HCNT register value must be equal or larger than 3.
- The IC_UFM_SCL_LCNT register Value must be equal or larger than 5.

3.15.4 Minimum IC_CLK Frequency

This section describes the minimum ic_clk frequencies that the DW_apb_i2c supports for each speed mode, and the associated high and low count values. In Slave mode, IC_SDA_HOLD (Thd;dat) and IC_SDA_SETUP (Tsu:dat) need to be programmed to satisfy the I2C protocol timing requirements.

The following examples are for the case where IC_FS_SPKLEN and IC_HS_SPKLEN are programmed to 2.

3.15.4.1 Standard Mode (SM), Fast Mode (FM), and Fast Mode Plus (FM+) with IC_CLK_FREQ_OPTIMIZATION = 0

This section details how to derive a minimum ic_clk value for standard and fast modes of the DW_apb_i2c. Although the following method shows how to do fast mode calculations, you can also use the same method in order to do calculations for standard mode and fast mode plus.



The following computations do not consider the SCL_Rise_time and SCL_Fall_time.

Given conditions and calculations for the minimum DW_apb_i2c ic_clk value in fast mode:

- Fast mode has data rate of 400kb/s; implies SCL period of $1/400\text{kHz} = 2.5\mu\text{s}$
- Minimum hcnt value of 14 as a seed value; IC_HCNT_FS = 14
- Protocol minimum SCL high and low times:
 - MIN_SCL_LOWtime_FS = 1300ns
 - MIN_SCL_HIGHTime_FS = 600ns

Derived equations:

$$\frac{\text{SCL_PERIOD_FS}}{\text{IC_HCNT_FS} + \text{IC_LCNT_FS}} = \text{IC_CLK_PERIOD}$$

$$\text{IC_LCNT_FS} \times \text{IC_CLK_PERIOD} = \text{MIN_SCL_LOWtime_FS}$$

Combined, the previous equations produce the following:

$$\text{IC_LCNT_FS} \times \frac{\text{SCL_PERIOD_FS}}{\text{IC_LCNT_FS} + \text{IC_HCNT_FS}} = \text{MIN_SCL_LOWtime_FS}$$

Solving for IC_LCNT_FS:

$$\text{IC_LCNT_FS} \times \frac{2.5\mu\text{s}}{\text{IC_LCNT_FS} + 14} = 1.3\mu\text{s}$$

The previous equation gives:

$$\text{IC_LCNT_FS} = \text{roundup}(15.166) = 16$$

These calculations produce IC_LCNT_FS = 16 and IC_HCNT_FS = 14, giving an ic_clk value of:

$$\frac{2.5\mu\text{s}}{16 + 14} = 83.3\text{ns} = 12\text{Mhz}$$

Testing these results shows that protocol requirements are satisfied.

3.15.4.2 High-Speed (HS) Mode With IC_CLK_FREQ_OPTIMIZATION = 0

The method used for standard and fast modes can also be used to derive ic_clk values for high-speed modes. For example, given a high-speed mode with a 100pf bus loading, using the standard and fast modes method produces the following:

- IC_LCNT_HS = 17
- IC_HCNT_HS = 14
- ic_clk = 105.4 Mhz

Table 3-5 lists the minimum ic_clk values for all modes with high and low count values.

Table 3-5 ic_clk in Relation to High and Low Counts When IC_CLK_FREQ_OPTIMIZATION = 0

Speed Mode	ic_clk _{freq} (MHz)	Minimum Value of IC_*_SPK LEN	SCL Low Time in ic_clks	SCL Low Program Value	SCL Low Time	SCL High Time in ic_clks	SCL High Program Value	SCL High Time
SS	2.7	1	13	12	4.7 μ s	14	6	5.2 μ s
FS	12.0	1	16	15	1.33 μ s	14	6	1.16 μ s
FM+	32	2	16	15	500 ns	16	7	500 ns
HS (400pf)	51	1	17	16	333 ns	14	6	274 ns
HS (100pf)	105.4	1	17	16	161 ns	14	6	132 ns



- The IC_*_SCL_LCNT and IC_*_SCL_HCNT registers are programmed using the SCL low and high program values in [Table 3-5](#), which are calculated using SCL low count minus 1, and SCL high counts minus 8, respectively.
- The values in [Table 3-5](#) are based on IC_SDA_RX_HOLD = 0. The maximum IC_SDA_RX_HOLD value depends on the IC_*_CNT registers in Master mode, as described in "[SDA Hold Timings in Receiver](#)" on page 91.
- In order to compute the HCNT and LCNT considering RC timings, use the following equations:

$$\text{IC_HCNT_*} = [(\text{HCNT} + \text{IC_*_SPKLEN} + 7) * \text{ic_clk}] + \text{SCL_Fall_time}$$

$$\text{IC_LCNT_*} = [(\text{LCNT} + 1) * \text{ic_clk}] - \text{SCL_Fall_time} + \text{SCL_Rise_time}$$

3.15.4.3 SM, FM, FM+ and HS Modes With IC_CLK_FREQ_OPTIMIZATION = 1

3.15.4.3.1 Master Mode

This section describes the minimum ic_clk frequencies that the DW_apb_i2c supports for each speed mode and the associated high and low count values. The following examples are for the case where IC_FS_SPKLEN = 1, IC_HS_SPKLEN = 1 and IC_CLK_FREQ_OPTIMIZATION = 1.

Below calculations show how to derive a minimum ic_clk value for fast mode of the DW_apb_i2c. Although the following method shows how to do fast mode calculations, you can also use the same method in order to do calculations for any speed mode.



The computation in this section does not consider SCL_Rise_time and SCL_Fall_time.

Following are the conditions and calculations for the minimum DW_apb_i2c ic_clk value in fast mode:

- Fast mode has data rate of 400kb/s; implies SCL period of 1/400KHz = 2.5 us

- Minimum hcnt value of 5 as a seed value; IC_HCNT_FS = 5
- Protocol minimum SCL high and low times:
 - MIN_SCL_LOWtime_FS = 1300 ns
 - MIN_SCL_HIGHtime_FS = 600 ns

Following are the derived equations:

$$\text{SCL_PERIOD_FS} / (\text{IC_HCNT_FS} + \text{IC_LCNT_FS}) = \text{IC_CLK_PERIOD}$$

$$\text{IC_LCNT_FS} \times \text{IC_CLK_PERIOD} = \text{MIN_SCL_LOWtime_FS}$$

Following is the result of combining previous equations:

$$\text{IC_LCNT_FS} \times \text{SCL_PERIOD_FS} / (\text{IC_LCNT_FS} + \text{IC_HCNT_FS}) = \text{MIN_SCL_LOWtime_FS}$$

By solving for IC_LCNT_FS:

$$\text{IC_LCNT_FS} \times 2.5 \mu\text{s} / (\text{IC_LCNT_FS} + 5) = 1.3 \mu\text{s}$$

The previous equation provides:

$$\text{IC_LCNT_FS} = \text{roundup}(5.417) = 6$$



Note Minimum IC_*_LCNT value should be equal 6. If derived value is less than 6, consider IC_LCNT_FS as 6 only.

These calculations produce IC_LCNT_FS = 6 and IC_HCNT_FS = 5, providing an ic_clk value of:

$$2.5 \mu\text{s} / (6 + 5) = 227.27\text{ns} = 4.4 \text{ MHz}$$

Testing these results shows that the protocol requirements are satisfied.

[Table 3-6](#) lists the minimum ic_clk values for all modes with high and low count values.

Table 3-6 ic_clk in Relation to High and Low Counts When IC_CLK_FREQ_OPTIMIZATION = 1

Speed Mode	ic_clk Frequency (MHz)	Minimum Value of IC_*_SPKLEN	SCL Low Time in ic_clks	SCL Low Program Value	SCL Low Time in ns	SCL High Time in ic_clks	SCL High Program Value	SCL High Time in ns
SS	1.1	1	6	6	5454.545	5	1	4545.455
FS	4.4	1	6	6	1363.636	5	1	1136.364
FM+	11	1	6	6	545.4545	5	1	454.5455
HS (400pf)	18.7	1	6	6	320.8527	5	1	267.3773
HS (100pf)	37.4	1	6	6	160.4236	5	1	133.6864



- The IC_*_SCL_LCNT and IC_*_SCL_HCNT registers are programmed using the SCL low and high program values in [Table 3-6](#), which are calculated as SCL low count, and SCL high count minus 4, respectively. The values in [Table 3-6](#) are based on IC_SDA_RX_HOLD = 0. The maximum IC_SDA_RX_HOLD value depends on the IC_*CNT registers in master mode, as described in “[SDA Hold Timings in Receiver](#)” on page [91](#).
- To compute the HCNT and LCNT considering RC timings, use the following equations:

$$\text{IC_HCNT_*} = [(\text{HCNT} + \text{IC_*_SPKLEN} + 3) * \text{ic_clk}] + \text{SCL_Fall_time}$$

$$\text{IC_LCNT_*} = [\text{LCNT} * \text{ic_clk}] - \text{SCL_Fall_time} + \text{SCL_Rise_time}$$

3.15.4.3.2 Slave Mode

DW_apb_i2c in slave mode requires minimum 5 ic_clk cycles [SPKLEN + 3 (Metastability removal, worst case) + 1] to drive SDA after a falling edge of SCL. Therefore, the ic_clk frequency must be selected such that the maximum data hold time (thd;dat)/data valid time (tVD;DAT) is not violated.

For example, in high-speed mode with a 100pf bus loading (SCLH clock frequency upto 3.4 MHz), the maximum data hold time is 70 ns. Therefore, the minimum frequency in which DW_apb_i2c can operate in slave mode without violating thd;dat is $70\text{ns}/5 = 14\text{ns} = 71.42\text{ MHz}$.

[Table 3-7](#) lists the minimum IC_CLK frequency in slave mode when IC_CLK_FREQ_OPTIMIZATION is set to 1.

Table 3-7 Minimum IC_CLK Frequency in Slave Mode When IC_CLK_FREQ_OPTIMIZATION=1

Speed Mode	ic_clk Frequency (MHz)	Minimum Value of IC_*_SPKLEN	Minimum data hold time in ic_clks	Maximum data hold time
SS	1.45	1	5	3.45 μs
FS	5.56	1	5	0.9 μs
FM+	11.11	1	5	0.45 μs
HS (400pf)	35.71	1	5	140 ns
HS (100pf)	71.42	1	5	70 ns

3.15.4.4 ULTRA-FAST Mode

3.15.4.4.1 Master mode

This section describes the minimum ic_clk frequency that the DW_apb_i2c supports for Ultra-Fast speed mode and the associated high and low count values.

The following calculations show how to derive a minimum ic_clk value.



Note The following computations do not consider the SCL_Rise_time and SCL_Fall_time.

Given conditions and calculations for the minimum DW_apb_i2c ic_clk value in Ultra-Fast mode:

- Fast mode has data rate of 5000kb/s; implies SCL period of $1/5000\text{kHz} = 200\text{ns}$
- Minimum hcnt value of 3 as a seed value; IC_UFM_SCL_HCNT = 3
- Protocol minimum SCL high and low times:
 - MIN_SCL_LOWtime_UFm = 50 ns
 - MIN_SCL_HIGHtime_UFm = 50ns

Derived equations:

- $\text{SCL_PERIOD_UFm}/(\text{IC_HCNT_UFm} + \text{IC_LCNT_UFm}) = \text{IC_CLK_PERIOD}$
- $\text{IC_LCNT_UFm} \times \text{IC_CLK_PERIOD} = \text{MIN_SCL_LOWtime_UFm}$

Combined, the previous equations produce the following:

$$\text{IC_LCNT_UFm} \times \text{SCL_PERIOD_UFm} / (\text{IC_LCNT_UFm} + \text{IC_HCNT_UFm}) = \text{MIN_SCL_LOWtime_UFm}$$

Solving for IC_LCNT_UFm:

$$\text{IC_LCNT_UFm} \times 200\text{ns} / (\text{IC_LCNT_UFm} + 3) = 50\text{ns}$$

The previous equation gives:

$$\text{IC_LCNT_UFm} = 1$$



Note Minimum IC_SCL_UFM_LCNT value should be equal 5. If derived value is less than 5, consider IC_LCNT_UFm as 5 only.

These calculations produce IC_LCNT_UFm = 5 and IC_HCNT_UFm = 3, giving an ic_clk value of:

$$200\text{ ns} / (5 + 3) = 25\text{ns} = 40\text{Mhz}$$

Testing these results shows that protocol requirements are satisfied.

[Table 3-8](#) describes the relation between the High and Low counts with ic_clk frequency

Table 3-8 ic_clk in relation to High and Low Counts when IC_ULTRA_FAST_MODE=1

Speed	ic_clk (freq) (Mhz)	SCL Low Program Value	SCL Low Time in ic_clks	SCL Low Time	SCL High Program Value	SCL HighTime in ic_clks	SCL HighTime
UltraFast Mode	40	5	5	125 ns	3	3	75 ns



- The IC_UFM_SCL_LCNT and IC_UFM_SCL_HCNT registers are programmed using the SCL low and high program values in [Table 3-8](#), which are calculated as SCL low count, and SCL high count, respectively. The values in [Table 3-8](#) are based on IC_SDA_RX_HOLD = 0. The maximum IC_SDA_RX_HOLD value depends on the IC_UFM_SCL_LCNT registers in Master mode, as described in “[SDA Hold Timings in Receiver](#)” on page [91](#).
- In order to compute the HCNT and LCNT considering RC timings, use the following equations:

$$\text{IC_UFM_SCL_HCNT} = [\text{HCNT} * \text{ic_clk}] + \text{SCL_Fall_time}$$

$$\text{IC_UFM_SCL_LCNT} = [\text{LCNT} * \text{ic_clk}] - \text{SCL_Fall_time} + \text{SCL_Rise_time}$$

3.15.4.4.2 Slave mode

DW_apb_i2c in slave mode requires minimum of 2 ic_clk cycles for SCL High period and SCL Low Period. Therefore, the minimum ic_clk frequency for the slave mode is 40 MHz.

3.15.4.5 Calculating High and Low Counts with IC_CLK_FREQ_OPTIMIZATION = 0

The calculations below show how to calculate SCL high and low counts for each speed mode in the DW_apb_i2c. For the calculations to work, the ic_clk frequencies used must not be less than the minimum ic_clk frequencies specified in [Table 3-5](#).

The DW_apb_i2c coreConsultant GUI can automatically calculate SCL high and low count values. By specifying an integer ic_clk period value in nanoseconds for the IC_CLK_PERIOD parameter, SCL high and low count values are automatically calculated for each speed mode. The ic_clk period must not specify a clock of a lower frequency than required for all supported speed modes. It is possible that the automatically calculated values may result in a baud rate higher than the maximum rate specified by the protocol. If this happens, either the low or high count values can be scaled up to reduce the baud rate.

The equation to calculate the proper number of ic_clk signals required for setting the proper SCL clocks high and low times is as follows:

$$\text{IC_xCNT} = (\text{ROUNDUP}(\text{MIN_SCL_xxxtime} * \text{OSCFREQ}, 0))$$

ROUNDUP is an explicit Excel function call that is used to convert a real number to its equivalent integer number.

$$\begin{aligned}\text{MIN_SCL_HIGHtime} &= \text{Minimum High Period} \\ \text{MIN_SCL_HIGHtime} &= 4000 \text{ ns for } 100 \text{ kbps} \\ &\quad 600 \text{ ns for } 400 \text{ kbps} \\ &\quad 260 \text{ ns for } 1000 \text{ kbps}\end{aligned}$$

60 ns for 3.4 Mbs, bus loading = 100pF
 120 ns for 3.4 Mbs, bus loading = 400pF

MIN_SCL_LOWtime = Minimum Low Period
 MIN_SCL_LOWtime = 4700 ns for 100 kbps
 1300 ns for 400 kbps
 500 ns for 1000 kbps
 160 ns for 3.4Mbs, bus loading = 100pF
 320 ns for 3.4Mbs, bus loading = 400pF

OSCFREQ = ic_clk Clock Frequency (Hz).

For example:

OSCFREQ = 100 MHz
 I2Cmode = fast, 400 kbit/s
 MIN_SCL_HIGHtime = 600 ns.
 MIN_SCL_LOWtime = 1300 ns.

```
IC_xCNT = (ROUNDUP(MIN_SCL_HIGH_LOWtime*OSCFREQ,0))  
  

IC_HCNT = (ROUNDUP(600 ns * 100 MHz,0))  

IC_HCNTSCL PERIOD = 60  

IC_LCNT = (ROUNDUP(1300 ns * 100 MHz,0))  

IC_LCNTSCL PERIOD = 130  

Actual MIN_SCL_HIGHtime = 60*(1/100 MHz) = 600 ns  

Actual MIN_SCL_LOWtime = 130*(1/100 MHz) = 1300 ns
```



Once the default values for SCL HighCount and LowCount are computed by the coreConsultant GUI, check that the values are consistent with the required baud rate. In case the computed values do not match with the required values, you can manually scale the values, as described in the section “[High-Speed \(HS\) Mode With IC_CLK_FREQ_OPTIMIZATION = 0](#)” on page 83.

3.15.4.6 Calculating High and Low counts with IC_CLK_FREQ_OPTIMIZATION = 1

The calculations below show how to calculate SCL high and low counts for each speed mode in the DW_apb_i2c. For the calculations to work, the ic_clk frequencies used must not be less than the minimum ic_clk frequencies specified in [Table 3-6](#).

The DW_apb_i2c coreConsultant GUI can automatically calculate SCL high and low count values. By specifying an integer ic_clk period value in nanoseconds for the IC_CLK_PERIOD parameter, SCL high and low count values are automatically calculated for each speed mode. The ic_clk period must not specify a clock of a lower frequency than required for all supported speed modes. It is possible that the automatically calculated values may result in a baud rate higher than the maximum rate specified by the protocol. If this happens, either the low or high count values can be scaled up to reduce the baud rate. For more information, see “[Master Mode](#)” on page 84.

The equation to calculate the proper number of ic_clk signals required for setting the proper SCL clocks high and low times is as follows:

```
IC_xCNT = (ROUNDUP(MIN_SCL_xxxtime*OSCFREQ,0))  

ROUNDUP is an explicit Excel function call that is used to convert a real number to its equivalent integer number.  

MIN_SCL_HIGHtime = Minimum High Period
```

```

MIN_SCL_HIGHTime = 4000 ns for 100 kbps
                  600 ns for 400 kbps
                  260 ns for 1000 kbps
                  60 ns for 3.4 Mbps, bus loading = 100pF
                  160 ns for 3.4 Mbps, bus loading = 400pF
MIN_SCL_LOWtime = Minimum Low Period
MIN_SCL_LOWtime = 4700 ns for 100 kbps
                  1300 ns for 400 kbps
                  500 ns for 1000 kbps
                  120 ns for 3.4Mbps, bus loading = 100pF
                  320 ns for 3.4Mbps, bus loading = 400pF
OSCFREQ = ic_clk Clock Frequency (Hz).

```

For example:

```

OSCFREQ = 100 MHz
I2Cmode = fast, 400 kbit/s
MIN_SCL_HIGHTime = 600 ns.
MIN_SCL_LOWtime = 1300 ns.

IC_xCNT = (ROUNDUP(MIN_SCL_HIGH_LOWtime*OSCFREQ,0))

IC_HCNT = (ROUNDUP(600 ns * 100 MHz,0))
IC_HCNTSCL PERIOD = 60
IC_LCNT = (ROUNDUP(1300 ns * 100 MHz,0))
IC_LCNTSCL PERIOD = 130
Actual MIN_SCL_HIGHTime = 60*(1/100 MHz) = 600 ns
Actual MIN_SCL_LOWtime = 130*(1/100 MHz) = 1300 ns

```



Note When the default values for SCL HighCount and LowCount are computed by the coreConsultant GUI, check that the values are consistent with the required baud rate. In case the computed values do not match with the required values, you can manually scale the values, as described in “Master mode” on page 86.

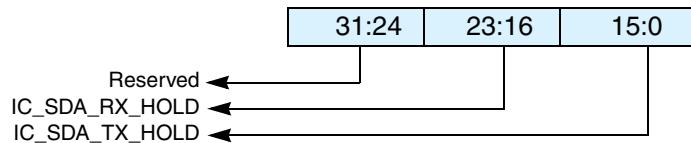
3.16 SDA Hold Time

The I²C protocol specification requires 300ns of hold time on the SDA signal (tHD;DAT) in standard mode and fast mode, and a hold time long enough to bridge the undefined part between logic 1 and logic 0 of the falling edge of SCL in high speed mode and fast mode plus.

Board delays on the SCL and SDA signals can mean that the hold-time requirement is met at the I²C master, but not at the I²C slave (or vice-versa). As each application encounters differing board delays, the DW_apb_i2c contains a software programmable register (IC_SDA_HOLD) to enable dynamic adjustment of the SDA hold-time.

The bits [15:0] are used to control the hold time of SDA during transmit in both slave and master mode (after SCL goes from HIGH to LOW).

The bits [23:16] are used to extend the SDA transition (if any) whenever SCL is HIGH in the receiver (in either master or slave mode).

Figure 3-31 IC_SDA_HOLD Register

If different SDA hold times are required for different speed modes, the IC_SDA_HOLD register must be reprogrammed when the speed mode is being changed. The IC_SDA_HOLD register can be programmed only when the DW_apb_i2c is disabled ($\text{IC_ENABLE}[0] = 0$).

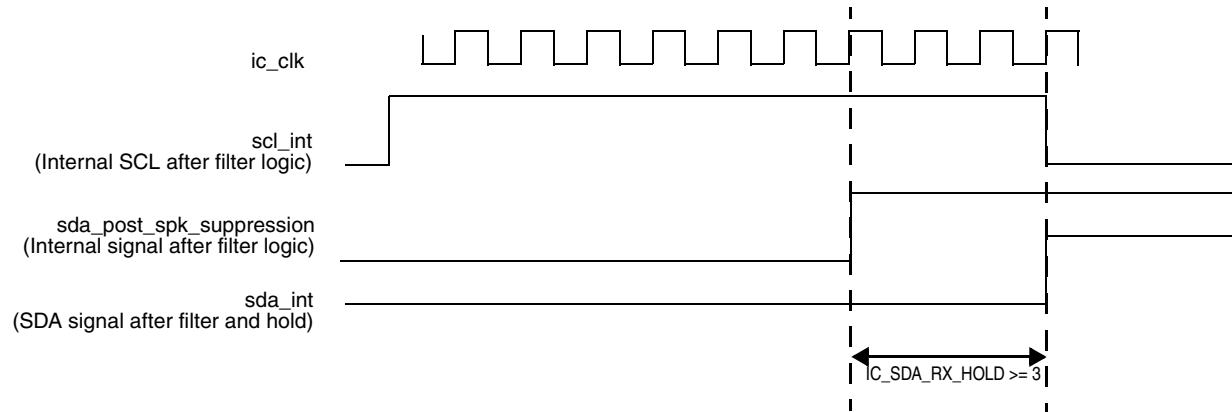
The reset value of the IC_SDA_HOLD register can be set via the coreConsultant parameter `IC_DEFAULT_SDA_HOLD`

3.16.1 SDA Hold Timings in Receiver

When DW_apb_i2c acts as a receiver, according to the I²C protocol, the device should internally hold the SDA line to bridge undefined gap between logic 1 and logic 0 of SCL.

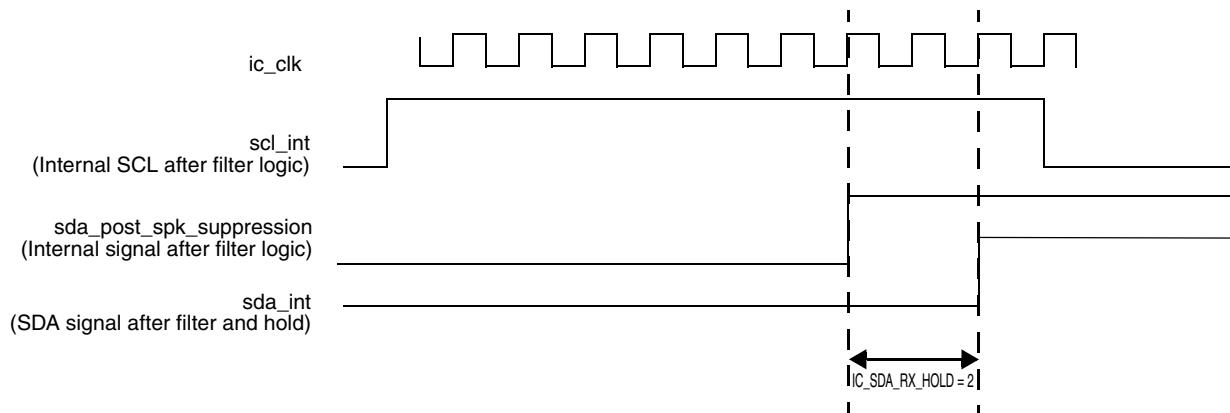
`IC_SDA_RX_HOLD` can be used to alter the internal hold time which DW_apb_i2c applies to the incoming SDA line. Each value in the `IC_SDA_RX_HOLD` register represents a unit of one `ic_clk` period. The minimum value of `IC_SDA_RX_HOLD` is 0. This hold time is applicable only when SCL is HIGH. The receiver does not extend the SDA after SCL goes LOW internally.

[Figure 3-32](#) shows the DW_apb_i2c as receiver with `IC_SDA_RX_HOLD` programmed to greater than or equal to 3.

Figure 3-32

If `IC_SDA_RX_HOLD` is greater than 3, DW_apb_i2c does not hold SDA beyond 3 `ic_clk` cycles, because SCL goes LOW internally.

[Figure 3-33](#) shows the DW_apb_i2c as receiver with `IC_SDA_RX_HOLD` programmed to 2.

Figure 3-33

The maximum values of IC_SDA_RX_HOLD that can be programmed in the register for the respective speed modes are derived from the equations show in [Table 3-9](#).

Table 3-9 Maximum Values for IC_SDA_RX_HOLD

Speed Mode	Maximum IC_SDA_RX_HOLD Value
Standard Mode	IC_SS_SCL_HCNT – IC_FS_SPKLEN – 3
Fast Mode or Fast Mode Plus	IC_FS_SCL_HCNT – IC_FS_SPKLEN – 3
High Speed (IC_CAP_LOADING =100)	Min {IC_FS_SCL_HCNT – IC_FS_SPKLEN – 3 , IC_HS_SCL_LCNT – IC_HS_SPKLEN – 3}
High Speed (IC_CAP_LOADING =400)	Min {IC_FS_SCL_HCNT – IC_FS_SPKLEN – 3 , (IC_HS_SCL_LCNT/2) – IC_HS_SPKLEN – 3}



The maximum values in [Table 3-9](#) is applicable in Master mode. In Slave mode, make sure the IC_SDA_RX_HOLD does not exceed the maximum SCL fall time (tf in SS and FS mode or tfcl in HS Mode).

3.16.2 SDA Hold Timings in Transmitter

The IC_SDA_TX_HOLD register can be used to alter the timing of the generated SDA (ic_data_oe) signal by the DW_apb_i2c. Each value in the IC_SDA_TX_HOLD register represents a unit of one ic_clk period.

When the DW_apb_i2c is operating in Master Mode, the minimum tHD:DAT timing is one ic_clk period. Therefore even when IC_SDA_TX_HOLD has a value of zero, the DW_apb_i2c will drive SDA (ic_data_oe) one ic_clk cycle after driving SCL (ic_clk_oe) to logic 0. For all other values of IC_SDA_TX_HOLD, the following is true:

- Drive on SDA (ic_data_oe) occurs IC_SDA_TX_HOLD ic_clk cycles after driving SCL (ic_clk_oe) to logic 0

When the DW_apb_i2c is operating in Slave Mode, the minimum tHD:DAT timing is $SPKLEN + 7$ ic_clk periods, where SPKLEN is:

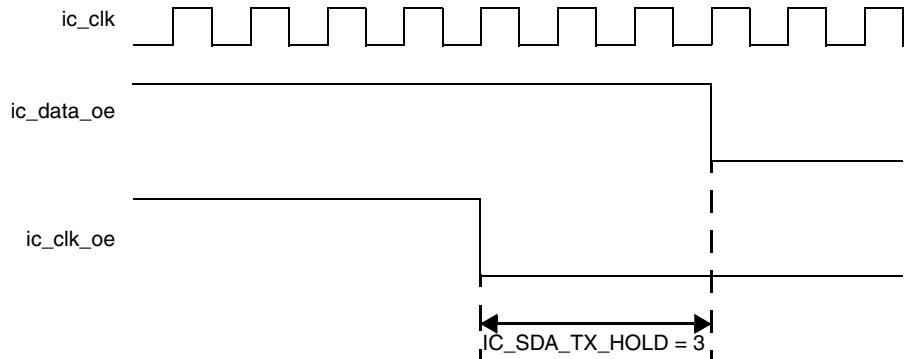
- IC_FS_SPKLEN if the component is operating in standard mode, fast mode, or fast mode plus
- IC_HS_SPKLEN if the component is operating in high speed mode

This delay allows for synchronization and spike suppression on the SCL (ic_clk_in_a) sample. Therefore, even when IC_SDA_TX_HOLD has a value less than $SPKLEN + 7$, the DW_apb_i2c drives SDA (ic_data_oe) $SPKLEN + 7$ ic_clk cycles after SCL (ic_clk_in) has transitioned to logic 0. For all other values of IC_SDA_TX_HOLD, the following is true:

- Drive on SDA (ic_data_oe) occurs $IC_SDA_TX_HOLD$ ic_clk cycles after SCL (ic_clk_in_a) has transitioned to logic 0.

Figure 3-34 shows the tHD:DAT timing generated by the DW_apb_i2c operating in Master Mode when $IC_SDA_TX_HOLD = 3$.

Figure 3-34 DW_apb_i2c Master Implementing tHD;DAT with IC_SDA_HOLD = 3



The programmed SDA hold time cannot exceed at any time the duration of the low part of scl. Therefore the programmed value cannot be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the scl period measured in ic_clk cycles.

3.17 DMA Controller Interface

The DW_apb_i2c has an optional built-in DMA capability that can be selected at configuration time; it has a handshaking interface to a DMA Controller to request and control transfers. The APB bus is used to perform the data transfer to or from the DMA. While the DW_apb_i2c DMA operation is designed in a generic way to fit any DMA controller as easily as possible, it is designed to work seamlessly, and best used, with the DesignWare DMA Controller, the DW_ahb_dmac. The settings of the DW_ahb_dmac that are relevant to the operation of the DW_apb_i2c are discussed here, mainly bit fields in the DW_ahb_dmac channel control register, CTL x , where x is the channel number.



Note When the DW_apb_i2c interfaces to the DW_ahb_dmac, the DW_ahb_dmac is always a flow controller; that is, it controls the block size. This must be programmed by software in the DW_ahb_dmac. The DW_ahb_dmac always transfers data using DMA burst transactions if possible, for efficiency. For more information, refer to the [DesignWare DW_ahb_dmac Databook](#). Other DMA controllers act in a similar manner.

The relevant DMA settings are discussed in the following sections.



Note The DMA output dma_finish is a status signal to indicate that the DMA block transfer is complete. DW_apb_i2c does not use this status signal, and therefore does not appear in the I/O port list.

3.17.1 Enabling the DMA Controller Interface

To enable the DMA Controller interface on the DW_apb_i2c, you must write the DMA Control Register (IC_DMA_CR). Writing a 1 into the TDMAE bit field of IC_DMA_CR register enables the DW_apb_i2c transmit handshaking interface. Writing a 1 into the RDMAE bit field of the IC_DMA_CR register enables the DW_apb_i2c receive handshaking interface.

3.17.2 Overview of Operation

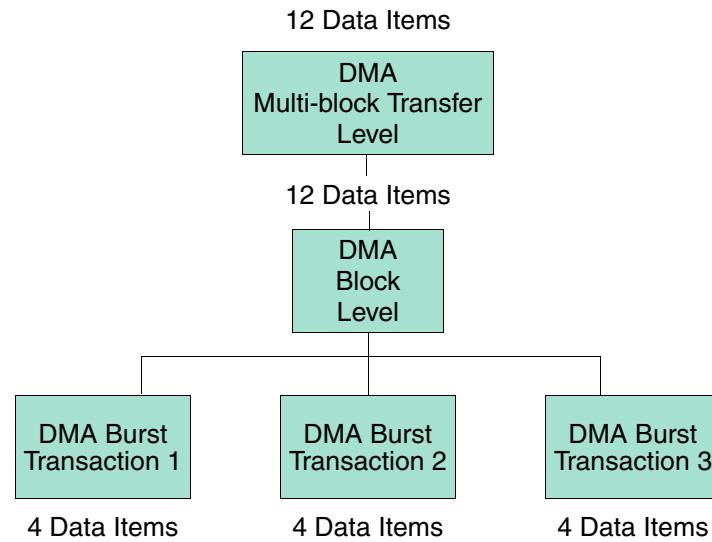
As a block flow control device, the DMA Controller is programmed by the processor with the number of data items (block size) that are to be transmitted or received by DW_apb_i2c; this is programmed into the BLOCK_TS field of the DW_ahb_dmac CTLx register.

The block is broken into a number of transactions, each initiated by a request from the DW_apb_i2c. The DMA Controller must also be programmed with the number of data items (in this case, DW_apb_i2c FIFO entries) to be transferred for each DMA request. This is also known as the burst transaction length and is programmed into the SRC_MSIZE/DEST_MSIZE fields of the DW_ahb_dmac CTLx register for source and destination, respectively.

Figure 3-35 shows a single block transfer, where the block size programmed into the DMA Controller is 12 and the burst transaction length is set to 4. In this case, the block size is a multiple of the burst transaction length. Therefore, the DMA block transfer consists of a series of burst transactions. If the DW_apb_i2c makes a transmit request to this channel, four data items are written to the DW_apb_i2c TX FIFO. Similarly, if the DW_apb_i2c makes a receive request to this channel, four data items are read from the DW_apb_i2c

RX FIFO. Three separate requests must be made to this DMA channel before all 12 data items are written or read.

Figure 3-35 Breakdown of DMA Transfer into Burst Transactions



Block Size: DMA.CTLx.BLOCK_TS=12

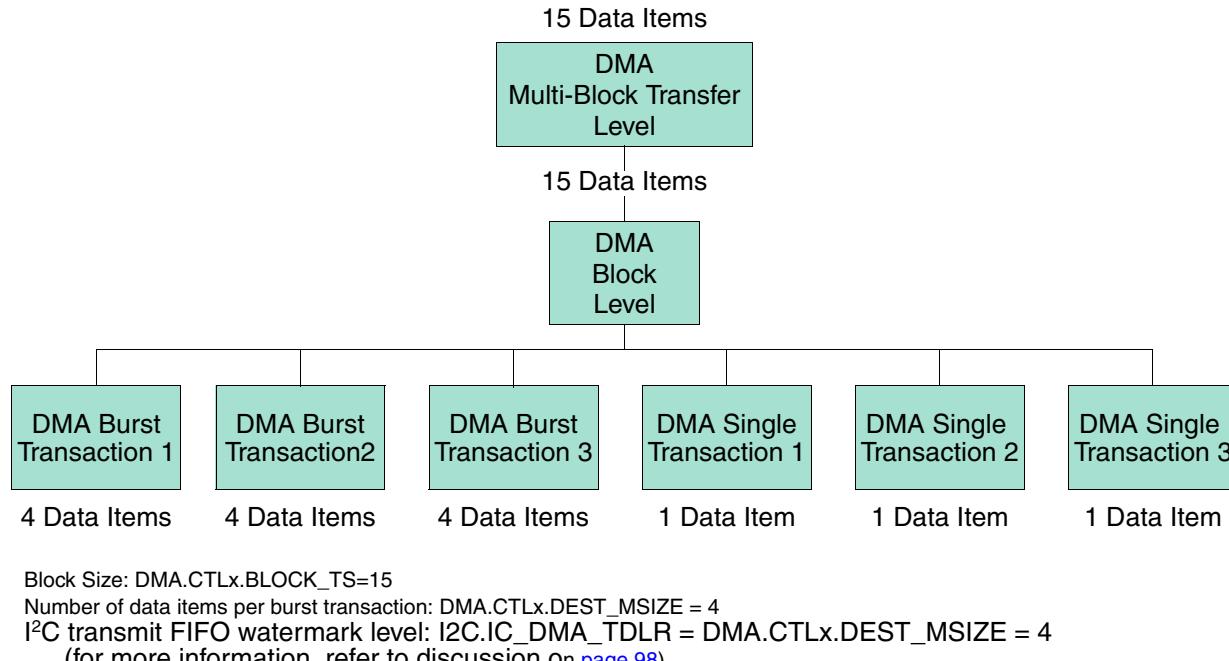
Number of data items per source burst transaction: DMA.CTLx.SRC_MSIZE = 4

I²C receive FIFO watermark level: I2C.DMARDLR + 1 = DMA.CTLx.SRC_MSIZE = 4

(for more information, refer to discussion on [page 99](#))

When the block size programmed into the DMA Controller is not a multiple of the burst transaction length, as shown in [Figure 3-36](#), a series of burst transactions followed by single transactions are needed to complete the block transfer.

Figure 3-36 Breakdown of DMA Transfer into Single and Burst Transactions



3.17.3 Transmit Watermark Level and Transmit FIFO Underflow

During DW_apb_i2c serial transfers, transmit FIFO requests are made to the DW_ahb_dmac whenever the number of entries in the transmit FIFO is less than or equal to the DMA Transmit Data Level Register (IC_DMA_TDRL) value; this is known as the watermark level. The DW_ahb_dmac responds by writing a burst of data to the transmit FIFO buffer, of length CTLx.DEST_MSIZE.

If IC_EMPTYFIFO_HOLD_MASTER_EN parameter is set to 0, data should be fetched from the DMA often enough for the transmit FIFO to perform serial transfers continuously; that is, when the FIFO begins to empty another DMA request should be triggered. Otherwise, the FIFO will run out of data causing a STOP to be inserted on the I²C bus. To prevent this condition, the user must set the watermark level correctly.

3.17.4 Choosing the Transmit Watermark Level

Consider the example where the assumption is made:

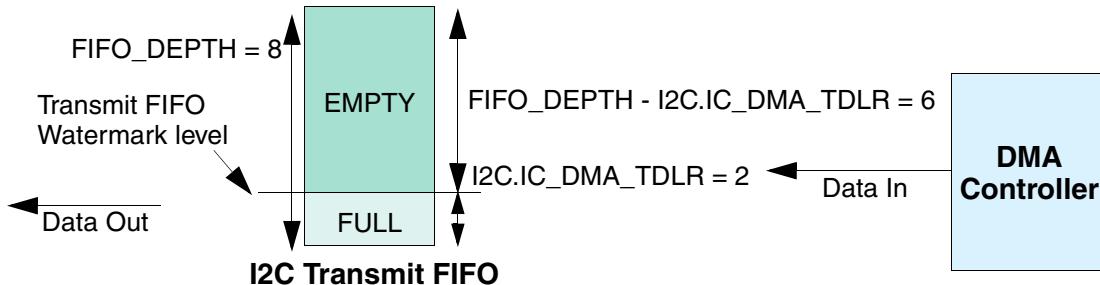
$$\text{DMA.CTLx.DEST_MSIZE} = \text{FIFO_DEPTH} - \text{I2C.IC_DMA_TDRL}$$

Here the number of data items to be transferred in a DMA burst is equal to the empty space in the Transmit FIFO. Consider two different watermark level settings.

3.17.4.1 Case 1: IC_DMA_TDLR = 2

- Transmit FIFO watermark level = I2C.IC_DMA_TDLR = 2
- DMA.CTLx.DEST_MSIZE = FIFO_DEPTH - I2C.IC_DMA_TDLR = 6
- I2C transmit FIFO_DEPTH = 8
- DMA.CTLx.BLOCK_TS = 30

Figure 3-37 Case 1 Watermark Levels



Therefore, the number of burst transactions needed equals the block size divided by the number of data items per burst:

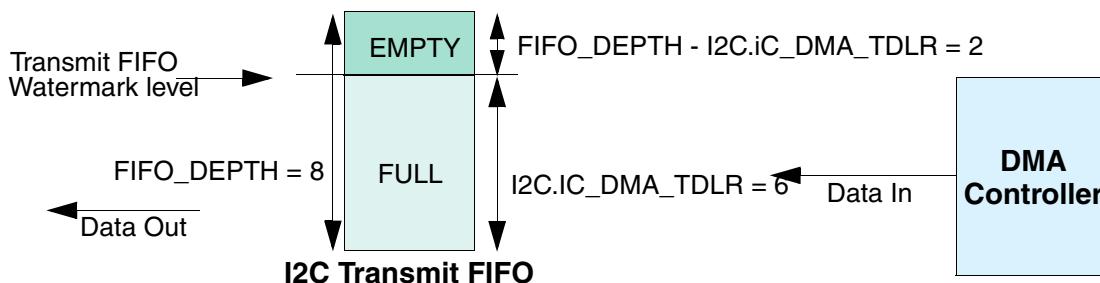
$$\text{DMA.CTLx.BLOCK_TS}/\text{DMA.CTLx.DEST_MSIZE} = 30/6 = 5$$

The number of burst transactions in the DMA block transfer is 5. But the watermark level, I2C.IC_DMA_TDLR, is quite low. Therefore, the probability of an I²C underflow is high where the I²C serial transmit line needs to transmit data, but where there is no data left in the transmit FIFO. This occurs because the DMA has not had time to service the DMA request before the transmit FIFO becomes empty.

3.17.4.2 Case 2: IC_DMA_TDLR = 6

- Transmit FIFO watermark level = I2C.IC_DMA_TDLR = 6
- DMA.CTLx.DEST_MSIZE = FIFO_DEPTH - I2C.IC_DMA_TDLR = 2
- I2C transmit FIFO_DEPTH = 8
- DMA.CTLx.BLOCK_TS = 30

Figure 3-38 Case 2 Watermark Levels



Number of burst transactions in Block:

$$\text{DMA.CTLx.BLOCK_TS}/\text{DMA.CTLx.DEST_MSIZE} = 30/2 = 15$$

In this block transfer, there are 15 destination burst transactions in a DMA block transfer. But the watermark level, I²C.IC_DMA_TDLR, is high. Therefore, the probability of an I²C underflow is low because the DMA controller has plenty of time to service the destination burst transaction request before the I²C transmit FIFO becomes empty.

Thus, the second case has a lower probability of underflow at the expense of more burst transactions per block. This provides a potentially greater amount of AMBA bursts per block and worse bus utilization than the former case.

Therefore, the goal in choosing a watermark level is to minimize the number of transactions per block, while at the same time keeping the probability of an underflow condition to an acceptable level. In practice, this is a function of the ratio of the rate at which the I²C transmits data to the rate at which the DMA can respond to destination burst requests.

For example, promoting the channel to the highest priority channel in the DMA, and promoting the DMA master interface to the highest priority master in the AMBA layer, increases the rate at which the DMA controller can respond to burst transaction requests. This in turn allows the user to decrease the watermark level, which improves bus utilization without compromising the probability of an underflow occurring.

3.17.5 Selecting DEST_MSIZEx and Transmit FIFO Overflow

As can be seen from [Figure 3-38](#) on page 97, programming DMA.CTLx.DEST_MSIZEx to a value greater than the watermark level that triggers the DMA request may cause overflow when there is not enough space in the I²C transmit FIFO to service the destination burst request. Therefore, the following equation must be adhered to in order to avoid overflow:

$$\text{DMA.CTL}x.\text{DEST_MSIZEx} \leq \text{I}^2\text{C.FIFO_DEPTH} - \text{I}^2\text{C.IC_DMA_TDLR} \quad (1)$$

In [Case 2: IC_DMA_TDLR = 6](#), the amount of space in the transmit FIFO at the time the burst request is made is equal to the destination burst length, DMA.CTLx.DEST_MSIZEx. Thus, the transmit FIFO may be full, but not overflowed, at the completion of the burst transaction.

Therefore, for optimal operation, DMA.CTLx.DEST_MSIZEx should be set at the FIFO level that triggers a transmit DMA request; that is:

$$\text{DMA.CTL}x.\text{DEST_MSIZEx} = \text{I}^2\text{C.FIFO_DEPTH} - \text{I}^2\text{C.IC_DMA_TDLR} \quad (2)$$

This is the setting used in [Figure 3-36](#) on page 96.

Adhering to equation (2) reduces the number of DMA bursts needed for a block transfer, and this in turn improves AMBA bus utilization.



The transmit FIFO will not be full at the end of a DMA burst transfer if the I²C has successfully transmitted one data item or more on the I²C serial transmit line during the transfer.

3.17.6 Receive Watermark Level and Receive FIFO Overflow

During DW_apb_i2c serial transfers, receive FIFO requests are made to the DW_ahb_dmac whenever the number of entries in the receive FIFO is at or above the DMA Receive Data Level Register; that is, IC_DMA_RDLR+1. This is known as the watermark level. The DW_ahb_dmac responds by fetching a burst of data from the receive FIFO buffer of length CTLx.SRC_MSIZEx.

Data should be fetched by the DMA often enough for the receive FIFO to accept serial transfers continuously; that is, when the FIFO begins to fill, another DMA transfer is requested. Otherwise, the FIFO will fill with data (overflow). To prevent this condition, the user must correctly set the watermark level.

3.17.7 Choosing the Receive Watermark level

Similar to choosing the transmit watermark level described earlier, the receive watermark level, IC_DMA_RDLR+1, should be set to minimize the probability of overflow, as shown in [Figure 3-39](#). It is a trade-off between the number of DMA burst transactions required per block versus the probability of an overflow occurring.

3.17.8 Selecting SRC_MSIZEx and Receive FIFO Underflow

As can be seen in [Figure 3-39](#), programming a source burst transaction length greater than the watermark level may cause underflow when there is not enough data to service the source burst request. Therefore, equation 3 below must be adhered to avoid underflow.

If the number of data items in the receive FIFO is equal to the source burst length at the time the burst request is made – DMA.CTLx.SRC_MSIZEx – the receive FIFO may be emptied, but not underflowed, at the completion of the burst transaction. For optimal operation, DMA.CTLx.SRC_MSIZEx should be set at the watermark level; that is:

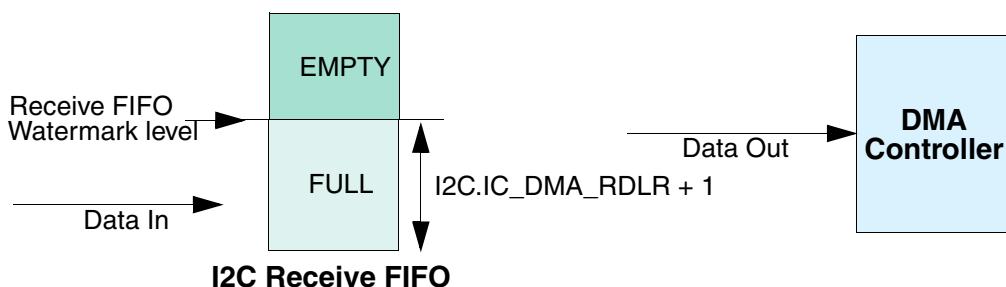
$$\text{DMA.CTL}x.\text{SRC_MSIZEx} = \text{I}^2\text{C.IC_DMA_RDLR} + 1 \quad (3)$$

Adhering to equation (3) reduces the number of DMA bursts in a block transfer, which in turn can avoid underflow and improve AMBA bus utilization.



The receive FIFO will not be empty at the end of the source burst transaction if the I²C has successfully received one data item or more on the I²C serial receive line during the burst.

Figure 3-39 I²C Receive FIFO



3.17.9 Handshaking Interface Operation

The following sections discuss the handshaking interface.

3.17.9.1 dma_tx_req, dma_rx_req

The request signals for source and destination, dma_tx_req and dma_rx_req, are activated when their corresponding FIFOs reach the watermark levels as discussed earlier.

The DW_ahb_dmac uses rising-edge detection of the dma_tx_req/dma_rx_req to identify a request on the channel. Upon reception of the dma_tx_ack/dma_rx_ack signal from the DW_ahb_dmac to indicate the burst transaction is complete, the DW_apb_i2c de-asserts the burst request signals, dma_tx_req/dma_rx_req, until dma_tx_ack/dma_rx_ack is de-asserted by the DW_ahb_dmac.

When the DW_apb_i2c samples that dma_tx_ack/dma_rx_ack is de-asserted, it can re-assert the dma_tx_req/dma_rx_req of the request line if their corresponding FIFOs exceed their watermark levels (back-to-back burst transaction). If this is not the case, the DMA request lines remain de-asserted.

Figure 3-40 shows a timing diagram of a burst transaction where pclk = hclk.

Figure 3-40 Burst Transaction – pclk = hclk

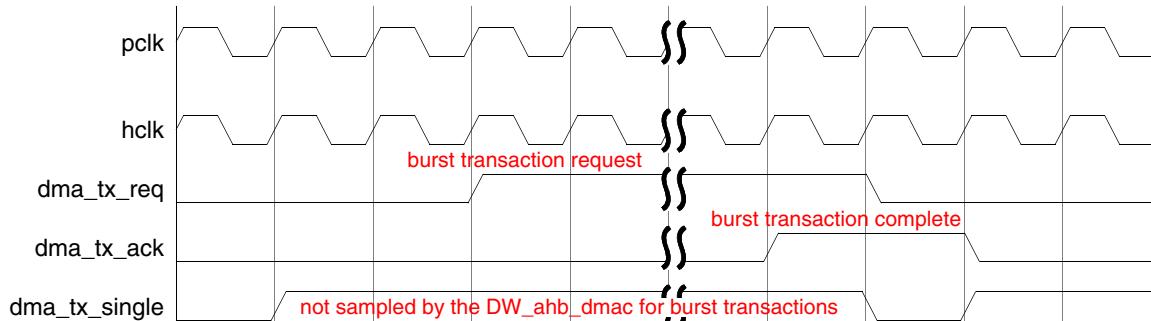
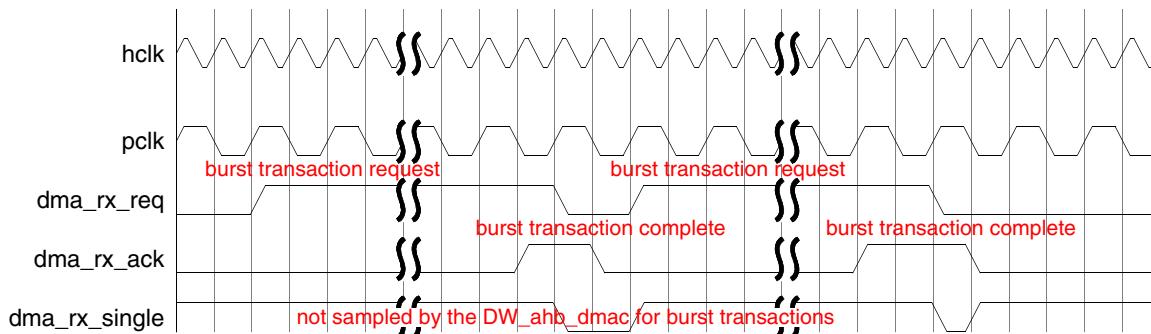


Figure 3-41 shows two back-to-back burst transactions where the hclk frequency is twice the pclk frequency.

Figure 3-41 Back-to-Back Burst Transactions – hclk = 2*pclk



The handshaking loop is as follows:

- dma_tx_req/dma_rx_req asserted by DW_apb_i2c
- > dma_tx_ack/dma_rx_ack asserted by DW_ahb_dmac
- > dma_tx_req/dma_rx_req de-asserted by DW_apb_i2c
- > dma_tx_ack/dma_rx_ack de-asserted by DW_ahb_dmac
- > dma_tx_req/dma_rx_req reasserted by DW_apb_i2c, if back-to-back transaction is required



Note The burst transaction request signals, `dma_tx_req` and `dma_rx_req`, are generated in the DW_apb_i2c off `pclk` and sampled in the DW_ahb_dmac by `hclk`. The acknowledge signals, `dma_tx_ack` and `dma_rx_ack`, are generated in the DW_ahb_dmac off `hclk` and sampled in the DW_apb_i2c of `pclk`. The handshaking mechanism between the DW_ahb_dmac and the DW_apb_i2c supports quasi-synchronous clocks; that is, `hclk` and `pclk` must be phase-aligned, and the `hclk` frequency must be a multiple of the `pclk` frequency.

Two things to note here:

1. The burst request lines, `dma_tx_req` signal/`dma_rx_req`, once asserted remain asserted until their corresponding `dma_tx_ack`/`dma_rx_ack` signal is received even if the respective FIFO's drop below their watermark levels during the burst transaction.
2. The `dma_tx_req`/`dma_rx_req` signals are de-asserted when their corresponding `dma_tx_ack`/`dma_rx_ack` signals are asserted, even if the respective FIFOs exceed their watermark levels.

3.17.9.2 `dma_tx_single`, `dma_rx_single`

The `dma_tx_single` signal is a status signal. It is asserted when there is at least one free entry in the transmit FIFO and cleared when the transmit FIFO is full. The `dma_rx_single` signal is a status signal. It is asserted when there is at least one valid data entry in the receive FIFO and cleared when the receive FIFO is empty.

These signals are needed by only the DW_ahb_dmac for the case where the block size, `CTLx.BLOCK_TS`, that is programmed into the DW_ahb_dmac is not a multiple of the burst transaction length, `CTLx.SRC_MSIZEx`, `CTLx.DEST_MSIZEx`, as shown in [Figure 3-36](#) on page [96](#). In this case, the DMA single outputs inform the DW_ahb_dmac that it is still possible to perform single data item transfers, so it can access all data items in the transmit/receive FIFO and complete the DMA block transfer. The DMA single outputs from the DW_apb_i2c are not sampled by the DW_ahb_dmac otherwise. This is illustrated in the following example.

Consider first an example where the receive FIFO channel of the DW_apb_i2c is as follows:

$$\text{DMA.CTLx.SRC_MSIZEx} = \text{I2C.iC_DMA_RDLR} + 1 = 4$$

$$\text{DMA.CTLx.BLOCK_TS} = 12$$

For the example in [Figure 3-35](#) on page [95](#), with the block size set to 12, the `dma_rx_req` signal is asserted when four data items are present in the receive FIFO. The `dma_rx_req` signal is asserted three times during the DW_apb_i2c serial transfer, ensuring that all 12 data items are read by the DW_ahb_dmac. All DMA requests read a block of data items and no single DMA transactions are required. This block transfer is made up of three burst transactions.

Now, for the following block transfer:

$$\text{DMA.CTLx.SRC_MSIZEx} = \text{I2C.iC_DMA_RDLR} + 1 = 4$$

$$\text{DMA.CTLx.BLOCK_TS} = 15$$

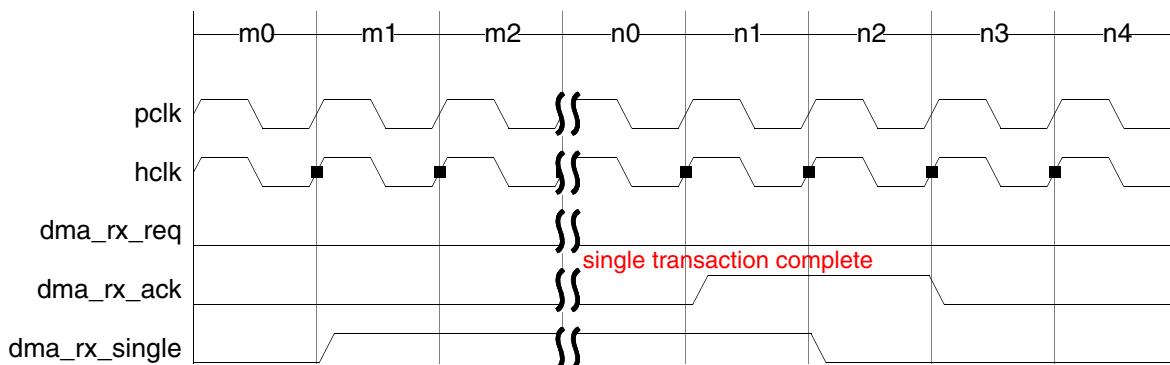
The first 12 data items are transferred as already described using three burst transactions. But when the last three data frames enter the receive FIFO, the `dma_rx_req` signal is not activated because the FIFO level is below the watermark level. The DW_ahb_dmac samples `dma_rx_single` and completes the DMA block

transfer using three single transactions. The block transfer is made up of three burst transactions followed by three single transactions.

[Figure 3-42](#) shows a single transaction. The handshaking loop is as follows:

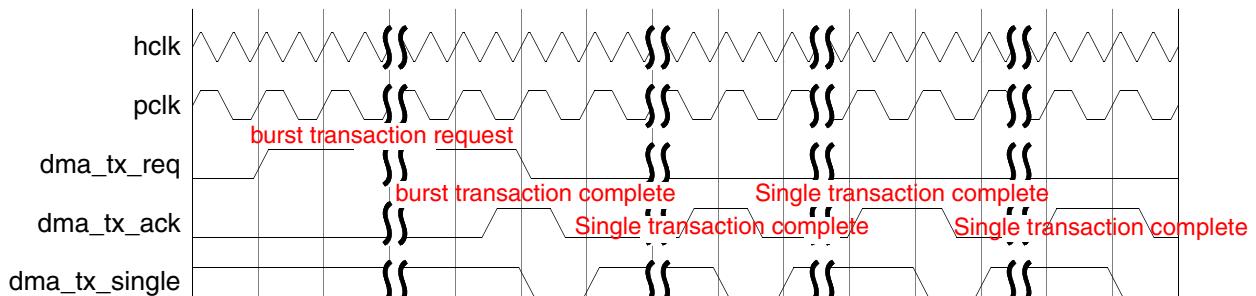
- dma_tx_single/dma_rx_single asserted by DW_apb_i2c
- > dma_tx_ack/dma_rx_ack asserted by DW_ahb_dmac
- > dma_tx_single/dma_rx_single de-asserted by DW_apb_i2c
- > dma_tx_ack/dma_rx_ack de-asserted by DW_ahb_dmac.

Figure 3-42 Single Transaction



[Figure 3-43](#) shows a burst transaction, followed by three back-to-back single transactions, where the hclk frequency is twice the pclk frequency.

Figure 3-43 Burst Transaction + 3 Back-to-Back Singles – hclk = 2*pclk



The single transaction request signals, `dma_tx_single` and `dma_rx_single`, are generated in the DW_apb_i2c on the pclk edge and sampled in DW_ahb_dmac on hclk. The acknowledge signals, `dma_tx_ack` and `dma_rx_ack`, are generated in the DW_ahb_dmac on the hclk edge hclk and sampled in the DW_apb_i2c on pclk. The handshaking mechanism between the DW_ahb_dmac and the DW_apb_i2c supports quasi-synchronous clocks; that is, hclk and pclk must be phase aligned and the hclk frequency must be a multiple of pclk frequency.

3.18 APB Interface

The host processor accesses data, control, and status information on the DW_apb_i2c through the APB interface. The DW_apb_i2c supports APB data bus widths of 8, 16, and 32 bits.

For more information about the APB Interface and data widths, refer to “[Integration Considerations](#)” on page [275](#).

4

Parameters

This chapter describes the configuration parameters used by the DW_apb_i2c. The settings of the configuration parameters determine the I/O signal list of the DW_apb_i2c peripheral.

4.1 Parameter Descriptions

You use coreConsultant or coreAssembler to configure the following parameters and generate the configured code.



Attention When using coreConsultant or coreAssembler, you can right-click on a parameter label to access a “What’s This” popup dialog that will tell you the details for that particular parameter. The information in each What’s This dialog essentially matches the information in the parameter descriptions below.

In the following tables, the values 0 and 1 occasionally appear in parentheses in the descriptions for the parameters. These are the logical values for parameter settings that appear in the coreConsultant and coreAssembler GUIs as check boxes, drop-down lists, a multiple selection, and so on.

4.2 Configuration Parameters

[Table 4-1](#) lists the DW_apb_i2c parameter descriptions.

Table 4-1 Top-Level Parameters

coreConsultant Field Label	Parameter Definition
System Configuration	
APB data bus width	Parameter Name: APB_DATA_WIDTH Legal Values: 8, 16, or 32 Default Value: 8 Dependencies: None Description: Width of the APB data bus.

Table 4-1 Top-Level Parameters (Continued)

coreConsultant Field Label	Parameter Definition
Device Configuration	
Highest speed I ² C mode supported	<p>Parameter Name: IC_MAX_SPEED_MODE</p> <p>Legal Values: Standard Mode (1), Fast Mode or Fast Mode Plus (2), High Speed Mode (3)</p> <p>Default Value: High Speed Mode (3)</p> <p>Dependencies: This Parameter is not applicable when Ultra-Fast Mode (IC_ULTRA_FAST_MODE=1) is enabled.</p> <p>Description: Maximum I²C mode supported. Controls the reset value of the SPEED bit field [2:1] of the I²C Control Register (<i>IC_CON</i>). Count registers are used to generate the outgoing clock SCL on the I²C interface. For speed modes faster than the configured maximum speed mode, the corresponding registers are not present in the top-level RTL as described as follows:</p> <ul style="list-style-type: none"> ■ If this parameter is set to “Standard,” then the <i>IC_FS_SCL_*</i>, <i>IC_HS_MADDR</i>, and <i>IC_HS_SCL_*</i> registers are not present. ■ If this parameter is set to “Fast,” then the <i>IC_HS_MADDR</i>, and <i>IC_HS_SCL_*</i> registers are not present.
Has I ² C default slave address of?	<p>Parameter Name: IC_DEFAULT_SLAVE_ADDR</p> <p>Legal Values: 0x000 to 0x3ff</p> <p>Default Value: 0x055</p> <p>Description: Reset value of DW_apb_i2c slave address. Controls the reset value of the I²C Slave Address Register (<i>IC_SAR</i>). The default values cannot be any of the reserved address locations: 0x00 to 0x07 or 0x78 to 0x7f.</p>
Has I ² C default target slave address of?	<p>Parameter Name: IC_DEFAULT_TAR_SLAVE_ADDR</p> <p>Legal Values: 0x000 to 0x3ff</p> <p>Default Value: 0x055</p> <p>Description: Reset value of DW_apb_i2c target slave address. Controls the reset value of the <i>IC_TAR</i> bit field (9:0) of the I²C Target Address Register (<i>IC_TAR</i>). The default values cannot be any of the reserved address locations: 0x00 to 0x07 or 0x78 to 0x7f.</p>
Has High Speed mode master code of?	<p>Parameter Name: IC_HS_MASTER_CODE</p> <p>Legal Values: 0x0 to 0x7</p> <p>Default Value: 0x1</p> <p>Dependencies: This parameter is enabled if IC_MAX_SPEED_MODE is set to High (3).</p> <p>This Parameter is not applicable when Ultra-Fast Mode (IC_ULTRA_FAST_MODE=1) is enabled.</p> <p>Description: High-speed mode master code of DW_apb_i2c. Controls the reset value of the I²C HS Master Mode Code Address Register (<i>IC_HS_MADDR</i>). This is a unique code that alerts other masters on the I²C bus that a high-speed mode transfer is going to begin. For more information about this code, refer to “Multiple Master Arbitration” on page 53.</p>

Table 4-1 Top-Level Parameters (Continued)

coreConsultant Field Label	Parameter Definition
Is an I ² C master?	<p>Parameter Name: IC_MASTER_MODE Legal Values: Unchecked (0) or Checked (1) Default Value: Checked (1) Dependencies: None Description: Controls whether DW_apb_i2c is enabled to be a master after reset. This parameter controls the reset value of bit 0 of the I²C Control Register (<i>IC_CON</i>). To enable the component to be a master, you must write a 1 in bit 0 of the <i>IC_CON</i> register. NOTE: If this parameter is checked (1), then you must ensure that the parameter IC_SLAVE_DISABLE is checked (1) as well.</p>
Disable Slave after reset?	<p>Parameter Name: IC_SLAVE_DISABLE Legal Values: Unchecked (0), Checked (1) Default Value: Checked (1) Dependencies: None. Description: Controls whether DW_apb_i2c has its slave enabled or disabled after reset. If checked, the DW_apb_i2c slave interface is disabled after reset. The slave also can be disabled by programming a 1 into bit 6 of the I²C Control Register (<i>IC_CON</i>). By default, the slave is enabled. NOTE: If this parameter is unchecked (0), then you must ensure that the parameter IC_MASTER_MODE is unchecked (0) as well.</p>
Supports 10-bit addressing in master mode?	<p>Parameter Name: IC_10BITADDR_MASTER Legal Values: Unchecked (0) or Checked (1) Default Value: Checked (1) Dependencies: None Description: Controls whether DW_apb_i2c supports 7- or 10-bit addressing on the I²C interface after reset when acting as a master. Controls the reset value of bit 4 of the I²C Control Register (<i>IC_CON</i>). Master-generated transfers use this number of address bits. Additionally, it can be reprogrammed by software by writing to the <i>IC_CON</i> register.</p>
Supports 10-bit addressing in slave mode?	<p>Parameter Name: IC_10BITADDR_SLAVE Legal Values: Unchecked (0) or Checked (1) Default Value: Checked (1) Dependencies: None Description: Controls whether DW_apb_i2c slave supports 7- or 10-bit addressing on the I²C interface after reset when acting as a slave. Controls reset value of part of the <i>IC_CON</i> register. DW_apb_i2c responds to this number of address bits when acting as a slave; it can be programmed by software.</p>

Table 4-1 Top-Level Parameters (Continued)

coreConsultant Field Label	Parameter Definition
Depth of transmit buffer is?	Parameter Name: IC_TX_BUFFER_DEPTH Legal Values: 2 to 256 Default Value: 8 Dependencies: None Description: Depth of the transmit buffer. The buffer is 9-bits wide; 8 bits for the data, and 1 bit for the read or write command.
Depth of receive buffer is?	Parameter Name: IC_RX_BUFFER_DEPTH Legal Values: 2 to 256 Default Value: 8 Dependencies: None Description: Depth of receive buffer; the buffer is 8 bits wide.
Transmit buffer threshold level is?	Parameter Name: IC_TX_TL Legal Values: 0 to (IC_TX_BUFFER_DEPTH – 1) Default Value: 0 Dependencies: None Description: Reset value for the threshold level of the transmit buffer. This parameter controls the reset value of the I ² C Transmit FIFO Threshold Level Register (<i>IC_TX_TL</i>).
Receive buffer threshold value is?	Parameter Name: IC_RX_TL Legal Values: 0 to (IC_RX_BUFFER_DEPTH – 1) Default Value: 0 Dependencies: None Description: Reset value for the threshold level of the receive buffer. This parameter controls the reset value of the I ² C Receive FIFO Threshold Level Register (<i>IC_RX_TL</i>).
Allow restart conditions to be sent when acting as a master?	Parameter Name: IC_RESTART_EN Legal Values: Checked (1) or Unchecked (0) Default Value: Checked (1) Dependencies: None Description: Controls the reset value of bit 5 (<i>IC_RESTART_EN</i>) in the <i>IC_CON</i> register. By default, this parameter is checked, which allows RESTART conditions to be sent when DW_apb_i2c is acting as a master. Some older slaves do not support handling RESTART conditions; however, RESTART conditions are used in several I ² C operations. When the RESTART is disabled, the DW_apb_i2c master is incapable of performing the following functions: <ul style="list-style-type: none"> ■ Sending a START BYTE ■ Performing any high-speed mode operation ■ Performing direction changes in combined format mode ■ Performing a read operation with a 10-bit address

Table 4-1 Top-Level Parameters (Continued)

coreConsultant Field Label	Parameter Definition
Hardware reset value for IC_SDA_SETUP register	<p>Parameter Name: IC_DEFAULT_SDA_SETUP Legal Values: 0x02 to 0xff Default Value: 0x64 Dependencies: This Parameter is not applicable when Ultra-Fast Mode (IC_ULTRA_FAST_MODE=1) is enabled. Description: Determines the reset value for the IC_SDA_SETUP register, which in turn controls the time delay—in terms of the number of ic_clk periods—introduced in the rising edge of SCL relative to SDA changing when a read-request is serviced.</p>
Hardware reset value for IC_SDA_HOLD register	<p>Parameter Name: IC_DEFAULT_SDA_HOLD Legal Values: 0x01 to 0xfffffff Default Value: 0x1 Dependencies: None Description: Determines the reset value for the IC_SDA_HOLD register, which in turn controls the SDA hold time implemented by DW_apb_i2c (when transmitting or receiving, as either master or slave). The relevant I2C requirement is tHD;DAT as detailed in the I2C Bus Specifications. The programmed SDA hold time as transmitter cannot exceed at any time the duration of the low part of scl. Therefore it is recommended that the configured default value should not be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the scl period measured in ic_clk cycles, for the maximum speed mode the component is configured for.</p>
IC_ACK_GENERAL_CALL set to acknowledge I ² C general calls on reset	<p>Parameter Name: IC_DEFAULT_ACK_GENERAL_CALL Legal Values: Unchecked (0) or Checked (1) Default Value: Checked (1) Dependencies: This Parameter is not applicable when Ultra-Fast Mode (IC_ULTRA_FAST_MODE=1) is enabled. Description: Assigns the default reset value for the IC_ACK_GENERAL_CALL register.</p>
External Configuration	
Include DMA handshaking interface signals?	<p>Parameter Name: IC_HAS_DMA Legal Values: Checked (1) or Unchecked (0) Default Value: Unchecked (0) Dependencies: None Description: When checked, includes the DMA handshaking interface signals at the top-level I/O. For more information about these signals, see “Signal Descriptions” on page 125.</p>
Single Interrupt output port present?	<p>Parameter Name: IC_INTR_IO Legal Values: Unchecked (0) or Checked (1) Default Value: Unchecked (0) Dependencies: None Description: If unchecked, each interrupt source has its own output. If checked, all interrupt sources are combined into a single output.</p>

Table 4-1 Top-Level Parameters (Continued)

coreConsultant Field Label	Parameter Definition
Polarity of interrupts is active high?	<p>Parameter Name: IC_INTR_POL</p> <p>Legal Values: Unchecked (0) or Checked (1)</p> <p>Default Value: Checked (1)</p> <p>Dependencies: None</p> <p>Description: By default, the polarity of the output interrupt lines is active high (checked).</p>
Internal Configuration	
Add Encoded Parameters	<p>Parameter Name: IC_ADD_ENCODED_PARAMS</p> <p>Legal Values: Unchecked (0) or Checked (1)</p> <p>Default Value: Checked (1)</p> <p>Dependencies: None</p> <p>Description: Adding the encoded parameters gives firmware an easy and quick way of identifying the DesignWare component within an I/O memory map. Some critical design-time options determine how a driver should interact with the peripheral. There is a minimal area overhead by including these parameters.</p> <p>When bit 7 of the <i>IC_COMP_PARAM_1</i> is read and contains a '1,' the encoded parameters can be read via software. If this bit is a '0,' then the entire register is '0' regardless of the setting of any of the other parameters that are encoded in the register's bits. For details about this register, see the <i>IC_COMP_PARAM_1</i> register on page 225.</p> <p>Note: Unique drivers must be developed for each configuration of the DW_apb_i2c. Based on the configuration, the registers in the IP can differ; thus the same driver cannot be used with different configurations of the IP.</p>
Specify clock counts directly instead of supplying clock frequency?	<p>Parameter Name: IC_USE_COUNTS</p> <p>Legal Values: Checked (1) or Unchecked (0)</p> <p>Default Value: Unchecked (0)</p> <p>Dependencies: None</p> <p>Description: Determines whether *CNT values are provided directly or by specifying the ic_clk clock frequency and letting coreConsultant (or coreAssembler) calculate the count values.</p> <p>When this parameter is checked, the reset values of the *CNT registers are specified by the corresponding *COUNT configuration parameters, which may be user-defined or derived (see the standard mode, fast mode or fast mode plus, and high speed mode parameters later in this table).</p> <p>When unchecked (default setting), the reset values of the *CNT registers are calculated from the configuration parameter IC_CLOCK_PERIOD.</p> <p>Note: For fast mode plus, reprogram the IC_FS_SCL_*CNT register to achieve the required data rate when unchecked.</p>

Table 4-1 Top-Level Parameters (Continued)

coreConsultant Field Label	Parameter Definition
Hard code the count values for each mode?	<p>Parameter Name: IC_HC_COUNT_VALUES Legal Values: Checked (1) or Unchecked (0) Default Value: Unchecked (0) Dependencies: None.</p> <p>Description: By checking this parameter, the *CNT registers are set to read only. Unchecking this parameter (default setting) allows the *CNT registers to be writable.</p> <p>Regardless of the setting, the *CNT registers are always readable and have reset values from the corresponding *COUNT configuration parameters, which may be user-defined or derived (see standard, fast, fast mode plus, or high speed mode parameters later in this table). The count registers begin on page 175.</p> <p>Note: Since the DW_apb_i2c uses the same high and low count registers for fast mode and fast mode plus, if this parameter is checked (1) the IC_FS_SCL_*CNT registers are hard coded to either fast mode or fast mode plus. Consequently, DW_apb_i2c can operate in either fast mode or fast mode plus, but not in both modes simultaneously.</p> <p>For fast mode plus, it is recommended that this parameter be Unchecked (0).</p>
ic_clk has a period of? (ns integers only)	<p>Parameter Name: IC_CLOCK_PERIOD Legal Values: 2 to 2147483647 (ns) Default Value: 10 (ns) – high-speed mode Dependencies: This parameter is disabled if the IC_USE_COUNTS parameter is checked (1).</p> <p>Description: Specifies the period of incoming ic_clk, which is used to generate outgoing I2C interface SCL clock (ns integers only). When the count values are used to generate the IC_CLOCK_PERIOD, then the IC_MAX_SPEED_MODE setting determines the actual period:</p> <ul style="list-style-type: none"> IC_MAX_SPEED_MODE = Standard => 500 ns IC_MAX_SPEED_MODE = Fast => 100 ns IC_MAX_SPEED_MODE = High => 10 ns IC_ULTRA_FAST_MODE =1 => 25ns <p>Note: For fast mode plus, reprogram the IC_FS_SCL_*CNT register to achieve the required data rate.</p>
Relationship between pclk and ic_clk is?	<p>Parameter Name: IC_CLK_TYPE Legal Values: Identical (0), Asynchronous (1) Default Value: Asynchronous (1) Dependencies: None.</p> <p>Description: Specifies the relationship between pclk and ic_clk.</p> <p>NOTE: ic_clk frequency must be greater than or equal to pclk frequency.</p> <p>Identical (0): clocks are identical; no metastability flops are used for data passing between clock domains.</p> <p>Asynchronous (1): clocks may be completely asynchronous to each other, metastability flops are used for data passing between clock domains.</p>

Table 4-1 Top-Level Parameters (Continued)

coreConsultant Field Label	Parameter Definition
Standard Speed Mode Configuration	
Std speed SCL high count is?	<p>Parameter Name: IC_SS_SCL_HIGH_COUNT Legal Values: Hex value in range 0x0006 to 0xffff Default Value: 0x0190 (400 based on 100 MHz ic_clk) Dependencies: This parameter is active when the IC_USE_COUNTS parameter is checked (1); otherwise, this value is automatically calculated using the IC_CLK_PERIOD parameter. This Parameter is not applicable when Ultra-Fast Mode (IC_ULTRA_FAST_MODE=1) is enabled.</p> <p>Description: Reset value of Standard Speed I2C Clock SCL High Count register (<i>IC_SS_SCL_HCNT</i>). The value must be calculated based on the I²C data rate desired and I²C clock frequency. For more information, see the IC_SS_SCL_HCNT register on page 175.</p>
Std speed SCL low count is?	<p>Parameter Name: IC_SS_SCL_LOW_COUNT Legal Values: Hex value in range 0x0008 to 0xffff Default Value: 0x01d6 (470 based on 100 MHz ic_clk) Dependencies: This parameter is active when the IC_USE_COUNTS parameter is checked (1); otherwise, this value is automatically calculated using the IC_CLK_PERIOD parameter. This Parameter is not applicable when Ultra-Fast Mode (IC_ULTRA_FAST_MODE=1) is enabled.</p> <p>Description: Reset value of Standard Speed I2C Clock SCL Low Count register (<i>IC_SS_SCL_HCNT</i>). Value must be calculated based on I²C data rate desired and I²C clock frequency. For more information, see IC_SS_SCL_LCNT register on page 176. When parameter IC_USE_COUNTS = 0, this parameter is automatically calculated using the IC_CLK_PERIOD parameter.</p>
Fast Mode or Fast Mode Plus	
Fast Mode or Fast Mode Plus SCL high count is?	<p>Parameter Name: IC_FS_SCL_HIGH_COUNT Legal Values: Hex value in range 0x0006 to 0xffff Default Value: 0x003c (60 based on 100 MHz ic_clk in Fast Mode) Dependencies: This parameter is active when the IC_USE_COUNTS parameter is checked (1); otherwise, this value is automatically calculated using the IC_CLK_PERIOD parameter. If the IC_MAX_SPEED_MODE parameter is set to “standard,” this parameter is disabled. This Parameter is not applicable when Ultra-Fast Mode (IC_ULTRA_FAST_MODE=1) is enabled.</p> <p>Description: Reset value of Fast Mode or Fast Mode Plus I2C Clock SCL High Count register (<i>IC_FS_SCL_HCNT</i>). Value must be calculated based on I²C data rate desired and I²C clock frequency. For more information, see IC_FS_SCL_HCNT register on page 177.</p>

Table 4-1 Top-Level Parameters (Continued)

coreConsultant Field Label	Parameter Definition
Fast Mode or Fast Mode Plus SCL low count is?	<p>Parameter Name: IC_FS_SCL_LOW_COUNT Legal Values: Hex value in range 0x0008 to 0xffff Default Value: 0x0082 (130 based on 100 MHz ic_clk in Fast Mode) Dependencies: This parameter is active when the IC_USE_COUNTS parameter is checked (1); otherwise, this value is automatically calculated using the IC_CLK_PERIOD parameter. If the IC_MAX_SPEED_MODE parameter is set to “standard,” this parameter is disabled. This Parameter is not applicable when Ultra-Fast Mode (IC_ULTRA_FAST_MODE=1) is enabled.</p> <p>Description: Reset value of Fast Mode or Fast Mode Plus I2C Clock SCL Low Count register (<i>IC_FS_SCL_LCNT</i>). Value must be calculated based on I²C data rate and I2C clock frequency. For more information, see the <i>IC_FS_SCL_LCNT</i> register on page 178.</p>
High Speed Mode	
For high speed mode systems the I ² C bus loading is? (pF)	<p>Parameter Name: IC_CAP_LOADING Legal Values: 100 or 400 Default Value: 100 Dependencies: This parameter is not present in non-high speed mode systems (IC_MAX_SPEED_MODE != high). This Parameter is not applicable when Ultra-Fast Mode (IC_ULTRA_FAST_MODE=1) is enabled.</p> <p>Description: For high-speed mode, the bus loading affects the high and low pulse width of SCL.</p>
High speed SCL high count is?	<p>Parameter Name: IC_HS_SCL_HIGH_COUNT Legal Values: Hex value in range 0x0006 to 0xffff Default Value: 0x006 (6 based on 100 MHz ic_clk, 400 pF bus loading) Dependencies: This parameter is active when the IC_USE_COUNTS parameter is checked (1); otherwise, this value is automatically calculated using the IC_CLK_PERIOD parameter. If the IC_MAX_SPEED_MODE parameter is set to “standard” or “fast”, this parameter is irrelevant. This Parameter is not applicable when Ultra-Fast Mode (IC_ULTRA_FAST_MODE=1) is enabled.</p> <p>Description: Reset value of High Speed I2C Clock SCL High Count register (<i>IC_HS_SCL_HCNT</i>). Value must be calculated based on I²C data rate desired and high speed I²C clock frequency. For more information, see <i>IC_HS_SCL_HCNT</i> register on page 179.</p>

Table 4-1 Top-Level Parameters (Continued)

coreConsultant Field Label	Parameter Definition
High speed SCL low count is?	<p>Parameter Name: IC_HS_SCL_LOW_COUNT Legal Values: Hex value in range 0x0008 to 0xffff Default Value: 0x0010 (16 based on 100 MHz ic_clk, 400 pF bus loading) Dependencies: This parameter is active when the IC_USE_COUNTS parameter is checked (1); otherwise, this value is automatically calculated using the IC_CLK_PERIOD parameter. If the IC_MAX_SPEED_MODE parameter is set to “standard” or “fast”, this parameter is irrelevant. This Parameter is not applicable when Ultra-Fast Mode (IC_ULTRA_FAST_MODE=1) is enabled.</p> <p>Description: Reset value of High Speed I2C Clock SCL Low Count register (IC_HS_SCL_LCNT). The value must be calculated based on I2C data rate and I2C clock frequency. For more information, see IC_HS_SCL_LCNT register on page 180.</p>
Spike Suppression Configuration	
Maximum length (in ic_clk cycles) of suppressed spikes in Standard Mode, Fast Mode, and Fast Mode Plus	<p>Parameter Name: IC_DEFAULT_FS_SPKLEN Legal Values: Hex value in range 0x01 to 0xFF Default Value: Max(1,ceiling(50/IC_CLOCK_PERIOD)) Dependencies: Initial value automatically calculated using IC_CLOCK_PERIOD. This Parameter is not applicable when Ultra-Fast Mode (IC_ULTRA_FAST_MODE=1) is enabled.</p> <p>Description: Reset value of maximum suppressed spike length register in Standard Mode, Fast Mode, and Fast Mode Plus (IC_FS_SPKLEN register). Spike length is expressed in ic_clk cycles, and this value is calculated based on the value of IC_CLOCK_PERIOD</p>
Maximum length (in ic_clk cycles) of suppressed spikes in HS mode	<p>Parameter Name: IC_DEFAULT_HS_SPKLEN Legal Values: Hex value in range 0x01 to 0xFF Default Value: Max(1,ceiling(10/IC_CLOCK_PERIOD)) Dependencies: Initial value automatically calculated using IC_CLOCK_PERIOD. If MAX_SPEED_MODE is set to standard or fast, this parameter is irrelevant. This Parameter is not applicable when Ultra-Fast Mode (IC_ULTRA_FAST_MODE=1) is enabled.</p> <p>Description: Reset value of maximum suppressed spike length register in HS modes (IC_HS_SPKLEN register). Spike length is expressed in ic_clk cycles, and this value is calculated based on the value of IC_CLOCK_PERIOD.</p>
Additional Features	
Allow dynamic updating of the TAR address?	<p>Parameter Name: I2C_DYNAMIC_TAR_UPDATE Legal Values: Unchecked (0) or Checked (1) Default Value: Unchecked (0) Dependencies: None</p> <p>Description: When checked, allows the IC_TAR register to be updated dynamically. Setting this parameter affects the operation of DW_apb_i2c when it is in master mode. For more details, see “Master Mode Operation” on page 60.</p>

Table 4-1 Top-Level Parameters (Continued)

coreConsultant Field Label	Parameter Definition
Enable register to generate NACKs for data received by Slave?	<p>Parameter Name: IC_SLV_DATA_NACK_ONLY Legal Values: Unchecked (0) or Checked (1) Default Value: Unchecked (0) Dependencies: This Parameter is not applicable when Ultra-Fast Mode (IC_ULTRA_FAST_MODE=1) is enabled.</p> <p>Description: Enables an additional register to control whether DW_apb_i2c generates a NACK after a data byte has been transferred to it. This NACK generation only occurs when DW_apb_i2c is a slave-receiver. If this register is set to a value of 1, it can only generate a NACK after a data byte is received; hence, the data transfer is aborted and the data received is not pushed to the receive buffer.</p> <p>When the register is set to a value of 0, it generates NACK/ACK, depending on normal criteria. If this option is selected, the default value of the IC_SLV_DATA_NACK_ONLY register is always 0. The register must be explicitly programmed to a value of 1 if NACKs are to be generated. The register can only be written to successfully if DW_apb_i2c is disabled (IC_ENABLE[0] = 0) or the slave part is inactive (IC_STATUS[6] = 0).</p>
Hold transfer when Tx FIFO is empty?	<p>Parameter Name: IC_EMPTYFIFO_HOLD_MASTER_EN Legal Values: Unchecked (0) or Checked (1) Default Value: Unchecked (0) Dependencies: None</p> <p>Description: If this parameter is set, the master only completes a transfer—that is, issues a STOP—when it finds a Tx FIFO entry tagged with a Stop bit. If the Tx FIFO empties and the last byte does not have the Stop bit set, the master stalls the transfer by holding the SCL line low.</p> <p>If this parameter is not set, the master completes a transfer when the Tx FIFO is empty. In SMBus Mode (IC_SMBUS=1), IC_EMPTYFIFO_HOLD_MASTER_EN should be always enabled.</p>
When Rx FIFO is physically full, hold the bus till Rx FIFO has space available?	<p>Parameter Name: IC_RX_FULL_HLD_BUS_EN Legal Values: Unchecked (0), Checked (1) Default Value: Unchecked (0) Dependencies: This Parameter is not applicable when Ultra-Fast Mode (IC_ULTRA_FAST_MODE=1) is enabled.</p> <p>Description: When the Rx FIFO is physically full to its RX_BUFFER_DEPTH, this parameter provides a hardware method to hold the bus till the Rx FIFO data is read out and there is space available in the FIFO.</p> <p>This parameter can be used when DW_apb_i2c is either a slave-receiver (that is, data is written to the device) or a master-receiver (that is, the device reads data from a slave).</p> <p>NOTE: If this parameter is checked, then the RX_OVER interrupt is never set to 1 as the criteria to set this interrupt are never met. The RX_OVER interrupt can be found in the IC_INTR_STAT and IC_RAW_INTR_STAT registers. It is also an optional output signal, ic_rx_over_intr(_n).</p>

Table 4-1 Top-Level Parameters (Continued)

coreConsultant Field Label	Parameter Definition
Enable restart detect interrupt in slave mode?	<p>Parameter Name: IC_SLV_RESTART_DET_EN Legal Values: Unchecked (0), Checked (1) Default Value: Unchecked (0) Dependencies: None Description: When checked, allows the slave to detect and issue the restart interrupt when the slave is addressed. Setting this parameter affects the operation of DW_apb_i2c only when it is in slave mode. This controls the RESTART_DET bit in the IC_RAW_INTR_STAT, IC_INTR_MASK, IC_INTR_STAT, and IC_CLR_RESTART_DET registers. This also controls the ic_restart_det_intr(_n) and ic_intr(_n) signals.</p>
Generate STOP_DET interrupt only if Master is active?	<p>Parameter Name: IC_STOP_DET_IF_MASTER_ACTIVE Legal Values: Unchecked (0), Checked (1) Default Value: Unchecked (0) Dependencies: This Parameter is not applicable when Ultra-Fast Mode (IC_ULTRA_FAST_MODE=1) is enabled. Description: Controls whether DW_apb_i2c generates a STOP_DET interrupt when the master is active. <ul style="list-style-type: none"> ■ Checked (1): Allows the master to detect and issue the stop interrupt when the master is active. ■ Unchecked (0): The master always detects and issues the stop interrupt irrespective of whether it is active. This parameter affects the operation of DW_apb_i2c when it is in master mode. This controls the STOP_DET bit of the C_RAW_INTR_STAT, IC_INTR_MASK, IC_INTR_STAT, and IC_CLR_STOP_DET registers. This parameter also controls the ic_stop_det_intr(_n) and ic_intr(_n) signals.</p>
Include Status bits to indicate the reason for clock stretching?	<p>Parameter Name: IC_STAT_FOR_CLK_STRETCH Legal Values: Unchecked (0), Checked (1) Default Value: Unchecked (0) Dependencies: This Parameter is not applicable when Ultra-Fast Mode (IC_ULTRA_FAST_MODE=1) is enabled. Description: If this parameter is set, the DW_apb_i2c consists of Status bits that indicate the reason for clock stretching in the IC_STATUS Register.</p>
Include programmable bit for blocking Master commands?	<p>Parameter Name: IC_TX_CMD_BLOCK Legal Values: Unchecked (0), Checked (1) Default Value: Unchecked (0) Dependencies: None Description: Controls whether DW_apb_i2c transmits data on I²C bus as soon as data is available in the Tx FIFO. When checked, allows the master to hold the transmission of data on the I²C bus when the Tx FIFO has data to transmit.</p>

Table 4-1 Top-Level Parameters (Continued)

coreConsultant Field Label	Parameter Definition
Enable blocking Master commands after reset?	<p>Parameter Name: IC_TX_CMD_BLOCK_DEFAULT</p> <p>Legal Values: Unchecked (0), Checked (1)</p> <p>Default Value: Unchecked (0)</p> <p>Dependencies: IC_TX_CMD_BLOCK=1</p> <p>Description: Controls whether DW_apb_i2c has its transmit command block enabled or disabled after reset. If checked, the DW_apb_i2c blocks the transmission of data on the I²C bus.</p>
Include First data byte indication in IC_DATA_CMD register?	<p>Parameter Name: IC_FIRST_DATA_BYTE_STATUS</p> <p>Legal Values: Unchecked (0), Checked (1)</p> <p>Default Value: Unchecked (0)</p> <p>Dependencies: None</p> <p>Description: Controls whether DW_apb_i2c generates the FIRST_DATA_BYTE status bit in the IC_DATA_CMD register. When checked, the master/slave receiver sets the FIRST_DATA_BYTE status bit in the IC_DATA_CMD register to indicate whether the data present in the IC_DATA_CMD register is the first data byte after the address phase of a receive transfer.</p> <p>Note: In the case when APB_DATA_WIDTH is set to 8, you must perform two APB reads to the IC_DATA_CMD register to get status on bit 11.</p>
Avoid Rx FIFO Flush on Transmit Abort?	<p>Parameter Name: IC_AVOID_RX_FIFO_FLUSH_ON_TX_ABRT</p> <p>Legal Values: Unchecked (0), Checked (1)</p> <p>Default Value: Unchecked (0)</p> <p>Dependencies: This Parameter is not applicable when Ultra-Fast Mode (IC_ULTRA_FAST_MODE=1) is enabled.</p> <p>Description: This Parameter controls the Rx FIFO Flush during the Transmit Abort. If this parameter is checked(1), only the Tx FIFO is flushed (not the Rx FIFO) on the Transmit Abort. If this parameter is unchecked(0). both the Tx FIFO and Rx FIFO are flushed on Transmit Abort.</p>
Enable IC_CLK Frequency Reduction?	<p>Parameter Name: IC_CLK_FREQ_OPTIMIZATION</p> <p>Legal Values: Unchecked (0), Checked (1)</p> <p>Default Value: Unchecked (0)</p> <p>Description: This parameter is used to reduce the system clock frequency (ic_clk) by reducing the internal latency required to generate the high period and low period of the SCL line</p> <p>Dependencies: DWC-APB-Advanced-Source License</p>

Table 4-1 Top-Level Parameters (Continued)

coreConsultant Field Label	Parameter Definition
I2C 3.0 Parameters	
Include Bus Clear feature?	<p>Parameter Name: IC_BUS_CLEAR_FEATURE Legal Values: Unchecked (0), Checked (1) Default Value: Unchecked (0)</p> <p>Dependencies: This Parameter is not applicable when Ultra-Fast Mode (IC_ULTRA_FAST_MODE=1) is enabled. In SMBus Mode (IC_SMBUS=1), this feature is always enabled.</p> <p>Description: If this parameter is set:</p> <ul style="list-style-type: none"> ■ If an SDA line is stuck at low for IC_SDA_STUCK_LOW_TIMEOUT period of ic_clk, DW_apb_i2c master generates a master transmit abort (IC_TX_ABRT_SOURCE[17]: ABRT_SDA_STUCK_AT_LOW) to indicate SDA stuck at low. ■ User can enable the SDA_STUCK_RECOVERY_EN (IC_ENABLE[3]) register bit to recover the SDA by sending at most 9 SCL clocks. ■ If SDA line is recovered, then the master generates a STOP and auto clear the 'SDA_STUCK_RECOVERY_EN' register bit and resume the normal I2C transfers. ■ If an SDA line is not recovered, then the master auto clears the SDA_STUCK_RECOVERY_EN register bit and asserts the SDA_STUCK_NOT_RECOVERED (IC_STATUS[12]) status bit to indicate the SDA is not recovered after sending 9 SCL clocks which intamate the user for system reset. ■ If SCL line is stuck at low for IC_SCL_STUCK_LOW_TIMEOUT period of ic_clk, DW_apb_i2c Master will generate an SCL_STUCK_AT_LOW (IC_INTR_RAW_STATUS[14]) interrupt to intamate the user for system reset..
Has SCL Stuck Timeout value of?	<p>Parameter Name: IC_SCL_STUCK_TIMEOUT_DEFAULT Legal Values: 0x00000000 to 0xFFFFFFFF Default Value: 0xFFFFFFFF</p> <p>Dependencies: IC_BUS_CLEAR_FEATURE=1</p> <p>Description: Default value of the IC_SCL_STUCK_LOW_TIMEOUT Register</p>
Has SDA Stuck Timeout value of?	<p>Parameter Name: IC_SDA_STUCK_TIMEOUT_DEFAULT Legal Values: 0x00000000 to 0xFFFFFFFF Default Value: 0xFFFFFFFF</p> <p>Dependencies: IC_BUS_CLEAR_FEATURE=1</p> <p>Description: Default value of the IC_SDA_STUCK_LOW_TIMEOUT Register</p>

Table 4-1 Top-Level Parameters (Continued)

coreConsultant Field Label	Parameter Definition
Enable DEVICE ID Feature?	<p>Parameter Name: IC_DEVICE_ID</p> <p>Legal Values: Unchecked (0), Checked (1)</p> <p>Default Value: Unchecked (0)</p> <p>Dependencies: This Parameter is not applicable when Ultra-Fast Mode (IC_ULTRA_FAST_MODE=1) is enabled.</p> <p>Description: If this parameter is enabled, the DW_apb_i2c Slave includes a 24-bit IC_DEVICE_ID Register to store the value of Device ID and transmits whenever master is requested.</p> <p>The Master mode includes a DEVICE_ID bit 13 in IC_TAR register to initiate the Device ID read for a particular slave address mentioned in IC_TAR[6:0] register.</p>
Has I2C slave DEVICE ID value of?	<p>Parameter Name: IC_DEVICE_ID_VALUE</p> <p>Legal Values: 0x000000 to 0xFFFFFFF</p> <p>Dependencies: This Parameter is enabled if IC_DEVICE_ID=1</p> <p>Default Value: 0x000000</p> <p>Dependencies: IC_DEVICE_ID=1</p> <p>Description: Device ID Value of the I2C Slave (24 bit, MSB is transferred first on the Device ID read from the master).</p>
I2C 6.0 Parameters	
Enable Ultra-Fast mode?	<p>Parameter Name: IC_ULTRA_FAST_MODE</p> <p>Legal Values: Unchecked (0) or Checked (1)</p> <p>Dependencies: DWC-APB-Advanced-Source License Required</p> <p>Default Value: Unchecked (0)</p> <p>Description: Controls whether DW_apb_i2c supports Ultra-Fast speed mode or not.</p> <p>If this Parameter is enabled, the Master:</p> <ul style="list-style-type: none"> ■ Disables the Arbitration, clock synchronization features, ■ Supports only write Transfers, ■ Does not check the validity of ACK/NACK for each byte, <p>The Slave:</p> <ul style="list-style-type: none"> ■ Supports only Write transfers, ■ Disables the logic to generate ACK/NACK after the end of each byte, ■ Disables the logic to stretch the clock if RX-FIFO is full.

Table 4-1 Top-Level Parameters (Continued)

coreConsultant Field Label	Parameter Definition
Ultra-Fast speed SCL high count is?	<p>Parameter Name: IC_UFM_SCL_HIGH_COUNT Legal Value: Hex value in range 0x0003 to 0xffff Dependencies: This parameter is active when the IC_USE_COUNTS and IC_ULTRA_FAST_MODE parameters are checked (1); otherwise, this value is automatically calculated using the IC_CLK_PERIOD parameter. Default Value: 0x5 (5 based on 100 MHz ic_clk) Description: Reset value of Ultra-Fast Speed I2C Clock SCL High Count register (IC_UFM_SCL_HCNT). The value must be calculated based on the I2C data rate desired and I2C clock frequency.</p>
Ultra-Fast speed SCL Low count is?	<p>Parameter Name: IC_UFM_SCL_LOW_COUNT Legal Value: Hex value in range 0x0005 to 0xffff Dependencies: This parameter is active when the IC_USE_COUNTS and IC_ULTRA_FAST_MODE parameters are checked (1); otherwise, this value is automatically calculated using the IC_CLK_PERIOD parameter. Default Value: 0x5 (5 based on 100 MHz ic_clk) Description: Reset value of Ultra-Fast Speed I2C Clock SCL Low Count register (IC_UFM_SCL_LCNT). The value must be calculated based on the I2C data rate desired and I2C clock frequency.</p>
Maximum length (in ic_clk cycles) of suppressed spikes in Ultra-Fast mode	<p>Parameter Name: IC_DEFAULT_UFM_SPKLEN Legal Value: Hex value in range 0x01 to 0xFF Dependencies: Included only if IC_ULTRA_FAST_MODE parameter is set to 1. Initial value automatically calculated using IC_CLK_PERIOD. Default Value: Max(1,ceiling(10/IC_CLOCK_PERIOD)) Description: Reset value of maximum suppressed spike length register in Ultra-Fast Mode (IC_UFM_SPKLEN register). Spike length is expressed in ic_clk cycles, and this value is calculated based on the value of IC_CLOCK_PERIOD</p>
Has Ultra Fast mode tBuf count Value of ?	<p>Parameter Name: IC_UFM_TBUF_CNT_DEFAULT Legal Value: Hex value in range 0x0000 to 0xFFFF Dependencies: This parameter is active when the IC_USE_COUNTS and IC_ULTRA_FAST_MODE parameters are checked (1); otherwise, this value is automatically calculated using the IC_CLK_PERIOD parameter Default Value: 0x0008 Description: Default value of the IC_UFM_TBUF_CNT Register.</p>

Table 4-1 Top-Level Parameters (Continued)

coreConsultant Field Label	Parameter Definition
SMBus Parameters	
Enable SMBus mode?	<p>Parameter Name: IC_SMBUS</p> <p>Legal Values: Unchecked (0) or Checked (1)</p> <p>Dependencies: DWC-APB-Advanced-Source License required.</p> <p>Default Value: 0x0</p> <p>Description: Controls whether DW_apb_i2c Master/Slave supports SMBus mode. If checked, the DW_apb_i2c includes the SMBus mode-related registers, real-time checks, timeout interrupts, and SMBus optional signals.</p> <p>NOTE: If this parameter is selected (1), then the user can set the parameter IC_MAX_SPEED_MODE to Standard mode(1) or Fast Mode/Fast Mode Plus (2).</p>
Has SMBus clock low Master extend default Timeout value of?	<p>Parameter Name: IC_SMBUS_CLK_LOW_MEXT_DEFAULT</p> <p>Legal Values: 0x00000000 to 0xFFFFFFFF</p> <p>Dependencies: IC_SMBUS=1</p> <p>Default Value: 0xFFFFFFFF</p> <p>Description: Specifies default value of the IC_SMBUS_CLK_LOW_MEXT register.</p>
Has SMBus clock low Slave extend default Timeout value of?	<p>Parameter Name: IC_SMBUS_CLK_LOW_SEXT_DEFAULT</p> <p>Legal Values: 0x00000000 to 0xFFFFFFFF</p> <p>Dependencies: IC_SMBUS=1</p> <p>Default Value: 0xFFFFFFFF</p> <p>Description: Specifies default value of the IC_SMBUS_CLK_LOW_SEXT register.</p>
Has SMBus Thigh;Max Idle count Value of?	<p>Parameter Name: IC_SMBUS_RST_IDLE_CNT_DEFAULT</p> <p>Legal Values: 0x0000 to 0xFFFF</p> <p>Dependencies: IC_SMBUS=1</p> <p>Default Value: 0xFFFF</p> <p>Description: Specifies default value of the IC_SMBUS_THIGH_MAX_IDLE_COUNT register.</p>
Include Optional Slave Address Register?	<p>Parameter Name: IC_OPTIONAL_SAR</p> <p>Legal Values: Unchecked (0), Checked (1)</p> <p>Dependencies: Enabled only if IC_SMBUS=1.</p> <p>Default Value: Unchecked (0),</p> <p>Description: Controls whether to include Optional Slave Address Register in SMBus Mode.</p>

Table 4-1 Top-Level Parameters (Continued)

coreConsultant Field Label	Parameter Definition
Has I2C Default Optional Slave address of?	<p>Parameter Name: IC_OPTIONAL_SAR_DEFAULT Legal Values: 0x0 to 0x7f Default Value: Unchecked (0) Dependencies: Enabled only if IC_OPTIONAL_SAR=1. Description: Controls whether to include Optional Slave Address Register in SMBus Mode.</p> <p>A user is not allowed to assign any reserved addresses. The reserved address are as follows:</p> <p>0x00 0x01 0x02 0x03 0x04 0x05 0x06 0x07 0x78 0x79 0x7a 0x7b 0x7c 0x7d 0x7e 0x7f</p>
Enable SMBUS Optional Signals?	<p>Parameter Name: IC_SMBUS_SUSPEND_ALERT Legal Values: Unchecked (0), Checked (1) Default Value: Unchecked (0), Dependencies: Enabled only if IC_SMBUS=1. Description: Controls whether DW_apb_i2c includes Optional SMBus Suspend and Alert signals on the interface.</p>
Enable Address Resolution Protocol?	<p>Parameter Name: IC_SMBUS_ARP Legal Values: Unchecked (0), Checked (1) Default Value: Unchecked (0) Dependencies: Enabled only if IC_SMBUS=1. Description: Controls whether DW_apb_i2c includes logic to detect and respond ARP commands in Slave mode. It also includes logic to generate/validate the PEC byte at the end of the transfer in Slave mode only.</p>
Has SMBUS Unique device identifier (MSB 96 bits) value of?	<p>Parameter Name: IC_SMBUS_UDID_MSB Legal Values: 0 to 2^96 -1 Default Value: 0, Dependencies: Enabled only if IC_SMBUS_ARP=1. Description: Stores the Static Unique Device Identifier used for Dynamic Address Resolution process in SMBus ARP Mode (Upper 96bits of UDID).</p>
Has Default SMBus Unique device identifier (LSB 32 bits) value of?	<p>Parameter Name: IC_SMBUS_UDID_LSB_DEFAULT Legal Values: 0 to 2^32 -1 Default Value: 0, Dependencies: Enabled only if IC_SMBUS_ARP=1. Description: Specifies default value of the IC_SMBUS_UDID_LSB register used for Dynamic Address Resolution process in SMBus ARP mode (Lower 32bits of UDID).</p>
Has Default Persistent Slave Address register bit Value of?	<p>Parameter Name: IC_PERSISTANT_SLV_ADDR_DEFAULT Legal Values: Unchecked (0), Checked (1) Default Value: Unchecked (0), Dependencies: Enabled only if IC_SMBUS_ARP=1. Description: Default value of the Persistent Slave Address register bit in IC_CON register.</p>

Table 4-2 includes parameters that are derived from the user selected parameters in coreConsultant.

Table 4-2 Derived Parameters

Parameter	Legal Range	Description
TX_ABW	1 to 8 Default: 3	Transmit data width of FIFO (for writes).
RX_ABW	1 to 8 Default: 3	Receive data width of FIFO (for reads)

These constants in the table are derived using the following equation:

$$X = IC_TX_BUFFER_DEPTH$$

$\log_2(IC_TX_BUFFER_DEPTH)$ rounded up to the nearest integer

5

Signal Descriptions

This chapter details all possible I/O signals in the core. For configurable IP titles, your actual configuration might not contain all of these signals.

Inputs are on the left of the signal diagrams; outputs are on the right.

Attention: For configurable IP titles, do not use this document to determine the exact I/O footprint of the core. It is for reference purposes only.

When you configure the core in coreConsultant, you must access the I/O signals for your actual configuration at workspace/report/IO.html or workspace/report/IO.xml after you have completed the report creation activity. That report comes from the exact same source as this chapter but removes all the I/O signals that are not in your actual configuration. This does not apply to non-configurable IP titles. In addition, all parameter expressions are evaluated to actual values. Therefore, the widths might change depending on your actual configuration.

Some expressions might refer to TCL functions or procedures (sometimes identified as <functionof>) that coreConsultant uses to make calculations. The exact formula used by these TCL functions is not provided in this chapter. However, when you configure the core in coreConsultant, all TCL functions and parameters are evaluated completely; and the resulting values are displayed where appropriate in the coreConsultant GUI reports.

The I/O signals are grouped as follows:

- Interrupts on [page 127](#)
- I2C Interface (Master/Slave) on [page 142](#)
- APB Slave Interface on [page 145](#)
- DMA Interface on [page 147](#)
- SMBus Interface on [page 149](#)
- I2C Debug on [page 150](#)

5.1 Interrupts Signals

- ic_intr
- ic_mst_on_hold_intr
- ic_start_det_intr
- ic_stop_det_intr
- ic_restart_det_intr
- ic_scl_stuck_at_low_intr
- ic_smbus_clk_sext_intr
- ic_smbus_clk_mext_intr
- ic_smbus_quick_cmd_det_intr
- ic_smbus_arp_prepare_intr
- ic_smbus_arp_reset_intr
- ic_smbus_arp_get_udid_intr
- ic_smbus_arp_assign_address_intr
- ic_smbus_host_notify_intr
- ic_smbus_slv_rx_pec_nack_intr
- ic_smbalert_det_intr
- ic_smbsus_det_intr
- ic_activity_intr
- ic_rx_done_intr
- ic_tx_abrt_intr
- ic_rd_req_intr
- ic_tx_empty_intr
- ic_tx_over_intr
- ic_rx_full_intr
- ic_rx_over_intr
- ic_rx_under_intr
- ic_gen_call_intr
- ic_intr_n
- ic_mst_on_hold_intr_n
- ic_start_det_intr_n
- ic_stop_det_intr_n
- ic_restart_det_intr_n
- ic_scl_stuck_at_low_intr_n
- ic_smbus_clk_sext_intr_n
- ic_smbus_clk_mext_intr_n
- ic_smbus_quick_cmd_det_intr_n
- ic_smbus_arp_prepare_intr_n
- ic_smbus_arp_reset_intr_n
- ic_smbus_arp_get_udid_intr_n
- ic_smbus_arp_assign_address_intr_n
- ic_smbus_host_notify_intr_n
- ic_smbus_slv_rx_pec_nack_intr_n
- ic_smbalert_det_intr_n
- ic_smbsus_det_intr_n
- ic_activity_intr_n
- ic_rx_done_intr_n
- ic_tx_abrt_intr_n
- ic_rd_req_intr_n
- ic_tx_empty_intr_n
- ic_tx_over_intr_n
- ic_rx_full_intr_n
- ic_rx_over_intr_n
- ic_rx_under_intr_n
- ic_gen_call_intr_n

Table 5-1 Interrupts Signals

Port Name	I/O	Description
ic_intr	O	<p>Optional. Combined active high interrupt. This signal is included on the interface when the configuration parameter IC_INTR_IO is checked (1) to indicate that only one interrupt line appears on the I/O (as opposed to individual interrupt signals).</p> <p>Exists: (IC_INTR_IO==1) && (IC_INTR_POL==1)</p> <p>Active State: High. Polarity is set by the configuration parameter IC_INTR_POL (checked(1) = active high).</p> <p>Synchronous to: pclk</p> <p>Registered: No</p>
ic_mst_on_hold_intr	O	<p>Optional. Master on hold I2C active high interrupt. This signal is included on the interface when the configuration parameters I2C_DYNAMIC_TAR_UPDATE and IC_EMPTYFIFO_HOLD_MASTER_EN are checked (1) and the configuration parameter IC_INTR_IO is unchecked (0), indicating that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==1) && (I2C_DYNAMIC_TAR_UPDATE==1 && IC_EMPTYFIFO_HOLD_MASTER_EN==1)</p> <p>Active State: High. Polarity is set by the configuration parameter IC_INTR_POL (checked(1) = active high).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>
ic_start_det_intr	O	<p>Optional. Start condition detect on I2C active high interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==1)</p> <p>Active State: High. Polarity is set by the configuration parameter IC_INTR_POL (checked(1) = active high).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>
ic_stop_det_intr	O	<p>Optional. Stop condition detect on I2C active high interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==1)</p> <p>Active State: High. Polarity is set by the configuration parameter IC_INTR_POL (checked(1) = active high).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>

Table 5-1 Interrupts Signals (Continued)

Port Name	I/O	Description
ic_restart_det_intr	O	<p>Optional. Restart condition detect on I2C active high interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==1) && (IC_SLV_RESTART_DET_EN==1)</p> <p>Active State: High. Polarity is set by the configuration parameter IC_INTR_POL (checked(1) = active high).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>
ic_scl_stuck_at_low_intr	O	<p>Optional. SCL Stuck condition detect on I2C active high interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==1) && (IC_BUS_CLEAR_FEATURE==1)</p> <p>Active State: High. Polarity is set by the configuration parameter IC_INTR_POL (checked = active high).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>
ic_smbus_clk_sext_intr	O	<p>Optional. SMBUS Slave clock extend timeout detect active high interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==1) && (IC_SMBUS==1)</p> <p>Active State: High. Polarity is set by the configuration parameter IC_INTR_POL (checked = active high).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>
ic_smbus_clk_mext_intr	O	<p>Optional. SMBUS Master clock extend timeout detect active high interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==1) && (IC_SMBUS==1)</p> <p>Active State: High. Polarity is set by the configuration parameter IC_INTR_POL (checked = active high).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>

Table 5-1 Interrupts Signals (Continued)

Port Name	I/O	Description
ic_smbus_quick_cmd_det_intr	O	<p>Optional. SMBUS Quick Command detect active high interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==1) && (IC_SMBUS==1)</p> <p>Active State: High. Polarity is set by the configuration parameter IC_INTR_POL (checked = active high).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>
ic_smbus_arp_prepare_intr	O	<p>Optional. SMBUS ARP Prepare Command detect active high interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==1) && (IC_SMBUS_ARP==1)</p> <p>Active State: High. Polarity is set by the configuration parameter IC_INTR_POL (checked = active high).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>
ic_smbus_arp_reset_intr	O	<p>Optional. SMBUS ARP Reset Command detect active high interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==1) && (IC_SMBUS_ARP==1)</p> <p>Active State: High. Polarity is set by the configuration parameter IC_INTR_POL (checked = active high).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>
ic_smbus_arp_get_udid_intr	O	<p>Optional. SMBUS ARP Get UDID Command detect active high interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==1) && (IC_SMBUS_ARP==1)</p> <p>Active State: High. Polarity is set by the configuration parameter IC_INTR_POL (checked = active high).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>

Table 5-1 Interrupts Signals (Continued)

Port Name	I/O	Description
ic_smbus_arp_assign_address_intr	O	<p>Optional. SMBUS ARP Assign Command detect active high interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==1) && (IC_SMBUS_ARP==1)</p> <p>Active State: High. Polarity is set by the configuration parameter IC_INTR_POL (checked = active high).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>
ic_smbus_host_notify_intr	O	<p>Optional. SMBUS ARP Host Notify Command detect active high interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==1) && (IC_SMBUS==1)</p> <p>Active State: High. Polarity is set by the configuration parameter IC_INTR_POL (checked = active high).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>
ic_smbus_slv_rx_pec_nack_intr	O	<p>Optional. SMBUS ARP Slave Received incorrect PEC Byte and generated Nack active high interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==1) && (IC_SMBUS_ARP==1)</p> <p>Active State: High. Polarity is set by the configuration parameter IC_INTR_POL (checked = active high).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>
ic_smbalert_det_intr	O	<p>Optional. SMBUS Alert detect active high interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==1) && (IC_SMBUS_SUSPEND_ALERT==1)</p> <p>Active State: High. Polarity is set by the configuration parameter IC_INTR_POL (checked = active high).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>

Table 5-1 Interrupts Signals (Continued)

Port Name	I/O	Description
ic_smbsus_det_intr	O	<p>Optional. SMBUS Suspend detect active high interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==1) && (IC_SMBUS_SUSPEND_ALERT==1)</p> <p>Active State: High. Polarity is set by the configuration parameter IC_INTR_POL (checked = active high).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>
ic_activity_intr	O	<p>Optional. I2C activity active high interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==1)</p> <p>Active State: High. Polarity is set by the configuration parameter IC_INTR_POL (checked(1) = active high).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>
ic_rx_done_intr	O	<p>Optional. Receive done active high interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==1) && (IC_ULTRA_FAST_MODE==0)</p> <p>Active State: High. Polarity is set by the configuration parameter IC_INTR_POL (checked(1) = active high).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>
ic_tx_abrt_intr	O	<p>Optional. Transmit abort active high interrupt.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==1)</p> <p>Active State: High. Polarity is set by the configuration parameter IC_INTR_POL (checked(1) = active high).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>

Table 5-1 Interrupts Signals (Continued)

Port Name	I/O	Description
ic_rd_req_intr	O	<p>Optional. Slave read request interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==1) && (IC_ULTRA_FAST_MODE==0)</p> <p>Active State: High. Polarity is set by the configuration parameter IC_INTR_POL (checked(1) = active high).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>
ic_tx_empty_intr	O	<p>Optional. Transmit buffer empty active high interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>When bit 0 of the IC_ENABLE register is 0, the TX FIFO is flushed and held in reset, where it looks like it has no data within it. The ic_tx_empty_intr bit is raised when bit 0 of the IC_ENABLE register is 0, provided there is activity in the master or slave state machines. When there is no longer activity, then this interrupt bit is masked with ic_en.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==1)</p> <p>Active State: High. Polarity is set by the configuration parameter IC_INTR_POL (checked(1) = active high).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>
ic_tx_over_intr	O	<p>Optional. Transmit buffer overflow active high interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>When the module is disabled, this interrupt keeps its level until the master or slave state machines go into idle and bit 0 of the IC_ENABLE register is 0. When ic_en goes to 0, this interrupt is cleared.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==1)</p> <p>Active State: High. Polarity is set by the configuration parameter IC_INTR_POL (checked(1) = active high).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>

Table 5-1 Interrupts Signals (Continued)

Port Name	I/O	Description
ic_rx_full_intr	O	<p>Optional. Receive buffer full active high interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>When bit 0 of the IC_ENABLE register is 0, the RX FIFO is flushed and held in reset the RX FIFO is not full so this ic_rx_full_intr bit is cleared once the ic_enable bit is programmed with a 0, regardless of the activity that continues.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==1) Active State: High. Polarity is set by the configuration parameter IC_INTR_POL (checked(1) = active high). Synchronous to: pclk Registered: Yes</p>
ic_rx_over_intr	O	<p>Optional. Receive buffer overflow active high interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>When the module is disabled, this interrupt keeps its level until the master or slave state machines go into idle and bit 0 of the IC_ENABLE register is 0. When ic_en goes to 0, this interrupt is cleared.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==1) Active State: High. Polarity is set by the configuration parameter IC_INTR_POL (checked(1) = active high). Synchronous to: pclk Registered: Yes</p>
ic_rx_under_intr	O	<p>Optional. Receive buffer underflow active high interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>When the module is disabled, this interrupt keeps its level until the master or slave state machines go into idle and bit 0 of the IC_ENABLE register is 0. When ic_en goes to 0, this interrupt is cleared.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==1) Active State: High. Polarity is set by the configuration parameter IC_INTR_POL (checked(1) = active high). Synchronous to: pclk Registered: Yes</p>

Table 5-1 Interrupts Signals (Continued)

Port Name	I/O	Description
ic_gen_call_intr	O	<p>Optional. General Call received active high interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==1)</p> <p>Active State: High. Polarity is set by the configuration parameter IC_INTR_POL (checked(1) = active high).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>
ic_intr_n	O	<p>Optional. Combined active low interrupt. This signal is included on the interface when the configuration parameter IC_INTR_IO is unchecked (0) to indicate that only one interrupt line appears on the I/O (as opposed to individual interrupt signals).</p> <p>Exists: (IC_INTR_IO==1) && (IC_INTR_POL==0)</p> <p>Active State: Low. Polarity is set by the configuration parameter IC_INTR_POL (unchecked = active low).</p> <p>Synchronous to: pclk</p> <p>Registered: No</p>
ic_mst_on_hold_intr_n	O	<p>Optional. Master on hold I2C active low interrupt. This signal is included on the interface when the configuration parameters I2C_DYNAMIC_TAR_UPDATE and IC_EMPTYFIFO_HOLD_MASTER_EN are checked (1) and the configuration parameter IC_INTR_IO is unchecked (0), indicating that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==0) && (I2C_DYNAMIC_TAR_UPDATE==1 && IC_EMPTYFIFO_HOLD_MASTER_EN==1)</p> <p>Active State: Low. Polarity is set by the configuration parameter IC_INTR_POL (unchecked = active low).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>
ic_start_det_intr_n	O	<p>Optional. Start condition detect on I2C active low interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==0)</p> <p>Active State: Low. Polarity is set by the configuration parameter IC_INTR_POL (unchecked(0) = active low).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>

Table 5-1 Interrupts Signals (Continued)

Port Name	I/O	Description
ic_stop_det_intr_n	O	<p>Optional. Stop condition detect on I2C active low interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==0)</p> <p>Active State: Low. Polarity is set by the configuration parameter IC_INTR_POL (unchecked(0) = active low).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>
ic_restart_det_intr_n	O	<p>Optional. Restart condition detect on I2C active low interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==0) && (IC_SLV_RESTART_DET_EN==1)</p> <p>Active State: Low. Polarity is set by the configuration parameter IC_INTR_POL (unchecked(0) = active low).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>
ic_scl_stuck_at_low_intr_n	O	<p>Optional. SCL Stuck condition detect on I2C active low interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==0) && (IC_BUS_CLEAR_FEATURE==1)</p> <p>Active State: Low. Polarity is set by the configuration parameter IC_INTR_POL (unchecked = active low).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>
ic_smbus_clk_sext_intr_n	O	<p>Optional. SMBUS Slave clock extend timeout detect active low interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==0) && (IC_SMBUS==1)</p> <p>Active State: Low. Polarity is set by the configuration parameter IC_INTR_POL (unchecked = active low).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>

Table 5-1 Interrupts Signals (Continued)

Port Name	I/O	Description
ic_smbus_clk_mext_intr_n	O	<p>Optional. SMBUS Master clock extend timeout detect active low interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==0) && (IC_SMBUS==1)</p> <p>Active State: Low. Polarity is set by the configuration parameter IC_INTR_POL (unchecked = active low).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>
ic_smbus_quick_cmd_det_intr_n	O	<p>Optional. SMBUS ARP Quick Command detect active low interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==0) && (IC_SMBUS==1)</p> <p>Active State: Low. Polarity is set by the configuration parameter IC_INTR_POL (unchecked = active low).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>
ic_smbus_arp_prepare_intr_n	O	<p>Optional. SMBUS ARP Prepare Command detect active low interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==0) && (IC_SMBUS_ARP==1)</p> <p>Active State: Low. Polarity is set by the configuration parameter IC_INTR_POL (unchecked = active low).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>
ic_smbus_arp_reset_intr_n	O	<p>Optional. SMBUS ARP Reset Command detect active low interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==0) && (IC_SMBUS_ARP==1)</p> <p>Active State: Low. Polarity is set by the configuration parameter IC_INTR_POL (unchecked = active low).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>

Table 5-1 Interrupts Signals (Continued)

Port Name	I/O	Description
ic_smbus_arp_get_udid_intr_n	O	<p>Optional. SMBUS ARP Get UDID Command detect active low interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==0) && (IC_SMBUS_ARP==1)</p> <p>Active State: Low. Polarity is set by the configuration parameter IC_INTR_POL (unchecked = active low).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>
ic_smbus_arp_assign_address_intr_n	O	<p>Optional. SMBUS ARP Assign Command detect active low interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==0) && (IC_SMBUS_ARP==1)</p> <p>Active State: Low. Polarity is set by the configuration parameter IC_INTR_POL (unchecked = active low).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>
ic_smbus_host_notify_intr_n	O	<p>Optional. SMBUS ARP Host Notify Command detect active low interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==0) && (IC_SMBUS==1)</p> <p>Active State: Low. Polarity is set by the configuration parameter IC_INTR_POL (unchecked = active low).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>
ic_smbus_slv_rx_pec_nack_intr_n	O	<p>Optional. SMBUS ARP Slave Received incorrect PEC Byte and generated Nack active low interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==0) && (IC_SMBUS_ARP==1)</p> <p>Active State: Low. Polarity is set by the configuration parameter IC_INTR_POL (unchecked = active low).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>

Table 5-1 Interrupts Signals (Continued)

Port Name	I/O	Description
ic_smbalert_det_intr_n	O	<p>Optional. SMBUS Alert detect active low interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==0) && (IC_SMBUS_SUSPEND_ALERT==1)</p> <p>Active State: Low. Polarity is set by the configuration parameter IC_INTR_POL (unchecked = active low).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>
ic_smbsus_det_intr_n	O	<p>Optional. SMBUS Suspend detect active low interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==0) && (IC_SMBUS_SUSPEND_ALERT==1)</p> <p>Active State: Low. Polarity is set by the configuration parameter IC_INTR_POL (unchecked = active low).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>
ic_activity_intr_n	O	<p>Optional. I2C activity active low interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==0)</p> <p>Active State: Low. Polarity is set by the configuration parameter IC_INTR_POL (unchecked(0) = active low).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>
ic_rx_done_intr_n	O	<p>Optional. Receive done active low interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==0) && (IC_ULTRA_FAST_MODE==0)</p> <p>Active State: Low. Polarity is set by the configuration parameter IC_INTR_POL (unchecked(0) = active low).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>

Table 5-1 Interrupts Signals (Continued)

Port Name	I/O	Description
ic_tx_abrt_intr_n	O	<p>Optional. Transmit abort active low interrupt.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==0)</p> <p>Active State: Low. Polarity is set by the configuration parameter IC_INTR_POL (unchecked(0) = active low).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>
ic_rd_req_intr_n	O	<p>Optional. Slave read request active low interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==0) && (IC_ULTRA_FAST_MODE==0)</p> <p>Active State: Low. Polarity is set by the configuration parameter IC_INTR_POL (unchecked(0) = active low).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>
ic_tx_empty_intr_n	O	<p>Optional. Transmit buffer empty active low interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>When bit 0 of the IC_ENABLE register is 0, the TX FIFO is flushed and held in reset, where it looks like it has no data within it. The ic_tx_empty_intr_n bit is raised when bit 0 of the IC_ENABLE register is 0, provided there is activity in the master or slave state machines. When there is no longer activity, then this interrupt bit is masked with ic_en.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==0)</p> <p>Active State: Low. Polarity is set by the configuration parameter IC_INTR_POL (unchecked(0) = active low).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>
ic_tx_over_intr_n	O	<p>Optional. Transmit buffer overflow active low interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>When the module is disabled, this interrupt keeps its level until the master or slave state machines go into idle and bit 0 of the IC_ENABLE register is 0. When ic_en goes to 0, this interrupt is cleared.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==0)</p> <p>Active State: Low. Polarity is set by the configuration parameter IC_INTR_POL (unchecked(0) = active low).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>

Table 5-1 Interrupts Signals (Continued)

Port Name	I/O	Description
ic_rx_full_intr_n	O	<p>Optional. Receive buffer full active low interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>When bit 0 of the IC_ENABLE register is 0, the RX FIFO is flushed and held in reset the RX FIFO is not full so this ic_rx_full_intr_n bit is cleared once the ic_enable bit is programmed with a 0, regardless of the activity that continues.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==0) Active State: Low. Polarity is set by the configuration parameter IC_INTR_POL (unchecked(0) = active low). Synchronous to: pclk Registered: Yes</p>
ic_rx_over_intr_n	O	<p>Optional. Receive buffer overflow active low interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>When the module is disabled, this interrupt keeps its level until the master or slave state machines go into idle and bit 0 of the IC_ENABLE register is 0. When ic_en goes to 0, this interrupt is cleared.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==0) Active State: Low. Polarity is set by the configuration parameter IC_INTR_POL (unchecked(0) = active low). Synchronous to: pclk Registered: Yes</p>
ic_rx_under_intr_n	O	<p>Optional. Receive buffer underflow active low interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>When the module is disabled, this interrupt keeps its level until the master or slave state machines go into idle and bit 0 of the IC_ENABLE register is 0. When ic_en goes to 0, this interrupt is cleared.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==0) Active State: Low. Polarity is set by the configuration parameter IC_INTR_POL (unchecked(0) = active low). Synchronous to: pclk Registered: Yes</p>

Table 5-1 Interrupts Signals (Continued)

Port Name	I/O	Description
ic_gen_call_intr_n	O	<p>Optional. General Call received active low interrupt. This signal is included on the interface when the configuration IC_INTR_IO parameter is unchecked (0), which indicates that individual interrupt lines appear on the I/O.</p> <p>Exists: (IC_INTR_IO==0) && (IC_INTR_POL==0)</p> <p>Active State: Low. Polarity is set by the configuration parameter IC_INTR_POL (unchecked(0) = active low).</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>

5.2 I2C Interface (Master/Slave) Signals

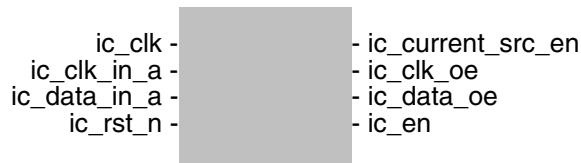


Table 5-2 I2C Interface (Master/Slave) Signals

Port Name	I/O	Description
ic_current_src_en	O	<p>Optional. Current source pull-up. Controls the polarity of the current source pull-up on the SCLH. This pull-up is used to shorten the rise time on SCLH by activating an user-supplied external current source pull-up circuit. It is disabled after a RESTART condition and after each A/A bit when acting as the active master.</p> <p>This signal enables other devices to delay the serial transfer by stretching the LOW period of the SCLH signal. The active master re-enables its current source pull-up circuit again when all devices have released and the SCLH signal reaches high level, therefore, shortening the last part of the SCLH signal's rise time.</p> <p>Exists: (IC_MAX_SPEED_MODE==3) Active State: High Synchronous to: ic_clk Registered: Yes</p>
ic_clk	I	<p>Peripheral clock. DW_apb_i2c runs on this clock and is used to clock transfers in standard, fast, and high-speed mode.</p> <p>NOTE: ic_clk frequency must be greater than or equal to pclk frequency.</p> <p>Exists: Always Active State: N/A Synchronous to: The configuration parameter IC_CLK_TYPE indicates the relationship between pclk and ic_clk. It can be asynchronous (1) or identical (0). Registered: N/A</p>

Table 5-2 I2C Interface (Master/Slave) Signals (Continued)

Port Name	I/O	Description
ic_clk_in_a	I	<p>In (IC_ULTRA_FAST_MODE = 0) mode - Incoming I2C clock. This is the input SCL signal. Double-registered for metastability synchronization.</p> <p>NOTE: DW_apb_i2c provides filtering on the SDA (ic_data_in_a) and SCL (ic_clk_in_a) inputs, suppressing noise and signal spikes with durations less than one ic_clk period.</p> <p>In Ultra-Fast(IC_ULTRA_FAST_MODE = 1) mode - Incoming I2C clock. This is the input SCL signal. Double-registered for metastability synchronization.</p> <p>NOTE: DW_apb_i2c provides filtering on the SDA (ic_data_in_a) and SCL (ic_clk_in_a) inputs, suppressing noise and signal spikes with durations less than one ic_clk period. This signal is used as USCL input for slave device.</p> <p>Exists: Always</p> <p>Active State: High</p> <p>Synchronous to: This signal is asynchronous to ic_clk.</p> <p>Registered: Yes</p>
ic_data_in_a	I	<p>In (IC_ULTRA_FAST_MODE = 0) mode - Incoming I2C Data. It is the input SDA signal. Double-registered for metastability synchronization.</p> <p>NOTE: DW_apb_i2c provides filtering on the SDA (ic_data_in_a) and SCL (ic_clk_in_a) inputs, suppressing noise and signal spikes with durations less than one ic_clk period.</p> <p>In Ultra-Fast(IC_ULTRA_FAST_MODE = 1) mode - Incoming I2C Data. It is the input SDA signal. Double-registered for metastability synchronization.</p> <p>NOTE: DW_apb_i2c provides filtering on the SDA (ic_data_in_a) and SCL (ic_clk_in_a) inputs, suppressing noise and signal spikes with durations less than one ic_clk period. This signal is used as USDA input for slave device.</p> <p>Exists: Always</p> <p>Active State: High</p> <p>Synchronous to: This signal is asynchronous to ic_clk.</p> <p>Registered: Yes</p>
ic_rst_n	I	<p>I2C reset. Used to reset flip-flops that are clocked by the ic_clk clock.</p> <p>NOTE: This signal does not reset DW_apb_i2c control, configuration, and status registers.</p> <p>Exists: Always</p> <p>Active State: Low</p> <p>Synchronous to: The signal is asserted asynchronously, but is deasserted synchronously after the rising edge of ic_clk. The synchronization must be provided external to this component.</p> <p>Registered: N/A</p>

Table 5-2 I2C Interface (Master/Slave) Signals (Continued)

Port Name	I/O	Description
ic_clk_oe	O	<p>In (IC_ULTRA_FAST_MODE = 0) mode - Outgoing I2C clock. Open drain synchronous with ic_clk.</p> <p>In Ultra-Fast(IC_ULTRA_FAST_MODE = 1) mode - Outgoing I2C clock, inverted. This signal is used as USCL out from master device.</p> <p>Exists: Always</p> <p>Active State: High</p> <p>Synchronous to: ic_clk</p> <p>Registered: Yes</p>
ic_data_oe	O	<p>In (IC_ULTRA_FAST_MODE = 0) mode - Outgoing I2C Data. Open Drain Synchronous to ic_clk.</p> <p>In Ultra-Fast(IC_ULTRA_FAST_MODE = 1) mode - Outgoing I2C Data, inverted. This signal is used as USDA out from master device.</p> <p>Exists: Always</p> <p>Active State: High</p> <p>Synchronous to: ic_clk</p> <p>Registered: Yes</p>
ic_en	O	<p>I2C interface enable. Indicates whether DW_apb_i2c is enabled; this signal is set to 0 when IC_ENABLE[0] is set to 0 (disabled). Because DW_apb_i2c always finishes its current transfer before turning off ic_en, this signal may be used by a clock generator to control whether the DW_apb_i2c ic_clk is active or inactive.</p> <p>Exists: Always</p> <p>Active State: Low</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>

5.3 APB Slave Interface Signals



Table 5-3 APB Slave Interface Signals

Port Name	I/O	Description
pclk	I	<p>APB clock for the bus interface unit. NOTE: ic_clk frequency must be greater than or equal to pclk frequency.</p> <p>Exists: Always Active State: N/A Synchronous to: The configuration parameter IC_CLK_TYPE indicates the relationship between pclk and ic_clk. It can be asynchronous (1) or identical (0). Registered: N/A</p>
presetn	I	<p>An APB interface domain reset.</p> <p>Exists: Always Active State: Low Synchronous to: The signal is asserted asynchronously, but is deasserted synchronously after the rising edge of pclk. The synchronization must be provided external to this component. Registered: N/A</p>
psel	I	<p>APB peripheral select that lasts for two pclk cycles. When asserted, indicates that the peripheral has been selected for a read/write operation.</p> <p>Exists: Always Active State: High Synchronous to: pclk Registered: No</p>
penable	I	<p>APB enable control. Asserted for a single pclk cycle and used for timing read/write operations.</p> <p>Exists: Always Active State: High Synchronous to: pclk Registered: No</p>

Table 5-3 APB Slave Interface Signals (Continued)

Port Name	I/O	Description
pwrite	I	<p>APB write control. When high, indicates a write access to the peripheral; when low, indicates a read access.</p> <p>Exists: Always Active State: N/A Synchronous to: pclk Registered: No</p>
paddr[IC_ADDR_SLICE_LHS:0]	I	<p>APB address bus. Uses lower 7 bits of the address bus for register decode.</p> <p>Exists: Always Active State: N/A Synchronous to: pclk Registered: No</p>
pwdata[(APB_DATA_WIDTH-1):0]	I	<p>APB write data bus. Driven by the bus master (DW_ahb to DW_apb bridge) during write cycles. Can be 8, 16, or 32 bits wide depending on APB_DATA_WIDTH parameter.</p> <p>Exists: Always Active State: N/A Synchronous to: pclk Registered: No</p>
prdata[(APB_DATA_WIDTH-1):0]	O	<p>APB readback data. Driven by the selected peripheral during read cycles. Can be 8, 16, or 32 bits wide depending on APB_DATA_WIDTH parameter.</p> <p>Exists: Always Active State: N/A Synchronous to: pclk Registered: Yes</p>

5.4 DMA Interface Signals

- dma_tx_ack -
 - dma_rx_ack -
 - dma_tx_req
 - dma_tx_single
 - dma_rx_req
 - dma_rx_single

Table 5-4 DMA Interface Signals

Port Name	I/O	Description
dma_tx_ack	I	<p>Optional. DMA Transmit Acknowledgement. Sent by the DMA Controller to acknowledge the end of each APB transfer burst to the transmit FIFO.</p> <p>Exists: (IC_HAS_DMA==1)</p> <p>Active State: High</p> <p>Synchronous to: pcclk</p> <p>Registered: No</p>
dma_tx_req	O	<p>Optional. Transmit FIFO DMA Request. Asserted when the transmit FIFO requires service from the DMA Controller; that is, the transmit FIFO is at or below the watermark level.</p> <p>0 not requesting 1 requesting</p> <p>Software must set up the DMA controller with the number of words to be transferred when a request is made. When using the DW_ahb_dmac, this value is programmed in the DEST_MSIZE field of the CTLx register.</p> <p>Exists: (IC_HAS_DMA==1)</p> <p>Active State: High</p> <p>Synchronous to: pcclk</p> <p>Registered: Yes</p>
dma_tx_single	O	<p>Optional. DMA Transmit FIFO Single Signal. This DMA status output informs the DMA Controller that there is at least one free entry in the transmit FIFO. This output does not request a DMA transfer.</p> <p>0: Transmit FIFO is full 1: Transmit FIFO is not full</p> <p>Exists: (IC_HAS_DMA==1)</p> <p>Active State: High</p> <p>Synchronous to: pcclk</p> <p>Registered: Yes</p>

Table 5-4 DMA Interface Signals (Continued)

Port Name	I/O	Description
dma_rx_ack	I	<p>Optional. DMA Receive Acknowledgement. Sent by the DMA controller to acknowledge the end of each APB transfer burst from the receive FIFO.</p> <p>Exists: (IC_HAS_DMA==1)</p> <p>Active State: High</p> <p>Synchronous to: pclk</p> <p>Registered: No</p>
dma_rx_req	O	<p>Optional. Receive FIFO DMA Request. Asserted when the receive FIFO requires service from the DMA Controller; that is, the receive FIFO is at or above the watermark level.</p> <p>0 not requesting 1 requesting</p> <p>Software must set up the DMA controller with the number of words to be transferred when a request is made. When using the DW_ahb_dmac, this value is programmed in the SRC_MSIZE field of the CTLx register.</p> <p>Exists: (IC_HAS_DMA==1)</p> <p>Active State: High</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>
dma_rx_single	O	<p>Optional. DMA Receive FIFO Single Signal. This DMA status output informs the DMA Controller that there is at least one valid data entry in the receive FIFO. This output does not request a DMA transfer.</p> <p>0: Receive FIFO is empty 1: Receive FIFO is not empty</p> <p>Exists: (IC_HAS_DMA==1)</p> <p>Active State: High</p> <p>Synchronous to: pclk</p> <p>Registered: Yes</p>

5.5 SMBus Interface Signals



Table 5-5 SMBus Interface Signals

Port Name	I/O	Description
ic_smbsus_in_n	I	<p>Incoming SMBus Suspend signal. This is the input SMBSUS signal. Double-registered for metastability synchronization.</p> <p>Exists: (IC_SMBUS_SUSPEND_ALERT==1)</p> <p>Active State: Low</p> <p>Synchronous to: This signal is asynchronous to pcclk</p> <p>Registered: Yes</p>
ic_smbalert_in_n	I	<p>Incoming SMBus Alert signal. This is the input SMBALERT signal. Double-registered for metastability synchronization.</p> <p>Exists: (IC_SMBUS_SUSPEND_ALERT==1)</p> <p>Active State: Low</p> <p>Synchronous to: This signal is asynchronous to pcclk</p> <p>Registered: Yes</p>
ic_smbsus_out_n	O	<p>Outgoing SMBus Suspend Signal. This signal is used to suspend the SMBus system, if DW_apb_i2c is used as SMBus Host.</p> <p>Exists: (IC_SMBUS_SUSPEND_ALERT==1)</p> <p>Active State: Low</p> <p>Synchronous to: pcclk</p> <p>Registered: Yes</p>
ic_smbalert_oe	O	<p>Outgoing SMBus Alert Signal. This signal is used to intimate the Host that slave wants to talk, if DW_apb_i2c is used as SMBus Slave.</p> <p>Exists: (IC_SMBUS_SUSPEND_ALERT==1)</p> <p>Active State: Low</p> <p>Synchronous to: pcclk</p> <p>Registered: Yes</p>

5.6 I2C Debug Signals

- debug_s_gen
 - debug_p_gen
 - debug_data
 - debug_addr
 - debug_rd
 - debug_wr
 - debug_hs
 - debug_master_act
 - debug_slave_act
 - debug_addr_10bit
 - debug_mst_cstate
 - debug_slv_cstate

Table 5-6 I2C Debug Signals

Port Name	I/O	Description
debug_s_gen	O	In the master mode of operation, this signal is set to 1 when DW_apb_i2c is driving a START condition on the bus. Exists: Always Active State: Low Synchronous to: ic_clk Registered: Yes
debug_p_gen	O	In the master mode of operation, this signal is set to 1 when DW_apb_i2c is driving a STOP condition on the bus. Exists: Always Active State: Low Synchronous to: ic_clk Registered: Yes
debug_data	O	In the master or slave mode of operation, this signal is set to 1 when a byte of data is actively being read or written by DW_apb_i2c. This bit remains 1 until the transaction has completed. Exists: Always Active State: High Synchronous to: N/A Registered: Yes
debug_addr	O	In the master or slave mode of operation, this signal is set to 1 when the addressing phase is active on the I2C bus. Exists: Always Active State: High Synchronous to: ic_clk Registered: Yes

Table 5-6 I2C Debug Signals (Continued)

Port Name	I/O	Description
debug_rd	O	<p>In the master mode of operation, this signal is set to 1 whenever the master is receiving data. This bit remains 1 until the transfer is complete or until the direction changes.</p> <p>Exists: Always Active State: High Synchronous to: ic_clk Registered: Yes</p>
debug_wr	O	<p>In the master mode of operation, this signal is set to 1 whenever the master is transmitting data. This bit remains 1 until the transfer is complete or the direction changes.</p> <p>Exists: Always Active State: High Synchronous to: ic_clk Registered: Yes</p>
debug_hs	O	<p>In the master mode of operation, this signal is set to 1 when DW_apb_i2c is performing high-speed mode transfers. This bit is set after the high-speed master code is transmitted and remains 1 until the master leaves high-speed mode.</p> <p>Exists: Always Active State: High Synchronous to: ic_clk Registered: Yes</p>
debug_master_act	O	<p>This bit is set to 1 when the master module is active.</p> <p>Exists: Always Active State: High Synchronous to: ic_clk Registered: Yes</p>
debug_slave_act	O	<p>This bit is set to 1 when the slave module is active.</p> <p>Exists: Always Active State: High Synchronous to: ic_clk Registered: Yes</p>
debug_addr_10bit	O	<p>In the Slave mode of operation, this signal is set if 10-bit addressing is enabled and if the slave has received a matching 10-bit address with respect to IC_SAR register.</p> <p>This signal is not applicable in Master Mode.</p> <p>Exists: Always Active State: High Synchronous to: ic_clk Registered: Yes</p>

Table 5-6 I2C Debug Signals (Continued)

Port Name	I/O	Description
debug_mst_cstate[4:0]	O	Master FSM state vector. Exists: Always Active State: N/A Synchronous to: ic_clk Registered: Yes
debug_slv_cstate[3:0]	O	Slave FSM state vector. Exists: Always Active State: N/A Synchronous to: ic_clk Registered: Yes

6

Registers

This section describes the programmable registers of the DW_apb_i2c.



Note There are references to both hardware parameters and software registers throughout this chapter. Parameters and many of the register bits are prefixed with an IC_*. However, the software register bits are distinguished in this chapter by italics. For instance, IC_MAX_SPEED_MODE is a hardware parameter and configured once using Synopsys coreConsultant, whereas the *IC_SLAVE_DISABLE* bit in the IC_CON register controls whether I2C has its slave disabled.

6.1 Register Memory Map



Note A read operation to an address location that contains unused bits results in a 0 value being returned on each of the unused bits.

Shipped with the DW_apb_i2c component is an address definition (memory map) C header file. This can be used when the DW_apb_i2c is programmed in a C environment.

[Table 6-1](#) provides the details of the DW_apb_i2c memory map. Reset values are affected by the configuration parameters specified in [Table 4-1](#) on page 105.

Table 6-1 Memory Map of DW_apb_i2c

Name	Address Offset	Width	R/W	Description
IC_CON	0x00	20 bits	R/W or R-only on bit 4 and bit 9 to 19.	<p>I²C Control</p> <p>R/W:</p> <ul style="list-style-type: none"> ■ I2C_DYNAMIC_TAR_UPDATE=1, bit 4 is read only. ■ IC_RX_FULL_HLD_BUS_EN =0, bit 9 is read only. ■ IC_STOP_DET_IF_MASTER_ACTIVE =0, bit 10 is read only. ■ IC_BUS_CLEAR_FEATURE=0, bit 11 is read only ■ IC_OPTIONAL_SAR=0, bit 16 is read only ■ IC_SMBUS=0, bit 17 is read only ■ IC_SMBUS_ARP=0, bits 18 and 19 are read only. <p>Reset Value:</p> <p>19: IC_PERSISTANT_SLV_ADDR_DEFAULT 17 to 18 : 0 16: IC_OPTIONAL_SAR_DEFAULT 15 to 7: 0 6: IC_SLAVE_DISABLE 5: IC_RESTART_EN 4: IC_10BITADDR_MASTER 3: IC_10BITADDR_SLAVE 2:1:IC_MAX_SPEED_MODE 0: IC_MASTER_MODE</p>
IC_TAR	0x04	12, 13, 14 or 16 bits	R/W	<p>I²C Target Address</p> <p>Width:</p> <p>If I2C_DYNAMIC_TAR_UPDATE=1, 13 bits If IC_DEVICE_ID=1, 14 bits If IC_SMBUS=1, 17 bits otherwise 12 bits</p> <p>Reset Value: Reset values for the four bit fields correspond to the following:</p> <p>13: 0x0 12: IC_10BITADDR_MASTER configuration parameter 11: 0x0 10: 0x0 9:0: IC_DEFAULT_TAR_SLAVE_ADDR</p>

Table 6-1 Memory Map of DW_apb_i2c

Name	Address Offset	Width	R/W	Description
IC_SAR	0x08	10 bits	R/W	I ² C Slave Address Reset Value: IC_DEFAULT_SLAVE_ADDR
IC_HS_MADDR	0x0C	3 bits	R/W	I ² C HS Master Mode Code Address Reset Value: IC_HS_MASTER_CODE
IC_DATA_CMD	0x10	Refer to Description	R/W	<p>I²C Rx/Tx Data Buffer and Command</p> <p>Reset Value: 0x0</p> <p>Width: Write:</p> <ul style="list-style-type: none"> ■ 11 bits when IC_EMPTYFIFO_HOLD_MASTER_EN=1 ■ 9 bits when IC_EMPTYFIFO_HOLD_MASTER_EN=0 <p>Read:</p> <ul style="list-style-type: none"> ■ 12 bits when IC_FIRST_DATA_BYTE_STATUS =1 ■ 8 bits when IC_FIRST_DATA_BYTE_STATUS = 0 <p>Notes:</p> <ul style="list-style-type: none"> ■ With nine or eleven bits required for writes, the DW_apb_i2c requires 16-bit data on the APB bus transfers when writing into the transmit FIFO. Eight-bit transfers remain for reads from the receive FIFO. ■ In order for the DW_apb_i2c to continue acknowledging reads, a read command should be written for every byte that is to be received; otherwise the DW_apb_i2c will stop acknowledging.
IC_SS_SCL_HCNT	0x14	16 bits	R/W	Standard speed I ² C Clock SCL High Count Reset Value: IC_SS_SCL_HIGH_COUNT
IC_SS_SCL_LCNT	0x18	16 bits	R/W	Standard speed I ² C Clock SCL Low Count Reset Value: IC_SS_SCL_LOW_COUNT
IC_FS_SCL_HCNT	0x1C	16 bits	R/W	Fast Mode and Fast Mode Plus I ² C Clock SCL High Count Reset Value: IC_FS_SCL_HIGH_COUNT
IC_FS_SCL_LCNT	0x20	16 bits	R/W	Fast Mode and Fast Mode Plus I ² C Clock SCL Low Count Reset Value: IC_FS_SCL_LOW_COUNT

Table 6-1 Memory Map of DW_apb_i2c

Name	Address Offset	Width	R/W	Description
IC_HS_SCL_HCNT	0x24	16 bits	R/W	High speed I ² C Clock SCL High Count Reset Value: IC_HS_SCL_HIGH_COUNT
IC_HS_SCL_LCNT	0x28	16 bits	R/W	High speed I ² C Clock SCL Low Count Reset Value: IC_HS_SCL_LOW_COUNT
IC_INTR_STAT	0x2C	15 bits	R	I ² C Interrupt Status Reset Value: 0x0
IC_INTR_MASK	0x30	15 bits	R/W or Read-only on bits 12 to 14	I ² C Interrupt Mask Reset Value: If IC_BUS_CLEAR_FEATURE=0, 14'h8ff If IC_BUS_CLEAR_FEATURE=1, 15'h48ff
IC_RAW_INTR_STAT	0x34	15 bits	R	I ² C Raw Interrupt Status Reset Value: 0x0
IC_RX_TL	0x38	8 bits	R/W	I ² C Receive FIFO Threshold Reset Value: IC_RX_TL configuration parameter
IC_TX_TL	0x3C	8 bits	R/W	I ² C Transmit FIFO Threshold Reset Value: IC_TX_TL configuration parameter
IC_CLR_INTR	0x40	1 bit	R	Clear Combined and Individual Interrupts Reset Value: 0x0
IC_CLR_RX_UNDER	0x44	1 bit	R	Clear RX_UNDER Interrupt Reset Value: 0x0
IC_CLR_RX_OVER	0x48	1 bit	R	Clear RX_OVER Interrupt Reset Value: 0x0
IC_CLR_TX_OVER	0x4C	1 bit	R	Clear TX_OVER Interrupt Reset Value: 0x0
IC_CLR_RD_REQ	0x50	1 bit	R	Clear RD_REQ Interrupt Reset Value: 0x0
IC_CLR_TX_ABRT	0x54	1 bit	R	Clear TX_ABRT Interrupt Reset Value: 0x0
IC_CLR_RX_DONE	0x58	1 bit	R	Clear RX_DONE Interrupt Reset Value: 0x0
IC_CLR_ACTIVITY	0x5c	1 bit	R	Clear ACTIVITY Interrupt Reset Value: 0x0

Table 6-1 Memory Map of DW_apb_i2c

Name	Address Offset	Width	R/W	Description
IC_CLR_STOP_DET	0x60	1 bit	R	Clear STOP_DET Interrupt Reset Value: 0x0
IC_CLR_START_DET	0x64	1 bit	R	Clear START_DET Interrupt Reset Value: 0x0
IC_CLR_GEN_CALL	0x68	1 bit	R	Clear GEN_CALL Interrupt Reset Value: 0x0
IC_ENABLE	0x6C	Refer to Description	R/W	I ² C Enable Width: <ul style="list-style-type: none">■ 2 bits if IC_TX_CMD_BLOCK = 0■ 3 bits if IC_TX_CMD_BLOCK = 1■ 4 bits if IC_BUS_CLEAR_FEATURE=1■ 17 bits if IC_SMBUS=1.■ 19 bits if IC_SMBUS_SUSPEND_ALERT=1. Reset Value: 0x0
IC_STATUS	0x70	Refer to Description	R	I ² C Status register Width: <ul style="list-style-type: none">■ 7 bits if IC_STAT_FOR_CLK_STRETCH = 0■ 11 bits if IC_STAT_FOR_CLK_STRETCH =1■ 12 bits if IC_BUS_CLEAR_FEATURE=1■ 17 bits if IC_SMBUS=1■ 19 bits if IC_SMBUS_ARP=1■ 21 bits if IC_SMBUS_SUSPEND_ALERT=1 Reset Value: 0x6
IC_TXFLR	0x74	TX_ABW+1	R	Transmit FIFO Level Register Reset Value: 0x0
IC_RXFLR	0x78	RX_ABW+1	R	Receive FIFO Level Register Reset Value: 0x0
IC_SDA_HOLD	0x7C	24 bits	R/W	SDA hold time length register Reset Value: IC_DEFAULT_SDA_HOLD
IC_TX_ABRT_SOURCE	0x80	32 bits	R	I ² C Transmit Abort Status Register Reset Value: 0x0
IC_SLV_DATA_NACK_ONLY	0x84	1 bit	R/W	Generate SLV_DATA_NACK Register Reset Value: 0x0

Table 6-1 Memory Map of DW_apb_i2c

Name	Address Offset	Width	R/W	Description
IC_DMA_CR	0x88	2 bits	R/W	DMA Control Register for transmit and receive handshaking interface Reset Value: 0x0
IC_DMA_TDLR	0x8c	TX_ABW	R/W	DMA Transmit Data Level Reset Value: 0x0
IC_DMA_RDLR	0x90	RX_ABW	R/W	DMA Receive Data Level Reset Value: 0x0
IC_SDA_SETUP	0x94	8 bits	R/W	I ² C SDA Setup Register Reset Value: IC_DEFAULT_SDA_SETUP configuration parameter
IC_ACK_GENERAL_CALL	0x98	1 bit	R/W	I ² C ACK General Call Register Reset Value: IC_DEFAULT_ACK_GENERAL_CALL configuration parameter
IC_ENABLE_STATUS	0x9C	3 bits	R	I ² C Enable Status Register Reset Value: 0x0
IC_FS_SPKLEN	0xA0	8 bits	R/W	ISS and FS spike suppression limit Reset Value: IC_DEFAULT_FS_SPKLEN configuration parameter
IC_HS_SPKLEN	0xA4	8 bits	R/W	HS spike suppression limit Reset Value: IC_DEFAULT_HS_SPKLEN configuration parameter
IC_CLR_RESTART_DET	0xA8	1 bit	R	Clear RESTART_DET Interrupt Reset Value: 0x0
IC_COMP_PARAM_1	0xf4	32 bits	R	Component Parameter Register Reset Value: Reset value depends on configuration parameters. For more information on component parameters and the values therefore set by them, refer to Table 4-1 on page 105 .
IC_COMP_VERSION	0xf8	32 bits	R	Component Version ID Reset Value: See the releases table in the AMBA 2 release notes
IC_COMP_TYPE	0xfc	32 bits	R	DesignWare Component Type Register Reset Value: 0x44570140

Table 6-1 Memory Map of DW_apb_i2c

Name	Address Offset	Width	R/W	Description
IC_SCL_STUCK_AT_LOW_TIMOUT	0xAC	32 bits	R/W	I ² C SCL stuck at low timeout register Reset Value: IC_SCL_STUCK_TIMEOUT_DEFAULT
IC_SDA_STUCK_AT_LOW_TIMOUT	0xB0	32 bits	R/W	I ² C SDA Stuck at Low Timeout Reset Value: IC_SDA_STUCK_TIMEOUT_DEFAULT
IC_CLR_SCL_STUCK_DET	0xB4	1 bit	R	Clear SCL Stuck at Low Detect Interrupt Register Reset Value: 0x0
IC_DEVICE_ID	0xb8	24 bits	R	I ² C Device ID Reset Value: IC_DEVICE_ID_VALUE
IC_UFM_SCL_HCNT	0x14	16 bits	R/W	Ultra-Fast mode I ² C Clock High Count Register Reset Value: IC_UFM_SCL_HIGH_COUNT
IC_UFM_SCL_LCNT	0x18	16 bits	R/W	Ultra-Fast mode I ² C Clock Low Count Register Reset Value: IC_UFM_SCL_LOW_COUNT
IC_UFM_TBUF_CNT	0x1c	16 bits	R/W	Ultra-Fast mode TBuf Idle Count Register Reset Value: IC_UFM_TBUF_CNT_DEFAULT
IC_UFM_SPKLEN	0xA0	8 bits	R/W	I ² C Ultra-Fast mode Spike suppression Register Reset Value: IC_DEFAULT_UFM_SPKLEN
IC_SMBUS_CLOCK_LOW_S_EXT	0xBC	32 bits	R/W	SMBUS Slave Clock Extend Timeout Register
IC_SMBUS_CLOCK_LOW_M_EXT	0xC0	32 bits	R/W	SMBUS Master extend clock Timeout Register
IC_SMBUS_THIGH_MAX_IDLE_COUNT	0xC4	16 bits	R/W	SMBus Thigh MAX Bus-Idle count Register
IC_SMBUS_INTR_STAT	0xC8	32 bits	R	I ² C SMBUS Interrupt Status Register
IC_SMBUS_INTR_MASK	0xcc	32 bits	R/W	I ² C Interrupt Mask Register
IC_SMBUS_INTR_RAW_STATUS	0xd0	32 bits	R	I ² C SMBUS Raw Interrupt Status Register
IC_CLR_SMBUS_INTR	0xD4	32 bits	W	Clear SMBUS Interrupt Register
IC_OPTIONAL_SAR	0xD8	7 bits	R/W	I ² C Optional Slave Address Register
IC_SMBUS_UIDID_LSB	0xDC	32 bits	R/W	SMBUS ARP UDID LSB Register

6.2 Operation of Interrupt Registers

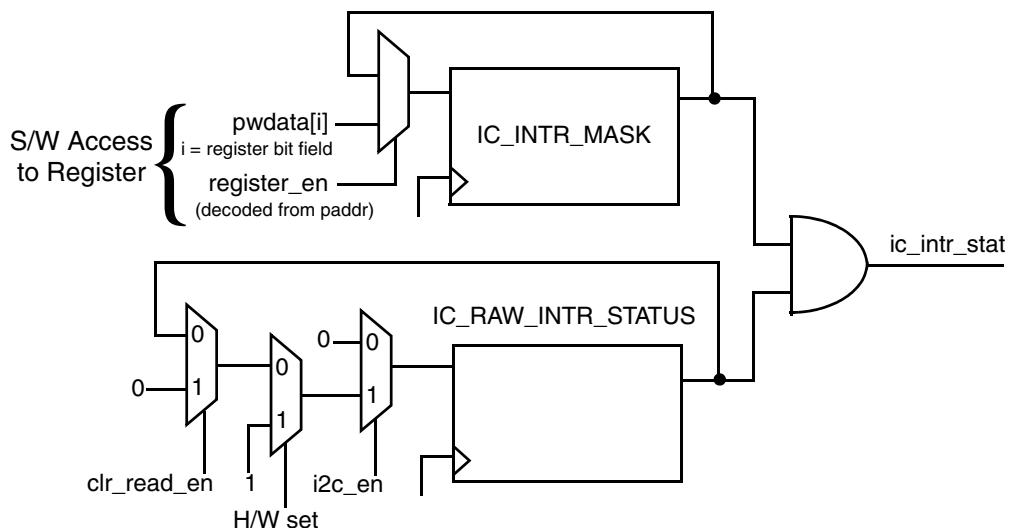
Table 6-2 lists the operation of the DW_apb_i2c interrupt registers and how they are set and cleared. Some bits are set by hardware and cleared by software, whereas other bits are set and cleared by hardware.

Table 6-2 Clearing and Setting of Interrupt Registers

Interrupt Bit Fields	Set by Hardware/ Cleared by Software	Set and Cleared by Hardware
MST_ON_HOLD	✗	✓
RESTART_DET	✓	✗
GEN_CALL	✓	✗
START_DET	✓	✗
STOP_DET	✓	✗
ACTIVITY	✓	✗
RX_DONE	✓	✗
TX_ABRT	✓	✗
RD_REQ	✓	✗
TX_EMPTY	✗	✓
TX_OVER	✓	✗
RX_FULL	✗	✓
RX_OVER	✓	✗
RX_UNDER	✓	✗

Figure 6-1 shows the operation of the interrupt registers where the bits are set by hardware and cleared by software.

Figure 6-1 Interrupt Scheme



6.3 Registers and Field Descriptions

This section describes the registers listed in [Table 6-1](#) on page [154](#). Registers are on the pclk domain, but status bits reflect actions that occur in the ic_clk domain. Therefore, there is delay when the pclk register reflects the activity that occurred on the ic_clk side.

Some registers may be written only when the DW_apb_i2c is disabled, programmed by the [IC_ENABLE](#) register. Software should not disable the DW_apb_i2c while it is active. If the DW_apb_i2c is in the process of transmitting when it is disabled, it stops as well as deletes the contents of the transmit buffer after the current transfer is complete. The slave continues receiving until the remote master aborts the transfer, in which case the DW_apb_i2c could be disabled. Registers that cannot be written to when the DW_apb_i2c is enabled are indicated in their descriptions.

Unless the clocks pclk and ic_clk are identical ([IC_CLK_TYPE = 0](#)), there is a two-register delay for synchronous and asynchronous modes.

6.3.1 IC_CON

- **Name:** I²C Control Register
- **Size:** 20 bits
- **Address Offset:** 0x00
- **Read/Write Access:**
 - If configuration parameter [I2C_DYNAMIC_TAR_UPDATE=1](#), bit 4 is read only.
 - If configuration parameter [IC_RX_FULL_HLD_BUS_EN =0](#), bit 9 is read only.
 - If configuration parameter [IC_STOP_DET_IF_MASTER_ACTIVE =0](#), bit 10 is read only.
 - If configuration parameter [IC_BUS_CLEAR_FEATURE=0](#), bit 11 is read only
 - If configuration parameter [IC_OPTIONAL_SAR=0](#), bit 16 is read only
 - If configuration parameter [IC_SMBUS=0](#), bit 17 is read only
 - If configuration parameter [IC_SMBUS_ARP=0](#), bits 18 and 19 are read only.

This register can be written only when the DW_apb_i2c is disabled, which corresponds to [IC_ENABLE\[0\]](#) being set to 0. Writes at other times have no effect.

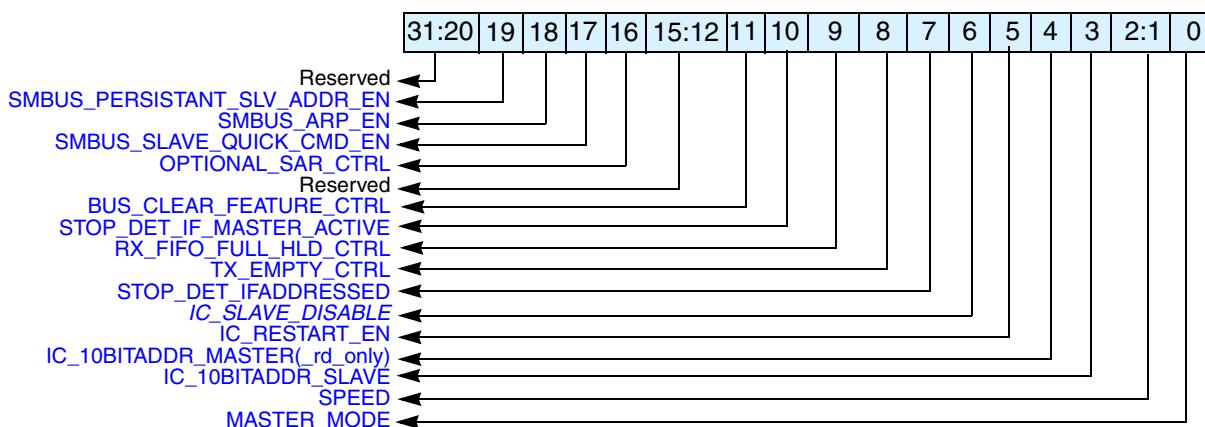


Table 6-3 IC_CON Register Fields

Bits	Name	R/W	Description
31:20	Reserved	N/A	Reserved
19	SMBUS_PERSISTANT_SLV_ADDR_EN		<p>This bit controls to enable DW_apb_i2c slave as persistent or non-persistent slave.</p> <p>If the slave is non-PSA then DW_apb_i2c slave device clears the Address valid flag for both General and Directed Reset ARP command else the address valid flag will always set to 1.</p> <p>Dependencies: This register bit is applicable only when the IC_SMBUS_ARP configuration parameter is set to 1.</p> <p>This bit is applicable only in Slave mode.</p> <p>Reset Value: IC_PERSISTANT_SLV_ADDR_DEFAULT</p>
18	SMBUS_ARP_EN	R/W	<p>This bit controls whether DW_apb_i2c should enable Address Resolution Logic in SMBus Mode. The Slave mode will decode the Address Resolution Protocol commands and respond to it. The DW_apb_i2c slave also includes the generation/validity of PEC byte for Address Resolution Protocol commands.</p> <p>This bit is applicable only in Slave mode.</p> <p>Dependencies: This register bit is applicable only when the IC_SMBUS_ARP configuration parameter is set to 1.</p> <p>Reset Value: 0x0</p>
17	SMBUS_SLAVE_QUICK_CMD_EN	R/W	<p>If this bit is set to 1, DW_apb_i2c slave only receives Quick commands in SMBus Mode.</p> <p>If this bit is set to 0, DW_apb_i2c slave receives all bus protocols but not Quick commands.</p> <p>This bit is applicable only in slave mode.</p> <p>Dependencies: This register bit is applicable only when the IC_SMBUS configuration parameter is set to 1.</p> <p>Reset Value: 0x0</p>
16	OPTIONAL_SAR_CTRL	R/W	<p>Enables the usage of IC_OPTIONAL_SAR register.</p> <p>If IC_OPTIONAL_SAR =1, IC_OPTIONAL_SAR value is used as additional slave address. User must program a valid address in IC_OPTIONAL_SAR before writing 1 to this field.</p> <p>If IC_OPTIONAL_SAR =0, IC_OPTIONAL_SAR value is not used as additional slave address. In this mode only one I2C slave address is used.</p> <p>Dependencies: This register bit is valid only if configuration parameter IC_OPTIONAL_SAR is set to 1</p> <p>Reset Value: IC_OPTIONAL_SAR_DEFAULT</p>
15:12	Reserved	R.W	Reserved

Table 6-3 IC_CON Register Fields (Continued)

Bits	Name	R/W	Description
11	BUS_CLEAR_FEATURE_CTRL	R/W	<p>In Master Mode:</p> <ul style="list-style-type: none"> ■ 1'b1: Bus Clear Feature is enabled ■ 1'b0: Bus Clear Feature is disabled <p>In Slave Mode, this register bit is not applicable.</p> <p>Reset Value: 1'b0</p> <p>Dependencies: This register bit value is applicable only when IC_BUS_CLEAR_FEATURE=1.</p> <p>This field is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1)</p>
10	STOP_DET_IF_MASTER_ACTIVE	R/W	<p>In Master mode</p> <ul style="list-style-type: none"> ■ 1'b1: Issues the STOP_DET interrupt only when the master is active ■ 1'b0: Issues the STOP_DET irrespective of whether the master is active <p>Reset value: 1'b0</p> <p>Dependencies: This Register bit value is applicable only when IC_STOP_DET_IF_MASTER_ACTIVE=1.</p> <p>This field is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1)</p>
9	RX_FIFO_FULL_HLD_CTRL	R/W or R	<p>This bit controls whether DW_apb_i2c should hold the bus when the Rx FIFO is physically full to its RX_BUFFER_DEPTH, as described in the IC_RX_FULL_HLD_BUS_EN parameter.</p> <p>Dependencies: This register bit value is applicable only when the IC_RX_FULL_HLD_BUS_EN configuration parameter is set to 1. If IC_RX_FULL_HLD_BUS_EN = 0, then this bit is read-only. If IC_RX_FULL_HLD_BUS_EN = 1, then this bit can be read or write.</p> <p>This field is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1)</p> <p>Reset value: 0x0</p>
8	TX_EMPTY_CTRL	R/W	<p>This bit controls the generation of the TX_EMPTY interrupt, as described in the IC_RAW_INTR_STAT register.</p> <p>Reset value: 0x0</p>

Table 6-3 IC_CON Register Fields (Continued)

Bits	Name	R/W	Description
7	<i>STOP_DET_IFADDRESSED</i>	R/W	<p>In slave mode:</p> <p>1'b1 – issues the STOP_DET interrupt only when it is addressed.</p> <p>1'b0 – issues the STOP_DET irrespective of whether it's addressed or not.</p> <p>Dependencies: This register bit value is applicable in the slave mode only (MASTER_MODE = 1'b0)</p> <p>Reset value: 1'b0</p> <p>NOTE: During a general call address, this slave does not issue the STOP_DET interrupt if STOP_DET_IF_ADDRESSED = 1'b1, even if the slave responds to the general call address by generating ACK. The STOP_DET interrupt is generated only when the transmitted address matches the slave address (SAR).</p>
6	<i>IC_SLAVE_DISABLE</i>	R/W	<p>This bit controls whether I²C has its slave disabled, which means once the presetn signal is applied, then this bit takes on the value of the configuration parameter IC_SLAVE_DISABLE. You have the choice of having the slave enabled or disabled after reset is applied, which means software does not have to configure the slave. By default, the slave is always enabled (in reset state as well). If you need to disable it after reset, set this bit to 1.</p> <p>If this bit is set (slave is disabled), DW_apb_i2c functions only as a master and does not perform any action that requires a slave.</p> <p>0: slave is enabled 1: slave is disabled</p> <p>Reset value: IC_SLAVE_DISABLE configuration parameter</p> <p>NOTE: Software should ensure that if this bit is written with '0,' then bit 0 should also be written with a '0'.</p>

Table 6-3 IC_CON Register Fields (Continued)

Bits	Name	R/W	Description
5	<i>IC_RESTART_EN</i>	R/W	<p>Determines whether RESTART conditions may be sent when acting as a master. Some older slaves do not support handling RESTART conditions; however, RESTART conditions are used in several DW_apb_i2c operations.</p> <p>0: disable 1: enable</p> <p>When the RESTART is disabled, the DW_apb_i2c master is incapable of performing the following functions:</p> <ul style="list-style-type: none"> ■ Sending a START BYTE ■ Performing any high-speed mode operation ■ Performing direction changes in combined format mode ■ Performing a read operation with a 10-bit address <p>By replacing RESTART condition followed by a STOP and a subsequent START condition, split operations are broken down into multiple DW_apb_i2c transfers. If the above operations are performed, it will result in setting bit 6 (<i>TX_ABRT</i>) of the <i>IC_RAW_INTR_STAT</i> register.</p> <p>Reset value: IC_RESTART_EN configuration parameter</p>
4	<i>IC_10BITADDR_MASTER</i> or <i>IC_10BITADDR_MASTER_rd_only</i>	R/W or R	<p>If the I2C_DYNAMIC_TAR_UPDATE configuration parameter is set to “No” (0), this bit is named <i>IC_10BITADDR_MASTER</i> and controls whether the DW_apb_i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master.</p> <p>If I2C_DYNAMIC_TAR_UPDATE is set to “Yes” (1), the function of this bit is handled by bit 12 of <i>IC_TAR</i> register, and becomes a read-only copy called <i>IC_10BITADDR_MASTER_rd_only</i>.</p> <p>0: 7-bit addressing 1: 10-bit addressing</p> <p>Dependencies: If I2C_DYNAMIC_TAR_UPDATE = 1, then this bit is read-only. If I2C_DYNAMIC_TAR_UPDATE = 0, then this bit can be read or write.</p> <p>Reset value: IC_10BITADDR_MASTER configuration parameter</p>
3	<i>IC_10BITADDR_SLAVE</i>	R/W	<p>When acting as a slave, this bit controls whether the DW_apb_i2c responds to 7- or 10-bit addresses.</p> <p>0: 7-bit addressing. The DW_apb_i2c ignores transactions that involve 10-bit addressing; for 7-bit addressing, only the lower 7 bits of the IC_SAR register are compared.</p> <p>1: 10-bit addressing. The DW_apb_i2c responds to only 10-bit addressing transfers that match the full 10 bits of the IC_SAR register.</p> <p>Reset value: IC_10BITADDR_SLAVE configuration parameter</p>

Table 6-3 IC_CON Register Fields (Continued)

Bits	Name	R/W	Description
 Note Bits 3 and 4 of this register can be programmed differently and in any combination depending on which format is required for the transfers. For example, master mode can be configured with 10-bit addressing and slave mode can be configured with 7-bit addressing.			
2:1	<i>SPEED</i>	R/W	<p>These bits control at which speed the DW_apb_i2c operates. Hardware protects against illegal values being programmed by software. These bits must be programmed appropriately for slave mode also, as it is used to capture correct value of spike filter as per the speed mode.</p> <p>This register should be programmed only with a value in the range of 1 to IC_MAX_SPEED_MODE; otherwise, hardware updates this register with the value of IC_MAX_SPEED_MODE.</p> <ul style="list-style-type: none"> ■ 1: standard mode (0 to 100 Kb/s) ■ 2: fast mode (\leq 400 Kb/s) or fast mode plus (\leq 1000 Kb/s) ■ 3: high speed mode (\leq 3.4 Mb/s) <p>NOTE: This field is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1)</p> <p>Reset value: IC_MAX_SPEED_MODE configuration</p>
0	<i>MASTER_MODE</i>	R/W	<p>This bit controls whether the DW_apb_i2c master is enabled.</p> <p>0: master disabled 1: master enabled</p> <p>Reset value: IC_MASTER_MODE configuration parameter</p> <p>NOTE: Software should ensure that if this bit is written with '1,' then bit 6 should also be written with a '1'.</p>

Certain combinations of the IC_SLAVE_DISABLE (bit 6) and MASTER_MODE (bit 0) result in a configuration error. [Table 6-4](#) lists the states that result from the combinations of these two bits.

Table 6-4 States for IC_SLAVE_DISABLE (bit 6) and MASTER_MODE (bit 0)

IC_SLAVE_DISABLE (IC_CON[6])	MASTER_MODE IC_CON[0]	State
0	0	Slave Device
0	1	Config Error
1	0	Config Error
1	1	Master Device



Because the DW_apb_i2c should only be used either as an I²C master or I²C slave (but not both) at any one time, care should be taken in software that certain combinations of the two bits IC_SLAVE_DISABLE and IC_MASTER_MODE are not programmed into the “IC_CON” on page 161 register. In particular, IC_SLAVE_DISABLE and IC_MASTER_MODE must not be set to ‘0’ and ‘1,’ respectively at any given time.

6.3.2 IC_TAR

- Name: I²C Target Address Register
- **Size:** 12 bits; when I2C_DYNAMIC_TAR_UPDATE = 0 and IC_DEVICE_ID = 0
13 bits; when I2C_DYNAMIC_TAR_UPDATE = 1 and IC_DEVICE_ID = 0
14 bits; when IC_DEVICE_ID = 1 irrespective of I2C_DYNAMIC_TAR_UPDATE is set
17 bits; when IC_SMBUS=1
- **Address Offset:** 0x04
- **Read/Write Access:** Read/Write

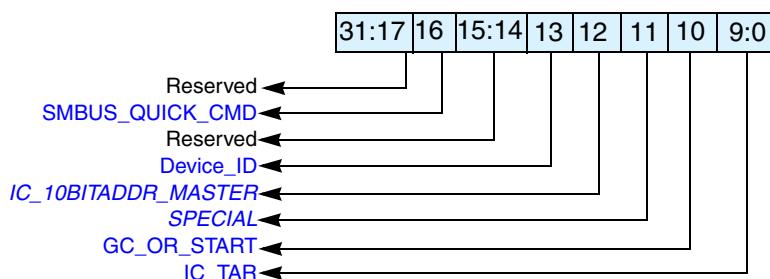
If the configuration parameter I2C_DYNAMIC_TAR_UPDATE is set to "No" (0), this register is 12 bits wide, and bits 31:12 are reserved. Writes to this register succeed only when IC_ENABLE[0] is set to 0.

However, if I2C_DYNAMIC_TAR_UPDATE = 1, then the register becomes 13 bits wide. In this case, writes to IC_TAR succeed when one of the following conditions are true:

- DW_apb_i2c is NOT enabled (IC_ENABLE[0] is set to 0); or
- DW_apb_i2c is enabled (IC_ENABLE[0]=1); AND
DW_apb_i2c is NOT engaged in any Master (tx, rx) operation (IC_STATUS[5]=0); AND
DW_apb_i2c is enabled to operate in Master mode (IC_CON[0]=1); AND
there are NO entries in the Tx FIFO (IC_STATUS[2]=1)¹

You can change the TAR address dynamically without losing the bus, only if the following conditions are met.

- DW_apb_i2c is enabled (IC_ENABLE[0]=1); AND IC_EMPTYFIFO_HOLD_MASTER_EN configuration parameter is set to 1; AND DW_apb_i2c is enabled to operate in Master mode (IC_CON[0]=1); AND there are NO entries in the Tx FIFO and the master is in HOLD state (IC_INTR_STAT[13]=1);1



1. If the software or application is aware the the DW_apb_i2c is not using the TAR address for the pending commands in the Tx FIFO, then it is possible to update the TAR address even while the Tx FIFO has entries (IC_STATUS[2]= 0).

Table 6-5 IC_TAR Register Fields

Bits	Name	R/W	Description
31:17	Reserved	N/A	Reserved
16	SMBUS_QUICK_CMD	R/W	If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a Quick command is to be performed by the DW_apb_i2c. Dependencies: This register bit is applicable only when the IC_SMBUS configuration parameter is set to 1. Reset Value: 0x0
15:14	Reserved	N/A	Reserved
13	Device_ID	R/W	If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a Device-ID of a particular slave mentioned in IC_TAR[6:0] is to be performed by the DW_apb_i2c Master. <ul style="list-style-type: none"> ■ 0: Device-ID is not performed and checks ic_tar[10] to perform either general call or START byte command. ■ 1: Device-ID transfer is performed and bytes based on the number of read commands in the Tx-FIFO are received from the targeted slave and put in the Rx-FIFO. Dependencies: This field is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1) Reset Value: 0x0
12	<i>IC_10BITADDR_MASTER</i>	R/W	This bit controls whether the DW_apb_i2c starts its transfers in 7-or 10-bit addressing mode when acting as a master. <ul style="list-style-type: none"> ■ 0: 7-bit addressing ■ 1: 10-bit addressing Dependencies: This bit exists in this register only if the I2C_DYNAMIC_TAR_UPDATE configuration parameter is set to Yes (1). Reset value: IC_10BITADDR_MASTER configuration parameter
11	<i>SPECIAL</i>	R/W	This bit indicates whether software performs a Device-ID, General Call or START BYTE command. <ul style="list-style-type: none"> ■ 0: ignore bit 10 <i>GC_OR_START</i> and use IC_TAR normally ■ 1: perform special I²C command as specified in Device-ID or <i>GC_OR_START</i> bit Reset value: 0x0

Table 6-5 IC_TAR Register Fields (Continued)

Bits	Name	R/W	Description
10	<i>GC_OR_START</i>	R/W	If bit 11 (<i>SPECIAL</i>) is set to 1 and bit 13 (Device-ID) is set to 0, then this bit indicates whether a General Call or START byte command is to be performed by the DW_apb_i2c. <ul style="list-style-type: none">■ 0: General Call Address – after issuing a General Call, only writes may be performed. Attempting to issue a read command results in setting bit 6 (TX_ABRT) of the <i>IC_RAW_INTR_STAT</i> register. The DW_apb_i2c remains in General Call mode until the <i>SPECIAL</i> bit value (bit 11) is cleared.■ 1: START BYTE Reset value: 0x0
9:0	<i>IC_TAR</i>	R/W	This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits. Reset value: IC_DEFAULT_TAR_SLAVE_ADDR configuration parameter If the <i>IC_TAR</i> and <i>IC_SAR</i> are the same, loopback exists but the FIFOs are shared between master and slave, so full loopback is not feasible. Only one direction loopback mode is supported (simplex), not duplex. A master cannot transmit to itself; it can transmit to only a slave.



Note It is not necessary to perform any write to this register if DW_apb_i2c is enabled as an I²C slave only.

6.3.3 IC_SAR

- Name: I²C Slave Address Register
- **Size:** 10 bits
- **Address Offset:** 0x08
- **Read/Write Access:** Read/Write

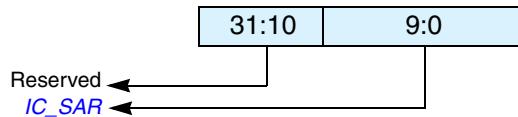


Table 6-6 IC_SAR Register Fields

Bits	Name	R/W	Description
31:10	Reserved	N/A	Reserved
9:0	IC_SAR	R/W	<p>The IC_SAR holds the slave address when the I²C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used.</p> <p>This register can be written only when the I²C interface is disabled, which corresponds to IC_ENABLE[0] being set to 0. Writes at other times have no effect.</p> <p>NOTE: The default values cannot be any of the reserved address locations: that is, 0x00 to 0x07, or 0x78 to 0x7f. The correct operation of the device is not guaranteed if you program the IC_SAR or IC_TAR to a reserved value. Refer to Table 3-1 on page 44 for a complete list of these reserved values.</p> <p>Reset value: IC_DEFAULT_SLAVE_ADDR configuration parameter</p>

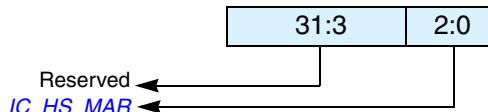


Note It is not necessary to perform any write to this register if DW_apb_i2c is enabled as an I²C master only.

6.3.4 IC_HS_MADDR

- Name: I²C High Speed Master Mode Code Address Register
- **Size:** 3 bits
- **Address Offset:** 0x0c
- **Read/Write Access:** Read/Write

This register is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE = 1).

**Table 6-7 IC_HS_MADDR Register Fields**

Bits	Name	R/W	Description
31:3	Reserved	N/A	Reserved
2:0	<i>IC_HS_MAR</i>	R/W	<p>This bit field holds the value of the I²C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight high-speed mode masters can be present on the same I²C bus system. Valid values are from 0 to 7. This register goes away and becomes read-only returning 0's if the IC_MAX_SPEED_MODE configuration parameter is set to either Standard (1) or Fast (2).</p> <p>This register can be written only when the I²C interface is disabled, which corresponds to IC_ENABLE[0] being set to 0. Writes at other times have no effect.</p> <p>Reset value: IC_HS_MASTER_CODE configuration parameter</p>



Note It is not necessary to perform any write to this register if DW_apb_i2c is enabled as an I²C slave only.

6.3.5 IC_DATA_CMD

- **Name:** I²C Rx/Tx Data Buffer and Command Register; this is the register the CPU writes to when filling the TX FIFO and the CPU reads from when retrieving bytes from RX FIFO



Note In order for the DW_apb_i2c to continue acknowledging reads, a read command should be written for every byte that is to be received; otherwise the DW_apb_i2c will stop acknowledging.

- **Size:**
 - Write
 - 11 bits when IC_EMPTYFIFO_HOLD_MASTER_EN=1
 - 9 bits when IC_EMPTYFIFO_HOLD_MASTER_EN=0
 - Read
 - 12 bits when IC_FIRST_DATA_BYTE_STATUS = 1
 - 8 bits when IC_FIRST_DATA_BYTE_STATUS = 0
- **Address Offset:** 0x10
- **Read/Write Access:** Read/Write

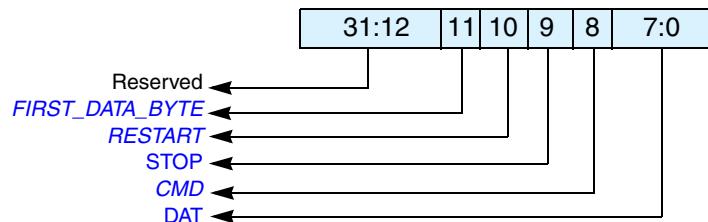


Table 6-8 IC_DATA_CMD Register Fields

Bits	Name	R/W	Description
31:12	Reserved	N/A	Reserved
11	FIRST_DATA_BYTE	R	<p>Indicates the first data byte received after the address phase for receive transfer in Master receiver or Slave receiver mode.</p> <p>Reset value: 0x0</p> <p>Dependencies: This Register bit value is applicable only when FIRST_DATA_BYTE_STATUS=1.</p> <p>Note: In case of APB_DATA_WIDTH=8:</p> <ol style="list-style-type: none"> 1. You must perform two APB Reads to IC_DATA_CMD to get status on 11 bit. 2. To read the 11 bit, you must perform the first data byte read [7:0] (offset 0x10) and then perform the second read[15:8](offset 0x11) to know the status of 11 bit (whether the data received in previous read is a first data byte). 3. The 11th bit is an optional read field. You can ignore 2nd byte read [15:8] (offset 0x11) if not interested in the FIRST_DATA_BYTE status.
10	RESTART	W	<p>This bit controls whether a RESTART is issued before the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1.</p> <ul style="list-style-type: none"> ■ 1 – If IC_RESTART_EN is 1, a RESTART is issued before the data is sent/received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead. ■ 0 – If IC_RESTART_EN is 1, a RESTART is issued only if the transfer direction is changing from the previous command; if IC_RESTART_EN is 0, a STOP followed by a START is issued instead.
9	STOP	W	<p>This bit controls whether a STOP is issued after the byte is sent or received. This bit is available only if IC_EMPTYFIFO_HOLD_MASTER_EN is configured to 1.</p> <ul style="list-style-type: none"> ■ 1 – STOP is issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master immediately tries to start a new transfer by issuing a START and arbitrating for the bus. ■ 0 – STOP is not issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master continues the current transfer by sending/receiving data bytes according to the value of the CMD bit. If the Tx FIFO is empty, the master holds the SCL line low and stalls the bus until a new command is available in the Tx FIFO.

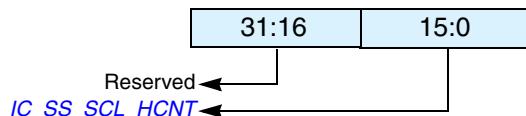
Table 6-8 IC_DATA_CMD Register Fields (Continued)

Bits	Name	R/W	Description
8	CMD	W	<p>This bit controls whether a read or a write is performed. This bit does not control the direction when the DW_apb_i2c acts as a slave. It controls only the direction when it acts as a master.</p> <ul style="list-style-type: none"> ■ 1 = Read ■ 0 = Write <p>When a command is entered in the TX FIFO, this bit distinguishes the write and read commands. In slave-receiver mode, this bit is a “don’t care” because writes to this register are not required. In slave-transmitter mode, a “0” indicates that the data in IC_DATA_CMD is to be transmitted.</p> <p>When programming this bit, you should remember the following: attempting to perform a read operation after a General Call command has been sent results in a <i>TX_ABRT</i> interrupt (bit 6 of the <i>IC_RAW_INTR_STAT</i> register), unless bit 11 (<i>SPECIAL</i>) in the <i>IC_TAR</i> register has been cleared.</p> <p>If a “1” is written to this bit after receiving a <i>RD_REQ</i> interrupt, then a <i>TX_ABRT</i> interrupt occurs.</p> <p>Dependencies: This field is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1)</p> <p>Reset value: 0x0</p>
7:0	DAT	R/W	<p>This register contains the data to be transmitted or received on the I²C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the DW_apb_i2c. However, when you read this register, these bits return the value of data received on the DW_apb_i2c interface.</p> <p>Reset value: 0x0</p>

6.3.6 IC_SS_SCL_HCNT

- **Name:** Standard Speed I²C Clock SCL High Count Register
- **Size:** 16 bits
- **Address Offset:** 0x14
- **Read/Write Access:** Read/Write

This register is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE = 1).

**Table 6-9 IC_SS_SCL_HCNT Register Fields**

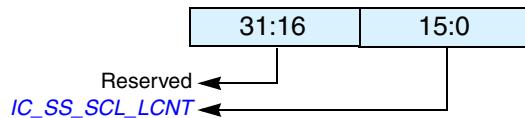
Bits	Name	R/W	Description
31:16	Reserved	N/A	Reserved
15:0	<i>IC_SS_SCL_HCNT</i>	R/W ¹	<p>This register must be set before any I²C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for standard speed. For more information, refer to “IC_CLK Frequency Configuration” on page 79.</p> <p>This register can be written only when the I²C interface is disabled which corresponds to IC_ENABLE[0] being set to 0. Writes at other times have no effect.</p> <p>The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH = 8, the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed.</p> <p>When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.</p> <p>NOTE: This register must not be programmed to a value higher than 65525, because DW_apb_i2c uses a 16-bit counter to flag an I²C bus idle condition when this counter reaches a value of IC_SS_SCL_HCNT + 10.</p> <p>Reset value: IC_SS_SCL_HIGH_COUNT configuration parameter</p>

¹Read-only if IC_HC_COUNT_VALUES = 1.

6.3.7 IC_SS_SCL_LCNT

- **Name:** Standard Speed I²C Clock SCL Low Count Register
- **Size:** 16 bits
- **Address Offset:** 0x18
- **Read/Write Access:** Read/Write

This register is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE = 1).

**Table 6-10 IC_SS_SCL_LCNT Register Fields**

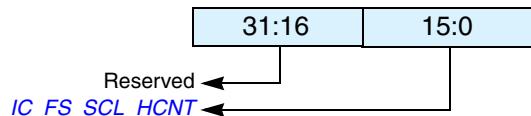
Bits	Name	R/W	Description
31:16	Reserved	N/A	Reserved
15:0	<i>IC_SS_SCL_LCNT</i>	R/W ¹	<p>This register must be set before any I²C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed. For more information, refer to “IC_CLK Frequency Configuration” on page 79.</p> <p>This register can be written only when the I²C interface is disabled which corresponds to IC_ENABLE[0] being set to 0. Writes at other times have no effect.</p> <p>The minimum valid value is 8; hardware prevents values less than this being written, and if attempted, results in 8 being set. For designs with APB_DATA_WIDTH = 8, the order of programming is important to ensure the correct operation of DW_apb_i2c. The lower byte must be programmed first, and then the upper byte is programmed.</p> <p>When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.</p> <p>Reset value: IC_SS_SCL_LOW_COUNT configuration parameter</p>

¹Read-only if IC_HC_COUNT_VALUES = 1.

6.3.8 IC_FS_SCL_HCNT

- **Name:** Fast Mode or Fast Mode Plus I²C Clock SCL High Count Register
- **Size:** 16 bits
- **Address Offset:** 0x1c
- **Read/Write Access:** Read/Write

This register is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE = 1).

**Table 6-11 IC_FS_SCL_HCNT Register Fields**

Bits	Name	R/W	Description
31:16	Reserved	N/A	Reserved
15:0	<i>IC_FS_SCL_HCNT</i>	R/W ¹	<p>This register must be set before any I²C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast mode or fast mode plus. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. For more information, refer to “IC_CLK Frequency Configuration” on page 79.</p> <p>This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE = standard. This register can be written only when the I²C interface is disabled, which corresponds to IC_ENABLE[0] being set to 0. Writes at other times have no effect.</p> <p>The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed.</p> <p>When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.</p> <p>Reset value: IC_FS_SCL_HIGH_COUNT configuration parameter</p>

¹Read-only if IC_HC_COUNT_VALUES = 1.

6.3.9 IC_FS_SCL_LCNT

- **Name:** Fast Mode or Fast Mode Plus I²C Clock SCL Low Count Register
- **Size:** 16 bits
- **Address Offset:** 0x20
- **Read/Write Access:** Read/Write

This register is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE = 1).

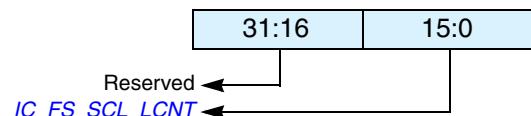


Table 6-12 IC_FS_SCL_LCNT Register Fields

Bits	Name	R/W	Description
31:16	Reserved	N/A	Reserved
15:0	<i>IC_FS_SCL_LCNT</i>	R/W ¹	<p>This register must be set before any I²C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for fast mode or fast mode plus. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. For more information, refer to “IC_CLK Frequency Configuration” on page 79.</p> <p>This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE = standard.</p> <p>This register can be written only when the I²C interface is disabled, which corresponds to IC_ENABLE[0] being set to 0. Writes at other times have no effect.</p> <p>The minimum valid value is 8; hardware prevents values less than this being written, and if attempted results in 8 being set. For designs with APB_DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 8.</p> <p>When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.</p> <p>Reset value: IC_FS_SCL_LOW_COUNT configuration parameter</p>

¹Read-only if IC_HC_COUNT_VALUES = 1.

6.3.10 IC_HS_SCL_HCNT

- **Name:** High Speed I²C Clock SCL High Count Register
- **Size:** 16 bits
- **Address Offset:** 0x24
- **Read/Write Access:** Read/Write

This register is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE = 1).

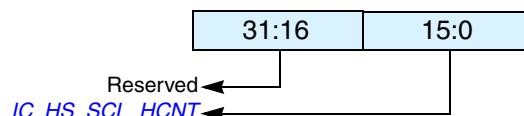


Table 6-13 IC_HS_SCL_HCNT Register Fields

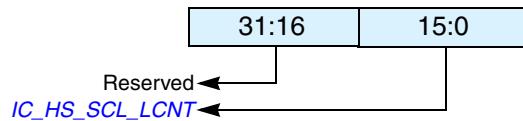
Bits	Name	R/W	Description
31:16	Reserved	N/A	Reserved
15:0	<i>IC_HS_SCL_HCNT</i>	R/W ¹	<p>This register must be set before any I²C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high period count for high speed. For more information, refer to “IC_CLK Frequency Configuration” on page 79.</p> <p>The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns.</p> <p>This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE != high.</p> <p>This register can be written only when the I²C interface is disabled, which corresponds to IC_ENABLE[0] being set to 0. Writes at other times have no effect.</p> <p>The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed.</p> <p>When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.</p> <p>Reset value: IC_HS_SCL_HIGH_COUNT configuration parameter</p>

¹Read-only if IC_HC_COUNT_VALUES = 1.

6.3.11 IC_HS_SCL_LCNT

- **Name:** High Speed I²C Clock SCL Low Count Register
- **Size:** 16 bits
- **Address Offset:** 0x28
- **Read/Write Access:** Read/Write

This register is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE = 1).

**Table 6-14 IC_HS_SCL_LCNT Register Fields**

Bits	Name	R/W	Description
31:16	Reserved	N/A	Reserved
15:0	IC_HS_SCL_LCNT	R/W ¹	<p>This register must be set before any I²C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for high speed. For more information, refer to “IC_CLK Frequency Configuration” on page 79.</p> <p>The SCL low time depends on the loading of the bus. For 100pF loading, the SCL low time is 160ns; for 400pF loading, the SCL low time is 320ns.</p> <p>This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE != high.</p> <p>This register can be written only when the I²C interface is disabled, which corresponds to IC_ENABLE[0] being set to 0. Writes at other times have no effect.</p> <p>The minimum valid value is 8; hardware prevents values less than this being written, and if attempted results in 8 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 8.</p> <p>When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.</p> <p>Reset value: IC_HS_SCL_LOW_COUNT configuration parameter</p>

¹Read-only if IC_HC_COUNT_VALUES = 1.

6.3.12 IC_INTR_STAT

- **Name:** I²C Interrupt Status Register
- **Size:** 15 bits
- **Address Offset:** 0x2C
- **Read/Write Access:** Read

Each bit in this register has a corresponding mask bit in the [IC_INTR_MASK](#) register. These bits are cleared by reading the matching interrupt clear register. The unmasked raw versions of these bits are available in the [IC_RAW_INTR_STAT](#) register.

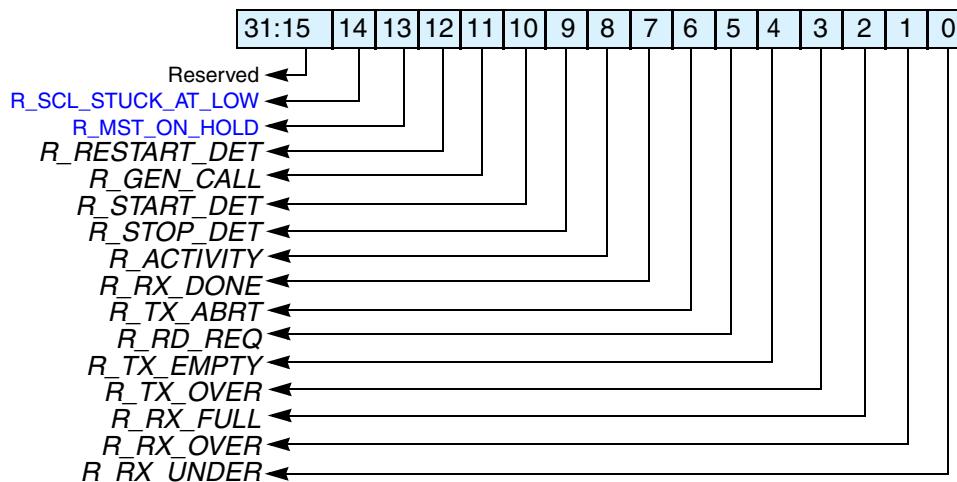


Table 6-15 IC_INTR_STAT Register Fields

Bits	Name	R/W	Description
31:15	Reserved	N/A	Reserved
14	R_SCL_STUCK_AT_LOW	R	<p>See IC_RAW_INTR_STAT for a detailed description of this bit.</p> <p>Dependencies: This field is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1).</p> <p>Reset value: 0x0</p>
13	R_MST_ON_HOLD	R	<p>See "IC_RAW_INTR_STAT" on page 186 for a detailed description of this bit.</p> <p>Reset value: 0x0</p>

Table 6-15 IC_INTR_STAT Register Fields (Continued)

Bits	Name	R/W	Description
12	<i>R_RESTART_DET</i>		
11	<i>R_GEN_CALL</i>		
10	<i>R_START_DET</i>		
9	<i>R_STOP_DET</i>		
8	<i>R_ACTIVITY</i>		
7	<i>R_RX_DONE</i>		
6	<i>R_TX_ABRT</i>		
5	<i>R_RD_REQ</i>		
4	<i>R_TX_EMPTY</i>		
3	<i>R_TX_OVER</i>		
2	<i>R_RX_FULL</i>		
1	<i>R_RX_OVER</i>		
0	<i>R_RX_UNDER</i>		

6.3.13 IC_INTR_MASK

- **Name:** I²C Interrupt Mask Register
- **Size:** 15 bits
- **Address Offset:** 0x30
- **Read/Write Access:** Read/Write
 - If configuration parameter IC_SLV_RESTART_DET = 0, bit 13 is read only.
 - If configuration parameter I2C_DYNAMIC_TAR_UPDATE = 0 or IC_EMPTYFIFO_HOLD_MASTER_EN = 0, bit 14 is read only.
 - If configuration parameter IC_BUS_CLEAR_FEATURE = 0, bit 15 is read only.

These bits mask their corresponding interrupt status bits. This register is active low; a value of 0 masks the interrupt, whereas a value of 1 unmasks the interrupt.

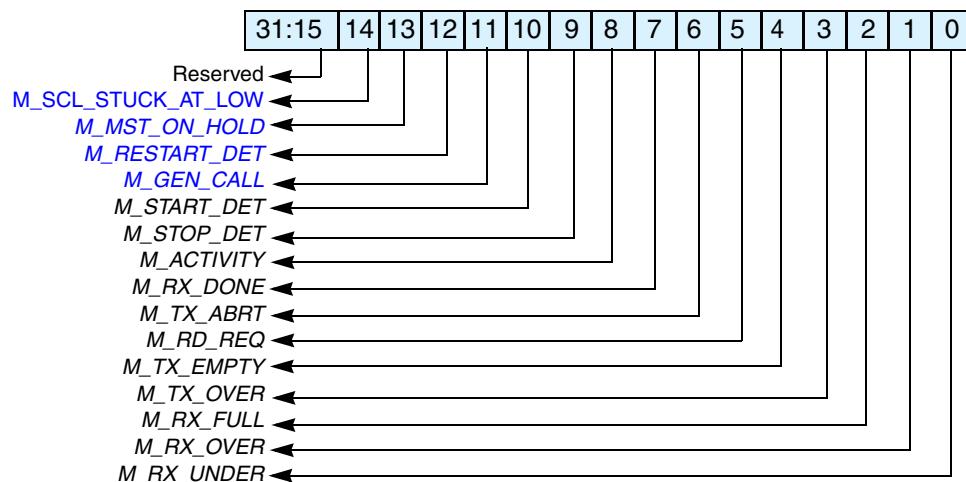


Table 6-16 IC_INTR_MASK Register Fields

Bits	Name	R/W	Description
31:15	Reserved	N/A	Reserved
14	M_SCL_STUCK_AT_LOW	R or R/W	<p>This bit masks the R_SCL_STUCK_AT_LOW interrupt bit in the IC_INTR_STAT register</p> <p>This bit is enabled only when IC_BUS_CLEAR_FEATURE = 1.</p> <p>Dependencies: This field is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1)</p> <p>Reset Value: 0x1</p>
13	M_MST_ON_HOLD	R or R/W	<p>This bit masks the R_MST_ON_HOLD interrupt bit in the IC_INTR_STAT register.</p> <p>Dependencies: If I2C_DYNAMIC_TAR_UPDATE = 1 and IC_EMPTY FIFO_HOLD_MASTER_EN = 1, then M_MST_ON_HOLD is read/write. Otherwise M_MST_ON_HOLD is read-only.</p> <p>Reset value: 14'h8ff</p>
12	M_RESTART_DET	R or R/W	<p>This bit masks the R_RESTART_DET interrupt status bit in the IC_INTR_STAT register.</p> <p>Dependencies: If IC_SLV_RESTART_DET_EN = 1, then M_RESTART_DET is read/write. Otherwise M_RESTART_DET is read-only.</p> <p>Reset value: 14'h8ff</p>

Table 6-16 IC_INTR_MASK Register Fields (Continued)

Bits	Name	R/W	Description
11	<i>M_GEN_CALL</i>		
10	<i>M_START_DET</i>		
9	<i>M_STOP_DET</i>		
8	<i>M_ACTIVITY</i>		
7	<i>M_RX_DONE</i>		
6	<i>M_TX_ABRT</i>		
5	<i>M_RD_REQ</i>		
4	<i>M_TX_EMPTY</i>		
3	<i>M_TX_OVER</i>		
2	<i>M_RX_FULL</i>		
1	<i>M_RX_OVER</i>		
0	<i>M_RX_UNDER</i>		

6.3.14 IC_RAW_INTR_STAT

- **Name:** I²C Raw Interrupt Status Register
- **Size:** 15 bits
- **Address Offset:** 0x34
- **Read/Write Access:** Read

Unlike the [IC_INTR_STAT](#) register, these bits are not masked so they always show the true status of the DW_apb_i2c.

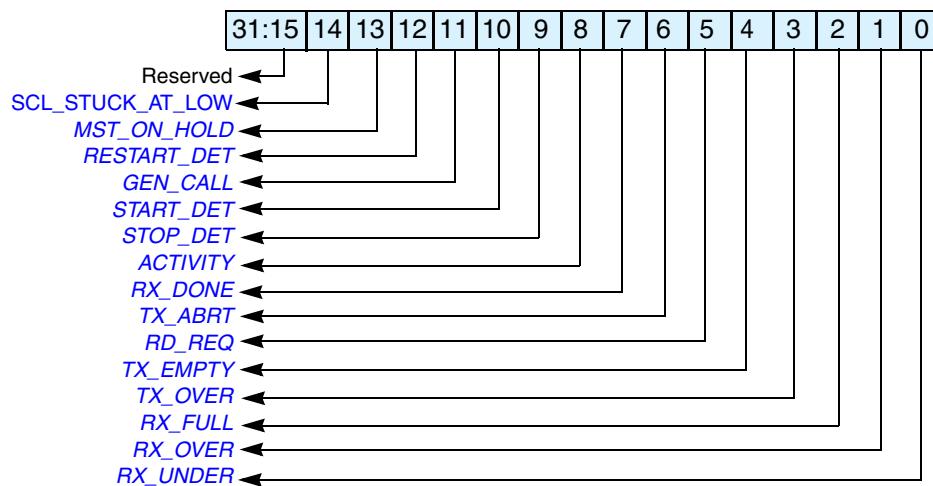


Table 6-17 IC_RAW_INTR_STAT Register Fields

Bits	Name	R/W	Description
31:15	Reserved	N/A	Reserved
14	SCL_STUCK_AT_LOW	R	<p>Indicates whether the SCL Line is stuck at low for the IC_SCL_STUCK_LOW_TIMOUT number of ic_clk periods.</p> <p>Enabled only when IC_BUS_CLEAR_FEATURE = 1</p> <p>Dependencies: This field is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1)</p> <p>Reset Value: 0x0</p>

Table 6-17 IC_RAW_INTR_STAT Register Fields (Continued)

Bits	Name	R/W	Description
13	<i>MST_ON_HOLD</i>	R	Indicates whether a master is holding the bus and the Tx FIFO is empty. Enabled only when I2C_DYNAMIC_TAR_UPDATE = 1 and IC_EMPTYFIFO_HOLD_MASTER_EN = 1 Reset value: 0x0
12	<i>RESTART_DET</i>	R	Indicates whether a RESTART condition has occurred on the I ² C interface when DW_apb_i2c is operating in slave mode and the slave is the addressed slave. Enabled only when IC_SLV_RESTART_DET_EN = 1 NOTE: However, in high-speed mode or during a START BYTE transfer, the RESTART comes before the address field as per the I ² C protocol. In this case, the slave is not the addressed slave when the RESTART is issued, therefore DW_apb_i2c does not generate the RESTART_DET interrupt. Reset value: 0x0
11	<i>GEN_CALL</i>	R	Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling DW_apb_i2c or when the CPU reads bit 0 of the <i>IC_CLR_GEN_CALL</i> register. DW_apb_i2c stores the received data in the Rx buffer. Reset value: 0x0
10	<i>START_DET</i>	R	Indicates whether a START or RESTART condition has occurred on the I ² C interface regardless of whether DW_apb_i2c is operating in slave or master mode. Reset value: 0x0
9	<i>STOP_DET</i>	R	Indicates whether a STOP condition has occurred on the I ² C interface regardless of whether DW_apb_i2c is operating in slave or master mode. In Slave Mode: <ul style="list-style-type: none"> ■ If IC_CON[7]=1'b1 (STOP_DET_IFADDRESSED), the STOP_DET interrupt is generated only if the slave is addressed. Note: During a general call address, this slave does not issue a STOP_DET interrupt if STOP_DET_IF_ADDRESSED=1'b1, even if the slave responds to the general call address by generating ACK. The STOP_DET interrupt is generated only when the transmitted address matches the slave address (SAR). ■ If IC_CON[7]=1'b0 (STOP_DET_IFADDRESSED), the STOP_DET interrupt is issued irrespective of whether it is being addressed. In Master Mode: <ul style="list-style-type: none"> ■ If IC_CON[10]=1'b1 (STOP_DET_IF_MASTER_ACTIVE), the STOP_DET interrupt is issued only if the master is active. ■ If IC_CON[10]=1'b0 (STOP_DET_IFADDRESSED), the STOP_DET interrupt is issued irrespective of whether the master is active. Reset value: 0x0

Table 6-17 IC_RAW_INTR_STAT Register Fields (Continued)

Bits	Name	R/W	Description
8	<i>ACTIVITY</i>	R	<p>This bit captures DW_apb_i2c activity and stays set until it is cleared. There are four ways to clear it:</p> <ul style="list-style-type: none"> ■ Disabling the DW_apb_i2c ■ Reading the <i>IC_CLR_ACTIVITY</i> register ■ Reading the <i>IC_CLR_INTR</i> register ■ System reset <p>Once this bit is set, it stays set unless one of the four methods is used to clear it. Even if the DW_apb_i2c module is idle, this bit remains set until cleared, indicating that there was activity on the bus.</p> <p>Reset value: 0x0</p>
7	<i>RX_DONE</i>	R	<p>When the DW_apb_i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.</p> <p>Dependencies: This field is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1)</p> <p>Reset value: 0x0</p>
6	<i>TX_ABRT</i>	R	<p>This bit indicates if DW_apb_i2c, as an I²C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO. This situation can occur both as an I²C master or an I²C slave, and is referred to as a “transmit abort”.</p> <p>When this bit is set to 1, the <i>IC_TX_ABRT_SOURCE</i> register indicates the reason why the transmit abort takes places.</p> <p>NOTE: The DW_apb_i2c flushes/resets/empties only the TX_FIFO whenever there is a transmit abort caused by any of the events tracked by the <i>IC_TX_ABRT_SOURCE</i> register. The Tx FIFO remains in this flushed state until the register <i>IC_CLR_TX_ABRT</i> is read. Once this read is performed, the Tx FIFO is then ready to accept more data bytes from the APB interface. RX FIFO is flushed because of TX_ABRT is controlled by the coreConsultant parameter <i>IC_AVOID_RX_FIFO_FLUSH_ON_TX_ABRT</i>.</p> <p>Reset value: 0x0</p>
5	<i>RD_REQ</i>	R	<p>This bit is set to 1 when DW_apb_i2c is acting as a slave and another I²C master is attempting to read data from DW_apb_i2c. The DW_apb_i2c holds the I²C bus in a wait state (SCL=0) until this interrupt is serviced, which means that the slave has been addressed by a remote master that is asking for data to be transferred. The processor must respond to this interrupt and then write the requested data to the <i>IC_DATA_CMD</i> register. This bit is set to 0 just after the processor reads the <i>IC_CLR_RD_REQ</i> register.</p> <p>Dependencies: This field is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1)</p> <p>Reset value: 0x0</p>

Table 6-17 IC_RAW_INTR_STAT Register Fields (Continued)

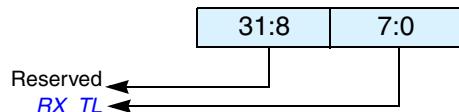
Bits	Name	R/W	Description
4	<i>TX_EMPTY</i>	R	<p>The behavior of the TX_EMPTY interrupt status differs based on the TX_EMPTY_CTRL selection in the IC_CON register.</p> <ul style="list-style-type: none"> ■ When TX_EMPTY_CTRL = 0: This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register. ■ When TX_EMPTY_CTRL = 1: This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register and the transmission of the address/data from the internal shift register for the most recently popped command is completed. <p>It is automatically cleared by hardware when the buffer level goes above the threshold. When IC_ENABLE[0] is set to 0, the TX FIFO is flushed and held in reset. There the TX FIFO looks like it has no data within it, so this bit is set to 1, provided there is activity in the master or slave state machines. When there is no longer any activity, then with ic_en=0, this bit is set to 0.</p> <p>Reset value: 0x0</p>
3	<i>TX_OVER</i>	R	<p>Set during transmit if the transmit buffer is filled to IC_RX_BUFFER_DEPTH and the processor attempts to issue another I²C command by writing to the IC_DATA_CMD register. When the module is disabled, this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.</p> <p>Reset value: 0x0</p>
2	<i>RX_FULL</i>	R	<p>Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register. It is automatically cleared by hardware when buffer level goes below the threshold. If the module is disabled (IC_ENABLE[0]=0), the RX FIFO is flushed and held in reset; therefore the RX FIFO is not full. So this bit is cleared once IC_ENABLE[0] is set to 0, regardless of the activity that continues.</p> <p>Reset value: 0x0</p>
1	<i>RX_OVER</i>	R	<p>Set if the receive buffer is completely filled to IC_RX_BUFFER_DEPTH and an additional byte is received from an external I²C device. The DW_apb_i2c acknowledges this, but any data bytes received after the FIFO is full are lost. If the module is disabled (IC_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.</p> <p>NOTE: If the configuration parameter IC_RX_FULL_HLD_BUS_EN is enabled and bit 9 of the IC_CON register (RX_FIFO_FULL_HLD_CTRL) is programmed to HIGH, then the RX_OVER interrupt never occurs, because the Rx FIFO never overflows.</p> <p>Reset value: 0x0</p>

Table 6-17 IC_RAW_INTR_STAT Register Fields (Continued)

Bits	Name	R/W	Description
0	<i>RX_UNDER</i>	R	Set if the processor attempts to read the receive buffer when it is empty by reading from the <i>IC_DATA_CMD</i> register. If the module is disabled (<i>IC_ENABLE[0]</i> =0), this bit keeps its level until the master or slave state machines go into idle, and when <i>ic_en</i> goes to 0, this interrupt is cleared. Reset value: 0x0

6.3.15 IC_RX_TL

- **Name:** I²C Receive FIFO Threshold Register
- **Size:** 8bits
- **Address Offset:** 0x38
- **Read/Write Access:** Read/Write

**Table 6-18 IC_RX_TL Register Fields**

Bits	Name	R/W	Description
31:8	Reserved	N/A	Reserved
7:0	<i>RX_TL</i>	R/W	Receive FIFO Threshold Level Controls the level of entries (or above) that triggers the <i>RX_FULL</i> interrupt (bit 2 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 1 entry, and a value of 255 sets the threshold for 256 entries. Reset value: IC_RX_TL configuration parameter

6.3.16 IC_TX_TL

- **Name:** I²C Transmit FIFO Threshold Register
- **Size:** 8 bits
- **Address Offset:** 0x3c
- **Read/Write Access:** Read/Write

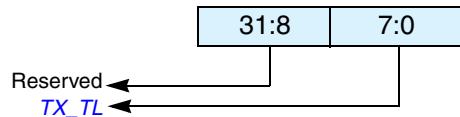


Table 6-19 IC_TX_TL Register Fields

Bits	Name	R/W	Description
31:8	Reserved	N/A	Reserved
7:0	<i>TX_TL</i>	R/W	<p>Transmit FIFO Threshold Level</p> <p>Controls the level of entries (or below) that trigger the <i>TX_EMPTY</i> interrupt (bit 4 in <i>IC_RAW_INTR_STAT</i> register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.</p> <p>A value of 0 sets the threshold for 0 entries, and a value of 255 sets the threshold for 255 entries.</p> <p>Reset value: IC_TX_TL configuration parameter</p>

6.3.17 IC_CLR_INTR

- **Name:** Clear Combined and Individual Interrupt Register
- **Size:** 1 bit
- **Address Offset:** 0x40
- **Read/Write Access:** Read

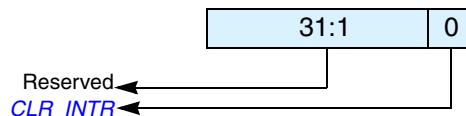


Table 6-20 IC_CLR_INTR Register Fields

Bits	Name	R/W	Description
31:1	Reserved	N/A	Reserved
0	<i>CLR_INTR</i>	R	<p>Read this register to clear the combined interrupt, all individual interrupts, and the <i>IC_TX_ABRT_SOURCE</i> register. This bit does not clear hardware clearable interrupts but software clearable interrupts. Refer to Bit 9 of the <i>IC_TX_ABRT_SOURCE</i> register for an exception to clearing <i>IC_TX_ABRT_SOURCE</i>.</p> <p>Reset value: 0x0</p>

6.3.18 IC_CLR_RX_UNDER

- **Name:** Clear RX_UNDER Interrupt Register
- **Size:** 1 bit
- **Address Offset:** 0x44
- **Read/Write Access:** Read

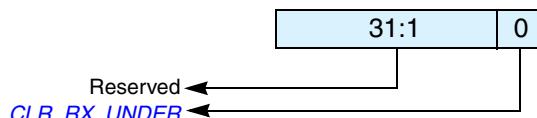


Table 6-21 IC_CLR_RX_UNDER Register Fields

Bits	Name	R/W	Description
31:1	Reserved	N/A	Reserved
0	<i>CLR_RX_UNDER</i>	R	<p>Read this register to clear the <i>RX_UNDER</i> interrupt (bit 0) of the <i>IC_RAW_INTR_STAT</i> register.</p> <p>Reset value: 0x0</p>

6.3.19 IC_CLR_RX_OVER

- **Name:** Clear RX_OVER Interrupt Register
- **Size:** 1 bit
- **Address Offset:** 0x48
- **Read/Write Access:** Read

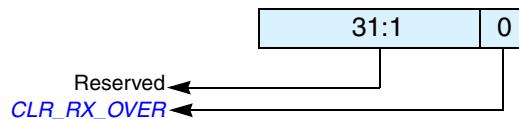


Table 6-22 IC_CLR_RX_OVER Register Fields

Bits	Name	R/W	Description
31:1	Reserved	N/A	Reserved
0	<i>CLR_RX_OVER</i>	R	Read this register to clear the <i>RX_OVER</i> interrupt (bit 1) of the <i>IC_RAW_INTR_STAT</i> register. Reset value: 0x0

6.3.20 IC_CLR_TX_OVER

- **Name:** Clear TX_OVER Interrupt Register
- **Size:** 1 bit
- **Address Offset:** 0x4c
- **Read/Write Access:** Read

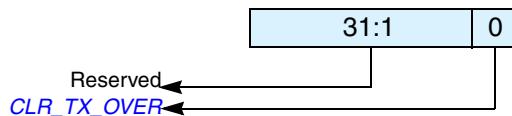


Table 6-23 IC_CLR_TX_OVER Register Fields

Bits	Name	R/W	Description
31:1	Reserved	N/A	Reserved
0	<i>CLR_TX_OVER</i>	R	Read this register to clear the <i>TX_OVER</i> interrupt (bit 3) of the <i>IC_RAW_INTR_STAT</i> register. Reset value: 0x0

6.3.21 IC_CLR_RD_REQ

- **Name:** Clear RD_REQ Interrupt Register
- **Size:** 1 bit
- **Address Offset:** 0x50
- **Read/Write Access:** Read
- **Dependencies:** This Register is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1)

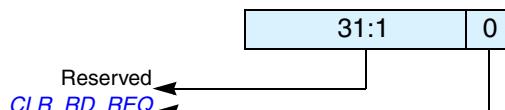


Table 6-24 IC_CLR_RD_REQ Register Fields

Bits	Name	R/W	Description
31:1	Reserved	N/A	Reserved
0	<i>CLR_RD_REQ</i>	R	Read this register to clear the <i>RD_REQ</i> interrupt (bit 5) of the <i>IC_RAW_INTR_STAT</i> register. Reset value: 0x0

6.3.22 IC_CLR_TX_ABRT

- **Name:** Clear TX_ABRT Interrupt Register
- **Size:** 1 bit
- **Address Offset:** 0x54
- **Read/Write Access:** Read

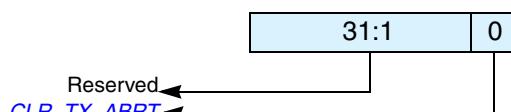


Table 6-25 IC_CLR_TX_ABRT Register Fields

Bits	Name	R/W	Description
31:1	Reserved	N/A	Reserved
0	<i>CLR_TX_ABRT</i>	R	Read this register to clear the <i>TX_ABRT</i> interrupt (bit 6) of the <i>IC_RAW_INTR_STAT</i> register, and the <i>IC_TX_ABRT_SOURCE</i> register. This also releases the Tx FIFO from the flushed/reset state, allowing more writes to the Tx FIFO. Refer to Bit 9 of the <i>IC_TX_ABRT_SOURCE</i> register for an exception to clearing <i>IC_TX_ABRT_SOURCE</i> . Reset value: 0x0

6.3.23 IC_CLR_RX_DONE

- **Name:** Clear RX_DONE Interrupt Register
- **Size:** 1 bit
- **Address Offset:** 0x58
- **Read/Write Access:** Read
- **Dependencies:** This Register is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1)

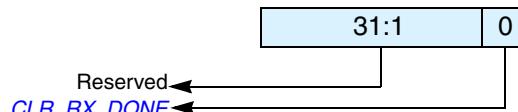


Table 6-26 IC_CLR_RX_DONE Register Fields

Bits	Name	R/W	Description
31:1	Reserved	N/A	Reserved
0	<i>CLR_RX_DONE</i>	R	Read this register to clear the <i>RX_DONE</i> interrupt (bit 7) of the <i>IC_RAW_INTR_STAT</i> register. Reset value: 0x0

6.3.24 IC_CLR_ACTIVITY

- **Name:** Clear ACTIVITY Interrupt Register
- **Size:** 1 bit
- **Address Offset:** 0x5c
- **Read/Write Access:** Read

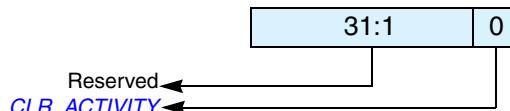


Table 6-27 IC_CLR_ACTIVITY Register Fields

Bits	Name	R.W	Description
31:1	Reserved	N/A	Reserved
0	<i>CLR_ACTIVITY</i>	R	Reading this register clears the <i>ACTIVITY</i> interrupt if the I ² C is not active anymore. If the I ² C module is still active on the bus, the <i>ACTIVITY</i> interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the <i>ACTIVITY</i> interrupt (bit 8) of the <i>IC_RAW_INTR_STAT</i> register. Reset value: 0x0

6.3.25 IC_CLR_STOP_DET

- **Name:** Clear STOP_DET Interrupt Register
- **Size:** 1 bit
- **Address Offset:** 0x60
- **Read/Write Access:** Read

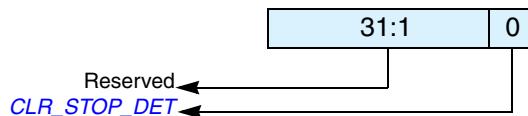


Table 6-28 IC_CLR_STOP_DET Register Fields

Bits	Name	R/W	Description
31:1	Reserved	N/A	Reserved
0	<i>CLR_STOP_DET</i>	R	Read this register to clear the <i>STOP_DET</i> interrupt (bit 9) of the <i>IC_RAW_INTR_STAT</i> register. Reset value: 0x0

6.3.26 IC_CLR_START_DET

- **Name:** Clear START_DET Interrupt Register
- **Size:** 1 bit
- **Address Offset:** 0x64
- **Read/Write Access:** Read

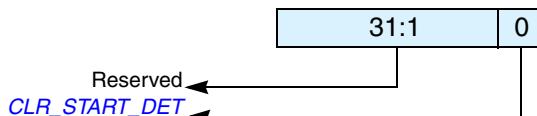


Table 6-29 IC_CLR_START_DET Register Fields

Bits	Name	R/W	Description
31:1	Reserved	N/A	Reserved
0	<i>CLR_START_DET</i>	R	Read this register to clear the <i>START_DET</i> interrupt (bit 10) of the <i>IC_RAW_INTR_STAT</i> register. Reset value: 0x0

6.3.27 IC_CLR_GEN_CALL

- **Name:** Clear GEN_CALL Interrupt Register
- **Size:** 1 bit
- **Address Offset:** 0x68
- **Read/Write Access:** Read

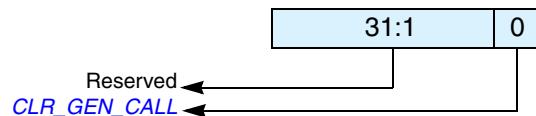


Table 6-30 IC_CLR_GEN_CALL Register Fields

Bits	Name	R/W	Description
31:1	Reserved	N/A	Reserved
0	<i>CLR_GEN_CALL</i>	R	Read this register to clear the <i>GEN_CALL</i> interrupt (bit 11) of <i>IC_RAW_INTR_STAT</i> register. Reset value: 0x0

6.3.28 IC_ENABLE

- Name: I²C Enable Register
- Size: 19 bits
- Address Offset: 0x6c
- Read/Write Access: Read/Write
 - Bit 2 is read only when IC_TX_CMD_BLOCK_DEFAULT=0
 - Bit 3 is read only when IC_BUS_CLEAR_FEATURE = 0
 - Bit 16 is read only when IC_SMBUS=0.
 - Bit 17 and 18 are read only when IC_SMBUS_SUSPEND_ALERT=0.

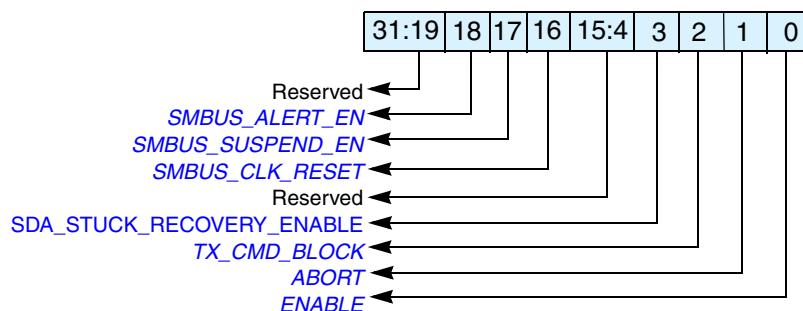


Table 6-31 IC_ENABLE Register Fields

Bits	Name	R/W	Description
31:19	Reserved	N/A	Reserved
18	SMBUS_ALERT_EN	R/W	<p>The SMBUS_ALERT_CTRL register bit is used to control assertion of SMBALERT signal. 1: Assert SMBALERT signal This register bit is auto-cleared after detection of Acknowledgement from master for Alert Response address.</p> <p>Dependencies: This Register bit value is applicable only when IC_SMBUS_SUSPEND_ALERT=1 Reset Value: 0x0</p>
17	SMBUS_SUSPEND_EN	R/W	<p>The SMBUS_SUSPEND_EN register bit is used to control assertion and de-assertion of SMBSUS signal. 0: De-assert SMBSUS signal 1: Assert SMBSUS signal</p> <p>Dependencies: This Register bit value is applicable only when IC_SMBUS_SUSPEND_ALERT=1 Reset Value: 0x0</p>

Table 6-31 IC_ENABLE Register Fields (Continued)

Bits	Name	R/W	Description
16	SMBUS_CLK_RESET	R/W	<p>This bit is used in SMBus Host mode to initiate the SMBus Master Clock Reset. This bit should be enabled only when Master is in idle. Whenever this bit is enabled, the SMBCLK is held low for the IC_SCL_STUCK_TIMEOUT ic_clk cycles to reset the SMBus Slave devices.</p> <p>Dependencies: This Register bit value is applicable only when IC_SMBUS=1</p> <p>Reset Value: 0x0</p>
15:4	Reserved	N/A	Reserved
3	SDA_STUCK_RECOVERY_ENABLE	R/W	<p>If SDA is stuck at low indicated through the TX_ABORT interrupt (IC_TX_ABRT_SOURCE[17]), then this bit is used as a control knob to initiate the SDA Recovery Mechanism (that is, send at most 9 SCL clocks and STOP to release the SDA line) and then this bit gets auto clear.</p> <p>This bit is enabled only when IC_BUS_CLEAR_FEATURE = 1.</p> <p>Dependencies: This field is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1)</p> <p>Reset Value: 0x0</p>
2	TX_CMD_BLOCK	R/W	<p>In Master mode</p> <ul style="list-style-type: none"> ■ 1'b1: Blocks the transmission of data on I²C bus even if Tx FIFO has data to transmit. ■ 1'b0: The transmission of data starts on I²C bus automatically, as soon as the first data is available in the Tx FIFO. <p>Reset value: IC_TX_CMD_BLOCK_DEFAULT</p> <p>Dependencies: This Register bit value is applicable only when IC_TX_CMD_BLOCK =1.</p> <p>Note: To block the execution of Master commands, set the TX_CMD_BLOCK bit only when Tx FIFO is empty (IC_STATUS[2]=1) and the master is in the Idle state (IC_STATUS[5] == 0). Any further commands put in the Tx FIFO are not executed until TX_CMD_BLOCK bit is unset.</p>
1	ABORT	R/W	<p>When set, the controller initiates the transfer abort.</p> <ul style="list-style-type: none"> ■ 0: ABORT not initiated or ABORT done ■ 1: ABORT operation in progress <p>The software can abort the I²C transfer in master mode by setting this bit. The software can set this bit only when ENABLE is already set; otherwise, the controller ignores any write to ABORT bit. The software cannot clear the ABORT bit once set. In response to an ABORT, the controller issues a STOP and flushes the Tx FIFO after completing the current transfer, then sets the TX_ABORT interrupt after the abort operation. The ABORT bit is cleared automatically after the abort operation.</p> <p>For a detailed description on how to abort I²C transfers, refer to “Aborting I²C Transfers” on page 63.</p> <p>Reset value: 0x0</p>

Table 6-31 IC_ENABLE Register Fields (Continued)

Bits	Name	R/W	Description
0	<i>ENABLE</i>	R/W	<p>Controls whether the DW_apb_i2c is enabled.</p> <ul style="list-style-type: none"> ■ 0: Disables DW_apb_i2c (TX and RX FIFOs are held in an erased state) ■ 1: Enables DW_apb_i2c <p>Software can disable DW_apb_i2c while it is active. However, it is important that care be taken to ensure that DW_apb_i2c is disabled properly. A recommended procedure is described in “Disabling DW_apb_i2c” on page 62. When DW_apb_i2c is disabled, the following occurs:</p> <ul style="list-style-type: none"> ■ The TX FIFO and RX FIFO get flushed. ■ Status bits in the <i>IC_INTR_STAT</i> register are still active until DW_apb_i2c goes into IDLE state. <p>If the module is transmitting, it stops as well as deletes the contents of the transmit buffer after the current transfer is complete. If the module is receiving, the DW_apb_i2c stops the current transfer at the end of the current byte and does not acknowledge the transfer.</p> <p>In systems with asynchronous pclk and ic_clk when IC_CLK_TYPE parameter set to asynchronous (1), there is a two ic_clk delay when enabling or disabling the DW_apb_i2c.</p> <p>For a detailed description on how to disable DW_apb_i2c, refer to “Disabling DW_apb_i2c” on page 62.</p> <p>Reset value: 0x0</p>

6.3.29 IC_STATUS

- **Name:** I²C Status Register
- **Size:** 32 bits
- **Address Offset:** 0x70
- **Read/Write Access:** Read

This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt.

When the I²C is disabled by writing 0 in bit 0 of the IC_ENABLE register:

- Bits 1 and 2 are set to 1
- Bits 3 to 10 are set to 0

When the master or slave state machines goes to idle and ic_en=0:

- Bits 5 and 6 are set to 0

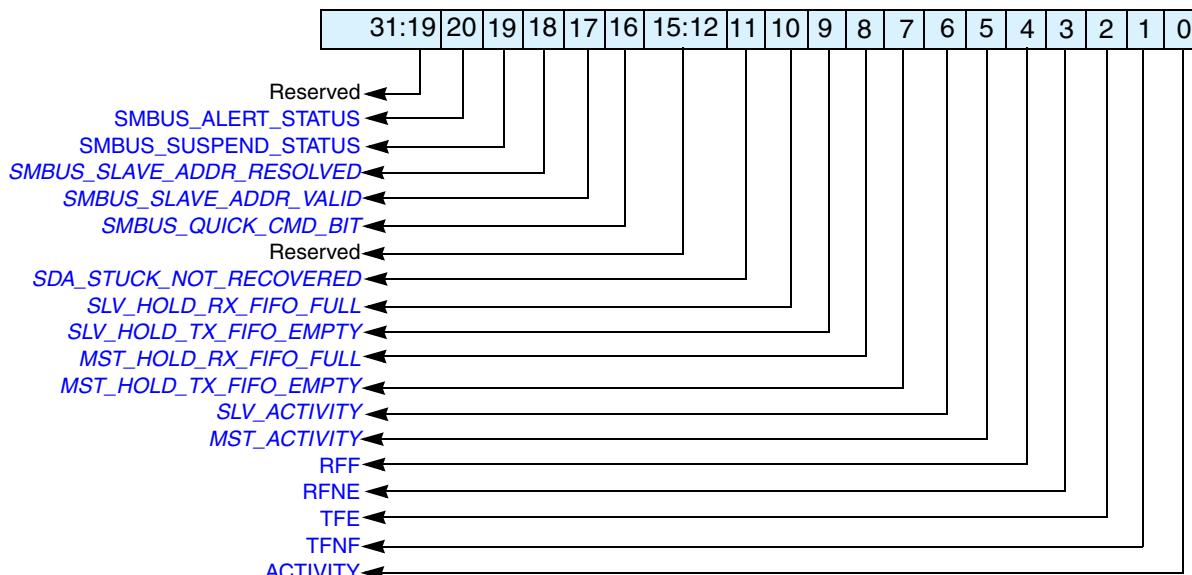


Table 6-32 IC_STATUS Register Fields

Bits	Name	R/W	Description
31:19	Reserved	N/A	Reserved
20	SMBUS_ALERT_STATUS	R	<p>This bit indicates whether the status of the input signal is ic_smbus_alert_in_n. This signal is asserted when the SMBus Alert signal is asserted by the SMBus Device.</p> <p>Dependencies: Enabled only when IC_SMBUS_SUSPEND_ALERT=1 is set to 1.</p> <p>Reset Value: 0x0</p>

Table 6-32 IC_STATUS Register Fields (Continued)

Bits	Name	R/W	Description
19	SMBUS_SUSPEND_STATUS	R	<p>This bit indicates whether the status of the input signal is ic_smbus_sus_in_n. This signal is asserted when the SMBus Suspend signal is asserted by the SMBus Host.</p> <p>Dependencies: Enabled only when IC_SMBUS_SUSPEND_ALERT=1 is set to 1.</p> <p>Reset Value: 0x0</p>
18	SMBUS_SLAVE_ADDR_RESOLVED	R	<p>This bit indicates whether the SMBus Slave address (ic_sar[6:0]) is Resolved by ARP Master.</p> <p>Dependencies: Enabled only when IC_SMBUS_ARP=1 is set to 1.</p> <p>Reset Value: 0x0</p>
17	SMBUS_SLAVE_ADDR_VALID	R	<p>This bit indicates whether the SMBus Slave address (ic_sar[6:0]) is valid or not.</p> <p>Dependencies: Enabled only when IC_SMBUS_ARP=1 is set to 1.</p> <p>Reset Value: 0x0</p>
16	SMBUS_QUICK_CMD_BIT	R	<p>This bit indicates the R/W bit of the Quick command received. This bit will be cleared after the user has read this bit.</p> <p>Dependencies: Enabled only when IC_SMBUS=1 is set to 1.</p> <p>Reset Value: 0x0</p>
15:12	Reserved	N/A	Reserved
11	SDA_STUCK_NOT_RECOVERED	R	<p>This bit indicates that an SDA stuck at low is not recovered after the recovery mechanism.</p> <p>This bit is enabled only when IC_BUS_CLEAR_FEATURE = 1.</p> <p>Reset Value: 0x0</p>
10	SLV_HOLD_RX_FIFO_FULL	R	<p>This bit indicates the BUS Hold in Slave mode due to the Rx FIFO being Full and an additional byte being received (this kind of Bus hold is applicable if IC_RX_FULL_HLD_BUS_EN is set to 1).</p> <p>Reset value: 0x0</p> <p>Dependencies: This Register bit value is applicable only when IC_STAT_FOR_CLK_STRETCH=1.</p>
9	SLV_HOLD_TX_FIFO_EMPTY	R	<p>This bit indicates the BUS Hold in Slave mode for the Read request when the Tx FIFO is empty. The Bus is in hold until the Tx FIFO has data to Transmit for the read request.</p> <p>Reset value: 0x0</p> <p>Dependencies: This Register bit value is applicable only when IC_STAT_FOR_CLK_STRETCH=1.</p>

Table 6-32 IC_STATUS Register Fields (Continued)

Bits	Name	R/W	Description
8	MST_HOLD_RX_FIFO_FULL	R	<p>This bit indicates the BUS Hold in Master mode due to Rx FIFO is Full and additional byte has been received (This kind of Bus hold is applicable if IC_RX_FULL_HLD_BUS_EN is set to 1).</p> <p>Reset value: 0x0</p> <p>Dependencies: This Register bit value is applicable only when IC_STAT_FOR_CLK_STRETCH=1</p>
7	MST_HOLD_TX_FIFO_EMPTY		<p>If the IC_EMPTYFIFO_HOLD_MASTER_EN parameter is set to 1, the DW_apb_i2c master stalls the write transfer when Tx FIFO is empty, and the the last byte does not have the Stop bit set.</p> <p>This bit indicates the BUS hold when the master holds the bus because of the Tx FIFO being empty, and the the previous transferred command does not have the Stop bit set. (This kind of Bus hold is applicable if IC_EMPTYFIFO_HOLD_MASTER_EN is set to 1).</p> <p>Reset value: 0x0</p> <p>Dependencies: This Register bit value is applicable only when IC_STAT_FOR_CLK_STRETCH=1</p>
6	SLV_ACTIVITY	R	<p>Slave FSM Activity Status. When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set.</p> <ul style="list-style-type: none"> ■ 0: Slave FSM is in IDLE state so the Slave part of DW_apb_i2c is not Active ■ 1: Slave FSM is not in IDLE state so the Slave part of DW_apb_i2c is Active <p>Reset value: 0x0</p>
5	MST_ACTIVITY	R	<p>Master FSM Activity Status. When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set.</p> <ul style="list-style-type: none"> ■ 0: Master FSM is in IDLE state so the Master part of DW_apb_i2c is not Active ■ 1: Master FSM is not in IDLE state so the Master part of DW_apb_i2c is Active <p>NOTE: IC_STATUS[0]—that is, ACTIVITY bit—is the OR of SLV_ACTIVITY and MST_ACTIVITY bits.</p> <p>Reset value: 0x0</p>

Table 6-32 IC_STATUS Register Fields (Continued)

Bits	Name	R/W	Description
4	<i>RFF</i>	R	<p>Receive FIFO Completely Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared.</p> <ul style="list-style-type: none"> ■ 0: Receive FIFO is not full ■ 1: Receive FIFO is full <p>Reset value: 0x0</p>
3	<i>RFNE</i>	R	<p>Receive FIFO Not Empty. This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty.</p> <ul style="list-style-type: none"> ■ 0: Receive FIFO is empty ■ 1: Receive FIFO is not empty <p>Reset value: 0x0</p>
2	<i>TFE</i>	R	<p>Transmit FIFO Completely Empty. When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt.</p> <ul style="list-style-type: none"> ■ 0: Transmit FIFO is not empty ■ 1: Transmit FIFO is empty <p>Reset value: 0x1</p>
1	<i>TFNF</i>	R	<p>Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full.</p> <ul style="list-style-type: none"> ■ 0: Transmit FIFO is full ■ 1: Transmit FIFO is not full <p>Reset value: 0x1</p>
0	<i>ACTIVITY</i>	R	<p>I²C Activity Status.</p> <p>Reset value: 0x0</p>

6.3.30 IC_TXFLR

- **Name:** I²C Transmit FIFO Level Register
- **Size:** TX_ABW + 1
- **Address Offset:** 0x74
- **Read/Write Access:** Read

This register contains the number of valid data entries in the transmit FIFO buffer. It is cleared whenever:

- The I²C is disabled
- There is a transmit abort—that is, TX_ABRT bit is set in the IC_RAW_INTR_STAT register
- The slave bulk transmit mode is aborted

The register increments whenever data is placed into the transmit FIFO and decrements when data is taken from the transmit FIFO.

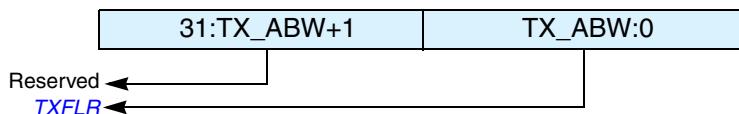


Table 6-33 IC_TXFLR Register Fields

Bits	Name	R/W	Description
31:TX_ABW+1	Reserved	N/A	Reserved
TX_ABW:0	TXFLR	R	Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO. Reset value: 0x0

6.3.31 IC_RXFLR

- **Name:** I²C Receive FIFO Level Register
- **Size:** RX_ABW + 1
- **Address Offset:** 0x78
- **Read/Write Access:** Read

This register contains the number of valid data entries in the receive FIFO buffer. It is cleared whenever:

- The I²C is disabled
- Whenever there is a transmit abort caused by any of the events tracked in *IC_TX_ABRT_SOURCE*

The register increments whenever data is placed into the receive FIFO and decrements when data is taken from the receive FIFO.

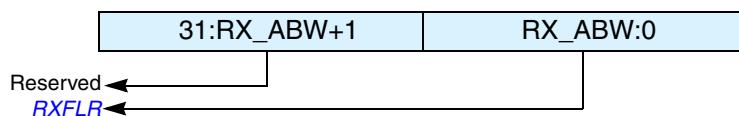


Table 6-34 IC_RXFLR Register Fields

Bits	Name	R/W	Description
31:RX_ABW+1	Reserved	N/A	Reserved
RX_ABW:0	RXFLR	R	Receive FIFO Level. Contains the number of valid data entries in the receive FIFO. Reset value: 0x0

6.3.32 IC_SDA_HOLD

- **Name:** I²C SDA Hold Time Length Register
- **Size:** 24 bits
- **Address Offset:** 0x7C
- **Read/Write Access:** Read/Write

The bits [15:0] of this register are used to control the hold time of SDA during transmit in both slave and master mode (after SCL goes from HIGH to LOW).

The bits [23:16] of this register are used to extend the SDA transition (if any) whenever SCL is HIGH in the receiver in either master or slave mode.

Writes to this register succeed only when IC_ENABLE[0]=0.

The values in this register are in units of ic_clk period. The value programmed in IC_SDA_TX_HOLD must be greater than the minimum hold time in each mode – one cycle in master mode, seven cycles in slave mode – for the value to be implemented.

The programmed SDA hold time during transmit (IC_SDA_TX_HOLD) cannot exceed at any time the duration of the low part of scl. Therefore the programmed value cannot be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the scl period measured in ic_clk cycles.

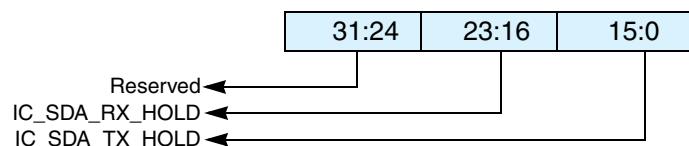


Table 6-35 IC_SDA_HOLD Register Fields

Bits	Name	R/W	Description
31:24	Reserved	N/A	Reserved
23:16	<i>IC_SDA_RX_HOLD</i>	R/W	Sets the required SDA hold time in units of ic_clk period, when DW_apb_i2c acts as a receiver. Reset value: IC_DEFAULT_SDA_HOLD
15:0	<i>IC_SDA_TX_HOLD</i>	R/W	Sets the required SDA hold time in units of ic_clk period, when DW_apb_i2c acts as a transmitter. Reset value: IC_DEFAULT_SDA_HOLD

6.3.33 IC_TX_ABRT_SOURCE

- **Name:** I²C Transmit Abort Source Register
- **Size:** 32 bits
- **Address Offset:** 0x80
- **Read/Write Access:** Read

This register has 32 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this register is cleared whenever the *IC_CLR_TX_ABRT* register or the *IC_CLR_INTR* register is read. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; RESTART must be enabled (*IC_CON*[5]=1), the SPECIAL bit must be cleared (*IC_TAR*[11]), or the GC_OR_START bit must be cleared (*IC_TAR*[10]).

Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

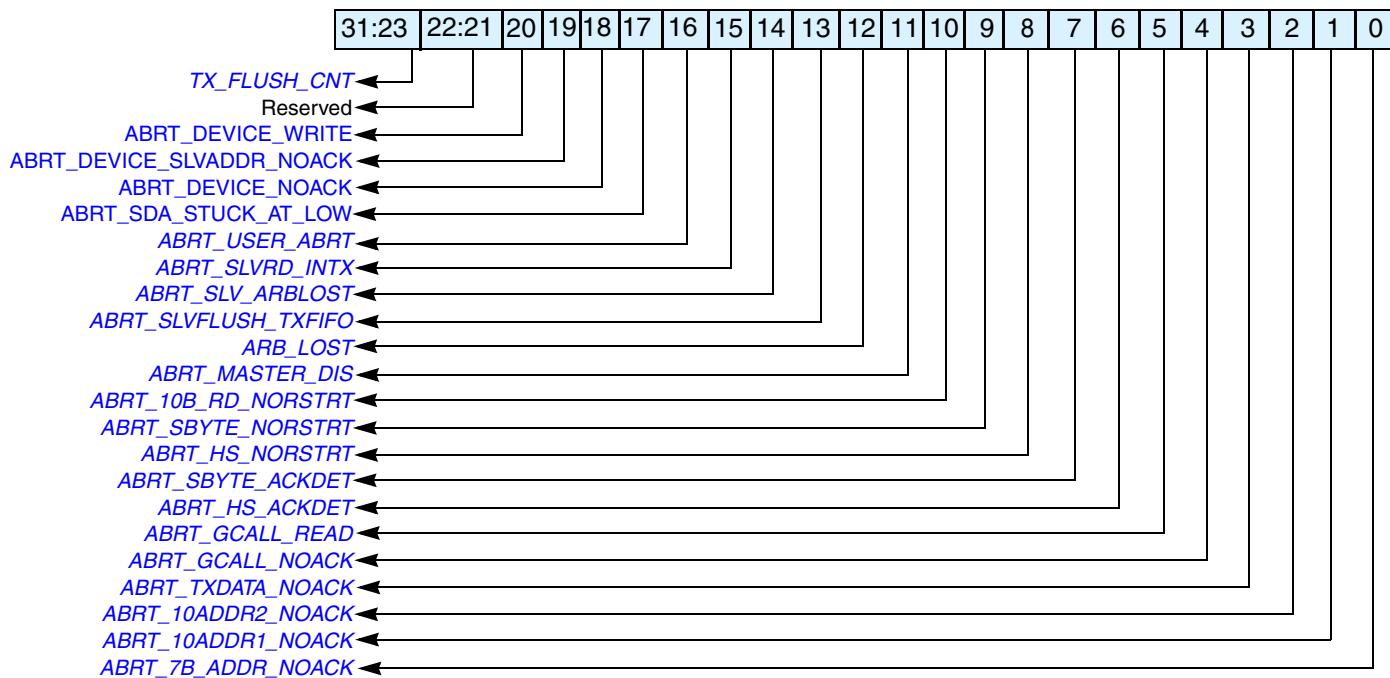


Table 6-36 IC_TX_ABRT_SOURCE Register Fields

Bits	Name	R/W	Description	Role of DW_apb_i2c
31:23	<i>TX_FLUSH_CNT</i>	R	This field indicates the number of Tx FIFO data commands that are flushed due to TX_ABRT interrupt. It is cleared whenever I ² C is disabled. Reset value: 0x0	Master-Transmitter or Slave-Transmitter
22:21	Reserved	R	These bits are reserved.	

Table 6-36 IC_TX_ABRT_SOURCE Register Fields (Continued)

Bits	Name	R/W	Description	Role of DW_apb_i2c
20	ABRT_DEVICE_WRITE	R	This is a master-mode-only bit. Master is initiating the DEVICE_ID transfer and the Tx-FIFO consists of write commands. Reset Value: 0x0	Master
19	ABRT_DEVICE_SLVADDR_NOACK	R	This is a master-mode-only bit. Master is initiating the DEVICE_ID transfer and the slave address sent was not acknowledged by any slave. Reset value: 0x0	Master
18	ABRT_DEVICE_NOACK	R	This is a master-mode-only bit. Master initiates the DEVICE_ID transfer and the device ID sent is not acknowledged by any slave. Dependency: This field is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1) Reset value: 0x0	Master
17	ABRT_SDA_STUCK_AT_LOW	R	This is a master-mode-only bit. Master detects the SDA is Stuck at low for the IC_SDA_STUCK_AT_LOW_TIMEOUT value of ic_clks. Dependency: This field is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1) Reset value: 0x0	Master
16	ABRT_USER_ABRT	R	This is a master-mode-only bit. Master has detected the transfer abort (IC_ENABLE[1]). Reset value: 0x0	Master-Transmitter
15	ABRT_SLVRD_INTX	R	1: When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in <i>CMD</i> (bit 8) of <i>IC_DATA_CMD</i> register. Dependency: This field is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1) Reset value: 0x0	Slave-Transmitter

Table 6-36 IC_TX_ABRT_SOURCE Register Fields (Continued)

Bits	Name	R/W	Description	Role of DW_apb_i2c
14	<i>ABRT_SLV_ARBLOST</i>	R	<ul style="list-style-type: none"> ■ 1: Slave lost the bus while transmitting data to a remote master. <i>IC_TX_ABRT_SOURCE[12]</i> is set at the same time. <p>Dependency: This field is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1) NOTE: Even though the slave never “owns” the bus, something could go wrong on the bus. This is a fail safe check. For instance, during a data transmission at the low-to-high transition of SCL, if what is on the data bus is not what is supposed to be transmitted, then DW_apb_i2c no longer own the bus. Dependency: Reset value: 0x0</p>	Slave-Transmitter
13	<i>ABRT_SLVFLUSH_TXFIFO</i>	R	<ul style="list-style-type: none"> ■ 1: Slave has received a read command and some data exists in the TX FIFO so the slave issues a <i>TX_ABRT</i> interrupt to flush old data in TX FIFO. <p>Dependency: This field is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1) Reset value: 0x0</p>	Slave-Transmitter
12	<i>ARB_LOST</i>	R	<ul style="list-style-type: none"> ■ 1: Master has lost arbitration, or if <i>IC_TX_ABRT_SOURCE[14]</i> is also set, then the slave transmitter has lost arbitration. <p>Dependency: This field is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1) Reset value: 0x0</p>	Master-Transmitter or Slave-Transmitter
11	<i>ABRT_MASTER_DIS</i>	R	<ul style="list-style-type: none"> ■ 1: User tries to initiate a Master operation with the Master mode disabled. <p>Reset value: 0x0</p>	Master-Transmitter or Master-Receiver

Table 6-36 IC_TX_ABRT_SOURCE Register Fields (Continued)

Bits	Name	R/W	Description	Role of DW_apb_i2c
10	<i>ABRT_10B_RD_NORSTRT</i>	R	<ul style="list-style-type: none"> ■ 1: The restart is disabled (<i>IC_RESTART_EN</i> bit (<i>IC_CON[5]</i>) = 0) and the master sends a read command in 10-bit addressing mode. <p>Dependencies: This field is not applicable in Ultra-Fast speed mode (<i>IC_ULTRA_FAST_MODE</i>=1).</p> <p>Reset value: 0x0</p>	Master-Receiver
9	<i>ABRT_SBYTE_NORSTRT</i>	R	<p>To clear Bit 9, the source of the <i>ABRT_SBYTE_NORSTRT</i> must be fixed first; restart must be enabled (<i>IC_CON[5]</i>=1), the SPECIAL bit must be cleared (<i>IC_TAR[11]</i>), or the GC_OR_START bit must be cleared (<i>IC_TAR[10]</i>). Once the source of the <i>ABRT_SBYTE_NORSTRT</i> is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the <i>ABRT_SBYTE_NORSTRT</i> is not fixed before attempting to clear this bit, bit 9 clears for one cycle and then gets re-asserted.</p> <ul style="list-style-type: none"> 1: The restart is disabled (<i>IC_RESTART_EN</i> bit (<i>IC_CON[5]</i>) = 0) and the user is trying to send a START Byte. <p>Reset value: 0x0</p>	Master
8	<i>ABRT_HS_NORSTRT</i>	R	<ul style="list-style-type: none"> ■ 1: The restart is disabled (<i>IC_RESTART_EN</i> bit (<i>IC_CON[5]</i>) = 0) and the user is trying to use the master to transfer data in High Speed mode. <p>Dependency: This field is not applicable in Ultra-Fast speed mode (<i>IC_ULTRA_FAST_MODE</i>=1)</p> <p>Reset value: 0x0</p>	Master-Transmitter or Master-Receiver
7	<i>ABRT_SBYTE_ACKDET</i>	R	<ul style="list-style-type: none"> ■ 1: Master has sent a START Byte and the START Byte was acknowledged (wrong behavior). <p>Dependency: This field is not applicable in Ultra-Fast speed mode (<i>IC_ULTRA_FAST_MODE</i>=1)</p> <p>Reset value: 0x0</p>	Master

Table 6-36 IC_TX_ABRT_SOURCE Register Fields (Continued)

Bits	Name	R/W	Description	Role of DW_apb_i2c
6	<i>ABRT_HS_ACKDET</i>	R	<ul style="list-style-type: none"> ■ 1: Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior). <p>Dependency: This field is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1) Reset value: 0x0</p>	Master
5	<i>ABRT_GCALL_READ</i>	R	<ul style="list-style-type: none"> ■ 1: DW_apb_i2c in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1). <p>Dependency: This field is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1) Reset value: 0x0</p>	Master-Transmitter
4	<i>ABRT_GCALL_NOACK</i>	R	<ul style="list-style-type: none"> ■ 1: DW_apb_i2c in master mode sent a General Call and no slave on the bus acknowledged the General Call. <p>Dependency: This field is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1) Reset value: 0x0</p>	Master-Transmitter
3	<i>ABRT_TXDATA_NOACK</i>	R	<ul style="list-style-type: none"> ■ 1: This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s). <p>Dependency: This field is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1) Reset value: 0x0</p>	Master-Transmitter
2	<i>ABRT_10ADDR2_NOACK</i>	R	<ul style="list-style-type: none"> ■ 1: Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave. <p>Dependency: This field is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1) Reset value: 0x0</p>	Master-Transmitter or Master-Receiver

Table 6-36 IC_TX_ABRT_SOURCE Register Fields (Continued)

Bits	Name	R/W	Description	Role of DW_apb_i2c
1	<i>ABRT_10ADDR1_NOACK</i>	R	<ul style="list-style-type: none"> ■ 1: Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave. <p>Dependency: This field is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1) Reset value: 0x0</p>	Master-Transmitter or Master-Receiver
0	<i>ABRT_7B_ADDR_NOACK</i>	R	<ul style="list-style-type: none"> ■ 1: Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave. <p>Dependency: This field is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1) Reset value: 0x0</p>	Master-Transmitter or Master-Receiver

6.3.34 IC_SLV_DATA_NACK_ONLY

- **Name:** Generate Slave Data NACK Register
- **Size:** 1 bit
- **Address Offset:** 0x84
- **Read/Write Access:** Read/Write
- **Dependency:** This Register is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1).

The register is used to generate a NACK for the data part of a transfer when DW_apb_i2c is acting as a slave-receiver. This register only exists when the IC_SLV_DATA_NACK_ONLY parameter is set to 1. When this parameter disabled, this register does not exist and writing to the register's address has no effect.

A write can occur on this register if both of the following conditions are met:

- DW_apb_i2c is disabled (IC_ENABLE[0] = 0)
- Slave part is inactive (IC_STATUS[6] = 0)



Note The IC_STATUS[6] is a register read-back location for the internal slv_activity signal; the user should poll this before writing the ic_slv_data_nack_only bit.

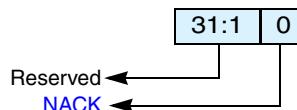


Table 6-37 IC_SLV_DATA_NACK_ONLY Register Fields

Bits	Name	R/W	Description
31:1	Reserved	N/A	Reserved
0	NACK	R/W	<p>Generate NACK. This NACK generation only occurs when DW_apb_i2c is a slave-receiver. If this register is set to a value of 1, it can only generate a NACK after a data byte is received; hence, the data transfer is aborted and the data received is not pushed to the receive buffer.</p> <p>When the register is set to a value of 0, it generates NACK/ACK, depending on normal criteria.</p> <ul style="list-style-type: none"> ■ 1 = generate NACK after data byte received ■ 0 = generate NACK/ACK normally <p>Reset value: 0x0</p>

6.3.35 IC_DMA_CR

- **Name:** DMA Control Register
- **Size:** 2 bits
- **Address Offset:** 0x88
- **Read/Write Access:** Read/Write

This register is only valid when DW_apb_i2c is configured with a set of DMA Controller interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist and writing to the register's address has no effect and reading from this register address will return zero. The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of IC_ENABLE.

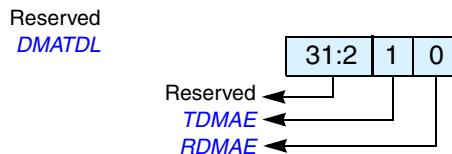


Table 6-38 IC_DMA_CR Register Fields

Bits	Name	R/W	Description
31:2	Reserved	N/A	Reserved
1	TDMAE	R/W	Transmit DMA Enable. This bit enables/disables the transmit FIFO DMA channel. <ul style="list-style-type: none"> ■ 0 = Transmit DMA disabled ■ 1 = Transmit DMA enabled Reset value: 0x0
0	RDMAE	R/W	Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel. <ul style="list-style-type: none"> ■ 0 = Receive DMA disabled ■ 1 = Receive DMA enabled Reset value: 0x0

6.3.36 IC_DMA_TDRL

- **Name:** DMA Transmit Data Level Register
- **Size:** TX_ABW-1:0
- **Address Offset:** 0x8c
- **Read/Write Access:** Read/Write

This register is only valid when the DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist; writing to its address has no effect; reading from its address returns zero.

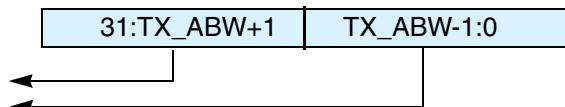


Table 6-39 IC_DMA_TDRL Register Fields

Bits	Name	R/W	Description
31:TX_ABW	Reserved	N/A	Reserved
TX_ABW-1:0	<i>DMATDL</i>	R/W	<p>Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the <i>dma_tx_req</i> signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and <i>TDMAE</i> = 1.</p> <p>Reset value: 0x0</p>

6.3.37 IC_DMA_RDLR

- **Name:** I²C Receive Data Level Register
- **Size:** RX_ABW-1:0
- **Address Offset:** 0x90
- **Read/Write Access:** Read/Write

This register is only valid when DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist; writing to its address has no effect; reading from its address returns zero.

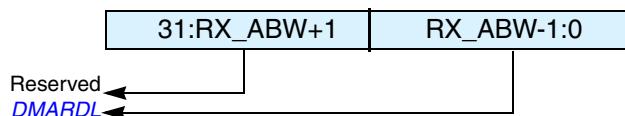


Table 6-40 IC_DMA_RDLR Register Fields

Bits	Name	R/W	Description
31:RX_ABW	Reserved	N/A	Reserved
RX_ABW-1:0	DMARDL	R/W	<p>Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = <i>DMARDL</i>+1; that is, <i>dma_rx_req</i> is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and <i>RDMAE</i> = 1. For instance, when <i>DMARDL</i> is 0, then <i>dma_rx_req</i> is asserted when 1 or more data entries are present in the receive FIFO.</p> <p>Reset value: 0x0</p>

6.3.38 IC_SDA_SETUP

- **Name:** I²C SDA Setup Register
- **Size:** 8 bits
- **Address Offset:** 0x94
- **Read/Write Access:** Read/Write
- **Dependency:** This register is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1).

This register controls the amount of time delay (in terms of number of ic_clk clock periods) introduced in the rising edge of SCL – relative to SDA changing – by holding SCL low when DW_apb_i2c services a read request while operating as a slave-transmitter. The relevant I²C requirement is $t_{SU:DAT}$ (note 4) as detailed in the *I2C Bus Specification*. This register must be programmed with a value equal to or greater than 2.

Writes to this register succeed only when IC_ENABLE[0] = 0.



Note The length of setup time is calculated using $[(IC_SDA_SETUP - 1) * (ic_clk_period)]$, so if the user requires 10 ic_clk periods of setup time, they should program a value of 11.

The IC_SDA_SETUP register is only used by the DW_apb_i2c when operating as a slave transmitter.

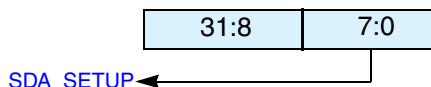


Table 6-41 IC_SDA_SETUP Register Fields

Bits	Name	R/W	Description
31:8	Reserved	N/A	Reserved
7:0	SDA_SETUP	R/W	SDA Setup. It is recommended that if the required delay is 1000ns, then for an ic_clk frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11. IC_SDA_SETUP must be programmed with a minimum value of 2. Default Reset value: 0x64, but can be hardcoded by setting the IC_DEFAULT_SDA_SETUP configuration parameter.

6.3.39 IC_ACK_GENERAL_CALL

- **Name:** I²C ACK General Call Register
- **Size:** 1 bit
- **Address Offset:** 0x98
- **Read/Write Access:** Read/Write
- **Dependency:** This register is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1).

The register controls whether DW_apb_i2c responds with an ACK or NACK when it receives an I²C General Call address. This register is applicable only when the DW_apb_i2c is in the slave mode.

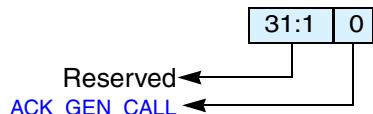


Table 6-42 IC_ACK_GENERAL_CALL Register Fields

Bits	Name	R/W	Description
31:1	Reserved	N/A	Reserved
0	ACK_GEN_CALL	R/W	ACK General Call. When set to 1, DW_apb_i2c responds with a ACK (by asserting ic_data_oe) when it receives a General Call. When set to 0, the DW_apb_i2c does not generate General Call interrupts. Default Reset value: 0x1, but can be hardcoded by setting the IC_DEFAULT_ACK_GENERAL_CALL configuration parameter.

6.3.40 IC_ENABLE_STATUS

- **Name:** I²C Enable Status Register
- **Size:** 3 bits
- **Address Offset:** 0x9C
- **Read/Write Access:** Read

The register is used to report the DW_apb_i2c hardware status when IC_ENABLE[0] is set from 1 to 0; that is, when DW_apb_i2c is disabled.

If IC_ENABLE[0] has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1.

If IC_ENABLE[0] has been set to 0, bits 2:1 is only valid as soon as bit 0 is read as '0'.



Note When IC_ENABLE[0] has been set to 0, a delay occurs for bit 0 to be read as 0 because disabling the DW_apb_i2c depends on I²C bus activities.

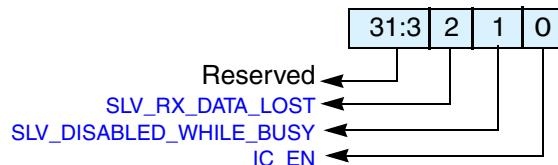


Table 6-43 IC_ENABLE_STATUS Register Fields

Bits	Name	R/W	Description
31:3	Reserved	N/A	Reserved
2	SLV_RX_DATA_LOST	R	<p>Slave Received Data Lost. This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I²C transfer due to setting IC_ENABLE[0] from 1 to 0. When read as 1, DW_apb_i2c is deemed to have been actively engaged in an aborted I²C transfer (with matching address) and the data phase of the I²C transfer has been entered, even though a data byte has been responded with a NACK.</p> <p>NOTE: If the remote I²C master terminates the transfer with a STOP condition before the DW_apb_i2c has a chance to NACK a transfer, and IC_ENABLE[0] has been set to 0, then this bit is also set to 1.</p> <p>When read as 0, DW_apb_i2c is deemed to have been disabled without being actively involved in the data phase of a Slave-Receiver transfer.</p> <p>NOTE: The CPU can safely read this bit when IC_EN (bit 0) is read as 0.</p> <p>Reset value: 0x0</p>

Table 6-43 IC_ENABLE_STATUS Register Fields (Continued)

Bits	Name	R/W	Description
1	<i>SLV_DISABLED_WHILE_BUSY</i>	R	<p>Slave Disabled While Busy (Transmit, Receive). This bit indicates if a potential or active Slave operation has been aborted due to setting bit 0 of the IC_ENABLE register from 1 to 0. This bit is set when the CPU writes a 0 to bit 0 of IC_ENABLE while: (a) DW_apb_i2c is receiving the address byte of the Slave-Transmitter operation from a remote master; OR, (b) address and data bytes of the Slave-Receiver operation from a remote master.</p> <p>When read as 1, DW_apb_i2c is deemed to have forced a NACK during any part of an I²C transfer, irrespective of whether the I²C address matches the slave address set in DW_apb_i2c (IC_SAR register) OR if the transfer is completed before bit 0 of IC_ENABLE is set to 0, but has not taken effect.</p> <p>NOTE: If the remote I²C master terminates the transfer with a STOP condition before the DW_apb_i2c has a chance to NACK a transfer, and bit 0 of IC_ENABLE has been set to 0, then this bit will also be set to 1.</p> <p>When read as 0, DW_apb_i2c is deemed to have been disabled when there is master activity, or when the I²C bus is idle.</p> <p>NOTE: The CPU can safely read this bit when <i>IC_EN</i> (bit 0) is read as 0.</p> <p>Reset value: 0x0</p>
0	<i>IC_EN</i>	R	<p>ic_en Status. This bit always reflects the value driven on the output port ic_en.</p> <ul style="list-style-type: none"> ■ When read as 1, DW_apb_i2c is deemed to be in an enabled state. ■ When read as 0, DW_apb_i2c is deemed completely inactive. <p>NOTE: The CPU can safely read this bit anytime. When this bit is read as 0, the CPU can safely read <i>SLV_RX_DATA_LOST</i> (bit 2) and <i>SLV_DISABLED_WHILE_BUSY</i> (bit 1).</p> <p>Reset value: 0x0</p>

6.3.41 IC_FS_SPKLEN

- **Name:** I²C SS and FS Spike Suppression Limit Register
- **Size:** 8 bits
- **Address Offset:** 0xA0
- **Read/Write Access:** Read/Write
- **Dependency:** This register is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1).

This register is used to store the duration, measured in *ic_clk* cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in standard mode, fast mode, or fast mode plus. The relevant I²C requirement is tSP (Table 4) as detailed in the *I²C Bus Specification*. This register must be programmed with a minimum value of 1.

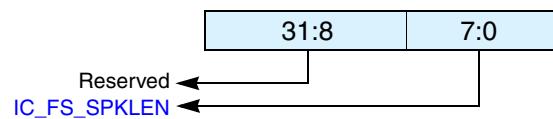


Table 6-44 IC_FS_SPKLEN Register Fields

Bits	Name	R/W	Description
31:8	Reserved		
7:0	<i>IC_FS_SPKLEN</i>	R/W	<p>This register must be set before any I²C bus transaction can take place to ensure stable operation. This register sets the duration, measured in <i>ic_clk</i> cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic; for more information, refer to “Spike Suppression” on page 64.</p> <p>This register can be written only when the I²C interface is disabled, which corresponds to IC_ENABLE[0] being set to 0. Writes at other times have no effect.</p> <p>The minimum valid value is 1; hardware prevents values less than this being written, and if attempted, results in 1 being set.</p> <p>Reset value: IC_DEFAULT_FS_SPKLEN configuration parameter</p>

6.3.42 IC_HS_SPKLEN

- **Name:** I²C HS Spike Suppression Limit Register
- **Size:** 8 bits
- **Address Offset:** 0xA4
- **Read/Write Access:** Read/Write
- **Dependency:** This register is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1).

This register is used to store the duration, measured in *ic_clk* cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in HS mode. The relevant I²C requirement is tSP (Table 6) as detailed in the *I²C Bus Specification*. This register must be programmed with a minimum value of 1 and is implemented only if the component is configured to support HS mode; that is, if the IC_MAX_SPEED_MODE parameter is set to 3.

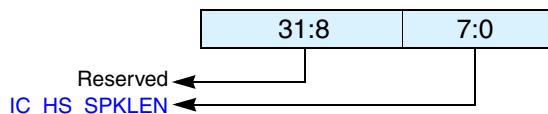


Table 6-45 IC_HS_SPKLEN Register Fields

Bits	Name	R/W	Description
31:8	Reserved		
7:0	IC_HS_SPKLEN	R/W	<p>This register must be set before any I²C bus transaction can take place to ensure stable operation. This register sets the duration, measured in <i>ic_clk</i> cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic; for more information, refer to “Spike Suppression” on page 64.</p> <p>This register can be written only when the I²C interface is disabled, which corresponds to IC_ENABLE[0] being set to 0. Writes at other times have no effect.</p> <p>The minimum valid value is 1; hardware prevents values less than this being written, and if attempted, results in 1 being set.</p> <p>This register is implemented only if the component is configured to support HS mode; that is, if the IC_MAX_SPEED_MODE parameter is set to 3.</p> <p>Reset value: IC_DEFAULT_HS_SPKLEN configuration parameter</p>

6.3.43 IC_CLR_RESTART_DET

- **Name:** Clear RESTART_DET Interrupt Register
- **Size:** 1 bit
- **Address Offset:** 0xA8
- **Read/Write Access:** Read



Table 6-46 IC_CLR_RESTART_DET Register Fields

Bits	Name	R/W	Description
31:1	Reserved	N/A	Reserved
0	CLR_RESTART_DET	R	<p>Read this register to clear the RESTART_DET interrupt (bit 12) of the IC_RAW_INTR_STAT register.</p> <p>Dependencies: This register is present only when IC_SLV_RESTART_DET_EN = 1.</p> <p>Reset value: 0x0</p>

6.3.44 IC_COMP_PARAM_1

- **Name:** Component Parameter Register 1
- **Size:** 32 bits
- **Address Offset:** 0xf4
- **Read/Write Access:** Read

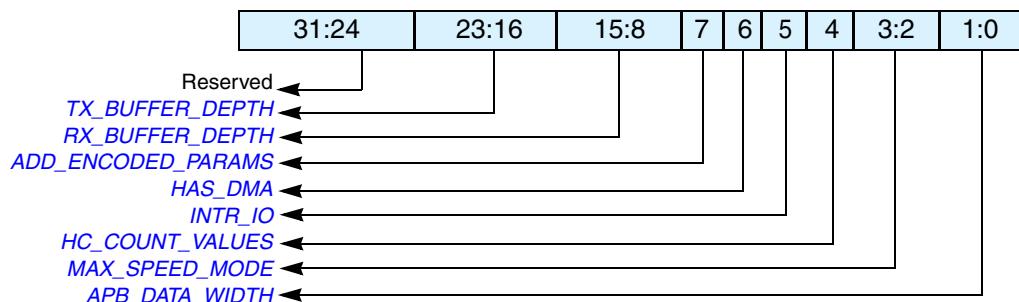


Table 6-47 IC_COMP_PARAM_1 Register Fields

Bits	Name	R/W	Description
Note This is a constant read-only register that contains encoded information about the component's parameter settings. The reset value depends on coreConsultant parameter(s).			
31:24	Reserved	N/A	Reserved
23:16	<i>TX_BUFFER_DEPTH</i>	R	<p>The value of this register is derived from the IC_TX_BUFFER_DEPTH coreConsultant parameter.</p> <ul style="list-style-type: none"> ■ 0x00 = Reserved ■ 0x01 = 2 ■ 0x02 = 3 ... ■ 0xFF = 256
15:8	<i>RX_BUFFER_DEPTH</i>	R	<p>The value of this register is derived from the IC_RX_BUFFER_DEPTH coreConsultant parameter. For a description of this parameter, see Table 4-1 on page 105.</p> <ul style="list-style-type: none"> ■ 0x00 = Reserved ■ 0x01 = 2 ■ 0x02 = 3 ... ■ 0xFF = 256

Table 6-47 IC_COMP_PARAM_1 Register Fields (Continued)

Bits	Name	R/W	Description
7	<i>ADD_ENCODED_PARAMS</i>	R	<p>The value of this register is derived from the IC_ADD_ENCODED_PARAMS coreConsultant parameter. For a description of this parameter, see Table 4-1 on page 105. Reading 1 in this bit means that the capability of reading these encoded parameters via software has been included. Otherwise, the entire register is 0 regardless of the setting of any other parameters that are encoded in the bits.</p> <ul style="list-style-type: none"> ■ 0: False ■ 1: True
6	<i>HAS_DMA</i>	R	<p>The value of this register is derived from the IC_HAS_DMA coreConsultant parameter. For a description of this parameter, see Table 4-1 on page 105.</p> <ul style="list-style-type: none"> ■ 0: False ■ 1: True
5	<i>INTR_IO</i>	R	<p>The value of this register is derived from the IC_INTR_IO coreConsultant parameter. For a description of this parameter, see Table 4-1 on page 105.</p> <ul style="list-style-type: none"> ■ 0: Individual ■ 1: Combined
4	<i>HC_COUNT_VALUES</i>	R	<p>The value of this register is derived from the IC_HC_COUNT_VALUES coreConsultant parameter. For a description of this parameter, see Table 4-1 on page 105.</p> <ul style="list-style-type: none"> ■ 0: False ■ 1: True
3:2	<i>MAX_SPEED_MODE</i>	R	<p>The value of this register is derived from the IC_MAX_SPEED_MODE coreConsultant parameter. For a description of this parameter, see Table 4-1 on page 105.</p> <ul style="list-style-type: none"> ■ 0x0 = Reserved ■ 0x1 = Standard ■ 0x2 = Fast ■ 0x3 = High <p>Dependency: This field is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1)</p>
1:0	<i>APB_DATA_WIDTH</i>	R	<p>The value of this register is derived from the APB_DATA_WIDTH coreConsultant parameter. For a description of this parameter, see Table 4-1 on page 105.</p> <ul style="list-style-type: none"> ■ 0x0 = 8 bits ■ 0x1 = 16 bits ■ 0x2 = 32 bits ■ 0x3 = Reserved

6.3.45 IC_COMP_VERSION

- **Name:** I²C Component Version Register
- **Size:** 32 bits
- **Address Offset:** 0xf8
- **Read/Write Access:** Read

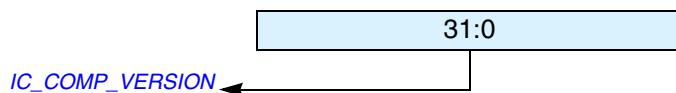


Table 6-48 IC_COMP_VERSION Register Fields

Bits	Name	R/W	Description
31:0	IC_COMP_VERSION	R	Specific values for this register are described in the Releases Table in the AMBA 2 release notes

6.3.46 IC_COMP_TYPE

- **Name:** I²C Component Type Register
- **Size:** 32 bits
- **Address Offset:** 0xfc
- **Read/Write Access:** Read

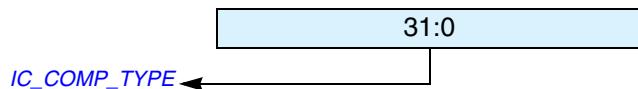


Table 6-49 IC_COMP_TYPE Register Fields

Bits	Name	R/W	Description
31:0	IC_COMP_TYPE	R	Designware Component Type number = 0x44_57_01_40. This assigned unique hex value is constant and is derived from the two ASCII letters "DW" followed by a 16-bit unsigned number.

6.3.47 IC_SCL_STUCK_AT_LOW_TIMEOUT

- **Name:** I²C SCL Stuck at Low Timeout
- **Size:** 32 bits
- **Address Offset:** 0xAC
- **Read/Write Access:** Read/Write
- **Dependencies:** This register is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE = 1).

This register is used to store the duration, measured in ic_clk cycles, used to generate an Interrupt (SCL_STUCK_AT_LOW) if SCL is held low for the IC_SCL_STUCK_LOW_TIMEOUT duration.

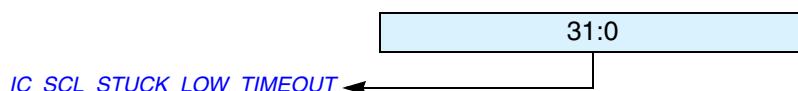


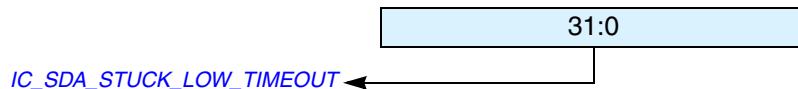
Table 6-50 IC_SCL_STUCK_AT_LOW_TIMEOUT Register Field

Bits	Name	R/W	Description
31:0	IC_SCL_STUCK_LOW_TIMEOUT	R/W	DW_apb_i2c generates the interrupt to indicate SCL stuck at low if it detects the SCL stuck at low for the IC_SCL_STUCK_LOW_TIMEOUT in units of ic_clk period. Reset Value: IC_SCL_STUCK_TIMEOUT_DEFAULT

6.3.48 IC_SDA_STUCK_AT_LOW_TIMEOUT

- **Name:** I²C SDA Stuck at Low Timeout
- **Size:** 32 bits
- **Address Offset:** 0xB0
- **Read/Write Access:** Read/Write
- **Dependencies:** This register is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1).

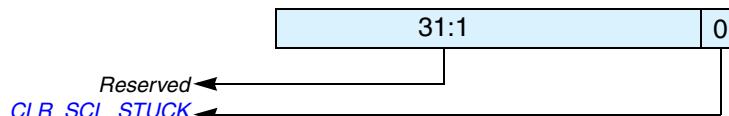
This register is used to store the duration, measured in ic_clk cycles, used to recover the Data (SDA) line through sending SCL pulses if SDA is held low for the mentioned duration.

**Table 6-51 IC_SDA_STUCK_AT_LOW_TIMEOUT Register Field**

Bits	Name	R/W	Description
31:0	IC_SDA_STUCK_LOW_TIMEOUT	R/W	DW_apb_i2c initiates the recovery of SDA line through enabling the SDA_STUCK_RECOVERY_EN (IC_ENABLE[3]) register bit, if it detects the SDA stuck at low for the IC_SDA_STUCK_LOW_TIMEOUT in units of ic_clk period. Reset Value: IC_SDA_STUCK_TIMEOUT_DEFAULT

6.3.49 IC_CLR_SCL_STUCK_DET

- **Name:** Clear SCL Stuck at Low Detect Interrupt Register
- **Size:** 1 bit
- **Address Offset:** 0xB4
- **Read/Write Access:** Read
- **Dependencies:** This register is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1).

**Table 6-52 IC_CLR_SCL_STUCK_DET Register Fields**

Bits	Name	R/W	Description
31:1	Reserved	N/A	Reserved
0	CLR_SCL_STUCK	R	Read this register to clear the SCL_STUCK_DET interrupt (bit 14) of the IC_RAW_INTR_STAT register. Reset value: 0x0

6.3.50 IC_DEVICE_ID

- **Name:** I²C Device ID
- **Size:** 24 bits
- **Address Offset:** 0xb8
- **Read/Write Access:** Read
- **Dependencies:** This register is not applicable in Ultra-Fast speed mode (IC_ULTRA_FAST_MODE=1).

This register contains the Device-ID of the component, which includes 12 bits of manufacturer name, 9 bits of part identification and 3 bits of die-version.

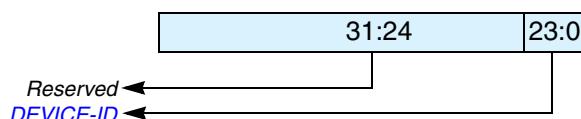


Table 6-53 IC_DEVICE_ID Register Fields

Bits	Name	R/W	Description
31:24	Reserved	NA	Reserved
23:0	DEVICE-ID	R	Contains the Device-ID of the component assigned through the configuration parameter IC_DEVICE_ID_VALUE Reset Value: IC_DEVICE_ID_VALUE

6.3.51 IC_UFM_SCL_HCNT

- **Name:** Ultra-Fast mode I²C Clock High Count Register
- **Size:** 16 bits
- **Address Offset:** 0x14
- **Read/Write Access:** Read/Write
- **Dependencies:** This register is present only if parameter IC_ULTRA_FAST_MODE is set to 1.

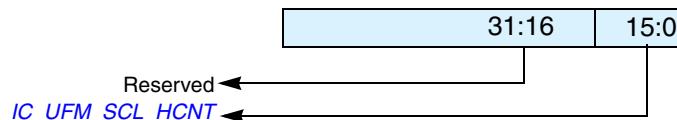


Table 6-54 Ultra-Fast Mode SCL High Counter Register Field Description

Bits	Name	R/W	Description
31:16	Reserved	NA	Reserved
15:0	IC_UFM_SCL_HCNT	R/W ¹	<p>This register must be set before any I²C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for Ultra-Fast speed.</p> <p>This register can be written only when the I²C interface is disabled which corresponds to IC_ENABLE[0] being set to 0. Writes at other times have no effect.</p> <p>For designs with APB_DATA_WIDTH = 8, the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first and then the upper byte is programmed. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.</p> <p>Reset value: IC_UFM_SCL_HIGH_COUNT configuration parameter</p>

¹Read-only if IC_HC_COUNT_VALUES = 1.

6.3.52 IC_UFM_SCL_LCNT

- Name:** Ultra-Fast mode I²C Clock Low Count Register
- Size:** 16 bits
- Address Offset:** 0x18
- Read/Write Access:** Read
- Dependencies:** This register is present only if parameter IC_ULTRA_FAST_MODE is set to 1.

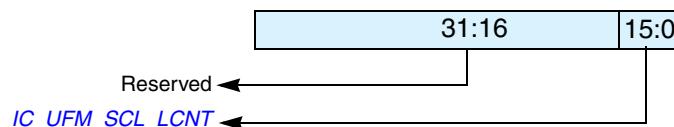


Table 6-55 Ultra-Fast Mode SCL Low Counter Register Field Description

Bits	Name	R/W	Description
31:16	Reserved	NA	Reserved
15:0	IC_UFM_SCL_LCNT	R/W ¹	<p>This register must be set before any I²C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low-period count for Ultra-Fast speed.</p> <p>This register can be written only when the I²C interface is disabled which corresponds to IC_ENABLE[0] being set to 0. Writes at other times have no effect.</p> <p>For designs with APB_DATA_WIDTH = 8, the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed and then the upper byte is programmed. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.</p> <p>Reset value: IC_UFM_SCL_LOW_COUNT configuration parameter</p>

¹Read-only if IC_HC_COUNT_VALUES = 1.

6.3.53 IC_UFM_SPKLEN

- Name:** I²C Ultra-Fast mode Spike suppression Register
- Size:** 8 bits
- Address Offset:** 0xA0
- Read/Write Access:** Read/Write
- Dependencies:** This register is present only if parameter IC_ULTRA_FAST_MODE is set to 1.

This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in Ultra-Fast mode. The relevant I²C

requirement is tSP as detailed in the I2C Bus Specification. This register must be programmed with a minimum value of 1.

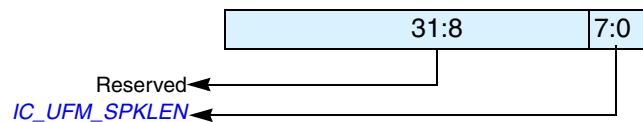


Table 6-56 UFM Spike Suppression Register

Bits	Name	R/W	Description
31:8	Reserved	NA	Reserved
7:0	IC_UFM_SPKLEN	R/W	<p>This register must be set before any I2C bus transaction can occur to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic.</p> <p>This register can be written only when the I2C interface is disabled, which corresponds to IC_ENABLE[0] being set to 0. Writes at other times have no effect.</p> <p>The minimum valid value is 1; hardware prevents values less than this being written, and if attempted, results in 1 being set.</p> <p>Reset value: IC_DEFAULT_UFM_SPKLEN configuration parameter.</p>

6.3.54 IC_UFM_TBUF_CNT

- **Name:** Ultra-Fast mode TBuf Idle Count Register
- **Size:** 16 bits
- **Address Offset:** 0x1c
- **Read/Write Access:** Read/Write
- **Dependencies:** This register is present only if parameter IC_ULTRA_FAST_MODE is set to 1.

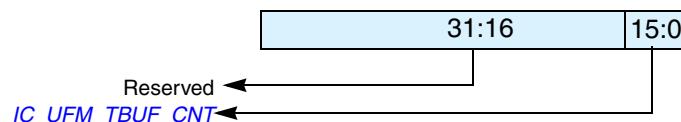


Table 6-57 Ultra-Fast Mode Tbuf Counter Register Field Description

Bits	Name	R/W	Description
31:16	Reserved	NA	Reserved
15:0	IC_UFM_TBUF_CNT	R/W ¹	<p>This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the tBuf Idle time count for Ultra-Fast speed.</p> <p>This register can be written only when the I2C interface is disabled which corresponds to IC_ENABLE[0] being set to 0. Writes at other times have no effect.</p> <p>For designs with APB_DATA_WIDTH = 8, the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first and then the upper byte is programmed. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only.</p> <p>NOTE:</p> <ul style="list-style-type: none"> ■ The DW_apb_i2c will add 9 ic_clks after tBuf time is expired to generate START on the Bus. <p>Reset value: IC_UFM_TBUF_CNT_DEFAULT configuration parameter</p>

¹Read-only if IC_HC_COUNT_VALUES = 1.

6.3.55 IC_SMBUS_CLOCK_LOW_SEXT

- **Name:** SMBUS Slave Clock Extend Timeout Register
- **Size:** 32 bits
- **Address Offset:** 0xBC
- **Read/Write Access:** Read/Write

This register contains the Timeout value used to determine the Slave Clock Extend Timeout in one transfer (from START to STOP). This register can be written only when the DW_apb_i2c is disabled, which corresponds to IC_ENABLE[0] being set to 0. This register is present only if configuration parameter IC_SMBUS is set to 1.

This register is used to store the duration, measured in ic_clk cycles, used to detect the slave clock extend timeout if slave extends the clock (SCL) for the mentioned duration.



Table 6-58 IC_SMBUS_CLOCK_LOW_SEXT Register Field Description

Bits	Name	R/W	Description
31:0	SMBUS_CLK_LOW_SEXT_TIMOUT	R/W	<p>This field is used to detect the Slave Clock Extend timeout (tLOW:SEXT) in master mode extended by the slave device in one message from the initial START to the STOP.</p> <p>The values in this register are in units of ic_clk period.</p> <p>Reset Value: IC_SMBUS_CLOCK_LOW_SEXT_DEFAULT</p>

6.3.56 IC_SMBUS_CLOCK_LOW_MEXT

- **Name:** SMBUS Master extend clock Timeout Register
- **Size:** 32 bits
- **Address Offset:** 0xC0
- **Read/Write Access:** Read/Write

This register contains the Timeout value used to determine the Master Clock Extend Timeout in one byte of transfer. This register can be written only when the DW_apb_i2c is disabled, which corresponds to IC_ENABLE[0] being set to 0. This register is present only if configuration parameter IC_SMBUS is set to 1.

This register is used to store the duration, measured in ic_clk cycles, used to detect the Master clock extend timeout if Master extends the clock (SCL) for the mentioned duration.

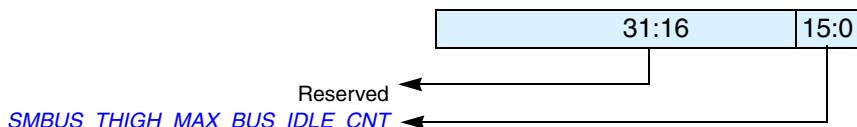
**Table 6-59 SMBUS Master extend clock Timeout Register Field Description**

Bits	Name	R/W	Description
31:0	SMBUS_CLK_LOW_MEXT_TI MEOUT	R/W	<p>This field is used to detect the Master extend SMBus clock (SCL) timeout defined from START-to-ACK, ACK-to-ACK, or ACK-to-STOP in Master mode.</p> <p>The values in this register are in units of ic_clk period.</p> <p>Reset Value: IC_SMBUS_CLOCK_LOW_SEXT_DEFAULT</p>

6.3.57 IC_SMBUS_THIGH_MAX_IDLE_COUNT

- **Name:** SMBus Thigh MAX Bus-Idle count Register
- **Size:** 16 bits
- **Address Offset:** 0xC4
- **Read/Write Access:** Read/Write

This register programs the Bus-idle time period used when a master has been dynamically added to the bus or when a master has generated a clock reset on the bus. This register is used to store the duration, measured in ic_clk cycles, used to detect the Bus Idle condition if SCL and SDA are held high for the mentioned duration. This register can be written only when the DW_apb_i2c is disabled, which corresponds to IC_ENABLE[0] being set to 0. This register is present only if configuration parameter IC_SMBUS is set to 1.

**Table 6-60 SMBus Thigh MAX Bus-Idle count Register Field Descriptions**

Bits	Name	R/W	Description
31:16	Reserved	NA	Reserved
15:0	SMBUS_THIGH_MAX_BUS_I DLE_CNT	R/W	<p>This field is used to set the required Bus-Idle time period used when a master has been dynamically added to the bus and may not have detected a state transition on the SMBCLK or SMBDAT lines.</p> <p>In this case, the master must wait to ensure that a transfer is not currently in progress.</p> <p>The values in this register are in units of ic_clk period.</p> <p>Reset value: IC_SMBUS_RST_IDLE_CNT_DEFAULT</p>

6.3.58 IC_SMBUS_INTR_STAT

- **Name:** I2C SMBUS Interrupt Status Register
- **Size:** 32 bits
- **Address Offset:** 0xC8
- **Read/Write Access:** Read

Each bit in this register has a corresponding mask bit in the IC_SMBUS_INTR_MASK register. These bits are cleared by writing the matching SMBus interrupt clear register (IC_CLR_SMBUS_INTR) bits. The unmasked raw versions of these bits are available in the IC_SMBUS_RAW_INTR_STAT register.

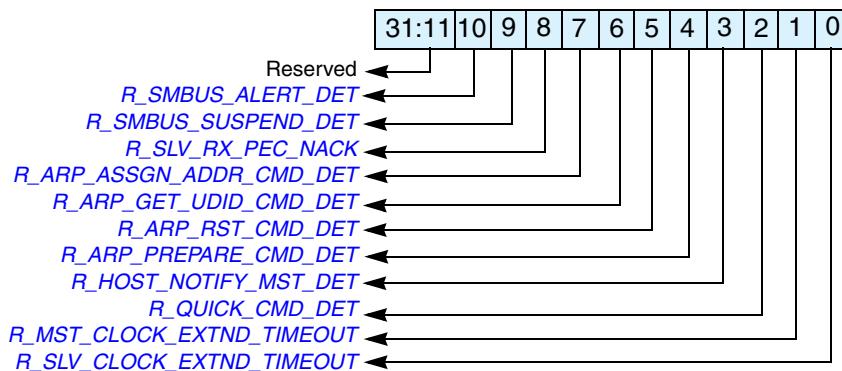


Table 6-61 I2C SMBUS Interrupt Status Register Field Descriptions

Bits	Name	R/W	Description
31:11	Reserved	NA	Reserved
10	R_SMBUS_ALERT_DET	R	See IC_SMBUS_INTR_RAW_STATUS for a detailed description of this bit. Reset value: 0x0
9	R_SMBUS_SUSPEND_DET	R	See IC_SMBUS_INTR_RAW_STATUS for a detailed description of this bit. Reset value: 0x0
8	R_SLV_RX_PEC_NACK	R	See IC_SMBUS_INTR_RAW_STATUS for a detailed description of this bit. Reset value: 0x0
7	R_ARP_ASSGN_ADDR_CMD_DET	R	See IC_SMBUS_INTR_RAW_STATUS for a detailed description of this bit. Reset value: 0x0
6	R_ARP_GET_UDID_CMD_DET	R	See IC_SMBUS_INTR_RAW_STATUS for a detailed description of this bit. Reset value: 0x0

Table 6-61 I2C SMBUS Interrupt Status Register Field Descriptions (Continued)

Bits	Name	R/W	Description
5	R_ARP_RST_CMD_DET	R	See IC_SMBUS_INTR_RAW_STATUS for a detailed description of this bit. Reset value: 0x0
4	R_ARP_PREPARE_CMD_DET	R	See IC_SMBUS_INTR_RAW_STATUS for a detailed description of this bit. Reset value: 0x0
3	R_HOST_NOTIFY_MST_DET	R	See IC_SMBUS_INTR_RAW_STATUS for a detailed description of this bit. Reset value: 0x0
2	R_QUICK_CMD_DET	R	See IC_SMBUS_INTR_RAW_STATUS for a detailed description of this bit. Reset value: 0x0
1	R_MST_CLOCK_EXTND_TIM_EOUT	R	See IC_SMBUS_INTR_RAW_STATUS for a detailed description of this bit. Reset value: 0x0
0	R_SLV_CLOCK_EXTND_TIM_EOUT	R	See IC_SMBUS_INTR_RAW_STATUS for a detailed description of this bit. Reset value: 0x0

6.3.59 IC_SMBUS_INTR_MASK

- **Name:** I2C Interrupt Mask Register
- **Size:** 32 bits
- **Address Offset:** 0xcc
- **Read/Write Access:** Read/Write

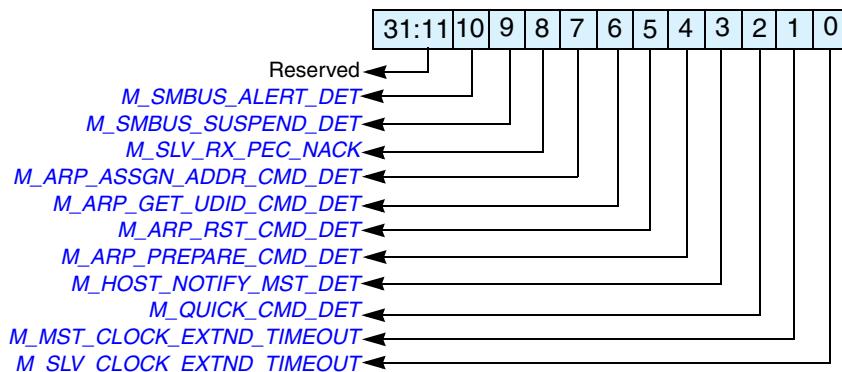


Table 6-62 I2C Interrupt Mask Register Field Descriptions

Bits	Name	R/W	Description
31:11	Reserved	NA	Reserved
10	M_SMBUS_ALERT_DET	R/W	<p>This bit masks the R_SMBUS_ALERT_DET interrupt bit in the IC_SMBUS_INTR_STAT register. This bit is enabled only when IC_SMBUS_SUSPEND_ALERT=1.</p> <p>Reset Value: 0x1</p>
9	M_SMBUS_SUSPEND_DET	R/W	<p>This bit masks the R_SMBUS_SUSPEND_DET interrupt bit in the IC_SMBUS_INTR_STAT register. This bit is enabled only when IC_SMBUS_SUSPEND_ALERT=1.</p> <p>Reset Value: 0x1</p>
8	M_SLV_RX_PEC_NACK	R/W	<p>This bit masks the R_SLV_RX_PEC_NACK interrupt bit in the IC_SMBUS_INTR_STAT register. This bit is enabled only when IC_SMBUS_ARP=1.</p> <p>Reset Value: 0x1</p>
7	M_ARP_ASSGN_ADDR_CMD_DET	R/W	<p>This bit masks the R_ARP_ASSGN_ADDR_CMD_DET interrupt bit in the IC_SMBUS_INTR_STAT register. This bit is enabled only when IC_SMBUS_ARP=1.</p> <p>Reset Value: 0x1</p>
6	M_ARP_GET_UDID_CMD_DET	R/W	<p>This bit masks the R_ARP_GET_UDID_CMD_DET interrupt bit in the IC_SMBUS_INTR_STAT register. This bit is enabled only when IC_SMBUS_ARP=1.</p> <p>Reset Value: 0x1</p>

Table 6-62 I2C Interrupt Mask Register Field Descriptions (Continued)

Bits	Name	R/W	Description
5	M_ARP_RST_CMD_DET	R/W	This bit masks the R_ARP_RST_CMD_DET interrupt bit in the IC_SMBUS_INTR_STAT register. This bit is enabled only when IC_SMBUS_ARP=1. Reset Value: 0x1
4	M_ARP_PREPARE_CMD_DET	R/W	This bit masks the R_ARP_PREPARE_CMD_DET interrupt bit in the IC_SMBUS_INTR_STAT register. This bit is enabled only when IC_SMBUS_ARP=1. Reset Value: 0x1
3	M_HOST_NOTIFY_MST_DET	R/W	This bit masks the R_HOST_NOTIFY_DET interrupt bit in the IC_SMBUS_INTR_STAT register. This bit is enabled only when IC_SMBUS =1. Reset Value: 0x1
2	M_QUICK_CMD_DET	R/W	This bit masks the R_QUICK_CMD_DET interrupt bit in the IC_SMBUS_INTR_STAT register. This bit is enabled only when IC_SMBUS=1. Reset Value: 0x1
1	M_MST_CLOCK_EXTND_TIM EOUT	R/W	This bit masks the R_MST_CLOCK_EXTND_TIMEOUT interrupt bit in the IC_SMBUS_INTR_STAT register. This bit is enabled only when IC_SMBUS=1. Reset Value: 0x1
0	M_SLV_CLOCK_EXTND_TIM EOUT	R/W	This bit masks the R_SLV_CLOCK_EXTND_TIMEOUT interrupt bit in the IC_SMBUS_INTR_STAT register. This bit is enabled only when IC_SMBUS=1. Reset Value: 0x1

6.3.60 IC_SMBUS_INTR_RAW_STATUS

- **Name:** I2C SMBUS Raw Interrupt Status Register
- **Size:** 32 bits
- **Address Offset:** 0xd0
- **Read/Write Access:** Read only

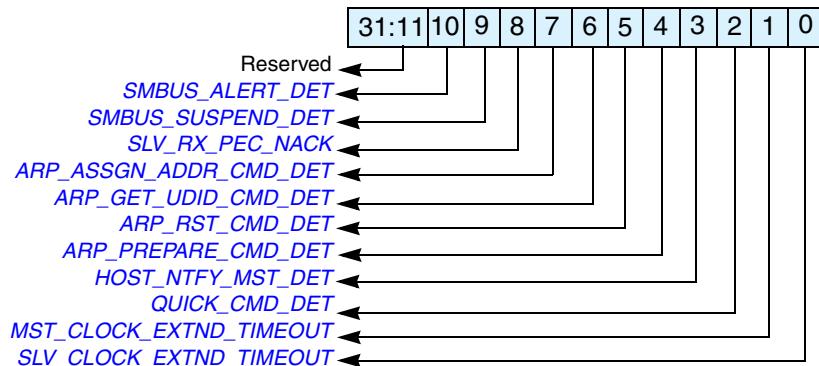


Table 6-63 I2C SMBUS Raw Interrupt Status Register Field Descriptions

Bits	Name	R/W	Description
31:11	Reserved	NA	Reserved
10	SMBUS_ALERT_DET	R	<p>Indicates whether a SMBALERT (ic_smbalert_in_n) signal is driven low by the slave.</p> <p>Dependencies: This register bit is valid only if configuration parameter IC_SMBUS_SUSPEND_ALERT is set to 1.</p> <p>Reset Value: 0x0</p>
9	SMBUS_SUSPEND_DET	R	<p>Indicates whether a SMBSUS (ic_smbsus_in_n) signal is driven low by the Host.</p> <p>Dependencies: This register bit is valid only if configuration parameter IC_SMBUS_SUSPEND_ALERT is set to 1.</p> <p>Reset Value: 0x0</p>
8	SLV_RX_PEC_NACK	R	<p>Indicates whether a Slave generates a NACK for the PEC Byte of the ARP command from the slave.</p> <p>Dependencies: This register bit is valid only if configuration parameter IC_SMBUS_ARP is set to 1.</p> <p>Reset Value: 0x0</p>
7	ARP_ASSGN_ADDR_CMD_DET	R	<p>Indicates whether an Assign Address ARP command has been received.</p> <p>Dependencies: This register bit is valid only if configuration parameter IC_SMBUS_ARP is set to 1.</p> <p>Reset Value: 0x0</p>

Table 6-63 I2C SMBUS Raw Interrupt Status Register Field Descriptions (Continued)

Bits	Name	R/W	Description
6	ARP_GET_UDID_CMD_DET	R	<p>Indicates whether a General or directed Get UDID ARP command has been received.</p> <p>Dependencies: This register bit is valid only if configuration parameter IC_SMBUS_ARP is set to 1.</p> <p>Reset Value: 0x0</p>
5	ARP_RST_CMD_DET	R	<p>Indicates whether a General or Directed Reset ARP command has been received.</p> <p>Dependencies: This register bit is valid only if configuration parameter IC_SMBUS_ARP is set to 1.</p> <p>Reset Value: 0x0</p>
4	ARP_PREPARE_CMD_DET	R	<p>Indicates whether a Prepare to ARP command has been received.</p> <p>Dependencies: This register bit is valid only if configuration parameter IC_SMBUS_ARP is set to 1.</p> <p>Reset Value: 0x0</p>
3	HOST_NTFY_MST_DET	R	<p>Indicates whether a Host Notify command has been received.</p> <p>Dependencies: This register bit is valid only if configuration parameter IC_SMBUS is set to 1.</p> <p>Reset Value: 0x0</p>
2	QUICK_CMD_DET	R	<p>Indicates whether a Quick command has been received on the SMBus interface regardless of whether DW_apb_i2c is operating in slave or master mode. This bit is enabled only when IC_SMBUS=1 is set to 1.</p> <p>Reset Value: 0x0</p>
1	MST_CLOCK_EXTND_TIMEOUT	R	<p>Indicates whether the Master device transaction (START-to-ACK, ACK-to-ACK, or ACK-to-STOP) from START to STOP exceeds IC_SMBUS_CLOCK_LOW_MEXT time in each byte of message. This bit is enabled only when:</p> <ul style="list-style-type: none"> ■ IC_SMBUS=1 ■ IC_CON[0]=1 ■ IC_EMPTYFIFO_HOLD_MASTER_EN=1 or IC_RX_FULL_HLD_BUS_EN=1
0	SLV_CLOCK_EXTND_TIMEOUT	R	<p>Indicates whether the transaction from Slave (that is, from START to STOP) exceeds IC_SMBUS_CLOCK_LOW_SEXT time. This bit is enabled only when</p> <ul style="list-style-type: none"> ■ IC_SMBUS=1 ■ IC_CON[0]=1

6.3.61 IC_CLR_SMBUS_INTR

- **Name:** Clear SMBUS Interrupt Register
- **Size:** 32 bits
- **Address Offset:** 0xD4
- **Read/Write Access:** Write only

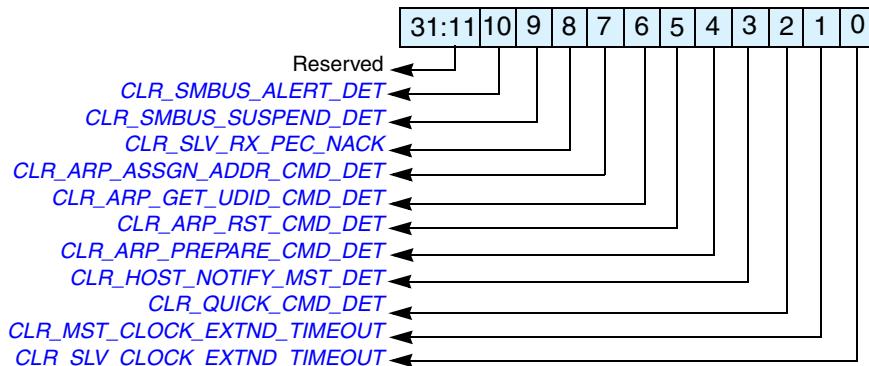


Table 6-64 Clear SMBUS Interrupt Register Field Descriptions

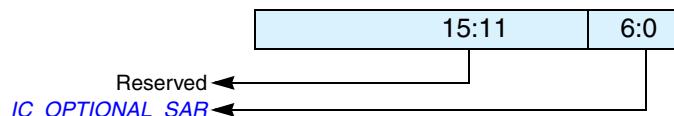
Bits	Name	R/W	Description
31:11	Reserved	NA	Reserved
10	CLR_SMBUS_ALERT_DET	W	Write this register to clear the SMBUS_ALERT_DET interrupt (bit 10) of the IC_SMBUS_RAW_INTR_STAT register. Reset value: 0x0
9	CLR_SMBUS_SUSPEND_DET	W	Write this register to clear the R_SMBUS_SUSPEND_DET interrupt (bit 9) of the IC_SMBUS_RAW_INTR_STAT register. Reset value: 0x0
8	CLR_SLV_RX_PEC_NACK	W	Write this register to clear the SLV_RX_PEC_NACK interrupt (bit 8) of the IC_SMBUS_RAW_INTR_STAT register. Reset value: 0x0
7	CLR_ARP_ASSGN_ADDR_CMD_DET	W	Write this register to clear the ARP_ASSGN_ADDR_CMD_DET interrupt (bit 7) of the IC_SMBUS_RAW_INTR_STAT register. Reset value: 0x0
6	CLR_ARP_GET_UDID_CMD_DET	W	Write this register to clear the ARP_GET_UDID_CMD_DET interrupt (bit 6) of the IC_SMBUS_RAW_INTR_STAT register. Reset value: 0x0
5	CLR_ARP_RST_CMD_DET	W	Write this register to clear the ARP_RST_CMD_DET interrupt (bit 5) of the IC_SMBUS_RAW_INTR_STAT register. Reset value: 0x0

Table 6-64 Clear SMBUS Interrupt Register Field Descriptions (Continued)

Bits	Name	R/W	Description
4	CLR_ARP_PREPARE_CMD_DET	W	Write this register to clear the ARP_PREPARE_CMD_DET interrupt (bit 4) of the IC_SMBUS_RAW_INTR_STAT register. Reset value: 0x0
3	CLR_HOST_NOTIFY_MST_DET	W	Write this register to clear the HOST_NOTIFY_MST_DET interrupt (bit 3) of the IC_SMBUS_RAW_INTR_STAT register. Reset value: 0x0
2	CLR_QUICK_CMD_DET	W	Write this register to clear the QUICK_CMD_DET interrupt (bit 2) of the IC_SMBUS_RAW_INTR_STAT register. Reset value: 0x0
1	CLR_MST_CLOCK_EXTND_TIMEOUT	W	Write this register to clear the MST_CLOCK_EXTND_TIMEOUT interrupt (bit 1) of the IC_SMBUS_RAW_INTR_STAT register. Reset value: 0x0
0	CLR_SLV_CLOCK_EXTND_TIMEOUT	W	Write this register to clear the SLV_CLOCK_EXTND_TIMEOUT interrupt (bit 0) of the IC_SMBUS_RAW_INTR_STAT register. Reset value: 0x0

6.3.62 IC_OPTIONAL_SAR

- **Name:** I2C Optional Slave Address Register
- **Size:** 7 bits
- **Address Offset:** 0xD8
- **Read/Write Access:** Read/Write

**Table 6-65 I2C Optional Slave Address Register Field Descriptions**

Bits	Name	R/W	Description
15:11	Reserved	NA	Reserved
6:0	IC_OPTIONAL_SAR	R/W	Optional Slave address for DW_apb_i2c when operating as a slave in SMBus Mode. Dependencies: This register bit is valid only if configuration parameter IC_OPTIONAL_SAR is set to 1. Reset Value: IC_OPTIONAL_SAR_DEFAULT

Table 6-65 I2C Optional Slave Address Register Field Descriptions (Continued)

Bits	Name	R/W	Description
0	CLR_SLV_CLOCK_EXTND_TI MEOUT	W	Write this register to clear the SLV_CLOCK_EXTND_TIMEOUT interrupt (bit 0) of the IC_SMBUS_RAW_INTR_STAT register. Reset value: 0x0

6.3.63 IC_SMBUS_UDID_LSB

- **Name:** SMBUS ARP UDID LSB Register
- **Size:** 32 bits
- **Address Offset:** 0xDC
- **Read/Write Access:** Read/Write
- **Dependencies:** This register is present only if IC_SMBUS_ARP =1.

This register can be written only when the DW_apb_i2c is disabled, which corresponds to IC_ENABLE[0] being set to 0. This register is present only if configuration parameter IC_SMBUS_ARP is set to 1.

This register is used to store the LSB 32 bit value of Slave UDID register used in Address Resolution Protocol of SMBus.

**Table 6-66 SMBUS ARP UDID LSB Register Field Description**

Bits	Name	R/W	Description
31:0	IC_SMBUS_ARP_UDID_LSB	R/W	This field is used to store the LSB 32 bit value of slave unique device identifier used in Address Resolution Protocol. Reset Value: IC_SMBUS_UDID_LSB_DEFAULT

Internal Parameter Descriptions

Provides a description of the internal parameters that might be indirectly referenced in expressions in the Signals, Parameters, or Registers chapters. These parameters are not visible in the coreConsultant GUI and most of them are derived automatically from visible parameters. **You must not set any of these parameters directly.**

Some expressions might refer to TCL functions or procedures (sometimes identified as **function_of**) that coreConsultant uses to make calculations. The exact formula used by these TCL functions is not provided in this chapter. However, when you configure the core in coreConsultant, all TCL functions and parameters are evaluated completely; and the resulting values are displayed where appropriate in the coreConsultant GUI reports.

Table 7-1 Internal Parameters

Parameter Name	Equals To
IC_ADDR_SLICE_LHS	3'b111
blank	intentionally left blank

8

Programming the DW_apb_i2c

The DW_apb_i2c can be programmed via software registers or the DW_apb_i2c low-level software driver.

8.1 Software Registers

For information about programming the software registers in terms of DW_apb_i2c operation, refer to “Slave Mode Operation” on page 56 and “Master Mode Operation” on page 60. The software registers are described in more detail in “Registers” on page 153.

8.2 Software Drivers

The family of DesignWare Synthesizable Components includes a Driver Kit for the DW_apb_i2c component. This low-level Driver Kit allows you to easily program a DW_apb_i2c component and integrate your code into a larger software system. The Driver Kit provides the following benefits to IP designers:

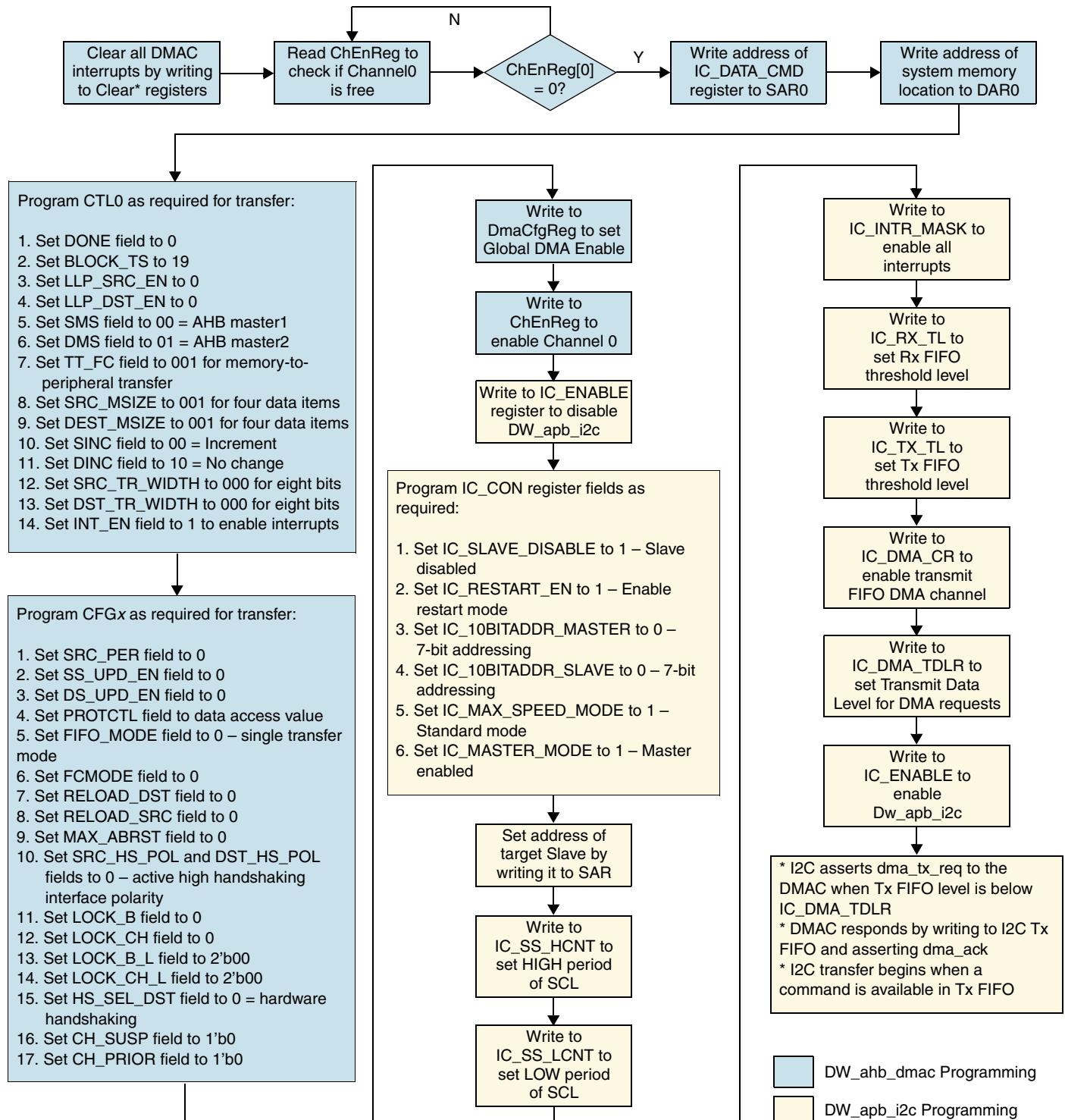
- Proven method of access to DW_apb_i2c minimizing usage errors
- Rapid software development with minimum overhead
- Detailed knowledge of DW_apb_i2c register bit fields not required
- Easy integration of DW_apb_i2c into existing software system
- Programming at register level eliminated

You must purchase a source code license (DWC-APB-Advanced-Source) to use the DW_apb_i2c Driver Kit. However, you can access some Driver Kit files and documentation in \$DESIGNWARE_HOME/drivers/DW_apb_i2c/latest. For more information about the Driver Kit, refer to the [DW_apb_i2c Driver Kit User Guide](#). For more information about purchasing the source code license and obtaining a download of the Driver Kit, contact Synopsys at designware@synopsys.com for details.

8.3 Programming Example

The flow diagram in [Figure 8-1](#) shows an overview of programming the DW_apb_i2c.

Figure 8-1 Flowchart for DW_ahb_dmac and DW_apb_i2c Programming Example





Note When there is at least one entry in the DW_apb_i2c Rx FIFO, the DW_apb_i2c asserts dma_single to the DMAC. When the number of entries in the DW_apb_i2c Rx FIFO reaches IC_DMA_RDLR, the DW_apb_i2c asserts dma_rx_req to the DMAC. In this example, in order to read nineteen data items from the DW_apb_i2c Rx FIFO, the DMAC samples dma_req for three BURST transfers of four beats of size 1 byte each, and it samples dma_single for three SINGLE transfers of size 1 byte each.

The following outlines details regarding reads and writes to/from DW_apb_i2c masters/slaves and VIP master/slaves:

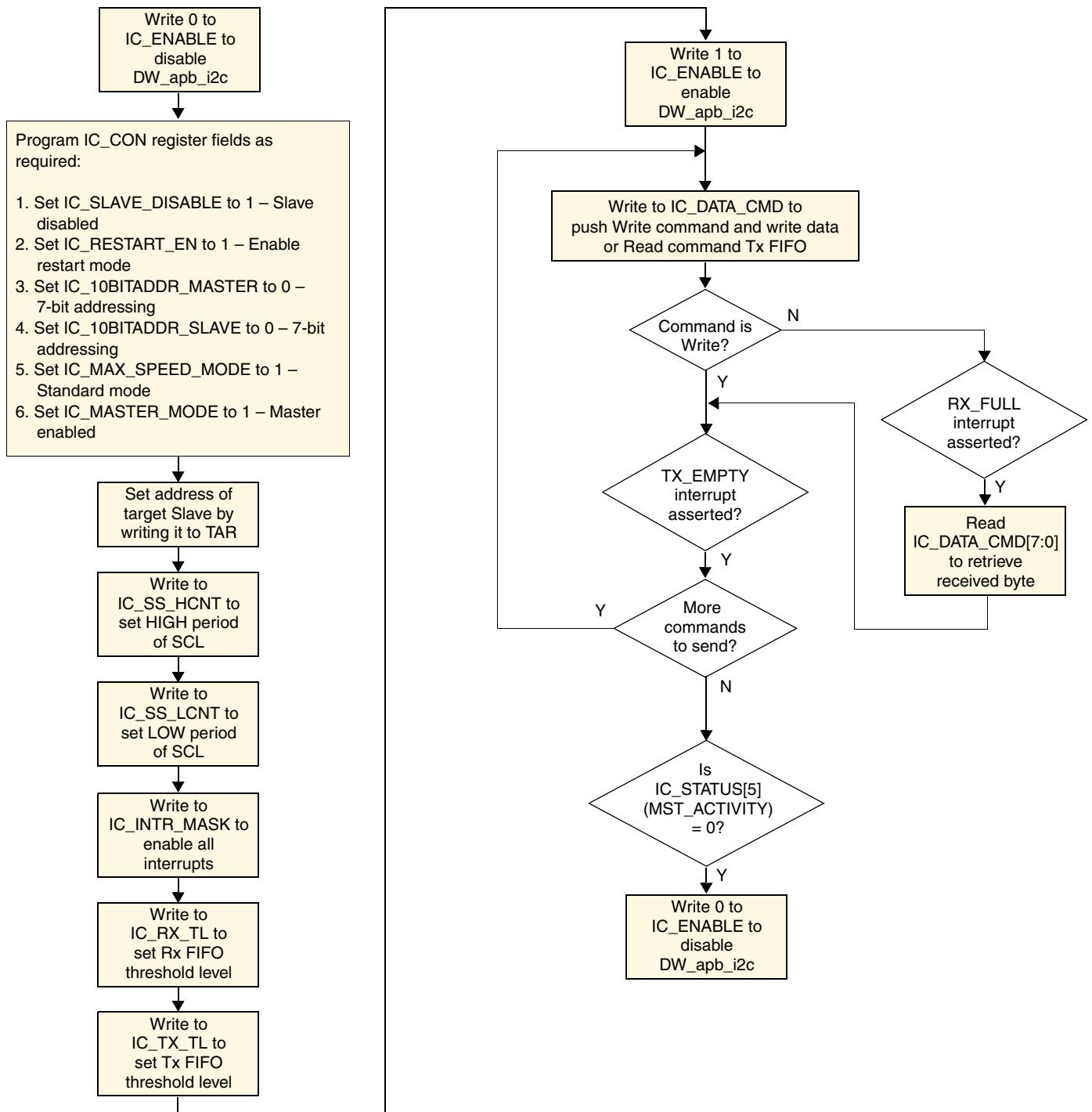
- For DW_apb_i2c master writes to a slave VIP model, bear in mind when using the DMA that you are writing characters from the byte stream. However, for a write, the DW_apb_i2c needs a halfword. To use the DMA, you should write software similar to the following:


```
short int temp_array[];
char * ptr=(char *) temp_array;
foreach byte in bytes {
    store byte ptr++;
    store '0x01' write command ptr++
}
```

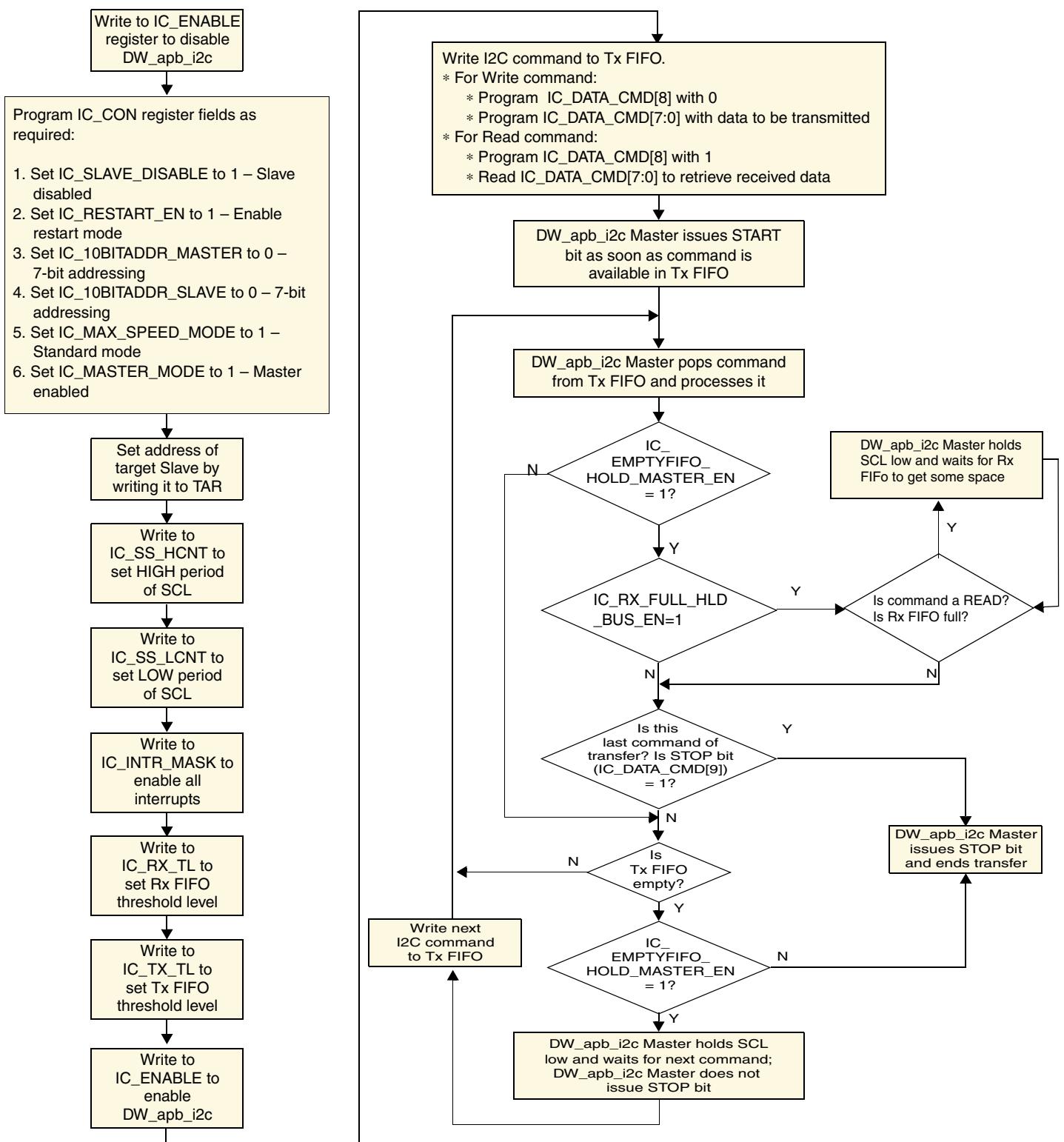
 - a. Program the DMA to read a stream of halfwords from memory and write them to the DW_apb_i2c using the hardware interface.
 - b. Program the DW_apb_i2c to do a write using the transmit DMA.
- For DW_apb_i2c master reads from a slave VIP model:
 - a. Create a read command halfword.
 - b. Program DMA channel 0 to do a fixed read of the read command halfword – that is, no address increment – to the DW_apb_i2c transmit buffer.
 - c. Program DMA channel 1 to read the data from the read buffer and store it in memory.
 - d. Program the DW_apb_i2c to do a master read by setting *both* DMA channels.
- For DW_apb_i2c slave writes from a master VIP model:
 - a. Program the DW_apb_i2c to be a slave with the RX buffer DMA enabled.
 - b. Program the DMA to read the buffer and store the bytes in memory.
- For DW_apb_i2c slave reads from a master VIP model:
 - a. Enable IC_INTR_MASK.RD_REQ; otherwise the DW_apb_i2c will not acknowledge the read.
 - b. When you get the RD_REQ interrupt, program the DMA to write the TX buffer with the read data.
 - c. Program the DW_apb_i2c to enable the TX DMA.

The flow diagram in [Figure 8-2](#) shows a programming example for the DW_apb_i2c Master.

Figure 8-2 Flowchart for DW_apb_i2c Master



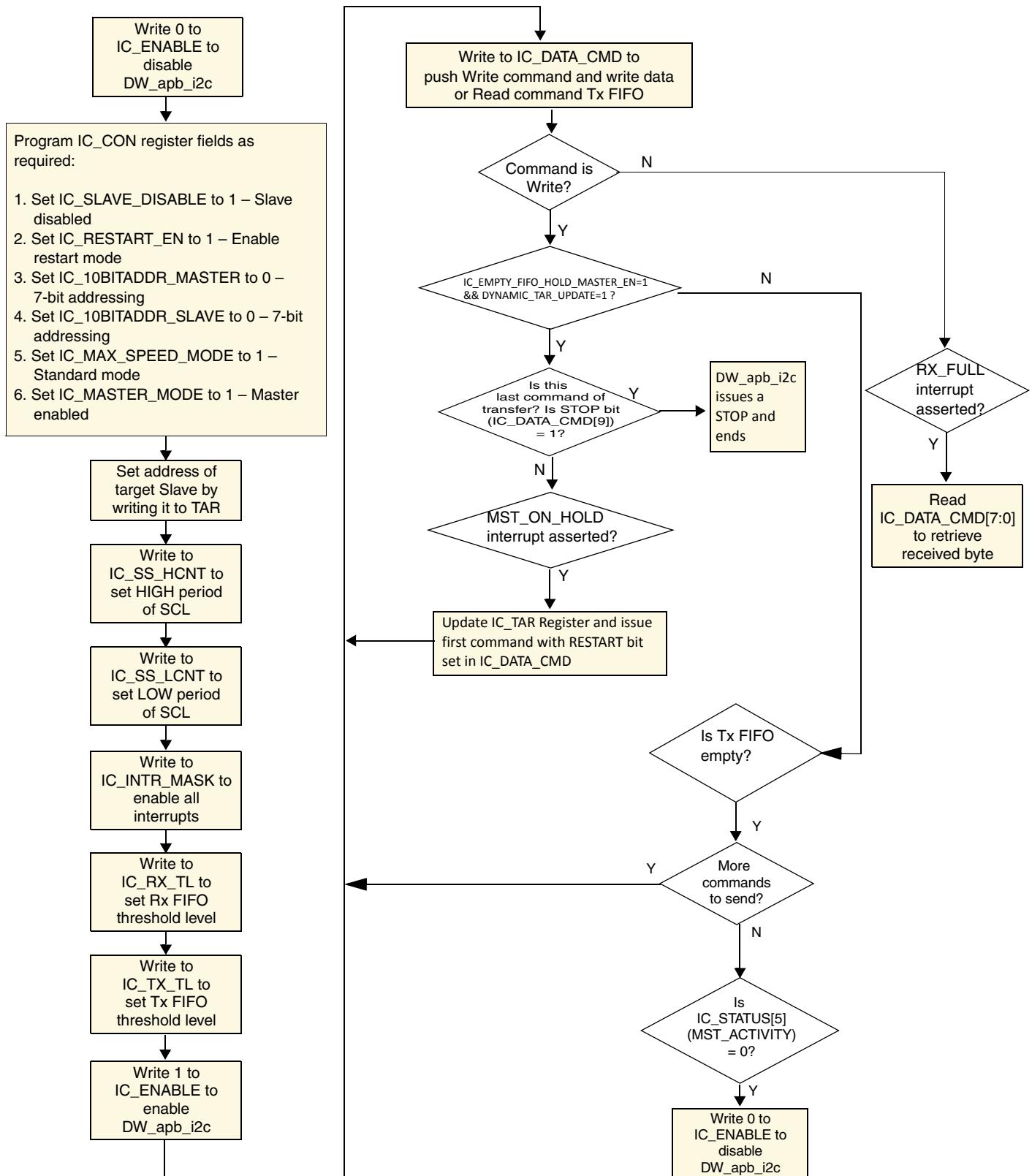
The flow diagram in [Figure 8-3](#) shows a programming example for the DW_apb_i2c master in standard mode, fast mode, or fast mode plus with 7-bit addressing.

Figure 8-3 Flowchart for DW_apb_i2c Master in Standard Mode, Fast Mode, or Fast Mode Plus

The flow diagram in [Figure 8-4](#) shows a programming example for DW_apb_i2c as master with TAR address update. This flow shows how the MST_ON_HOLD interrupt is used when the software needs information from the hardware to safely update the TAR address.

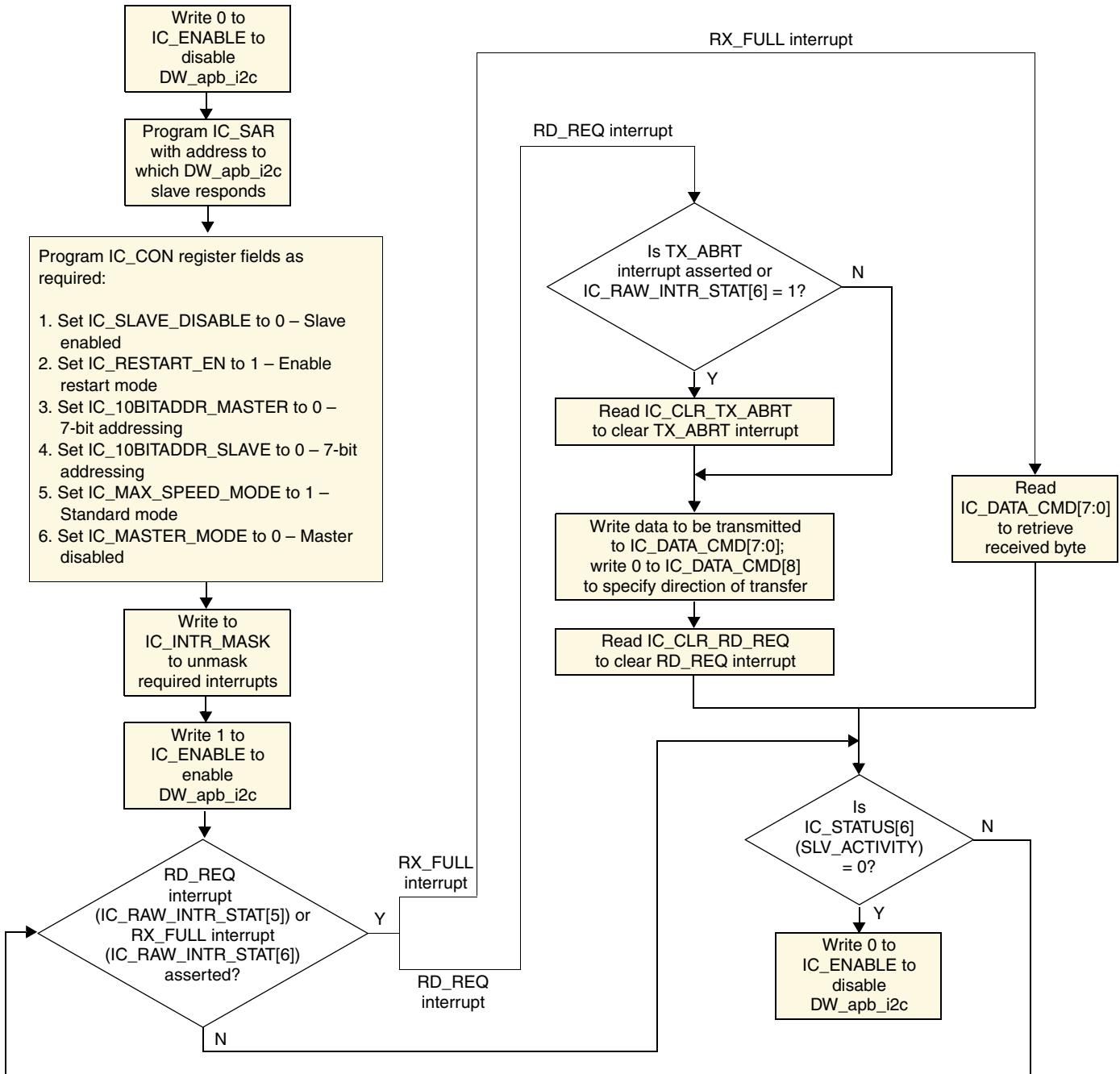


When the software has full knowledge of when it is safe to update the TAR address without requiring information from hardware, the MST_ON_HOLD interrupt is not required to update the TAR address.

Figure 8-4 Flowchart for DW_apb_i2c Master with TAR Address Update

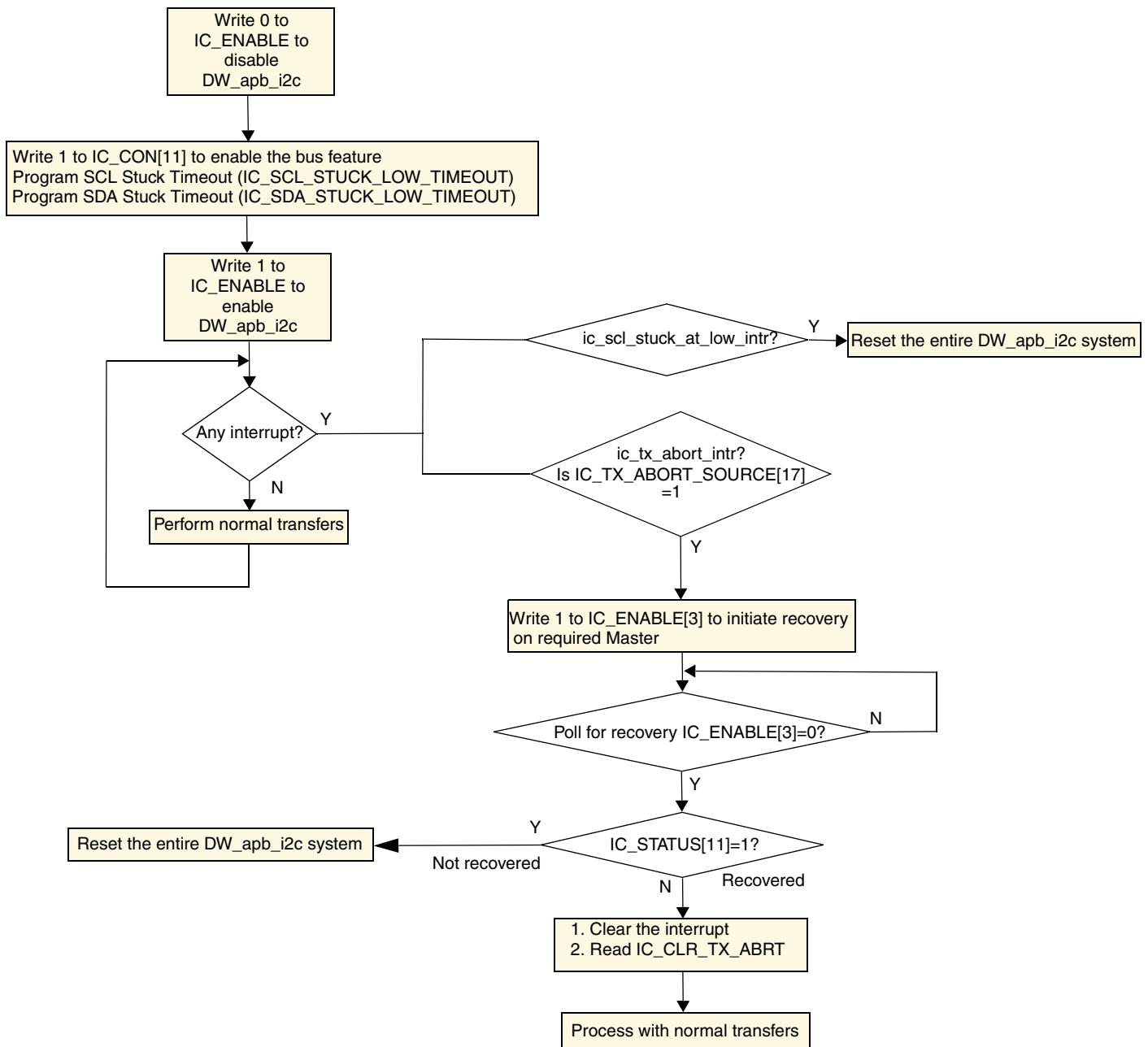
The flow diagram in [Figure 8-5](#) shows a programming example for the DW_apb_i2c Slave in standard mode, fast mode, or fast mode plus with 7-bit addressing.

Figure 8-5 Flowchart for DW_apb_i2c Slave in Standard Mode, Fast Mode, or Fast Mode Plus with 7-bit Addressing



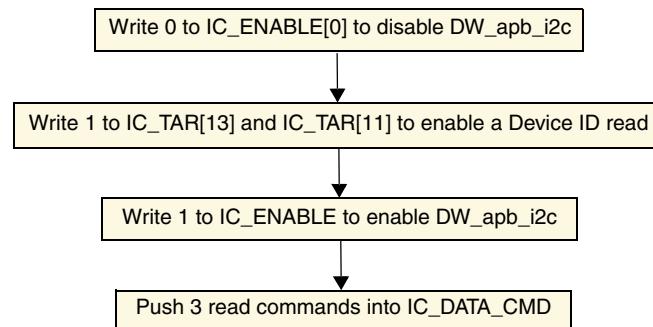
8.4 Programming Flow for SCL and SDA Bus Recovery

The flow diagram in [Figure 8-6](#) shows a programming example for SCL and SDA bus recovery.

Figure 8-6 Flowchart for SCL and SDA Bus Recovery

8.5 Programming Flow for Reading the Device ID

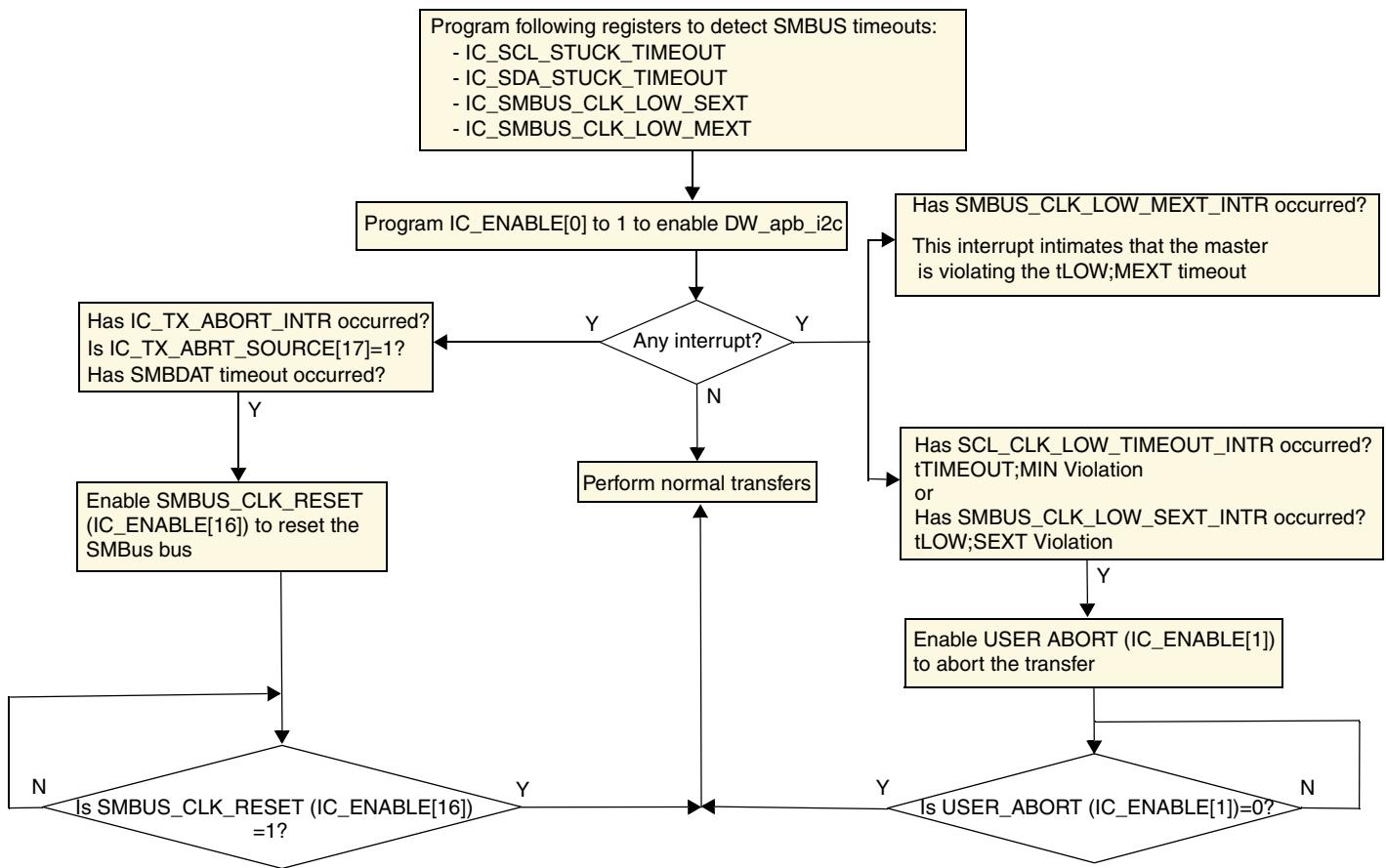
Figure 8-7 shows a programming flow in the master to initiate a Device ID read.

Figure 8-7 Flowchart for Reading a Device ID

As the Device ID consists of 3 bytes, the user must issue 3 read commands in IC_DATA_CMD register. One read command populates one byte of Device ID in RX FIFO. If more than 3 commands are issued, the Device ID will roll back.

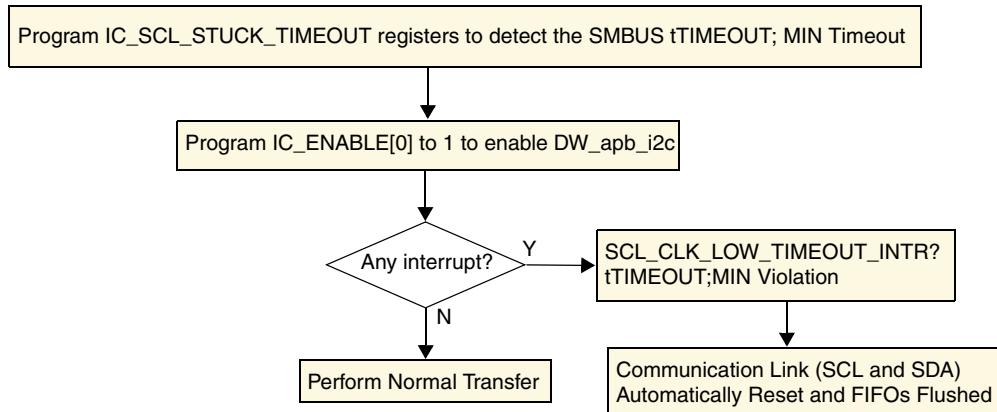
8.6 Programming Flow for SMBUS Timeout in Master Mode

Figure 8-8 shows a programming flow for SMBus timeout in master mode.

Figure 8-8 SMBUS Timeout Programming Flow in Master Mode

8.7 Programming Flow for SMBUS Timeout in Slave Mode

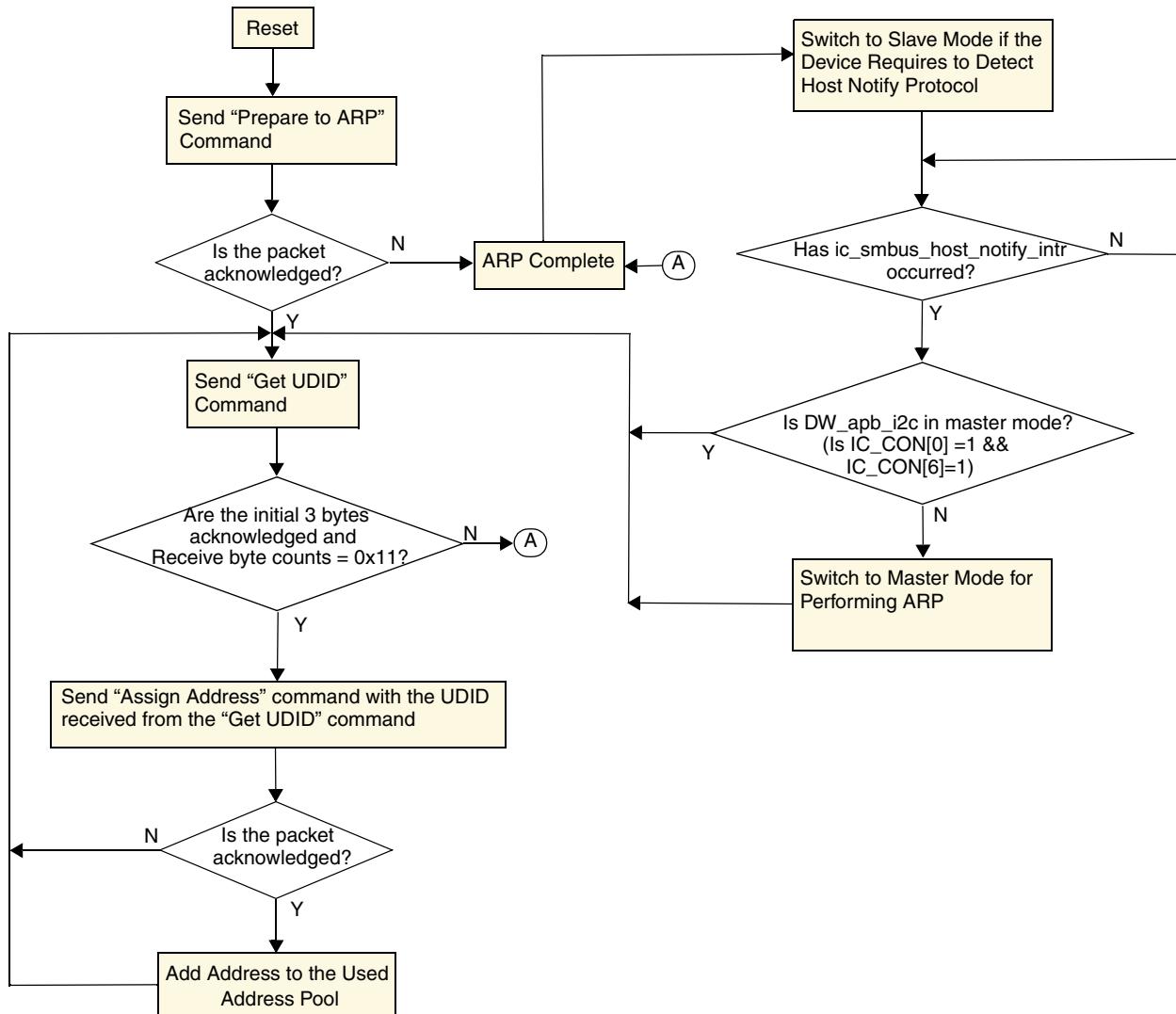
Figure 8-9 shows a programming flow for SMBus timeout in slave mode.

Figure 8-9 SMBUS Timeout Programming Flow in Slave Mode

8.8 ARP Master Programming Flow

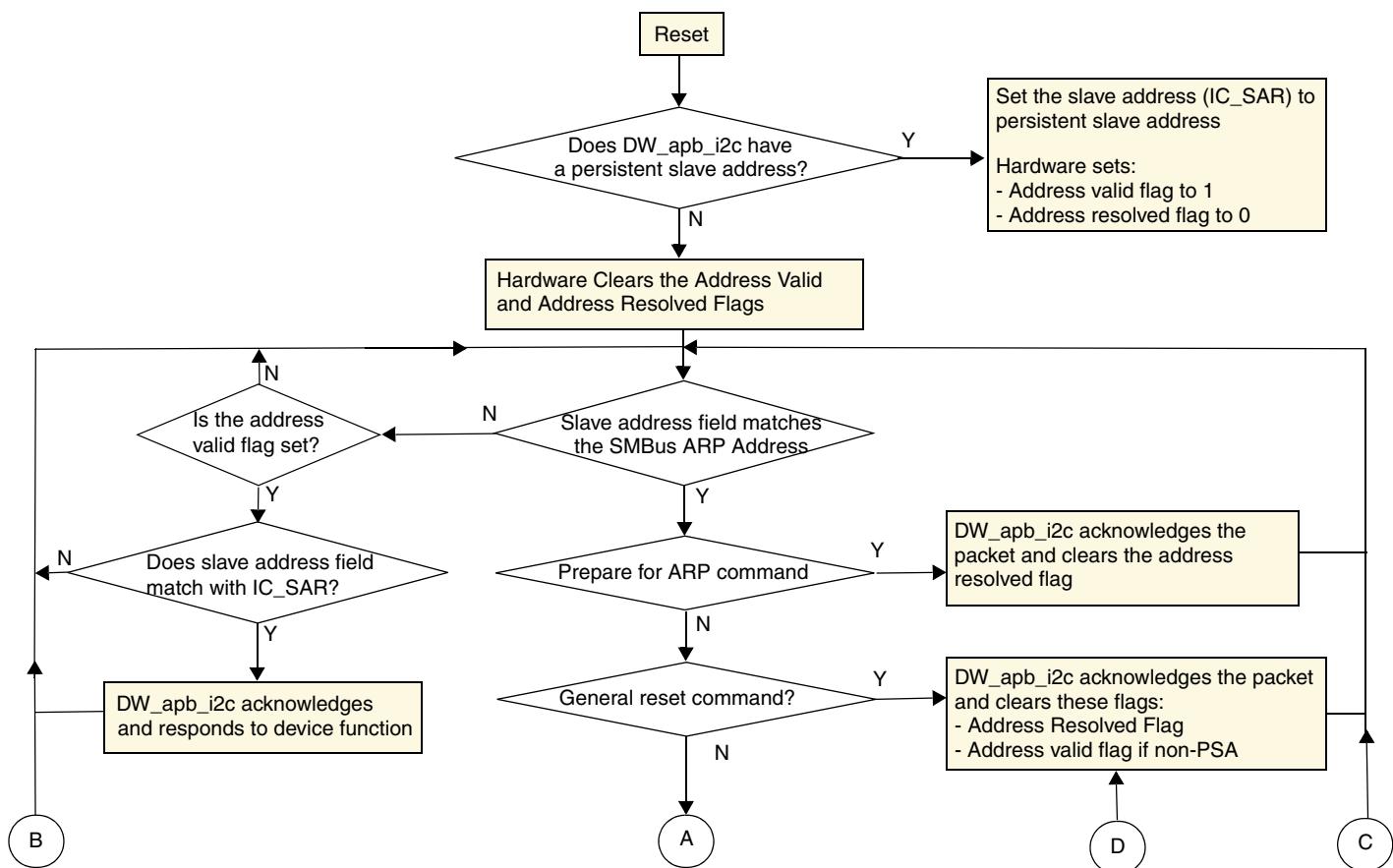
Figure 8-10 shows the programming flow for an ARP master.

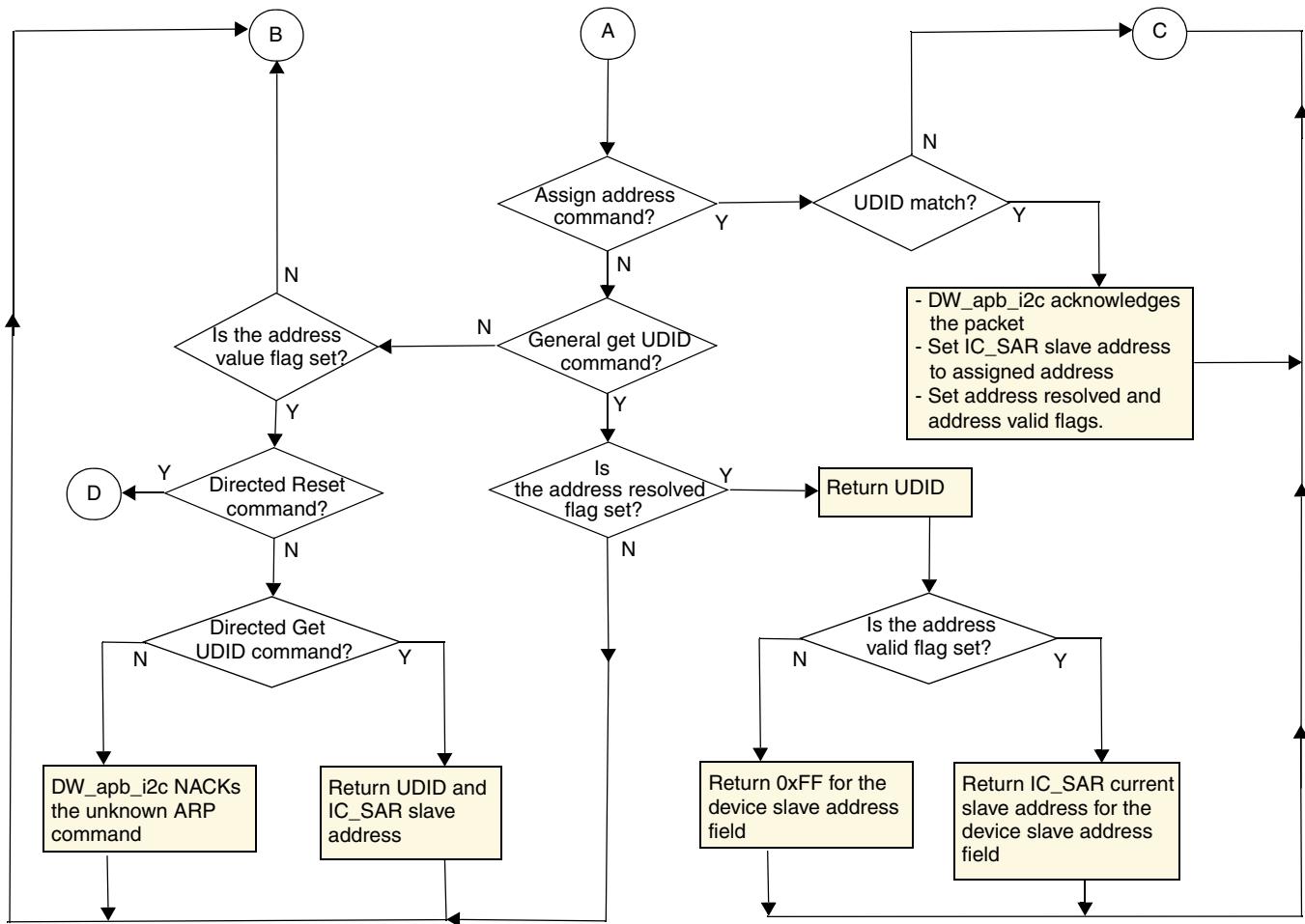
Figure 8-10 ARP Master Programming Flow



8.9 ARP Slave Programming Flow

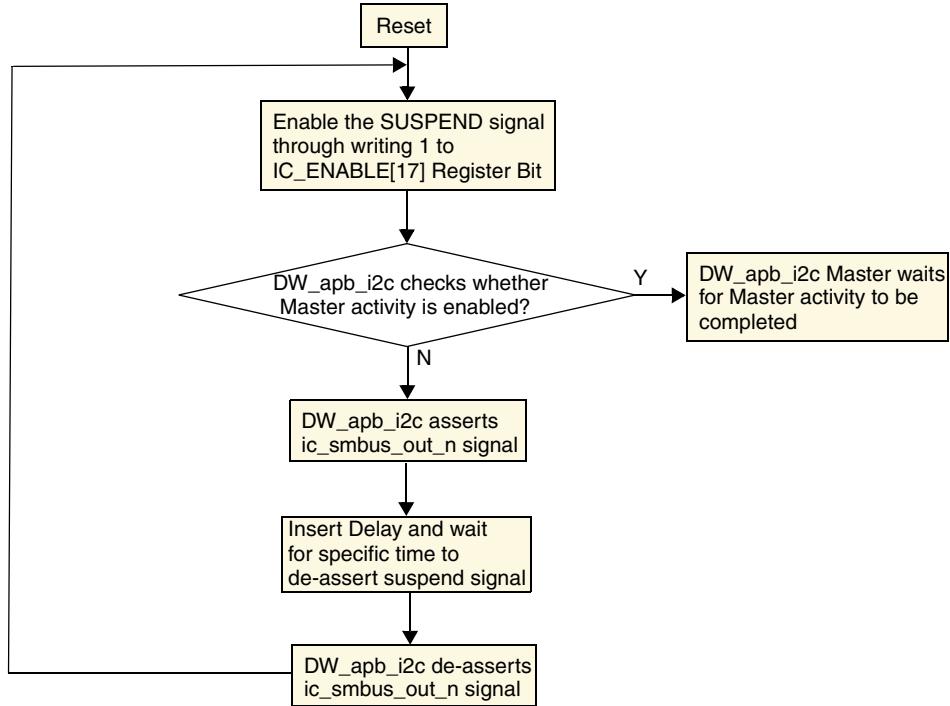
Figure 8-11 shows the programming flow for an ARP slave.

Figure 8-11 ARP Slave Programming Flow



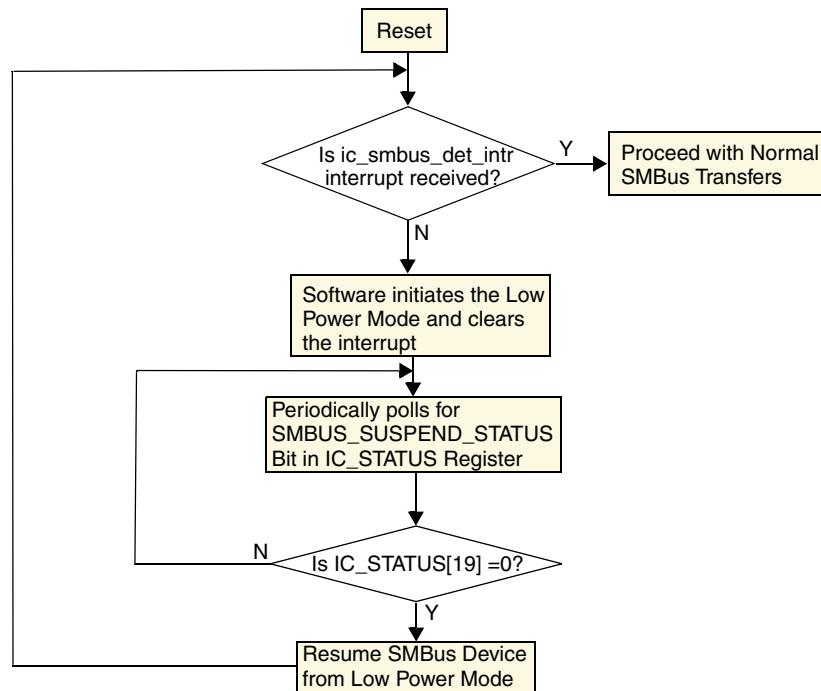
8.10 SMBus SUSPEND Programming Flow in Host Mode

Figure 8-12 Suspend Programming Flow in Host Mode



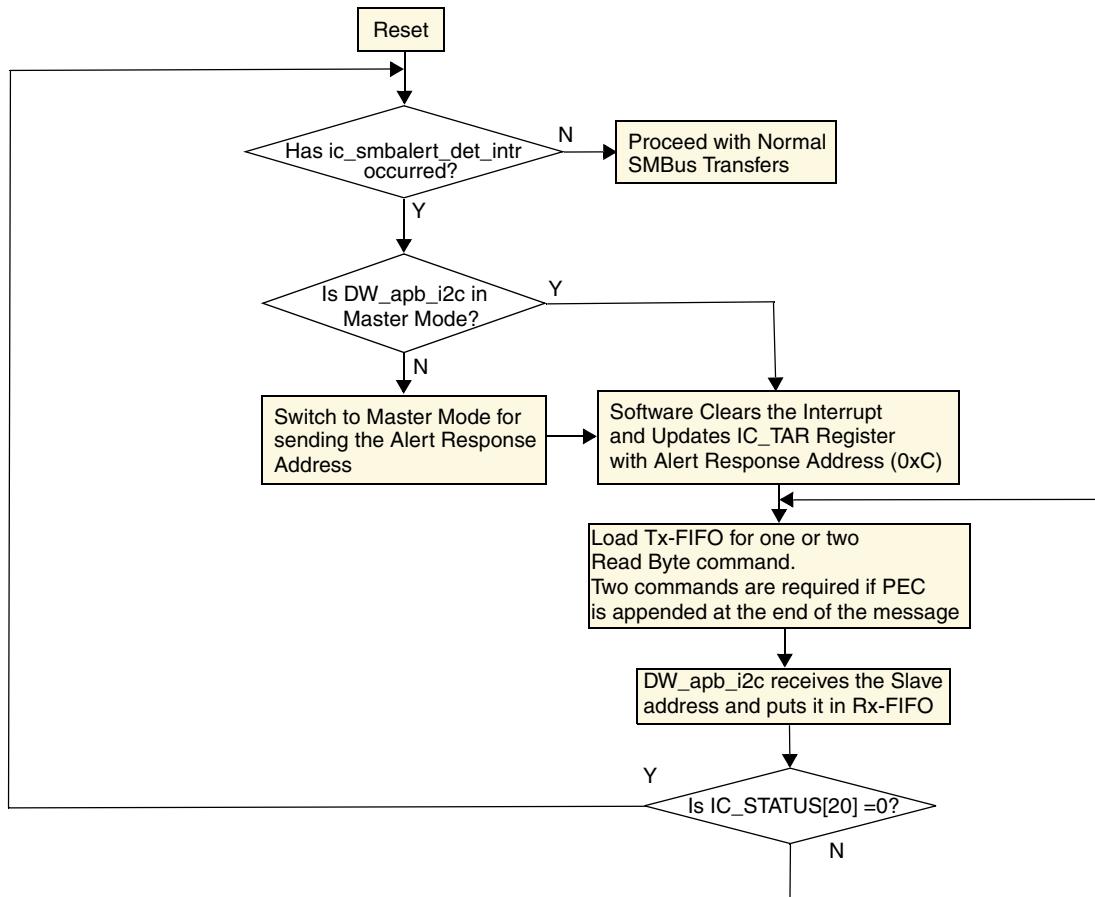
8.11 SMBus SUSPEND Programming Flow in Device Mode

Figure 8-13 SMBus SUSPEND Programming flow in Device Mode



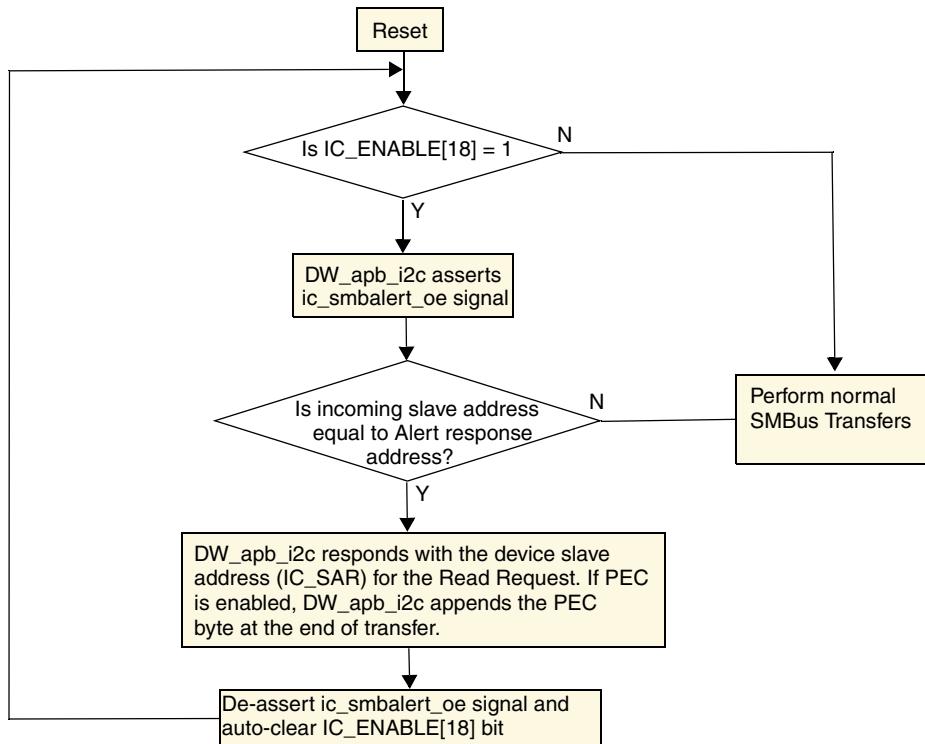
8.12 SMBus ALERT Programming Flow in Host Mode

Figure 8-14 SMBus Alert Programming Flow in Host Mode



8.13 SMBus ALERT Programming Flow in Device Mode

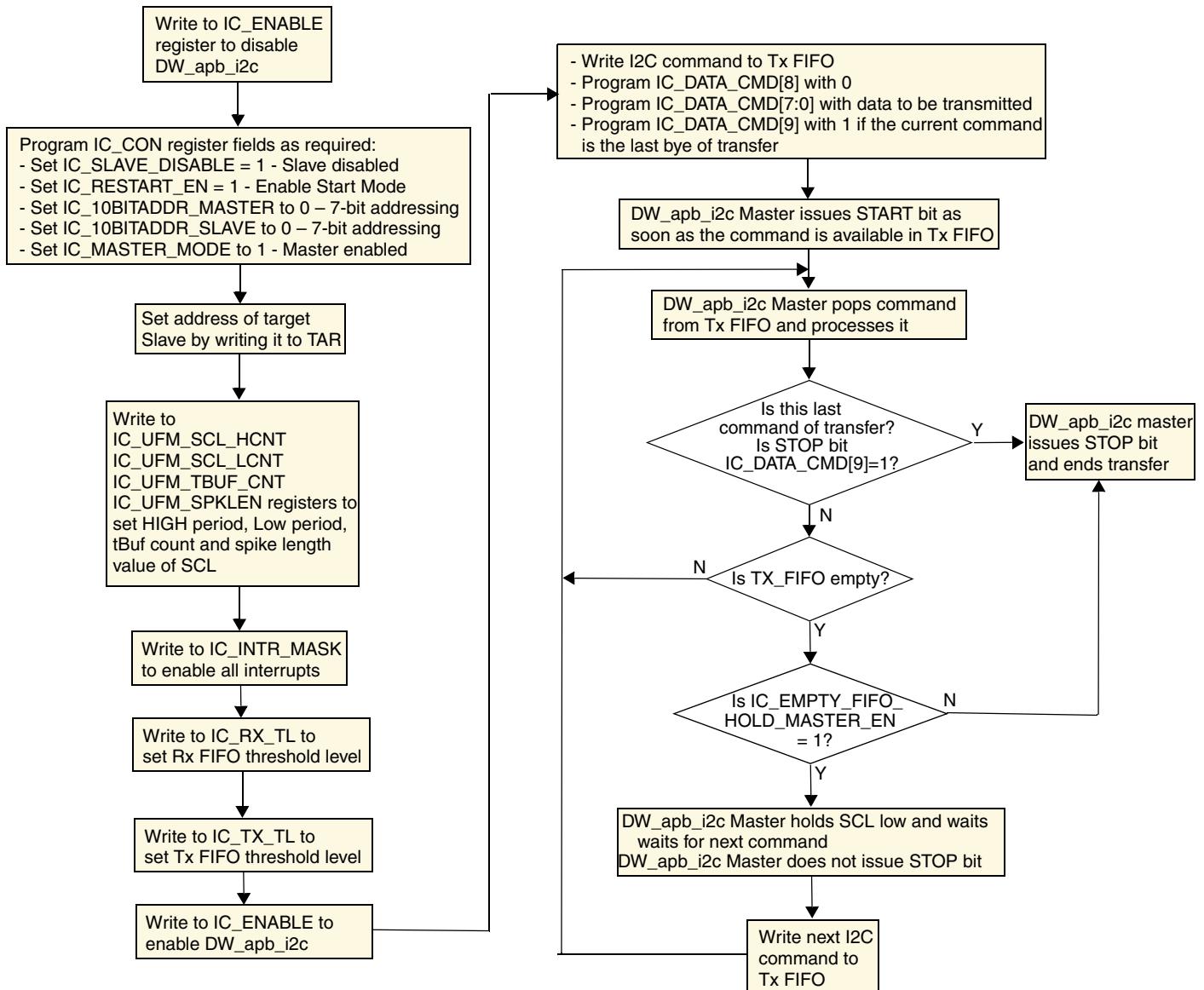
Figure 8-15 SMBus Alert Programming Flow in Device Mode



8.14 Programming Flow Of DW_apb_i2c in Ultra-Fast Mode

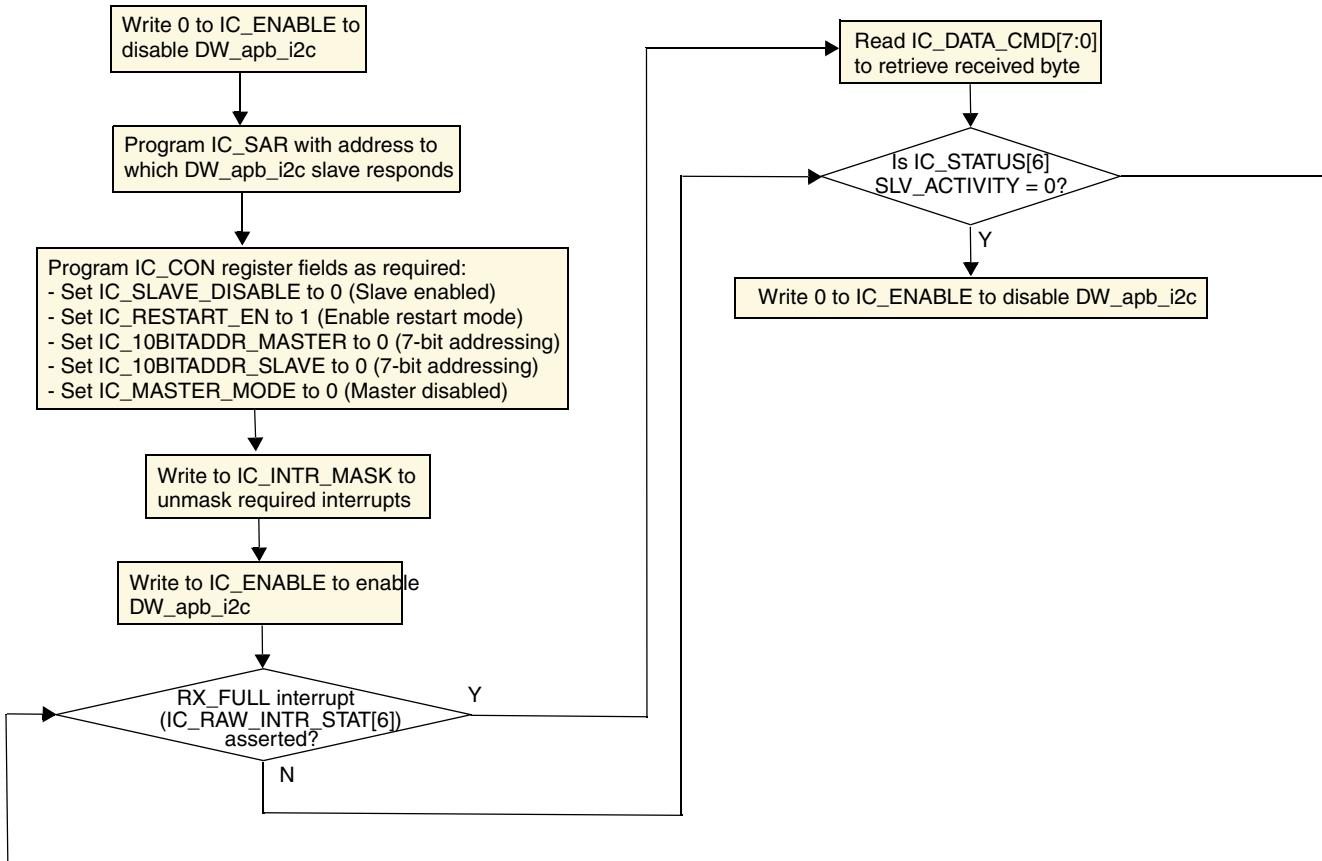
8.14.1 DW_apb_i2c Master Mode

Figure 8-16 DW_apb_i2c Ultra-Fast Master Mode



8.14.2 DW_apb_i2c Slave Mode

Figure 8-17 DW_apb_i2c Ultra-Fast Slave Mode



Verification

This chapter provides an overview of the testbench available for DW_apb_i2c verification. Once you have configured the DW_apb_i2c in coreConsultant and have set up the verification environment, you can run simulations automatically.



Note The DW_apb_i2c verification testbench is built with DesignWare Verification IP (VIP). Please make sure you have the supported version of the VIP components for this release, otherwise, you may experience some tool compatibility problems. For more information about supported tools in this release, refer to the following web page:
www.synopsys.com/products/designware/docs/doc/amba/latest/dw_amba_install.pdf

9.1 Overview of Vera Tests

The DW_apb_i2c verification testbench performs the following set of tests that have been written to exhaustively verify the functionality and have also achieved maximum RTL code coverage.



All tests use the APB Interface to program memory mapped registers dynamically during tests.

9.1.1 APB Slave Interface

This suite of tests is run to verify that the APB interface functions correctly by checking the following:

- All non-configuration parameter register reset values are verified.
- All read-only registers are written to with opposite values to verify that they are read only.
- All writable registers are written to with opposite values to verify that they can be written.
- Some registers can be written only when the DW_apb_i2c is disabled. Confirm that those registers are non-writable in that mode. Attempt to write the opposite values to those registers while the DW_apb_i2c is disabled and verify that the writes are ignored.
- The *CNT registers can be written to only if the configuration parameter IC_HC_COUNT_VALUES = 0. Verify that the registers are read-only when IC_HC_COUNT_VALUES = 0 and writable when IC_HC_COUNT_VALUES = 1.

- Confirm that it is not possible to write the transmit buffer threshold level (IC_TX_TL) higher than the size of the transmit buffer. Verify that if a larger value is written that the value becomes set to the size of the transmit buffer (max).
- Confirm that it is not possible to write the receive buffer threshold level (IC_RX_TL) higher than the size of the transmit buffer. Verify that if a larger value is written that the value becomes set to the size of the transmit buffer (max).
- Write illegal value 0 to SPEED bits in IC_CON and verify that the new value is parameter IC_MAX_SPEED_MODE.
- Verify that the SPEED bits in IC_CON cannot be written to higher speeds than configuration parameter IC_MAX_SPEED_MODE.

9.1.2 DW_apb_i2c Master Operation

This suite of tests is run only when the DW_apb_i2c is configured as a master. For instance, these tests go through all combinations of speed, addressing, read/write, and multi-byte transfers. Commands are issued to the DW_apb_i2c, and the I²C Slave is the target and used to verify the transfers. The tests also verify the following:

- SCL low and SCL high times are with I²C specification
- Operation of all registers
- Master arbitration
- Debug outputs
- Disabling of DW_apb_i2c shown correctly on ic_en output
- Programmed count values for all the *CNT registers
- The current source enable output operates correctly
- Combined format operation (7- and 10-bit addressing modes)
- Restart enable and disable
- Clock synchronization by stretching SCL
- Loop-back operation by performing simultaneous master-transmitter, slave-receiver sending multiple bytes. A single-byte transfer with master-receiver, slave-transmitter is also performed

9.1.3 DW_apb_i2c Slave Operation

This suite of tests is run only when the DW_apb_i2c is configured as a slave. Similar to the tests developed for the master, the driving force is the Serial Master BFM. For instance, these tests go through all combinations of speed, addressing, read/write, and multi-byte transfers. The I²C master is used to generate transfers and the DW_apb_i2c is the target; the AHB Master is used to verify the transfers. The tests also verify the following:

- Operation of all registers
- Debug outputs

- Disabling of DW_apb_i2c shown correctly on ic_en output
- Combined format operation (7- and 10-bit addressing modes)

9.1.4 DW_apb_i2c Interrupts

These tests verify that the DW_apb_i2c generates and handles the servicing of interrupts correctly. They also verify operation of the debug ports.

9.1.5 DMA Handshaking Interface

These tests verify that DW_apb_i2c generates and responds through the handshaking interface. Transfers are generated within the DMA BFM and transmitted through the I²C protocol from the DUT to the ALT_DUT and vice versa. Different watermark levels are selected to control the clearing on the dma_tx_req/dma_rx_req lines once an acknowledgement is received. A random number of bytes are transferred using only the handshaking interface.

9.1.6 DW_apb_i2c Dynamic IC_TAR and IC_10BITADDR_MASTER Update

This test is run only if the DW_apb_i2c is configured as a master and the parameter I2C_DYNAMIC_TAR_UPDATE = 1. This test verifies that DW_apb_i2c Master Target address (IC_TAR) and the parameter IC_10BITADDR_MASTER can be updated dynamically while the DW_apb_i2c Slave is involved in an I2C transfer on the I2C bus.

9.1.7 Generate NACK as a Slave-Receiver

This test is always run and tests the functionality of DW_apb_i2c, depending on whether the parameter IC_SLV_DATA_NACK_ONLY is set to 0 or 1. This test verifies that ACK/NACKs are generated correctly when DW_apb_i2c is acting as a slave-receiver, depending on whether IC_SLV_DATA_NACK_ONLY register exists (set by having parameter IC_SLV_DATA_NACK_ONLY=1). If the register exists, its value is set to 1 for the duration of the test. If the register exists (and therefore its value is 1), a NACK is generated by the slave when data is sent to it, the transfer is aborted, and data is not written to the receive buffer. Otherwise, ACKs are generated for the duration of the transfer, the transfer completes successfully, and the data is written to the receive buffer successfully.

9.1.8 SCL Held Low for Duration Specified in IC_SDA_SETUP

This test verifies that during a Slave-Receive I²C transfer, DW_apb_i2c asserts the output port ic_data_oe, holding SCL low for the minimum period specified in the [IC_SDA_SETUP](#) register. This only happens every time the I²C master ACKs a data byte, and the transmit FIFO in DW_apb_i2c is not filled to satisfy this read request.

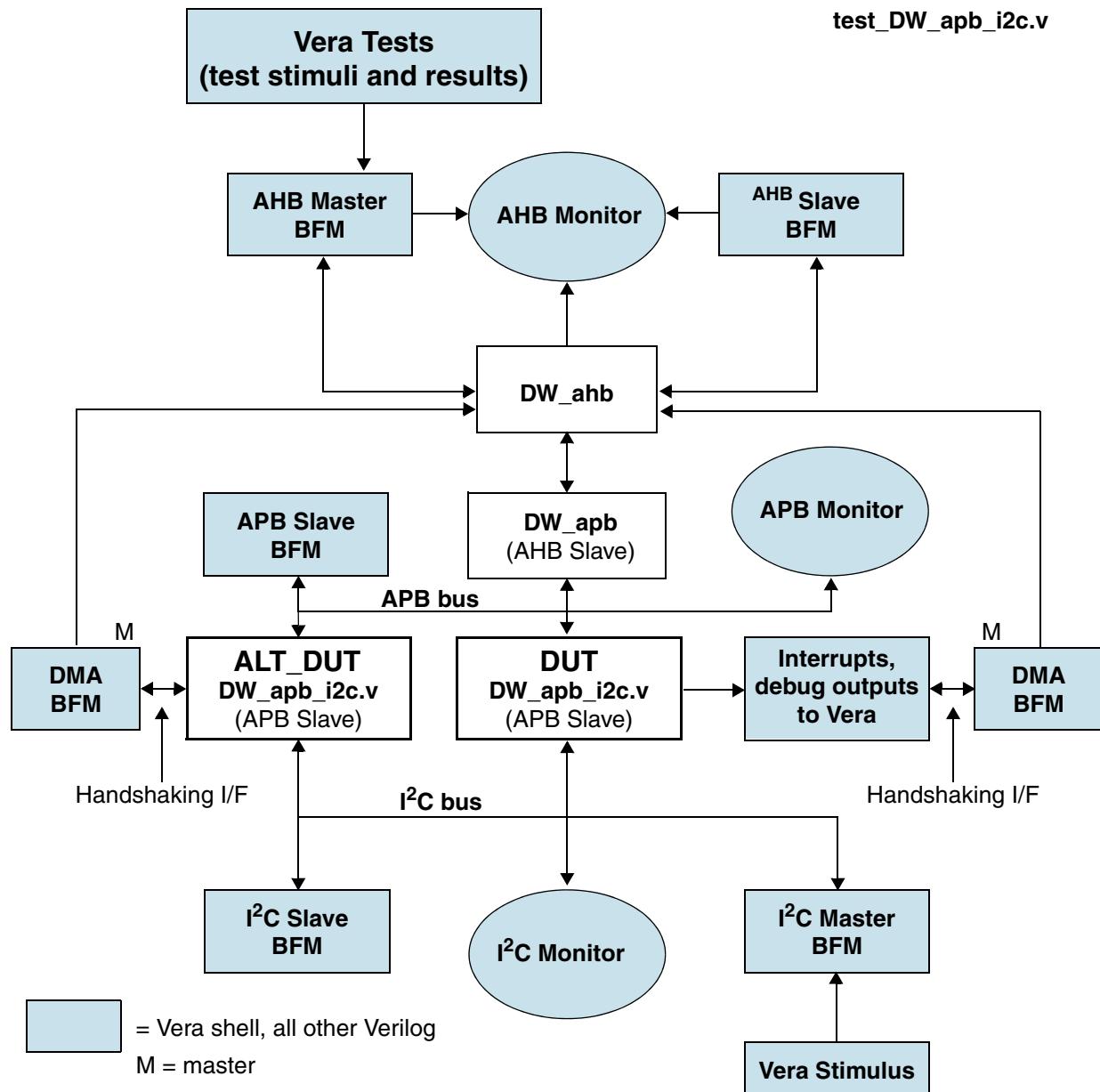
9.1.9 Generate ACK/NACK for General Call

This test verifies that the IC_ACK_GENERAL_CALL bit controls whether DW_apb_i2c ACK or NACKs an I²C general call address.

9.2 Overview of DW_apb_i2c Testbench

As illustrated in [Figure 9-1](#), the Verilog DW_apb_i2c testbench includes two instantiations of the design under test (DUT), AHB and APB Bridge bus models, and a Vera shell. The Vera shell consists of a number of serial slave BFM, a master slave BFM, and a DMA BFM to simulate and stimulate traffic to and from the DW_apb_i2c.

Figure 9-1 DW_apb_i2c Testbench



The test_DW_apb_i2c.v file shows the instantiation of the top-level MacroCell in a testbench and resides in the *workspace/sim/testbench* directory. The testbench tests the user configuration specified in the Specify Configuration task of coreConsultant. The testbench also tests that the component is AMBA-compliant and includes a self-checking mechanism. When a coreKit has been unpacked and configured, the verification

environment is stored in *workspace/sim*. Files in *workspace/sim/test_i2c* form the actual testbench for DW_apb_i2c.

10

Integration Considerations

After you have configured, tested, and synthesized your component with the coreTools flow, you can integrate the component into your own design environment. The following sections discuss general integration considerations.

10.1 Accessing Top-level Constraints

To get SDC constraints out of coreConsultant, you need to first complete the synthesis activity and then use the “write_sdc” command to write out the results:

1. This cC command sets synthesis to write out scripts only, without running DC:

```
set_activity_parameter Synthesize ScriptsOnly 1
```

2. This cC command autocompletes the activity:

```
autocomplete_activity Synthesize
```

3. Finally, this cC command writes out SDC constraints:

```
write_sdc <filename>
```

Performing

This section discusses performance and the hardware configuration parameters that affect the performance of the DW_apb_i2c.

10.1.1 Area

This section provides information to help you configure area for your configuration.

The following table includes synthesis results that have been generated using the TSMC 65nm technology library.

Table 10-1 Synthesis Results Using TSMC 65nmTechnology Library

Configuration	Operating Frequency	Gate Count
Default Configuration	166 MHz	11419 gates

Table 10-1 Synthesis Results Using TSMC 65nm Technology Library (Continued)

Configuration	Operating Frequency	Gate Count
Minimum Configuration: IC_CLK_TYPE=0 IC_MAX_SPEED_MODE=1 IC_10BITADDR_MASTER=0 IC_10BITADDR_SLAVE=0 IC_MASTER_MODE=0 IC_TX_BUFFER_DEPTH=2 IC_RX_BUFFER_DEPTH=2 IC_HC_COUNT_VALUES=1	166 MHz	6253 gates
Maximum Configuration: IC_CLK_TYPE=1 APB_DATA_WIDTH=32 IC_TX_BUFFER_DEPTH=16 IC_RX_BUFFER_DEPTH=16	166 MHz	12768 gates

The following table includes synthesis results that have been generated using the TSMC 28nm technology library.

Table 10-2 Synthesis Results Using TSMC 28nm Technology Library

Configuration	Operating Frequency	Gate Count
Default Configuration	166 MHz	11164 gates
Minimum Configuration: IC_CLK_TYPE=0 IC_MAX_SPEED_MODE=1 IC_10BITADDR_MASTER=0 IC_10BITADDR_SLAVE=0 IC_MASTER_MODE=0 IC_TX_BUFFER_DEPTH=2 IC_RX_BUFFER_DEPTH=2 IC_HC_COUNT_VALUES=1	166 MHz	6151 gates
Maximum Configuration: IC_CLK_TYPE=1 APB_DATA_WIDTH=32 IC_TX_BUFFER_DEPTH=16 IC_RX_BUFFER_DEPTH=16	166 MHz	12659 gates

10.1.2 Power Consumption

The following table provides information about the power consumption of the DW_apb_i2c using the TSMC 65nm technology library and how it affects performance.

Table 10-3 Power Consumption of DW_apb_i2c Using TSMC 65nm Technology Library

Configuration	Operating Frequency	Static Power Consumption	Dynamic Power Consumption
Default Configuration	166 MHz	3.0260 µW	1.2895 mW
Minimum Configuration: IC_CLK_TYPE=0 IC_MAX_SPEED_MODE=1 IC_10BITADDR_MASTER=0 IC_10BITADDR_SLAVE=0 IC_MASTER_MODE=0 IC_TX_BUFFER_DEPTH=2 IC_RX_BUFFER_DEPTH=2 IC_HC_COUNT_VALUES=1	166 MHz	1.6878 µW	671.0817 µW
Maximum Configuration: IC_CLK_TYPE=1 APB_DATA_WIDTH=32 IC_TX_BUFFER_DEPTH=16 IC_RX_BUFFER_DEPTH=16	166 MHz	3.3545 µW	1.4755 mW

The following table provides information about the power consumption of the DW_apb_i2c using the TSMC 28nm technology library and how it affects performance.

Table 10-4 Power Consumption of DW_apb_i2c Using TSMC 28nm Technology Library

Configuration	Operating Frequency	Static Power Consumption	Dynamic Power Consumption
Default Configuration	166 MHz	1.1252 mW	877.4711 µW
Minimum Configuration: IC_CLK_TYPE=0 IC_MAX_SPEED_MODE=1 IC_10BITADDR_MASTER=0 IC_10BITADDR_SLAVE=0 IC_MASTER_MODE=0 IC_TX_BUFFER_DEPTH=2 IC_RX_BUFFER_DEPTH=2 IC_HC_COUNT_VALUES=1	166 MHz	625.7431 µW	452.3128 µW
Maximum Configuration: IC_CLK_TYPE=1 APB_DATA_WIDTH=32 IC_TX_BUFFER_DEPTH=16 IC_RX_BUFFER_DEPTH=16	166 MHz	1.2889 mW	999.9554 µW

A

Synchronizer Methods

This appendix describes the synchronizer methods (blocks of synchronizer functionality) that are used in the DW_apb_i2c to cross clock boundaries.

This appendix contains the following sections:

- “[Synchronizers Used in DW_apb_i2c](#)” on page [280](#)
- “[Synchronizer 1: Simple Double Register Synchronizer](#)” on page [281](#)
- “[Synchronizer 2: Simple Double Register Synchronizer with Configurable Polarity Reset](#)” on page [281](#)

**Note**

The DesignWare Building Blocks (DWBB) contains several synchronizer components with functionality similar to methods documented in this appendix. For more information about the DWBB synchronizer components go to:

www.synopsys.com/products/designware/docs/doc/dwf/datasheets/interface_cdc_overview.pdf

A.1 Synchronizers Used in DW_apb_i2c

Each of the synchronizers and synchronizer sub-modules are comprised of verified DesignWare Basic Core (BCM) RTL designs. The BCM synchronizer designs are identified by the synchronizer type. The corresponding RTL files comprising the BCM synchronizers used in the DW_apb_i2c are listed and cross referenced to the synchronizer type in [Table A-1](#). Note that certain BCM modules are contained in other BCM modules, as they are used in a building block fashion.

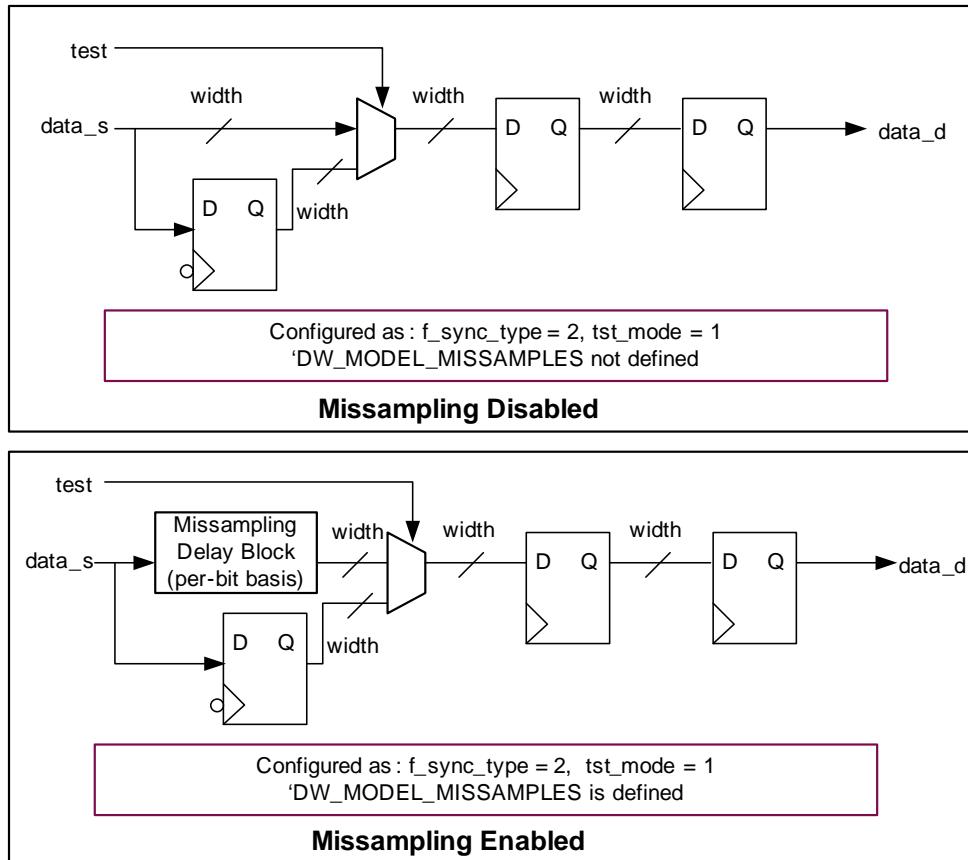
Table A-1 Synchronizers used in DW_apb_i2c

Synchronizer module file	Sub module file	Synchronizer Type and Number
DW_apb_i2c_bcm21.v		Synchronizer 1: Simple Multiple Register Synchronizer
DW_apb_i2c_bcm41.v	DW_apb_i2c_bcm21.v	Synchronizer 2: Simple Multiple Register Synchronizer with Configurable Polarity Reset

A.2 Synchronizer 1: Simple Double Register Synchronizer

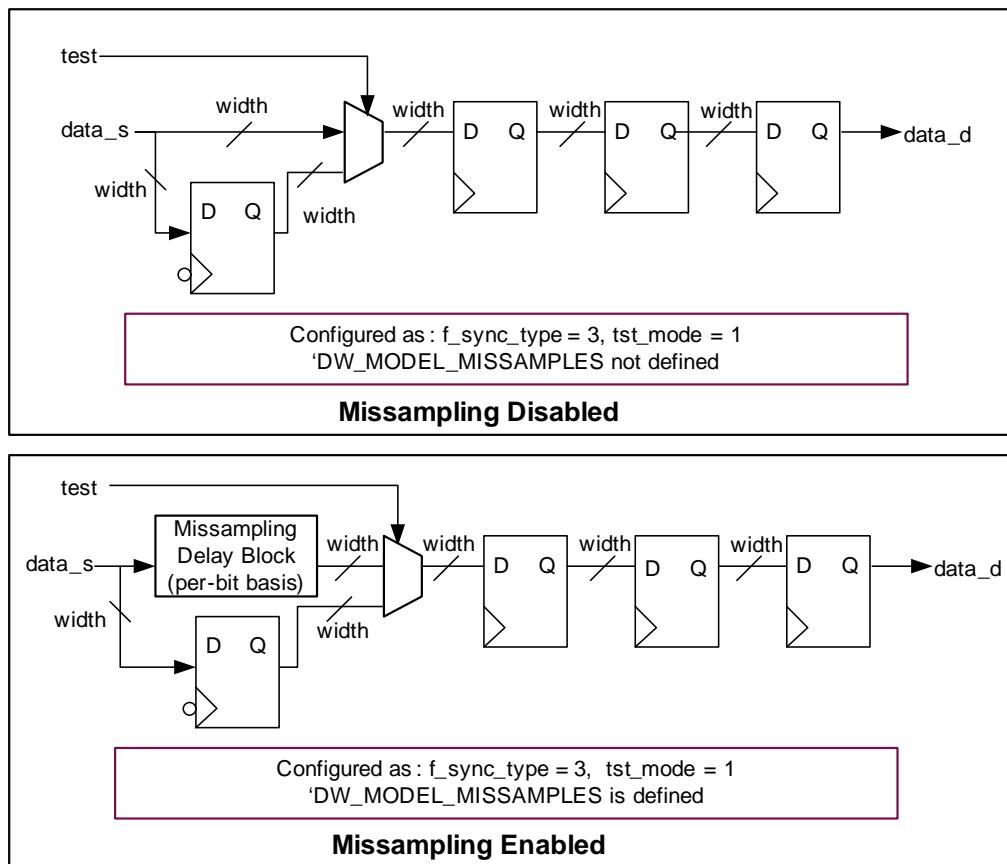
This is a single clock data bus synchronizer for synchronizing data that crosses asynchronous clock boundaries. The synchronization scheme depends on core configuration. If pclk and ic_clk are asynchronous (IC_CLK_TYPE = ASYNC) then DW_apb_i2c_bcm21 is instantiated inside the core for synchronization. This uses two stage synchronization process () both using positive edge of clock.

Figure A-1 Block Diagram of Synchronizer 1 With Two Stage Synchronization (Both Positive Edges)



A.3 Synchronizer 2: Simple Double Register Synchronizer with Configurable Polarity Reset

This is a single clock data bus synchronizer for synchronizing data that crosses asynchronous clock boundaries with configurable polarity reset. The synchronization scheme depends on core configuration. If pclk and ic_clk are asynchronous (IC_CLK_TYPE = ASYNC) then DW_apb_i2c_bcm41 is instantiated inside the core for synchronization of ic_clk_in_a and ic_data_in_a input signals. This DW_apb_i2c_bcm41 synchronizer is similar to the DW_apb_i2c_bcm21 synchronizer and the polarity of the output of this synchronizer can be configured. [Figure A-2](#) shows the block diagram of Synchronizer 2.

Figure A-2 Block Diagram of Synchronizer 2 With Two Stage Synchronization (Both Positive Edges)

B**Glossary**

active command queue	Command queue from which a model is currently taking commands; see also command queue.
activity	A set of functions in coreConsultant that step you through configuration, verification, and synthesis of a selected core.
AHB	Advanced High-performance Bus — high-performance system backbone bus. AHB supports the efficient connection of processors, on-chip memories and off-chip external memory interfaces (ARM Limited specification).
AMBA	Advanced Microcontroller Bus Architecture — a trademarked name by ARM Limited that defines an on-chip communication standard for high speed microcontrollers.
APB	Advanced Peripheral Bus — optimized for minimal power consumption and reduced interface complexity to support peripheral functions (ARM Limited specification).
APB bridge	DW_apb submodule that converts protocol between the AHB bus and APB bus.
application design	Overall chip-level design into which a subsystem or subsystems are integrated.
arbiter	AMBA bus submodule that arbitrates bus activity between masters and slaves.
BFM	Bus-Functional Model — A simulation model used for early hardware debug. A BFM simulates the bus cycles of a device and models device pins, as well as certain on-chip functions. See also Full-Functional Model.
big-endian	Data format in which most significant byte comes first; normal order of bytes in a word.
blocked command stream	A command stream that is blocked due to a blocking command issued to that stream; see also command stream, blocking command, and non-blocking command.

blocking command	A command that prevents a testbench from advancing to next testbench statement until this command executes in model. Blocking commands typically return data to the testbench from the model.
bus bridge	Logic that handles the interface and transactions between two bus standards, such as AHB and APB. See APB bridge.
command channel	Manages command streams. Models with multiple command channels execute command streams independently of each other to provide full-duplex mode function.
command stream	The communication channel between the testbench and the model.
component	A generic term that can refer to any synthesizable IP or verification IP in the DesignWare Library. In the context of synthesizable IP, this is a configurable block that can be instantiated as a single entity (VHDL) or module (Verilog) in a design.
configuration	The act of specifying parameters for a core prior to synthesis; can also be used in the context of VIP.
configuration intent	Range of values allowed for each parameter associated with a reusable core.
core	Any configurable block of synthesizable IP that can be instantiated as a single entity (VHDL) or module (Verilog) in a design. Core is the preferred term for a big piece of IIP. Anything that requires coreConsultant for configuration, as well as anything in the DesignWare Cores library, is a core.
core developer	Person or company who creates or packages a reusable core. All the cores in the DesignWare Library are developed by Synopsys.
core integrator	Person who uses coreConsultant or coreAssembler to incorporate reusable cores into a system-level design.
coreAssembler	Synopsys product that enables automatic connection of a group of cores into a subsystem. Generates RTL and gate-level views of the entire subsystem.
coreConsultant	A Synopsys product that lets you configure a core and generate the design views and synthesis views you need to integrate the core into your design. Can also synthesize the core and run the unit-level testbench supplied with the core.
coreKit	An unconfigured core and associated files, including the core itself, a specified synthesis methodology, interfaces definitions, and optional items such as verification environment files and core-specific documentation.
cycle command	A command that executes and causes HDL simulation time to advance.
decoder	Software or hardware subsystem that translates from and “encoded” format back to standard format.
design context	Aspects of a component or subsystem target environment that affect the synthesis of the component or subsystem.
design creation	The process of capturing a design as parameterized RTL.

Design View	A simulation model for a core generated by coreConsultant.
DesignWare Synthesizable Components	The Synopsys name for the collection of AMBA-compliant coreKits and verification models delivered with DesignWare and used with coreConsultant or coreAssembler to quickly build DesignWare Synthesizable Component designs.
DesignWare cores	A specific collection of synthesizable cores that are licensed individually. For more information, refer to www.synopsys.com/designware .
DesignWare Library	A collection of synthesizable IP and verification IP components that is authorized by a single DesignWare license. Products include SmartModels, VMT model suites, DesignWare Memory Models, Building Block IP, and the DesignWare Synthesizable Components.
dual role device	Device having the capabilities of function and host (limited).
endian	Ordering of bytes in a multi-byte word; see also little-endian and big-endian.
Full-Functional Mode	A simulation model that describes the complete range of device behavior, including code execution. See also BFM.
GPIO	General Purpose Input Output.
GTECH	A generic technology view used for RTL simulation of encrypted source code by non-Synopsys simulators.
hard IP	Non-synthesizable implementation IP.
HDL	Hardware Description Language – examples include Verilog and VHDL.
IIP	Implementation Intellectual Property — A generic term for synthesizable HDL and non-synthesizable “hard” IP in all of its forms (coreKit, component, core, MacroCell, and so on).
implementation view	The RTL for a core. You can simulate, synthesize, and implement this view of a core in a real chip.
instantiate	The act of placing a core or model into a design.
interface	Set of ports and parameters that defines a connection point to a component.
IP	Intellectual property — A term that encompasses simulation models and synthesizable blocks of HDL code.
little-endian	Data format in which the least-significant byte comes first.
MacroCell	Bigger IP blocks (6811, 8051, memory controller) available in the DesignWare Library and delivered with coreConsultant.
master	Device or model that initiates and controls another device or peripheral.
model	A Verification IP component or a Design View of a core.
monitor	A device or model that gathers performance statistics of a system.

non-blocking command	A testbench command that advances to the next testbench statement without waiting for the command to complete.
peripheral	Generally refers to a small core that has a bus connection, specifically an APB interface.
RTL	Register Transfer Level. A higher level of abstraction that implies a certain gate-level structure. Synthesis of RTL code yields a gate-level design.
SDRAM	Synchronous Dynamic Random Access Memory; high-speed DRAM adds a separate clock signal to control signals.
SDRAM controller	A memory controller with specific connections for SDRAMs.
slave	Device or model that is controlled by and responds to a master.
SoC	System on a chip.
soft IP	Any implementation IP that is configurable. Generally referred to as synthesizable IP.
static controller	Memory controller with specific connections for Static memories such as asynchronous SRAMs, Flash memory, and ROMs.
subsystem	In relation to coreAssembler, highest level of RTL that is automatically generated.
synthesis intent	Attributes that a core developer applies to a top-level design, ports, and core.
synthesizable IP	A type of Implementation IP that can be mapped to a target technology through synthesis. Sometimes referred to as Soft IP.
technology-independent	Design that allows the technology (that is, the library that implements the gate and via widths for gates) to be specified later during synthesis.
Testsuite Regression Environment (TRE)	A collection of files for stand-alone verification of the configured component. The files, tests, and functionality vary from component to component.
VIP	Verification Intellectual Property — A generic term for a simulation model in any form, including a Design View.
workspace	A network location that contains a personal copy of a component or subsystem. After you configure the component or subsystem (using coreConsultant or coreAssembler), the workspace contains the configured component/subsystem and generated views needed for integration of the component/subsystem at the top level.
wrap, wrapper	Code, usually VHDL or Verilog, that surrounds a design or model, allowing easier interfacing. Usually requires an extra, sometimes automated, step to create the wrapper.
zero-cycle command	A command that executes without HDL simulation time advancing.

Index

- A**
- active command queue
 - definition [283](#)
 - activity
 - definition [283](#)
 - AHB
 - definition [283](#)
 - AMBA
 - definition [283](#)
 - APB
 - definition [283](#)
 - APB bridge
 - definition [283](#)
 - APB Interface, and DW_apb_i2c [103](#)
 - APB_DATA_WIDTH [105](#)
 - application design
 - definition [283](#)
 - arbiter
 - definition [283](#)
 - Arbitration, of master [53](#)
- B**
- BFM
 - definition [283](#)
 - big-endian
 - definition [283](#)
 - Block diagram, of DW_apb_i2c [19](#)
 - blocked command stream
 - definition [283](#)
 - blocking command
 - definition [284](#)
 - bus bridge
 - definition [284](#)
- C**
- Clock synchronization [55](#)
 - command channel
 - definition [284](#)
 - command stream
 - definition [284](#)
 - component
 - definition [284](#)
 - Configuration
 - of IC_CLK frequency [79](#)
 - configuration
 - definition [284](#)
 - configuration intent
 - definition [284](#)
 - Configuration parameters [105](#)
 - core
 - definition [284](#)
 - core developer
 - definition [284](#)
 - core integrator
 - definition [284](#)
 - coreAssembler
 - definition [284](#)
 - overview of usage flow [30](#)
 - coreConsultant
 - definition [284](#)
 - overview of usage flow [24](#)
 - coreKit
 - definition [284](#)
 - Customer Support [10](#)
 - cycle command
 - definition [284](#)
- D**
- decoder
 - definition [284](#)
 - design context
 - definition [284](#)
 - design creation
 - definition [284](#)
 - Design View

- definition 285
- DesignWare cores
definition 285
- DesignWare Library
definition 285
- DesignWare Synthesizable Components
definition 285
- Disabling DW_apb_i2c
version 1.06a 62
- DMA Controller
and DW_apb_i2c 93
- dual role device
definition 285
- DW_apb_i2c
block diagram of 19
functional behavior 37
functional overview 19
memory map of 154
operation modes 56
overview of 37
parameters 105
programming of 153
protocols 43
registers 161
testbench
 overview of 272
 overview of tests 269
- Dynamic update of IC_TAR
 initial configuration of master mode 60
 or 10-bit addressing for master mode 61
- E**
- endian
definition 285
- Environment, licenses 21
- F**
- Full-Functional Mode
definition 285
- Functional behavior, of DW_apb_i2c 37
- Functional overview, of DW_apb_i2c 19
- G**
- GPIO
definition 285
- GTECH
definition 285
- H**
- hard IP
definition 285
- HDL
definition 285
- I**
- IC_10BITADDR_MASTER 107
IC_ACK_GENERAL_CALL 219
IC_ADD_ENCODED_PARAMS 110
IC_CAP_LOADING 113
IC_CLK frequency, configuration of 79
IC_CLOCK_FREQ 111
IC_CLR_ACTIVITY 195
IC_CLR_GEN_CALL 197
IC_CLR_INTR 192
IC_CLR_RD_REQ 194
IC_CLR_RX_DONE 195
IC_CLR_RX_OVER 193
IC_CLR_RX_UNDER 192
IC_CLR_START_DET 196
IC_CLR_STOP_DET 196
IC_CLR_TX_ABRT 194
IC_CLR_TX_OVER 193
IC_CON 161
IC_DATA_CMD 173
IC_DEFAULT_ACK_GENERAL_CALL 109
IC_DEFAULT_FS_SPKLEN 114
IC_DEFAULT_HS_SPKLEN 114
IC_DEFAULT_SDA_HOLD 109
IC_DEFAULT_SDA_SETUP 109
IC_DEFAULT_SLAVE_ADDR 106
IC_DMA_CR 215
IC_DMA_RDLR 217
IC_DMA_TDRLR 216
IC_ENABLE 198
IC_ENABLE_STATUS 220
IC_FS_SCL_HCNT 177
IC_FS_SCL_HIGH_COUNT 112
IC_FS_SCL_LCNT 178
IC_FS_SCL_LOW_COUNT 113
IC_HC_COUNT_VALUES 111
IC_HS_MADDR 171
IC_HS_MASTER_CODE 106

IC_HS_SCL_HCNT 179
IC_HS_SCL_HIGH_COUNT 113
IC_HS_SCL_LCNT 180
IC_HS_SCL_LOW_COUNT 107, 114
IC_INTR_IO 109
IC_INTR_MASK 183
IC_INTR_POL 110
IC_INTR_STAT 182
IC_MASTER_MODE 107
IC_MAX_SPEED_MODE 106
IC_RAW_INTR_STAT 186
IC_RESTART_EN 108
IC_RX_BUFFER_DEPTH 108
IC_RX_TL 108, 190
IC_RXFLR 206
IC_SAR 171
IC_SDA_HOLD 207
IC_SDA_SETUP 218
IC_SLV_DATA_NACK_ONLY 214
IC_SS_CDNT 176
IC_SS_HCNT 175
IC_SS_SCL_HIGH_COUNT 112
IC_SS_SCL_LOW_COUNT 112
IC_STATUS 201
IC_TAR 168
IC_TX_ABRT_SOURCE 208
IC_TX_BUFFER_DEPTH 108
IC_TX_TL 108, 191
IC_TXFLR 205
IC_USE_COUNTS 110
IP
 definition 285
implementation view
 definition 285
instance
 definition 285
interface
 definition 285
Interfaces
 APB 103
 DMA Controller 93
IP
 definition 285

L
Licenses 21
little-endian
 definition 285
M
MacroCell
 definition 285
master
 definition 285
Master arbitration 53
Master mode 60
Memory map, of DW_apb_i2c 154
model
 definition 285
monitor
 definition 285
N
non-blocking command
 definition 286
O
Operation modes 56
Output files
 GTECH 35
 RTL-level 35
 Simulation model 35
 synthesis 36
 verification 36
P
Parameters
 description of 105
peripheral
 definition 286
Programming DW_apb_i2c
 memory map 153
 registers 161
Protocols, of I²C 43
R
Register
 IC_HS_MADDR 171
Registers
 Clear ACTIVITY Interrupt 195
 Clear Combined and Individual Interrupts 192
 Clear GEN_CALL Interrupt 197
 Clear RD_REQ Interrupt 194

Clear RX_DONE Interrupt 195
Clear RX_OVER Interrupt 193
Clear RX_UNDER Interrupt 192
Clear START_DET Interrupt 196
Clear STOP_DET Interrupt 196
Clear TX_ABRT Interrupt 194
Clear TX_OVER Interrupt 193
Control 161
DMA Control 215
DMA Transmit Data Level 216
Enable Status 220
Fast Speed I2C Clock SCL High Count 177
Fast Speed I2C Clock SCL Low Count 178
Generate Slave Data NACK 214
High Speed I2C Clock SCL High Count 179
High Speed I2C Clock SCL Low Count 180
HS Master Mode Code Address 171
HS Spike Suppression Limit 223
I2C Enable 198
I2C Receive Data Level 217
IC_ACK_GENERAL_CALL 219
IC_CLR_ACTIVITY 195
IC_CLR_GEN_CALL 197
IC_CLR_INTR 192
IC_CLR_RD_REQ 194
IC_CLR_RX_DONE 195
IC_CLR_RX_OVER 193
IC_CLR_RX_UNDER 192
IC_CLR_START_DET 196
IC_CLR_STOP_DET 196
IC_CLR_TX_ABRT 194
IC_CLR_TX_OVER 193
IC_CON 161
IC_DATA_CMD 173
IC_DMA_CR 215
IC_DMA_RDLR 217
IC_DMA_TDLR 216
IC_ENABLE 198
IC_ENABLE_STATUS 220
IC_FS_SCL_HCNT 177
IC_FS_SCL_LCNT 178
IC_FS_SPKLENS 222
IC_HS_SCL_HCNT 179
IC_HS_SCL_LCNT 180
IC_HS_SPKLENS 223
IC_INTR_MASK 183
IC_INTR_STAT 182
IC_RAW_INTR_STAT 186
IC_RX_TL 190
IC_RXFLR 206
IC_SAR 171
IC_SDA_HOLD 207
IC_SDA_SETUP 218
IC_SLV_DATA_NACK_ONLY 214
IC_SS_HCNT 175
IC_SS_LCNT 176
IC_STATUS 201
IC_TAR 168
IC_TX_ABRT_SOURCE 208
IC_TX_TL 191
IC_TXFLR 205
Interrupt Mask 183
Interrupt Status 186
of DW_apb_i2c 161
Raw Interrupt Status 182
Receive Buffer Threshold 190
Rx/Tx Data buffer and Command 173
SDA Setup 218
Slave Address 171
SS/FS Spike Suppression Limit 222
Standard Speed I2C Clock SCL High Count 175
Standard Speed I2C Clock SCL Low Count 176
Target Address 168
Transmit Buffer Threshold 191
RTL
 definition 286
S
SDRAM
 definition 286
SDRAM controller
 definition 286
Simple double register synchronizer 281
Simulation
 of DW_apb_i2c 272
slave
 definition 286
Slave mode 56
SoC
 definition 286
SoC Platform
 AHB contained in 17
 APB, contained in 17
 defined 17
soft IP
 definition 286
SSI_HAS_DMA 109
static controller

definition [286](#)

subsystem

definition [286](#)

Synchronizer

simple double register [281](#)

synthesis intent

definition [286](#)

synthesizable IP

definition [286](#)

T

technology-independent

definition [286](#)

`test_DW_apb_i2c.v` [272](#)

Testsuite Regression Environment (TRE)

definition [286](#)

TRE

definition [286](#)

V

Vera, overview of tests [269](#)

Verification

and Vera tests [269](#)

of DW_apb_i2c [272](#)

VIP

definition [286](#)

W

workspace

definition [286](#)

wrap

definition [286](#)

wrapper

definition [286](#)

Z

zero-cycle command

definition [286](#)

