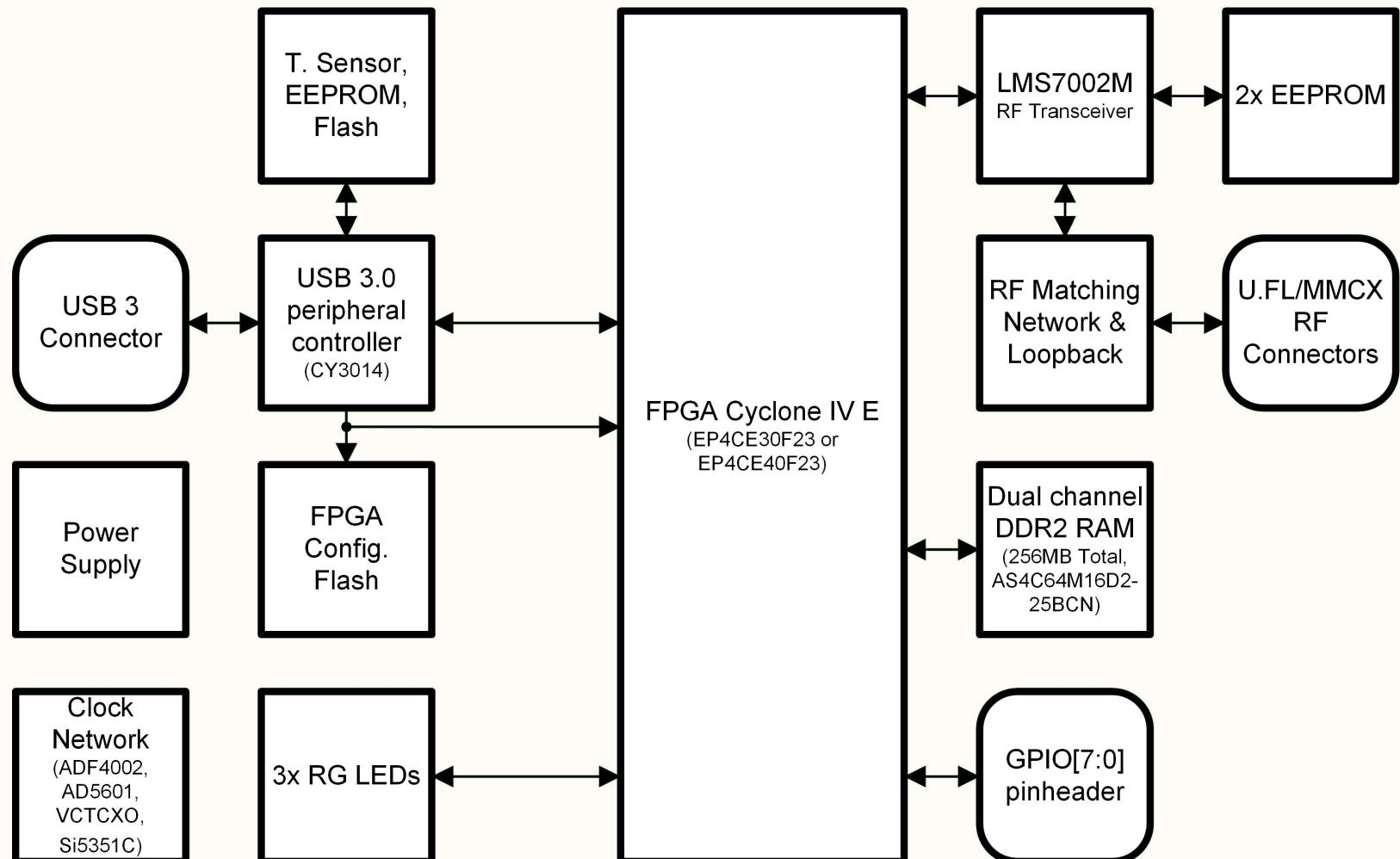


## Block diagram



Project name: *LimeSDR-USB\_1v4s.PrjPcb*

Title: *Block diagram*

Size: *A4* Revision: *v1.4s*

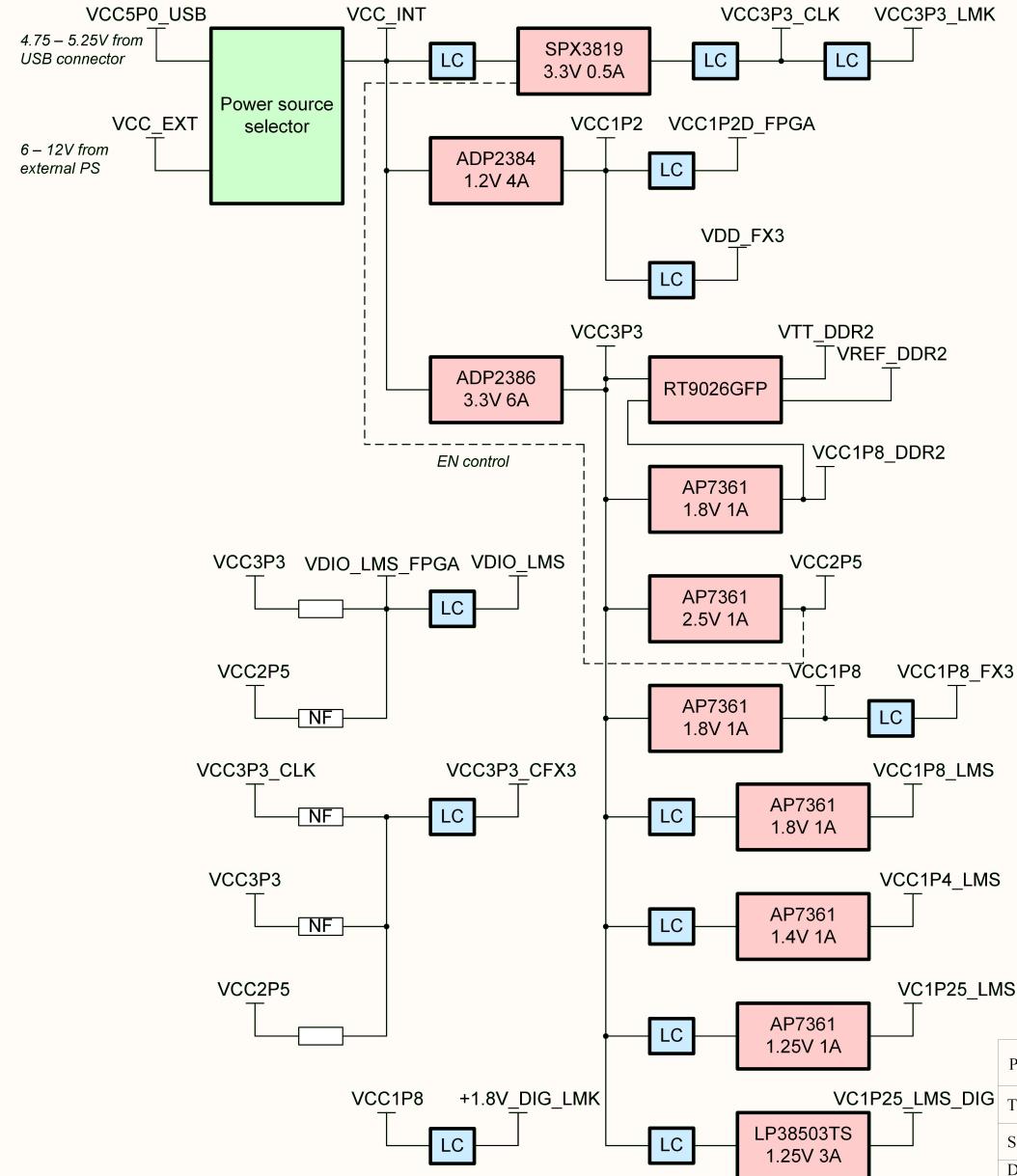
Date: *2017-02-01* Time: *15:09:54* Sheet *1* of *15*

File: *01\_BlockDiagram.SchDoc*

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Surrey  
United Kingdom



## Power diagram



Project name: **LimeSDR-USB\_1v4s.PrjPcb**

Title: **Power diagram**

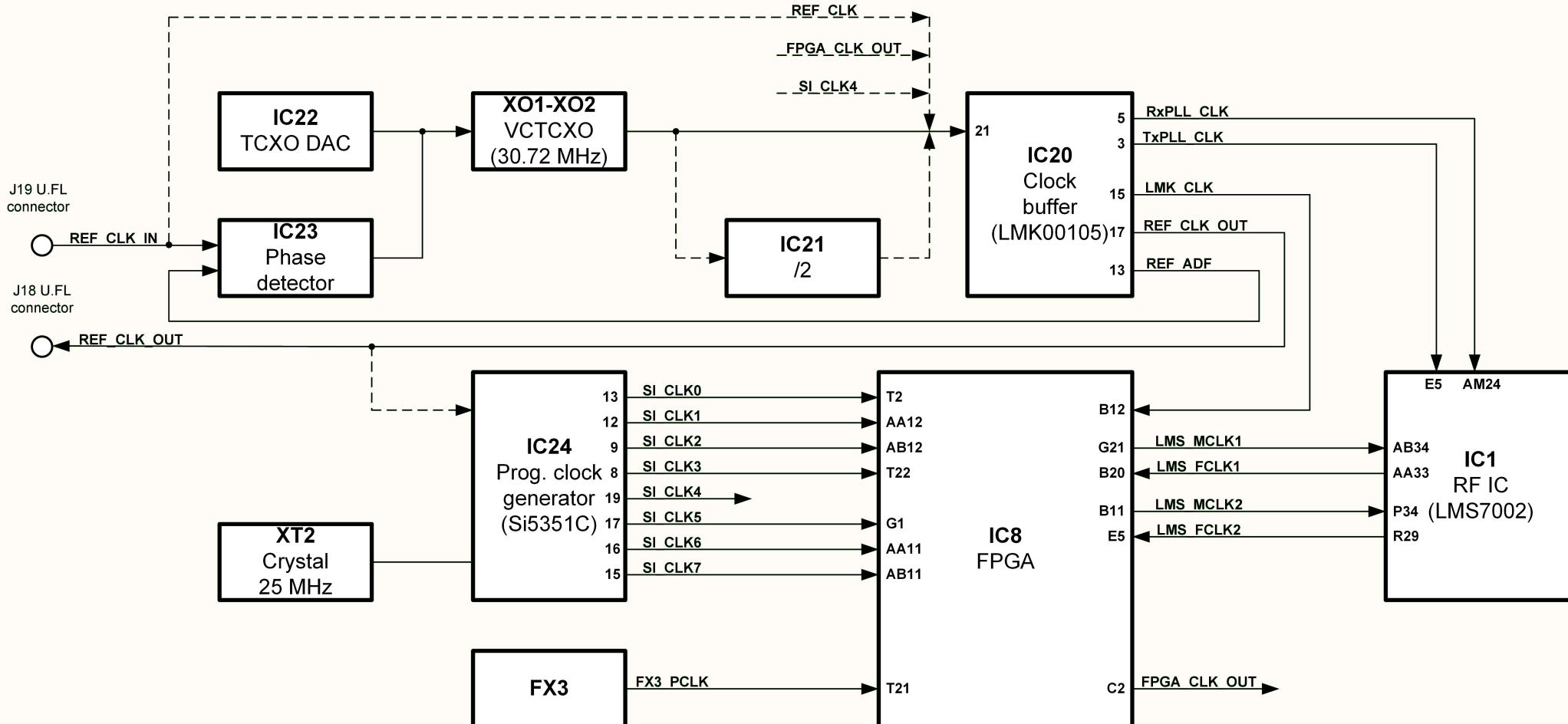
Size: **A4** Revision: **v1.4s**

Date: **2017-02-01** Time: **15:09:58** Sheet**2** of **15**

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## Clock diagram



Project name: *LimeSDR-USB\_1v4s.PrjPcb*

Title: *Clock diagram*

Size: A4 Revision: v1.4s

Date: 2017-02-01 Time: 15:10:08 Sheet 3 of 15

File: 03\_ClockDiagram.SchDoc

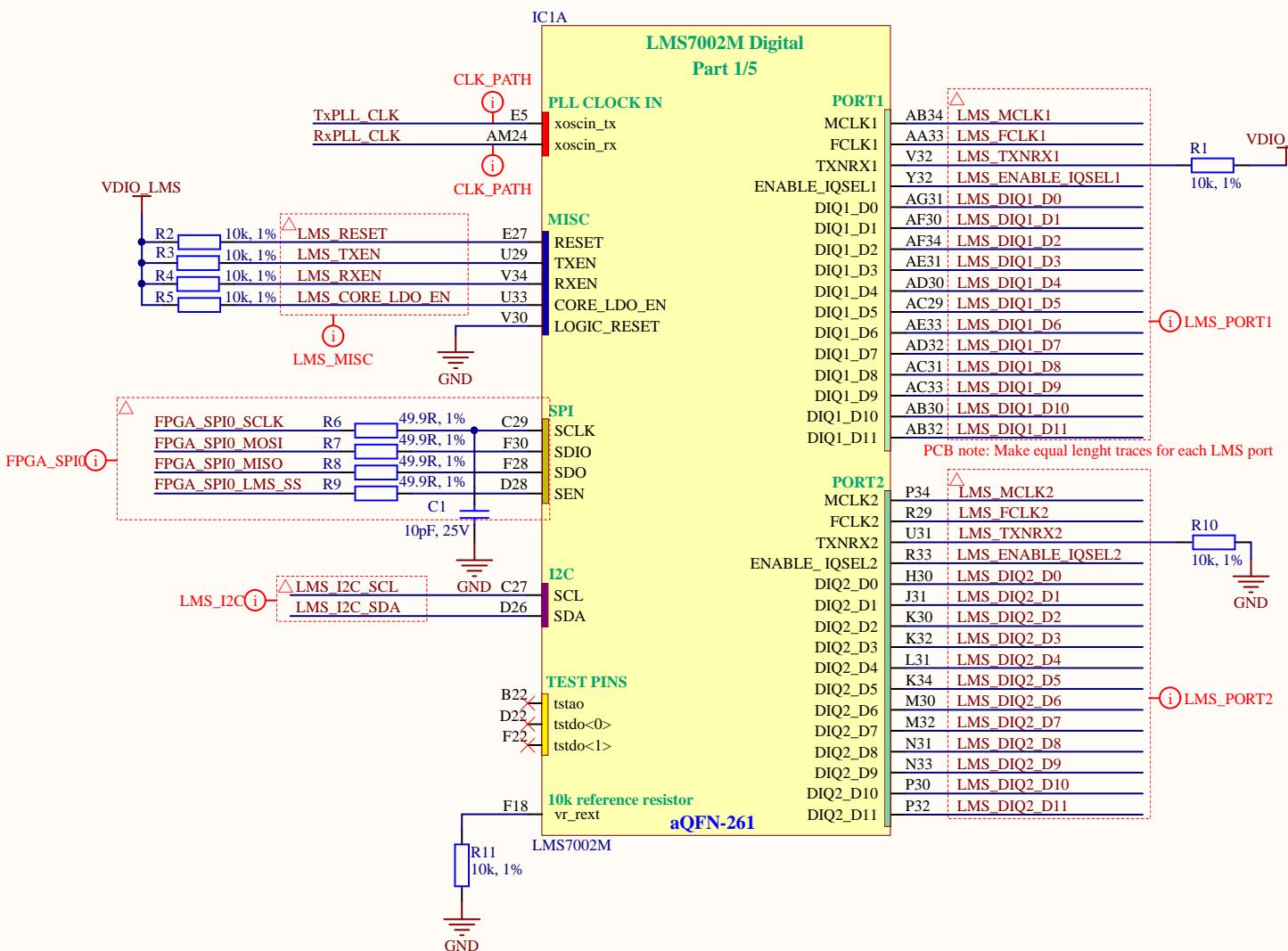
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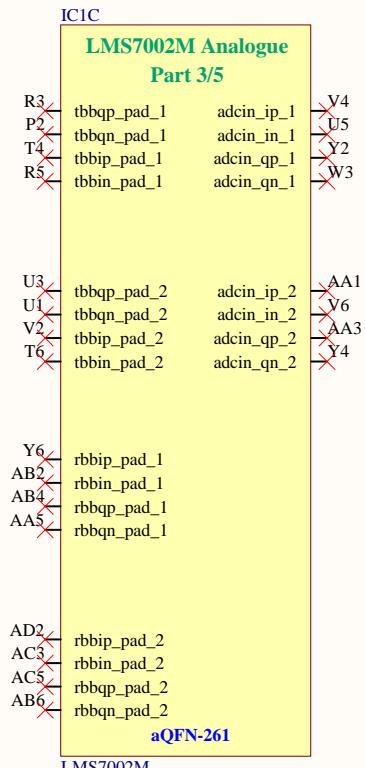
NF elements on sheet: -  
Number of NF elements on sheet: 0

## LMS7002M misc

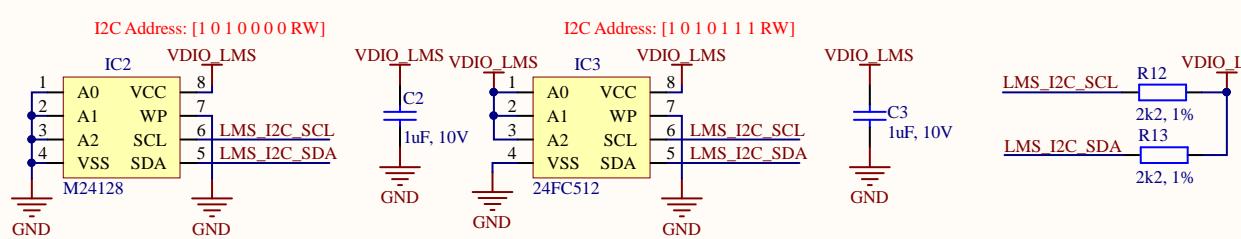
### Digital interfaces



### Baseband external IO



### LMS EEPROMs



Project name: LimeSDR-USB\_1v4s.PrjPcb

Title: LMS7002M misc

Size: A3 Revision: v1.4s

Date: 2017-02-01 Time: 15:10:14 Sheet 4 of 15

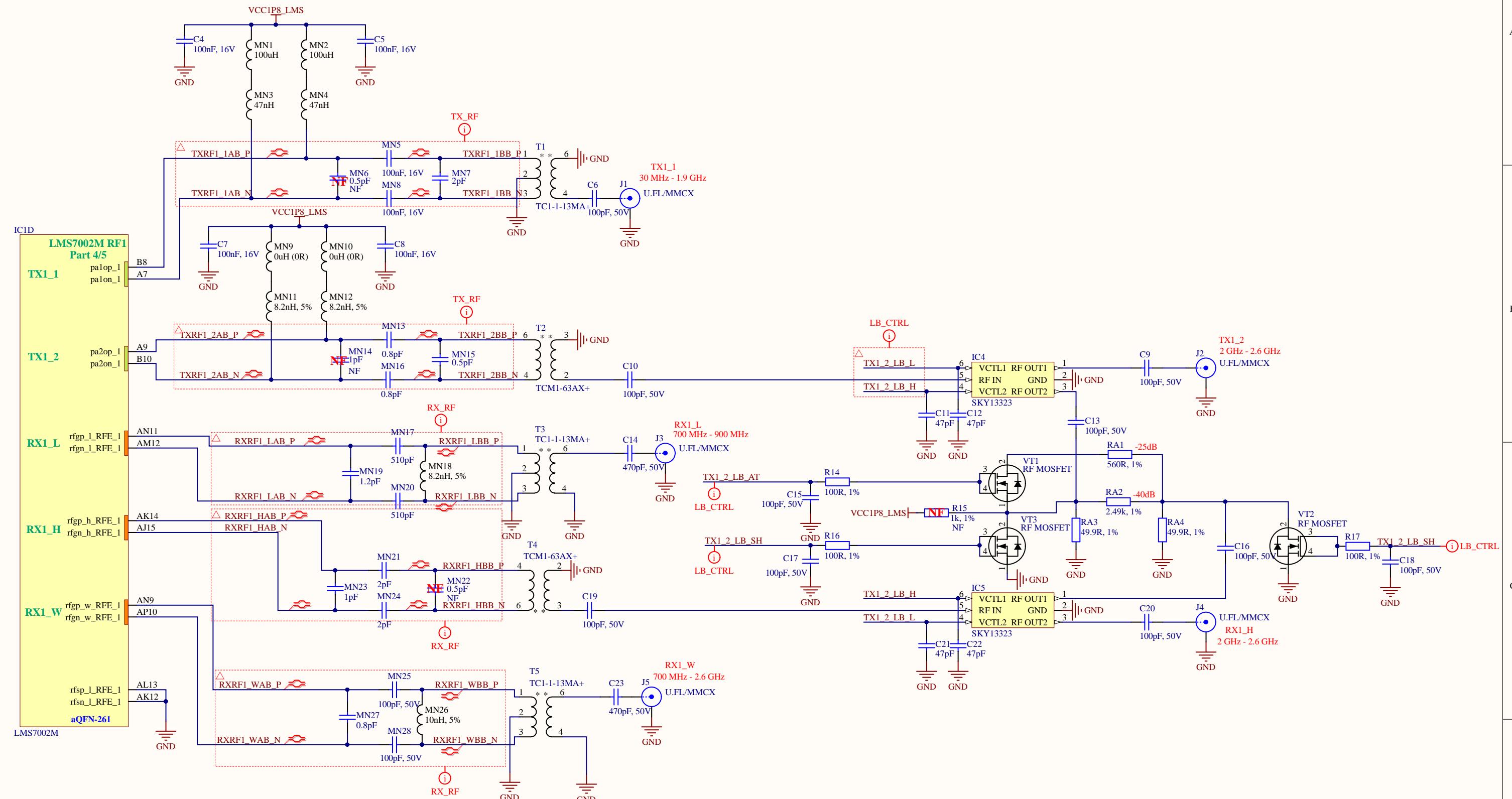
File: 04\_LMS7002M\_Misc.SchDoc

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NF elements on sheet: MN6, MN14, MN22, R15  
 Number of NF elements on sheet: 4

## LMS7002M RF1 circuits



Project name: LimeSDR-USB\_1v4s.PrfPcb

Title: LMS7002M RF

Size: A3 Revision: v1.4s

Date: 2017-02-01 Time: 15:10:17 Sheet 5 of 15

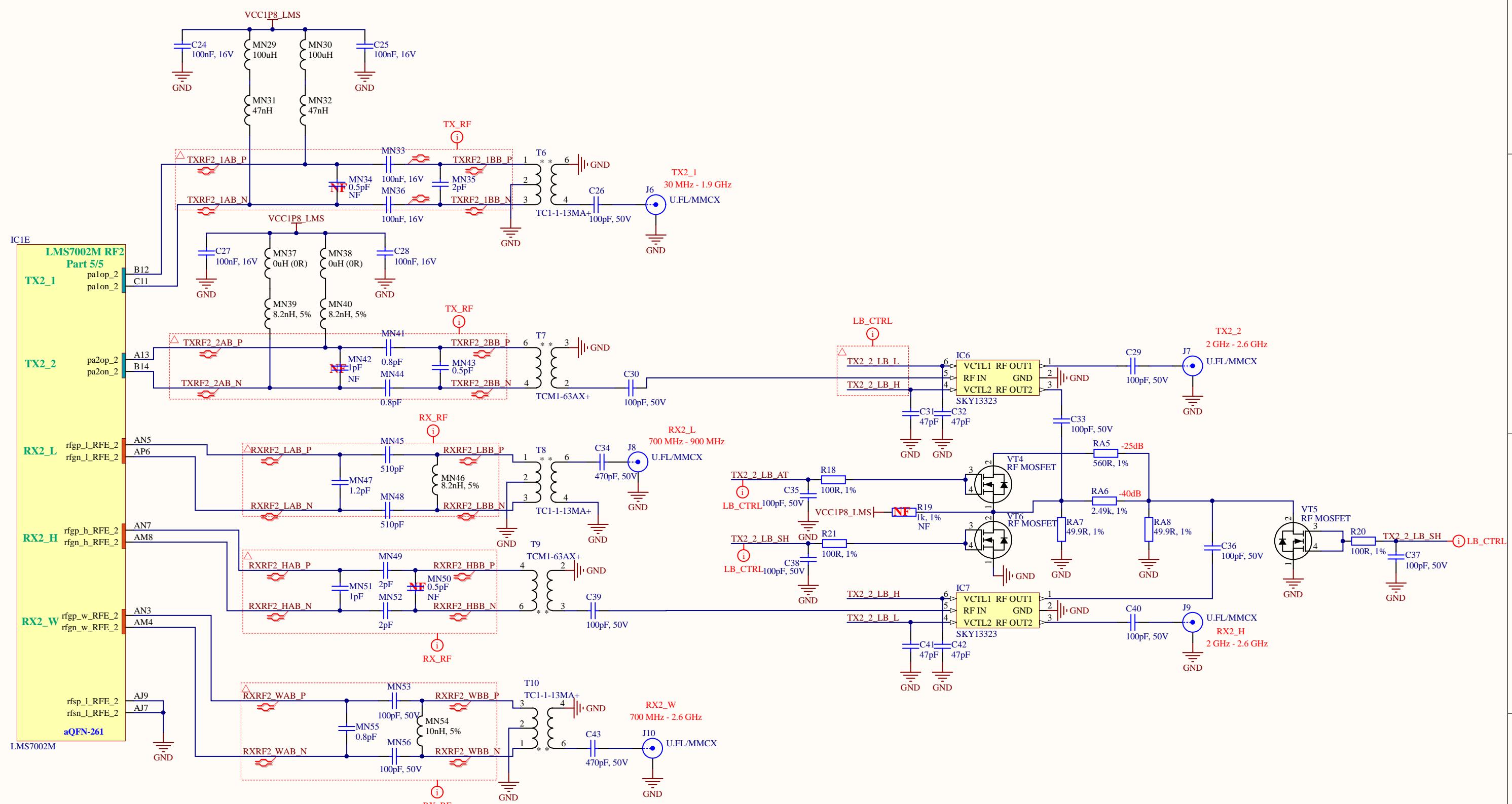
File: 05\_LMS7002M\_RF1.SchDoc

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NF elements on sheet: MN34, MN42, MN50, R19  
 Number of NF elements on sheet: 4

## LMS7002M RF2 circuits



Project name: LimeSDR-USB\_Iv4s.PrjPcb

Title: LMS7002M RF

Size: A3 Revision: v1.4s

Date: 2017-02-01 Time: 15:10:19 Sheet 6 of 15

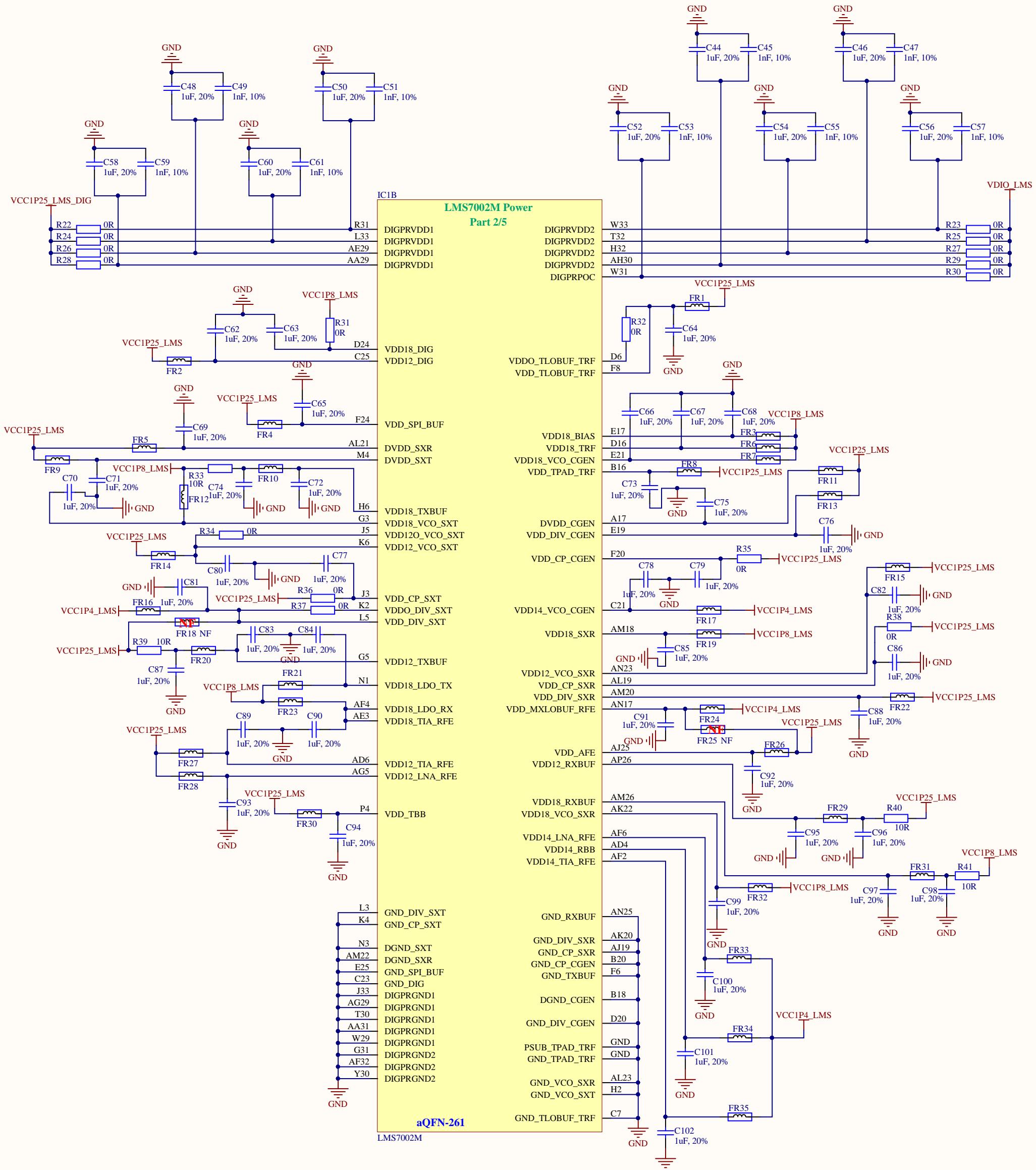
File: 06\_LMS7002M\_RF2.SchDoc

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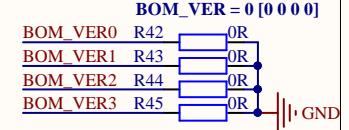
NF elements on sheet: FR18, FR25  
Number of NF elements on sheet: 2

## LMS7002M power supply circuit



## FPGA banks 1, 2, 3, 4

NF elements on sheet: -  
Number of NF elements on sheet: 0



A

**BANK 1**  
**VCC3P3**

IC8A  
VCC3P3

IO, DIFFIO\_L1p, (DQ2L)/(DQ1L)/(DQ1L)  
IO, DIFFIO\_L1n, (DQ2L)/(DQ1L)/(DQ1L)  
IO, DIFFIO\_L2p, (DQ2L)/(DQ1L)/(DQ1L)  
IO, DIFFIO\_L2n, (DQ2L)/(DQ1L)/(DQ1L)  
IO, VREFB1N0  
IO, DIFFIO\_L4p, (nRESET), (DQ2L)/(DQ1L)/(DQ1L)  
IO, DIFFIO\_L4n, (DQ2L)/(DQ1L)/(DQ1L)  
IO, DIFFIO\_L7p, (DQS2L/CQ3L,CDPCLK0)/(DQS2L/CQ3L,CDPCLK0)  
IO, DIFFIO\_L7n, (DQ2L)/(DQ1L)/(DQ1L)  
IO, DIFFIO\_L8p, (DQ2L)/(DQ1L)/(DQ1L)  
IO, DIFFIO\_L8n, (DATA1,ASDO)  
IO, VREFB1N1  
IO, DIFFIO\_L9p, (DQ2L)/(DQ1L)/(DQ1L)  
IO, DIFFIO\_L9n, (DQ2L)/(DQ1L)/(DQ1L)  
IO, DIFFIO\_L10p, (FLASH\_nCE,nCSO)  
IO, DIFFIO\_L10n, (.),(DQ1L)/(DQ1L)  
IO, DIFFIO\_L12p, (DM2L)/(DM1L/BWS#1L)/(DM1L/BWS#1L)  
IO, DIFFIO\_L12n, (DQ0L)/(DQ1L)/(DQ1L)  
IO, DIFFIO\_L14p  
IO, DIFFIO\_L14n  
IO, DIFFIO\_L18n  
IO, VREFB1N2  
IO, DIFFIO\_L20p  
IO, DIFFIO\_L20n  
IO, DIFFIO\_L21p  
IO, DIFFIO\_L21n  
IO, FX3\_LED\_R  
IO, FPGA\_SPI1\_MOSI  
IO, FPGA\_SPI1\_SCLK  
IO, FPGA\_I2C\_SDA  
IO, BRDG\_SPI\_FPGA\_SS  
IO, FPGA\_LED2\_G  
IO, H2\_FPGA\_GPIO2  
IO, H1\_FPGA\_GPIO3  
IO, J3\_FPGA\_SPI1\_DAC\_SS  
IO, J2\_ADF\_MUXOUT  
IO, J1\_FPGA\_UART\_RX  
IO, K1\_FPGA\_AS\_DATA0  
G4\_FPGA\_GPIO4  
G3\_FPGA\_GPIO5  
B2\_BRDG\_SPI\_SCLK  
B1\_BRDG\_SPI\_MOSI  
J5\_FX3\_LED\_G  
E4\_FAN\_CTRL  
E3\_FPGA\_LED1\_R  
C2\_FPGA\_CLK\_OUT  
C1\_BRDG\_SPI\_MISO  
D1\_FPGA\_AS\_ASDO  
J7\_FPGA\_I2C\_SCL  
H6\_FPGA\_GPIO1  
J6\_LM75\_OS  
E2\_FPGA\_AS\_NCSO  
E1\_FPGA\_LED2\_R  
F2\_FPGA\_GPIO6  
F1\_FPGA\_GPIO7  
H8\_FPGA\_GPIO0  
J8\_FPGA\_UART\_TX  
S5\_FPGA\_SPI1\_ADF\_SS  
H5\_FX3\_LED\_R  
J8\_FPGA\_SPI1\_MOSI  
K8\_FPGA\_SPI1\_SCLK  
J7\_FPGA\_I2C\_SDA  
K7\_BRDG\_SPI\_FPGA\_SS  
J4\_FPGA\_LED2\_G  
H2\_FPGA\_GPIO2  
H1\_FPGA\_GPIO3  
J3\_FPGA\_SPI1\_DAC\_SS  
J2\_ADF\_MUXOUT  
J1\_FPGA\_UART\_RX  
K1\_FPGA\_AS\_DATA0  
IO, (DQS0L/CQ1L,DPCLK0)/(DQS0L/CQ1L,DPCLK0)  
IO, DIFFIO\_L23p, (DQ0L)/(DQ1L)/(DQ1L)  
IO, DIFFIO\_L23n, (DQ0L)/(DQ1L)/(DQ1L)  
IO, VREFB1N3  
IO, DIFFIO\_L24p, (DQ0L)/(DQ1L)/(DQ1L)  
IO, DIFFIO\_L24n, (DQ0L)/(DQ1L)/(DQ1L)  
IO, (DATA0)

EP4CE40F23C8N

IC8B  
**BANK 2**  
**VCC1P8**

IO, DIFFIO\_L26p, (DQ0L)/(DQ1L)/(DQ1L)  
IO, DIFFIO\_L26n, (DQ0L)/(DQ1L)/(DQ1L)  
IO, DIFFIO\_L27p, (DQ0L)/(DQ1L)/(DQ1L)  
IO, DIFFIO\_L27n, (.),(DQ1L)/(DQ1L)  
IO, DIFFIO\_L28p, (DM0L)/(DM1L/BWS#1L)/(DM1L/BWS#1L)  
IO, DIFFIO\_L28n, (DQ1L)/(DQ3L)/(DQ1L)  
IO, DIFFIO\_L30n, (DQ1L)/(DQ3L)/(DQ1L)  
IO, VREFB2N0  
IO, DIFFIO\_L32p, (DQ1L)/(DQ3L)/(DQ1L)  
IO, DIFFIO\_L32n, (DQ1L)/(DQ3L)/(DQ1L)  
IO, DIFFIO\_L33p, (DQ1L)/(DQ3L)/(DQ1L)  
IO, DIFFIO\_L33n, (DQ1L)/(DQ3L)/(DQ1L)  
IO, (DQS1L/CQ1L#,DPCLK1)/(DQS1L/CQ1L#,DPCLK1)  
IO, DIFFIO\_L34n, (DQ1L)/(DQ3L)/(DQ1L)  
IO, DIFFIO\_L35p, (DM1L/BWS#1L)/(DM3L/BWS#1L)/(DM1L/BWS#1L)  
IO, DIFFIO\_L35n, (DQ3L)/(DQ3L)/(DQ1L)  
IO, DIFFIO\_L38p, (DQ3L)/(DQ3L)/(DQ1L)  
IO, DIFFIO\_L38n, (DQ3L)/(DQ3L)/(DQ1L)  
IO, VREFB2N1  
IO, DIFFIO\_L41p, (DQ3L)/(DQ1L)/(DQ1L)  
IO, DIFFIO\_L41n, (DQ1L)/(DQ1L)/(DQ1L)  
IO, DIFFIO\_L42p, (DQ1L)/(DQ1L)/(DQ1L)  
IO, DIFFIO\_L42n, (DQ1L)/(DQ1L)/(DQ1L)  
IO, DIFFIO\_L44p, (DQ3L)/(DQ3L)/(DQ1L)  
IO, DIFFIO\_L44n, (DQ3L)/(DQ3L)/(DQ1L)  
IO, DIFFIO\_L45p, (DQ3L)/(DQ3L)/(DQ1L)  
IO, DIFFIO\_L45n, (DQ3L)/(DQ3L)/(DQ1L)  
IO, VREFB2N2  
IO, DIFFIO\_L49p, (DQ3L)/(DQ3L)/(DQ1L)  
IO, DIFFIO\_L49n, (DQ3L)/(DQ3L)/(DQ1L)  
IO, DIFFIO\_L50n, (DQ3L)/(DQ3L)/(DQ1L)  
IO, RUP1  
IO, RDN1  
IO, DIFFIO\_L52p, (DQ3L)/(DQ3L)/(DQ1L)  
IO, (DQS3L/CQ3L#,CDPCLK1)/(DQS3L/CQ3L#,CDPCLK1)  
IO, VREFB2N3  
IO, DIFFIO\_L53p, (DQ3L)/(DQ3L)/(DQ1L)  
IO, DIFFIO\_L53n, (DQ3L)/(DQ3L)/(DQ1L)  
P4  
P3  
U2\_BOM\_VER2  
U1\_BOM\_VER3  
Y2\_DDR2\_2\_BA2  
V1\_DDR2\_1\_BA2  
P5  
N6\_FX3\_CTL12  
M7\_FX3\_CTL7  
M8\_FX3\_CTL8  
T8\_DDR2\_2\_A7  
W2\_DDR2\_1\_A11  
W1\_DDR2\_1\_A0  
Y2\_DDR2\_1\_A6  
Y1\_DDR2\_1\_A8  
T3  
N7\_FX3\_DCTL10  
P7\_DDR2\_2\_A5  
AA1\_DDR2\_1\_A4  
Y4\_DDR2\_1\_BA0  
Y3\_DDR2\_1\_BA1  
P6\_DDR2\_1\_ODT  
T5\_DDR2\_1\_RASn  
T4\_DDR2\_1\_CASn  
R5  
R6\_DDR2\_1\_CSn  
R7\_DDR2\_1\_CKE  
T7\_DDR2\_1\_WEn

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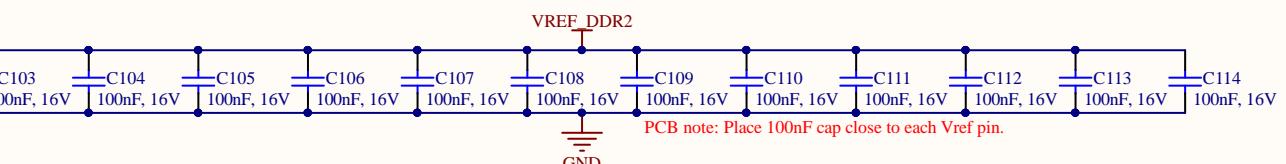
B

**BANK 3**  
**VCC1P8**

IC8C  
VCC1P8

IO, DIFFIO\_B1p, (DM3B/BWS#3B)/(DM3B/BWS#3B)/(DM5B/BWS#5B)  
IO, DIFFIO\_B3p, (DQ1L)/(DQ1L)/(DQ1L)  
IO, VREFB3N3  
Y4  
Y6\_DDR2\_1\_A3  
Y5\_DDR2\_1\_DM1  
U7\_DDR2\_1\_CLK\_P  
U8\_DDR2\_1\_CLK\_N  
VREF\_DDR2  
Y3\_DDR2\_1\_A2  
Y6\_DDR2\_1\_A10  
AA3\_DDR2\_1\_A1  
AB3\_DDR2\_1\_A5  
W6\_DDR2\_1\_DQ8  
V7\_DDR2\_1\_A9  
AA4\_DDR2\_1\_DQ15  
VREF\_DDR2  
AA5\_DDR2\_1\_DQ9  
AB5\_DDR2\_1\_A7  
T8\_DDR2\_1\_A12  
T9\_DDR2\_2\_WEn  
W7\_DDR2\_1\_DQ10  
Y7\_DDR2\_1\_DQ13  
J9\_DDR2\_1\_DQ14  
V8\_DDR2\_1\_DQ11  
V8\_DDR2\_1\_DQ12  
AA7\_DDR2\_1\_DM0  
AB7\_DDR2\_1\_DQ2  
T8\_DDR2\_2\_CSn  
T10\_DDR2\_2\_CASn  
T11\_DDR2\_2\_RASn  
V9  
V10\_DDR2\_1\_DQS1  
U10\_DDR2\_1\_DQ0  
AA8\_DDR2\_1\_DQ6  
AB8\_DDR2\_1\_DQ1  
AA9\_DDR2\_1\_DQ3  
AB9\_DDR2\_1\_DQS0  
V11  
V11\_DDR2\_1\_DQ4  
U10\_DDR2\_1\_DQ5  
Y10\_DDR2\_1\_DQ7  
AA10\_DDR2\_2\_DM1  
AB10\_DDR2\_2\_CKE  
IO, VREFB3N1  
IO, DIFFIO\_B17n, (DQS5B)/(DQ3B)/(DQ5B)  
IO, DIFFIO\_B18p, (DQ5B)/(DQ3B)/(DQ5B)  
IO, DIFFIO\_B18n, (DQ5B)/(DQ3B)/(DQ5B)  
IO, DIFFIO\_B21p, (DQ5B)/(DQ3B)/(DQ5B)  
IO, VREFB3N0  
IO, DIFFIO\_B25n, (DQ5B)/(DQ3B)/(DQ5B)  
IO, DIFFIO\_B26p, (DQ5B)/(DQ3B)/(DQ5B)  
IO, DIFFIO\_B26n, (DQ5B)/(DQ3B)/(DQ5B)  
IO, DIFFIO\_B27p, (DM4B)/(DM5B/BWS#5B)/(DM5B/BWS#5B)  
IO, DIFFIO\_B27n, (.),(DQ5B)/(DQ5B)

EP4CE40F23C8N



IC8D

**BANK 4**  
**VCC1P8**

IC8D  
VCC1P8

IO, DIFFIO\_B28p, (DQ4B)/(DQ5B)/(DQ5B)  
IO, DIFFIO\_B28n, (DQ4B)/(DQ5B)/(DQ5B)  
IO, DIFFIO\_B29p, (DQ4B)/(DQ5B)/(DQ5B)  
IO, DIFFIO\_B29n, (DQ4B)/(DQ5B)/(DQ5B)  
IO, VREFB4N3  
IO, DIFFIO\_B32p, (DQ4B)/(DQ5B)/(DQ5B)  
IO, DIFFIO\_B32n, (DQS4B/CQ5B,DPCLK4)/(DQS4B/CQ5B,CQ5B,DPCLK4)  
IO, DIFFIO\_B33p, (DQ4B)/(DQ5B)/(DQ5B)  
IO, DIFFIO\_B33n, (DQ4B)/(DQ5B)/(DQ5B)  
IO, DIFFIO\_B34p, (DQ4B)/(DQ5B)/(DQ5B)  
IO, DIFFIO\_B35p, (DM2B)/(DM5B/BWS#5B)/(DM5B/BWS#5B)  
IO, DIFFIO\_B35n, (DQ2B)/(DQ5B)/(DQ5B)  
IO, DIFFIO\_B36p, (DQ2B)/(DQ5B)/(DQ5B)  
IO, DIFFIO\_B36n, (DQ2B)/(DQ5B)/(DQ5B)  
IO, VREFB4N2  
IO, DIFFIO\_B38n, (DQ2B)/(DQ5B)/(DQ5B)  
IO, DIFFIO\_B39p, (DQ2B)/(DQ5B)/(DQ5B)  
IO, DIFFIO\_B39n, (DQ2B)/(DQ5B)/(DQ5B)  
IO, DIFFIO\_B40p, (DQ2B)/(DQ5B)/(DQ5B)  
IO, DIFFIO\_B41n, (DQ2B)/(DQ5B)/(DQ5B)  
IO, DIFFIO\_B42p, (DQ2B)/(DQ5B)/(DQ5B)  
IO, DIFFIO\_B42n, (DQ2B)/(DQ5B)/(DQ5B)  
IO, (DQS2B/CQ3B,DPCLK5)/(DQS2B/CQ3B,DPCLK5)/(DQS2B/CQ3B,DPCLK5)  
IO, VREFB4N2  
IO, DIFFIO\_B38n, (DQ2B)/(DQ5B)/(DQ5B)  
IO, DIFFIO\_B39p, (DQ2B)/(DQ5B)/(DQ5B)  
IO, DIFFIO\_B40p, (DQ2B)/(DQ5B)/(DQ5B)  
IO, DIFFIO\_B41n, (DQ2B)/(DQ5B)/(DQ5B)  
IO, DIFFIO\_B42p, (DQ2B)/(DQ5B)/(DQ5B)  
IO, DIFFIO\_B42n, (DQ2B)/(DQ5B)/(DQ5B)  
IO, DIFFIO\_B43p, (DQ2B)/(DQ5B)/(DQ5B)  
IO, DIFFIO\_B43n, (DQ2B)/(DQ5B)/(DQ5B)  
IO, VREFB4N1  
IO, RUP2  
IO, RDN2  
V17\_DDR2\_2\_DQ5  
Y17\_DDR2\_2\_A3  
AB13\_DDR2\_2\_DQ9  
AB13\_DDR2\_2\_DQ12  
AA14\_DDR2\_2\_DQ12  
AB14\_DDR2\_2\_DQ11  
VREF\_DDR2  
V12  
W14\_DDR2\_2\_DQ50  
W14\_DDR2\_2\_BA0  
Y14\_DDR2\_2\_DQ1  
U14\_DDR2\_2\_A12  
U15\_DDR2\_2\_A0  
IO, DIFFIO\_B39n, (DQ2B)/(DQ5B)/(DQ5B)  
IO, DIFFIO\_B40p, (DQ2B)/(DQ5B)/(DQ5B)  
IO, DIFFIO\_B41n, (DQ2B)/(DQ5B)/(DQ5B)  
IO, DIFFIO\_B42p, (DQ2B)/(DQ5B)/(DQ5B)  
IO, DIFFIO\_B42n, (DQ2B)/(DQ5B)/(DQ5B)  
IO, DIFFIO\_B43p, (DQ2B)/(DQ5B)/(DQ5B)  
IO, DIFFIO\_B43n, (DQ2B)/(DQ5B)/(DQ5B)  
IO, VREFB4N1  
IO, RUP2  
IO, RDN2  
V17\_DDR2\_2\_DQ5  
Y17\_DDR2\_2\_A3  
AB13\_DDR2\_2\_DQ9  
AB13\_DDR2\_2\_DQ12  
AA14\_DDR2\_2\_DQ12  
AB14\_DDR2\_2\_DQ11  
VREF\_DDR2  
R46 49.9R, 1%  
R47 49.9R, 1%  
GND

EP4CE40F23C8N

Project name: LimeSDR-USB\_1v4s.PjrPcb

Title: FPGA banks 1, 2, 3, 4

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Guildford GU2 7YG  
Surrey  
United Kingdom

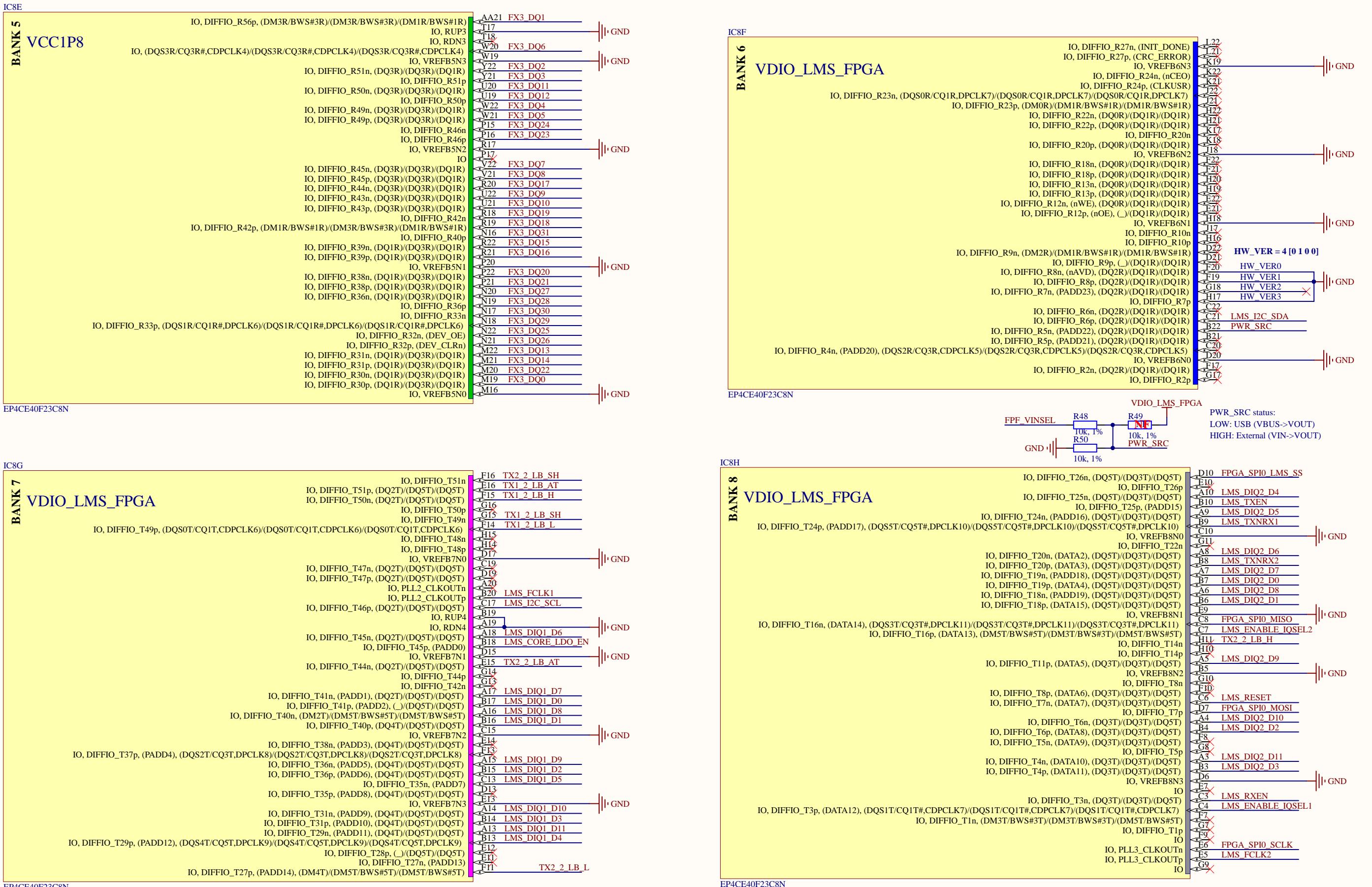
Size: A3 Revision: v1.4s

Date: 2017-02-01 Time: 15:10:25 Sheet 8 of 15

File: 08 FPGA banks 1\_2\_3\_4.SchDoc

NF elements on sheet: R49  
Number of NF elements on sheet: 1

## FPGA banks 5, 6, 7, 8



Project name: **LimeSDR-USB\_1v4s.PrbPcb**

Title: **FPGA banks 5, 6, 7, 8**

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Surrey  
United Kingdom



Size: **A3** Revision: **v1.4s**

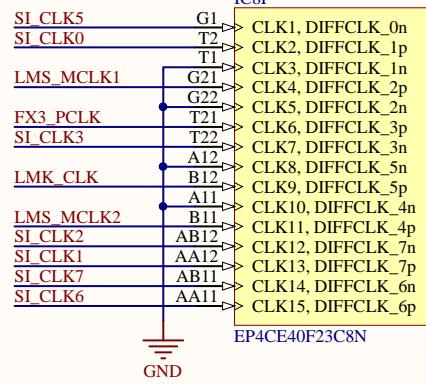
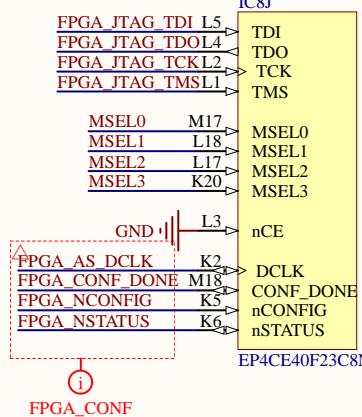
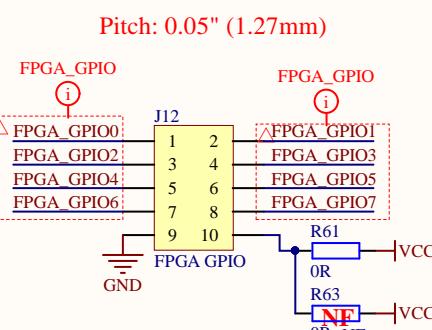
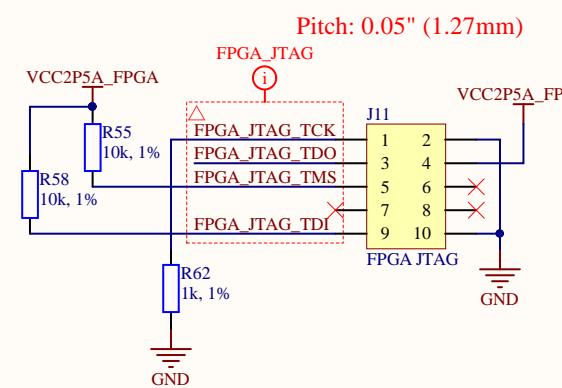
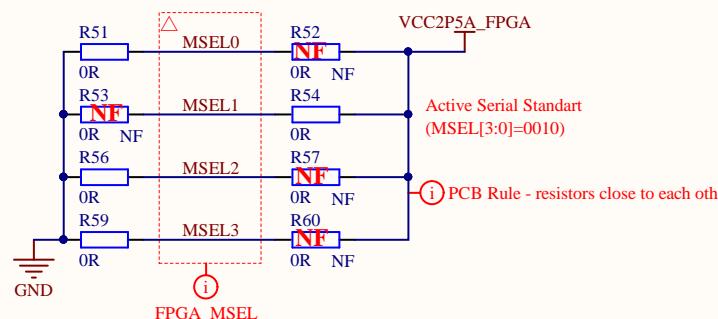
Date: **2017-02-01** Time: **15:10:28** Sheet **9** of **15**

File: **09\_FPGA\_banks\_5\_6\_7\_8.SchDoc**

NF elements on sheet: R52, R53, R57, R60, R63, R65, R74, J13, C142  
Number of NF elements on sheet: 9

## FPGA misc (power, clocks, config)

### MSEL config

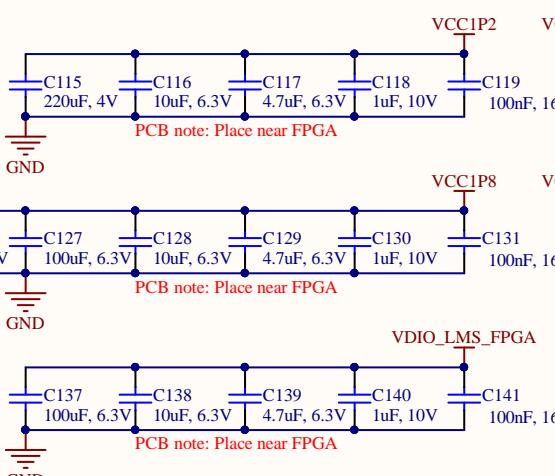
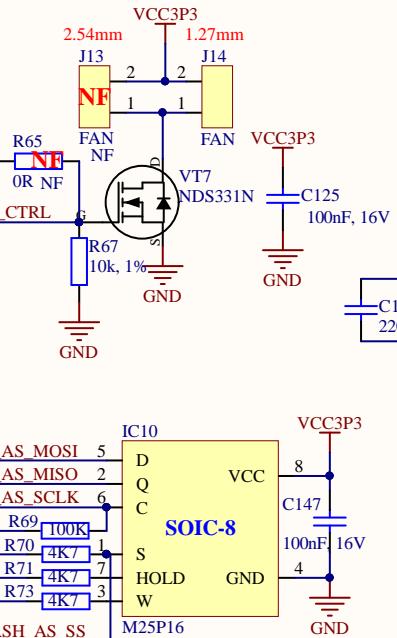
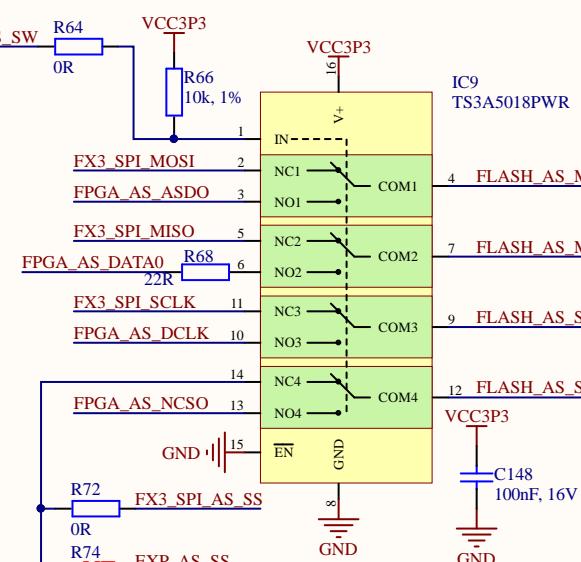


### FPGA AS FLASH + Switch

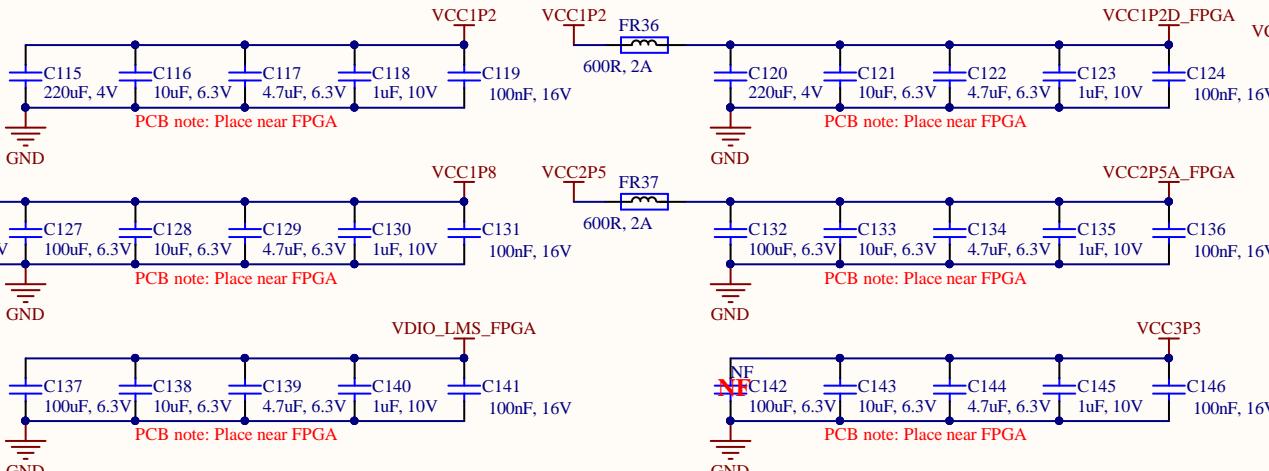
IN:

0: FLASH connected to FX3 (NC to COM)

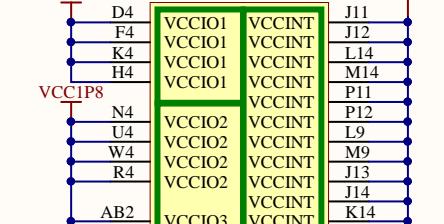
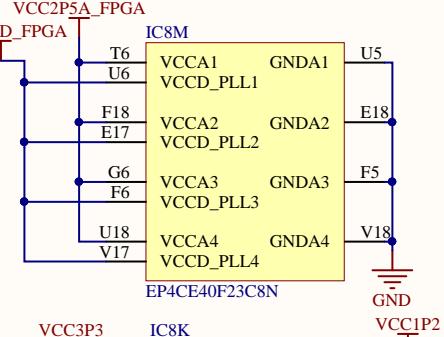
1: FLASH connected to FPGA (NO to COM)



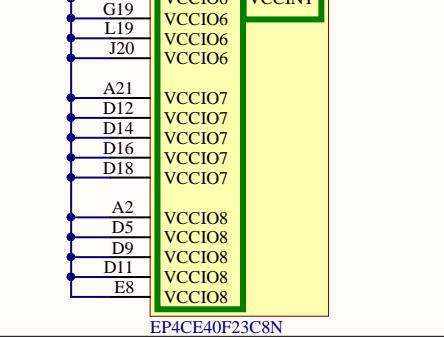
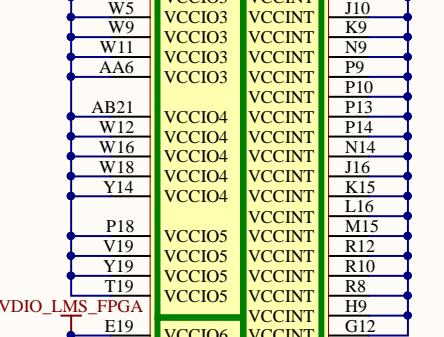
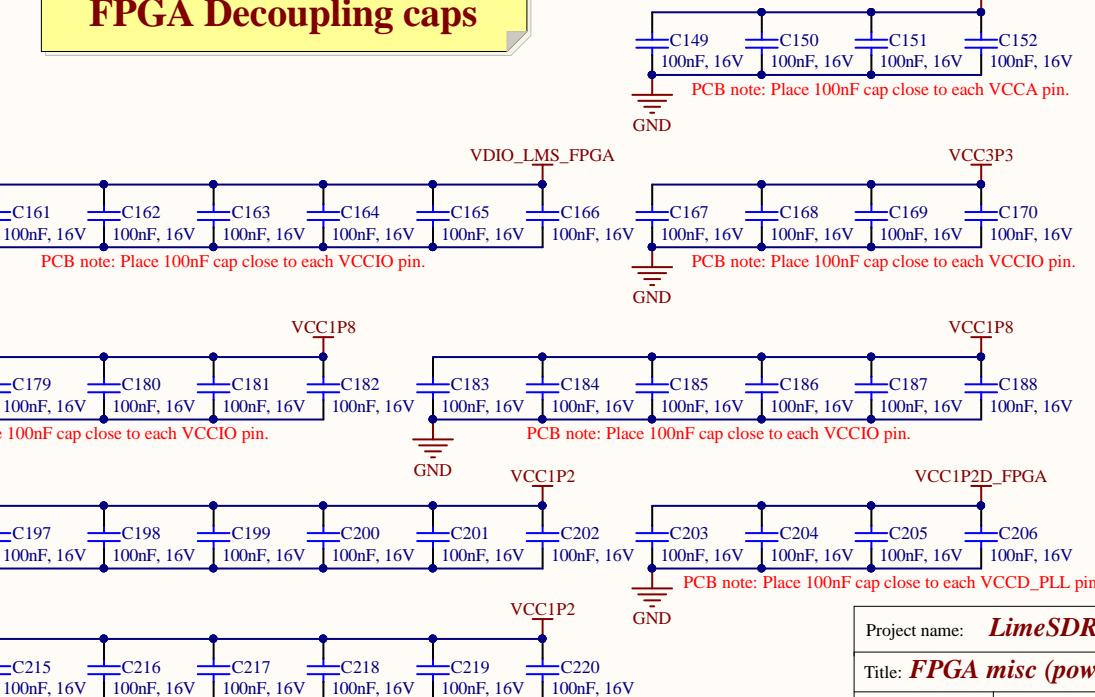
### FPGA Bulk caps



### FPGA Power



### FPGA Decoupling caps



L10	GND	GND	C16
L11	GND	GND	A22
M10	GND	GND	E20
M11	GND	GND	G20
L12	GND	GND	L20
L13	GND	GND	P19
M12	GND	GND	V20
M13	GND	GND	Y20
N11	GND	GND	AB22
K11	GND	GND	Y18
N12	GND	GND	Y16
K12	GND	GND	Y12
K13	GND	GND	Y11
N13	GND	GND	Y9
N10	GND	GND	Y5
K10	GND	GND	AB1
J9	GND	GND	N3
F12	GND	GND	U3
H12	GND	GND	W3
H13	GND	GND	D3
J15	GND	GND	F3
K16	GND	GND	K3
L15	GND	GND	G2
N15	GND	GND	AA2
R13	GND	GND	AA22
R11	GND	GND	H3
R9	GND	GND	R3
P8	GND	GND	AB6
A1	GND	GND	Y15
C5	GND	GND	T20
C9	GND	GND	J19
C11	GND	GND	C18
C12	GND	GND	D8
C14	GND	GND	GND

EP4CE40F23C8N

Project name: LimeSDR-USB\_1v4s.PrfPcb

Title: FPGA misc (power, clocks, config)

Size: A3 Revision: v1.4s

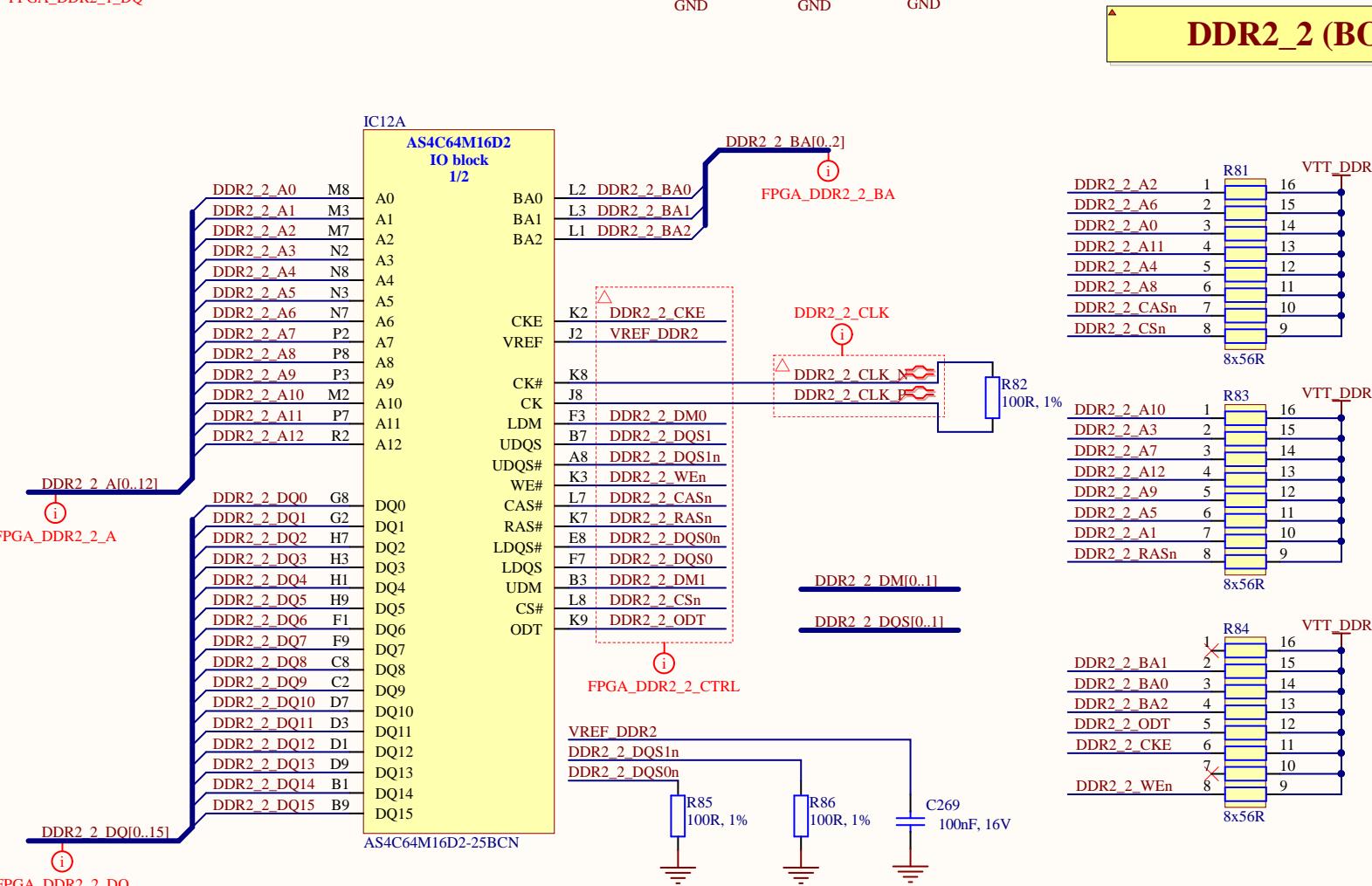
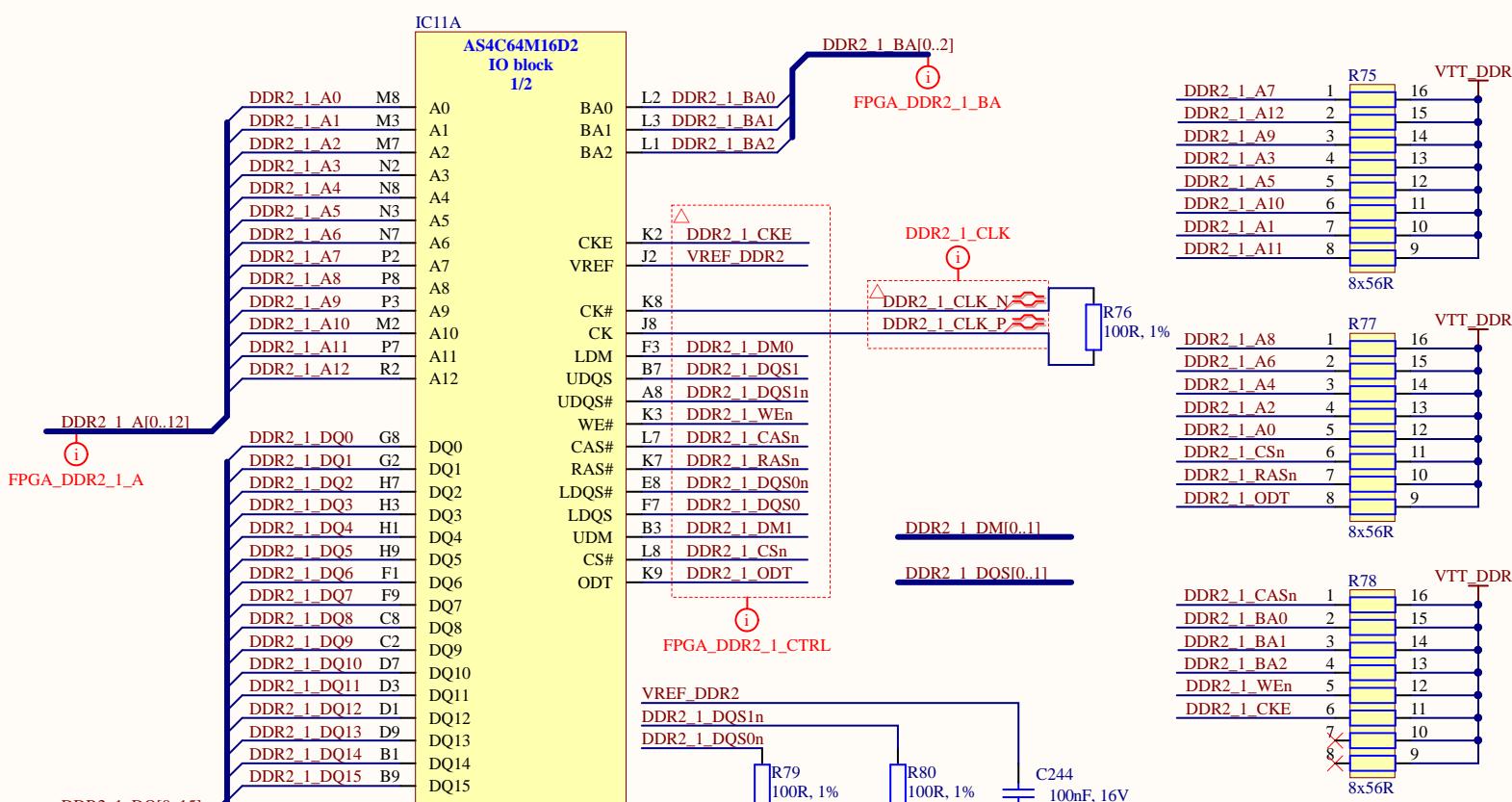
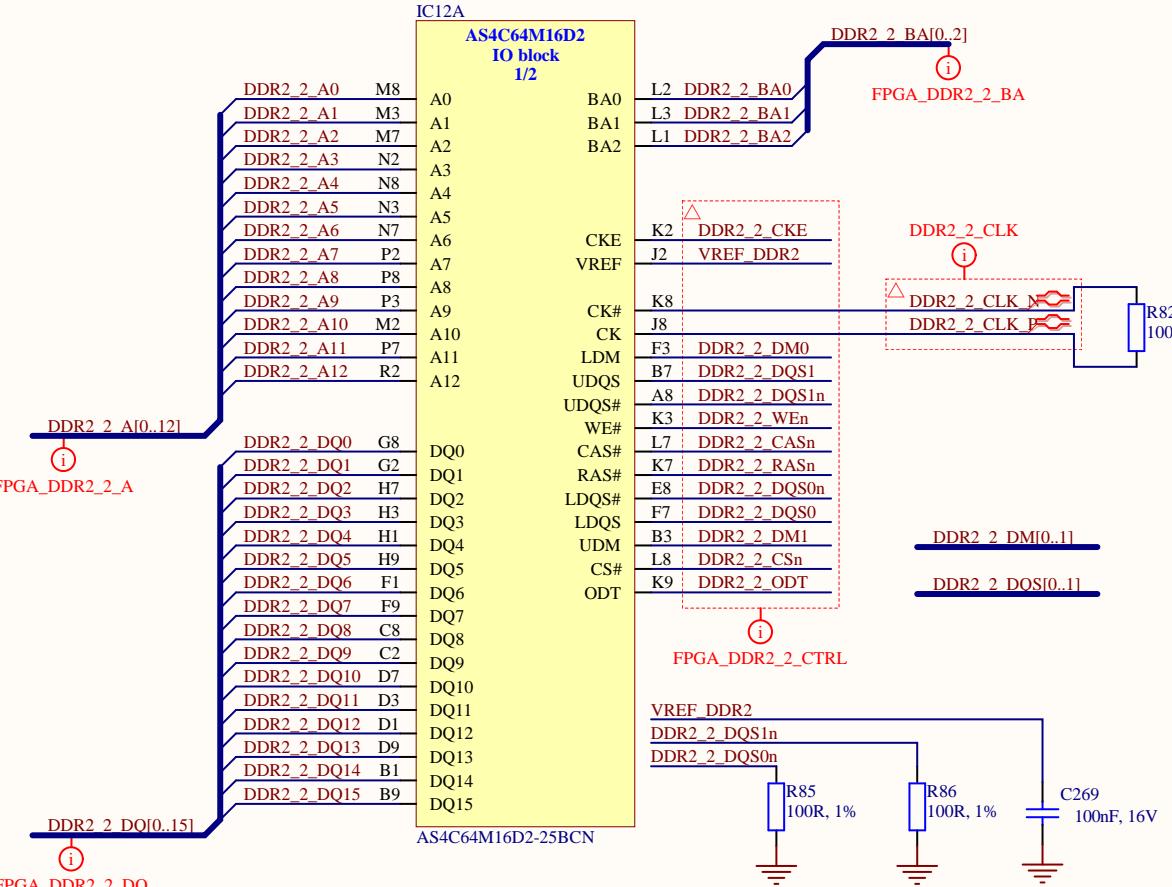
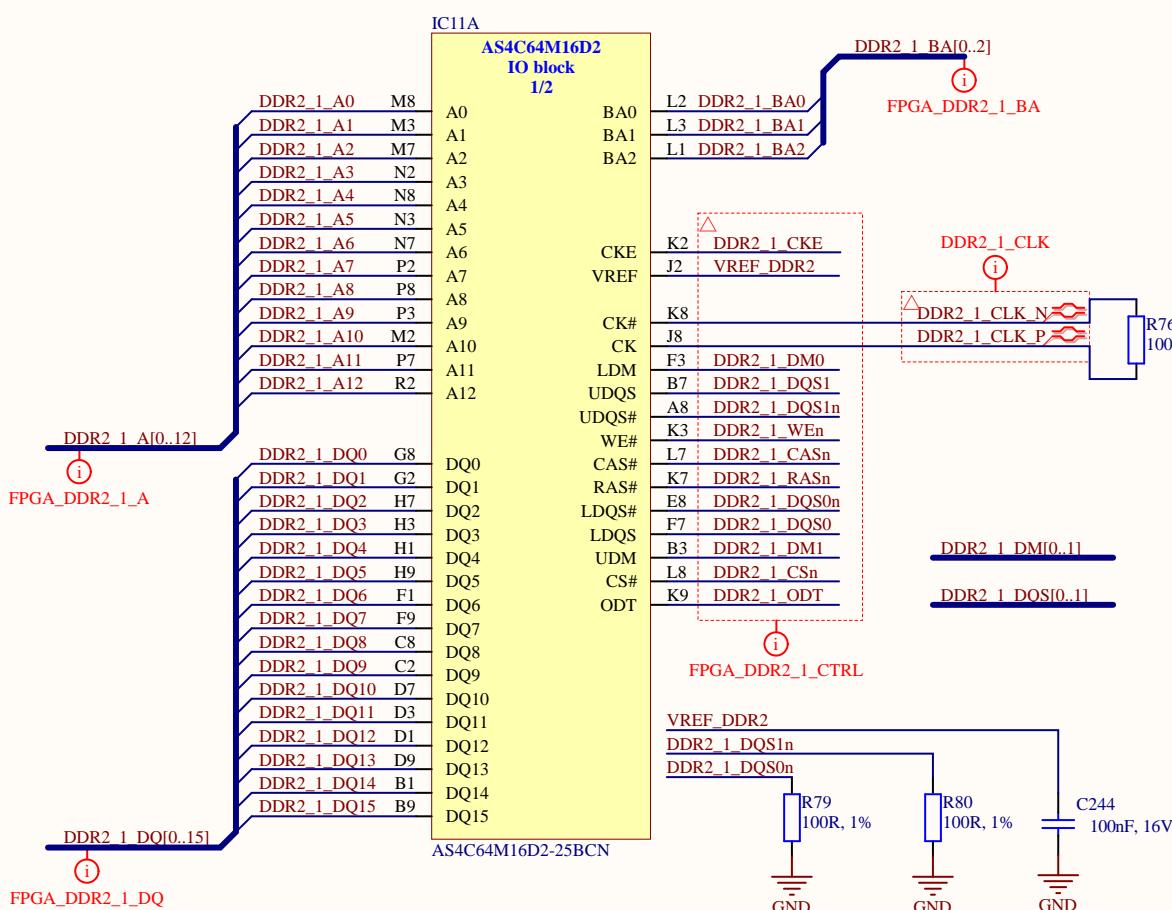
Date: 2017-02-01 Time: 15:10:33 Sheet 10 of 15

File: 10\_FPGA\_mis.SchDoc

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NF elements on sheet: -  
Number of NF elements on sheet: 0

## DDR2\_1 (BOT L)



Project name: LimeSDR-USB\_1v4s.PrbPcb

Title: RAM DDR2

Size: A3 Revision: v1.4s

Date: 2017-02-01 Time: 15:10:36 Sheet 11 of 15

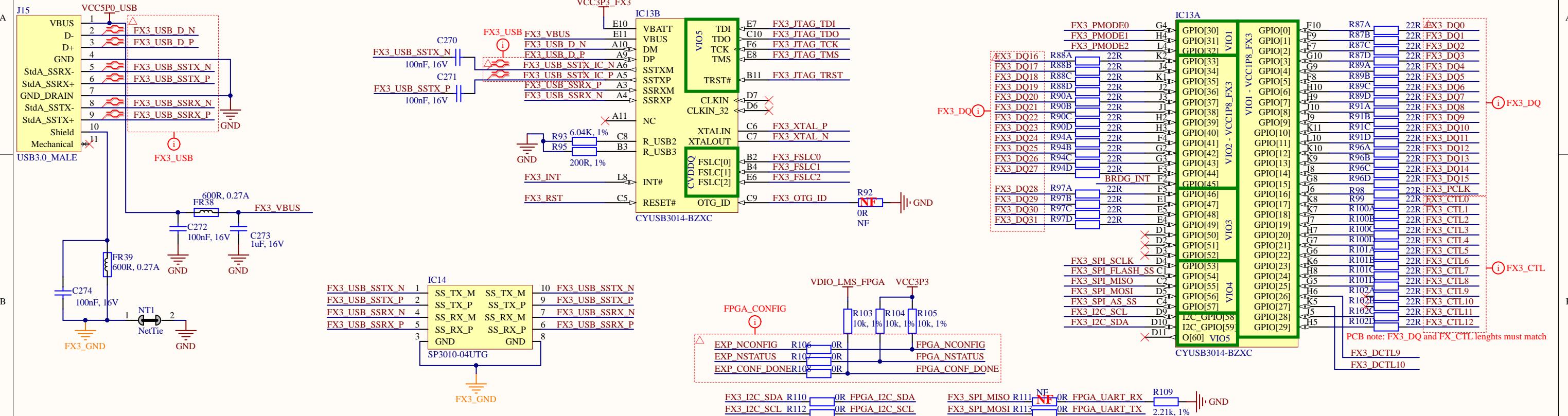
File: 11\_DDR2.SchDoc

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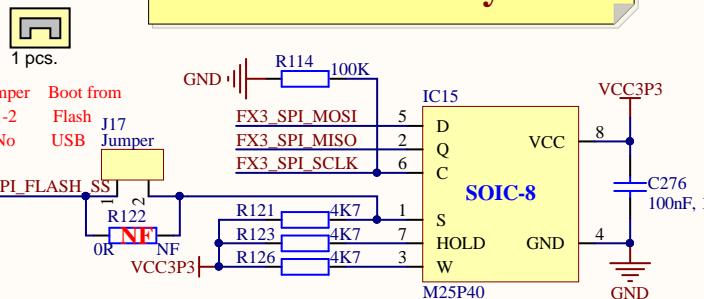


NF elements on sheet: R92, R111, R116, R119, R120, R122, R124, IC19  
Number of NF elements on sheet: 8

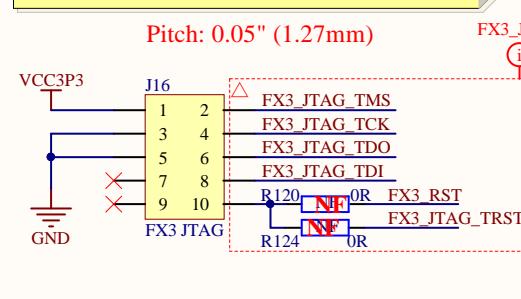
## FX3 (USB3) core



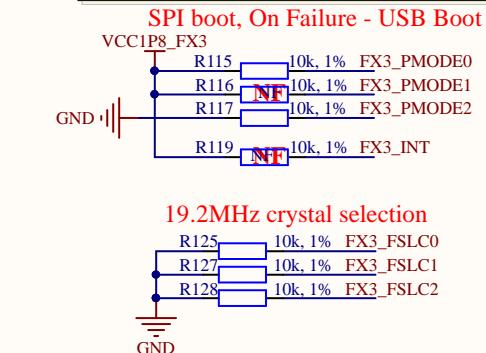
## FX3 memory



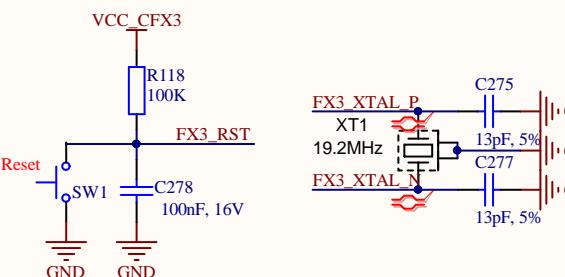
## FX3 JTAG (10 pin)



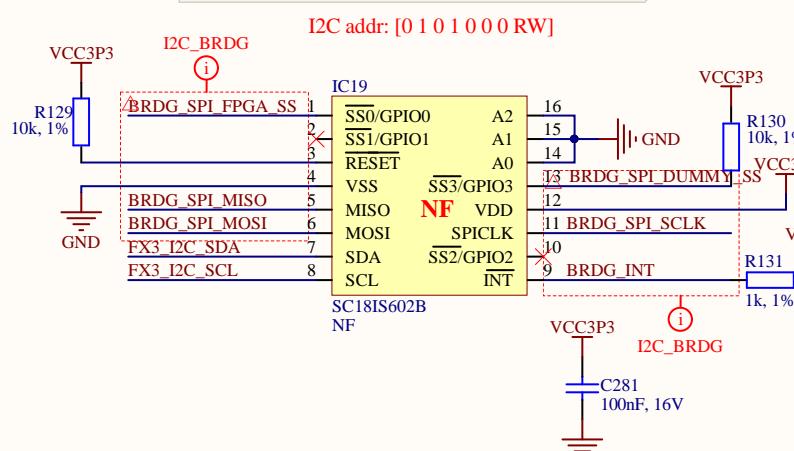
## FX3 Config



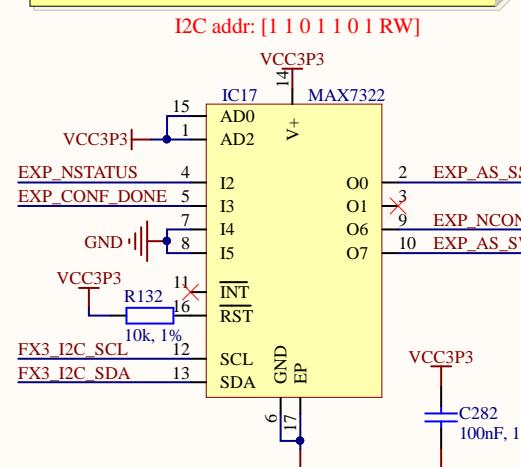
## FX3 Misc



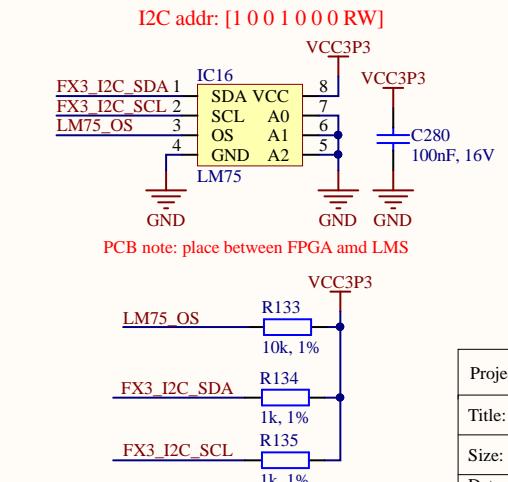
## I2C SPI Bridge



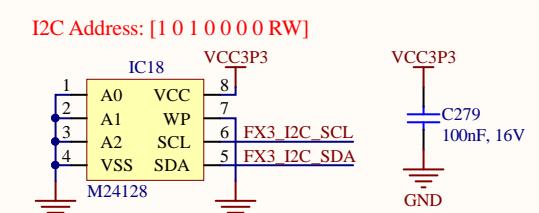
## I2C Port Expander



## I2C Temperature sensor



## I2C EEPROM



Project name: LimeSDR-USB\_1v4s.PrbPcb

Title: USB3.0 device

Size: A3 Revision: v1.4s

Date: 2017-02-01 Time: 15:10:40 Sheet 12 of 15

File: 12\_USB3\_0\_device.SchDoc

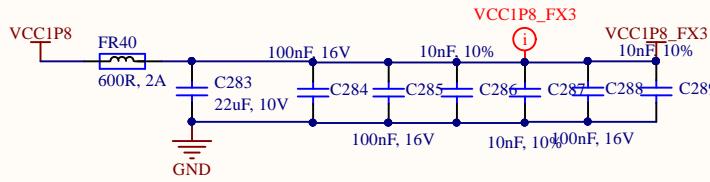
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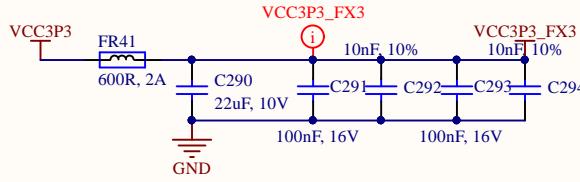
NF elements on sheet: FR42, FR43  
Number of NF elements on sheet: 2

## USB3 power

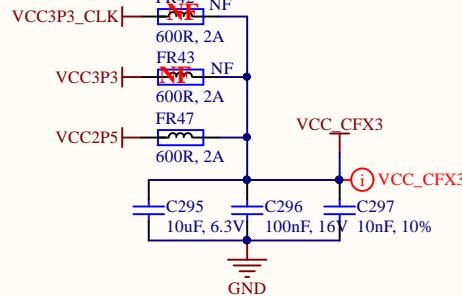
A



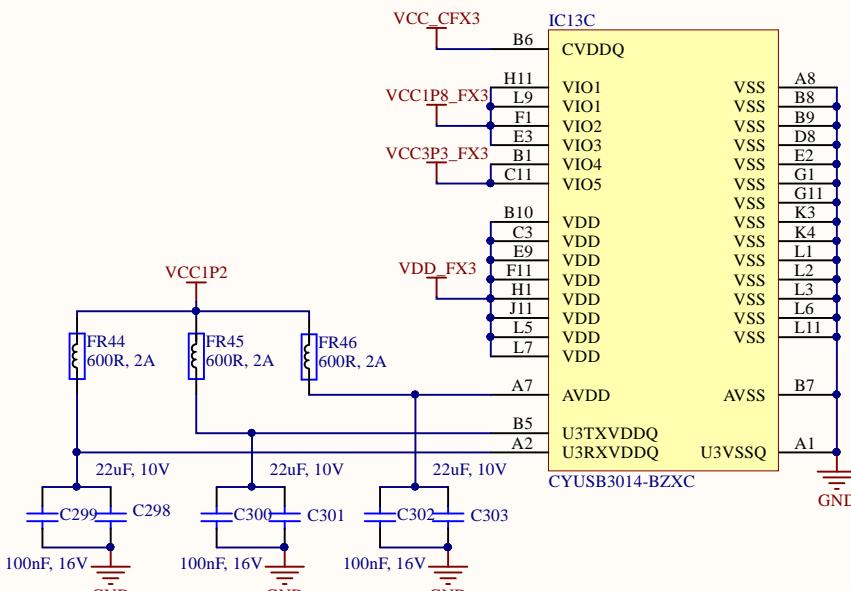
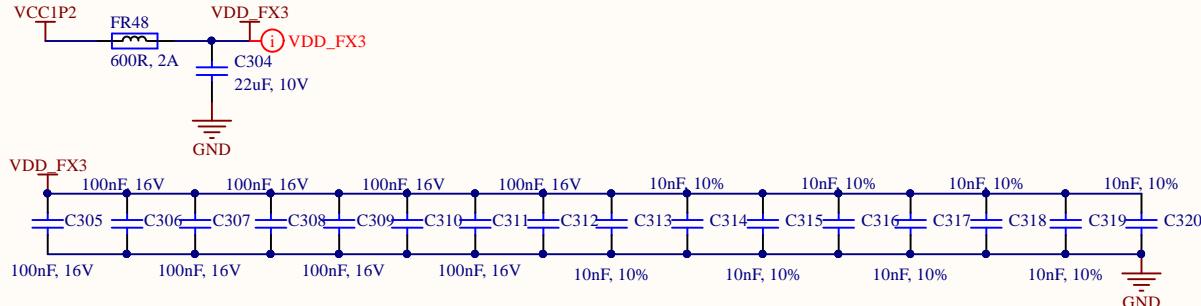
B



C



D



Project name: LimeSDR-USB\_1v4s.PrjPcb

Title: USB3.0 power

Size: A4 Revision: v1.4s

Date: 2017-02-01 Time: 15:10:44 Sheet 13 of 15

File: 13\_USB3\_0\_power.SchDoc

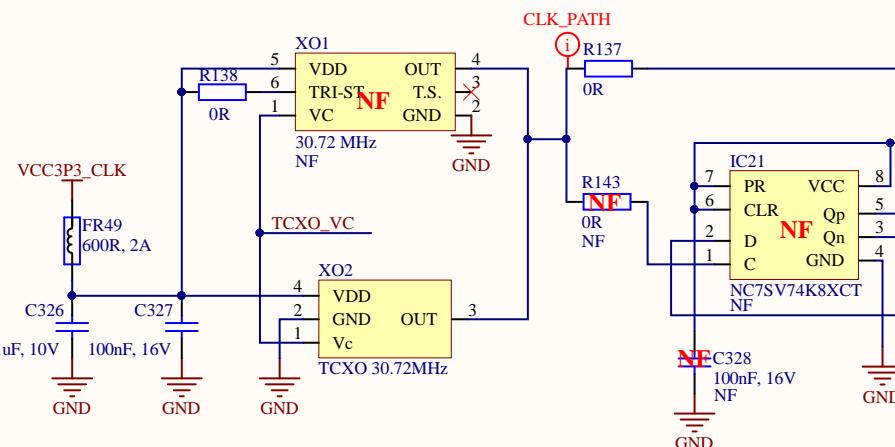
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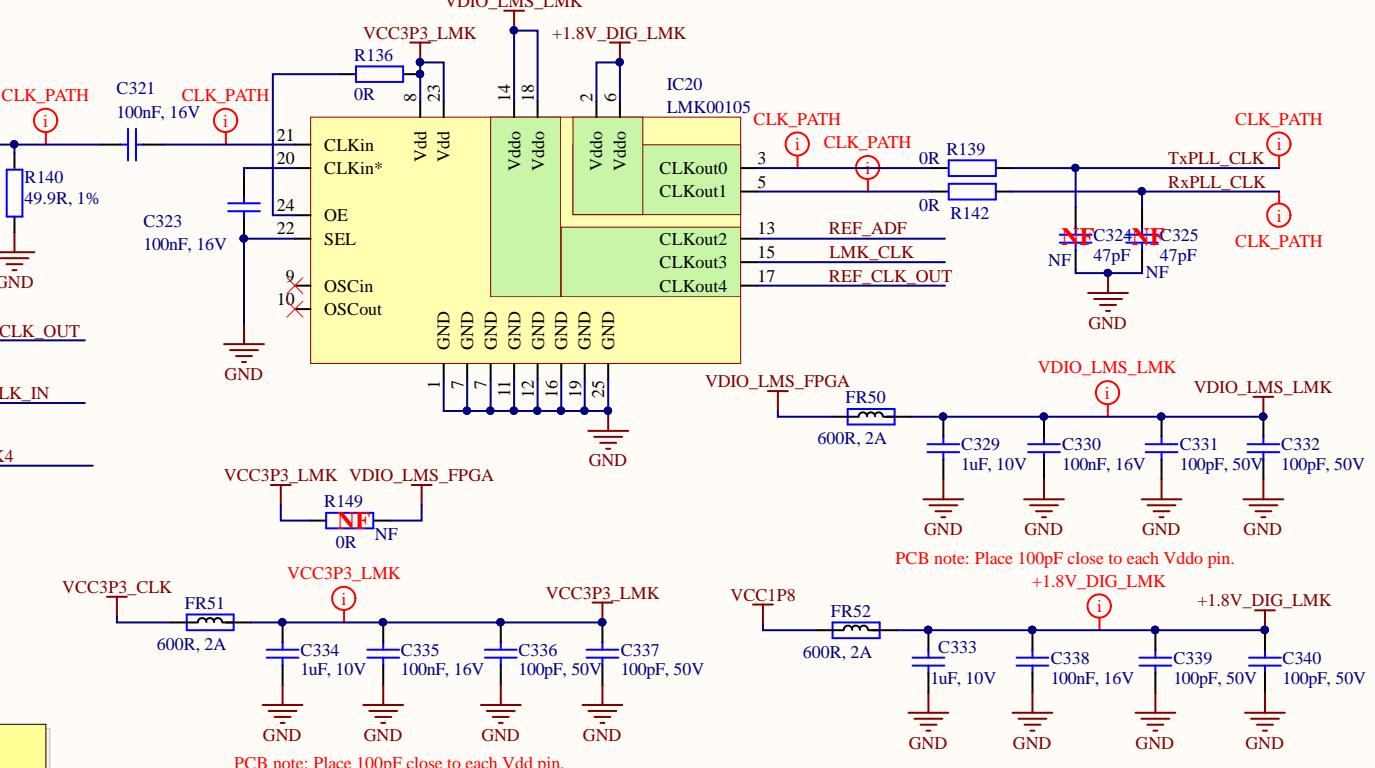
NF elements on sheet: XO1, R141, R143, R144, R145, R146, R147, R148, R149, R151, R155, C324, C325, C328, C341, IC21  
Number of NF elements on sheet: 16

## Clock circuits

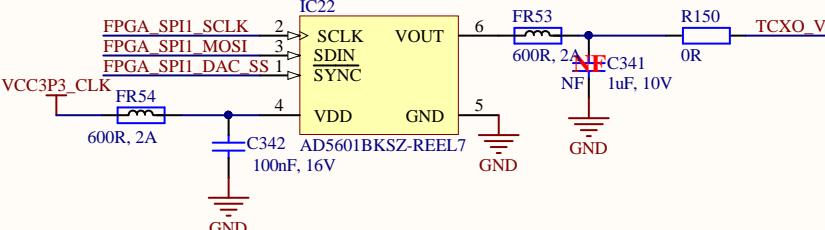
### (VC)TCXO



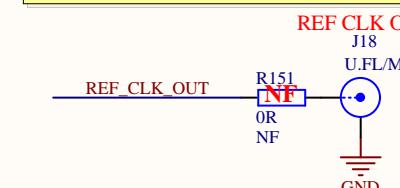
### Clock buffer



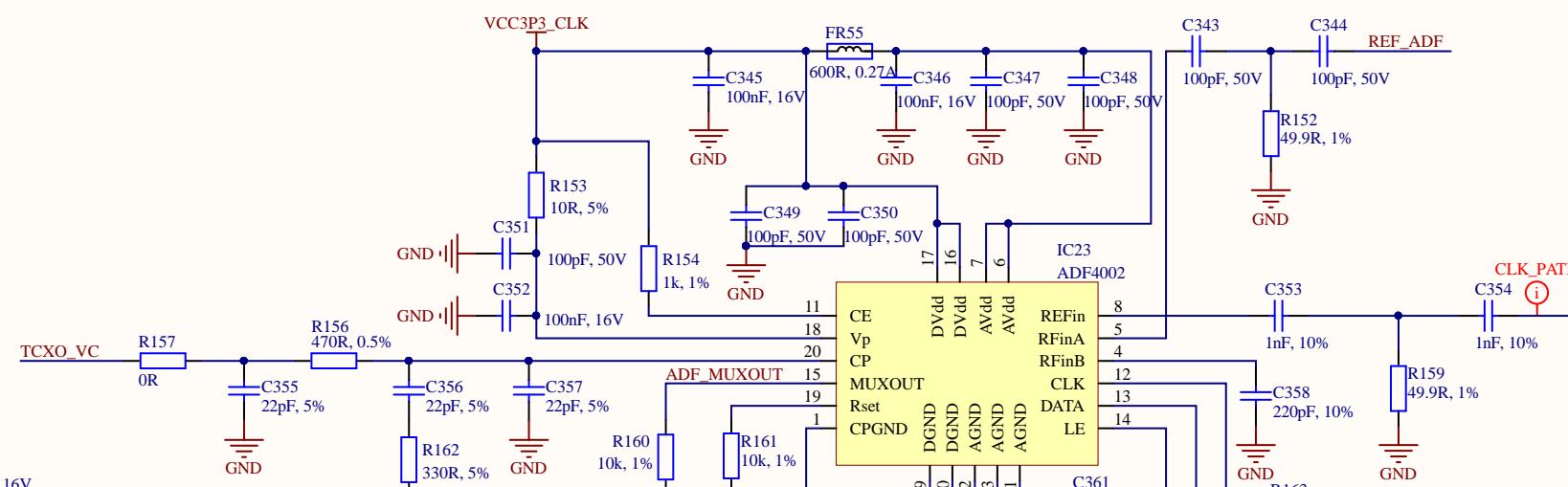
### TCXO DAC



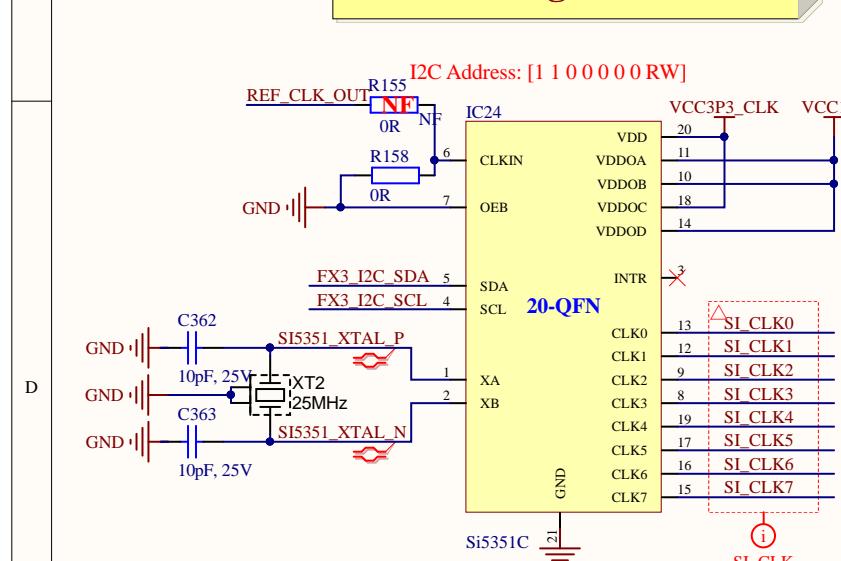
### REF CLK OUT



### Phase detector



### Clock generator



Project name: LimeSDR-USB\_1v4s.PrfPcb

Title: Clocks

Size: A3

Revision: v1.4s

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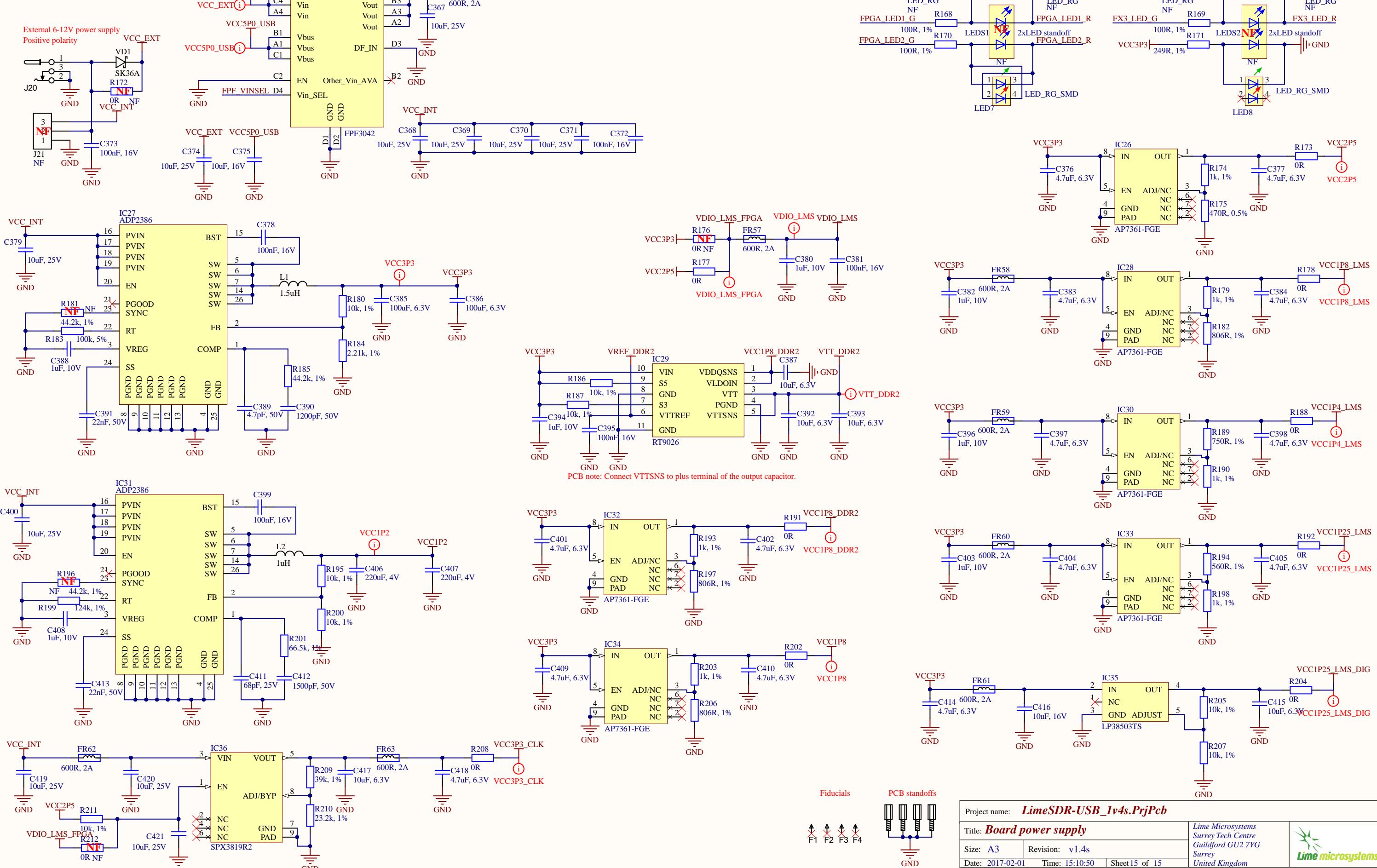
File: 14\_Clocks.SchDoc

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## Board power circuits

NF elements on sheet: R166, R167, R172, R176, R181, R196, R212, J21, LED3, LED4, LED5, LED6, LEDS1, LEDS2  
Number of NF elements on sheet: 14  
Total number of NF elements on all sheets: 60



Project name: **LimeSDR-USB\_1v4s.PrbPcb**

Title: **Board power supply**

Size: **A3** Revision: **v1.4s**

Date: **2017-02-01** Time: **15:10:50**

Sheet **15** of **15**

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