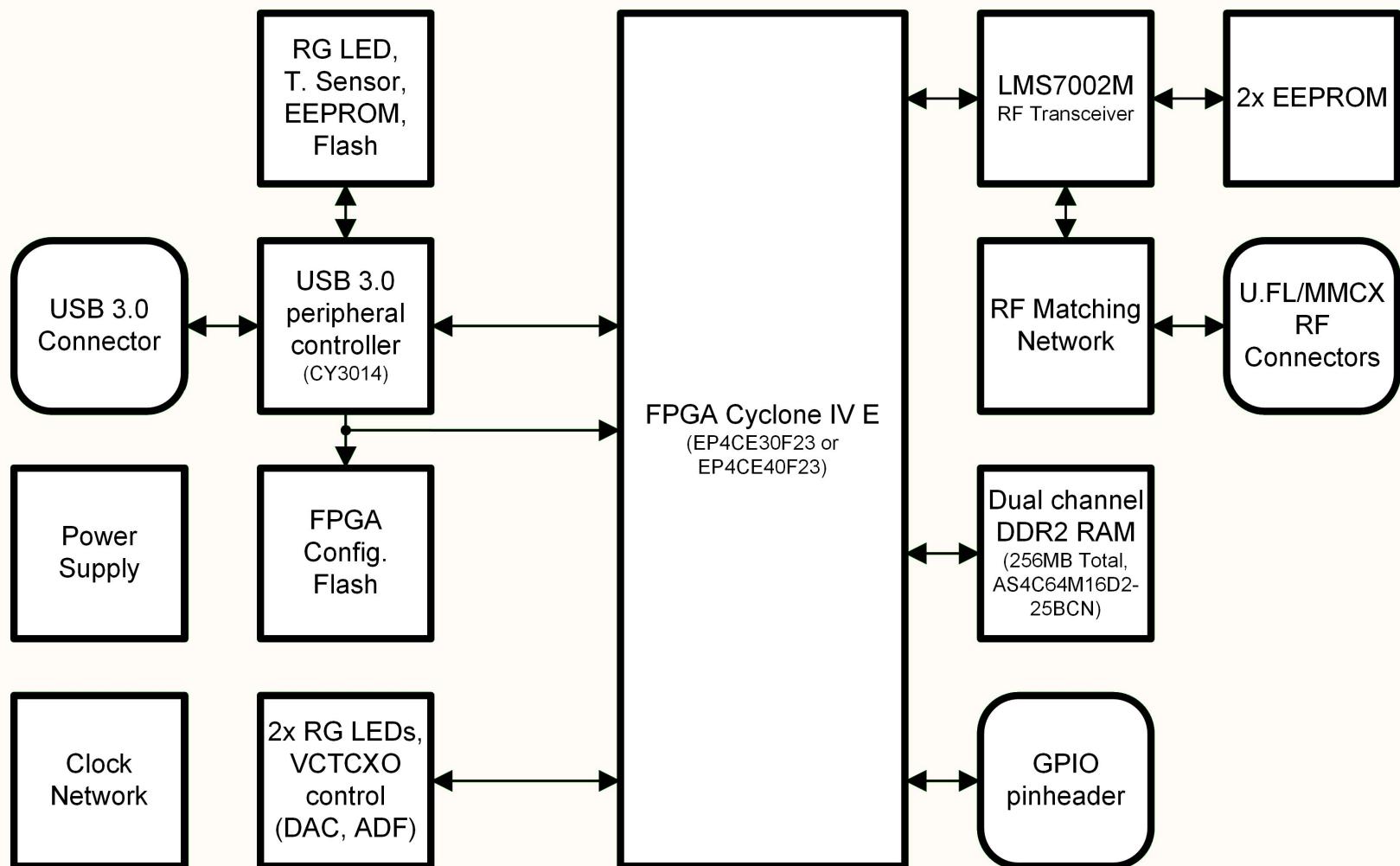


Block diagram



Project name: **LimeSDR_Iv2s.Pcb**

Title: **Block diagram**

Size: **A4** Revision: **v1.2**

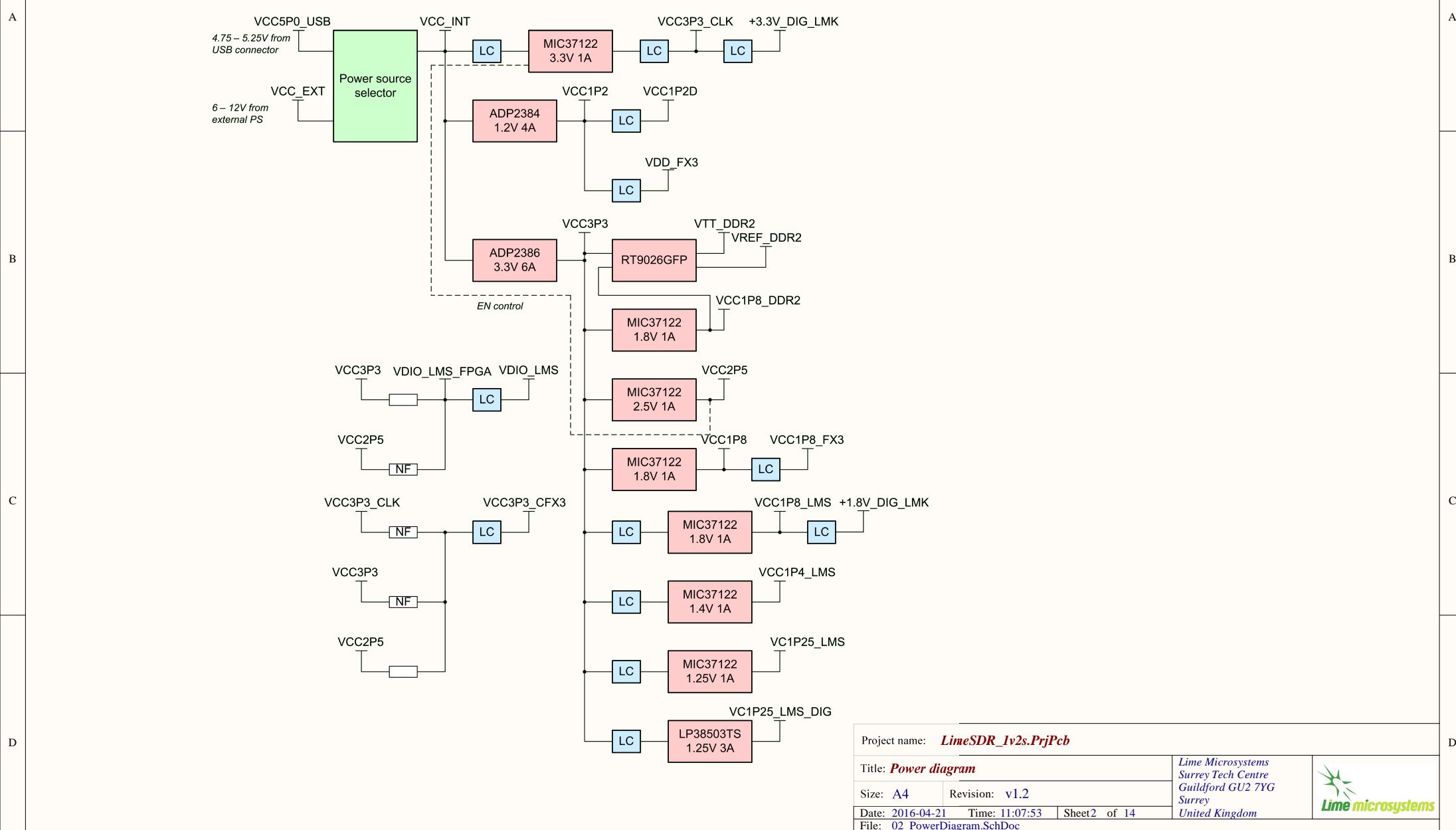
Date: 2016-04-21 Time: 11:07:49 Sheet 1 of 14

File: 01_BlockDiagram.SchDoc

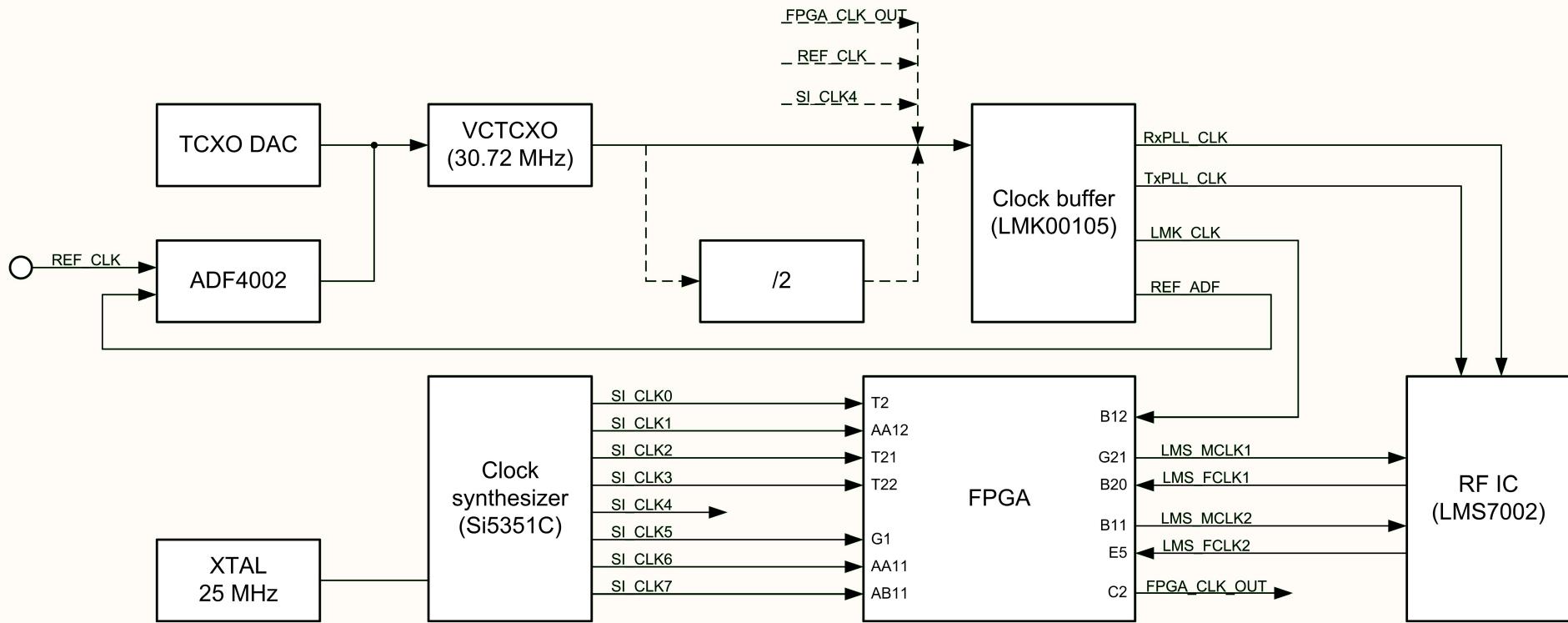
Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom



Power diagram



Clock diagram



Project name: **LimeSDR_Iv2s.PrbPcb**

Title: **Clock diagram**

Size: **A4** Revision: **v1.2**

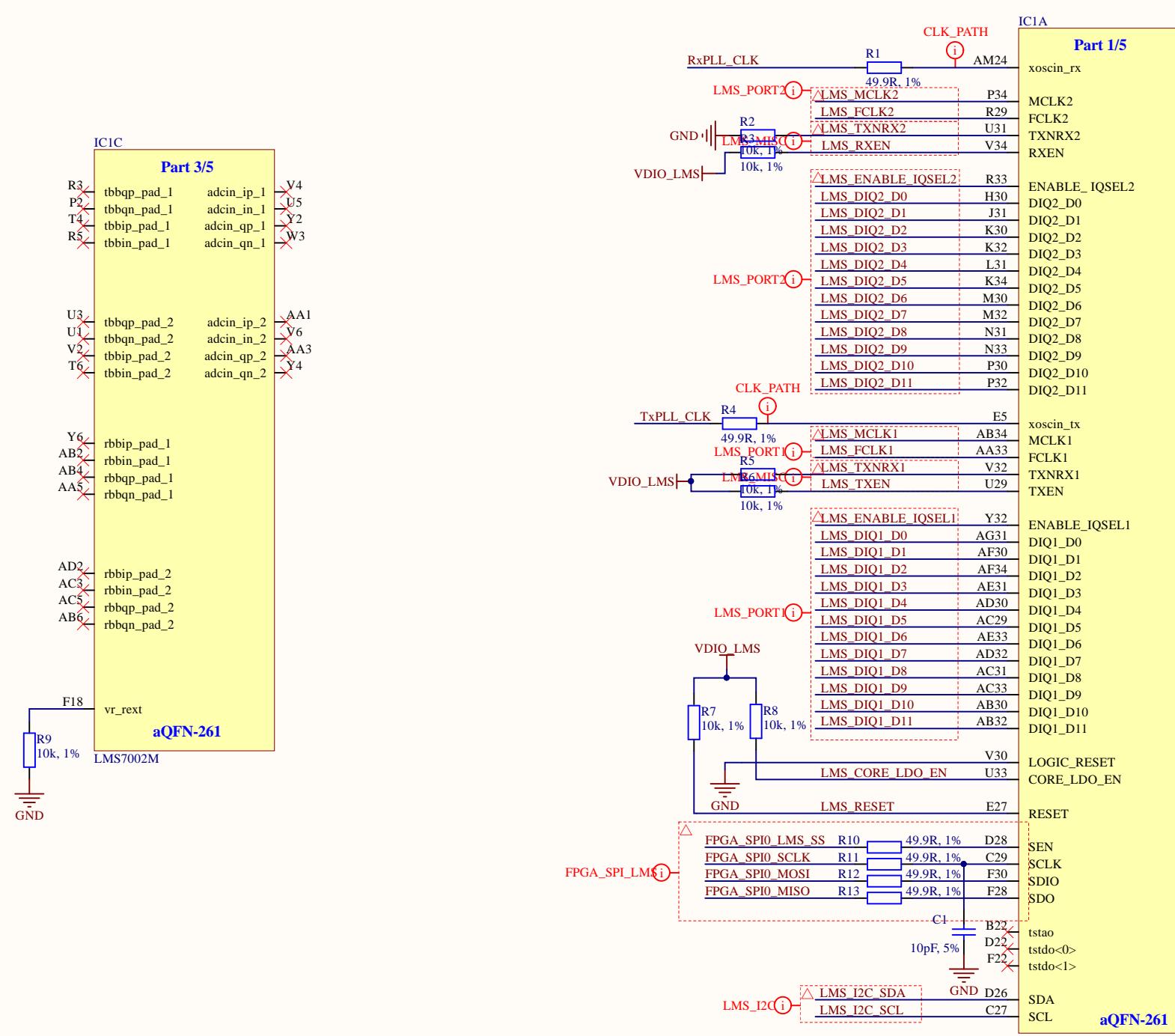
Date: 2016-04-21 Time: 11:08:04 Sheet 3 of 14

File: 03_ClockDiagram.SchDoc

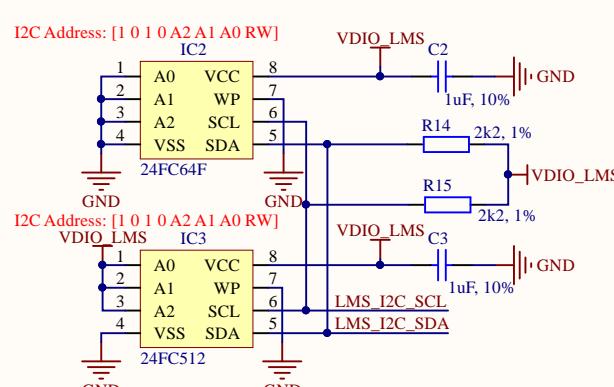
Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom



LMS7002M digital circuit



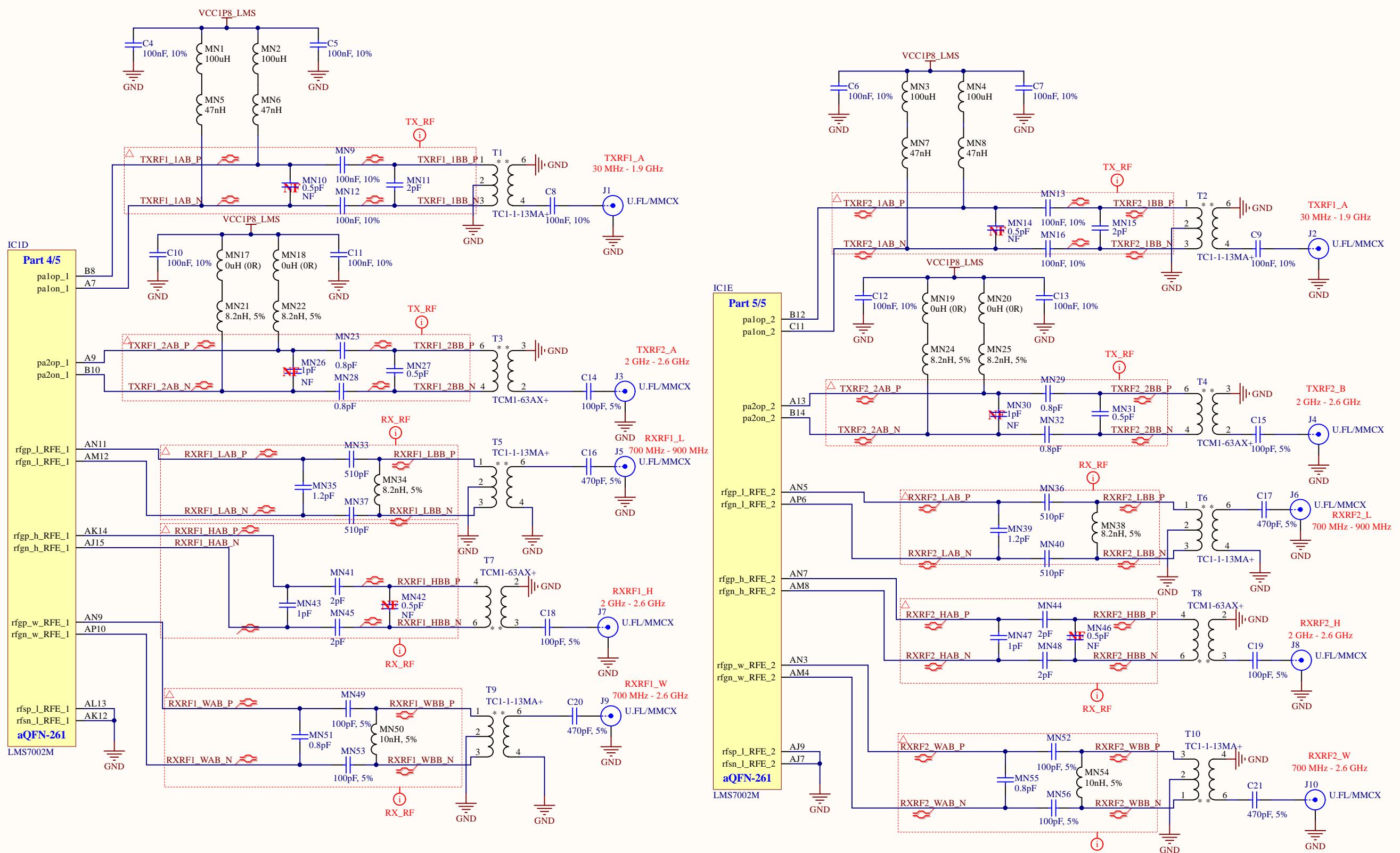
LMS EEPROMs



Project name: LimeSDR_1v2s.PrjPcb			
Title: LMS7002M digital circuit		Lime Microsystems	
Size: A3	Revision: v1.2	Surrey Tech Centre	
Date: 2016-04-21	Time: 11:08:09	Guildford GU2 7YG	
File: 04_LMS7002M_Digital.SchDoc	Sheet 4 of 14	Surrey	United Kingdom
			Lime Microsystems

NF elements on sheet: MN10, MN26, MN42, MN14, MN30, MN46
Number of NF elements on sheet: 6

LMS7002M RF circuits



Project name: LimeSDR_Iv2s.PrbPcb

Title: LMS7002M RF

Size: A3 Revision: v1.2

Date: 2016-04-21 Time: 11:08:12 Sheet 5 of 14

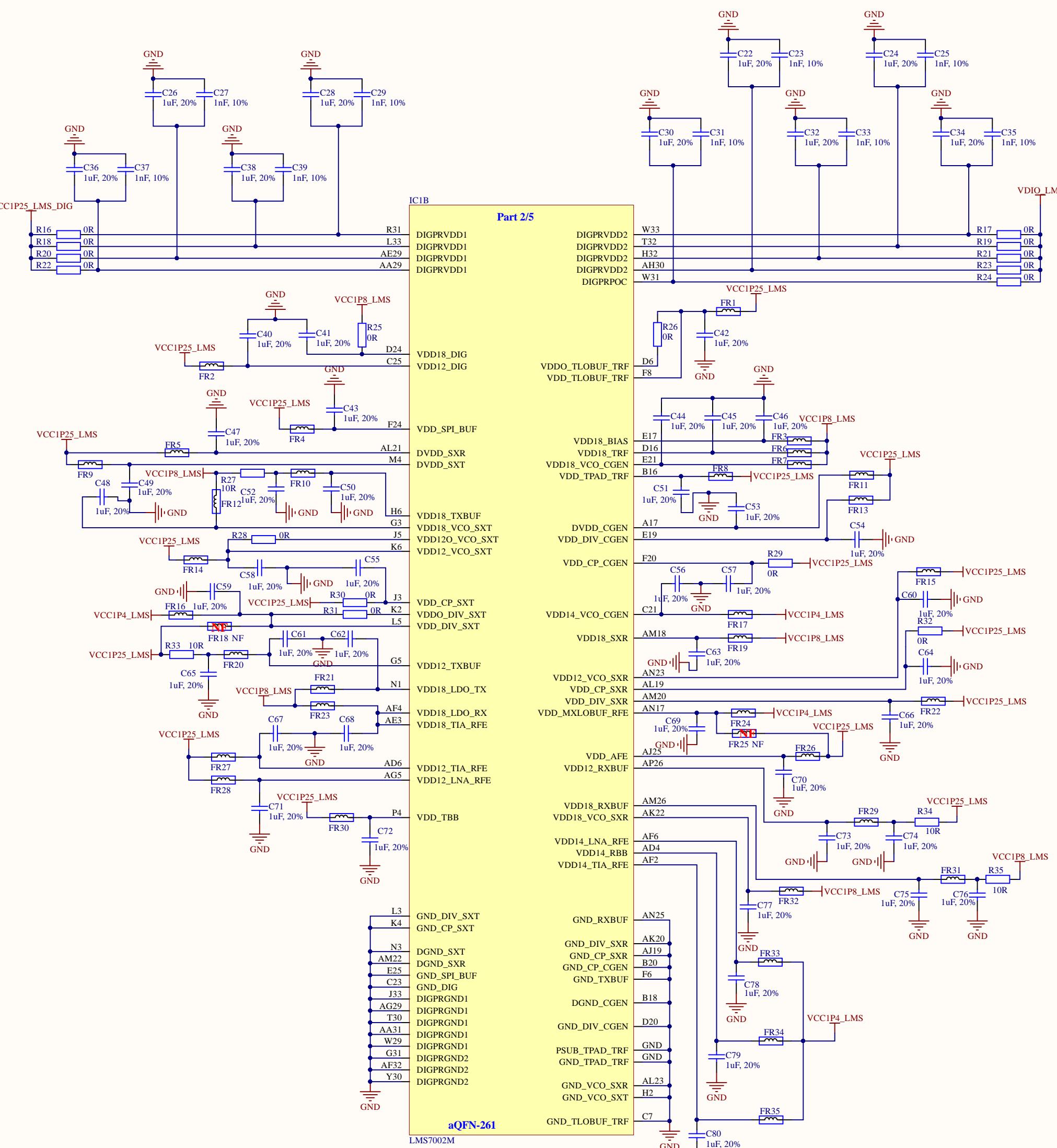
File: 05_LMS7002M_RF.SchDoc

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Surrey
United Kingdom



NF elements on sheet: FR18, FR25
Number of NF elements on sheet: 2

LMS7002M power supply circuit



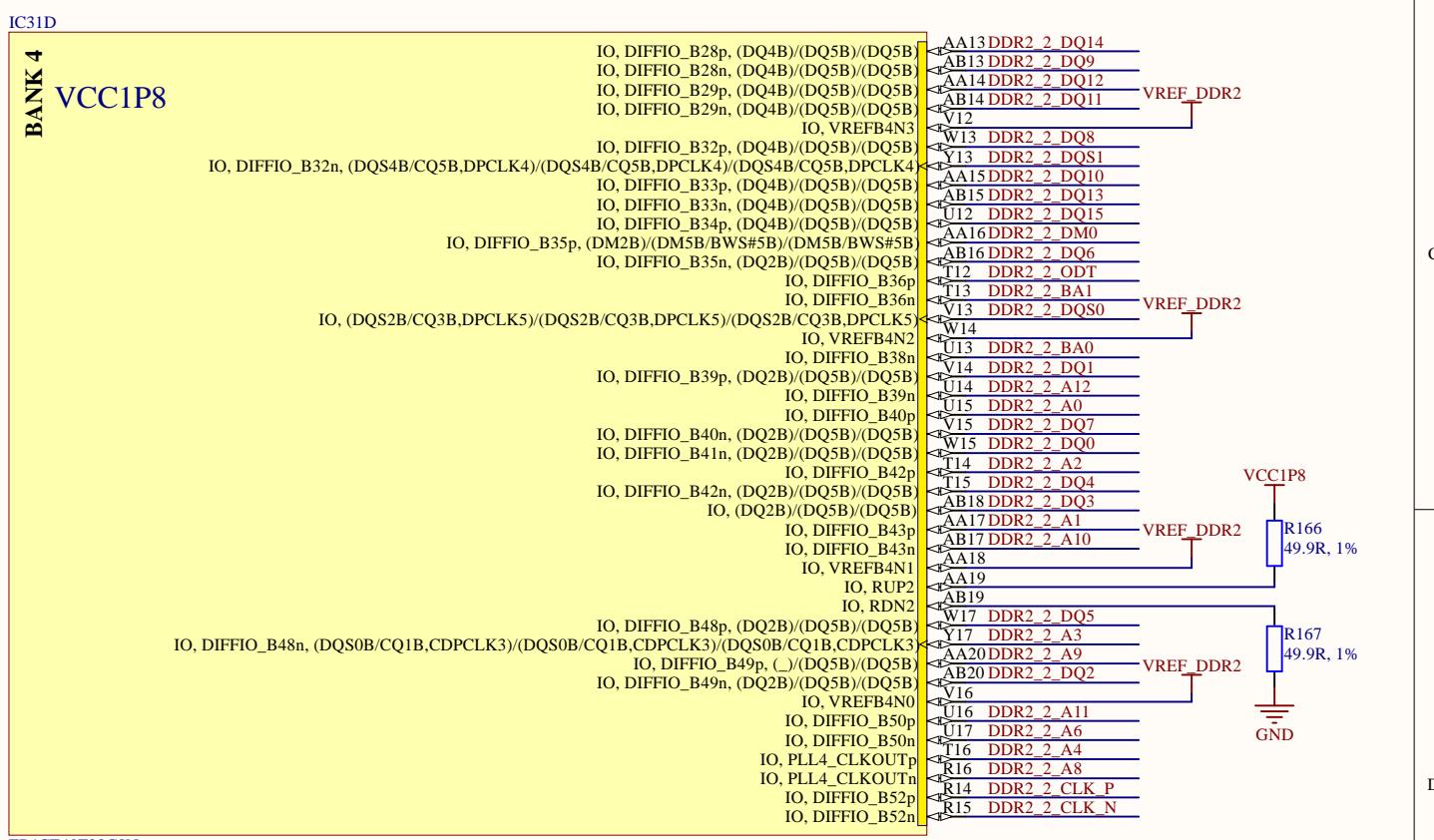
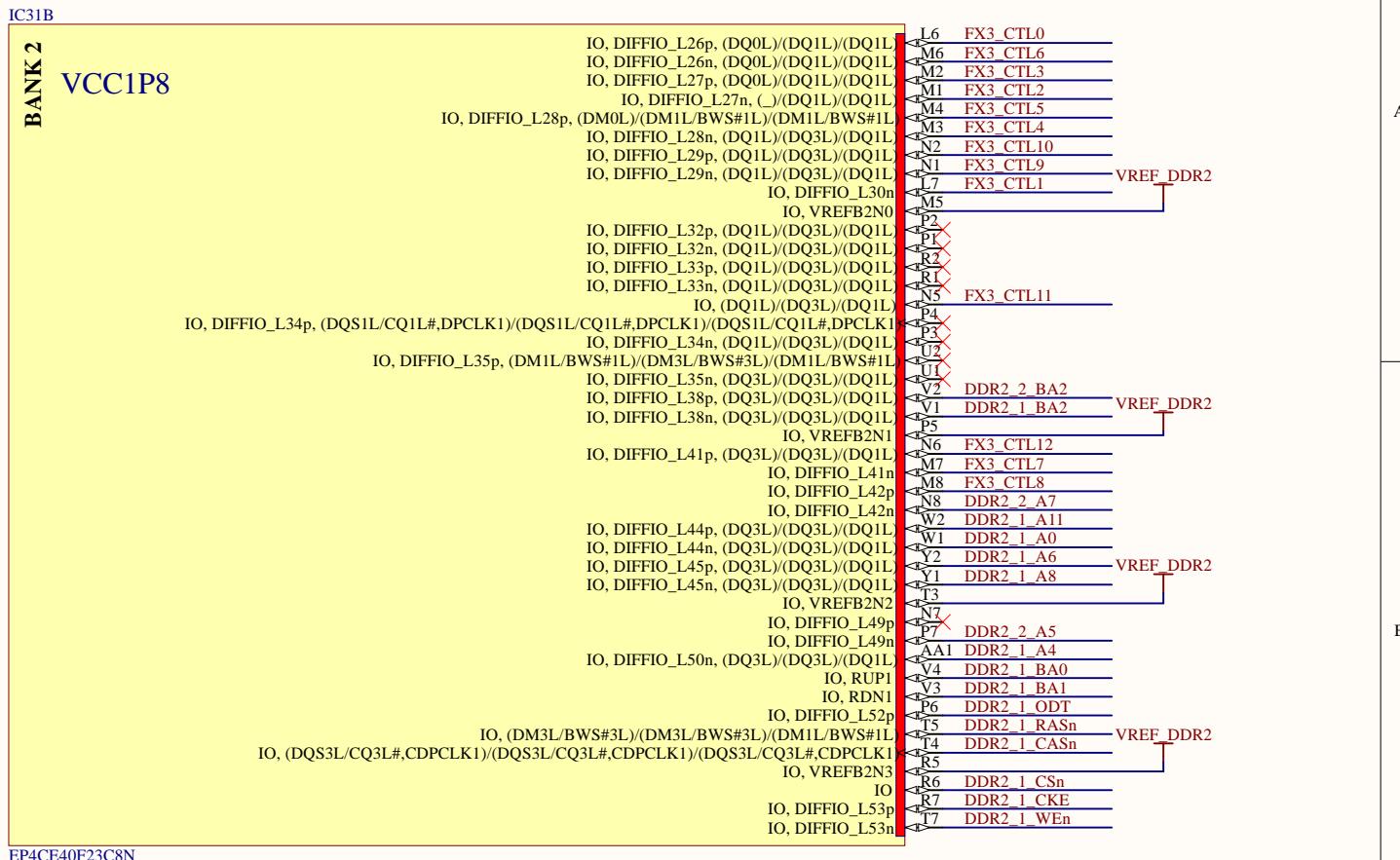
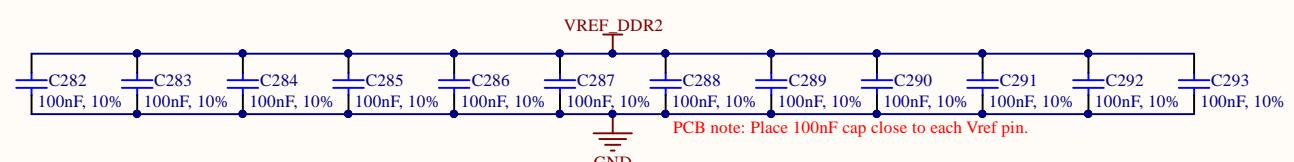
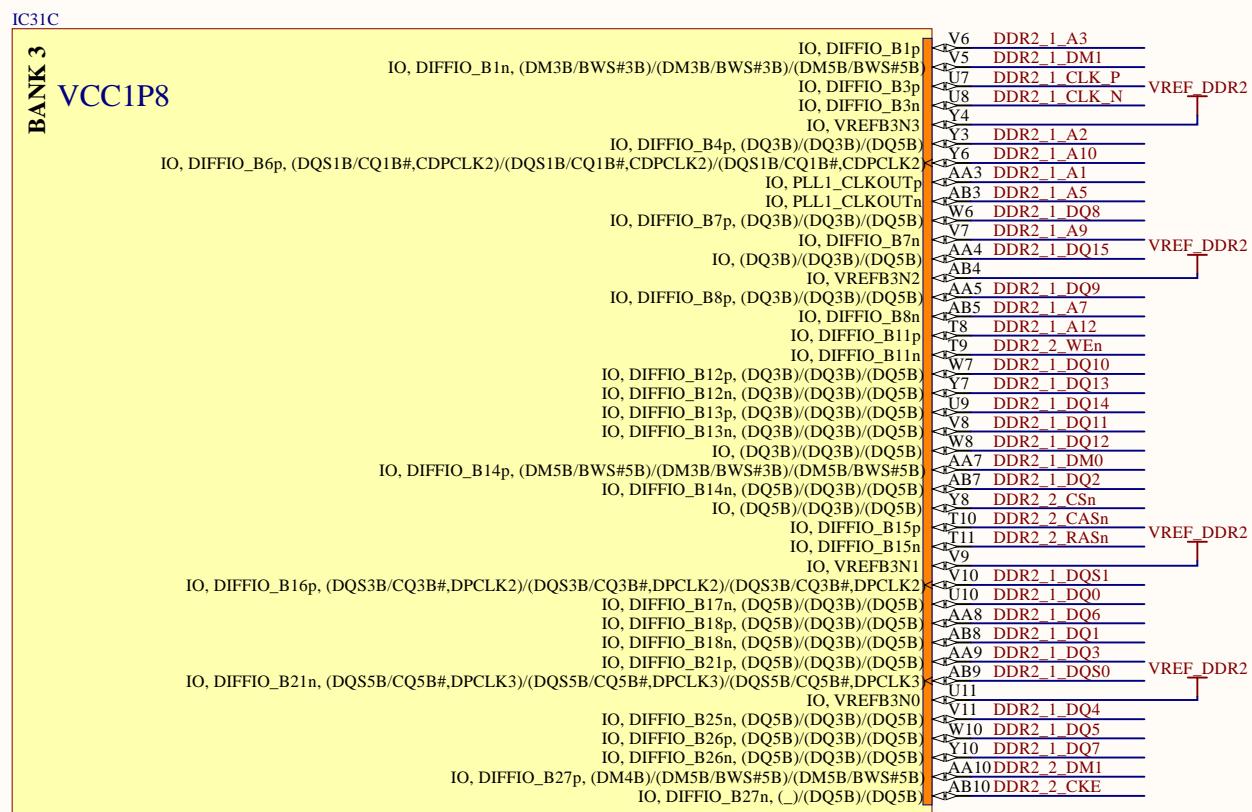
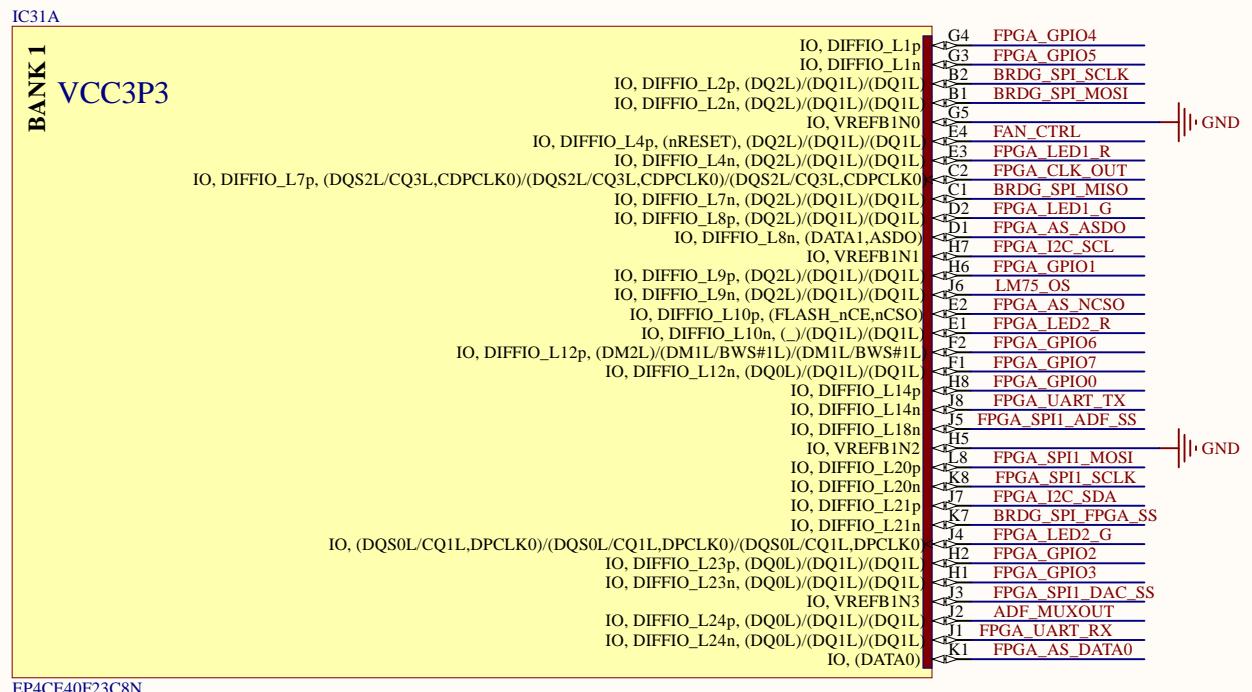
GND

Project name: **LimeSDR_InvS.PrfJrcd**

Title: LMS7002M power supply		<i>Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom</i>	 Lime microsystems
Size: A3	Revision: v1.2		
Date: 2016-04-21	Time: 11:08:15	Sheet 6 of 14	
File: 06_LMS7002M_Power SchDoc			

NF elements on sheet: -
Number of NF elements on sheet: 0

FPGA banks 1, 2, 3, 4



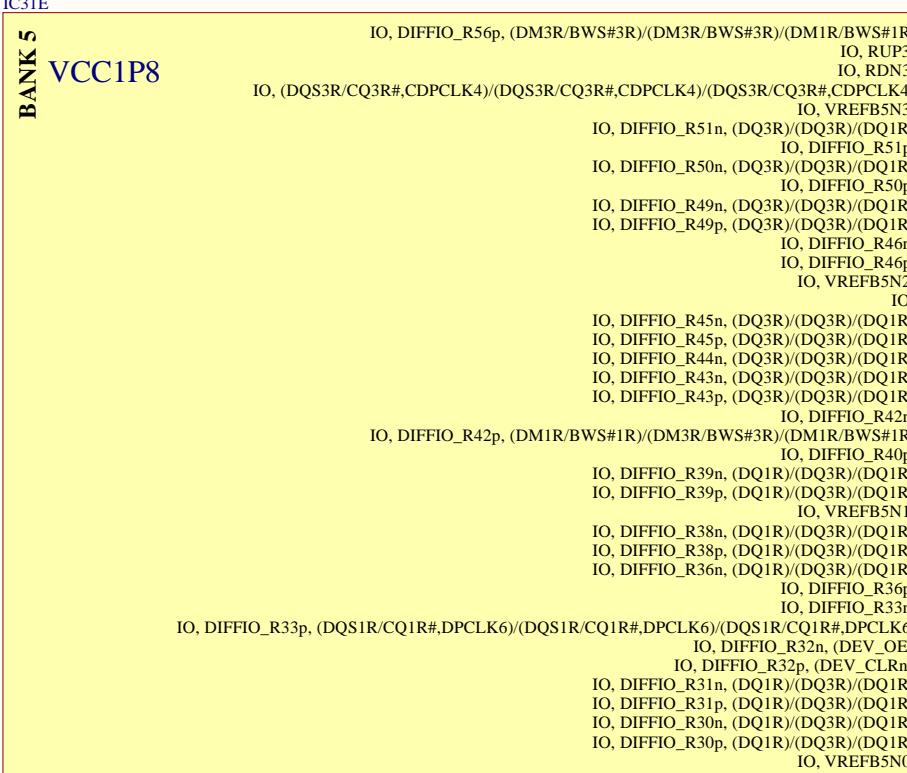
Project name: LimeSDR_Iv2s.PrjPcb			
Title: FPGA banks 1, 2, 3, 4		<i>Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom</i>	
Size: A3	Revision: v1.2		
Date: 2016-04-21 Time: 11:08:18		Sheet 7	of 14
File: 07_FPGA_banks_1_2_3_4.SchDoc			

NF elements on sheet: -
Number of NF elements on sheet: 0

FPGA banks 5, 6, 7, 8

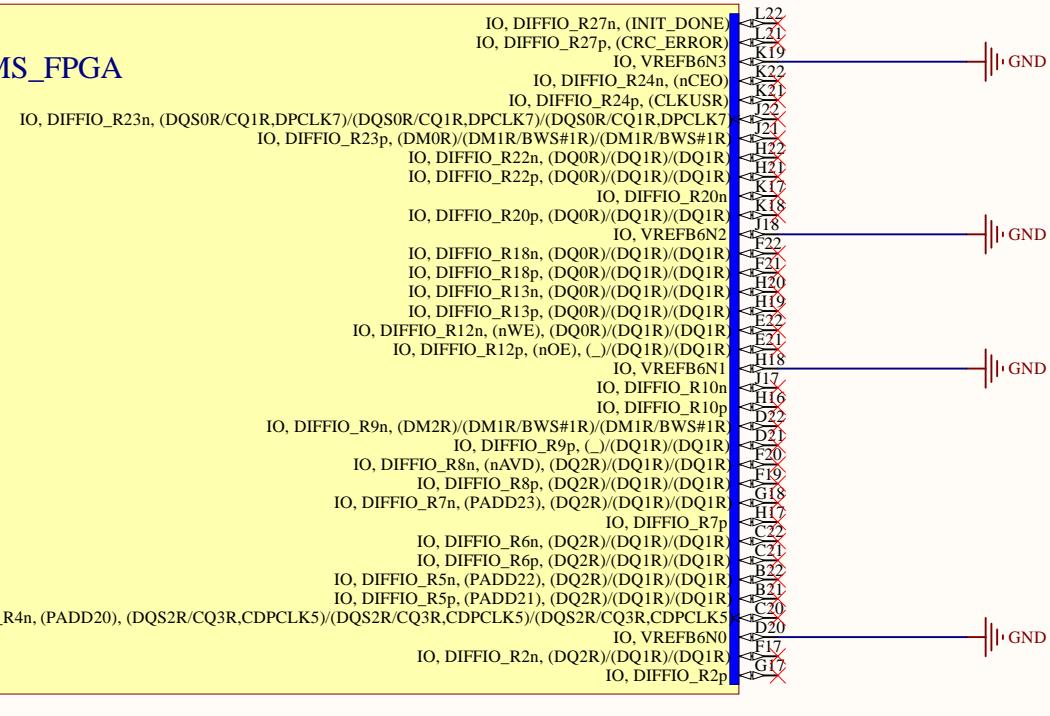
IC31E

VCC1P8



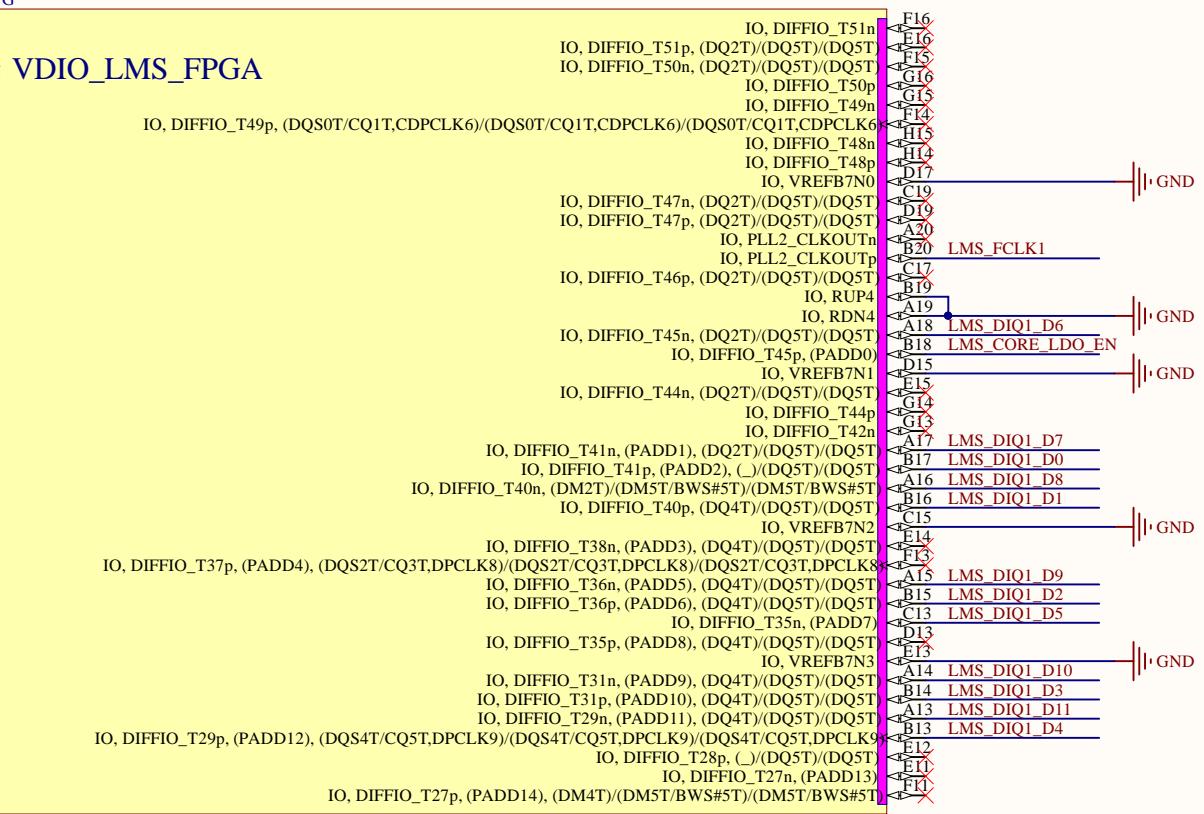
IC31F

VDIO_LMS_FPGA



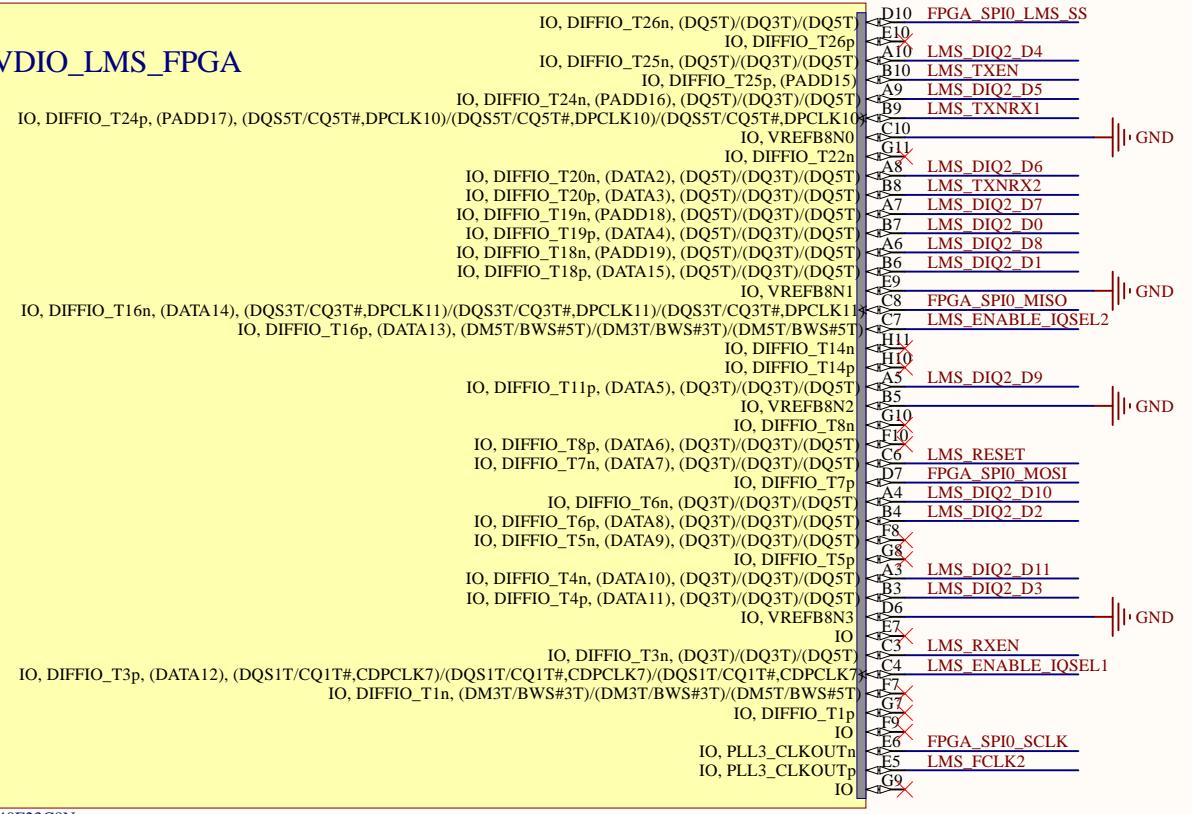
IC31G

VDIO_LMS_FPGA



IC31H

VDIO_LMS_FPGA



Project name: LimeSDR_Iv2s.PrbPcb

Title: **FPGA banks 5, 6, 7, 8**

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United Kingdom



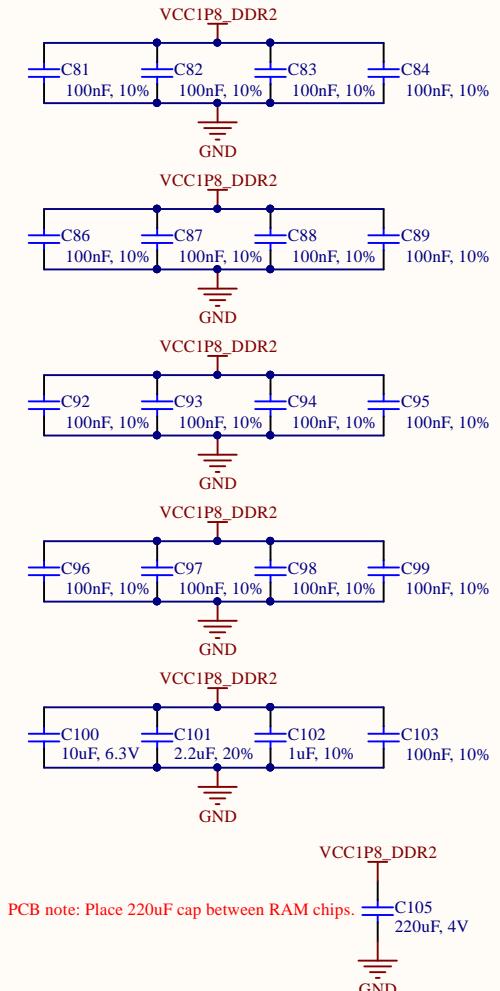
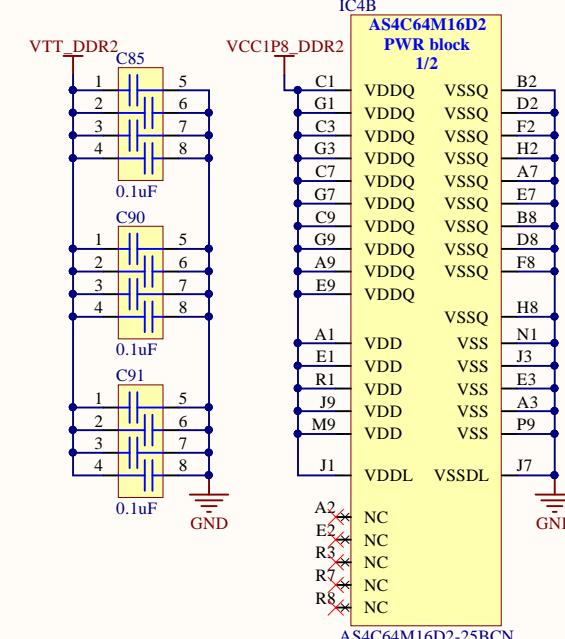
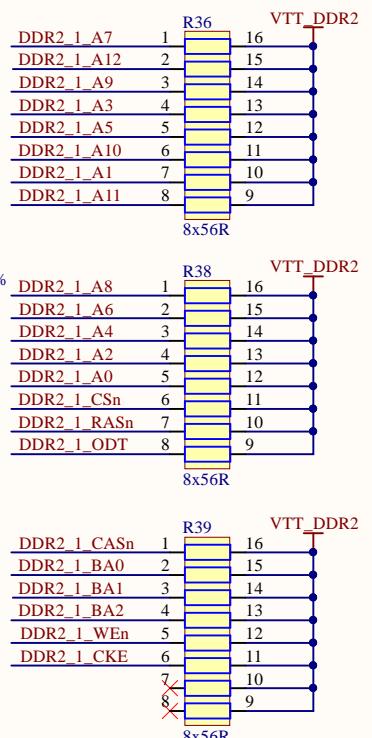
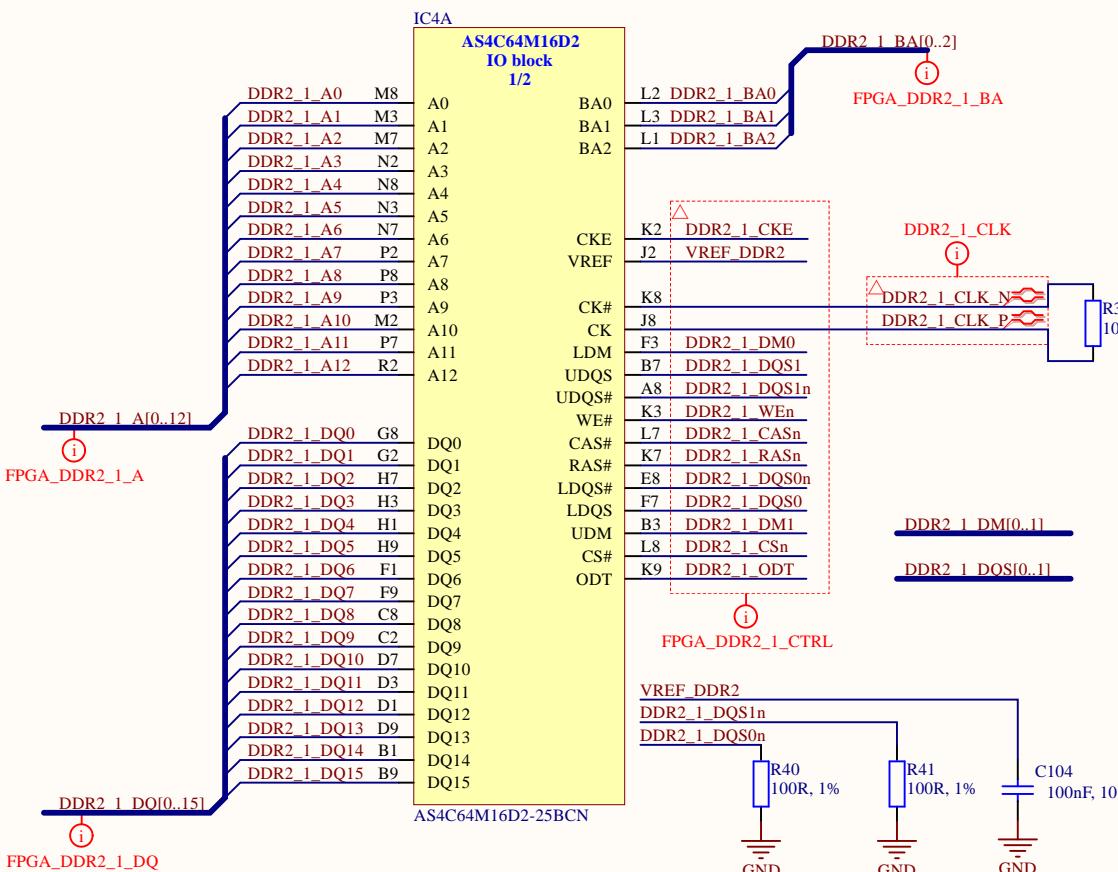
Size: A3 Revision: v1.2

Date: 2016-04-21 Time: 11:08:21 Sheet 8 of 14

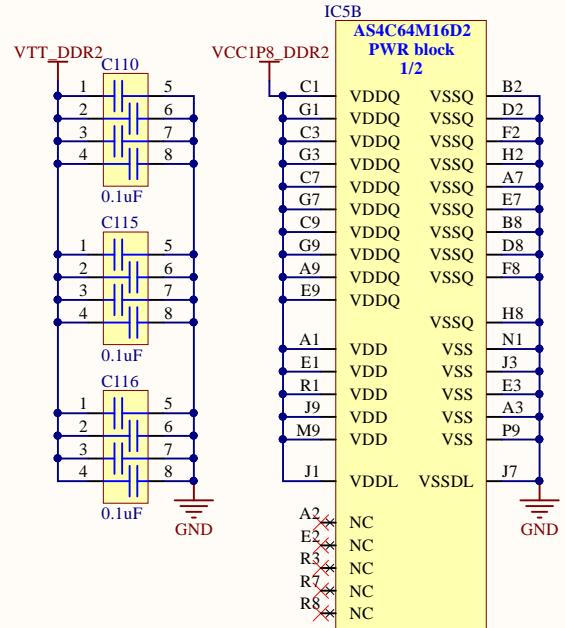
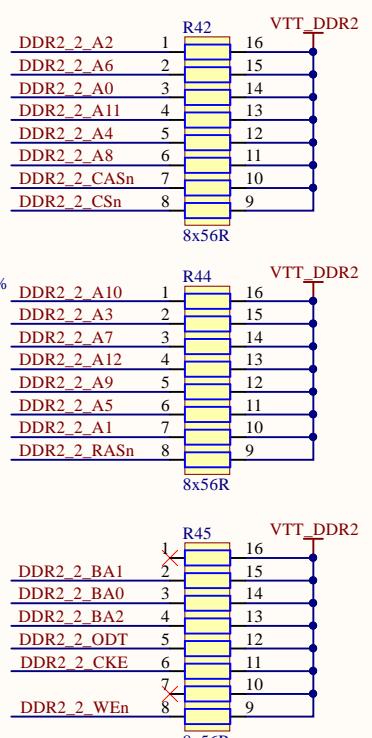
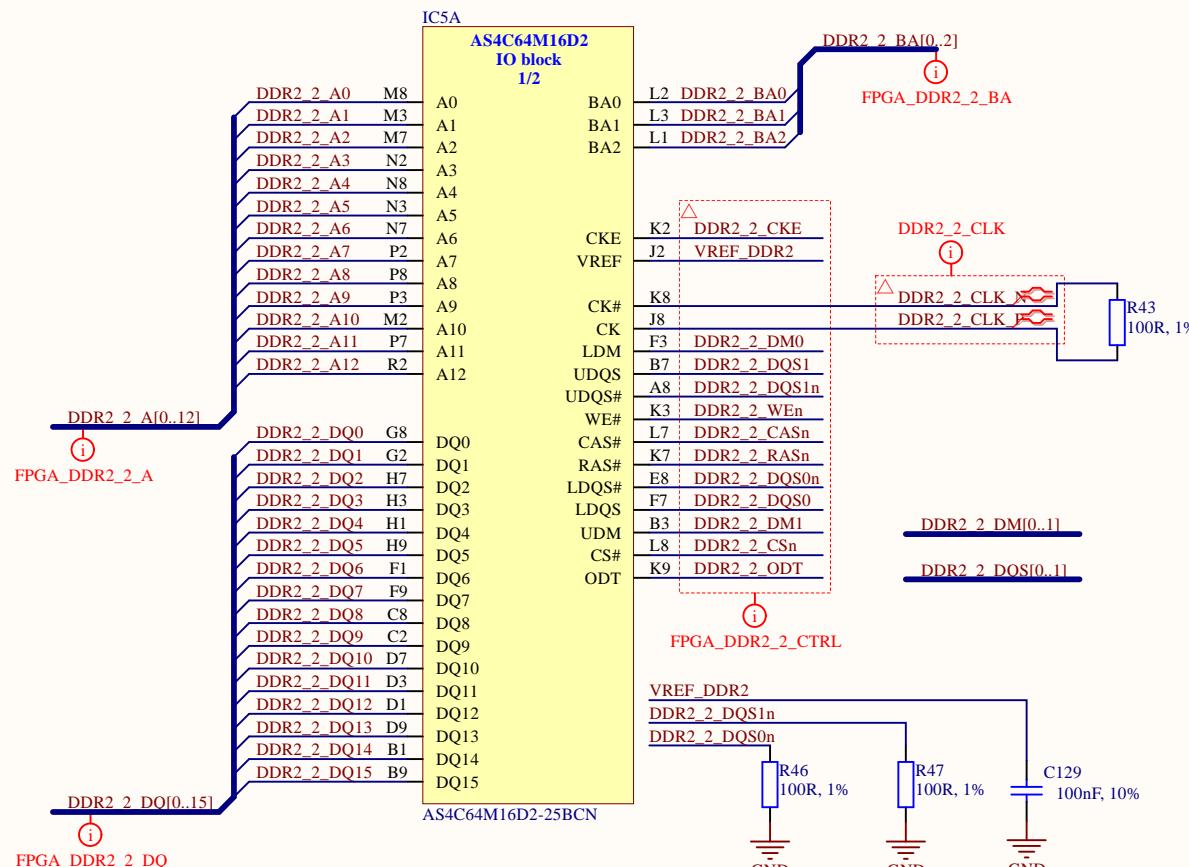
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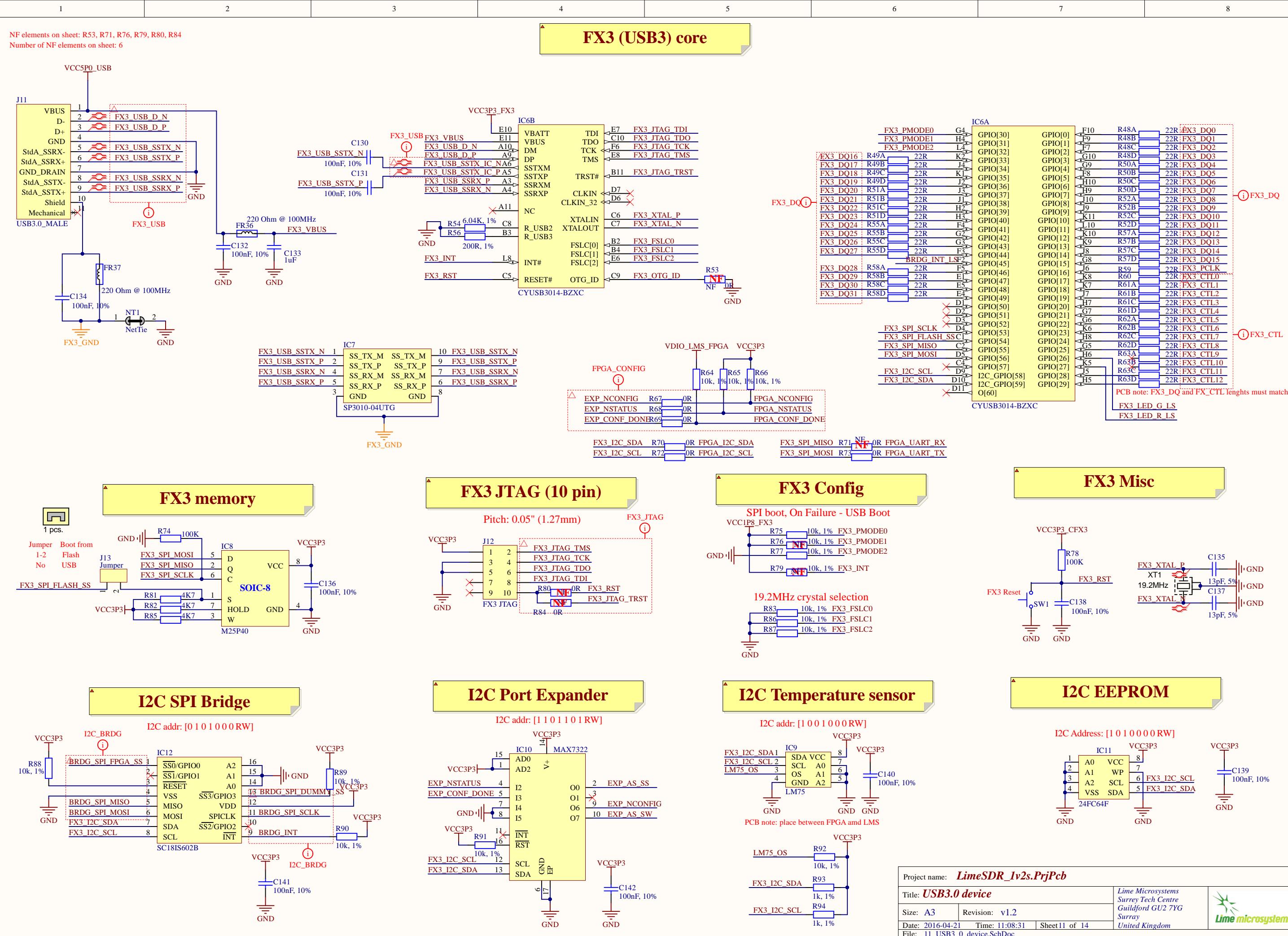
NF elements on sheet: -
Number of NF elements on sheet: 0

DDR2_1 (BOT L)



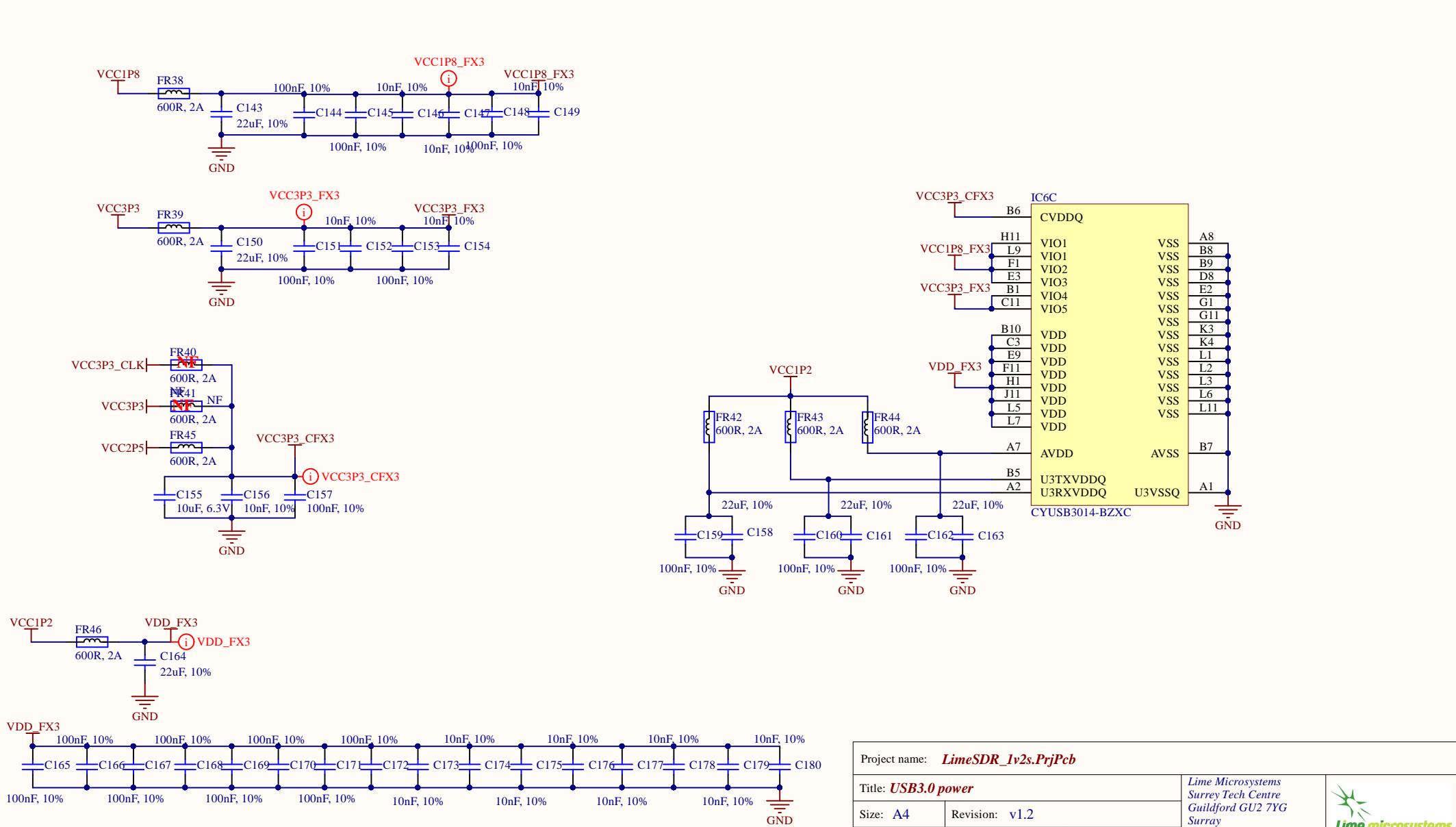
DDR2_2 (BOT R)





NF elements on sheet: FR40, FR41
Number of NF elements on sheet: 2

USB3 power block



Project name: *LimeSDR Lv2s BriBab*

Table 1

Size: A4 Revision: v1

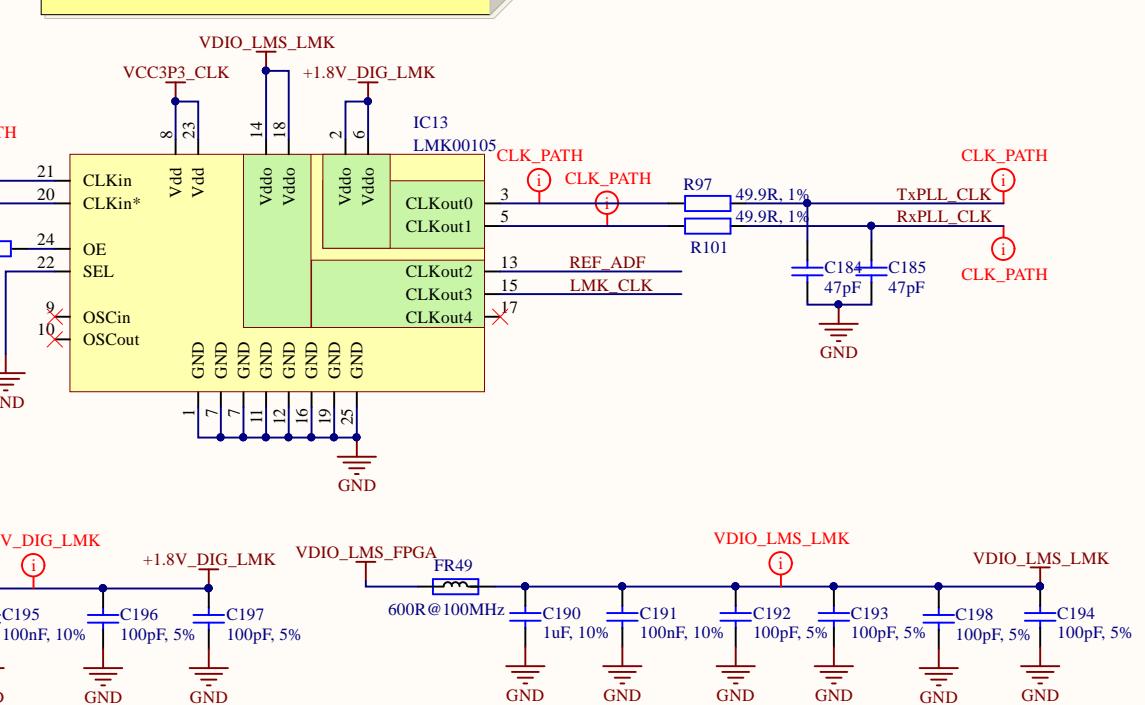
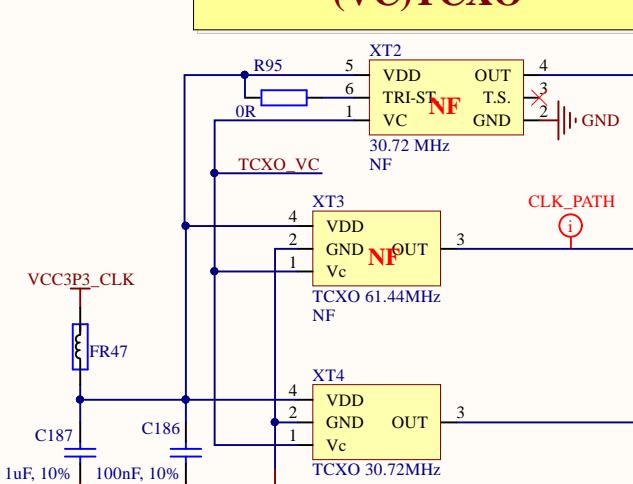
Size: A4 Revision: V1.2 Date: 2015-04-21 Title: 11-00-22 S1 - 12 - f - 14

Date: 2016-04-21 Time: 11:00

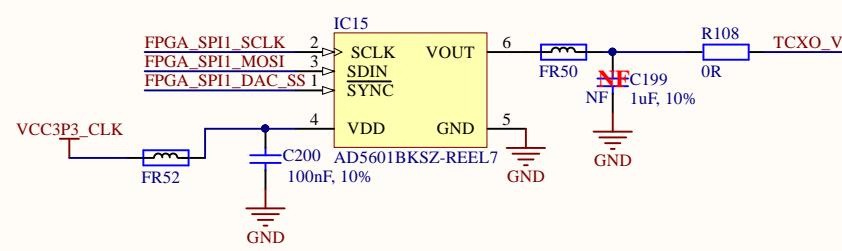
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Guildford GU2 7YG
Surrey
United Kingdom*



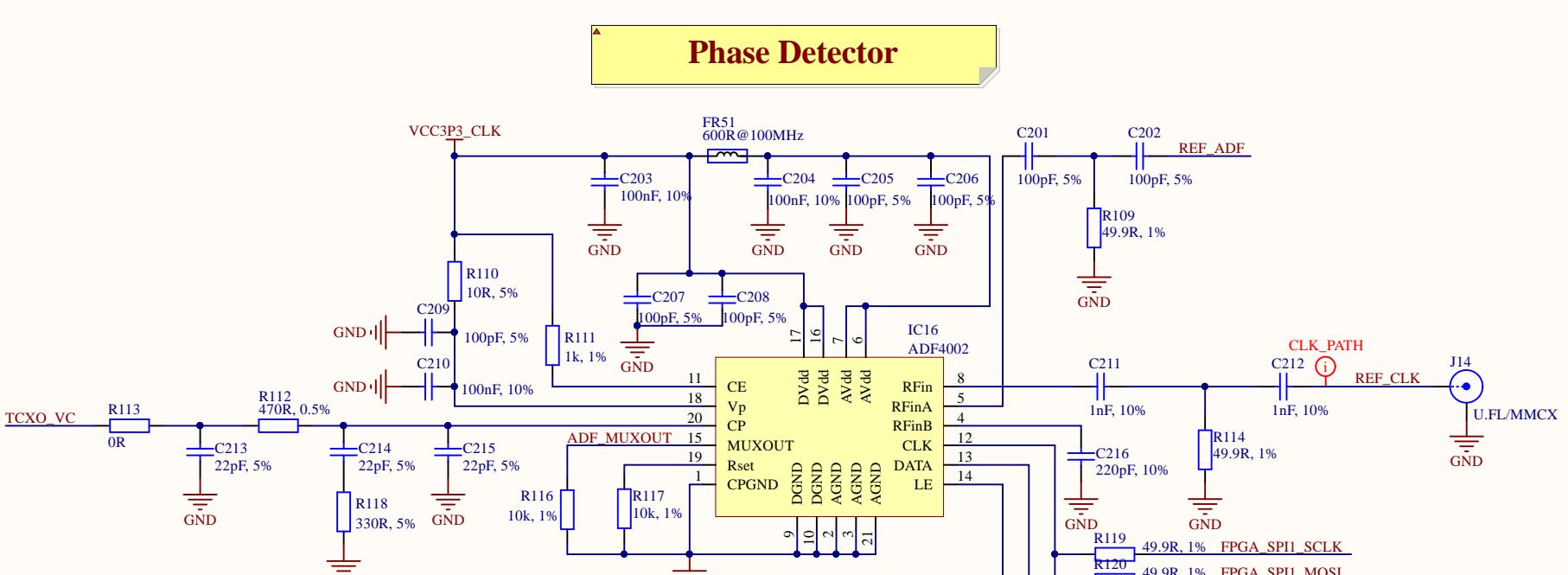
Clock circuits



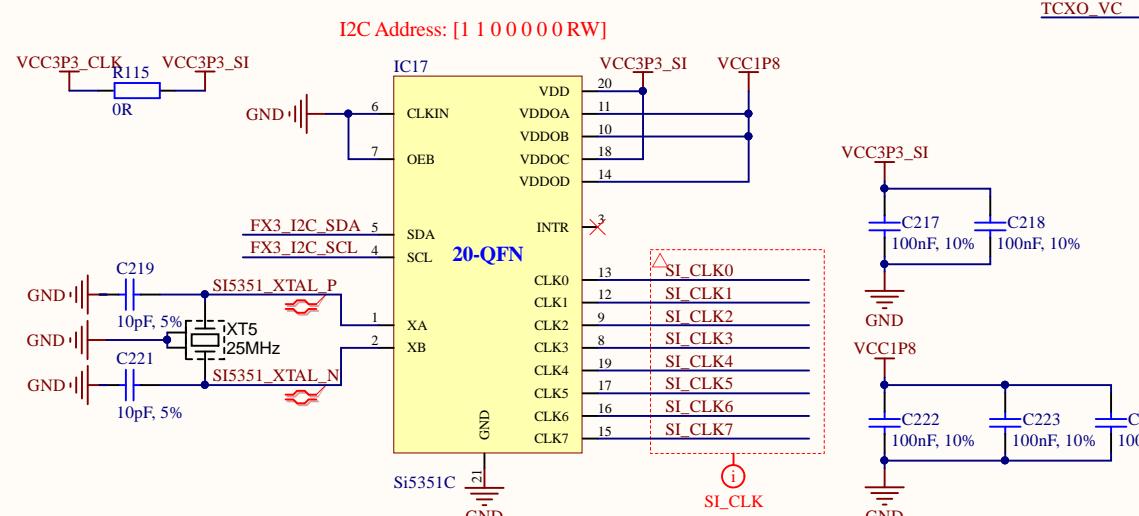
DAC



Phase Detector



Clock generator



Project name: **LimeSDR_1v2s.PriPcl**

Title: **Clocks** Lime Microsystems
Source: Tech Group

Lime Microsystems
Sensor Tech Group



