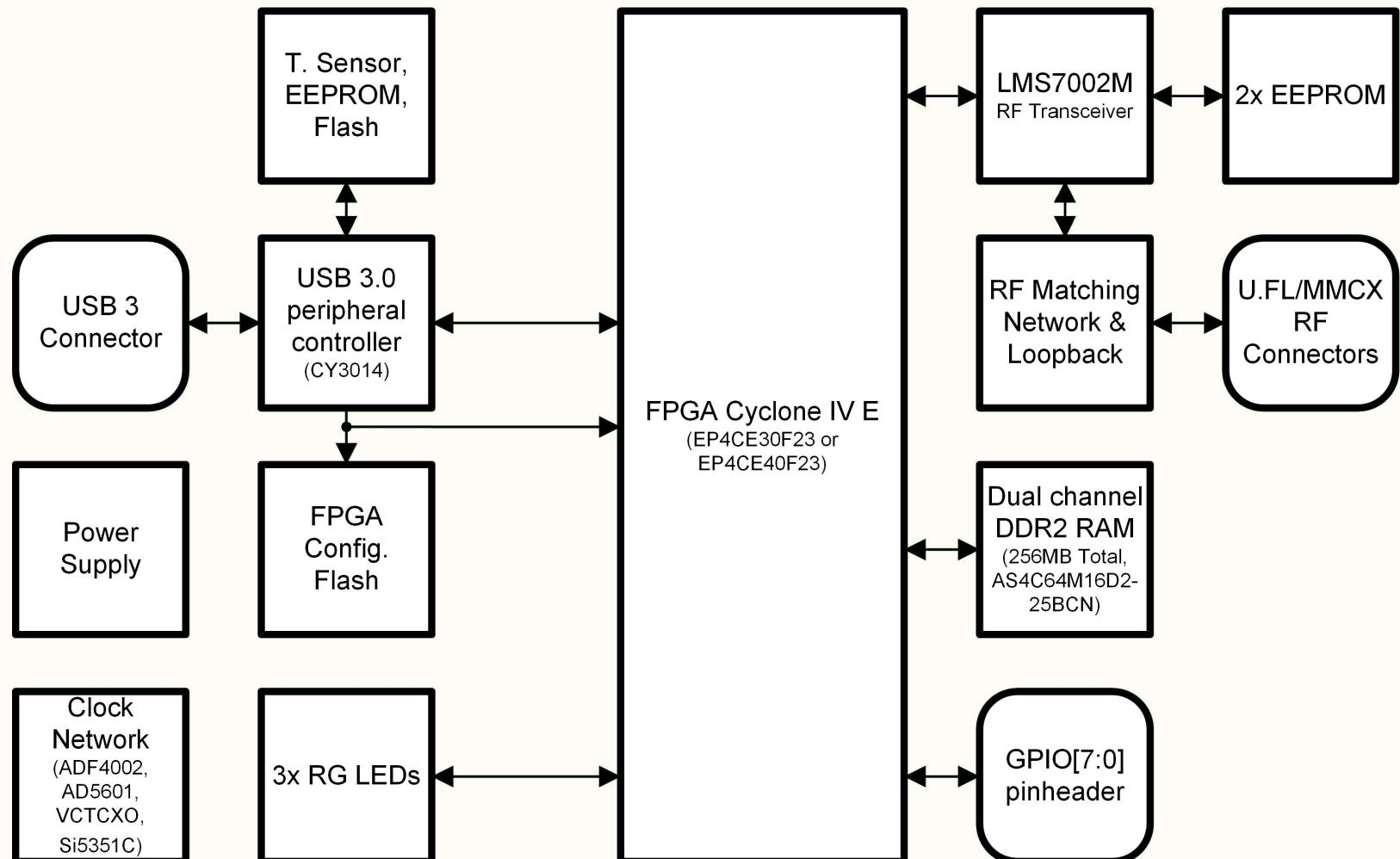


## Block diagram



Project name: [LimeSDR-USB\\_1v4.PrjPcb](#)

Title: [Block diagram](#)

Size: A4 Revision: v1.4

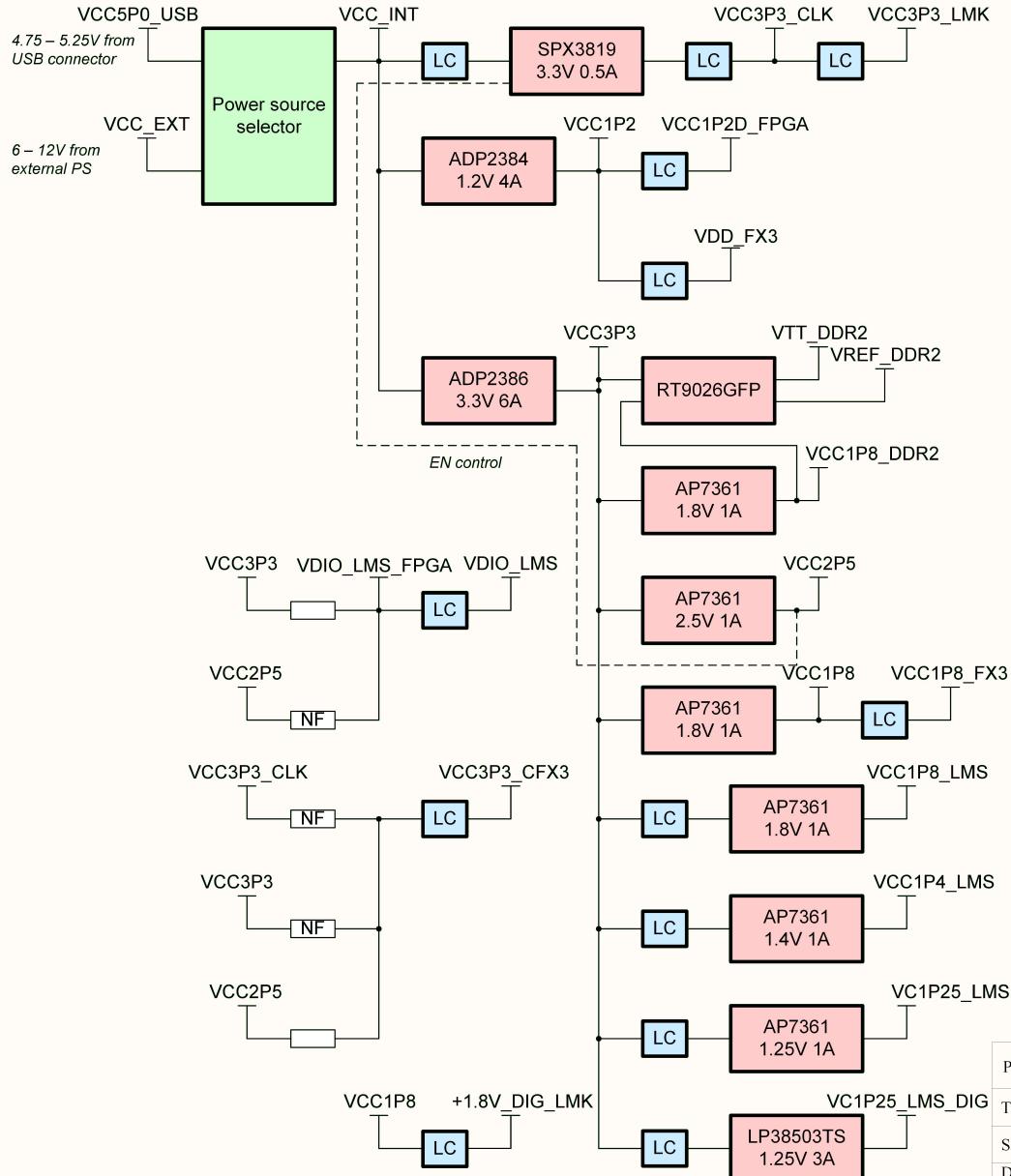
Date: 2017-02-01 Time: 14:57:34 Sheet 1 of 15

File: 01\_BlockDiagram.SchDoc

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Surrey  
United Kingdom



## Power diagram



Project name: **LimeSDR-USB\_Iv4.PrbPcb**

Title: **Power diagram**

Size: **A4**

Revision: **v1.4**

Date: **2017-02-01**

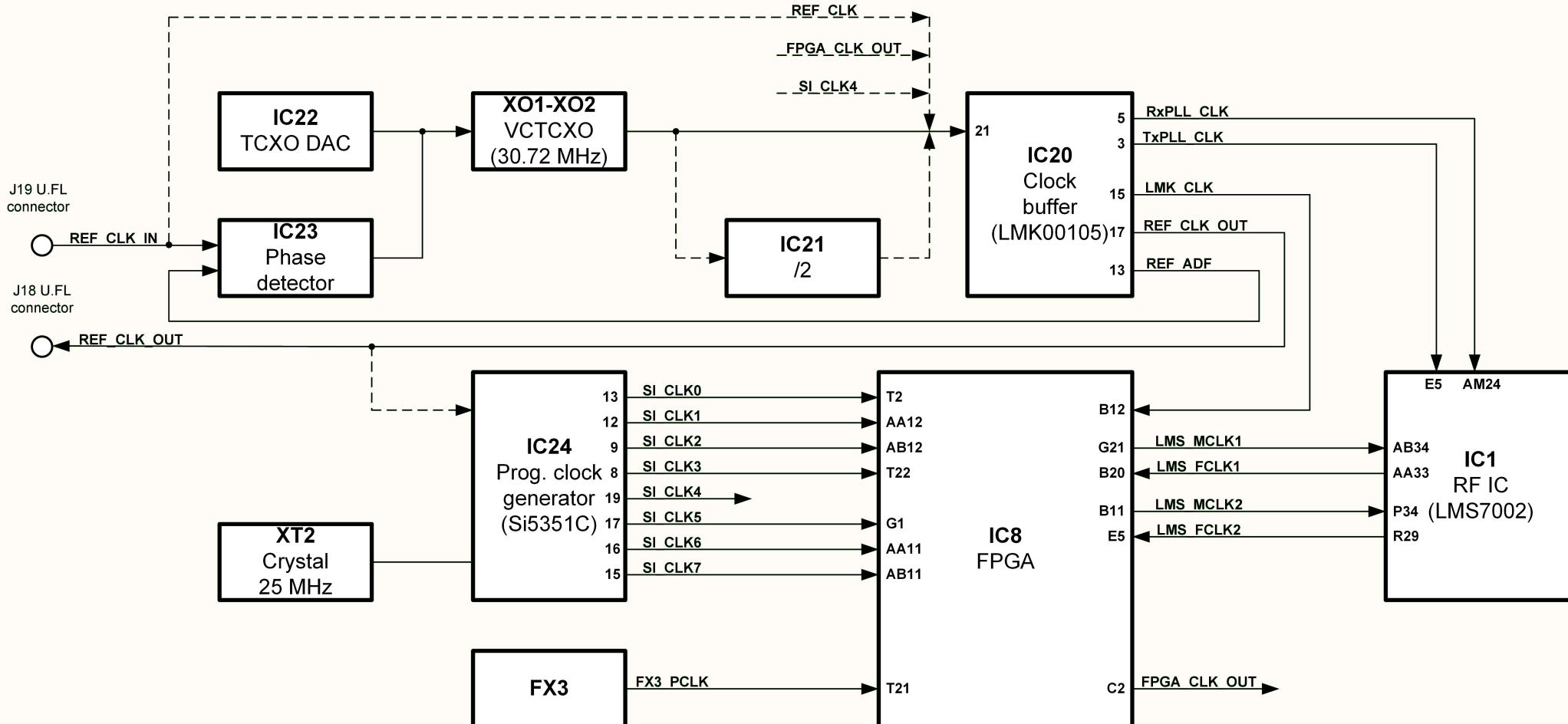
Time: **14:57:38**

Sheet **2** of **15**

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United Kingdom



## Clock diagram



Project name: *LimeSDR-USB\_Iv4.PpjPcb*

Title: *Clock diagram*

Size: A4 Revision: v1.4

Date: 2017-02-01 Time: 14:57:47 Sheet 3 of 15

File: 03\_ClockDiagram.SchDoc

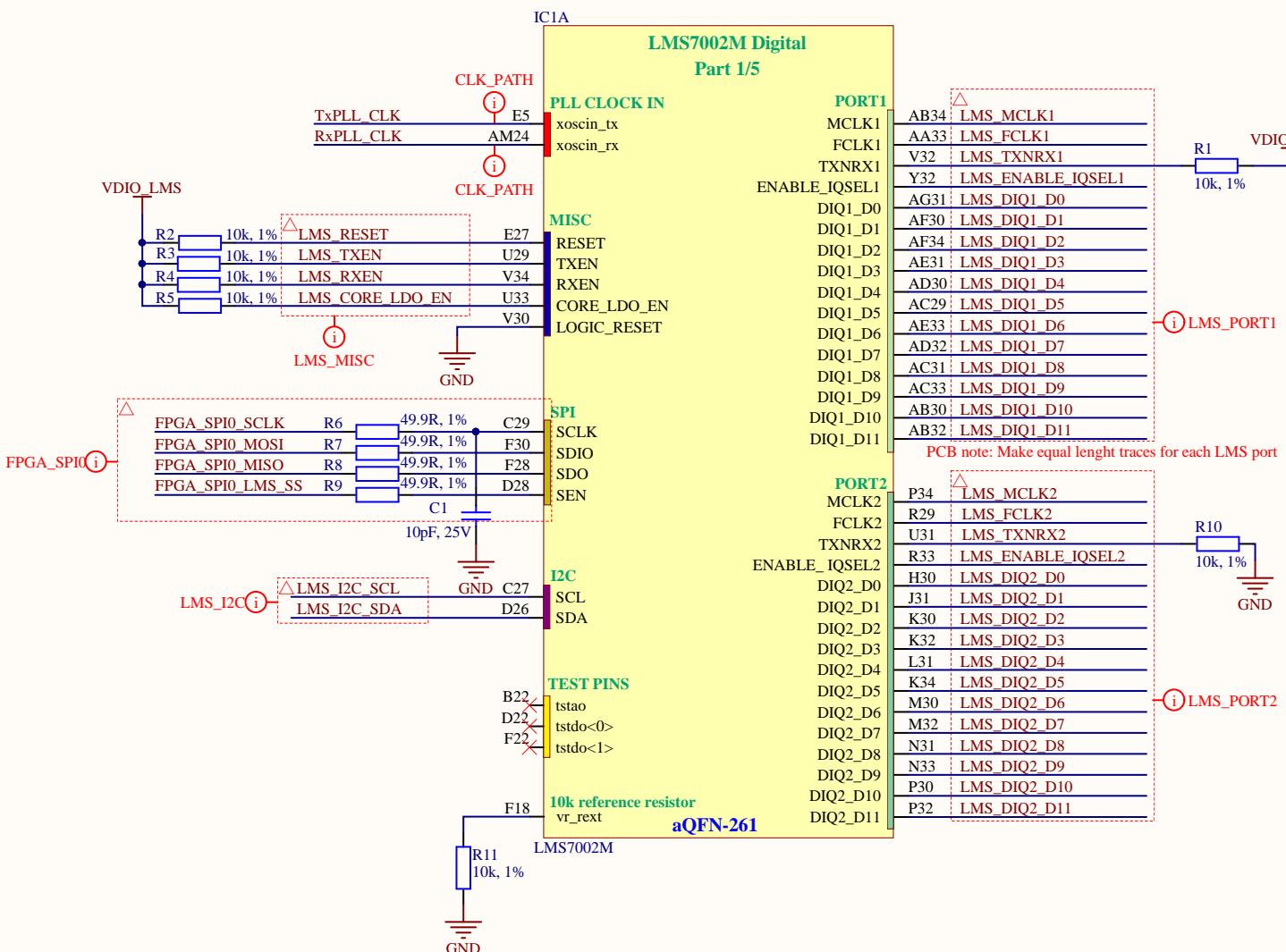
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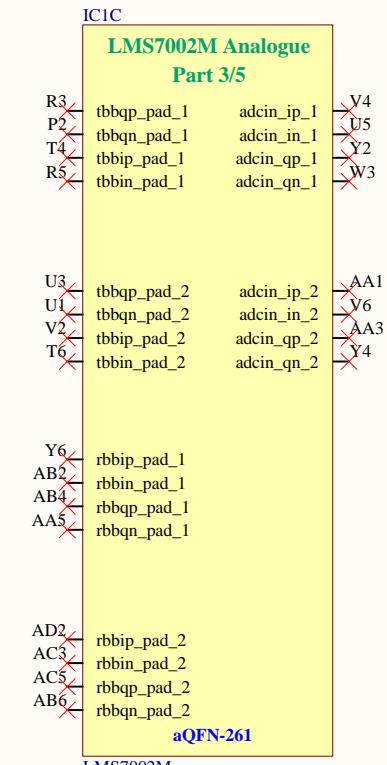
NF elements on sheet: -  
Number of NF elements on sheet: 0

## LMS7002M misc

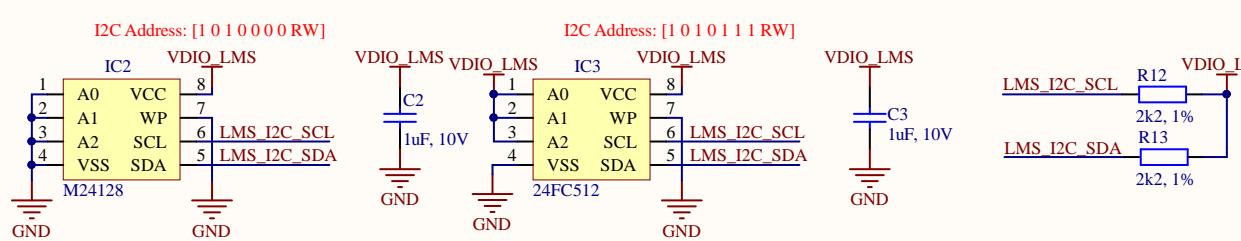
### Digital interfaces



### Baseband external IO



### LMS EEPROMs



Project name: LimeSDR-USB\_1v4.PrfPcb

Title: LMS7002M misc

Size: A3 Revision: v1.4

Date: 2017-02-01 Time: 14:57:54 Sheet 4 of 15

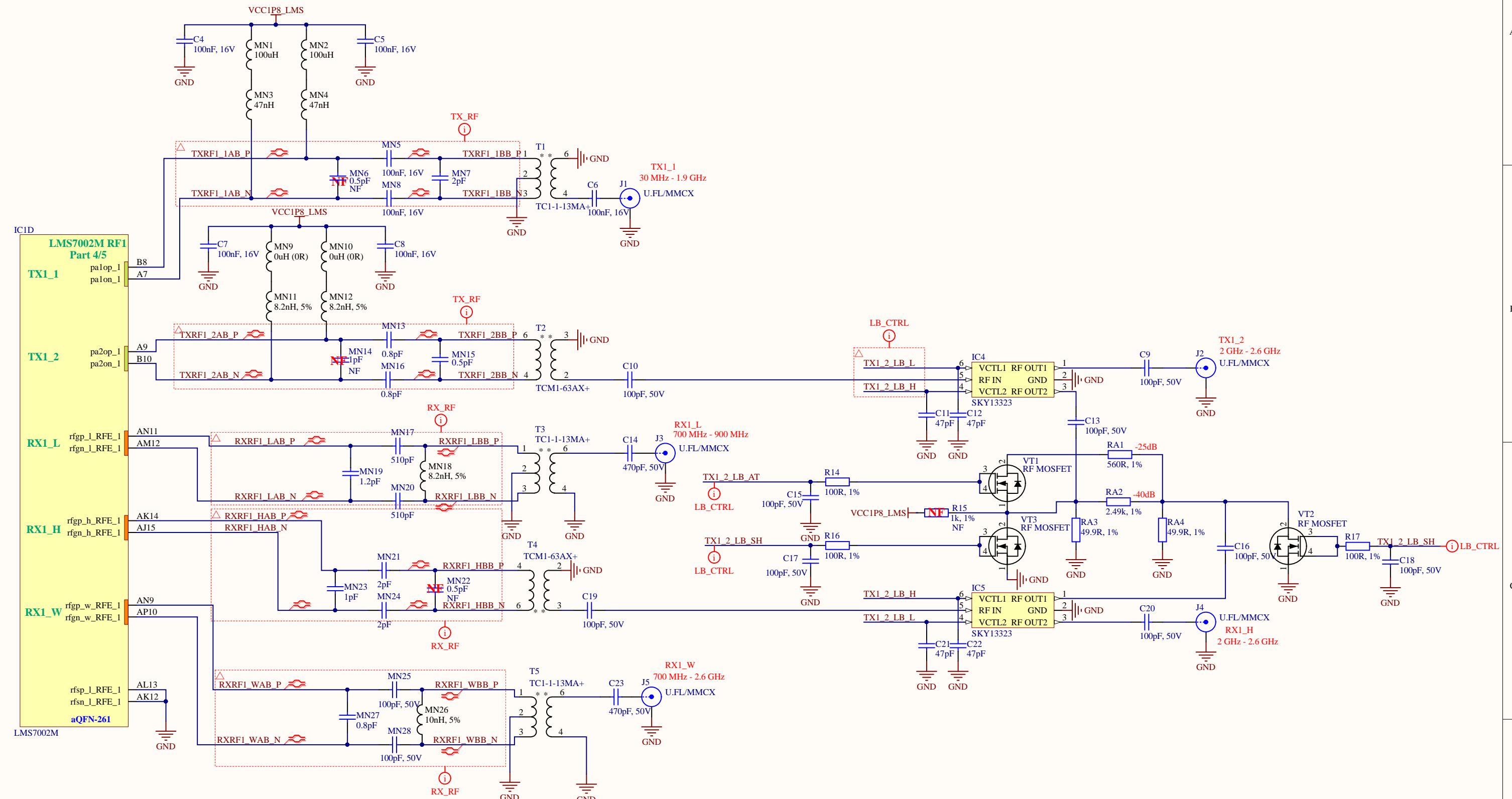
File: 04\_LMS7002M\_Misc.SchDoc

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NF elements on sheet: MN6, MN14, MN22, R15  
Number of NF elements on sheet: 4

## LMS7002M RF1 circuits



Project name: LimeSDR-USB\_1v4.PnjPcb

Title: LMS7002M RF

Size: A3 Revision: v1.4

Date: 2017-02-01 Time: 14:57:57 Sheet 5 of 15

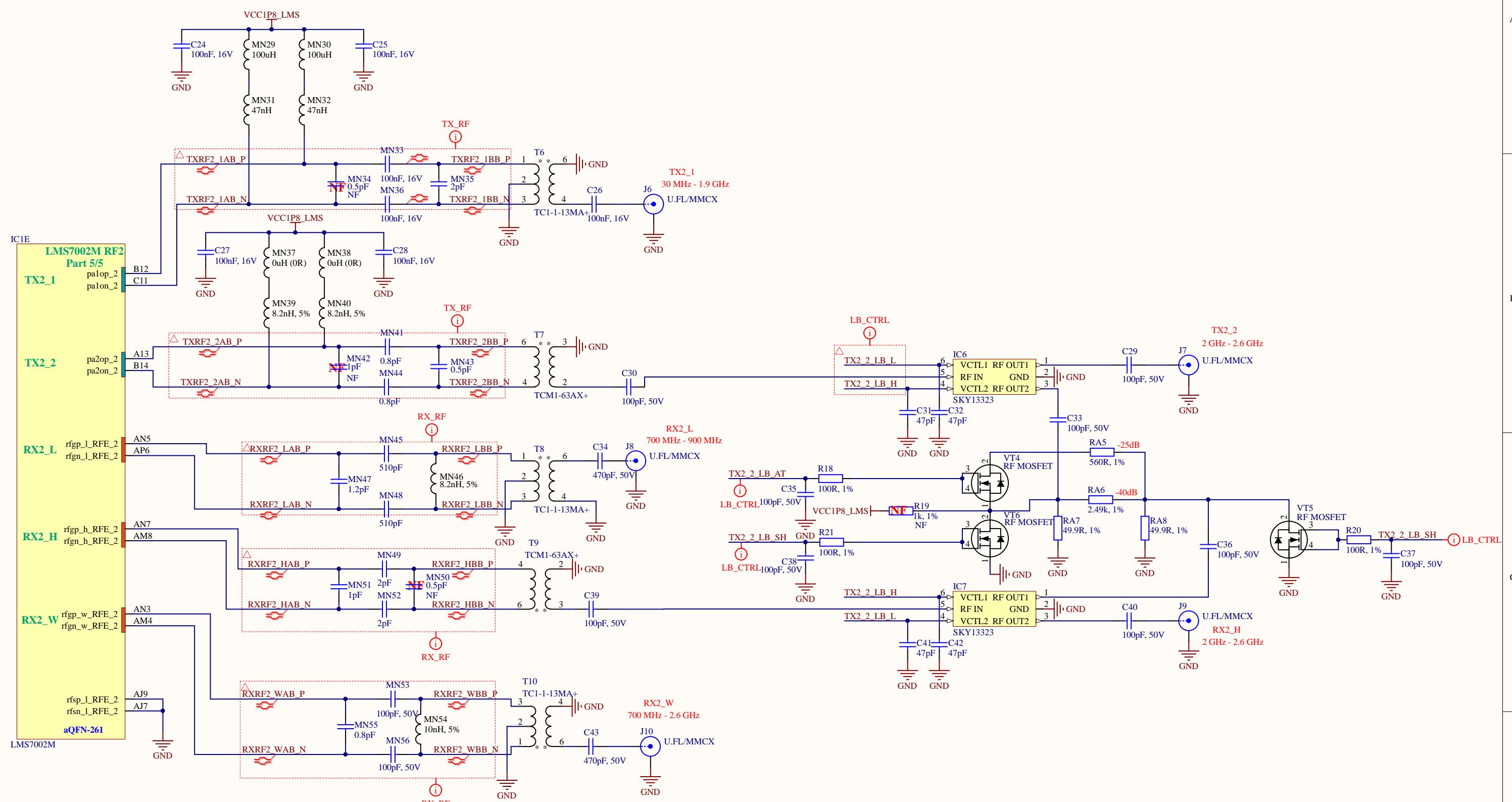
File: 05\_LMS7002M\_RF1.SchDoc

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NF elements on sheet: MN34, MN42, MN50, R19  
 Number of NF elements on sheet: 4

## LMS7002M RF2 circuits



Project name: LimeSDR-USB\_Iv4.PrjPcb

Title: LMS7002M RF

Size: A3 Revision: v1.4

Date: 2017-02-01 Time: 14:57:59 Sheet 6 of 15

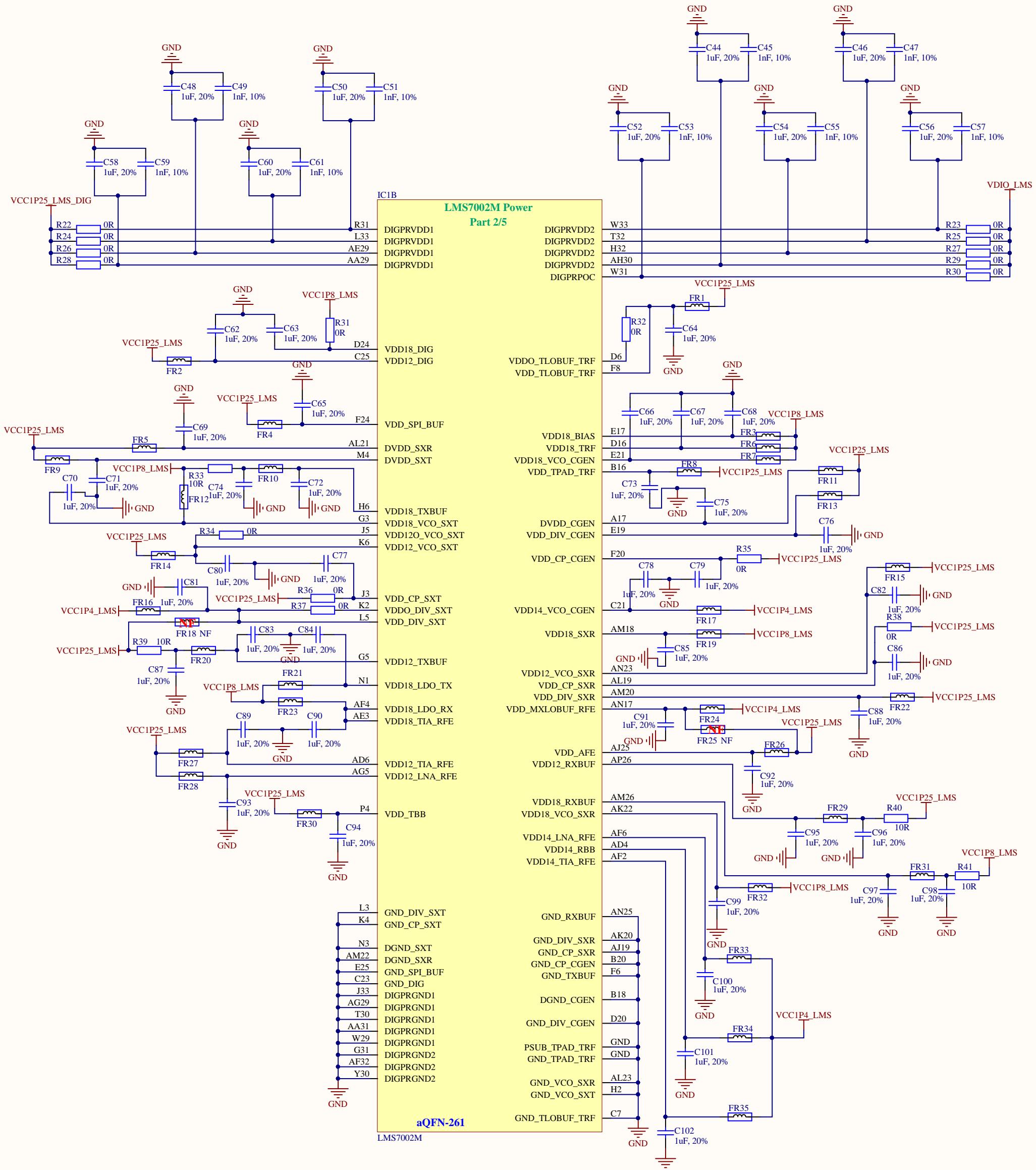
File: 06\_LMS7002M\_RF2.SchDoc

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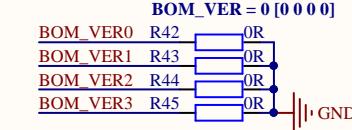
NF elements on sheet: FR18, FR25  
Number of NF elements on sheet: 2

## LMS7002M power supply circuit



## FPGA banks 1, 2, 3, 4

NF elements on sheet: -  
Number of NF elements on sheet: 0



A

**IC8A**  
**BANK 1**  
**VCC3P3**

IO, DIFFIO\_L1p, (DQ2L)/(DQ1L)/(DQ1L)  
IO, DIFFIO\_L1n  
IO, DIFFIO\_L2p, (DQ2L)/(DQ1L)/(DQ1L)  
IO, DIFFIO\_L2n, (DQ2L)/(DQ1L)/(DQ1L)  
IO, VREFB1N0  
IO, DIFFIO\_L4p, (nRESET), (DQ2L)/(DQ1L)/(DQ1L)  
IO, DIFFIO\_L4n, (DQ2L)/(DQ1L)/(DQ1L)  
IO, DIFFIO\_L7p, (DQS2L/CQ3L,CDPCLK0)/(DQS2L/CQ3L,CDPCLK0)  
IO, DIFFIO\_L7n, (DQ2L)/(DQ1L)/(DQ1L)  
IO, DIFFIO\_L8p, (DQ2L)/(DQ1L)/(DQ1L)  
IO, DIFFIO\_L8n, (DATA1,ASDO)  
IO, VREFB1N1  
IO, DIFFIO\_L9p, (DQ2L)/(DQ1L)/(DQ1L)  
IO, DIFFIO\_L9n, (DQ2L)/(DQ1L)/(DQ1L)  
IO, DIFFIO\_L10p, (FLASH\_nCE,nCSO)  
IO, DIFFIO\_L10n, (.),(DQ1L)/(DQ1L)  
IO, DIFFIO\_L12p, (DM2L)/(DM1L/BWS#1L)/(DM1L/BWS#1L)  
IO, DIFFIO\_L12n, (DQ0L)/(DQ1L)/(DQ1L)  
IO, DIFFIO\_L14p  
IO, DIFFIO\_L14n  
IO, DIFFIO\_L18n  
IO, VREFB1N2  
IO, DIFFIO\_L20p  
IO, DIFFIO\_L20n  
IO, DIFFIO\_L21p  
IO, DIFFIO\_L21n  
IO, FX3\_LED\_R  
IO, FPGA\_SPI1\_MOSI  
IO, FPGA\_SPI1\_SCLK  
IO, FPGA\_I2C\_SDA  
IO, BRDG\_SPI\_FPGA\_SS  
IO, FPGA\_LED2\_G  
IO, FPGA\_GPIO2  
IO, FPGA\_GPIO3  
IO, FPGA\_SPI1\_DAC\_SS  
IO, ADF\_MUXOUT  
IO, FPGA\_UART\_RX  
IO, FPGA\_AS\_DATA0  
IO, (DQS0L/CQ1L,DPCLK0)/(DQS0L/CQ1L,DPCLK0)  
IO, DIFFIO\_L23p, (DQ0L)/(DQ1L)/(DQ1L)  
IO, DIFFIO\_L23n, (DQ0L)/(DQ1L)/(DQ1L)  
IO, VREFB1N3  
IO, DIFFIO\_L24p, (DQ0L)/(DQ1L)/(DQ1L)  
IO, DIFFIO\_L24n, (DQ0L)/(DQ1L)/(DQ1L)  
IO, (DATA0)

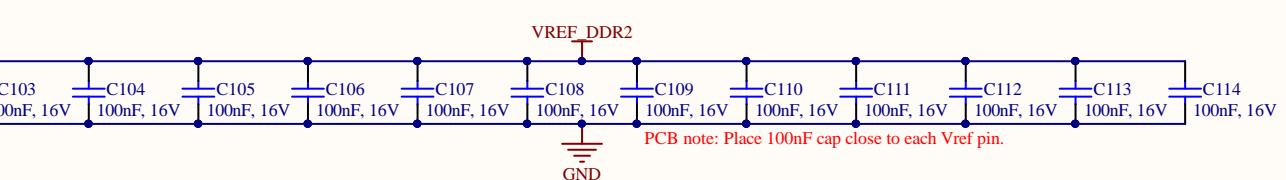
EP4CE40F23C8N

B

**IC8C**  
**BANK 3**  
**VCC1P8**

IO, DIFFIO\_B1p, (DM3B/BWS#3B)/(DM3B/BWS#3B)/(DM5B/BWS#5B)  
IO, DIFFIO\_B3p  
IO, VREFB3N3  
Y4  
Y6 DDR2\_1\_A3  
Y5 DDR2\_1\_DM1  
Y7 DDR2\_1\_CLK\_P  
Y8 DDR2\_1\_CLK\_N  
VREF\_DDR2  
Y3 DDR2\_1\_A2  
Y6 DDR2\_1\_A10  
AA3 DDR2\_1\_A1  
AB3 DDR2\_1\_A5  
W6 DDR2\_1\_DQ8  
Y7 DDR2\_1\_A9  
AA4 DDR2\_1\_DQ15  
VREF\_DDR2  
AB4  
AA5 DDR2\_1\_DQ9  
AB5 DDR2\_1\_A7  
T8 DDR2\_1\_A12  
T9 DDR2\_2\_WEn  
W7 DDR2\_1\_DQ10  
Y7 DDR2\_1\_DQ13  
J9 DDR2\_1\_DQ14  
V8 DDR2\_1\_DQ11  
V8 DDR2\_1\_DQ12  
AA7 DDR2\_1\_DM0  
AB7 DDR2\_1\_DQ2  
Y8 DDR2\_2\_CSn  
T10 DDR2\_2\_CASn  
T11 DDR2\_2\_RASn  
VREF\_DDR2  
V10 DDR2\_1\_DQS1  
U10 DDR2\_1\_DQ0  
AA8 DDR2\_1\_DQ6  
AB8 DDR2\_1\_DQ1  
AA9 DDR2\_1\_DQ3  
AB9 DDR2\_1\_DQS0  
V11  
V11 DDR2\_1\_DQ4  
W10 DDR2\_1\_DQ5  
Y10 DDR2\_1\_DQ7  
AA10 DDR2\_2\_DM1  
AB10 DDR2\_2\_CKE  
IO, VREFB3N1  
IO, DIFFIO\_B17n, (DQS5B)/(DQ3B)/(DQ5B)  
IO, DIFFIO\_B18p, (DQ5B)/(DQ3B)/(DQ5B)  
IO, DIFFIO\_B18n, (DQ5B)/(DQ3B)/(DQ5B)  
IO, DIFFIO\_B21p, (DQ5B)/(DQ3B)/(DQ5B)  
IO, DIFFIO\_B21n, (DQS5B/CQ5B#,DPCLK3)/(DQS5B/CQ5B#,DPCLK3)/(DQS5B/CQ5B#,DPCLK3)  
IO, VREFB3N0  
IO, DIFFIO\_B25n, (DQ5B)/(DQ3B)/(DQ5B)  
IO, DIFFIO\_B26p, (DQ5B)/(DQ3B)/(DQ5B)  
IO, DIFFIO\_B26n, (DQ5B)/(DQ3B)/(DQ5B)  
IO, DIFFIO\_B27p, (DM4B)/(DM5B/BWS#5B)/(DM5B/BWS#5B)  
IO, DIFFIO\_B27n, (.),(DQ5B)/(DQ5B)

EP4CE40F23C8N



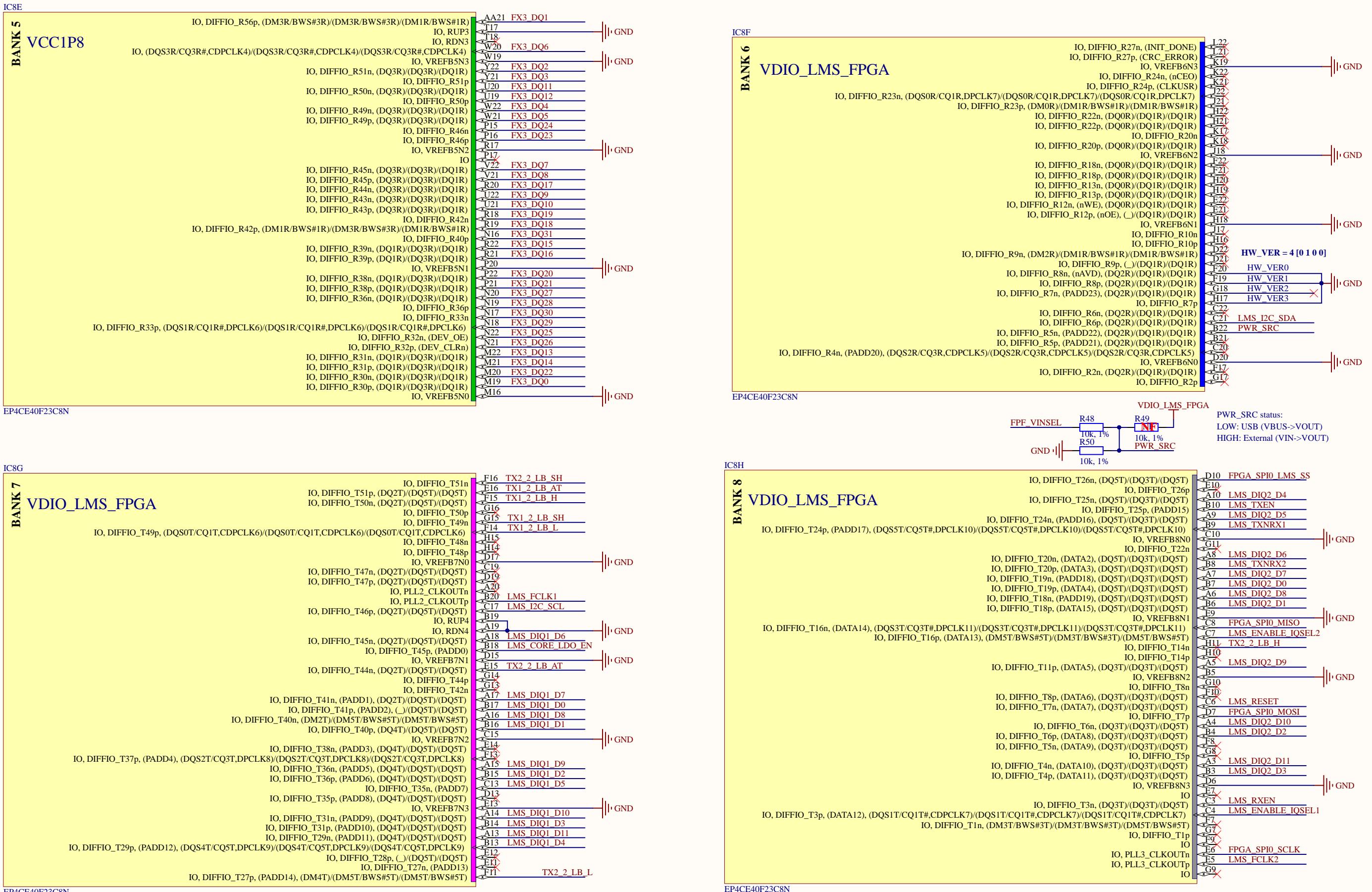
IC8B

**BANK 2**  
**VCC1P8**

IO, DIFFIO\_L26p, (DQ0L)/(DQ1L)/(DQ1L)  
IO, DIFFIO\_L26n, (DQ0L)/(DQ1L)/(DQ1L)  
IO, DIFFIO\_L27p, (DQ0L)/(DQ1L)/(DQ1L)  
M1 FX3\_CTL2  
M2 FX3\_CTL3  
M3 FX3\_CTL4  
M4 FX3\_CTL5  
M5 FX3\_CTL6  
M6 FX3\_CTL0  
M7 FX3\_CTL1  
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M440 FX3\_CTL439  
M441 FX3\_CTL440  
M442 FX3\_CTL441  
M443 FX3\_CTL442  
M444 FX3\_CTL443  
M445 FX3\_CTL444  
M446 FX3\_CTL445  
M447 FX3\_CTL446  
M448 FX3\_CTL447  
M449 FX3\_CTL448  
M450 FX3\_CTL449  
M451 FX3\_CTL450  
M452 FX3\_CTL451  
M453 FX3\_CTL452  
M454 FX3\_CTL453<br

NF elements on sheet: R49  
Number of NF elements on sheet: 1

## FPGA banks 5, 6, 7, 8



Project name: **LimeSDR-USB\_1v4.PnjPcb**

Title: **FPGA banks 5, 6, 7, 8**

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Guildford GU2 7YG  
Surrey  
United Kingdom



Size: **A3** Revision: **v1.4**

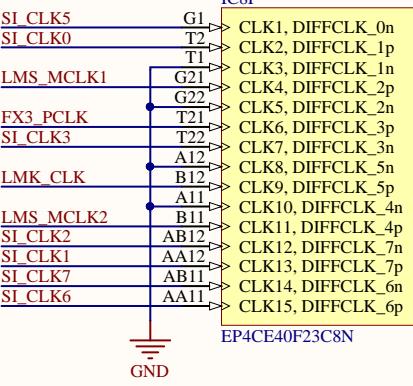
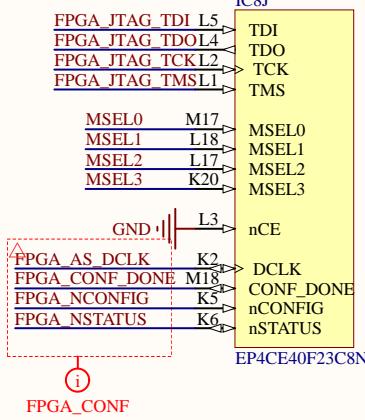
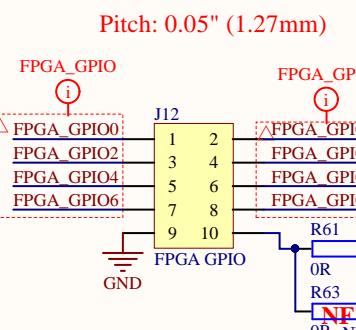
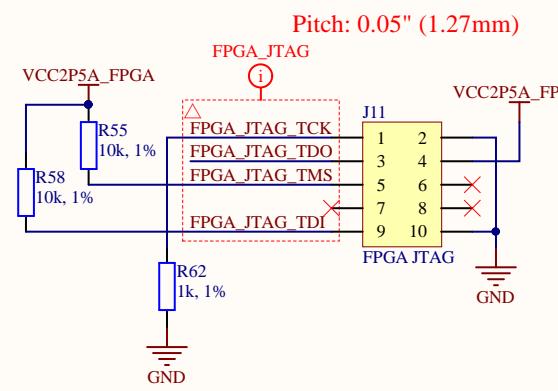
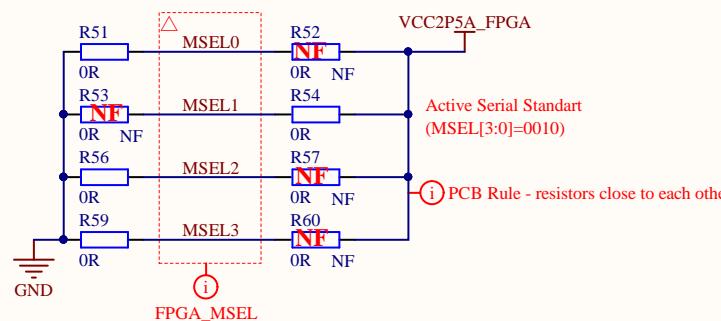
Date: **2017-02-01** Time: **14:58:08** Sheet **9** of **15**

File: **09\_FPGA\_banks\_5\_6\_7\_8.SchDoc**

NF elements on sheet: R52, R53, R57, R60, R63, R65, R74, J13, C142  
Number of NF elements on sheet: 10

## FPGA misc (power, clocks, config)

### MSEL config

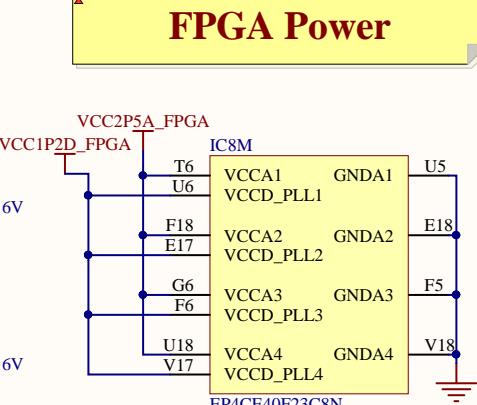
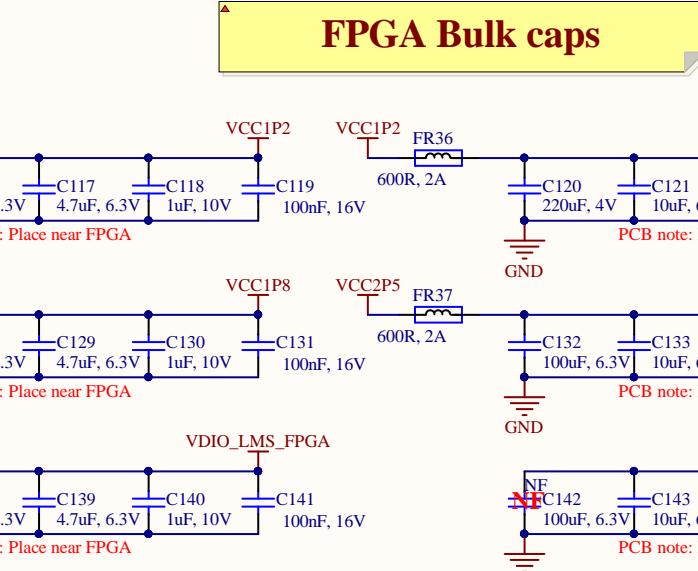
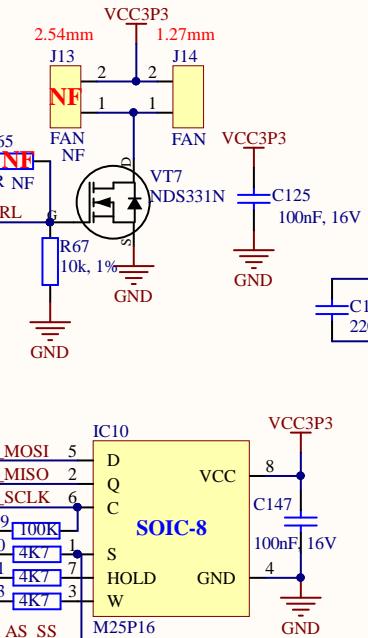
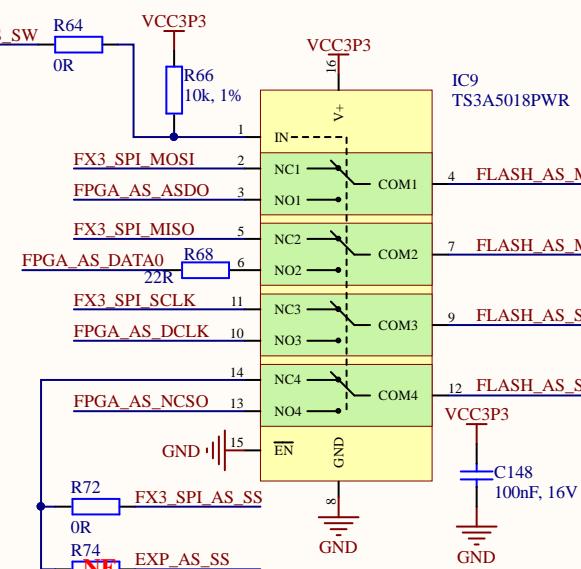


### FPGA AS FLASH + Switch

IN:

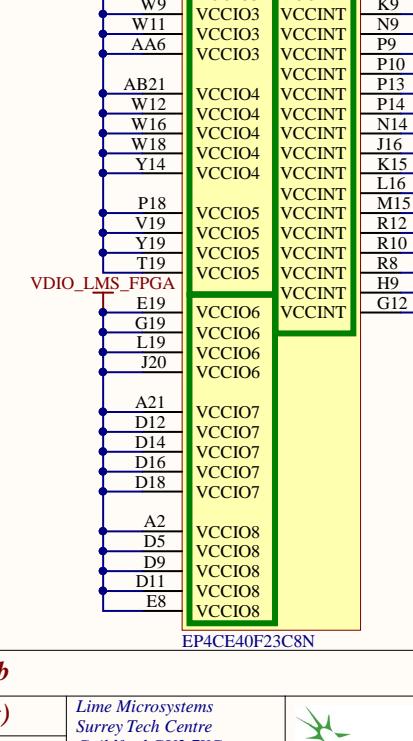
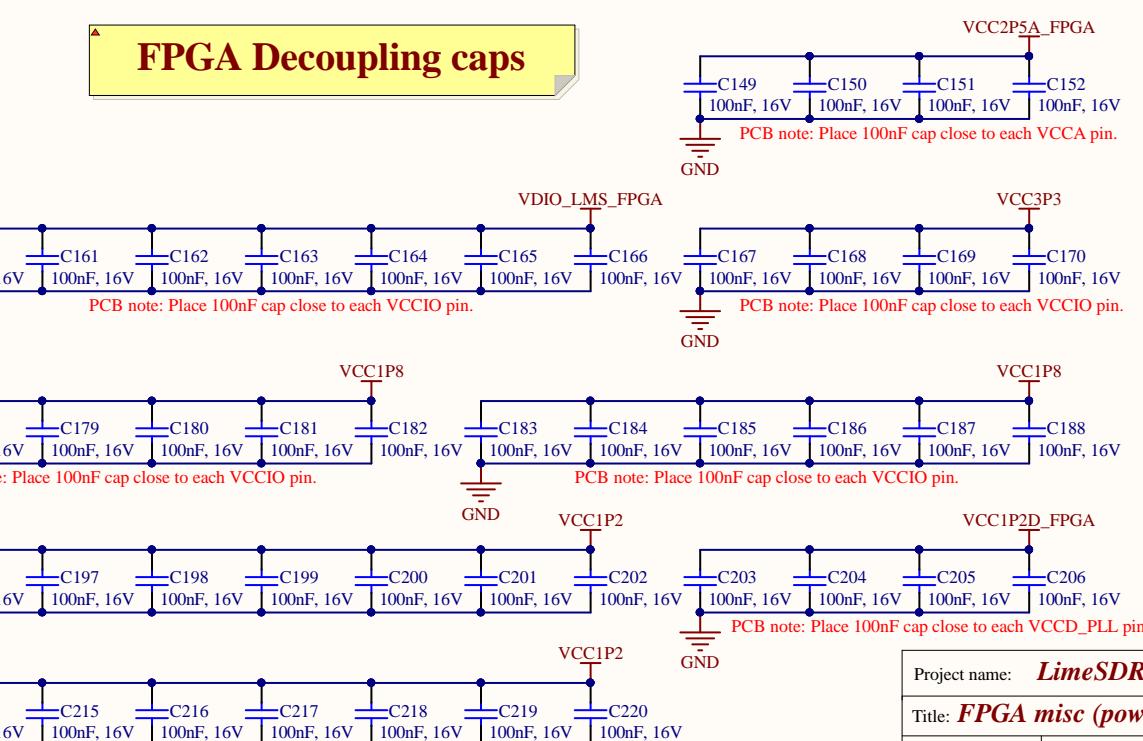
0: FLASH connected to FX3 (NC to COM)

1: FLASH connected to FPGA (NO to COM)



L10	GND	GND	C16
L11	GND	GND	A22
M10	GND	GND	E20
M11	GND	GND	G20
L12	GND	GND	L20
L13	GND	GND	P19
M12	GND	GND	V20
M13	GND	GND	Y20
N11	GND	GND	AB22
K11	GND	GND	Y18
N12	GND	GND	Y16
K12	GND	GND	Y12
K13	GND	GND	Y11
N13	GND	GND	Y9
N10	GND	GND	Y5
K10	GND	GND	AB1
J9	GND	GND	N3
F12	GND	GND	U3
H12	GND	GND	W3
H13	GND	GND	D3
J15	GND	GND	F3
K16	GND	GND	K3
L15	GND	GND	G2
N15	GND	GND	AA2
R13	GND	GND	AA22
R11	GND	GND	H3
R9	GND	GND	R3
P8	GND	GND	AB6
A1	GND	GND	Y15
C5	GND	GND	T20
C9	GND	GND	J19
C11	GND	GND	C18
C12	GND	GND	D8
C14	GND	GND	GND

### FPGA Decoupling caps



Project name: LimeSDR-USB\_1v4.PrjPcb

Title: FPGA misc (power, clocks, config)

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United Kingdom

Size: A3 Revision: v1.4

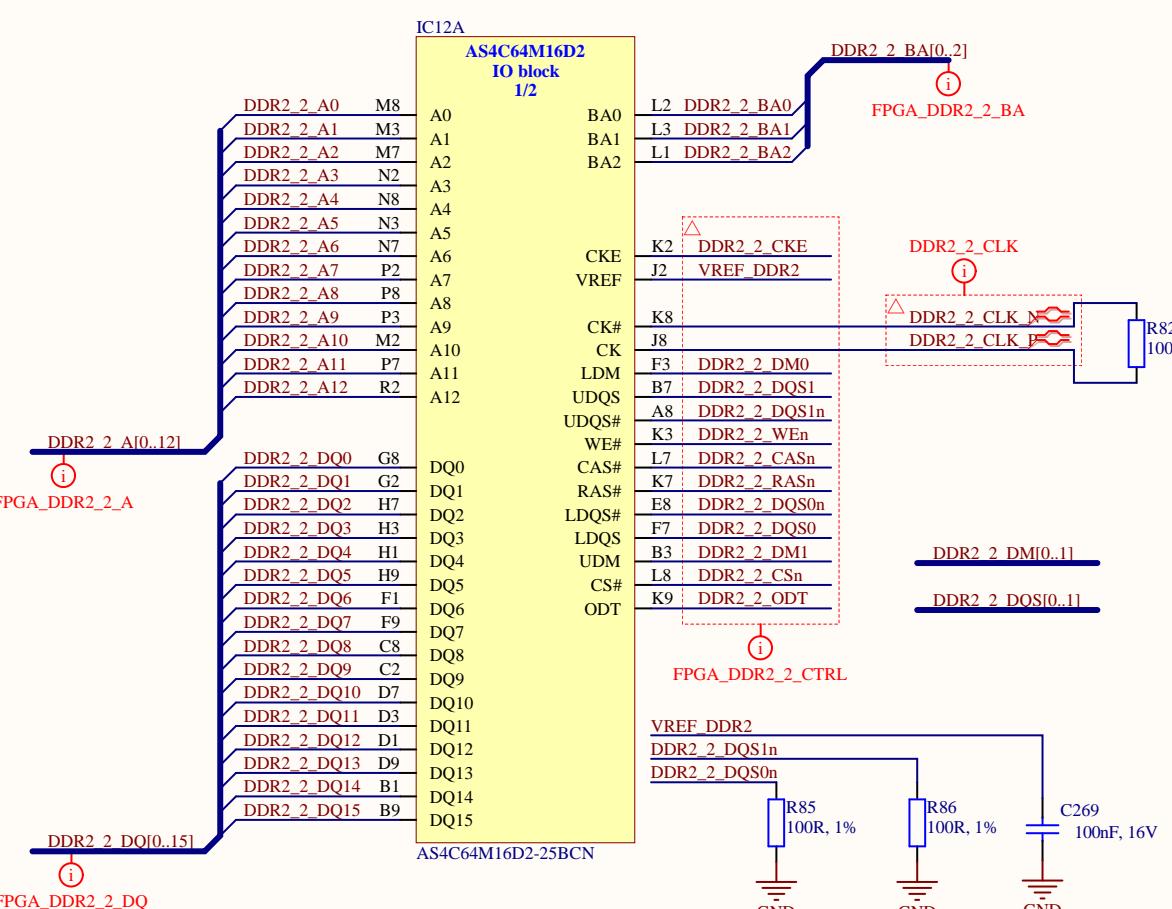
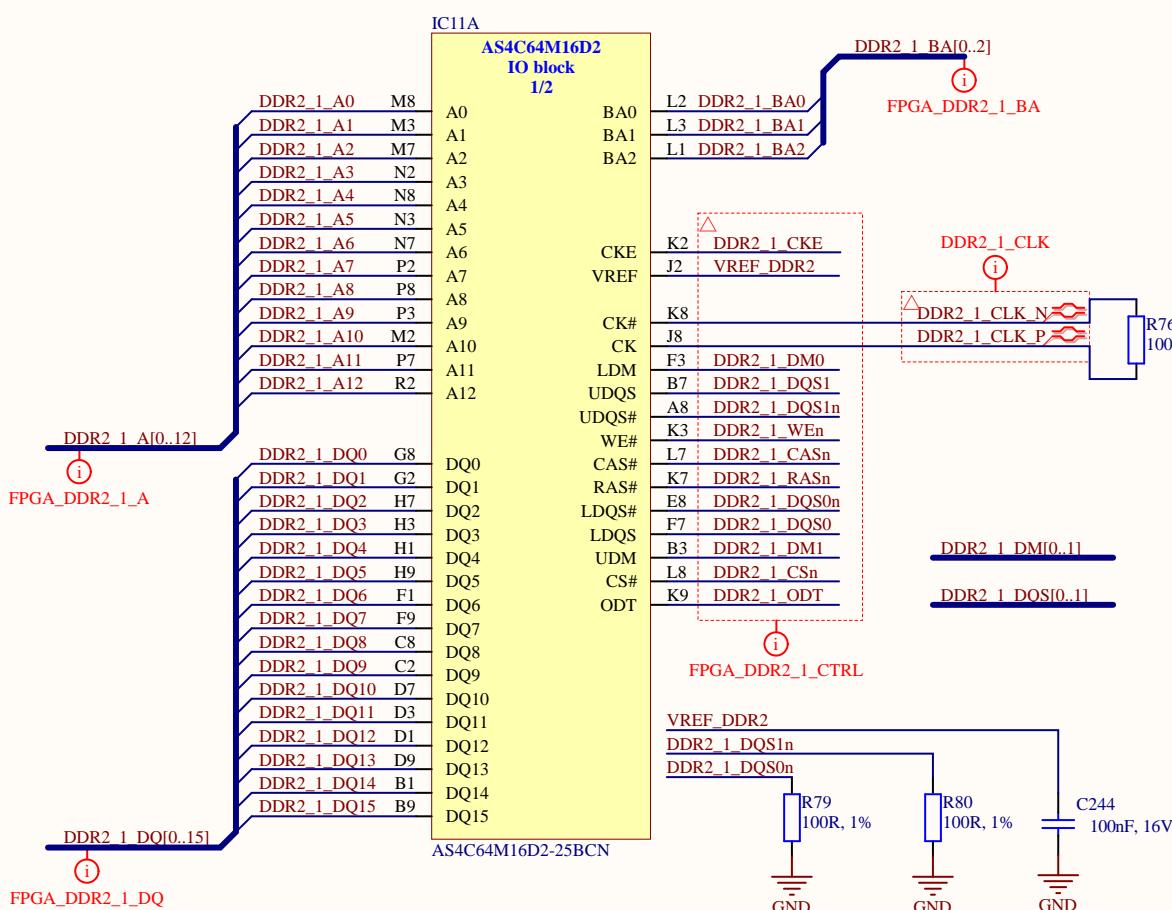
Date: 2017-02-01 Time: 14:58:12 Sheet 10 of 15

File: 10\_FPGA\_mis.SchDoc

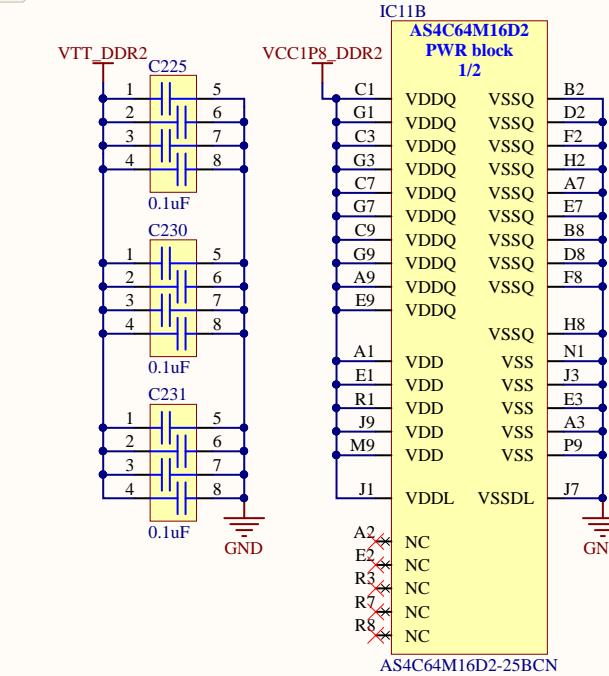


NF elements on sheet: -  
Number of NF elements on sheet: 0

## DDR2\_1 (BOT L)



## DDR2\_2 (BOT R)



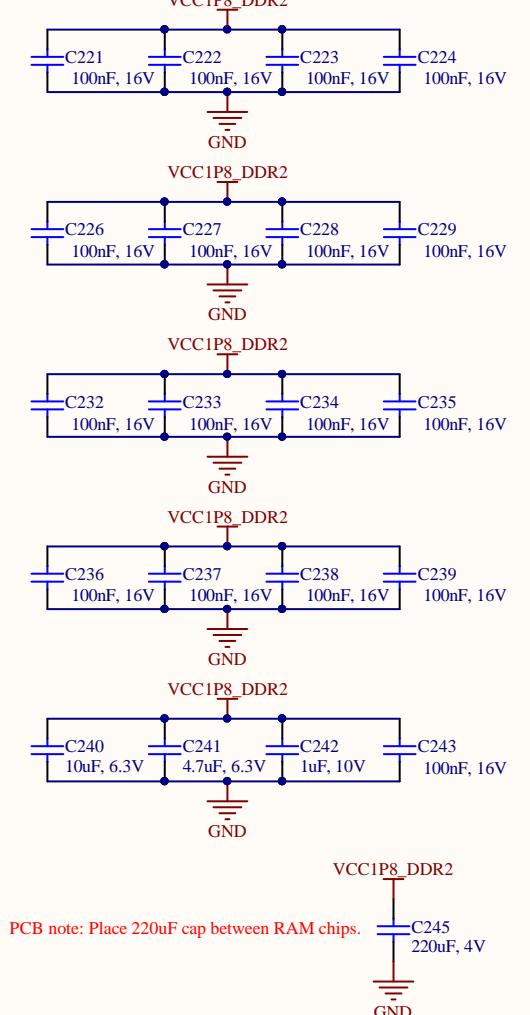
Project name: LimeSDR-USB\_1v4.PnjPcb

Title: RAM DDR2

Size: A3 Revision: v1.4

Date: 2017-02-01 Time: 14:58:16 Sheet 11 of 15

File: 11\_DDR2.SchDoc

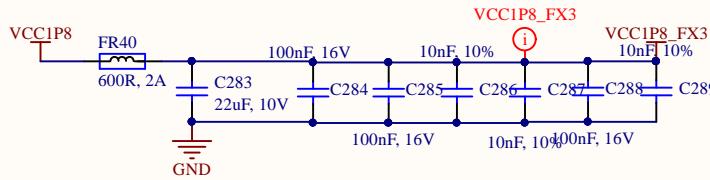




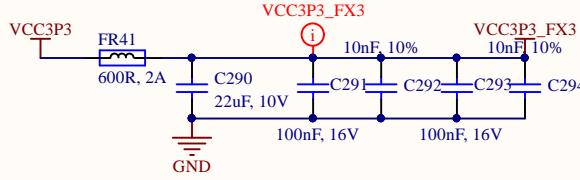
NF elements on sheet: FR42, FR43  
Number of NF elements on sheet: 2

## USB3 power

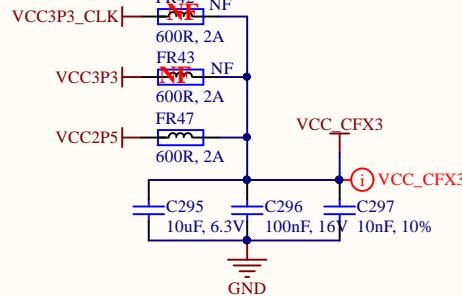
A



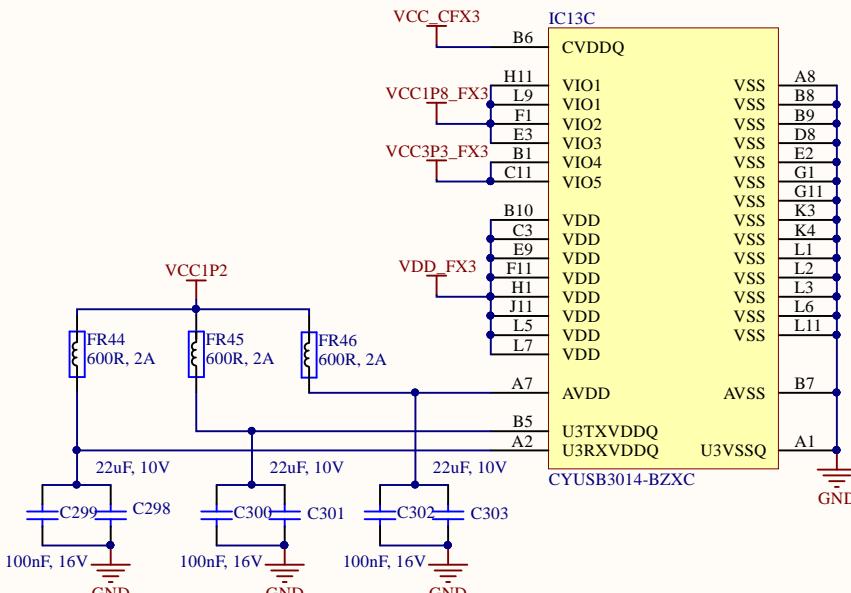
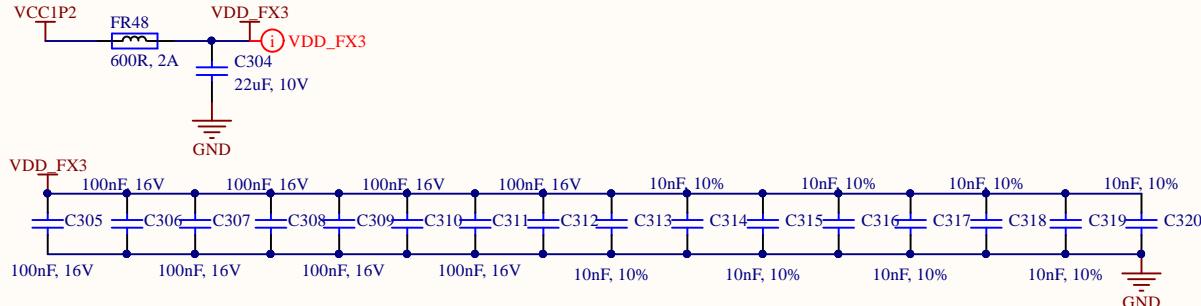
B



C



D



Project name: *LimeSDR-USB\_Iv4.PrbPcb*

Title: *USB3.0 power*

Size: *A4* Revision: *v1.4*

Date: *2017-02-01* Time: *14:58:23* Sheet *13 of 15*

File: *13\_USB3\_0\_power.SchDoc*

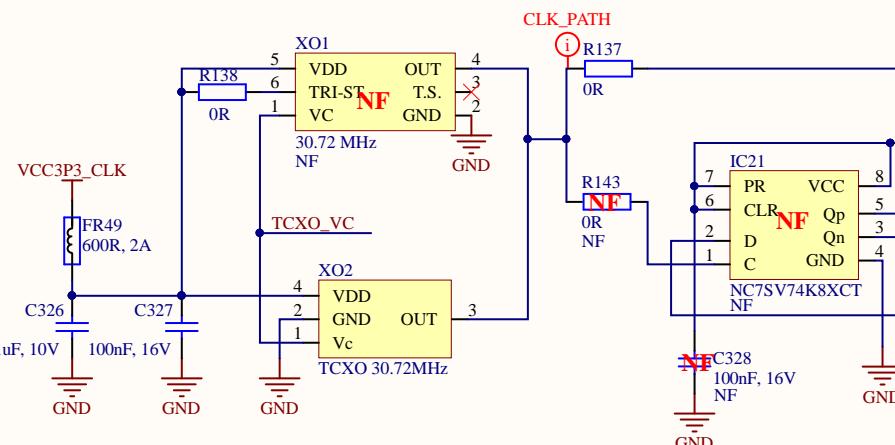
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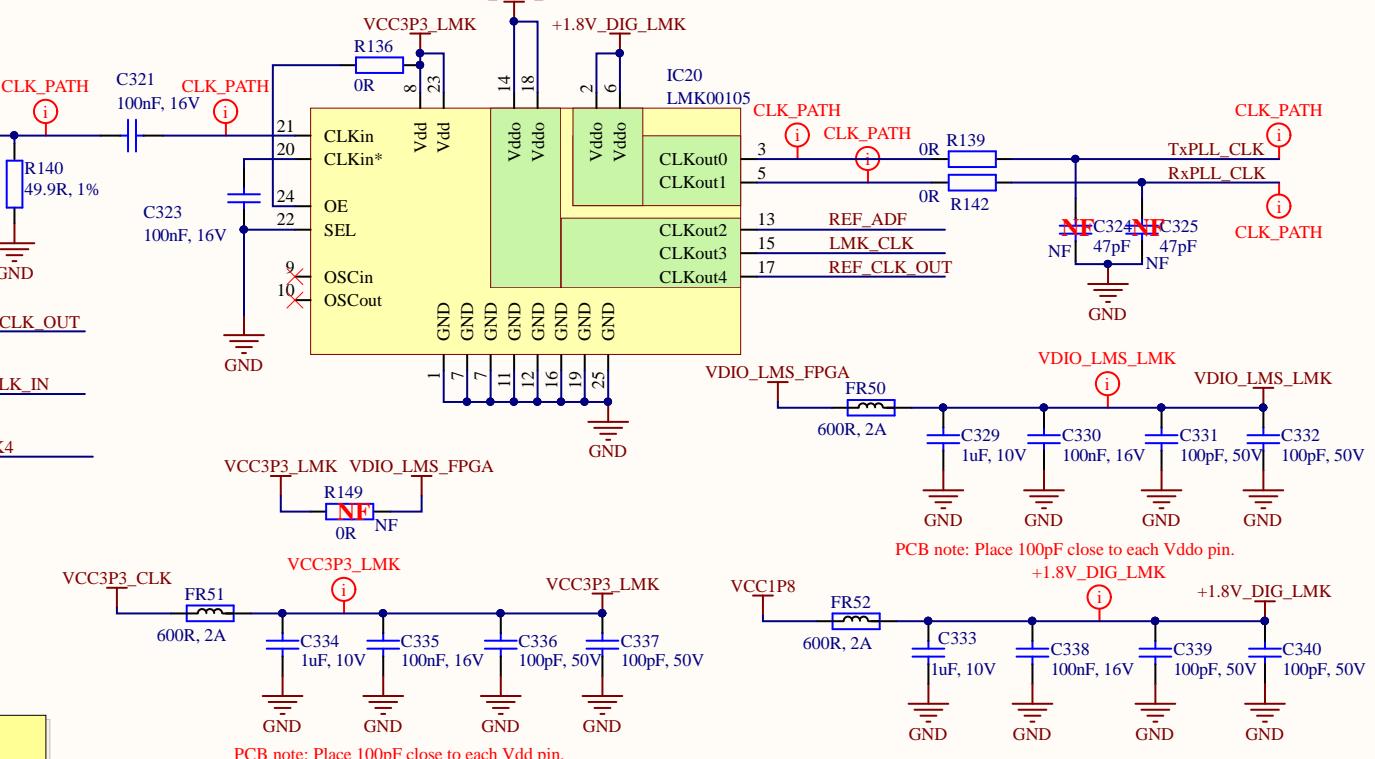
NF elements on sheet: XO1, R141, R143, R144, R145, R146, R147, R148, R149, R151, R155, C324, C325, C328, C341, IC21  
Number of NF elements on sheet: 16

## Clock circuits

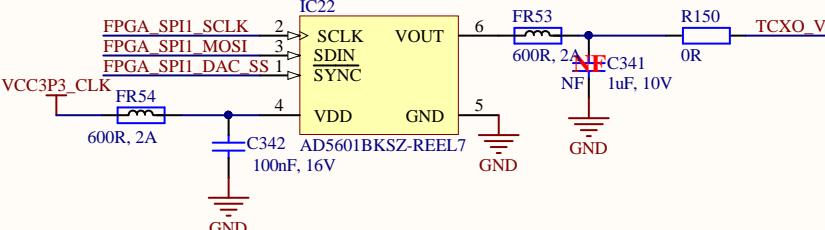
### (VC)TCXO



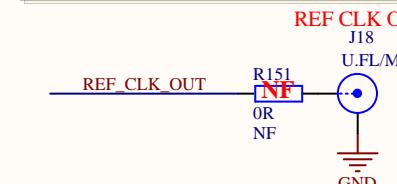
### Clock buffer



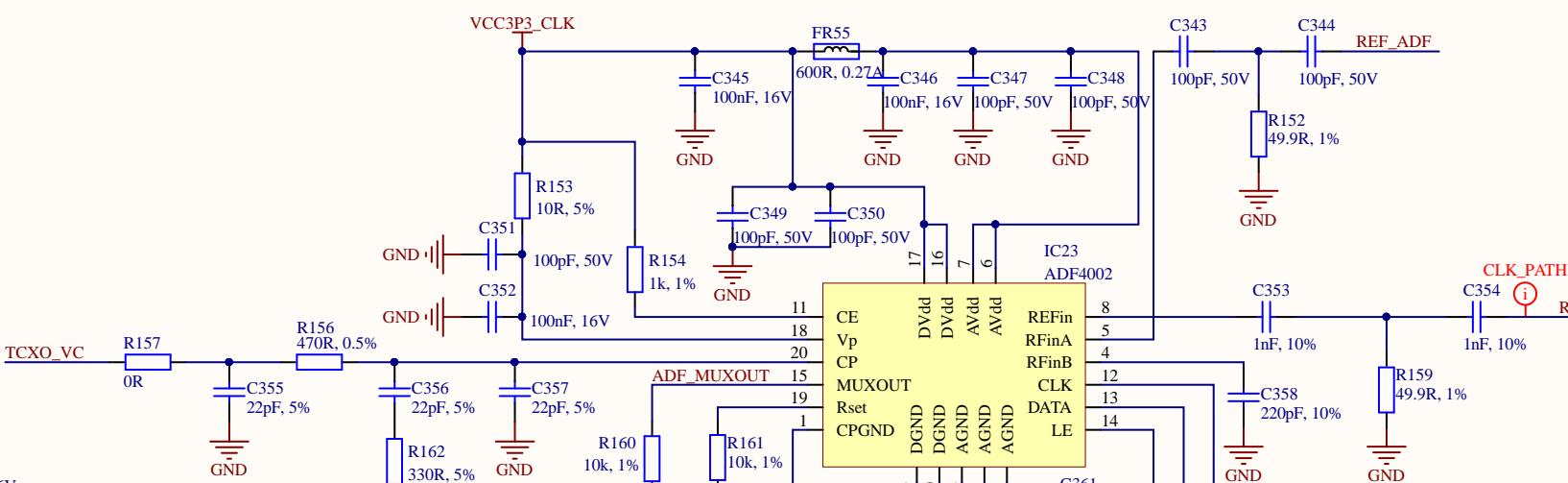
### TCXO DAC



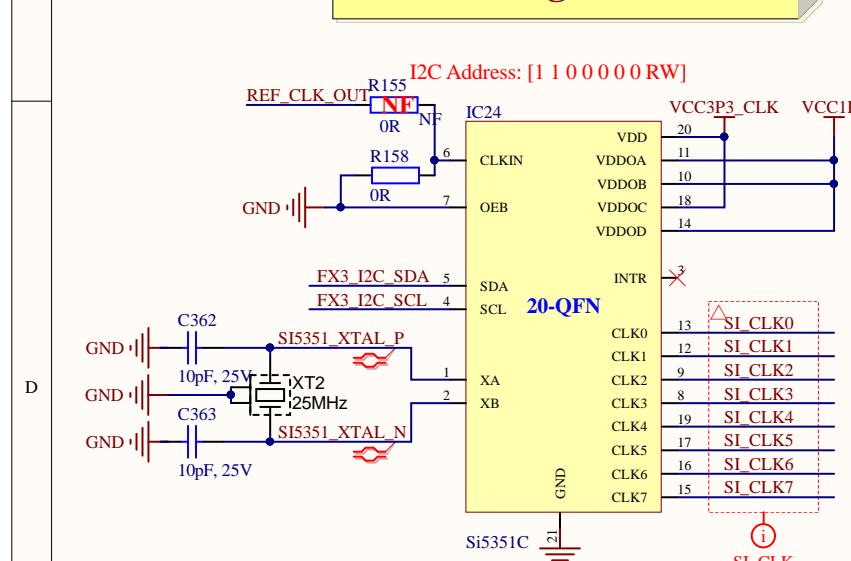
### REF CLK OUT



### Phase detector



### Clock generator



Project name: LimeSDR-USB\_1v4.PnjPcb

Title: Clocks

Size: A3

Revision: v1.4

Date: 2017-02-01

Time: 14:58:26

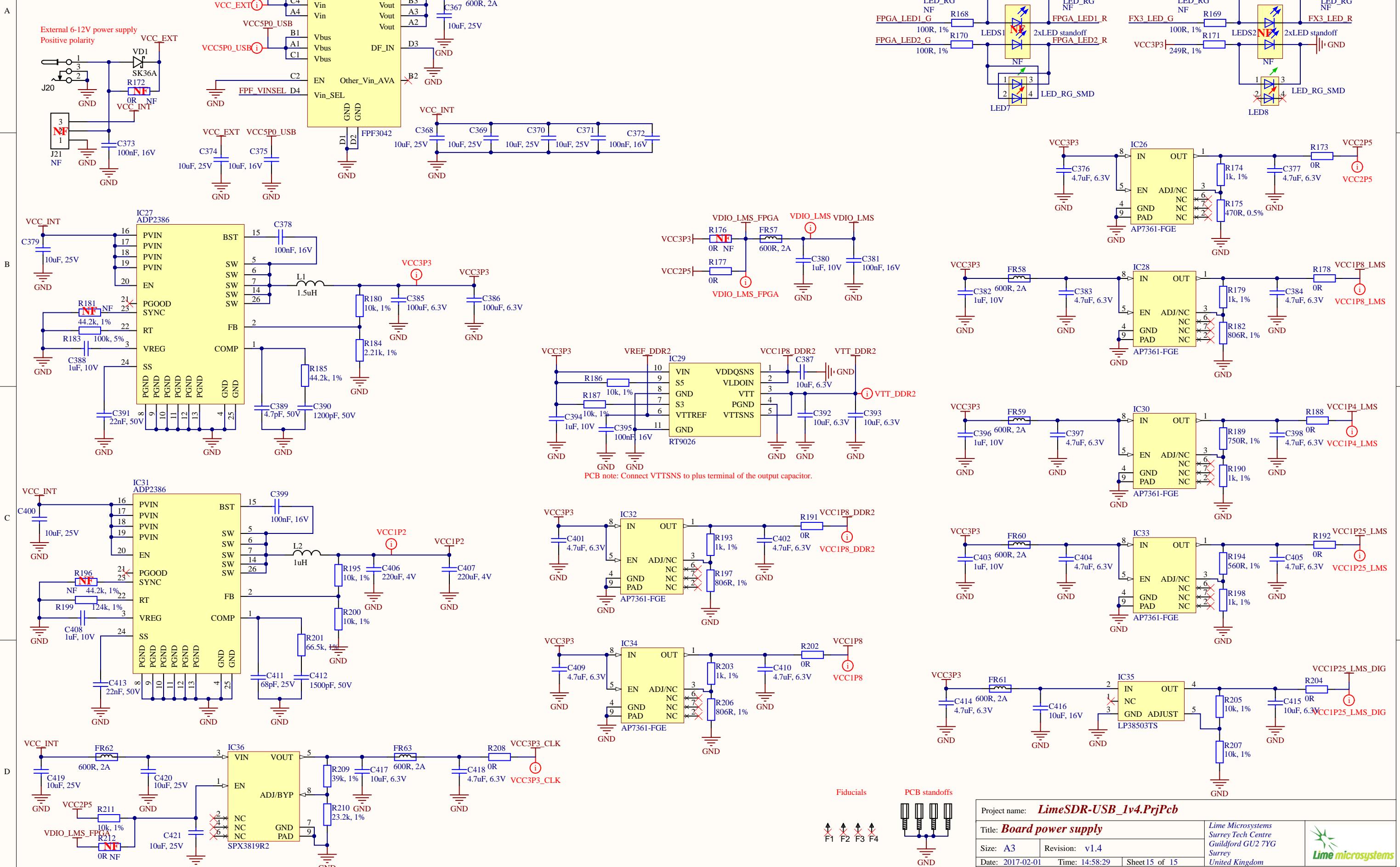
Sheet 14 of 15

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NF elements on sheet: R166, R167, R172, R176, R181, R196, R212, J21, LED3, LED4, LED5, LED6, LEDS1, LEDS2  
Number of NF elements on sheet: 14  
Total number of NF elements on all sheets: 60

## Board power circuits



Project name: **LimeSDR-USB\_1v4.PnjPcb**

Title: **Board power supply**

Size: **A3** Revision: **v1.4**

Date: **2017-02-01** Time: **14:58:29**

Sheet **15** of **15**

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