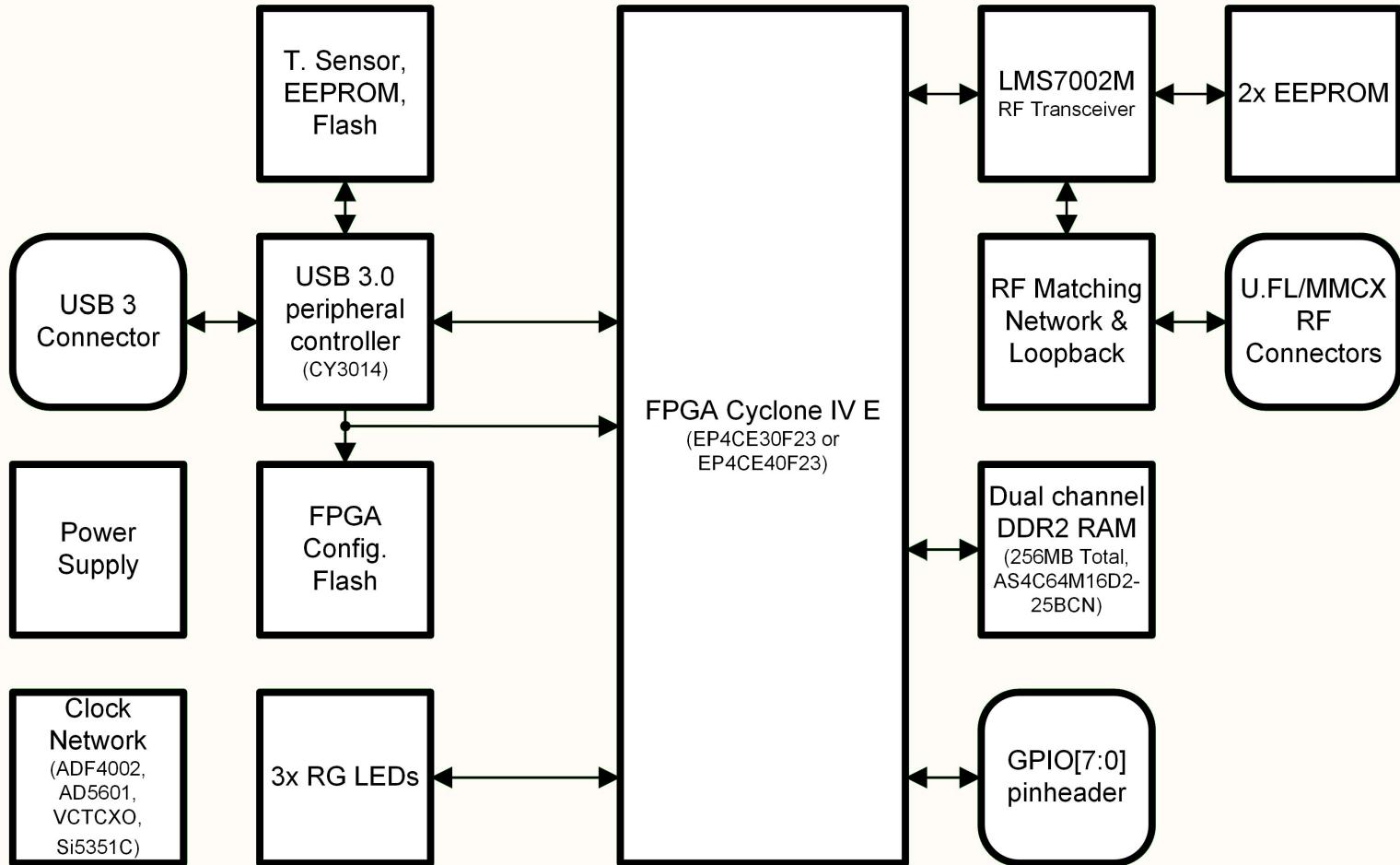


Block diagram



Project name: *LimeSDR-USB_1v4s.PrbPcb*

Title: *Block diagram*

Size: *A4* Revision: *v1.4s*

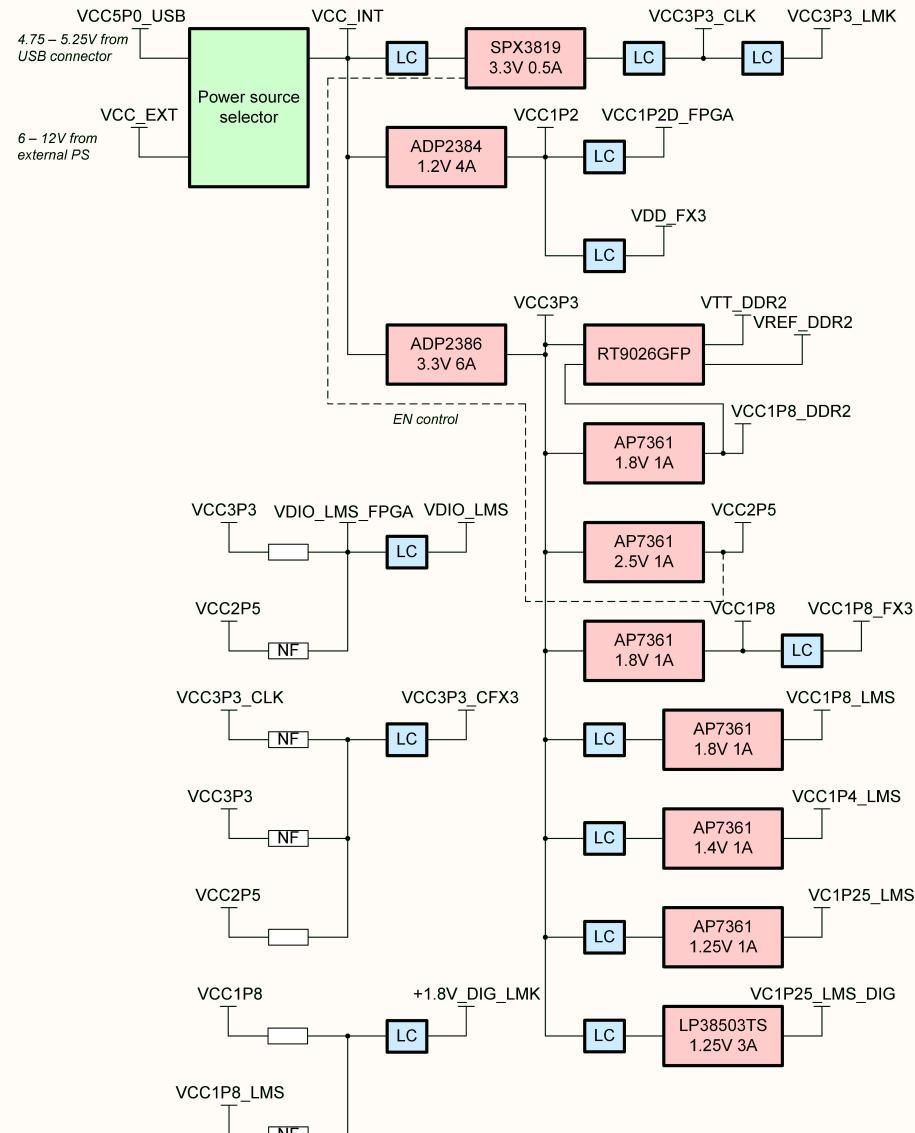
Date: *10/7/2016* Time: *1:14:36 PM* Sheet *1* of *15*

File: *01_BlockDiagram.SchDoc*

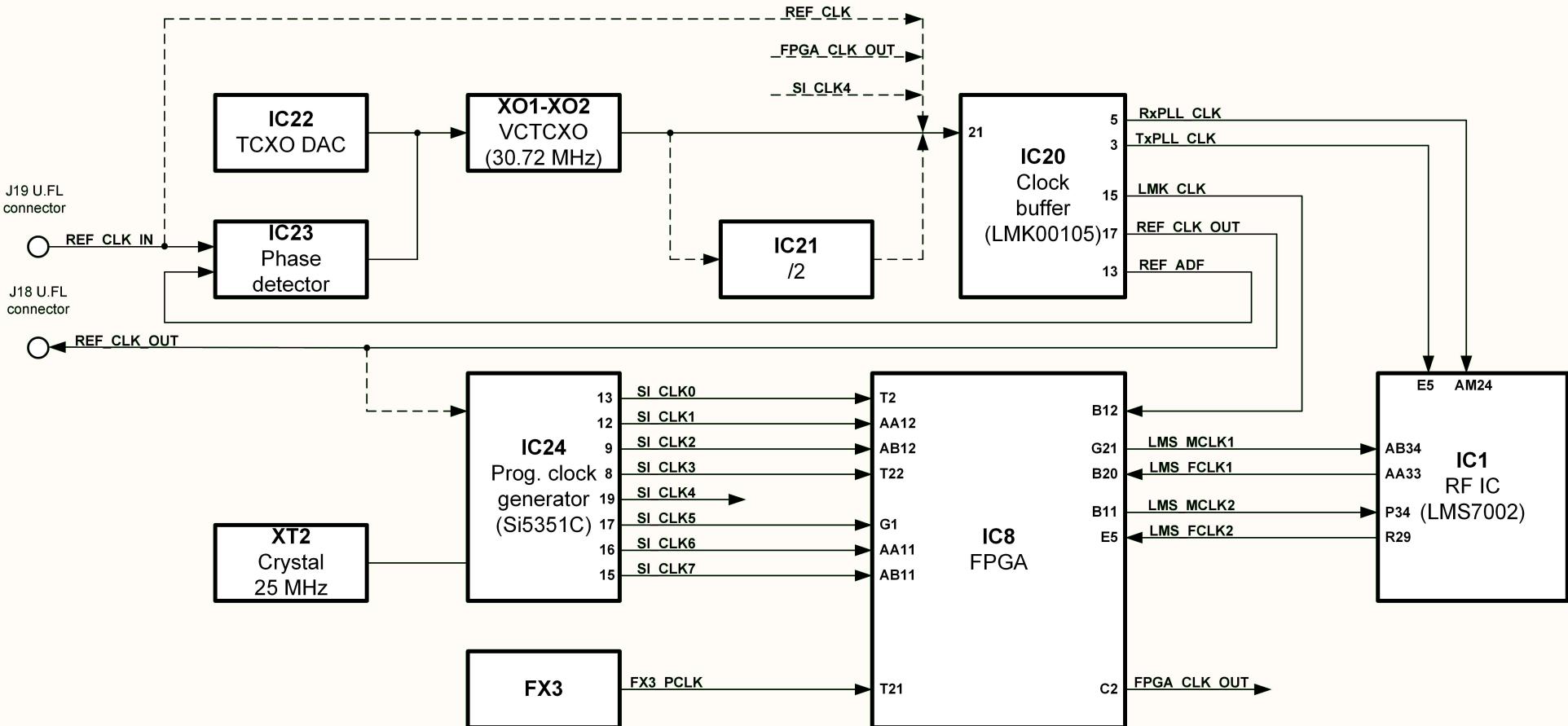
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Surrey
United Kingdom



Power diagram



Clock diagram



Project name: *LimeSDR-USB_1v4s.PrjPcb*

Title: *Clock diagram*

Size: *A4* Revision: *v1.4s*

Date: *10/7/2016* Time: *1:14:37 PM* Sheet *3* of *15*

File: *03_ClockDiagram.SchDoc*

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NF elements on sheet: -
Number of NF elements on sheet: 0

LMS7002M misc

A

A

B

B

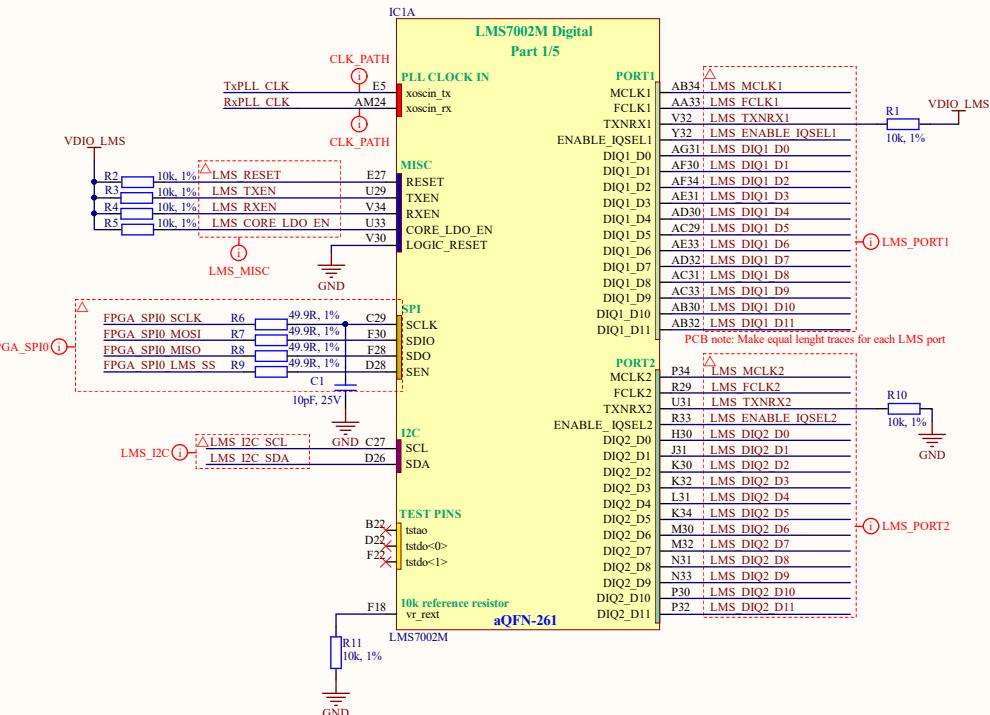
C

C

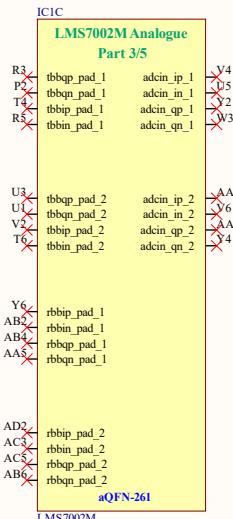
D

D

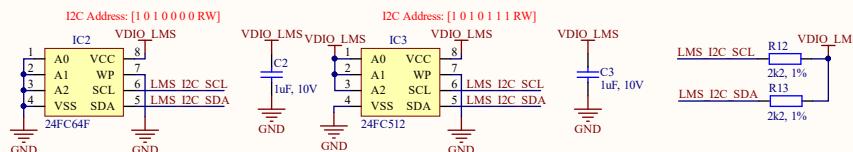
Digital interfaces



Baseband external IO



LMS EEPROMS



Project name: LimeSDR-USB_1v4s.PnjPcb

Title: LMS7002M misc

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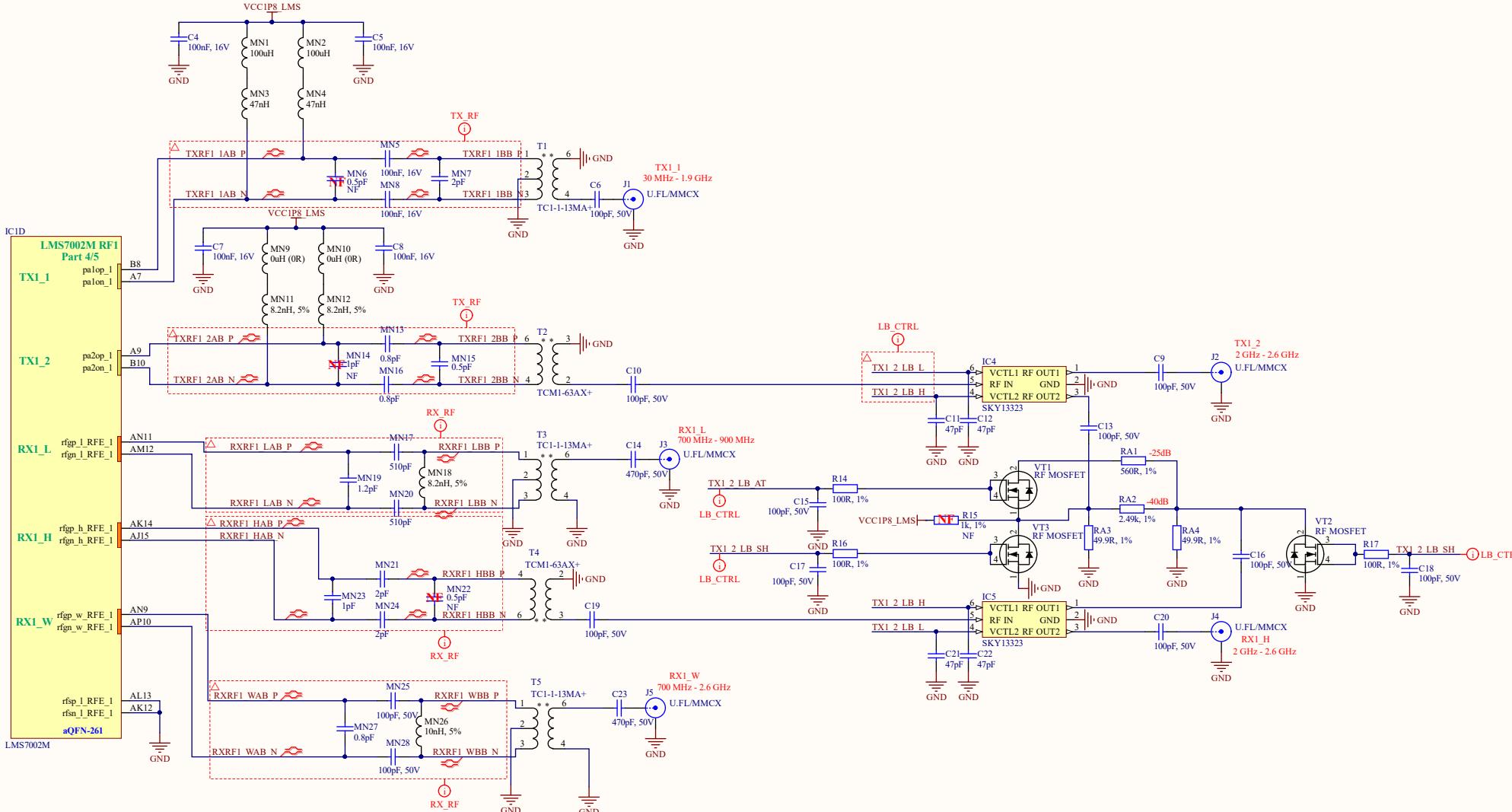
Size: A3 Revision: v1.4s

Date: 10/7/2016 Time: 11:43:38 PM Sheet 4 of 15

File: 04_LMS7002M_Misc.SchDoc

NF elements on sheet: MN6, MN14, MN22, R15
Number of NF elements on sheet: 4

LMS7002M RF1 circuits



Project name: LimeSDR-USB_Iv4s.PnjPcb

Title: LMS7002M RF

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Size: A3

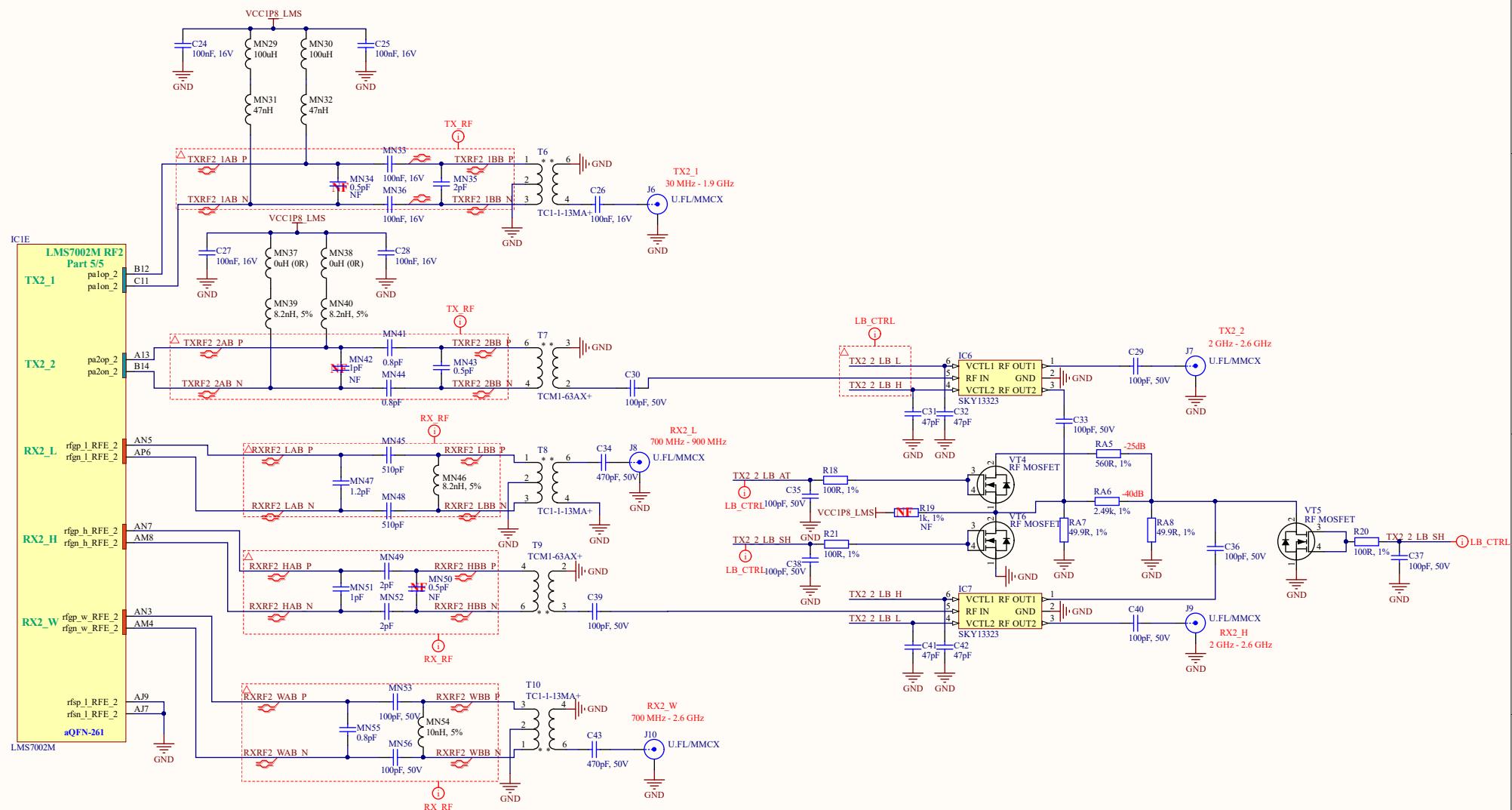
Revision: v1.4s

Date: 10/7/2016 Time: 1:14:38 PM Sheet 5 of 15

File: 05_LMS7002M_RF1.SchDoc

NF elements on sheet: MN34, MN42, MN50, R19
Number of NF elements on sheet: 4

LMS7002M RF2 circuits



Project name: LimeSDR-USB_Iv4s.PnjPcb

Title: LMS7002M RF

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United Kingdom

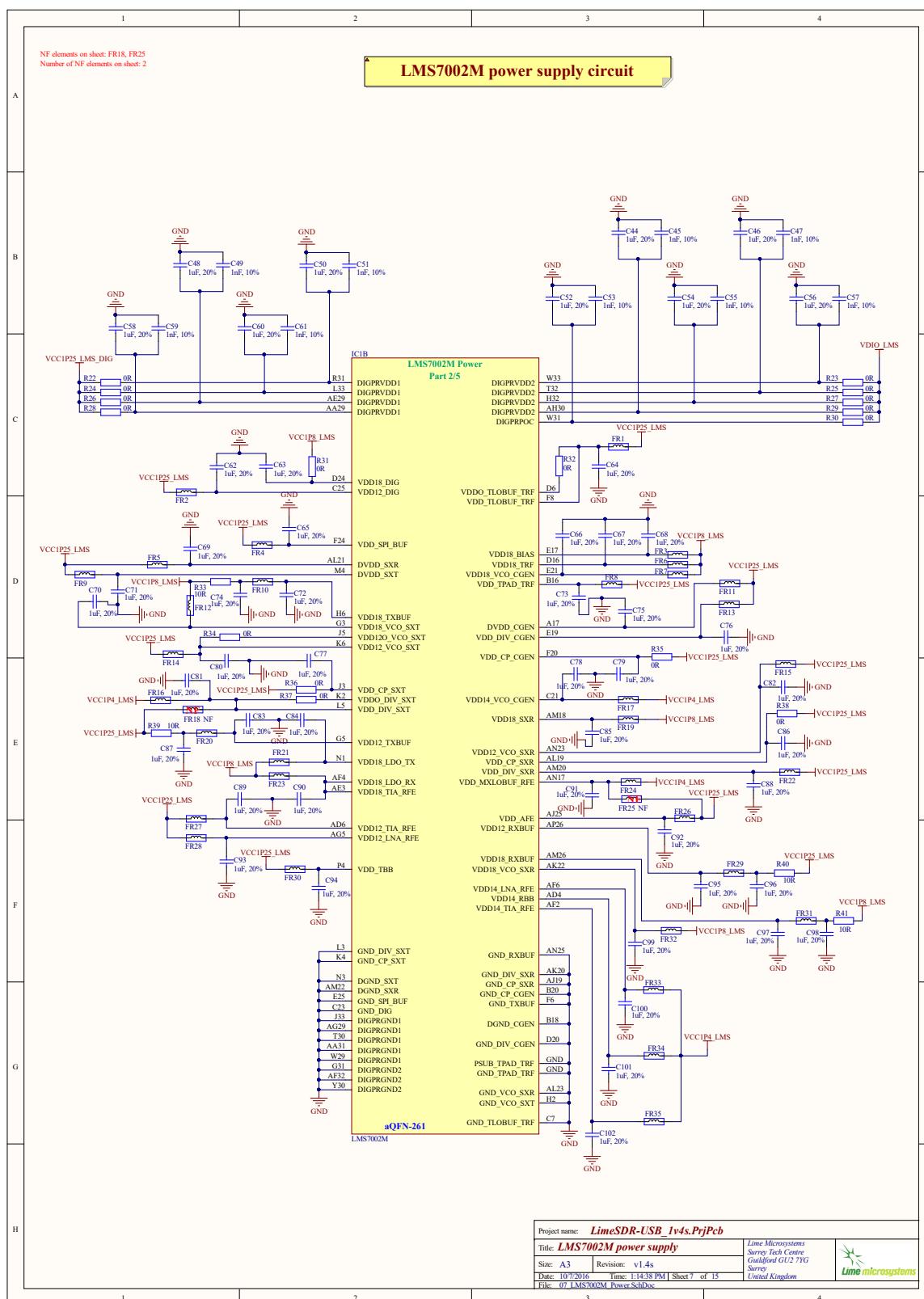


Size: A3

Revision: v1.4s

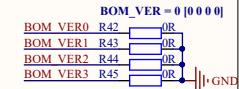
Date: 10/7/2016 Time: 1:14:38 PM Sheet 6 of 15

File: 06_LMS7002M_RF2.SchDoc



FPGA banks 1, 2, 3, 4

NF elements on sheet: -
Number of NF elements on sheet: 0



A
IC8A
BANK 1
VCC3P3

| | |
|--|-----------------------|
| IO, DIFFIO_L1p, (DQ1L)(DQ1L)(DQ1L) | G4 FPGA GPIO4 |
| IO, DIFFIO_L1n, (DQ1L)(DQ1L)(DQ1L) | B23 FPGA GPIO5 |
| IO, DIFFIO_L2p, (DQ2L)(DQ1L)(DQ1L) | B22 BRDG SPI SCLK |
| IO, DIFFIO_L2n, (DQ2L)(DQ1L)(DQ1L) | B21 BRDG SPI MOSI |
| IO, VREFB1N0 | G5 FX3 LED G |
| IO, DIFFIO_L4p, (nRESET), (DQ2L)(DQ1L)(DQ1L) | I4 FAN CTRL |
| IO, DIFFIO_L4n, (DQ2L)(DQ1L)(DQ1L) | I5 FPGA LED1 R |
| IO, DIFFIO_L5p, (DQ3L)(CDPCLK0)(DQS2L)(CQ3L,CDPCLK0) | C2 FPGA CLK OUT |
| IO, DIFFIO_L5n, (DQ3L)(CDPCLK0)(DQS2L)(CQ3L,CDPCLK0) | C1 BRDG SPI MISO |
| IO, DIFFIO_L7p, (DQ1L)(DQ1L)(DQ1L) | D2 FPGA LED1 G |
| IO, DIFFIO_L8p, (DQ1L)(DQ1L)(DQ1L) | D1 FPGA AS ASDO |
| IO, DIFFIO_L8n, (DATA1,ASDO) | I7 FPGA I2C SCL |
| IO, VREFB1N1 | I6 FPGA GPIO1 |
| IO, DIFFIO_L9p, (DQ2L)(DQ1L)(DQ1L) | L75 OS |
| IO, DIFFIO_L9n, (DQ2L)(DQ1L)(DQ1L) | E2 FPGA AS NCSD |
| IO, DIFFIO_L10p, (FLASH_nCE,CS0) | E1 BRDG SPI MOSI |
| IO, DIFFIO_L10n, () (DQ1L)(DQ1L) | D2 FPGA LED1 G |
| IO, DIFFIO_L12p, (DM2L)(DM1L/BWS#1L)(DM1L/BWS#1L) | D1 FPGA AS ASDO |
| IO, DIFFIO_L12n, (DQ0L)(DQ1L)(DQ1L) | I7 FPGA I2C SCL |
| IO, DIFFIO_L14p, (DQ1L)(DQ1L)(DQ1L) | I6 FPGA GPIO1 |
| IO, DIFFIO_L14n, (DQ1L)(DQ1L)(DQ1L) | I5 FX3 LED R |
| IO, VREFB1N2 | I8 FPGA SPII ADF SS |
| IO, DIFFIO_L15p, (DQ1L)(DQ1L)(DQ1L) | I7 BRDG SPI FGPA_SS |
| IO, DIFFIO_L15n, (DQ1L)(DQ1L)(DQ1L) | I8 FPGA LED2 R |
| IO, DIFFIO_L16p, (DQ1L)(DQ1L)(DQ1L) | I9 FPGA GPIO6 |
| IO, DIFFIO_L16n, (DQ1L)(DQ1L)(DQ1L) | I10 FPGA GPIO7 |
| IO, DIFFIO_L18p, (DQ1L)(DQ1L)(DQ1L) | I11 FPGA GPIO8 |
| IO, DIFFIO_L18n, (DQ1L)(DQ1L)(DQ1L) | I12 FPGA SPII DAC SS |
| IO, VREFB1N3 | I13 FPGA I2C SDA |
| IO, DIFFIO_L20p, (DQ0L)(DQ1L)(DQ1L) | I14 FPGA LED2 G |
| IO, DIFFIO_L20n, (DQ0L)(DQ1L)(DQ1L) | I15 BRDG SPI FGPA_SS |
| IO, DIFFIO_L22p, (DQ1L)(DQ1L)(DQ1L) | I16 FPGA GPIO2 |
| IO, DIFFIO_L22n, (DQ1L)(DQ1L)(DQ1L) | I17 FPGA GPIO3 |
| IO, DIFFIO_L24p, (DQ0L)(DQ1L)(DQ1L) | I18 FPGA SPIII DAC SS |
| IO, DIFFIO_L24n, (DQ0L)(DQ1L)(DQ1L) | I19 ADF MUXOUT |
| IO, DATA0 | I20 FPGA UART RX |
| | I21 FPGA AS DATA0 |

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C
IC8C
BANK 3
VCC1P8

| | |
|--|-----------------|
| IO, DIFFIO_B1p, (DM3B/BWS#3B)(DM3B/BWS#3B)(DM5B/BWS#5B) | V6 DDR2_1_A3 |
| IO, DIFFIO_B3p, (DQ3B)(DQ3B)(DQ3B) | V5 DDR2_1_DM1 |
| IO, VREFB3N3 | V7 DDR2_1_CLK_P |
| IO, VREFB3N4 | V8 DDR2_1_CLK_N |
| IO, DIFFIO_B6p, (DQS1B/CQ1B#,CDPCLK2)(DQS1B/CQ1B#,CDPCLK2) | V9 DDR2_1_Q0 |
| IO, PLL_CKOUTTr | V10 DDR2_1_A2 |
| IO, PLL_CKOUTTr | V11 DDR2_1_A10 |
| IO, DIFFIO_B7p, (DQ3B)(DQ3B)(DQ3B) | V12 DDR2_1_A5 |
| IO, PLL_CKOUTTr | V13 DDR2_1_DQ8 |
| IO, DIFFIO_B7n, (DQ3B)(DQ3B)(DQ3B) | V14 DDR2_1_A9 |
| IO, VREFB3N1 | V15 DDR2_1_DQ15 |
| IO, DIFFIO_B8p, (DQ3B)(DQ3B)(DQ3B) | V16 DDR2_1_DQ09 |
| IO, DIFFIO_B8n, (DQ3B)(DQ3B)(DQ3B) | V17 DDR2_1_A7 |
| IO, DIFFIO_B8t, (DQ3B)(DQ3B)(DQ3B) | V18 DDR2_1_A12 |
| IO, DIFFIO_B9p, (DQ3B)(DQ3B)(DQ3B) | V19 DDR2_1_DQ10 |
| IO, DIFFIO_B11p, (DQ3B)(DQ3B)(DQ3B) | V20 DDR2_1_DQ13 |
| IO, DIFFIO_B12p, (DQ3B)(DQ3B)(DQ3B) | V21 DDR2_1_DQ14 |
| IO, DIFFIO_B12n, (DQ3B)(DQ3B)(DQ3B) | V22 DDR2_1_DQ15 |
| IO, DIFFIO_B13p, (DQ3B)(DQ3B)(DQ3B) | V23 DDR2_1_DQ12 |
| IO, DIFFIO_B13n, (DQ3B)(DQ3B)(DQ3B) | V24 DDR2_1_DQ13 |
| IO, DIFFIO_B14p, (DMS5B/BWS#5B)(DM3B/BWS#3B)(DM5B/BWS#5B) | V25 DDR2_1_DQ07 |
| IO, DIFFIO_B14n, (DQ5B)(DQ3B)(DQ3B) | V26 DDR2_2_C5n |
| IO, DIFFIO_B15p, (DQ5B)(DQ3B)(DQ3B) | V27 DDR2_2_CASn |
| IO, DIFFIO_B15n, (DQ5B)(DQ3B)(DQ3B) | V28 DDR2_2_RASn |
| IO, VREFB3N1 | V29 DDR2_1_DQ05 |
| IO, DIFFIO_B16p, (DQS3B/CQ3B#,DPCLK2)(DQS3B/CQ3B#,DPCLK2) | V30 DDR2_1_DQ01 |
| IO, DIFFIO_B16n, (DQS3B/CQ3B#,DPCLK2) | V31 DDR2_1_DQ00 |
| IO, DIFFIO_B17p, (DQS3B/CQ3B#,DPCLK2) | V32 DDR2_1_DQ06 |
| IO, DIFFIO_B17n, (DQS3B/CQ3B#,DPCLK2) | V33 DDR2_1_DQ01 |
| IO, DIFFIO_B18p, (DQS3B/CQ3B#,DPCLK2) | V34 DDR2_1_DQ03 |
| IO, DIFFIO_B18n, (DQS3B/CQ3B#,DPCLK2) | V35 DDR2_1_DQ02 |
| IO, DIFFIO_B19p, (DQS3B/CQ3B#,DPCLK2) | V36 DDR2_1_DQ00 |
| IO, DIFFIO_B19n, (DQS3B/CQ3B#,DPCLK2) | V37 DDR2_1_DQ01 |
| IO, DIFFIO_B20p, (DQS3B/CQ3B#,DPCLK2) | V38 DDR2_1_DQ03 |
| IO, DIFFIO_B20n, (DQS3B/CQ3B#,DPCLK2) | V39 DDR2_1_DQ02 |
| IO, DIFFIO_B21p, (DQS5B/CQ5B#,DPCLK3)(DQS5B/CQ5B#,DPCLK3) | V40 DDR2_1_DQ05 |
| IO, DIFFIO_B21n, (DQS5B/CQ5B#,DPCLK3)(DQS5B/CQ5B#,DPCLK3) | V41 DDR2_1_DQ04 |
| IO, DIFFIO_B22p, (DQS5B/CQ5B#,DPCLK3)(DQS5B/CQ5B#,DPCLK3) | V42 DDR2_1_DQ05 |
| IO, DIFFIO_B22n, (DQS5B/CQ5B#,DPCLK3)(DQS5B/CQ5B#,DPCLK3) | V43 DDR2_1_DQ07 |
| IO, DIFFIO_B23p, (DQS5B/CQ5B#,DPCLK3)(DQS5B/CQ5B#,DPCLK3) | V44 DDR2_2_DM1 |
| IO, DIFFIO_B23n, (DQS5B/CQ5B#,DPCLK3)(DQS5B/CQ5B#,DPCLK3) | V45 DDR2_2_DM1 |
| IO, DIFFIO_B24p, (DQS5B/CQ5B#,DPCLK3)(DQS5B/CQ5B#,DPCLK3) | V46 DDR2_2_DM1 |
| IO, DIFFIO_B24n, (DQS5B/CQ5B#,DPCLK3)(DQS5B/CQ5B#,DPCLK3) | V47 DDR2_2_DM1 |
| IO, DIFFIO_B25p, (DQS5B/CQ5B#,DPCLK3)(DQS5B/CQ5B#,DPCLK3) | V48 DDR2_2_DM1 |
| IO, DIFFIO_B25n, (DQS5B/CQ5B#,DPCLK3)(DQS5B/CQ5B#,DPCLK3) | V49 DDR2_2_DM1 |
| IO, DIFFIO_B26p, (DQS5B/CQ5B#,DPCLK3)(DQS5B/CQ5B#,DPCLK3) | V50 DDR2_2_DM1 |
| IO, DIFFIO_B26n, (DQS5B/CQ5B#,DPCLK3)(DQS5B/CQ5B#,DPCLK3) | V51 DDR2_2_DM1 |
| IO, DIFFIO_B27p, (DM4B)(DM5B/BWS#5B)(DM5B/BWS#5B) | V52 DDR2_2_CKE |
| IO, DIFFIO_B27n, () (DQS5B)(DQS5B) | V53 DDR2_2_DM1 |

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VREF DDR2

PCB note: Place 100nF cap close to each Vref pin.

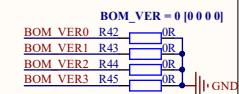
GND

NF elements on sheet: -
Number of NF elements on sheet: 0

B
IC8B
BANK 2
VCC1P8

| | |
|---|-------------------|
| IO, DIFFIO_L26p, (DQ0L)(DQ1L)(DQ1L) | L6 FX3 CTL0 |
| IO, DIFFIO_L27p, (DQ0L)(DQ1L)(DQ1L) | M1 FX3 CTL6 |
| IO, DIFFIO_L28p, (DQ0L)(DQ1L)(DQ1L) | M2 FX3 CTL1 |
| IO, DIFFIO_L28n, (DQ0L)(DQ1L)(DQ1L) | M3 FX3 CTL2 |
| IO, DIFFIO_L29p, (DQ0L)(DQ1L)(DQ1L) | M4 FX3 CTL5 |
| IO, DIFFIO_L29n, (DQ0L)(DQ1L)(DQ1L) | M5 FX3 CTL4 |
| IO, DIFFIO_L30p, (DQ0L)(DQ1L)(DQ1L) | N1 FX3 CTL9 |
| IO, DIFFIO_L30n, (DQ0L)(DQ1L)(DQ1L) | N2 FX3 CTL10 |
| IO, DIFFIO_L34p, (DQS1L/CQ1L#,DPCLK1)(DQS1L/CQ1L#,DPCLK1) | N3 FX3 CTL11 |
| IO, DIFFIO_L35p, (DM1L/BWS#1L)(DM3L/BWS#3L)(DM1L/BWS#1L) | N4 FX3 CTL12 |
| IO, DIFFIO_L35n, (DM1L/BWS#1L)(DM3L/BWS#3L)(DM1L/BWS#1L) | N5 FX3 CTL7 |
| IO, DIFFIO_L36p, (DQ3L)(DQ3L)(DQ3L) | N6 FX3 CTL8 |
| IO, DIFFIO_L36n, (DQ3L)(DQ3L)(DQ3L) | N7 FX3 CTL9 |
| IO, DIFFIO_L41p, (DQ3L)(DQ3L)(DQ3L) | N8 DDR2_2_A7 |
| IO, DIFFIO_L41n, (DQ3L)(DQ3L)(DQ3L) | N9 DDR2_1_A11 |
| IO, DIFFIO_L44p, (DQ3L)(DQ3L)(DQ3L) | N10 DDR2_1_A0 |
| IO, DIFFIO_L44n, (DQ3L)(DQ3L)(DQ3L) | N11 DDR2_1_A6 |
| IO, RDNI | N12 DDR2_1_A8 |
| IO, RUP1 | N13 DDR2_1_BA1 |
| IO, DDR2_1_BA1 | N14 DDR2_1_BA1 |
| IO, DDR2_1_BA4 | N15 DDR2_1_BA4 |
| IO, DDR2_1_BA5 | N16 DDR2_2_BA5 |
| IO, DDR2_1_BA6 | N17 DDR2_2_BA6 |
| IO, DDR2_1_BA7 | N18 DDR2_2_BA7 |
| IO, DDR2_1_BA9 | N19 DDR2_2_BA9 |
| IO, DDR2_1_BA10 | N20 DDR2_2_BA10 |
| IO, DDR2_1_BA11 | N21 DDR2_2_BA11 |
| IO, DDR2_1_BA12 | N22 DDR2_2_BA12 |
| IO, DDR2_1_BA13 | N23 DDR2_2_BA13 |
| IO, DDR2_1_BA14 | N24 DDR2_2_BA14 |
| IO, DDR2_1_BA15 | N25 DDR2_2_BA15 |
| IO, DDR2_1_BA16 | N26 DDR2_2_BA16 |
| IO, DDR2_1_BA17 | N27 DDR2_2_BA17 |
| IO, DDR2_1_BA18 | N28 DDR2_2_BA18 |
| IO, DDR2_1_BA19 | N29 DDR2_2_BA19 |
| IO, DDR2_1_BA20 | N30 DDR2_2_BA20 |
| IO, DDR2_1_BA21 | N31 DDR2_2_BA21 |
| IO, DDR2_1_BA22 | N32 DDR2_2_BA22 |
| IO, DDR2_1_BA23 | N33 DDR2_2_BA23 |
| IO, DDR2_1_BA24 | N34 DDR2_2_BA24 |
| IO, DDR2_1_BA25 | N35 DDR2_2_BA25 |
| IO, DDR2_1_BA26 | N36 DDR2_2_BA26 |
| IO, DDR2_1_BA27 | N37 DDR2_2_BA27 |
| IO, DDR2_1_BA28 | N38 DDR2_2_BA28 |
| IO, DDR2_1_BA29 | N39 DDR2_2_BA29 |
| IO, DDR2_1_BA30 | N40 DDR2_2_BA30 |
| IO, DDR2_1_BA31 | N41 DDR2_2_BA31 |
| IO, DDR2_1_BA32 | N42 DDR2_2_BA32 |
| IO, DDR2_1_BA33 | N43 DDR2_2_BA33 |
| IO, DDR2_1_BA34 | N44 DDR2_2_BA34 |
| IO, DDR2_1_BA35 | N45 DDR2_2_BA35 |
| IO, DDR2_1_BA36 | N46 DDR2_2_BA36 |
| IO, DDR2_1_BA37 | N47 DDR2_2_BA37 |
| IO, DDR2_1_BA38 | N48 DDR2_2_BA38 |
| IO, DDR2_1_BA39 | N49 DDR2_2_BA39 |
| IO, DDR2_1_BA40 | N50 DDR2_2_BA40 |
| IO, DDR2_1_BA41 | N51 DDR2_2_BA41 |
| IO, DDR2_1_BA42 | N52 DDR2_2_BA42 |
| IO, DDR2_1_BA43 | N53 DDR2_2_BA43 |
| IO, DDR2_1_BA44 | N54 DDR2_2_BA44 |
| IO, DDR2_1_BA45 | N55 DDR2_2_BA45 |
| IO, DDR2_1_BA46 | N56 DDR2_2_BA46 |
| IO, DDR2_1_BA47 | N57 DDR2_2_BA47 |
| IO, DDR2_1_BA48 | N58 DDR2_2_BA48 |
| IO, DDR2_1_BA49 | N59 DDR2_2_BA49 |
| IO, DDR2_1_BA50 | N60 DDR2_2_BA50 |
| IO, DDR2_1_BA51 | N61 DDR2_2_BA51 |
| IO, DDR2_1_BA52 | N62 DDR2_2_BA52 |
| IO, DDR2_1_BA53 | N63 DDR2_2_BA53 |
| IO, DDR2_1_BA54 | N64 DDR2_2_BA54 |
| IO, DDR2_1_BA55 | N65 DDR2_2_BA55 |
| IO, DDR2_1_BA56 | N66 DDR2_2_BA56 |
| IO, DDR2_1_BA57 | N67 DDR2_2_BA57 |
| IO, DDR2_1_BA58 | N68 DDR2_2_BA58 |
| IO, DDR2_1_BA59 | N69 DDR2_2_BA59 |
| IO, DDR2_1_BA60 | N70 DDR2_2_BA60 |
| IO, DDR2_1_BA61 | N71 DDR2_2_BA61 |
| IO, DDR2_1_BA62 | N72 DDR2_2_BA62 |
| IO, DDR2_1_BA63 | N73 DDR2_2_BA63 |
| IO, DDR2_1_BA64 | N74 DDR2_2_BA64 |
| IO, DDR2_1_BA65 | N75 DDR2_2_BA65 |
| IO, DDR2_1_BA66 | N76 DDR2_2_BA66 |
| IO, DDR2_1_BA67 | N77 DDR2_2_BA67 |
| IO, DDR2_1_BA68 | N78 DDR2_2_BA68 |
| IO, DDR2_1_BA69 | N79 DDR2_2_BA69 |
| IO, DDR2_1_BA70 | N80 DDR2_2_BA70 |
| IO, DDR2_1_BA71 | N81 DDR2_2_BA71 |
| IO, DDR2_1_BA72 | N82 DDR2_2_BA72 |
| IO, DDR2_1_BA73 | N83 DDR2_2_BA73 |
| IO, DDR2_1_BA74 | N84 DDR2_2_BA74 |
| IO, DDR2_1_BA75 | N85 DDR2_2_BA75 |
| IO, DDR2_1_BA76 | N86 DDR2_2_BA76 |
| IO, DDR2_1_BA77 | N87 DDR2_2_BA77 |
| IO, DDR2_1_BA78 | N88 DDR2_2_BA78 |
| IO, DDR2_1_BA79 | N89 DDR2_2_BA79 |
| IO, DDR2_1_BA80 | N90 DDR2_2_BA80 |
| IO, DDR2_1_BA81 | N91 DDR2_2_BA81 |
| IO, DDR2_1_BA82 | N92 DDR2_2_BA82 |
| IO, DDR2_1_BA83 | N93 DDR2_2_BA83 |
| IO, DDR2_1_BA84 | N94 DDR2_2_BA84 |
| IO, DDR2_1_BA85 | N95 DDR2_2_BA85 |
| IO, DDR2_1_BA86 | N96 DDR2_2_BA86 |
| IO, DDR2_1_BA87 | N97 DDR2_2_BA87 |
| IO, DDR2_1_BA88 | N98 DDR2_2_BA88 |
| IO, DDR2_1_BA89 | N99 DDR2_2_BA89 |
| IO, DDR2_1_BA90 | N100 DDR2_2_BA90 |
| IO, DDR2_1_BA91 | N101 DDR2_2_BA91 |
| IO, DDR2_1_BA92 | N102 DDR2_2_BA92 |
| IO, DDR2_1_BA93 | N103 DDR2_2_BA93 |
| IO, DDR2_1_BA94 | N104 DDR2_2_BA94 |
| IO, DDR2_1_BA95 | N105 DDR2_2_BA95 |
| IO, DDR2_1_BA96 | N106 DDR2_2_BA96 |
| IO, DDR2_1_BA97 | N107 DDR2_2_BA97 |
| IO, DDR2_1_BA98 | N108 DDR2_2_BA98 |
| IO, DDR2_1_BA99 | N109 DDR2_2_BA99 |
| IO, DDR2_1_BA100 | N110 DDR2_2_BA100 |
| IO, DDR2_1_BA101 | N111 DDR2_2_BA101 |
| IO, DDR2_1_BA102 | N112 DDR2_2_BA102 |
| IO, DDR2_1_BA103 | N113 DDR2_2_BA103 |
| IO, DDR2_1_BA104 | N114 DDR2_2_BA104 |

EP4CE40F23C8N



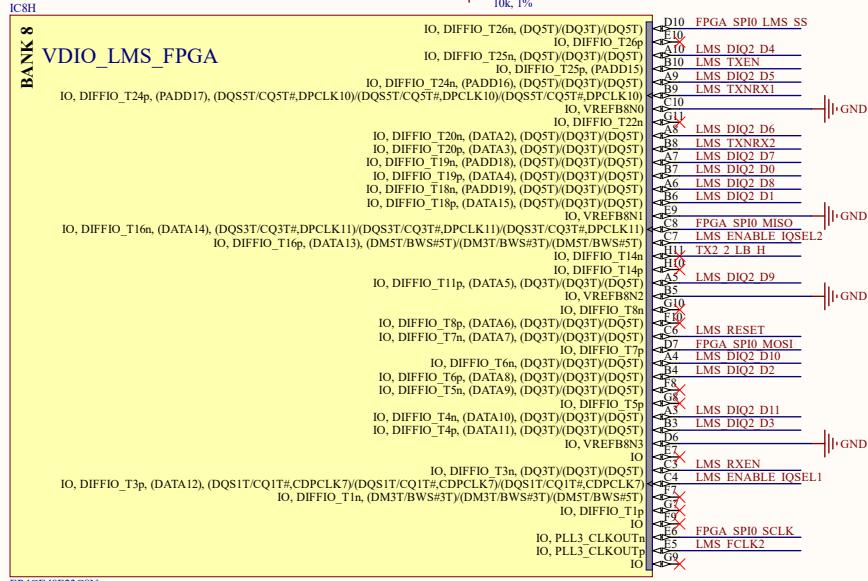
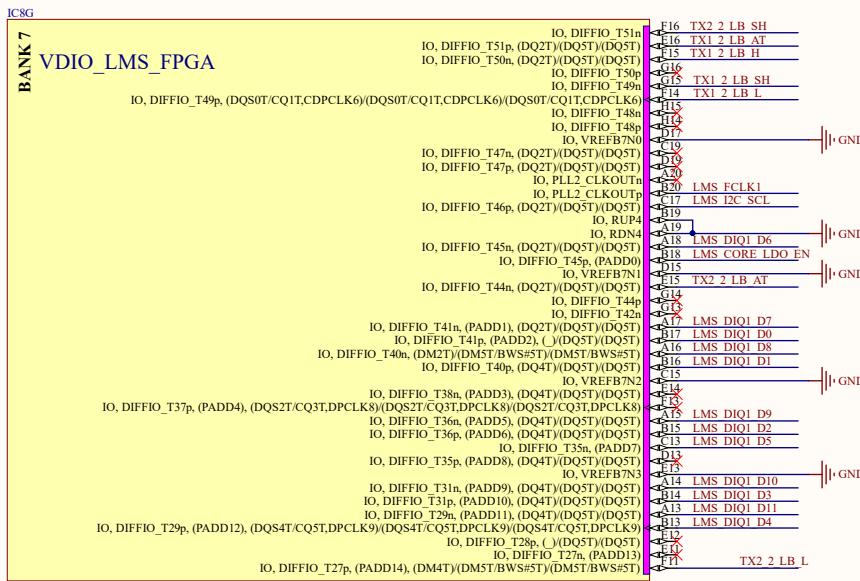
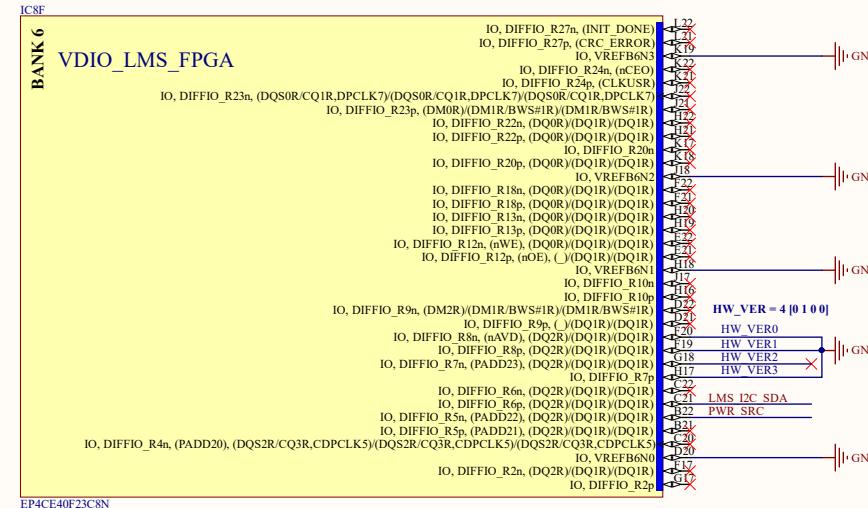
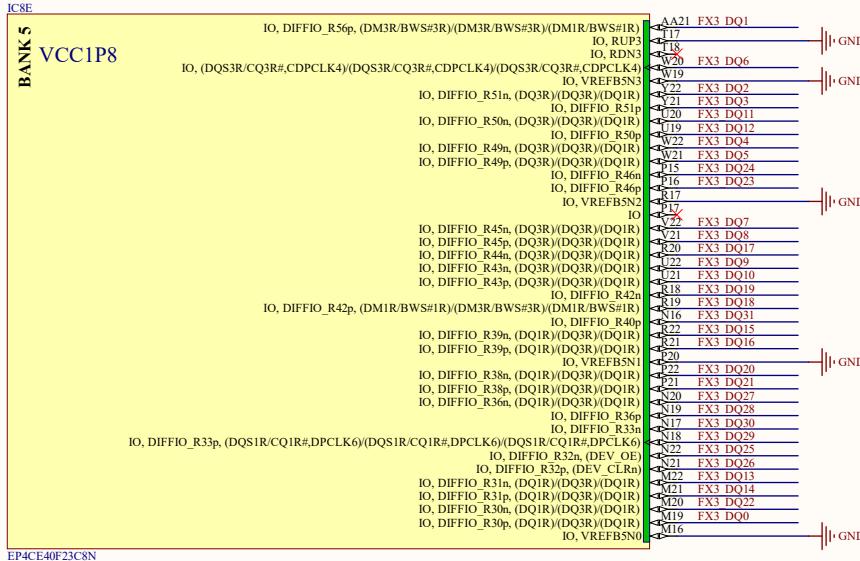
NF elements on sheet: -
Number of NF elements on sheet: 0

D
IC8D
BANK 4
VCC1P8

| | |
|-------------------------------------|-----------------|
| IO, DIFFIO_B28p, (DQ4B)(DQ5B)(DQ5B) | A13 DDR2_2_DQ14 |
| IO, DIFFIO_B28n, (DQ4B)(DQ5B)(DQ5B) | A14 DDR2_2_DQ12 |
| IO, DIFFIO_B29p, (DQ4B)(DQ5B)(DQ5B) | A14 DDR2_2_DQ11 |
| IO, DIFFIO_B29n, (DQ4B)(DQ5B)(DQ5B) | A14 DDR2_2_DQ10 |
| IO, DIFFIO_B30p, (DQ4B)(DQ5B)(DQ5B) | A15 DDR2_2_DQ13 |
| IO, DIFFIO_B30n, (DQ4B)(DQ5B)(DQ5B) | A15 DDR2_2_DQ12 |
| IO, DIFFIO_B31p, (DQ4B)(DQ5B)(DQ5B) | A15 DDR2_2_DQ11 |
| IO, DIFFIO_B31n, (DQ4B)(DQ5B)(DQ5B) | A15 DDR2_2_DQ10 |
| IO, DIFFIO_B32p, (DQ4B)(DQ5B)(DQ5B) | A16 DDR2_2_DM0 |
| IO, DIFFIO_B32n, (DQ4B)(DQ5B)(DQ5B) | A16 DDR2_2_DM0 |
| IO, DIFFIO_B33p, (DQ4B)(DQ5B)(DQ5B) | A16 DDR2_2_DM0 |
| IO, DIFFIO_B33n, (DQ4B)(DQ5B)(DQ5B) | A16 DDR2_2_DM0 |
| IO, DIFFIO_B34p, (DQ4B)(DQ5B)(DQ5B) | A16 DDR2_2_DM0 |
| IO, DIFFIO_B34n, (DQ4B)(DQ5B)(DQ5B) | A16 DDR2_2_DM0 |
| IO, DIFFIO_B35p, (DQ2B)(DQ5B)(DQ5B) | A17 DDR2_2_DM0 |
| IO, DIFFIO_B35n, (DQ2B)(DQ5B)(DQ5B) | A17 DDR2_2_DM0 |
| IO, DIFFIO_B36p, (DQ2B)(DQ5B)(DQ5B) | A17 DDR2_2_DM0 |
| IO, DIFFIO_B36n, (DQ2B)(DQ5B)(DQ5B) | A17 DDR2_2_DM0 |
| IO, DIFFIO_B37p, (| |

NF elements on sheet: R49
Number of NF elements on

FPGA banks 5, 6, 7, 8



Project name: **LimeSDR-USB_Iv4s.PjrPcb**
 Title: **FPGA banks 5, 6, 7, 8**
 Size: A3 Revision: v1.4s
 Date: 10/7/2016 Time: 1:14:39 PM Sheet 9 of 15
9 FPGA banks 5, 6, 7, 8 SchDoc

1

2

3

4

5

6

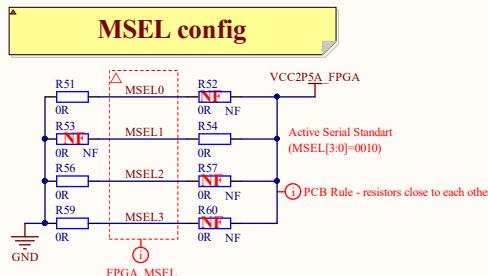
7

8

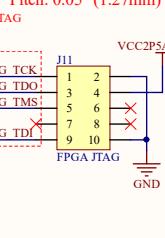
FPGA misc (power, clocks, config)

MSEL config

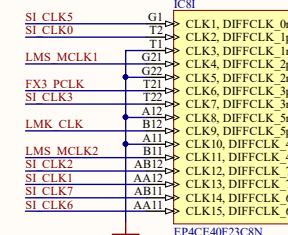
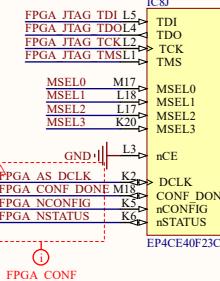
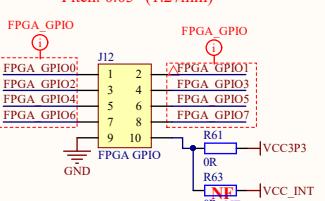
NF elements on sheet: R52, R53, R57, R60, R63, R65, R67, R72, J13, C142
Number of NF elements on sheet: 10



Pitch: 0.05" (1.27mm)

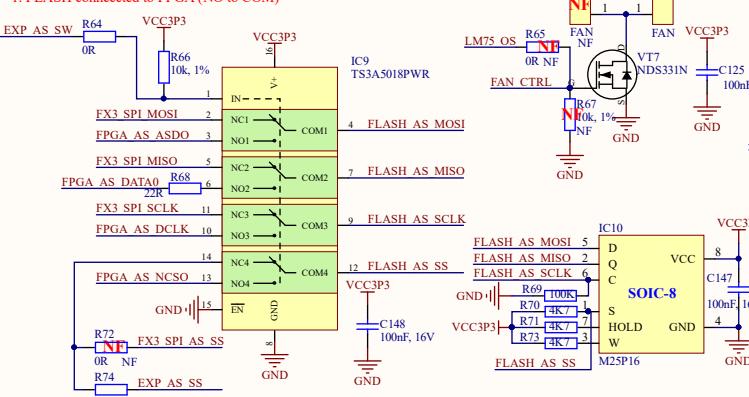


Pitch: 0.05" (1.27mm)



FPGA AS FLASH + Switch

IN:
0: FLASH connected to FX3 (NC to COM)
1: FLASH connected to FPGA (NO to COM)



IC8L

L10

GND

GND

C16

A22

E20

GND

GND

M10

GND

GND

C20

GND

GND

L20

GND

GND

L12

GND

GND

L13

GND

GND

M12

GND

GND

V20

GND

GND

Y20

GND

GND

N11

GND

GND

AB22

GND

GND

K1

GND

GND

Y18

GND

GND

N12

GND

GND

K12

GND

GND

Y12

GND

GND

N13

GND

GND

Y9

GND

GND

K10

GND

GND

AB1

GND

N3

GND

U3

GND

H2

GND

W3

GND

D3

GND

J15

GND

GND

K3

GND

L15

GND

GND

N15

GND

AA2

GND

R13

GND

H3

GND

R9

GND

R3

GND

AB6

GND

A1

GND

C5

GND

T20

GND

C9

GND

J19

GND

C11

GND

C12

GND

C14

GND

D8

GND

GND

EP4CE40F23C8N

GND

GND

C18

GND

GND

C207

GND

C208

GND

C209

GND

C210

GND

C211

GND

C212

GND

C213

GND

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GND

C217

GND

C218

GND

C219

GND

C220

GND

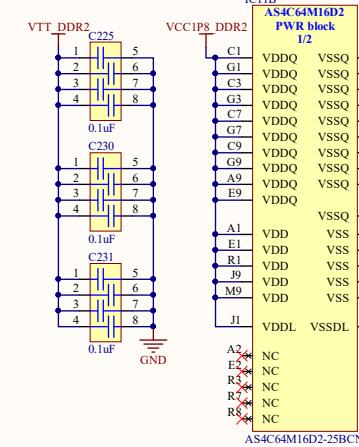
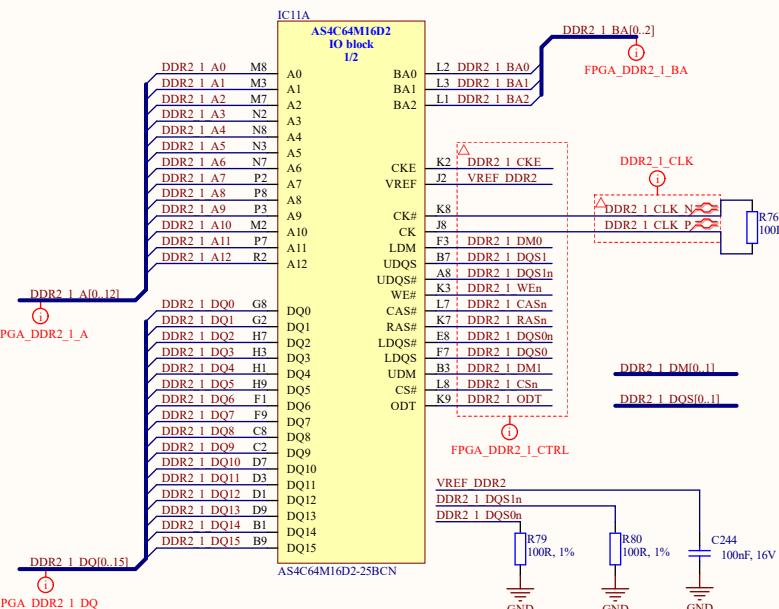
FPGA Bulk caps

Project name: LimesDR-USB_Iv4s.PjxPcb

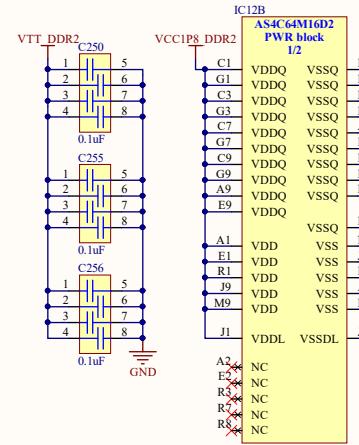
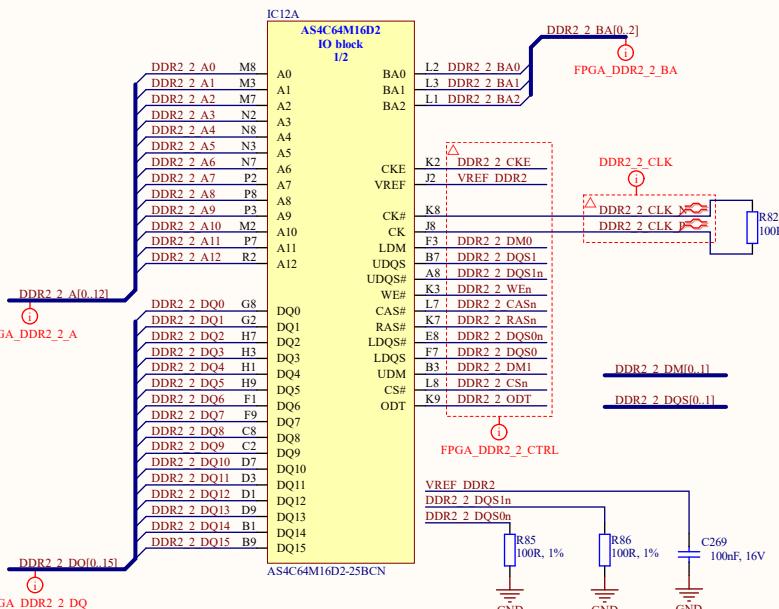
Title: **FPGA misc (power, clocks, config)**Title: **LimesDR-USB_Iv4s.PjxPcb**Title: **FPGA misc**

NF elements on sheet: -
Number of NF elements on sheet: 0

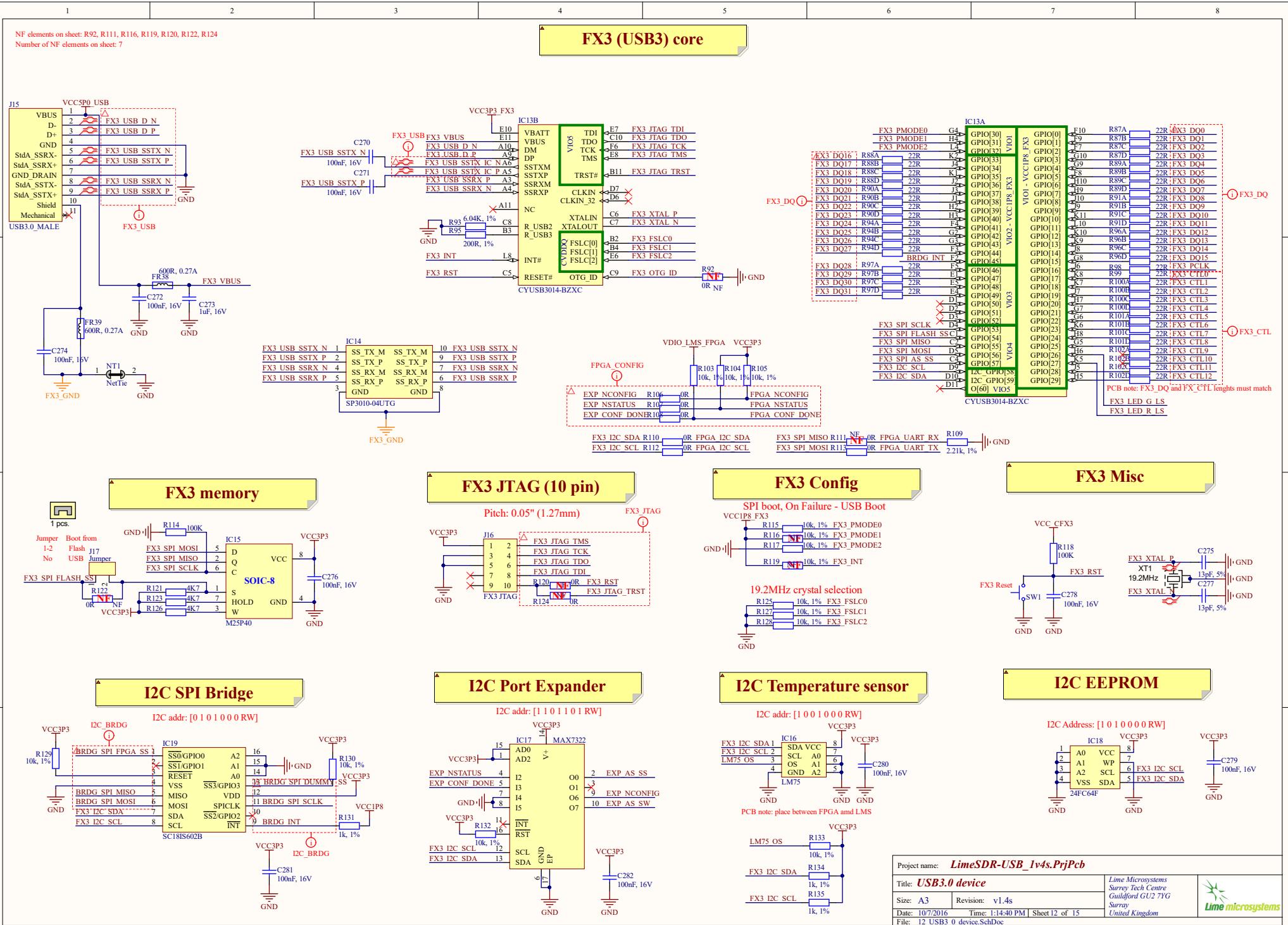
DDR2_1 (BOT L)



DDR2_2 (BOT R)



| | | |
|---------------------------------------|-------------------|---|
| Project name: LimeSDR-USB_Iv4s.PrbPcb | | Lime Microsystems |
| Title: RAM DDR2 | Lime Microsystems | |
| Size: A3 | Revision: v1.4s | Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom |
| Date: 10/7/2016 | Time: 1:14:39 PM | Sheet 11 of 15 |
| File: 11_DDR2.SchDoc | | Lime Microsystems |



1

2

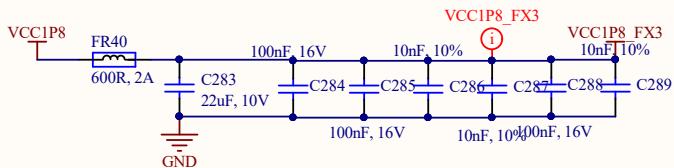
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4

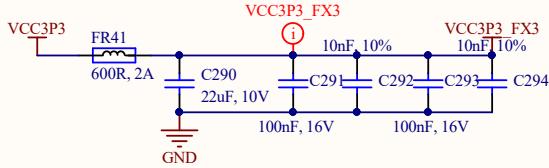
USB3 power

NF elements on sheet: FR42, FR43
Number of NF elements on sheet: 2

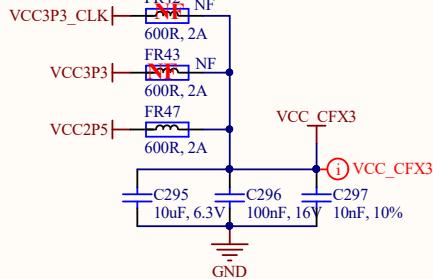
A



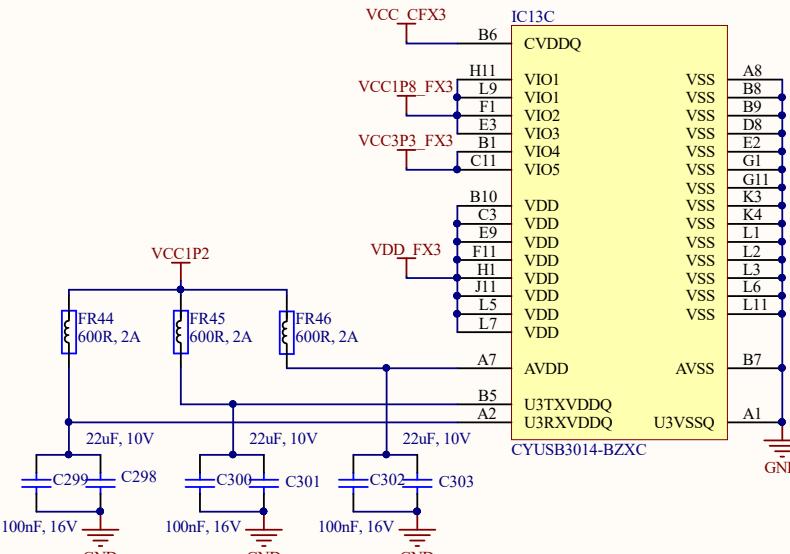
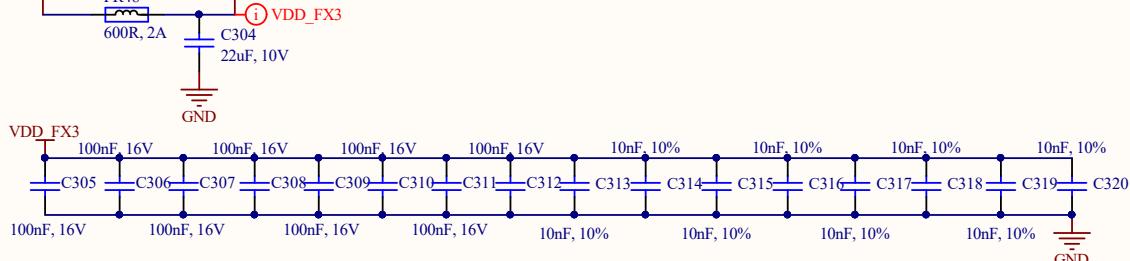
B



C



D



Project name: LimeSDR-USB_1v4s.PrtPcb

Title: USB3.0 power

Size: A4 Revision: v1.4s

Date: 10/7/2016 Time: 1:14:40 PM Sheet 13 of 15

File: 13_USB3_0_power.SchDoc

Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom



1

2

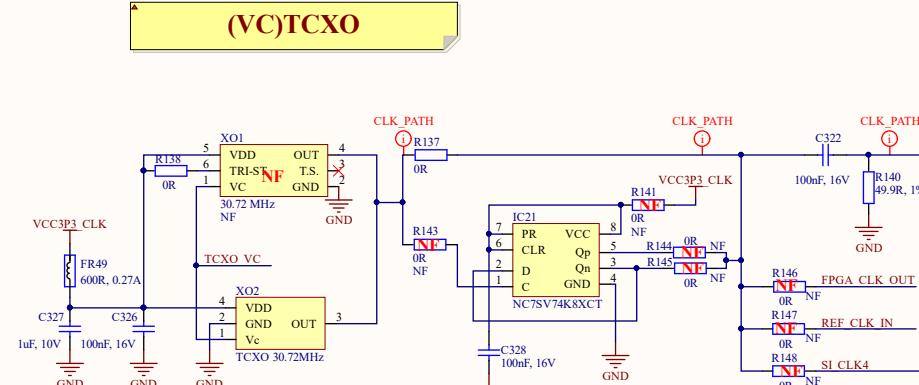
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4

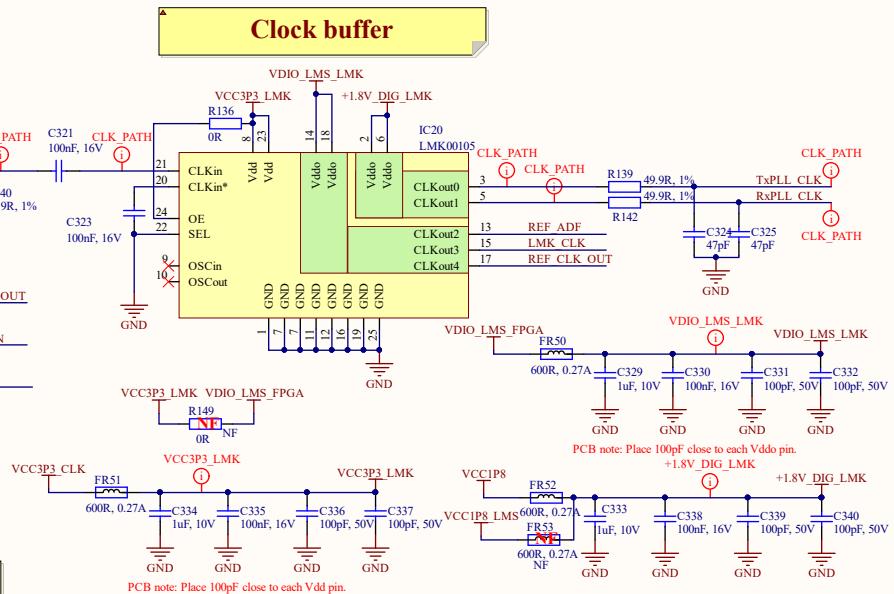
NF elements on sheet: XO1, R141, R143, R144, R145, R146, R147, R148, R149, R151, R155, C341, FR53
 Number of NF elements on sheet: 13

Clock circuits

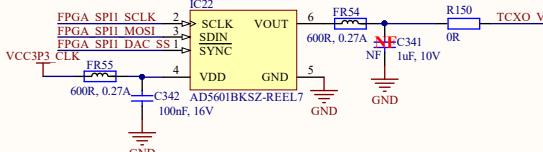
(VC)TCXO



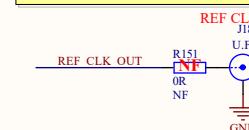
Clock buffer



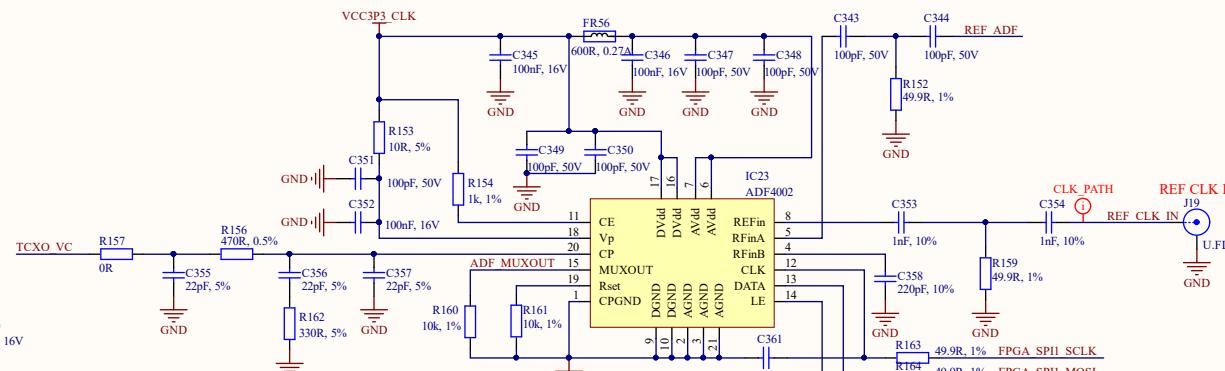
TCXO DAC



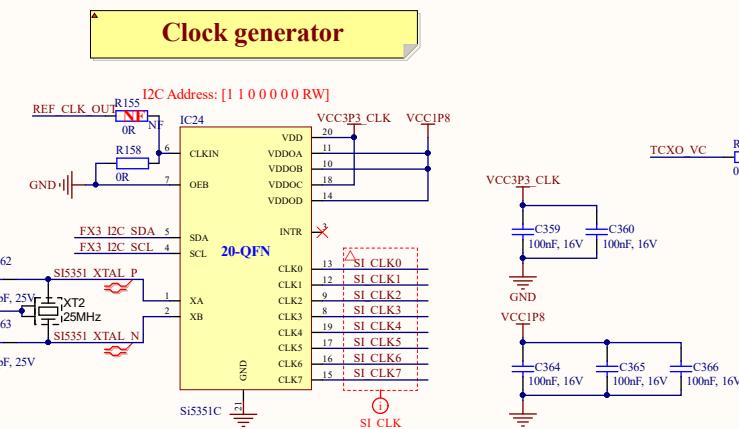
REF CLK OUT



Phase detector



Clock generator



Project name: LimeSDR-USB_Iv4s.PjrPcb

Title: Clocks

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 Guildford GU2 7YG
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 United Kingdom



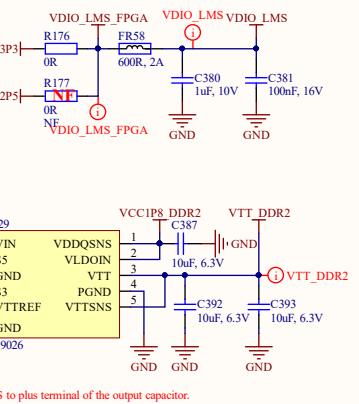
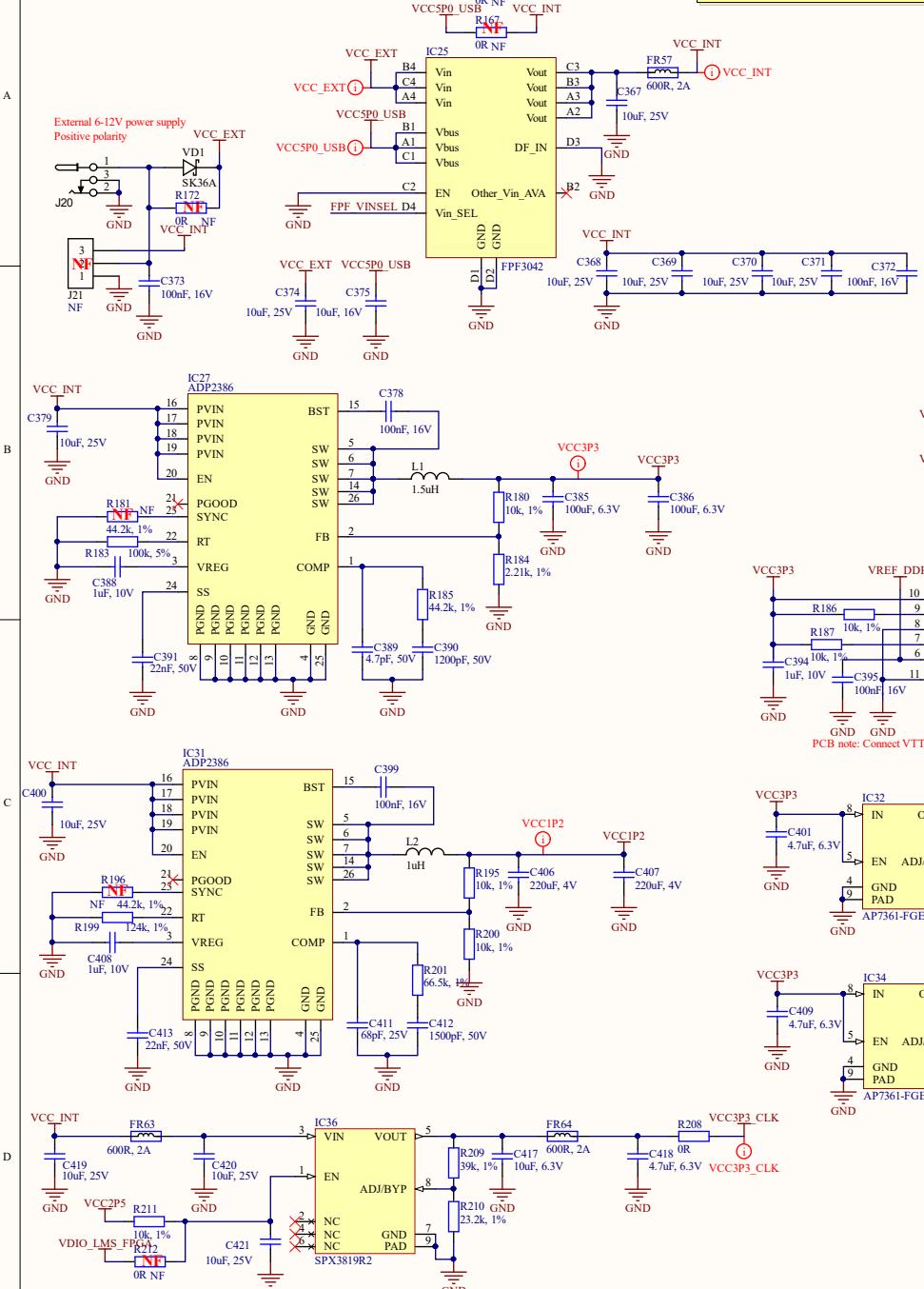
Size: A3 Revision: v1.4s

Date: 10/7/2016 Time: 1:14:40 PM Sheet 14 of 15

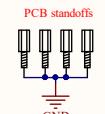
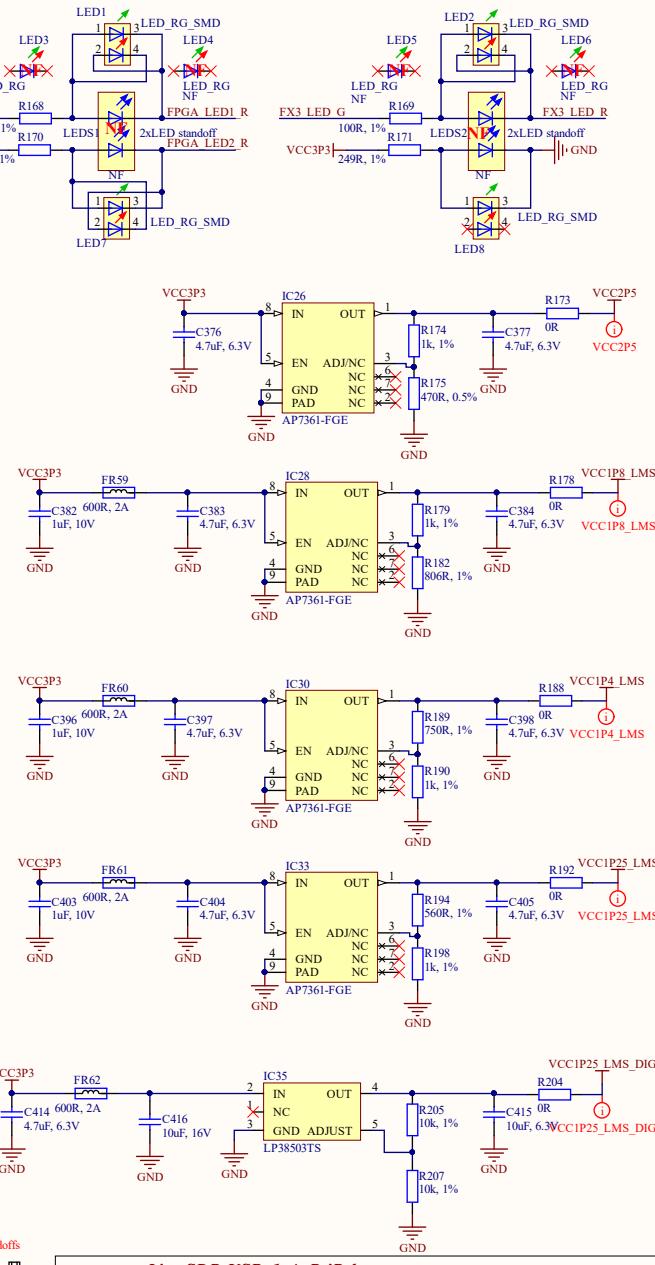
File: 14_Clocks.SchDoc



Board power circuits



*CB note: Connect VTT/SNS to plus terminal of the output capacitor.



| | | | |
|---------------|--------------------------------|--|--|
| Project name: | LimeSDR-USB_Iv4s.PrtPcb | | |
| Title: | Board power supply | Lime Microsystems Survey Tech Centre Guildford GU2 7YG Survey United Kingdom |  Lime microsystems |
| Size: | A3 | Revision: v1.4s | |
| Date: | 10/7/2016 | Time: 1:14:40 PM | Sheet 15 of 15 |