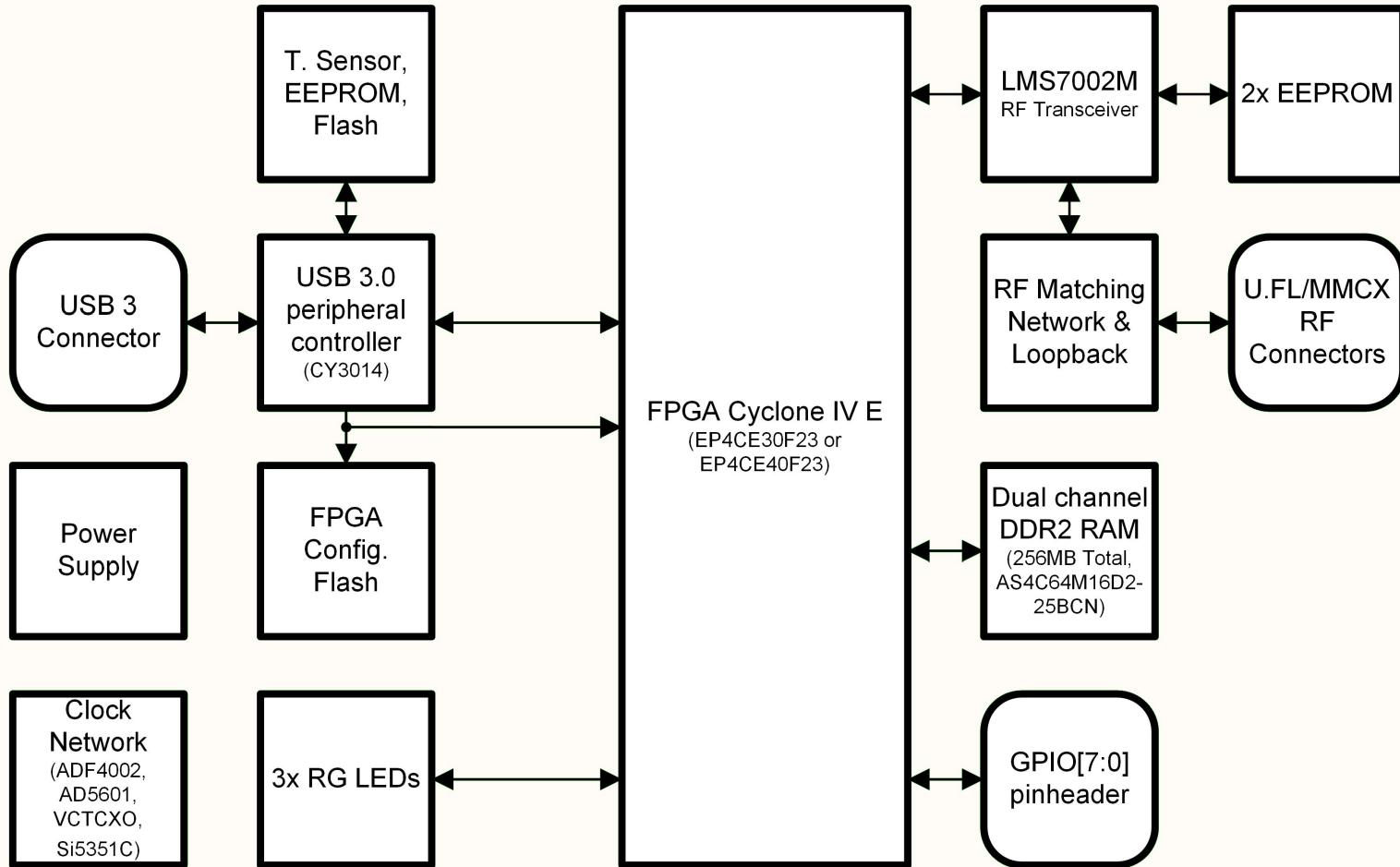


Block diagram



Project name: *LimeSDR-USB_1v4.PrjPcb*

Title: *Block diagram*

Size: A4 Revision: v1.4

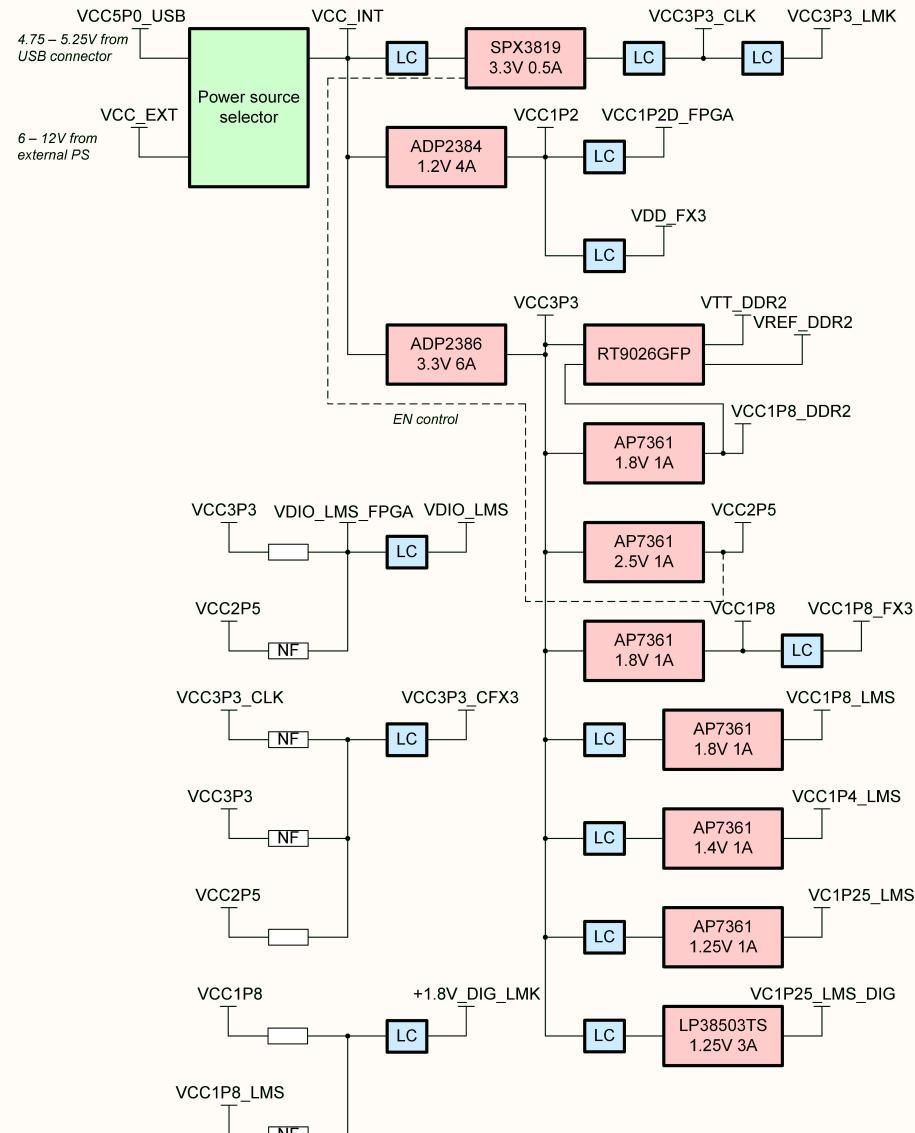
Date: 10/7/2016 Time: 1:08:45 PM Sheet 1 of 15

File: 01_BlockDiagram.SchDoc

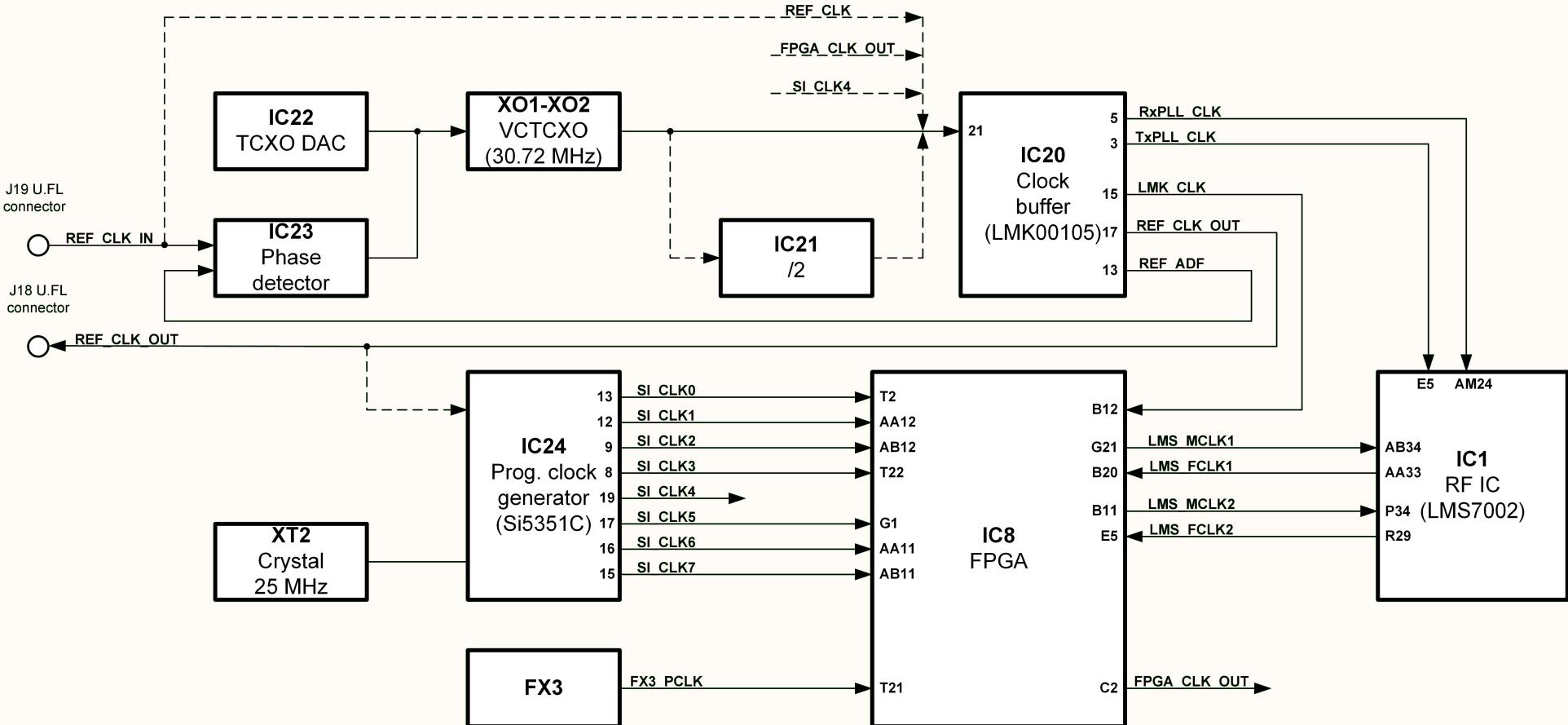
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Guildford GU2 7YG
Surrey
United Kingdom



Power diagram



Clock diagram



Project name: *LimeSDR-USB_Iv4.PnjPcb*

Title: *Clock diagram*

Size: **A4** Revision: **v1.4**

Date: **10/7/2016** Time: **1:08:47 PM** Sheet **3** of **15**

File: **03_ClockDiagram.SchDoc**

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Surrey
United Kingdom



NF elements on sheet: -
Number of NF elements on sheet: 0

LMS7002M misc

A

A

B

B

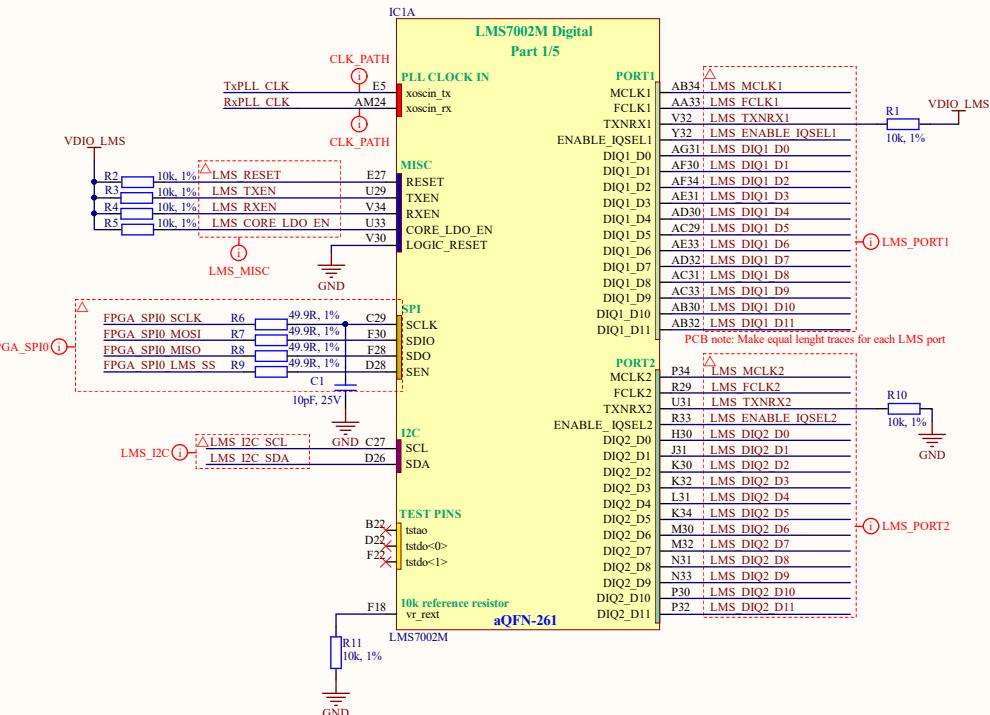
C

C

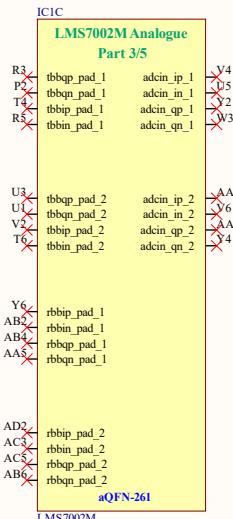
D

D

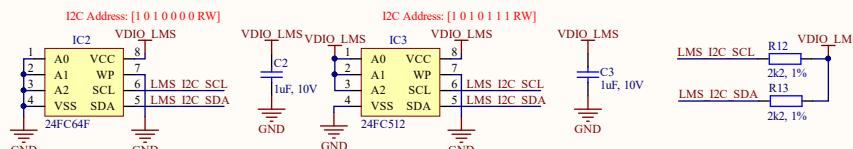
Digital interfaces



Baseband external IO



LMS EEPROMS



Project name: LimeSDR-USB_Iv4.PrbPcb

Title: LMS7002M misc

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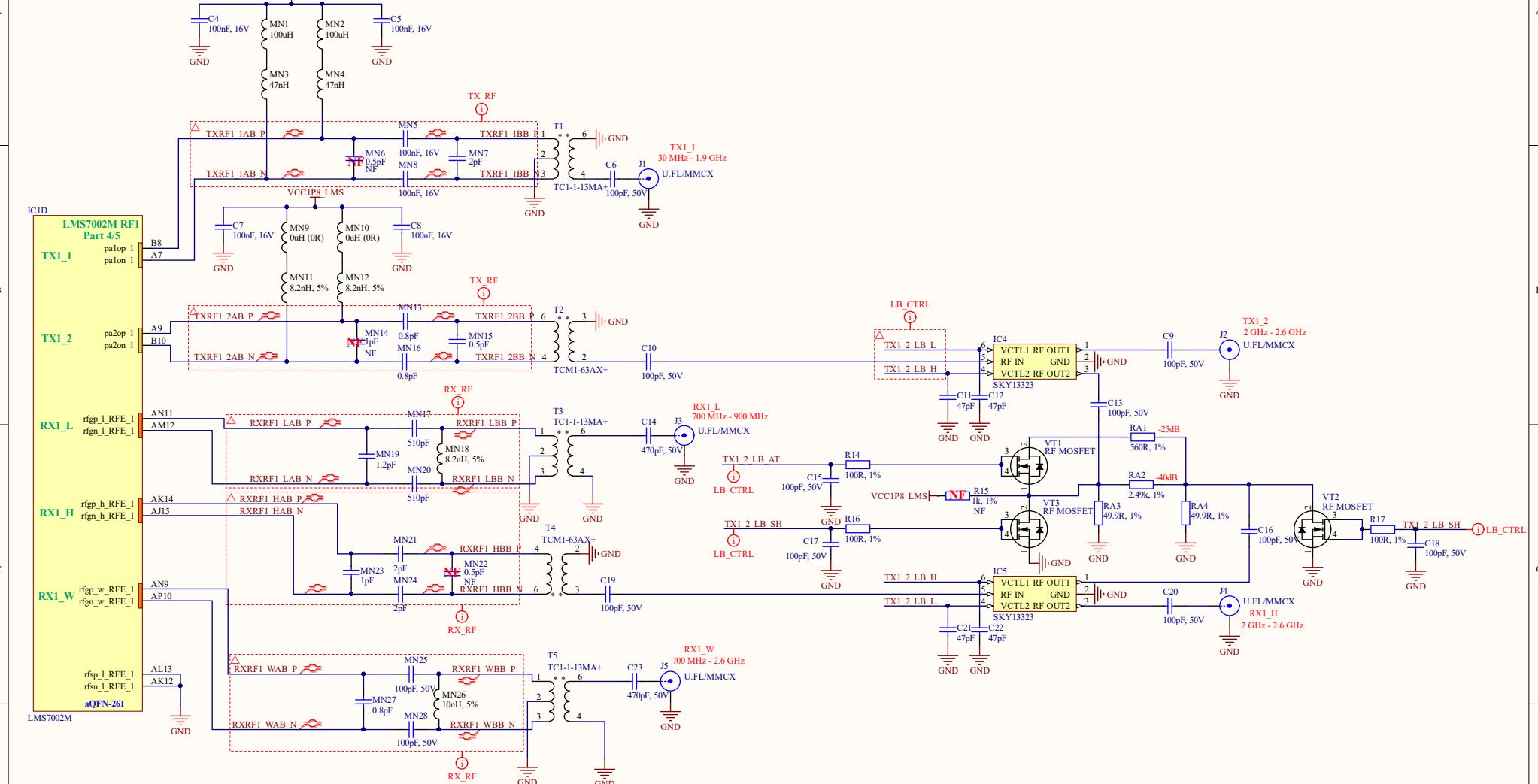


Size: A3 Revision: v1.4
Date: 10/7/2016 Time: 1:08:47 PM Sheet 4 of 15
File: 04_LMS7002M_Misc.SchDoc

NF elements on sheet: MN6, MN14, MN22, R15

Number of NF elements on sheet: 4

LMS7002M RF1 circuits



Project name: LimeSDR-USB_Iv4.PrbPcb

Title: LMS7002M RF

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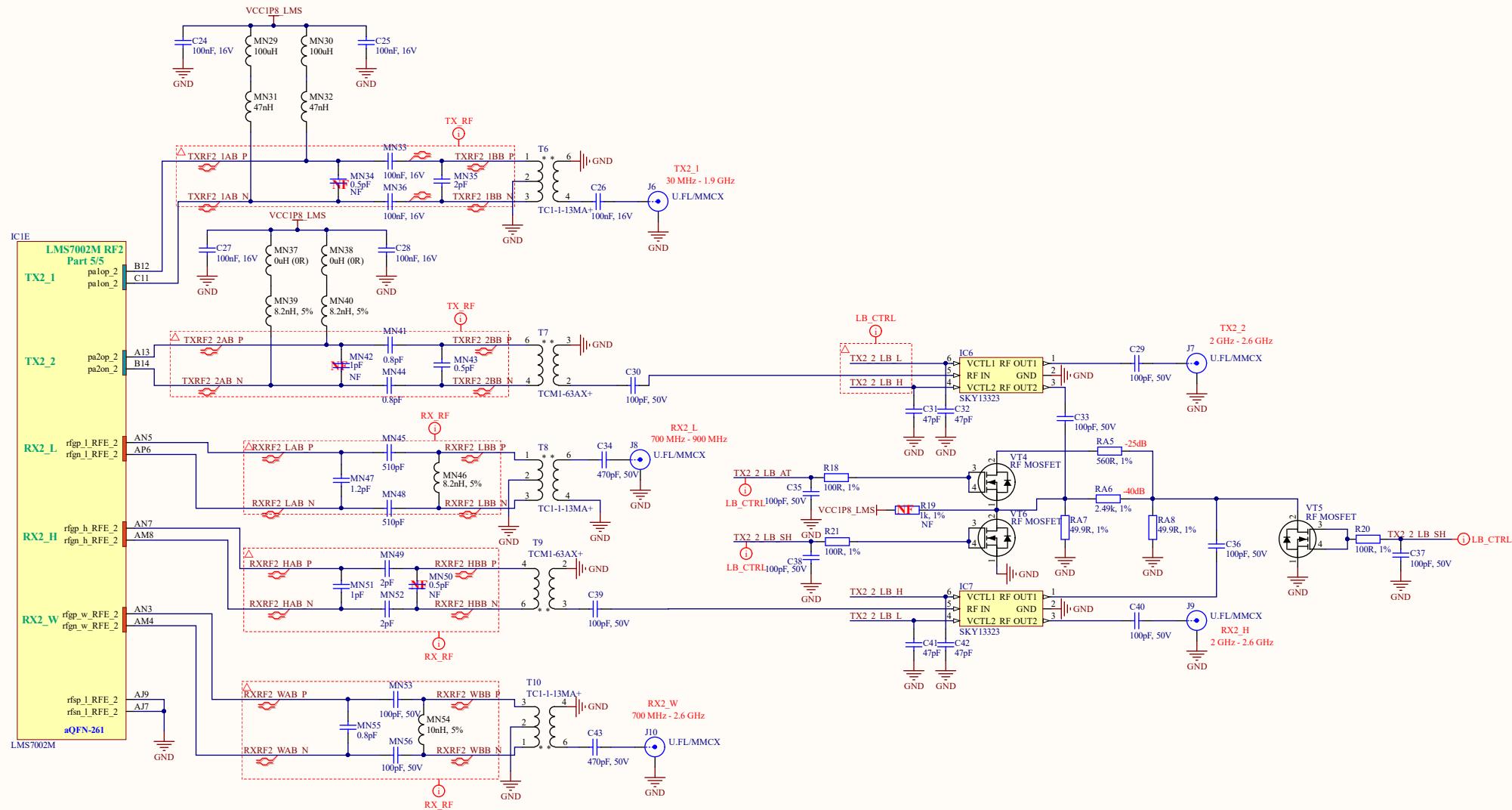
Size: A3 Revision: v1.4

Date: 10/7/2016 Time: 1:08:47 PM Sheet 5 of 15

File: 05_LMS7002M_RF1.SchDoc

NF elements on sheet: MN34, MN42, MN50, R19
Number of NF elements on sheet: 4

LMS7002M RF2 circuits



Project name: LimeSDR-USB_Iv4.PrbPcb

Title: LMS7002M RF

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Size: A3

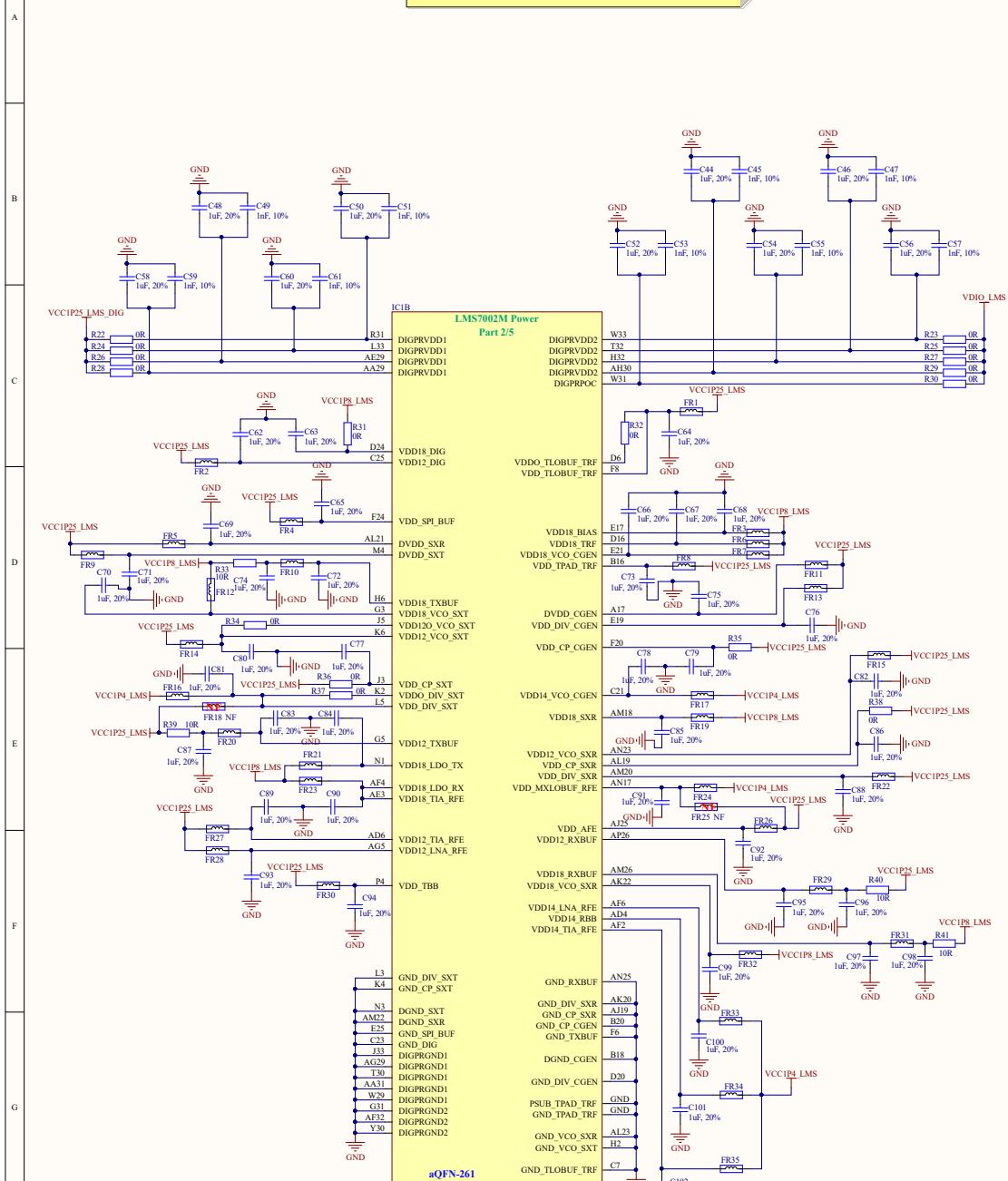
Revision: v1.4

Date: 10/7/2016 Time: 1:08:48 PM Sheet 6 of 15

File: 06_LMS7002M_RF2.SchDoc

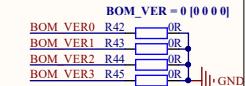
NF elements on sheet: FR18, FR25
Number of NF elements on sheet: 2

LMS7002M power supply circuit



FPGA banks 1, 2, 3, 4

NF elements on sheet: -
Number of NF elements on sheet: 0



A
IC8A
BANK 1
VCC3P3

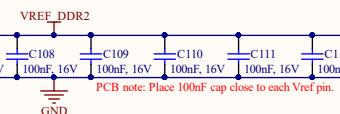
IO, DIFFIO_L1p, (DQ1L)(DQ1L)(DQ1L)	G4 FPGA GPIO4
IO, DIFFIO_L1n, (DQ1L)(DQ1L)(DQ1L)	B23 FPGA GPIO5
IO, DIFFIO_L2p, (DQ2L)(DQ1L)(DQ1L)	B22 BRDG SPI SCLK
IO, DIFFIO_L2n, (DQ2L)(DQ1L)(DQ1L)	B21 BRDG SPI MOSI
IO, VREFB1N0	G5 FX3 LED G
IO, DIFFIO_L4p, (nRESET), (DQ2L)(DQ1L)(DQ1L)	I4 FAN CTRL
IO, DIFFIO_L4n, (DQ2L)(DQ1L)(DQ1L)	I5 FPGA LED1 R
IO, DIFFIO_L5p, (DQ3L)(CDPCLK0)(DQS2L)(CQ3L,CDPCLK0)	C2 FPGA CLK OUT
IO, DIFFIO_L5n, (DQ3L)(CDPCLK0)(DQS2L)(CQ3L,CDPCLK0)	C1 BRDG SPI MISO
IO, DIFFIO_L7p, (DQ1L)(DQ1L)(DQ1L)	D2 FPGA LED1 G
IO, DIFFIO_L8p, (DQ1L)(DQ1L)(DQ1L)	D1 FPGA AS ASDO
IO, DIFFIO_L8n, (DATA1,ASDO)	I7 FPGA I2C SCL
IO, VREFB1N1	I6 FPGA GPIO1
IO, DIFFIO_L9p, (DQ2L)(DQ1L)(DQ1L)	L75 OS
IO, DIFFIO_L9n, (DQ2L)(DQ1L)(DQ1L)	E2 FPGA AS NCSD
IO, DIFFIO_L10p, (FLASH_nCE,CS0)	E1 BRDG SPI MOSI
IO, DIFFIO_L10n, () (DQ1L)(DQ1L)	D2 FPGA LED1 G
IO, DIFFIO_L12p, (DM2L)(DM1L/BWS#1L)(DM1L/BWS#1L)	D1 FPGA AS ASDO
IO, DIFFIO_L12n, (DQ0L)(DQ1L)(DQ1L)	I7 FPGA I2C SCL
IO, DIFFIO_L14p, (DQ1L)(DQ1L)(DQ1L)	I6 FPGA GPIO1
IO, DIFFIO_L14n, (DQ1L)(DQ1L)(DQ1L)	I5 FX3 LED R
IO, VREFB1N2	I8 FPGA SPII ADF_SS
IO, DIFFIO_L15p, (DQ1L)(DQ1L)(DQ1L)	I7 FPGA SPII DAC_SS
IO, DIFFIO_L15n, (DQ1L)(DQ1L)(DQ1L)	I6 FX3 LED G LS
IO, DIFFIO_L16p, (DQ1L)(DQ1L)(DQ1L)	P1 BOM VER0
IO, DIFFIO_L16n, (DQ1L)(DQ1L)(DQ1L)	P2 BOM VER1
IO, DIFFIO_L18p, (DQ1L)(DQ1L)(DQ1L)	R1 BRDG INT
IO, DIFFIO_L18n, (DQ1L)(DQ1L)(DQ1L)	R2 FX3 CTL11
IO, VREFB1N3	I7 FX3 CTL0
IO, DIFFIO_L19p, (DQ1L)(DQ1L)(DQ1L)	M6 FX3 CTL6
IO, DIFFIO_L19n, (DQ1L)(DQ1L)(DQ1L)	M1 FX3 CTL2
IO, DIFFIO_L20p, (DQ1L)(DQ1L)(DQ1L)	M4 FX3 CTL5
IO, DIFFIO_L20n, (DQ1L)(DQ1L)(DQ1L)	M3 FX3 CTL4
IO, DIFFIO_L21p, (DQ1L)(DQ1L)(DQ1L)	N2 FX3 CTL10
IO, DIFFIO_L21n, (DQ1L)(DQ1L)(DQ1L)	N1 FX3 CTL9
IO, DIFFIO_L24p, (DQ0L)(DQ1L)(DQ1L)	I7 FX3 CTL1
IO, DIFFIO_L24n, (DQ0L)(DQ1L)(DQ1L)	M5 VREF DDR2
IO, DATA0	I2 FX3 LED G LS

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B
IC8C
BANK 3
VCC1P8

IO, DIFFIO_B1p, (DM3B/BWS#3B)(DM3B/BWS#3B)(DM3B/BWS#5B)	V6 DDR2_1_A3
IO, DIFFIO_B3p, (DQ3L)(CQ1B#,CDPCLK2)(DQS1B/CQ1B#,CDPCLK2)	V5 DDR2_1_DM1
IO, VREFB3N3	V8 DDR2_1_CLK_P
IO, VREFB3N4	V8 DDR2_1_CLK_N
IO, DIFFIO_B4p, (DQ3B)(DQ3B)(DQ5B)	VREF DDR2
IO, PLL_CKOUTTr	V3 DDR2_1_A2
IO, PLL_CKOUTTr	V6 DDR2_1_A10
IO, PLL_CKOUTTr	V6 DDR2_1_DQ8
IO, DIFFIO_B7p, (DQ3B)(DQ3B)(DQ5B)	V7 DDR2_1_A9
IO, DIFFIO_B7n, (DQ3B)(DQ3B)(DQ5B)	V4A4 DDR2_1_D015
IO, VREFB3N2	V4A5 DDR2_1_D09
IO, DIFFIO_B8p, (DQ3B)(DQ3B)(DQ5B)	V4B5 DDR2_1_A7
IO, DIFFIO_B8n, (DQ3B)(DQ3B)(DQ5B)	V4B2 DDR2_1_A12
IO, DIFFIO_B11p, (DQ3B)(DQ3B)(DQ5B)	V7 DDR2_1_DQ10
IO, DIFFIO_B11n, (DQ3B)(DQ3B)(DQ5B)	V7 DDR2_1_DQ13
IO, DIFFIO_B12p, (DQ3B)(DQ3B)(DQ5B)	V9 DDR2_1_DQ14
IO, DIFFIO_B12n, (DQ3B)(DQ3B)(DQ5B)	V8 DDR2_1_DQ12
IO, DIFFIO_B13p, (DQ3B)(DQ3B)(DQ5B)	V7 DDR2_1_DQ11
IO, DIFFIO_B13n, (DQ3B)(DQ3B)(DQ5B)	V7 DDR2_1_DQ07
IO, DIFFIO_B14p, (DMS5B/BWS#5B)(DM3B/BWS#3B)(DM3B/BWS#5B)	V7 DDR2_1_D007
IO, DIFFIO_B14n, (DQ5B)(DQ3B)(DQ5B)	V8 DDR2_2_C5n
IO, DIFFIO_B15p, (DQ5B)(DQ3B)(DQ5B)	V10 DDR2_2_CASn
IO, DIFFIO_B15n, (DQ5B)(DQ3B)(DQ5B)	V11 DDR2_2_RASn
IO, VREFB3N1	VREF DDR2
IO, DIFFIO_B16p, (DQS3B/CQ3B#,DPCLK2)(DQS3B/CQ3B#,DPCLK2)	V10 DDR2_1_D051
IO, DIFFIO_B16n, (DQS3B/CQ3B#,DPCLK2)	V10 DDR2_1_D000
IO, DIFFIO_B18p, (DQS3B/CQ3B#,DPCLK2)	A8A8 DDR2_1_D06
IO, DIFFIO_B18n, (DQS3B/CQ3B#,DPCLK2)	A8B8 DDR2_1_D01
IO, DIFFIO_B21p, (DQ5B)(DQ3B)(DQ5B)	A9A9 DDR2_1_D03
IO, DIFFIO_B21n, (DQS5B/CQ5B#,DPCLK3)(DQS5B/CQ5B#,DPCLK3)	A9B9 DDR2_1_D050
IO, VREFB3N0	V11 DDR2_1_D04
IO, DIFFIO_B25n, (DQ5B)(DQ3B)(DQ5B)	W10 DDR2_1_D05
IO, DIFFIO_B26n, (DQ5B)(DQ3B)(DQ5B)	Y10 DDR2_1_D07
IO, DIFFIO_B27p, (DM4B)(DM5B/BWS#5B)(DM5B/BWS#5B)	A10A10 DDR2_2_DM1
IO, DIFFIO_B27n, () (DQ5B)(DQ5B)	A10B10 DDR2_2_CKE

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C
IC8D
BANK 4
VCC1P8

IO, DIFFIO_B28p, (DQ4B)(DQ5B)(DQ5B)	AA13 DDR2_2_DQ14
IO, DIFFIO_B28n, (DQ4B)(DQ5B)(DQ5B)	AA14 DDR2_2_DQ12
IO, DIFFIO_B29p, (DQ4B)(DQ5B)(DQ5B)	AA14 DDR2_2_DQ11
IO, DIFFIO_B29n, (DQ4B)(DQ5B)(DQ5B)	V12
IO, VREFB2N1	W13 DDR2_2_D08
IO, DIFFIO_L41p, (DQ3L)(CQ1L#,DPCLK1)(DQS1L/CQ1L#,DPCLK1)	Y13 DDR2_2_D051
IO, DDR2_1_BA0	AA15 DDR2_2_D010
IO, RDN1	U12 DDR2_2_D015
IO, DDR2_1_BA1	AA16 DDR2_2_DM0
IO, DDR2_1_BA2	T12 DDR2_2_ODT
IO, DDR2_1_BA3	V13 DDR2_2_BA1
IO, DDR2_1_BA4	W14 DDR2_2_D050
IO, DDR2_1_BA5	V15 DDR2_2_D07
IO, DDR2_1_BA6	W15 DDR2_2_BA0
IO, DDR2_1_BA7	Y14 DDR2_2_D01
IO, DDR2_1_BA8	Y15 DDR2_2_D01
IO, DDR2_1_BA9	Y16 DDR2_2_D05
IO, DDR2_1_BA10	V17 DDR2_2_BA0
IO, DDR2_1_BA11	V18 DDR2_2_D051
IO, DDR2_1_BA12	V19 DDR2_2_D050
IO, DDR2_1_BA13	V20 DDR2_2_D051
IO, DDR2_1_BA14	V21 DDR2_2_D050
IO, DDR2_1_BA15	V22 DDR2_2_D051
IO, DDR2_1_BA16	V23 DDR2_2_D050
IO, DDR2_1_BA17	V24 DDR2_2_D051
IO, DDR2_1_BA18	V25 DDR2_2_D050
IO, DDR2_1_BA19	V26 DDR2_2_D051
IO, RDN2	V27 DDR2_2_BA0
IO, B40n, (DQ2B)(DQ5B)(DQ5B)	W15 DDR2_2_DQ0
IO, B41n, (DQ2B)(DQ5B)(DQ5B)	Y14 DDR2_2_D04
IO, B42n, (DQ2B)(DQ5B)(DQ5B)	Y15 DDR2_2_D04
IO, B43p, (DQ2B)(DQ5B)(DQ5B)	AB18 DDR2_2_D03
IO, B44p, (DQ2B)(DQ5B)(DQ5B)	AB19 DDR2_2_A1
IO, B45p, (DQ2B)(DQ5B)(DQ5B)	AB17 DDR2_2_A10
IO, VREFB4N1	AA18 DDR2_2_A10
IO, B46p, (DQ2B)(DQ5B)(DQ5B)	AA19 DDR2_2_A11
IO, B47p, (DQ2B)(DQ5B)(DQ5B)	R46 49.9%, 1%
IO, B48n, (DQ2B)(DQ5B)(DQ5B)	W17 DDR2_2_D05
IO, B49p, () (DQ5B)(DQ5B)	Y17 DDR2_2_A3
IO, B49n, (DQ2B)(DQ5B)(DQ5B)	AA20 DDR2_2_A9
IO, B50p, (DQ5B)(DQ5B)(DQ5B)	AB20 DDR2_2_DQ2
IO, VREFB4N0	V16
IO, B50p, (DQ5B)(DQ5B)(DQ5B)	IO, DIFFIO_B50p
IO, B51p, (DQ5B)(DQ5B)(DQ5B)	U17 DDR2_2_A6
IO, PLL4_CLKOUTTr	U16 DDR2_2_A4
IO, PLL4_CLKOUTTr	K16 DDR2_2_A8
IO, DIFFIO_B52p	K14 DDR2_2_CLK_P
IO, DIFFIO_B52n	K15 DDR2_2_CLK_N

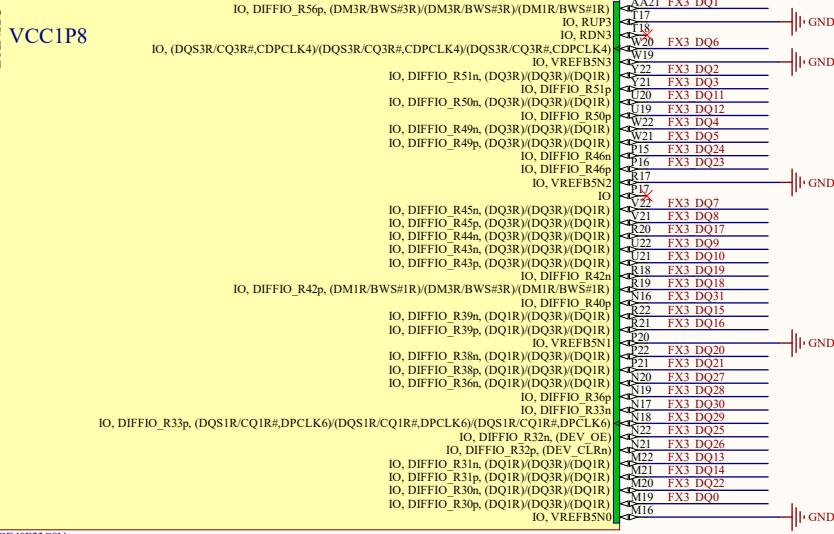
D
IC8E
BANK 4
VCC1P8

Project name: LimeSDR-USB_Iv4.PrfPcb	
Title: FPGA banks 1, 2, 3, 4	Lime Microsystems
Size: A3	Revision: v1.4
Date: 10/7/2016	Time: 1:08:48 PM
File: 08 FPGA banks 1, 2, 3, 4.SchDoc	Sheet 8 of 15 United Kingdom

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Number of NF elements on sheet: 1

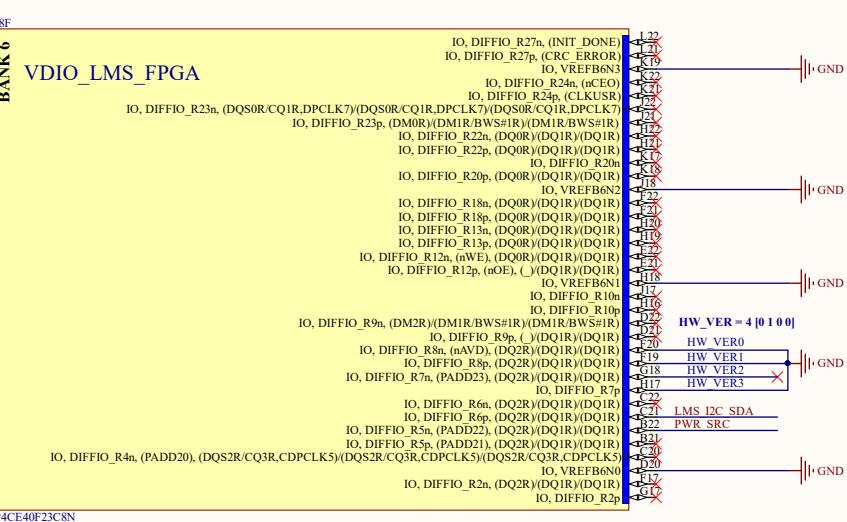
FPGA banks 5, 6, 7, 8

IC8E



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IC8F

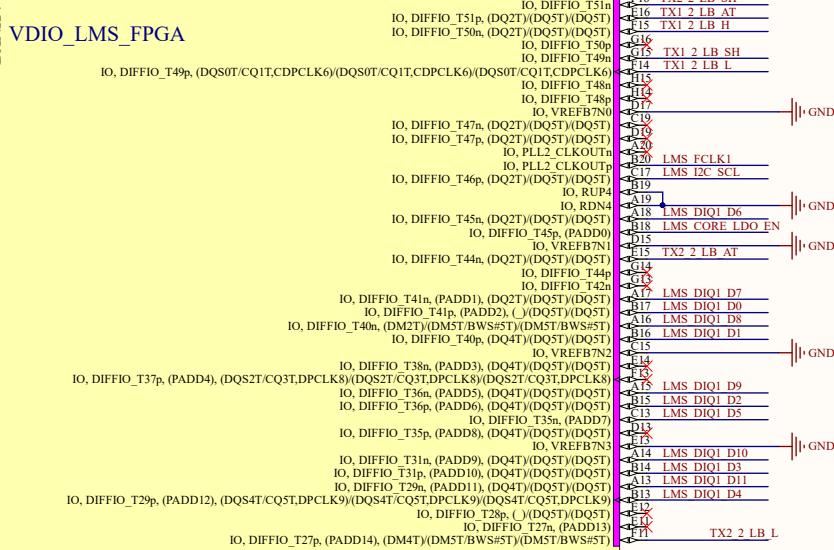


EP4CE40F23C8N

PWR_SRC status:
LOW: USB (VBUS->VOUT)
HIGH: External (VIN->VOUT)

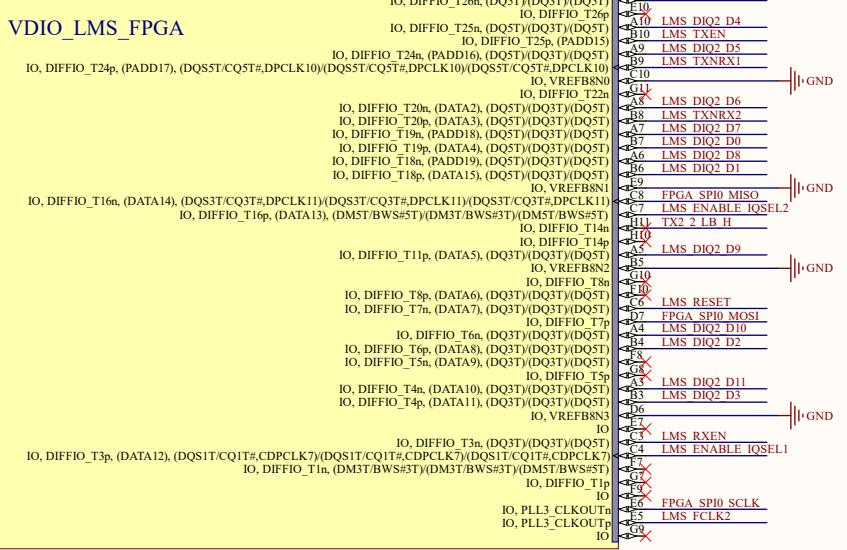


IC8G



EP4CE40F23C8N

IC8H



EP4CE40F23C8N

Project name: LimeSDR-USB_1v4.PrbPcb

Title: FPGA banks 5, 6, 7, 8

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Surrey

United Kingdom

Size: A3 Revision: v1.4

Date: 10/7/2016 Time: 1:08:48 PM Sheet 9 of 15

File: 09 FPGA banks 5_6_7_8.SchDoc



Lime

microsystems

1

2

3

4

5

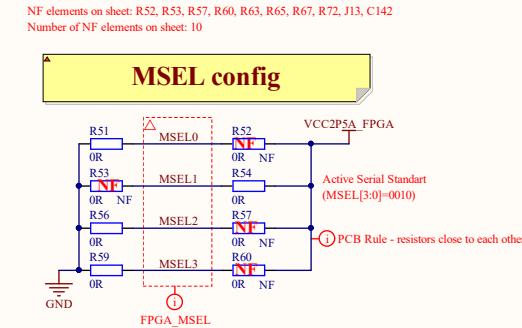
6

7

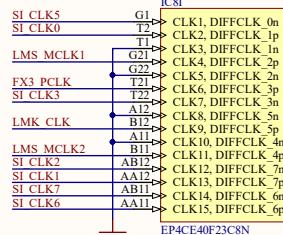
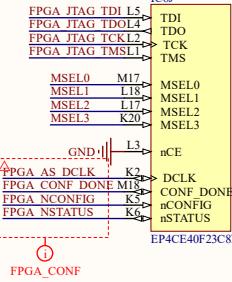
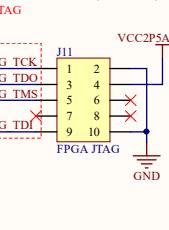
8

FPGA misc (power, clocks, config)

MSEL config

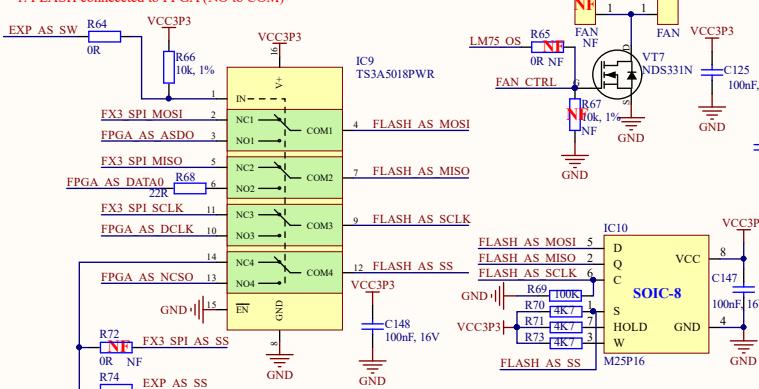


Pitch: 0.05" (1.27mm)

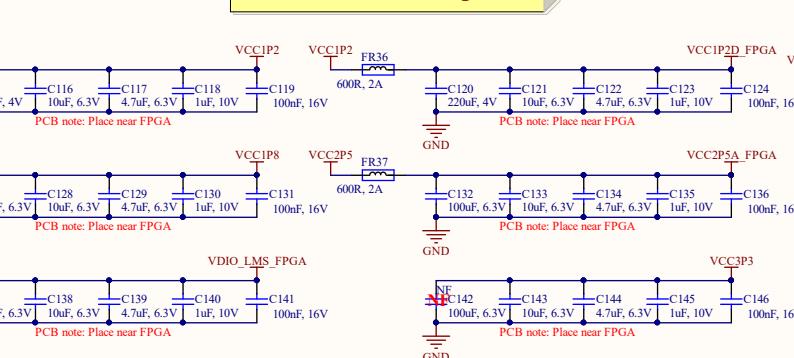


FPGA AS FLASH + Switch

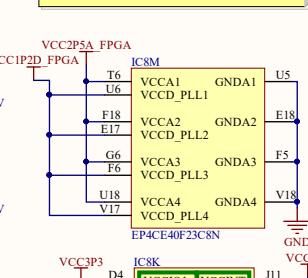
IN:
0: FLASH connected to FX3 (NC to COM)
1: FLASH connected to FPGA (NO to COM)



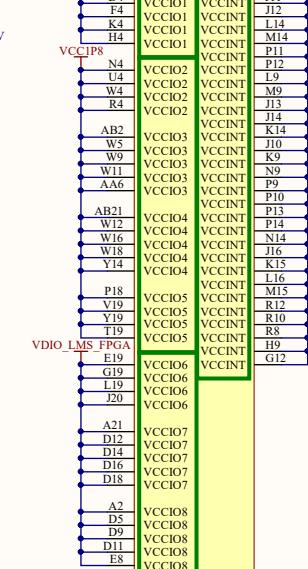
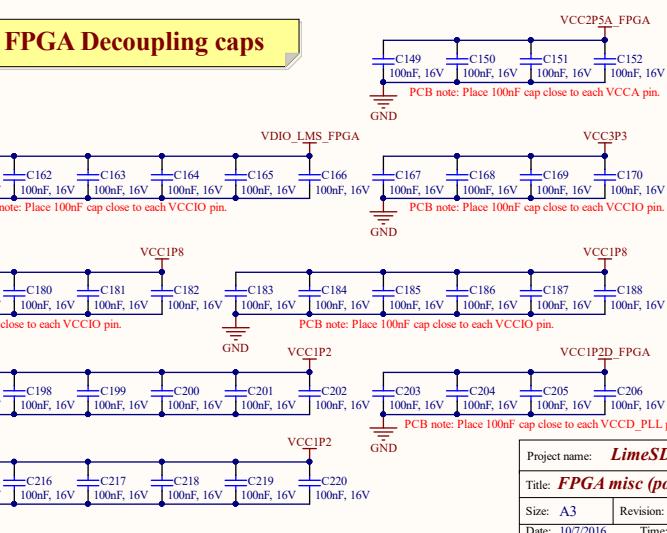
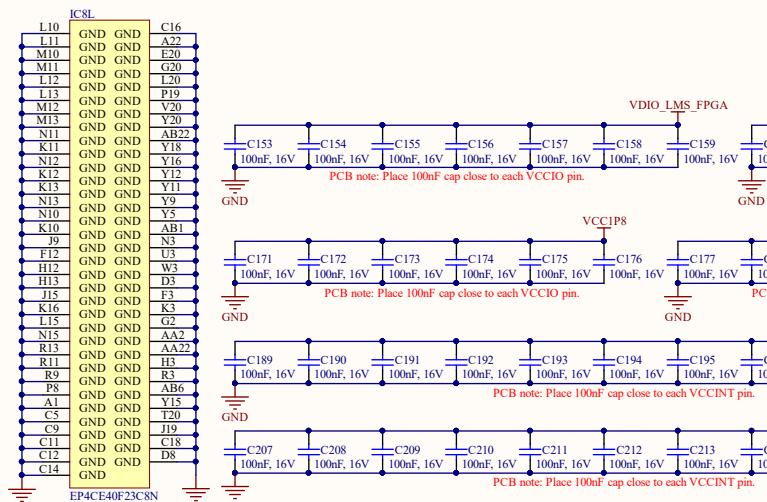
FPGA Bulk caps



FPGA Power



FPGA Decoupling caps



Project name: LimeSDR-USB_Iv4.PrbPcb

Title: **FPGA misc (power, clocks, config)**

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Surry United Kingdom

File: 10_FPGA_msc.SchDoc

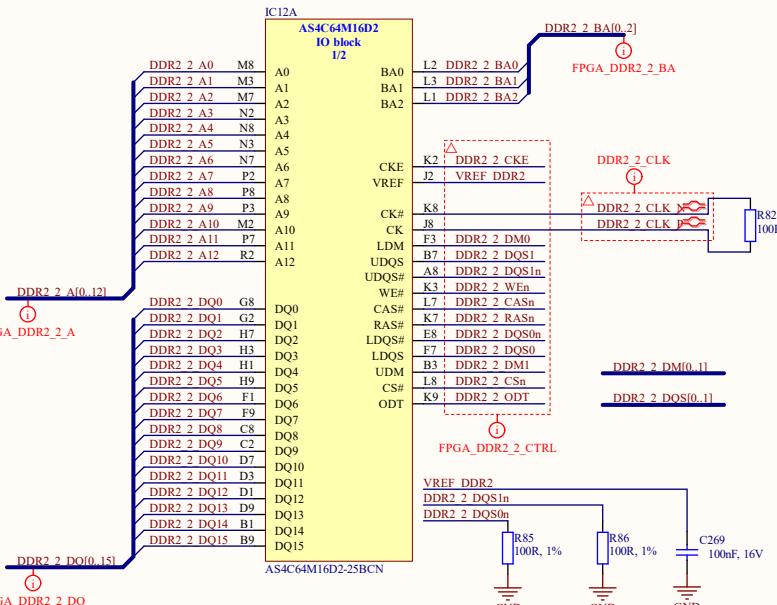
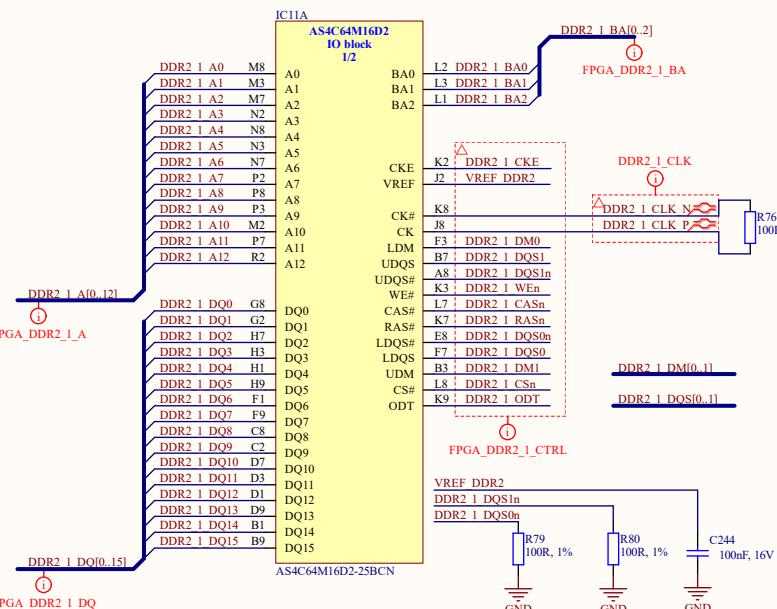
Date: 10/7/2016 Time: 1:08:48 PM Sheet 10 of 15

Size: A3 Revision: v1.4

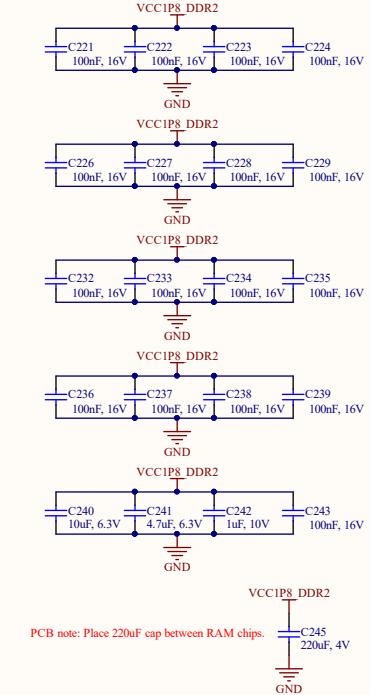
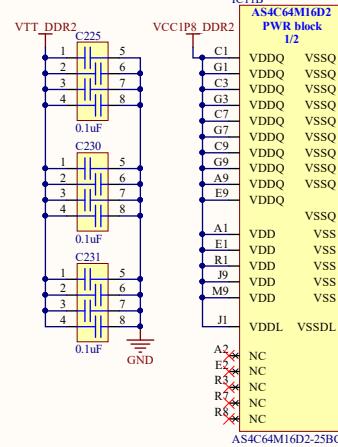
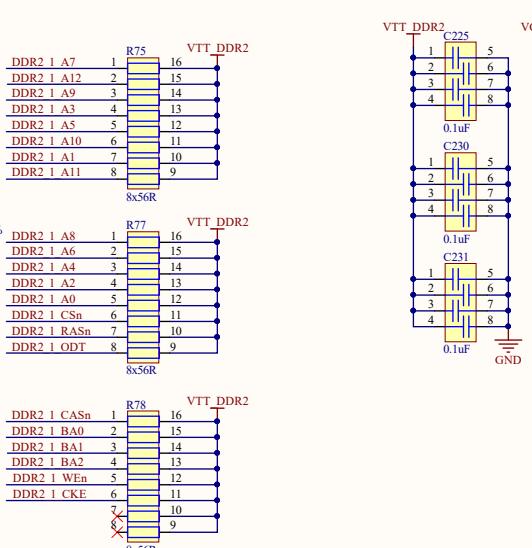
Page: 1

NF elements on sheet: -
Number of NF elements on sheet: 0

DDR2_1 (BOT L)



DDR2_2 (BOT R)



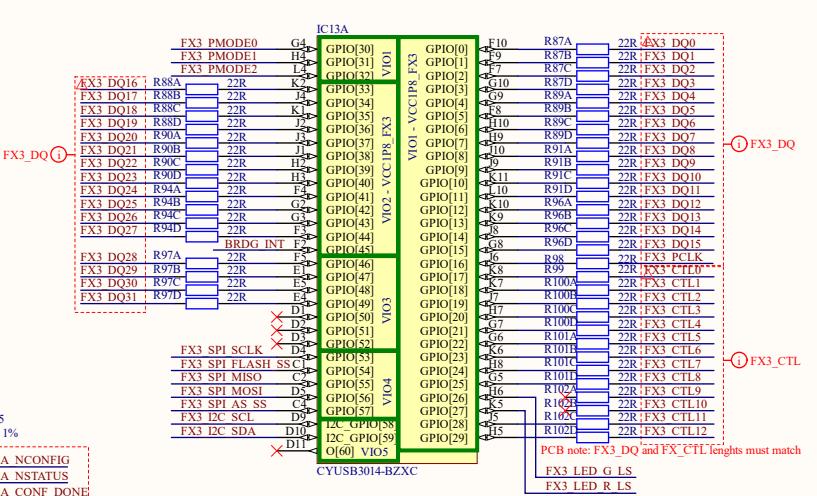
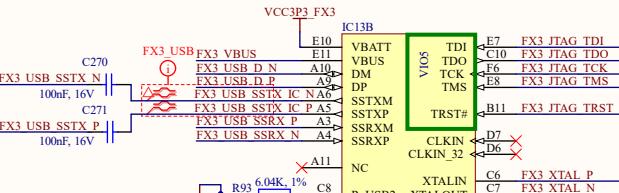
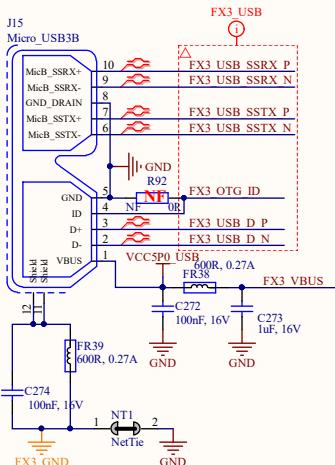
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Title:	RAM DDR2
Size:	A3
Revision:	v1.4
Date:	10/7/2016
Time:	1:08:49 PM
Sheet:	Sheet 11 of 15
File:	11_DDR2.SchDoc



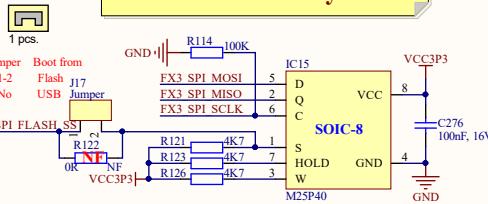
FX3 (USB3) core

NF elements on sheet: R92, R111, R116, R119, R120, R122, R124

Number of NF elements on sheet: 7



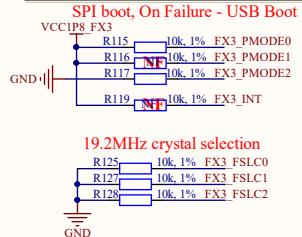
FX3 memory



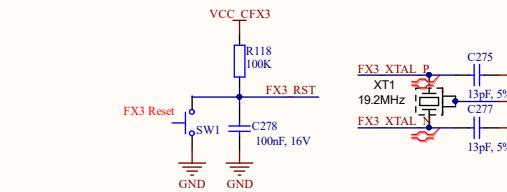
FX3 JTAG (10 pin)



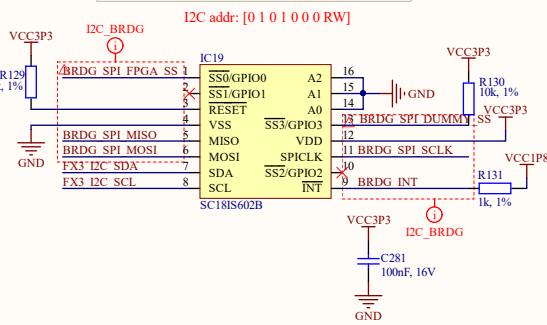
FX3 Config



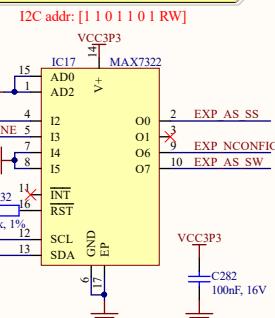
FX3 Misc



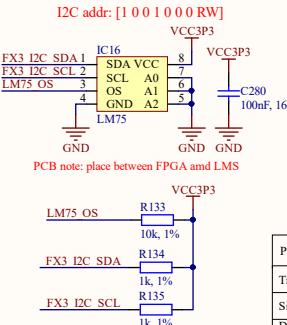
I2C SPI Bridge



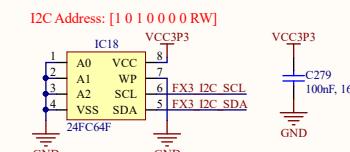
I2C Port Expander



I2C Temperature sensor



I2C EEPROM



Project name: LimeSDR-USB_Iv4.PrfPcb

Title: **USB3.0 device**

Lime Microsystems

Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom



Size: A3 Revision: v1.4

Date: 10/7/2016 Time: 1:08:49 PM Sheet 12 of 15

File: 12_USB3_0.device.SchDoc

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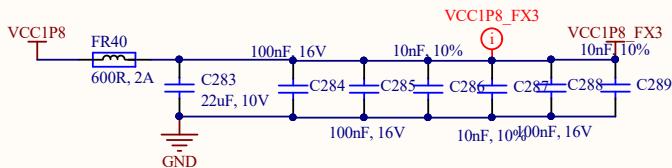
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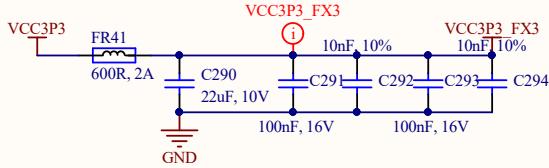
NF elements on sheet: FR42, FR43
Number of NF elements on sheet: 2

USB3 power

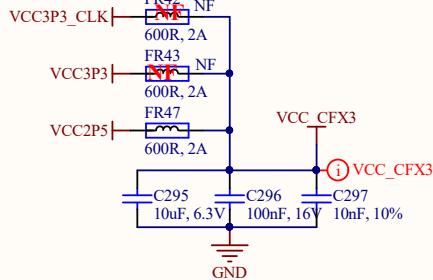
A



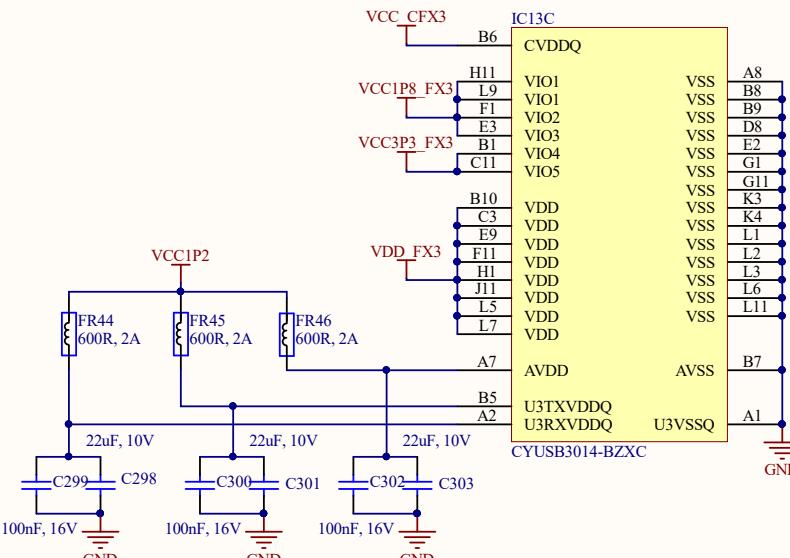
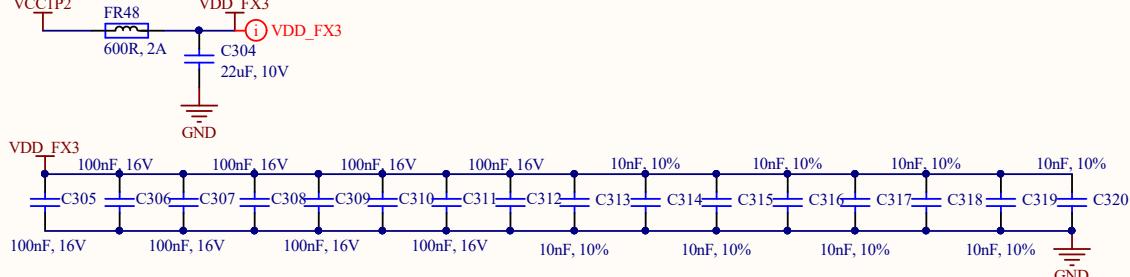
B



C



D



Project name: LimeSDR-USB_1v4.PrjPcb

Title: USB3.0 power

Size: A4 Revision: v1.4

Date: 10/7/2016 Time: 1:08:49 PM Sheet 13 of 15

File: 13_USB3_0_power.SchDoc

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United Kingdom



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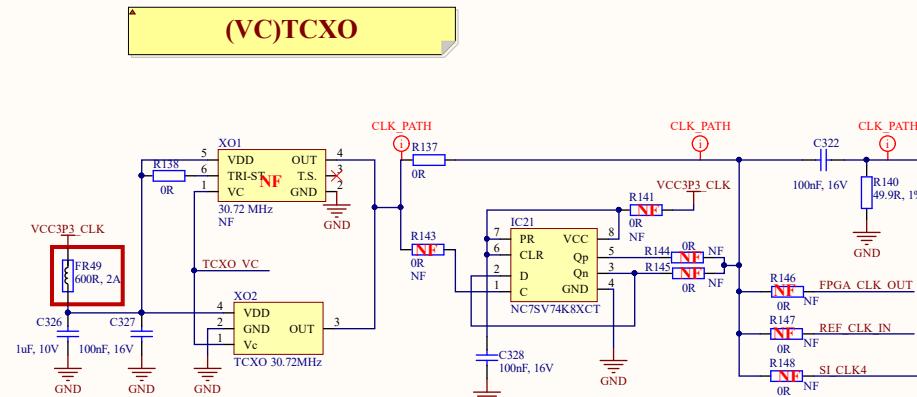
7

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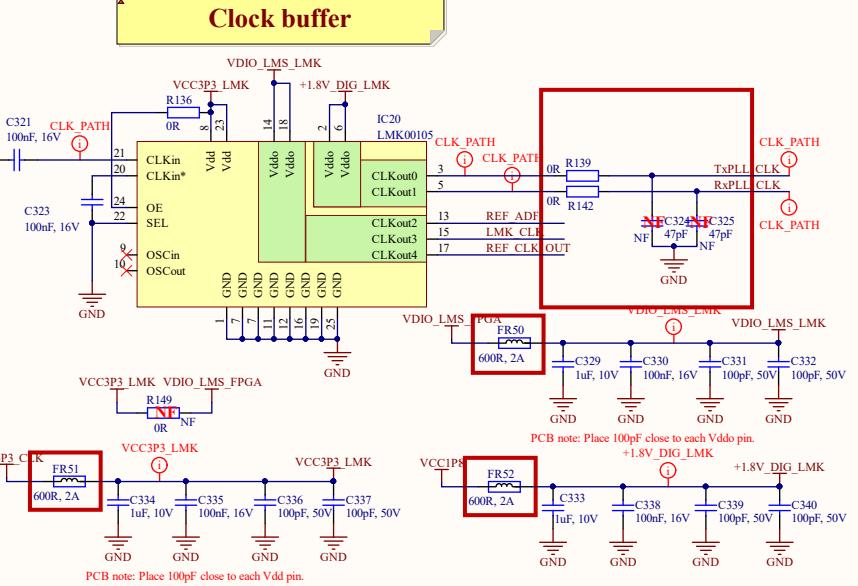
NF elements on sheet: X01, R141, R143, R144, R145, R146, R147, R148, R149, R151, R155, C324, C325, C341
 Number of NF elements on sheet: 14

Clock circuits

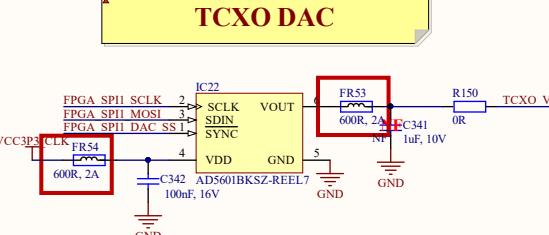
(VC)TCXO



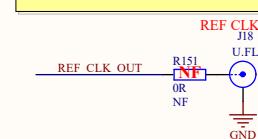
Clock buffer



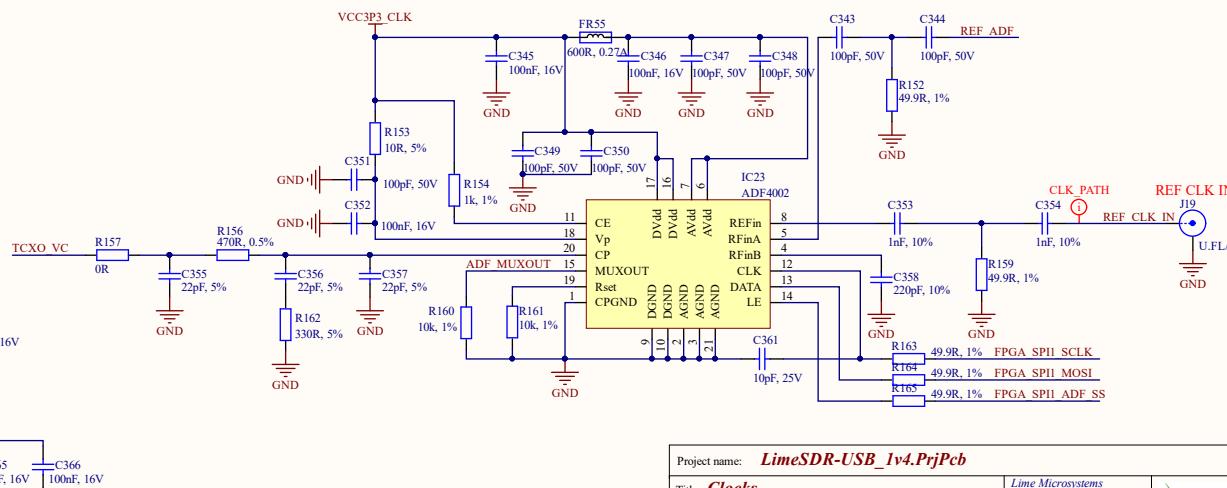
TCXO DAC



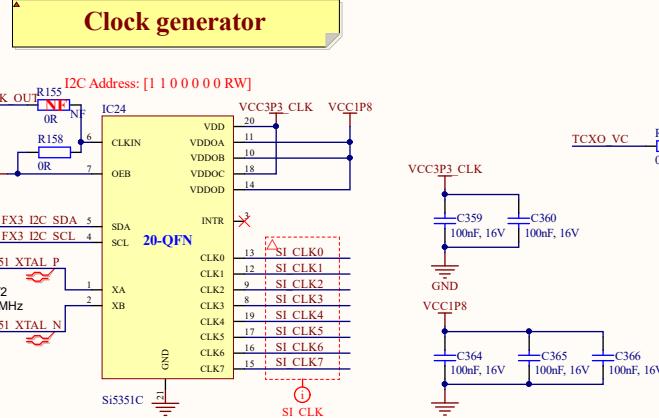
REF CLK OUT



Phase detector



Clock generator



Project name: LimeSDR-USB_Iv4.PrbPcb

Title: Clocks

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Size: A3 Revision: v1.4

Date: 10/7/2016 Time: 1:08:49 PM Sheet 14 of 15

File: 14_Clocks.SchDoc

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Board power circuits

