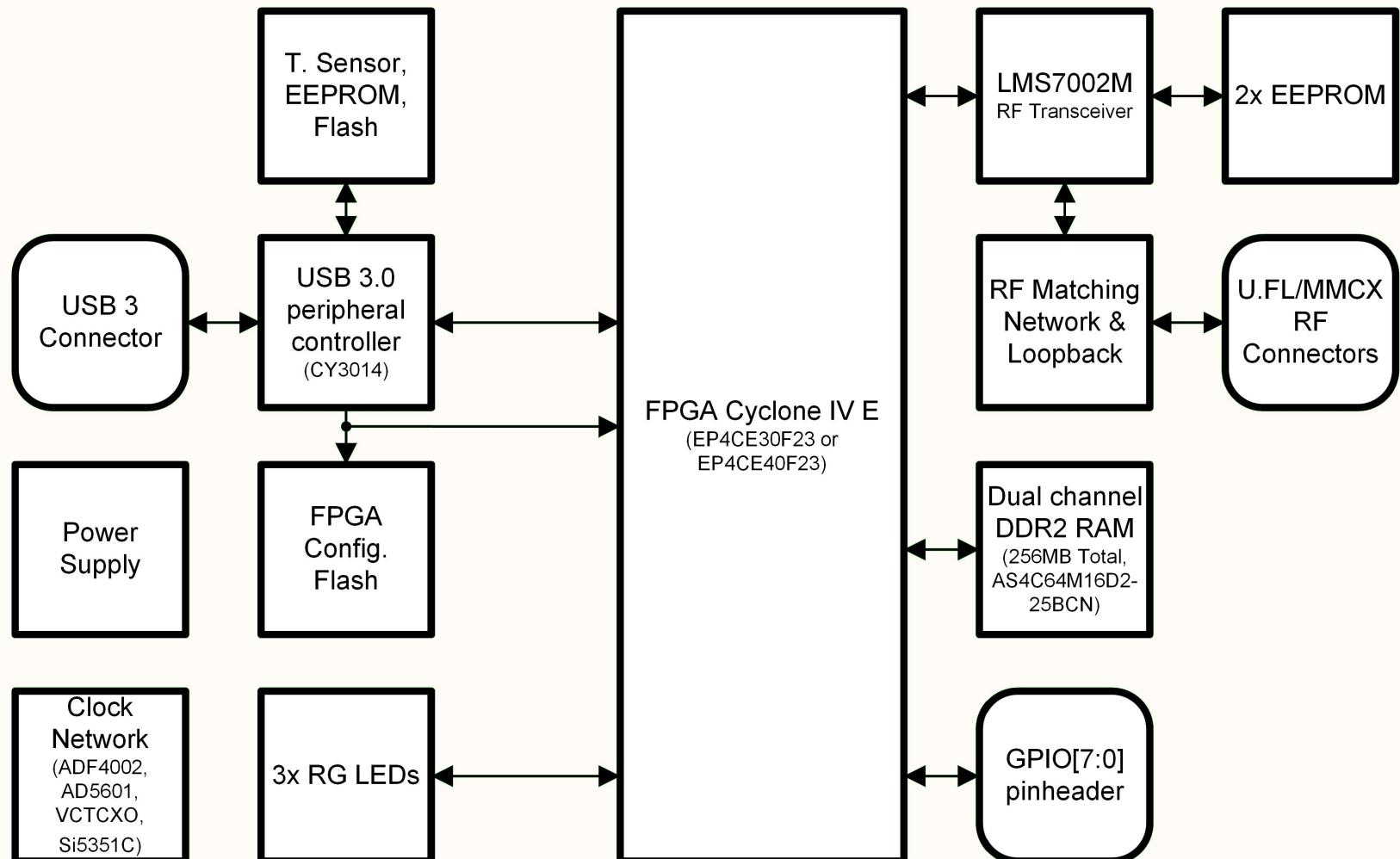


Block diagram



Project name: **LimeSDR-USB_Iv4.PrjPcb**

Title: **Block diagram**

Size: **A4** Revision: **v1.4**

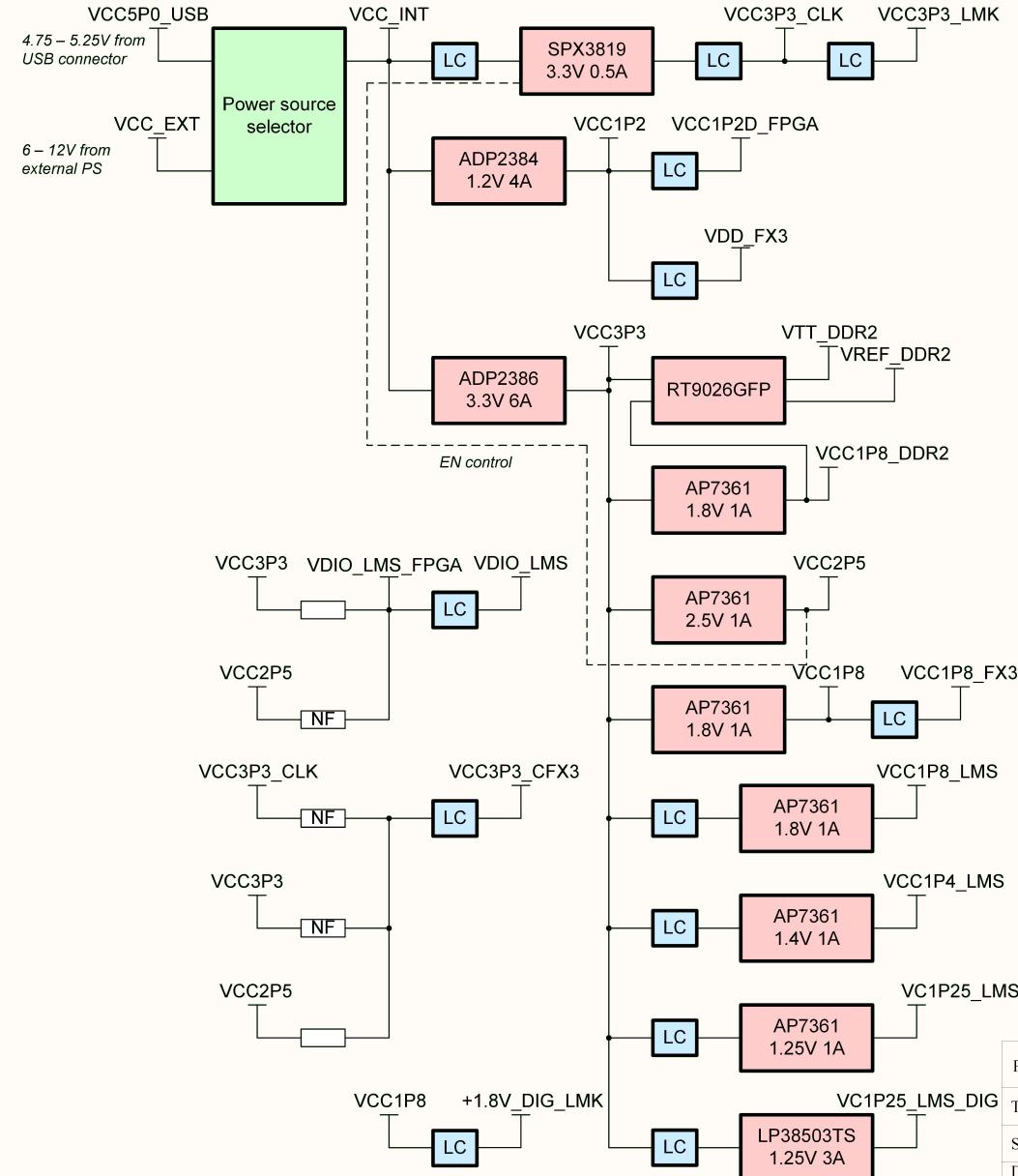
Date: **2020-09-30** Time: **14:07:24** Sheet **1** of **15**

File: **01_BlockDiagram.SchDoc**

Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom



Power diagram



Project name: **LimeSDR-USB_Iv4.PrjPcb**

Title: **Power diagram**

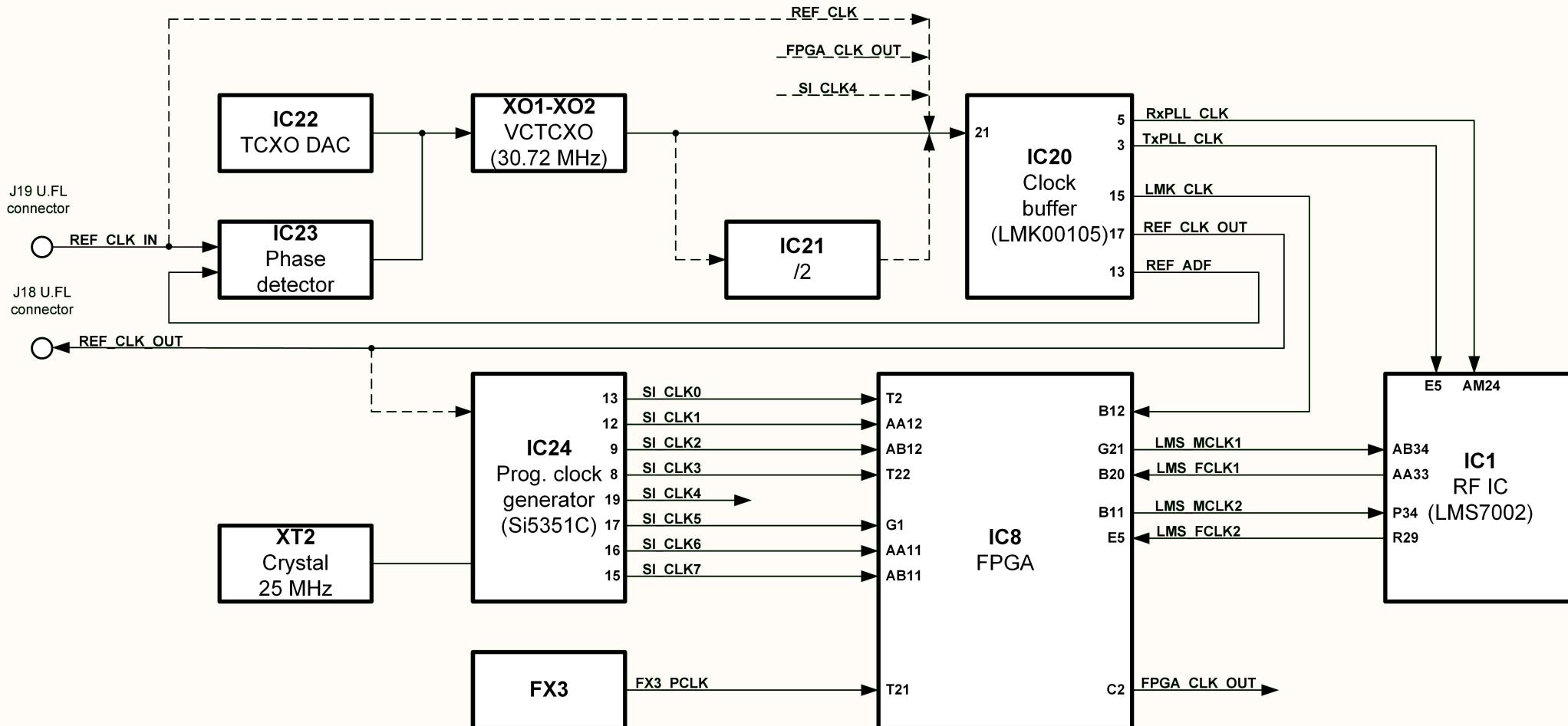
Size: **A4** Revision: **v1.4**

Date: **2020-09-30** Time: **14:07:31** Sheet**2** of **15**

Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom



Clock diagram



Project name: *LimeSDR-USB_Iv4.PpjPcb*

Title: *Clock diagram*

Size: **A4** Revision: **v1.4**

Date: **2020-09-30** Time: **14:07:46** Sheet**3** of **15**

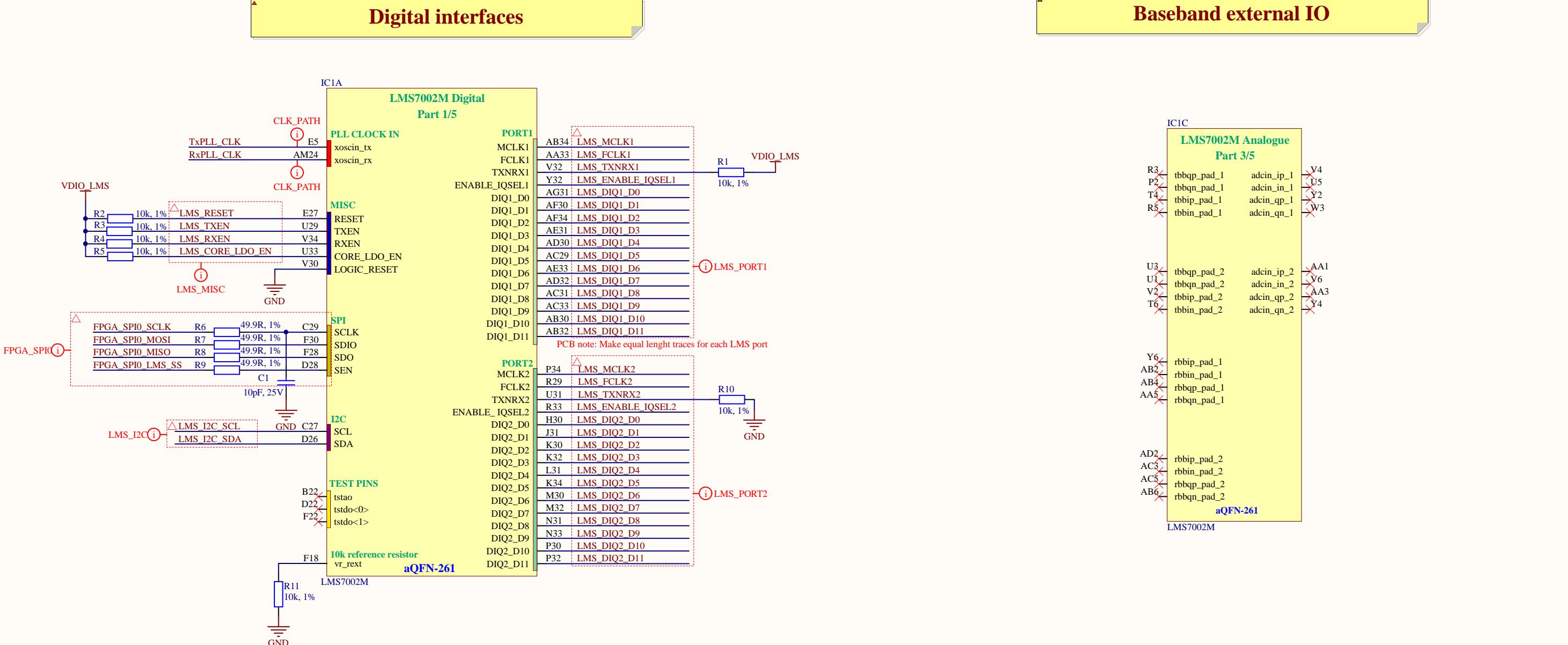
File: **03_ClockDiagram.SchDoc**

Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom

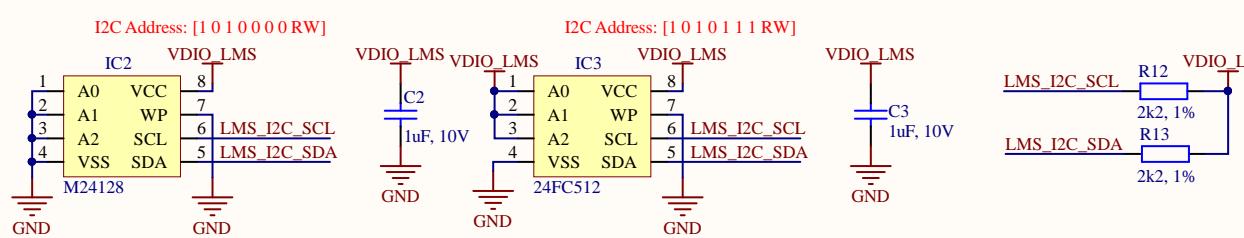


NF elements on sheet: -
Number of NF elements on sheet: 0

LMS7002M misc



LMS EEPROMs



Project name: LimeSDR-USB_1v4.PnjPcb

Title: LMS7002M misc

Size: A3 Revision: v1.4

Date: 2020-09-30 Time: 14:07:55 Sheet 4 of 15

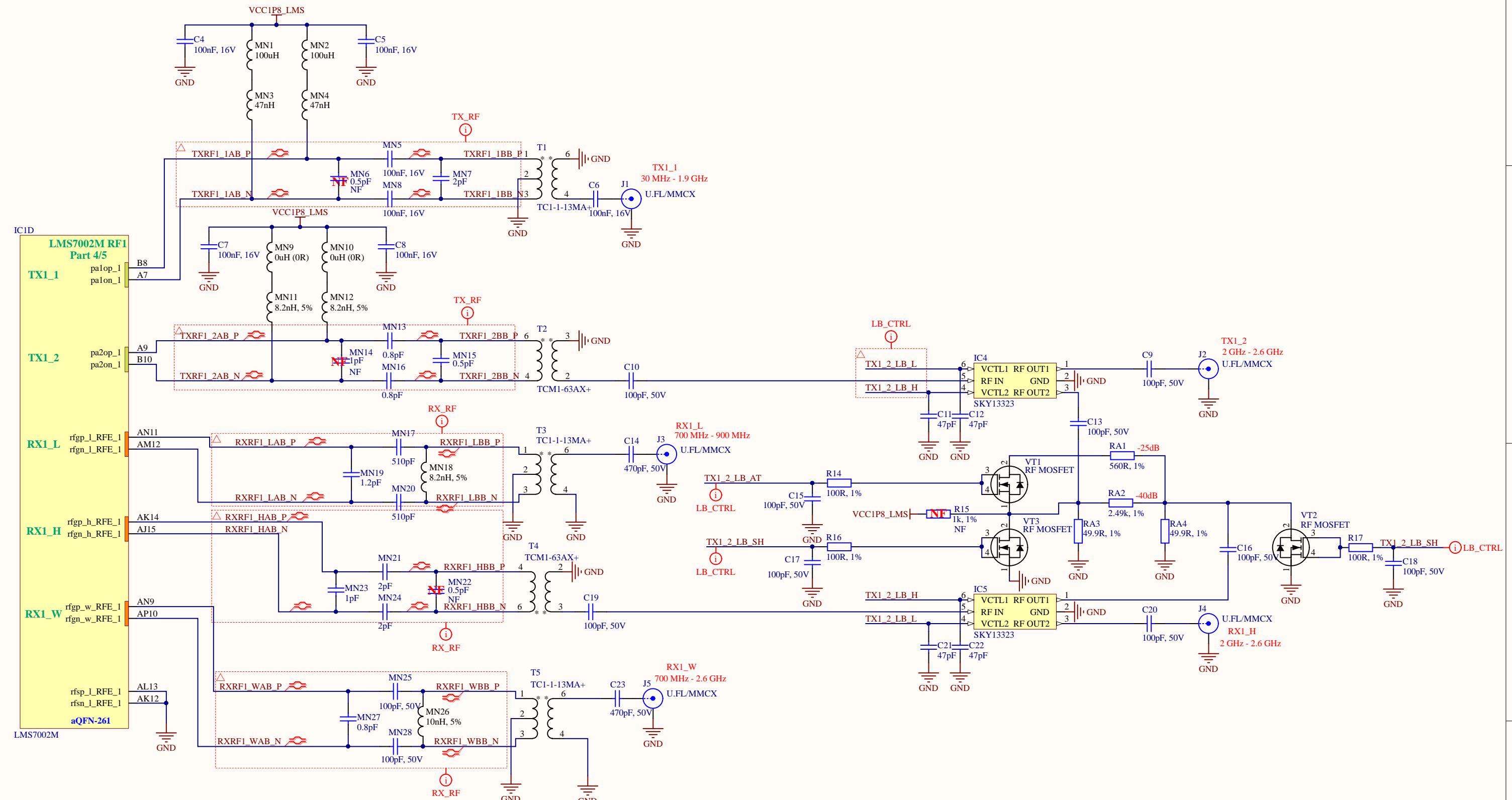
File: 04_LMS7002M_Misc.SchDoc

Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom



NF elements on sheet: MN6, MN14, MN22, R15
Number of NF elements on sheet: 4

LMS7002M RF1 circuits



Project name: LimeSDR-USB_1v4.PnjPcb

Title: LMS7002M RF

Size: A3 Revision: v1.4

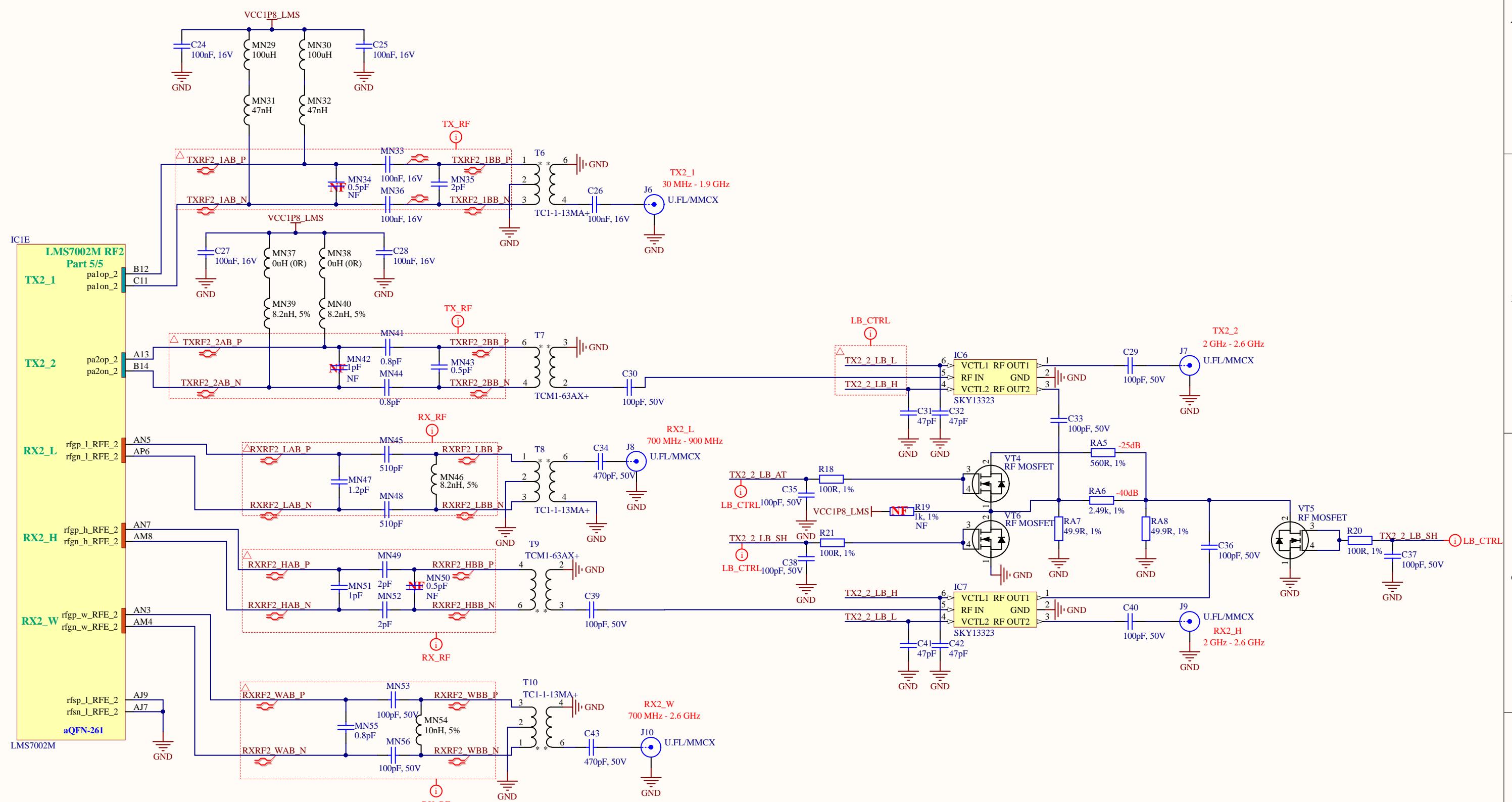
Date: 2020-09-30 Time: 14:07:59 Sheet 5 of 15

File: 05_LMS7002M_RF1.SchDoc



NF elements on sheet: MN34, MN42, MN50, R19
 Number of NF elements on sheet: 4

LMS7002M RF2 circuits



Project name: LimeSDR-USB_1v4.PnjPcb

Title: LMS7002M RF

Size: A3 Revision: v1.4

Date: 2020-09-30 Time: 14:08:04 Sheet 6 of 15

File: 06_LMS7002M_RF2.SchDoc

Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom



LMS7002M power supply circuit

NF elements on sheet: FR18, FR25
Number of NF elements on sheet: 2

A

A

B

B

C

C

D

D

E

E

F

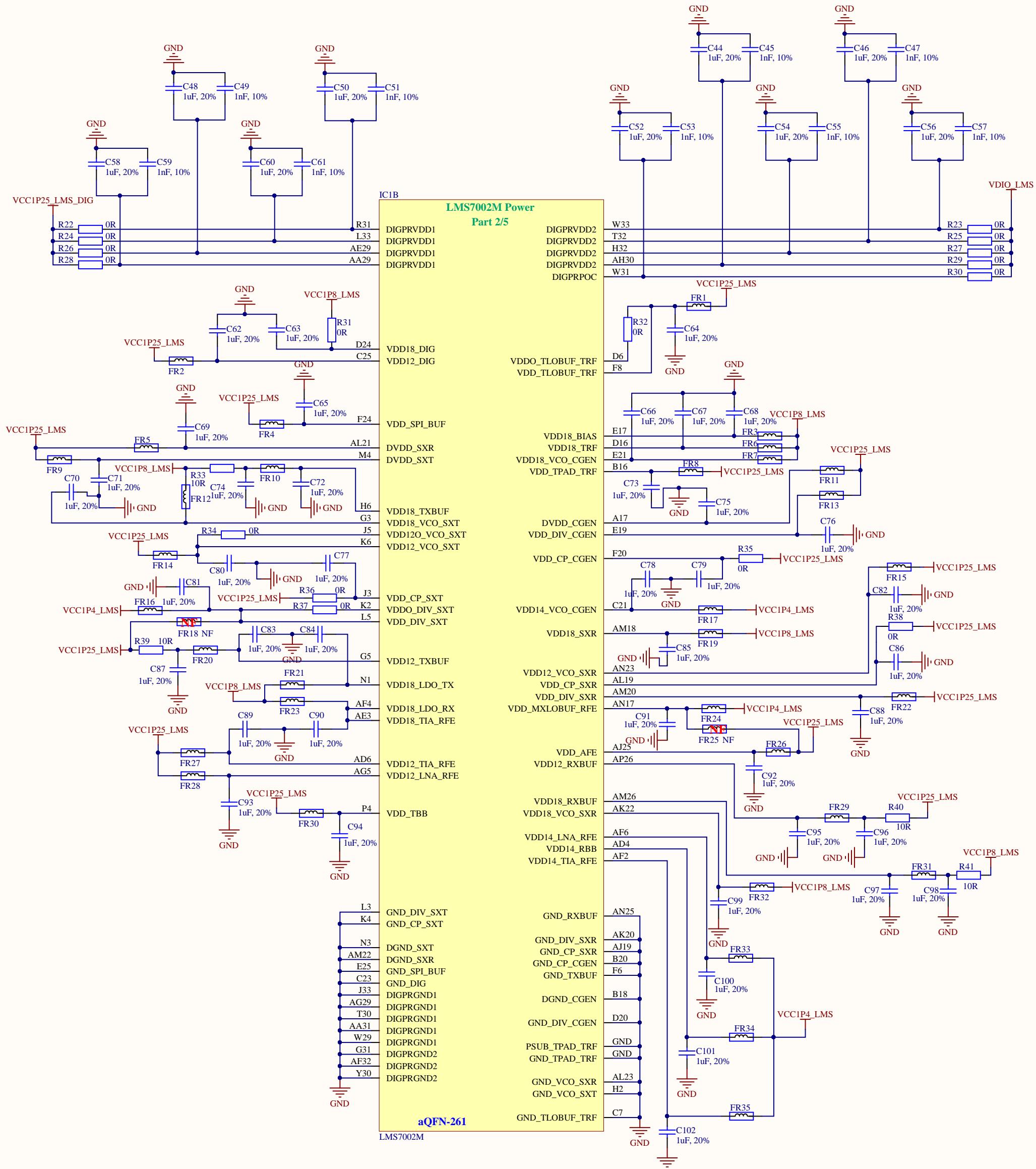
F

G

G

H

H



Project name: LimeSDR-USB_1v4.PrjPcb

Title: LMS7002M power supply

Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom



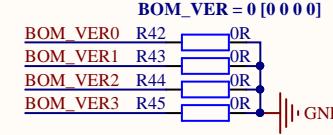
Size: A3 Revision: v1.4

Date: 2020-09-30 Time: 14:08:10 Sheet 7 of 15

File: 07_LMS7002M_Power.SchDoc

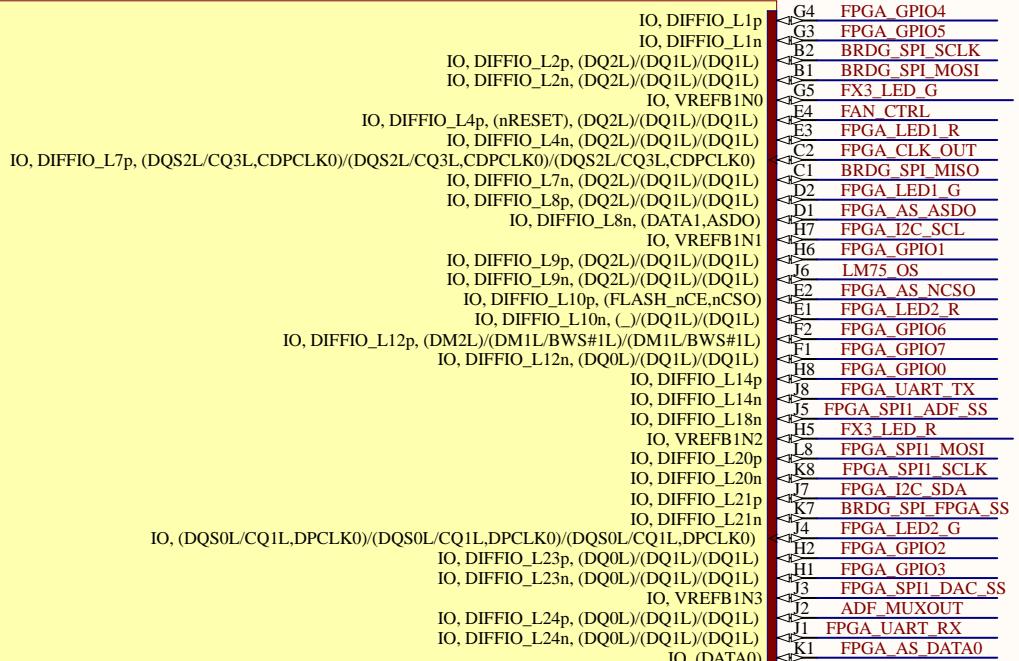
FPGA banks 1, 2, 3, 4

NF elements on sheet: -
Number of NF elements on sheet: 0



A

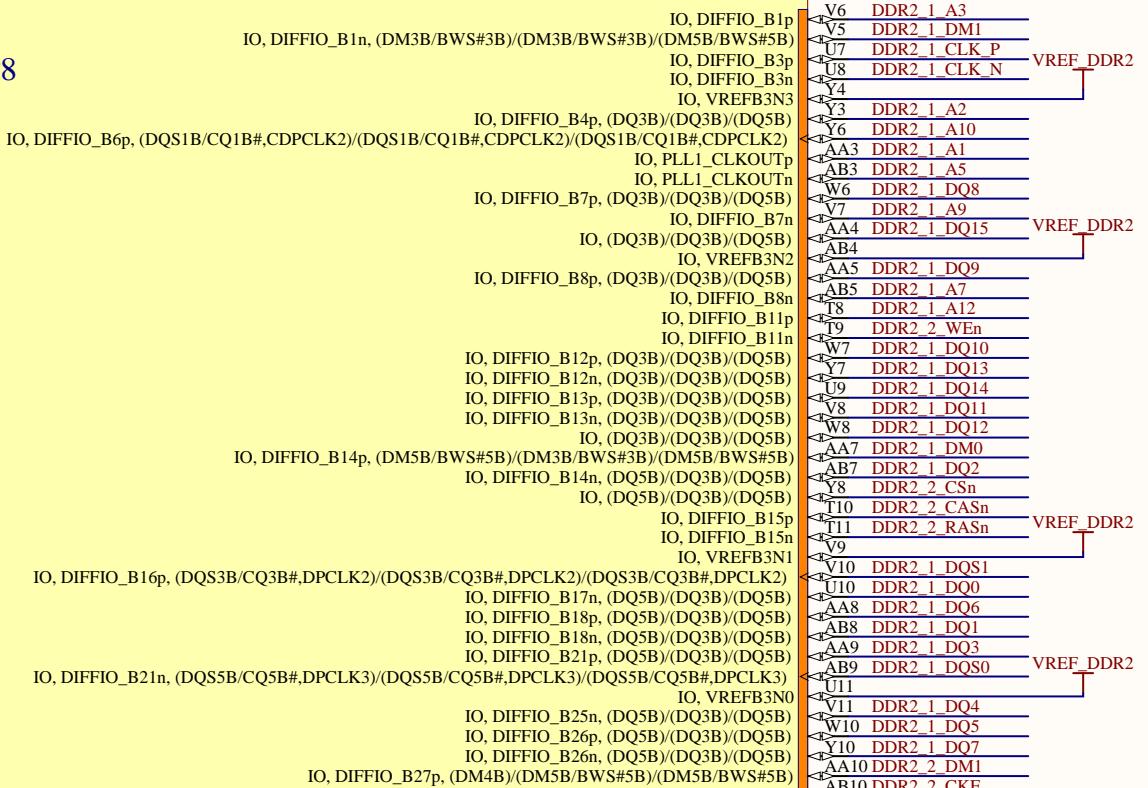
IC8A
BANK 1
VCC3P3



EP4CE40F23C8N

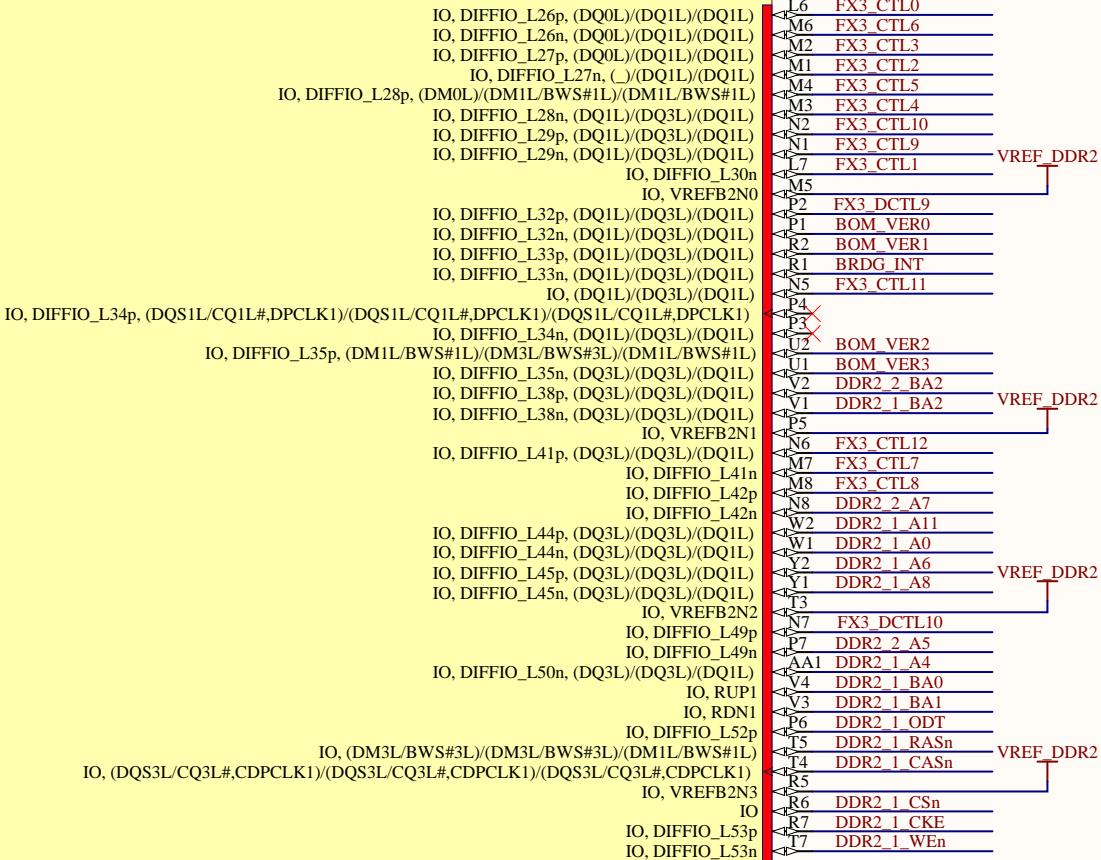
B

IC8C
BANK 3
VCC1P8



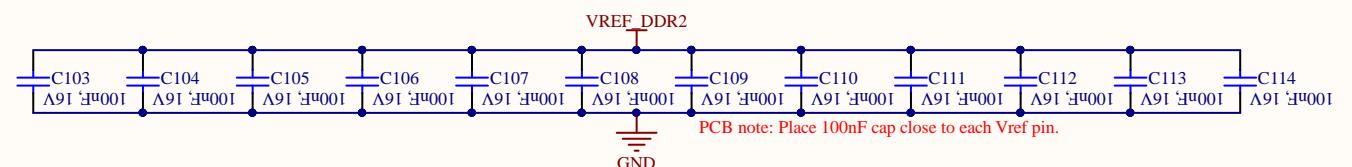
EP4CE40F23C8N

IC8B
BANK 2
VCC1P8



EP4CE40F23C8N

D



1

2

3

4

5

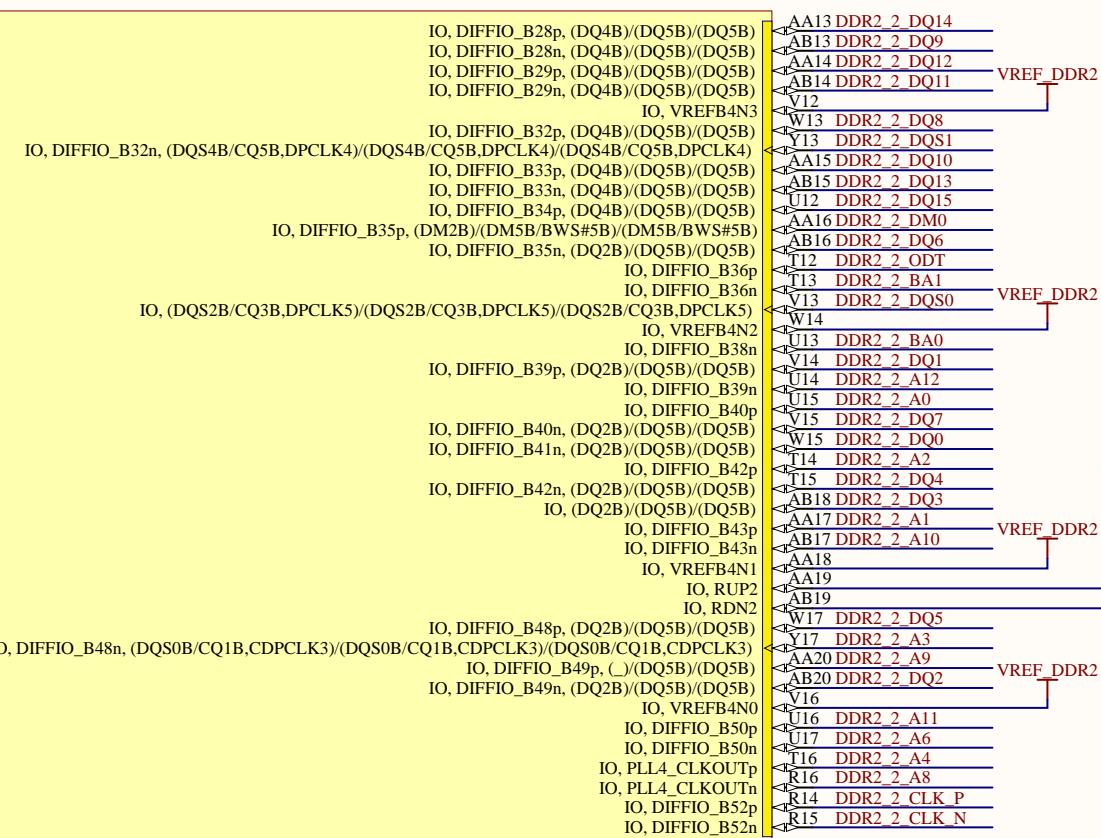
6

7

8

PCB note: Place 100nF cap close to each Vref pin.

IC8D
BANK 4
VCC1P8



EP4CE40F23C8N

Project name: LimeSDR-USB_1v4.PjrPcb

Title: **FPGA banks 1, 2, 3, 4**

Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom



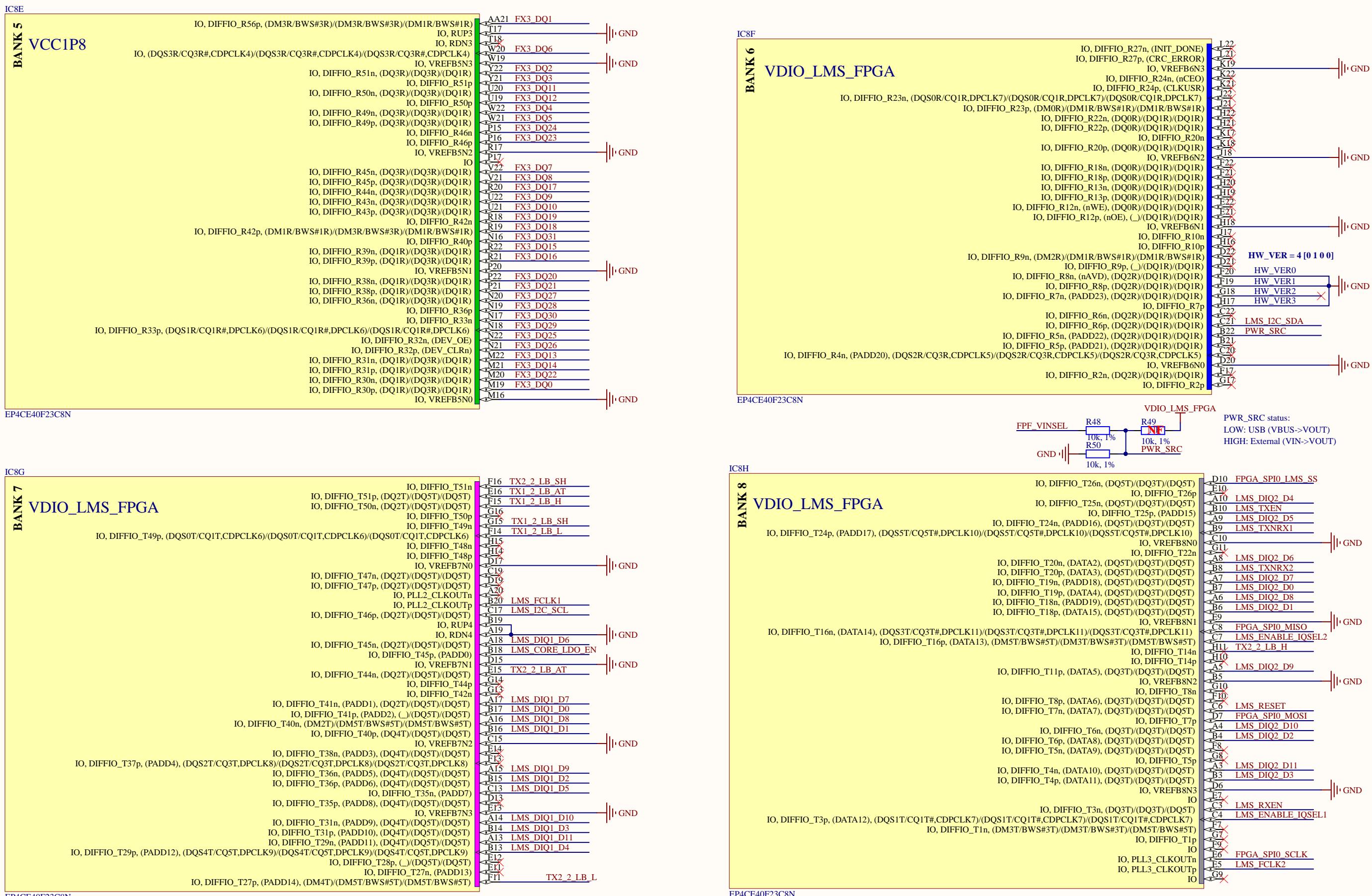
Size: A3 Revision: v1.4

Date: 2020-09-30 Time: 14:08:16 Sheet 8 of 15

File: 08_FPGA_banks_1_2_3_4.SchDoc

NF elements on sheet: R49
Number of NF elements on sheet: 1

FPGA banks 5, 6, 7, 8



Project name: LimeSDR-USB_1v4.PrfPcb

Title: **FPGA banks 5, 6, 7, 8**

Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom



Size: A3 Revision: v1.4

Date: 2020-09-30 Time: 14:08:22 Sheet 9 of 15

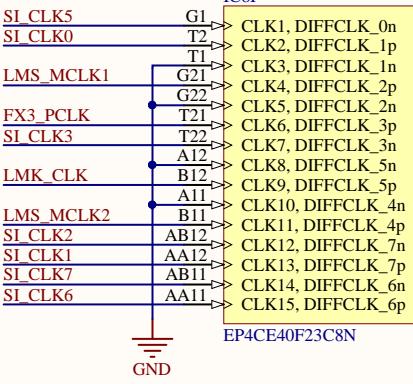
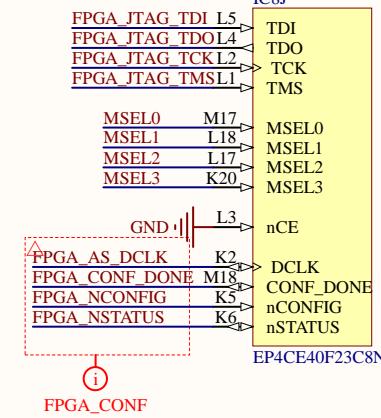
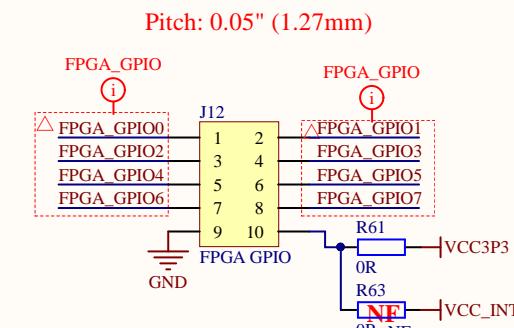
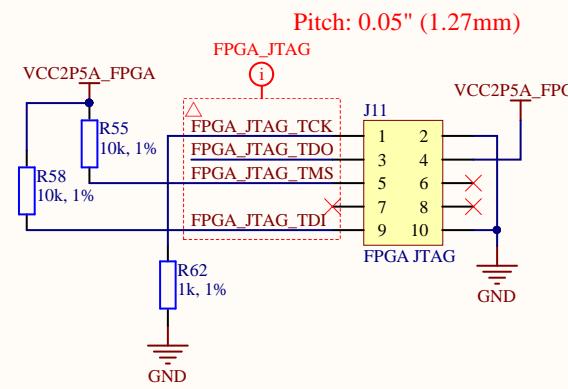
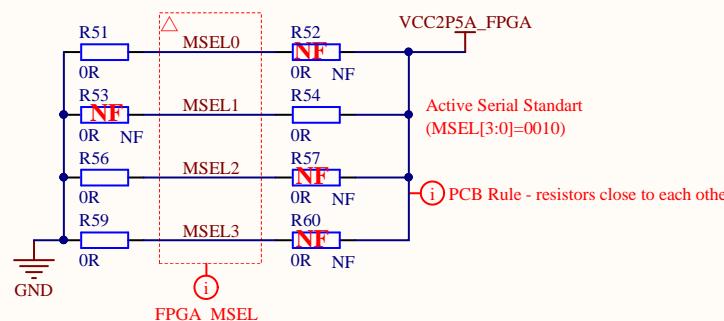
File: 09_FPGA_banks_5_6_7_8.SchDoc

FPGA misc (power, clocks, config)

NF elements on sheet: R52, R53, R57, R60, R63, R65, R74, J13, C142

Number of NF elements on sheet: 10

MSEL config

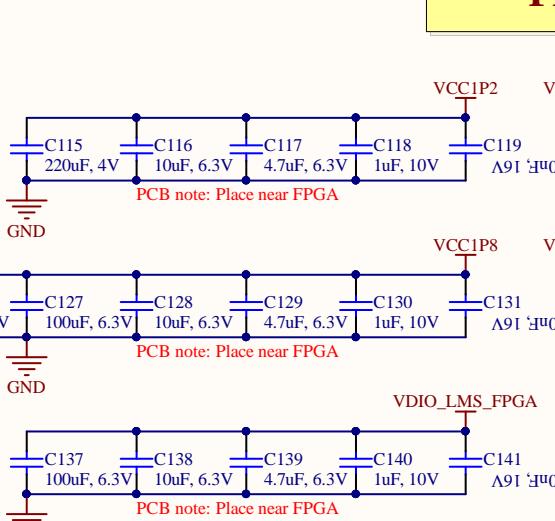
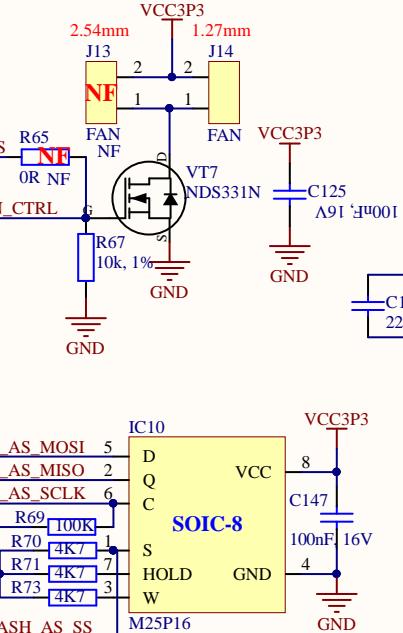
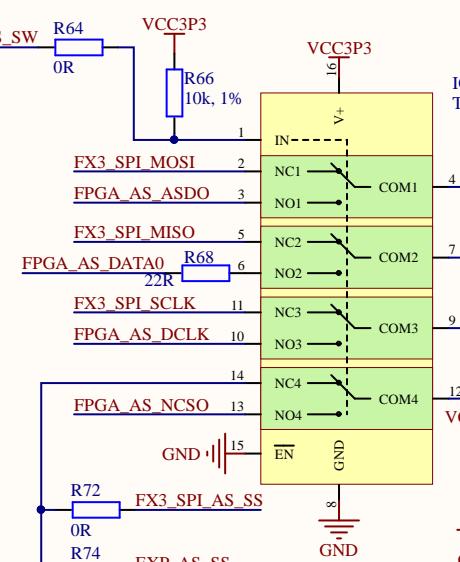


FPGA AS FLASH + Switch

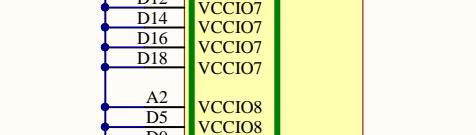
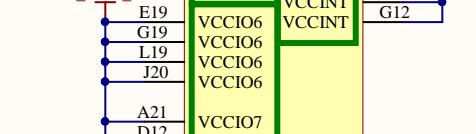
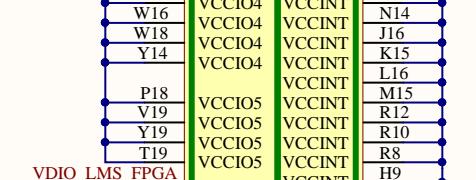
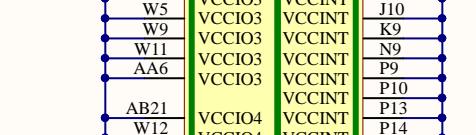
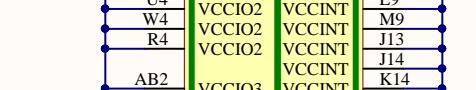
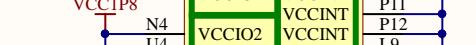
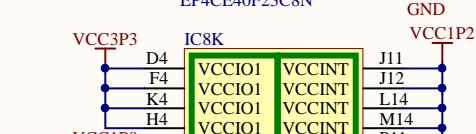
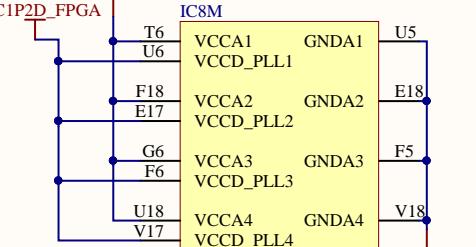
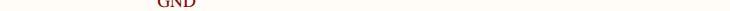
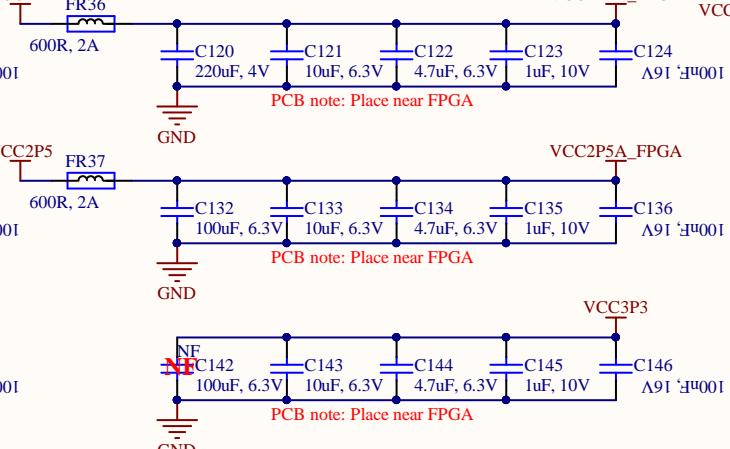
IN:

0: FLASH connected to FX3 (NC to COM)

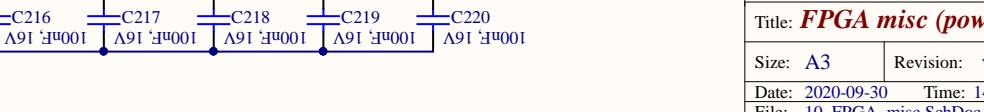
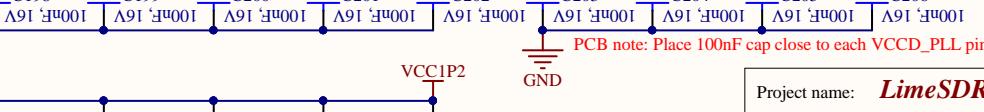
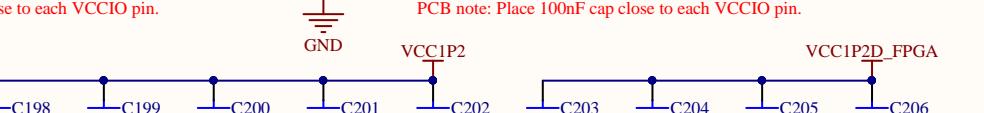
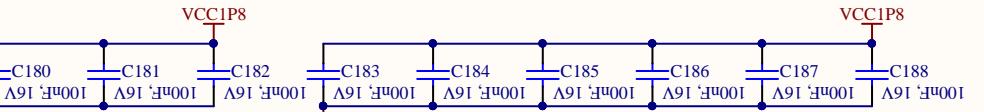
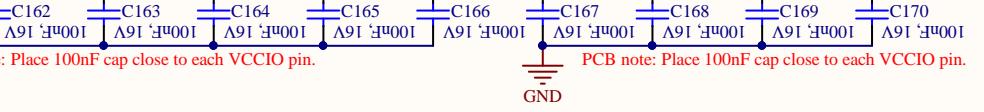
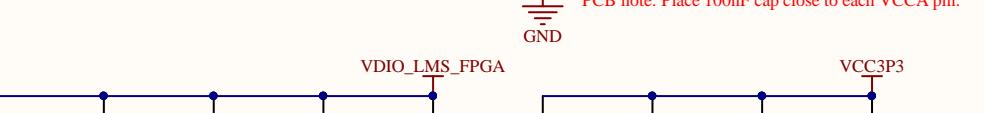
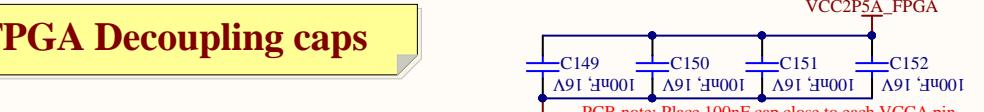
1: FLASH connected to FPGA (NO to COM)



FPGA Bulk caps



FPGA Decoupling caps



Project name: LimeSDR-USB_1v4.PnjPcb

Title: FPGA misc (power, clocks, config)

Size: A3 Revision: v1.4

Date: 2020-09-30 Time: 14:08:29 Sheet 10 of 15

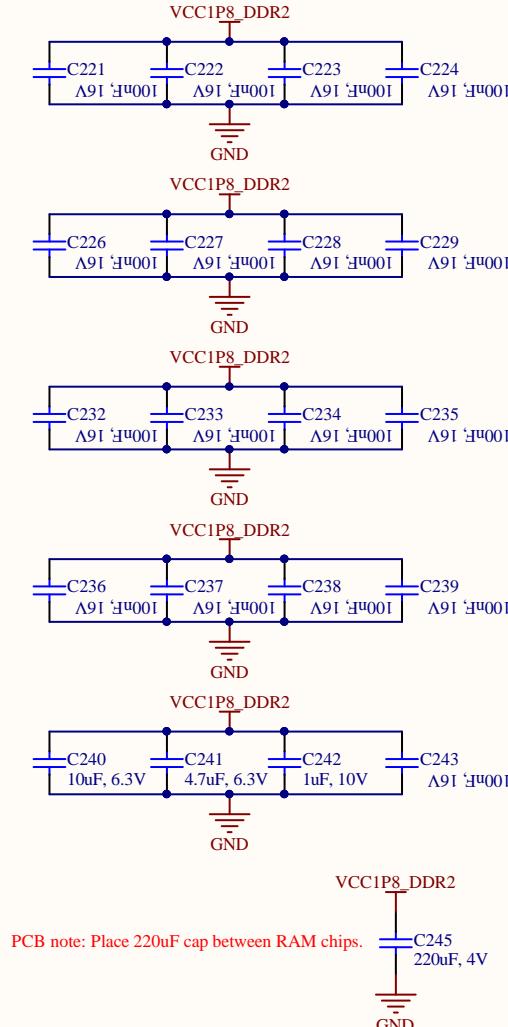
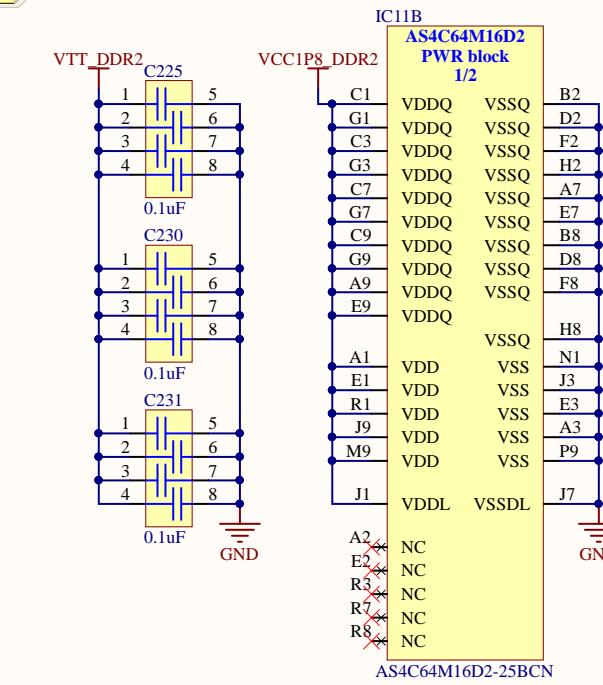
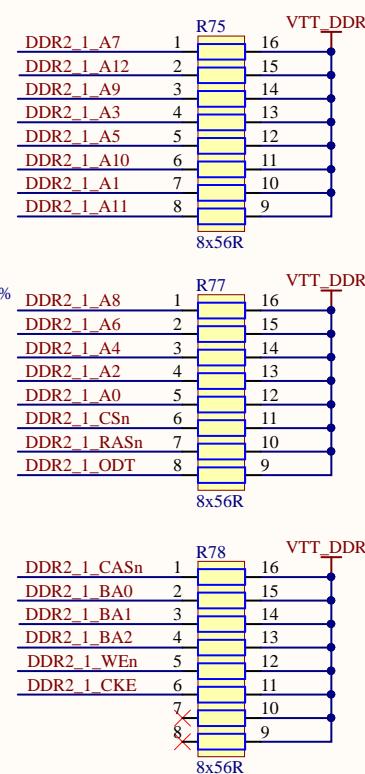
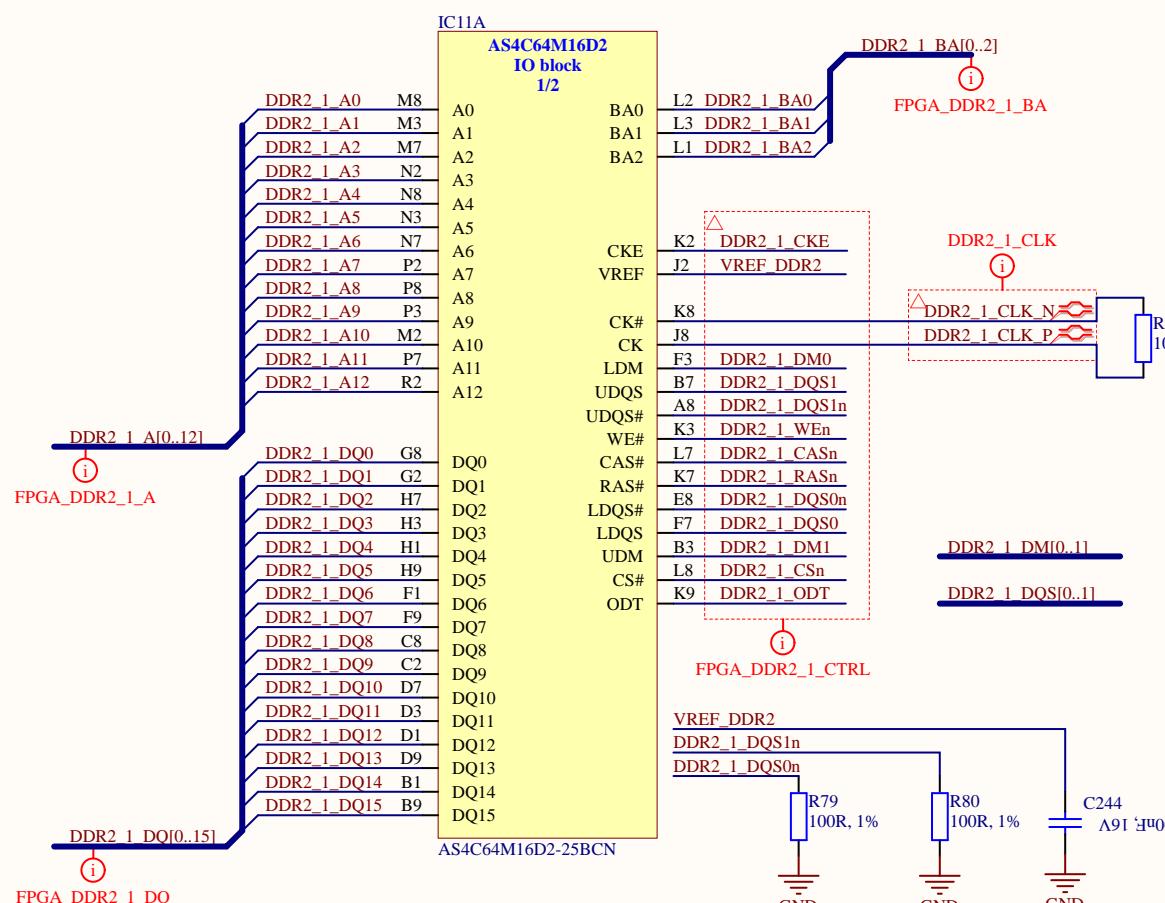
File: 10_FPGA_msc.SchDoc

Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom

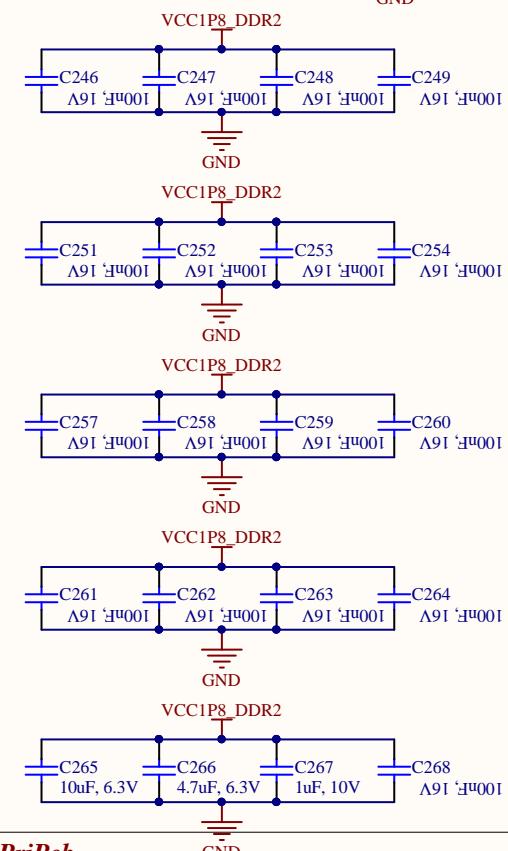
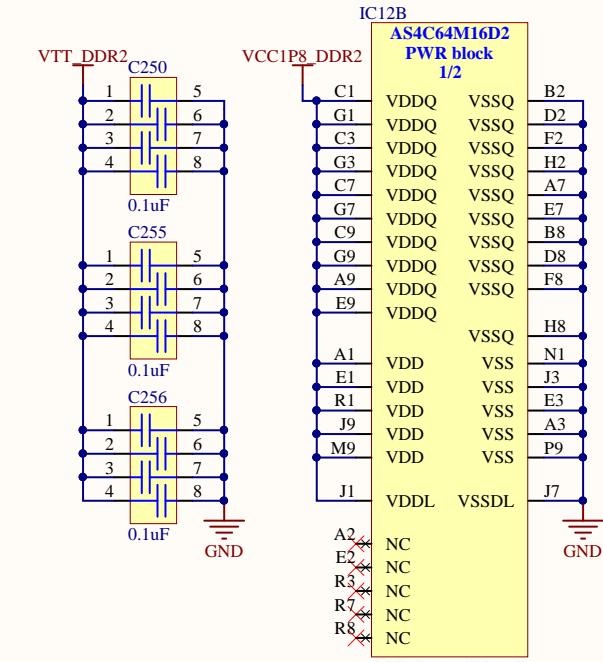
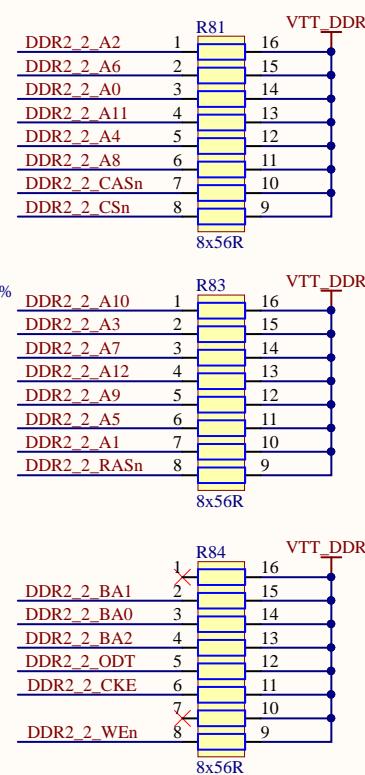
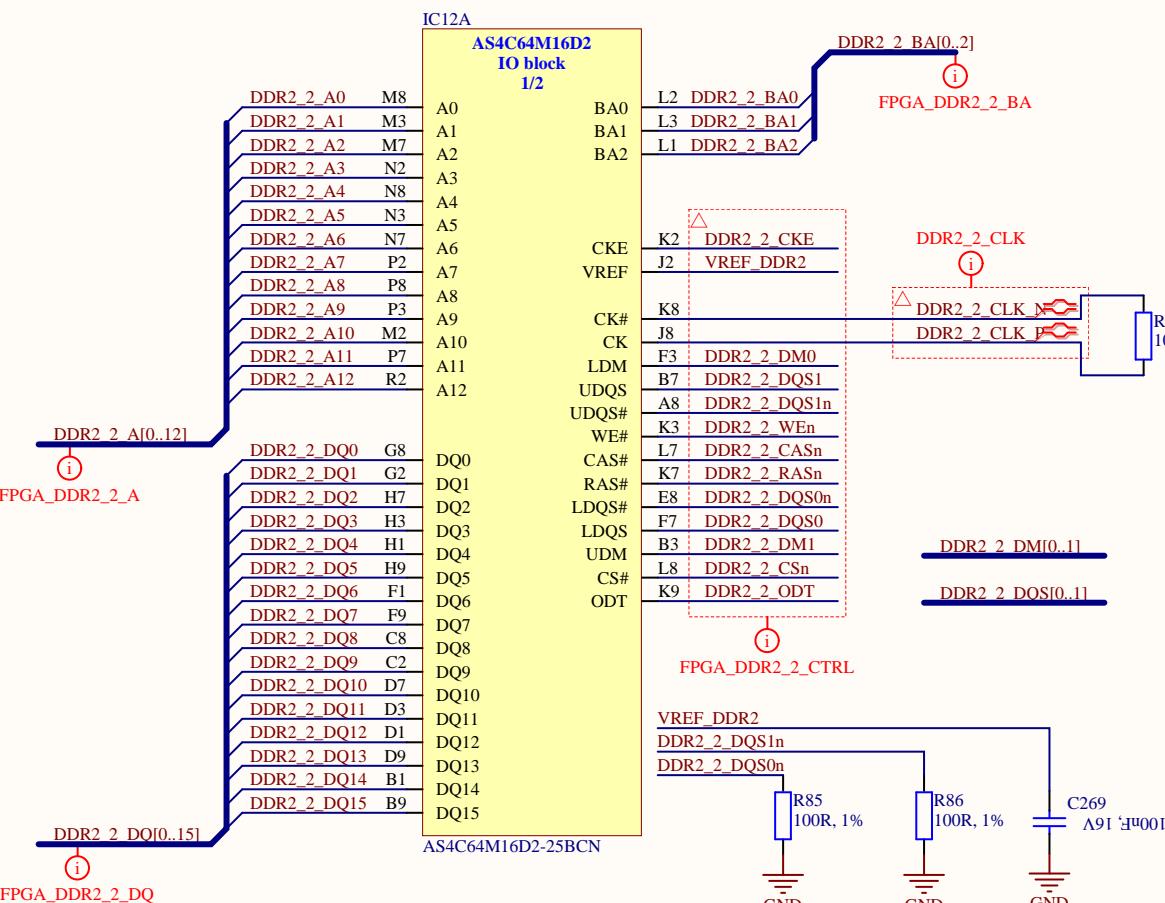


NF elements on sheet: -
Number of NF elements on sheet: 0

DDR2_1 (BOT L)



DDR2_2 (BOT R)



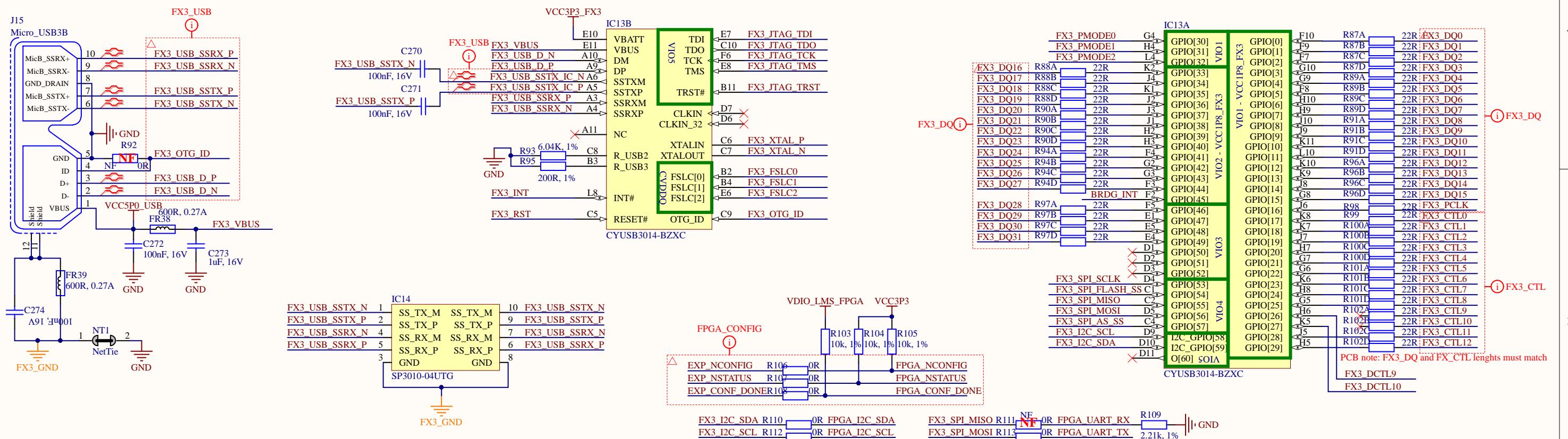
PCB note: Place 220uF cap between RAM chip

Project name: LimeSDR-USB_1v4.PrjPcc

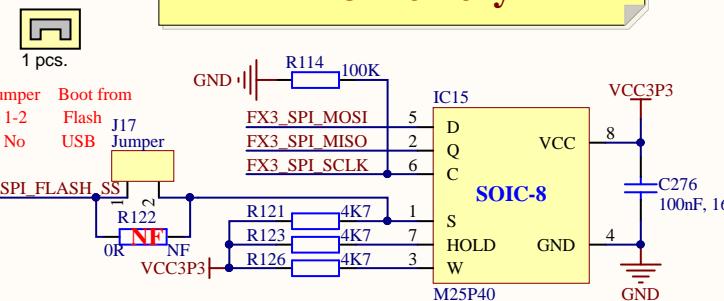
Title: RAM DDR2		<i>Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom</i>	
Size: A3	Revision: v1.4		
Date: 2020-09-30	Time: 14:08:35	Sheet 11 of 15	
File: 11_DDR2.SchDoc			

NF elements on sheet: R92, R111, R116, R119, R120, R122, R124, IC19
Number of NF elements on sheet: 8

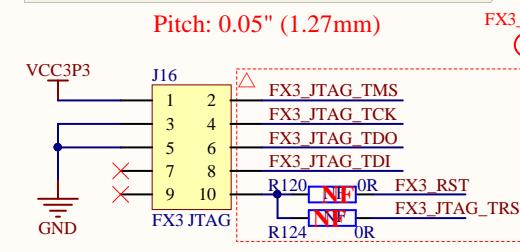
FX3 (USB3) core



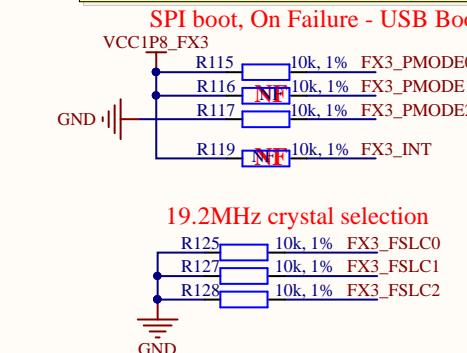
FX3 memory



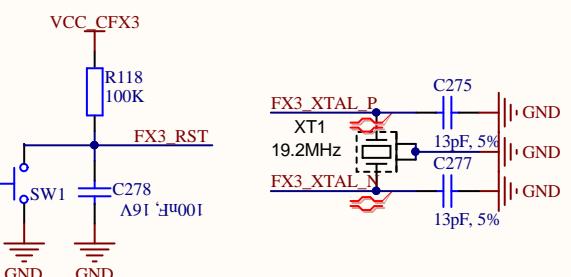
FX3 JTAG (10 pin)



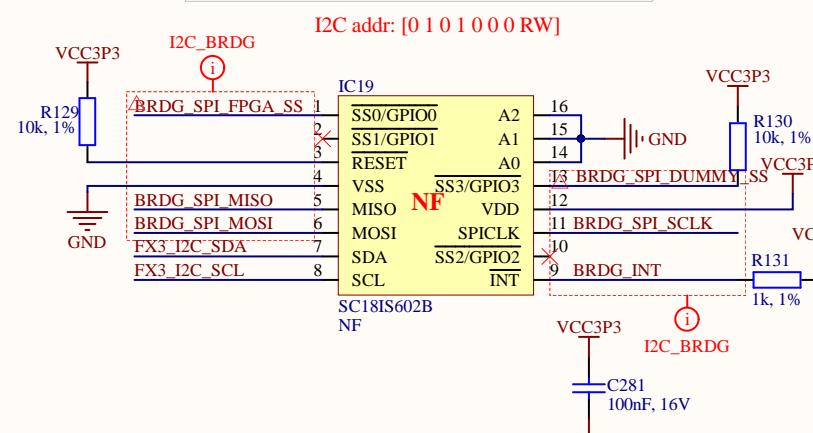
FX3 Config



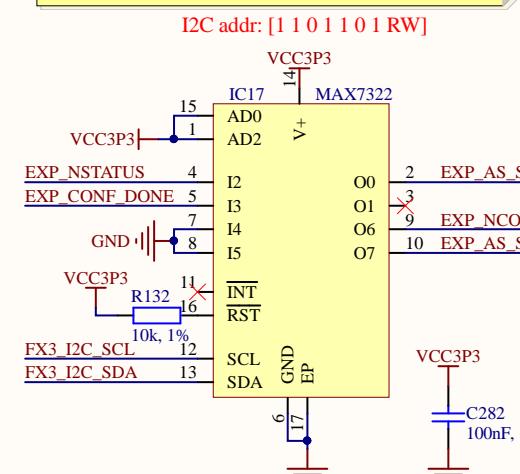
FX3 Misc



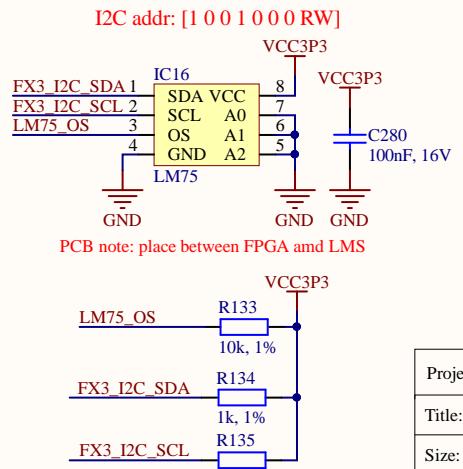
I2C SPI Bridge



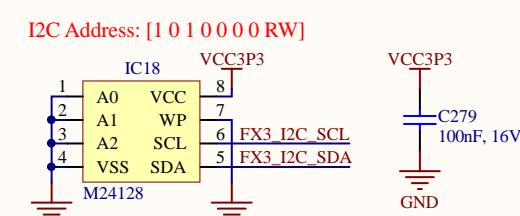
I2C Port Expander



I2C Temperature sensor



I2C EEPROM



Project name: LimeSDR-USB_1v4.PjPcb

Title: **USB3.0 device**

Size: **A3** Revision: **v1.4**

Date: 2020-09-30 Time: 14:08:41 Sheet 12 of 15

File: 12_USB3_0_device.SchDoc

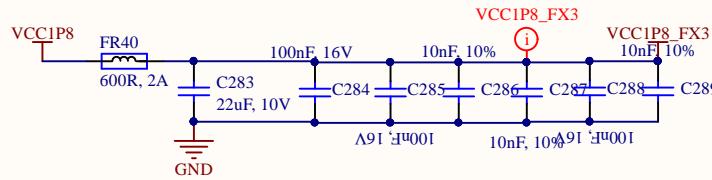
Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom



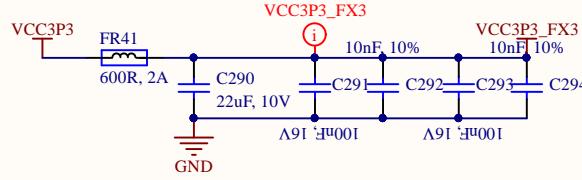
NF elements on sheet: FR42, FR43
Number of NF elements on sheet: 2

USB3 power

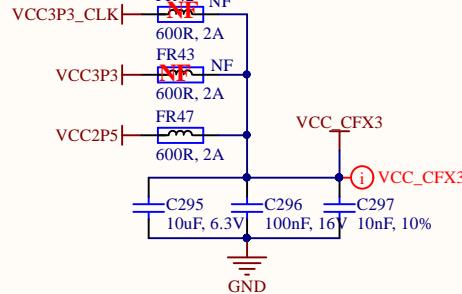
A



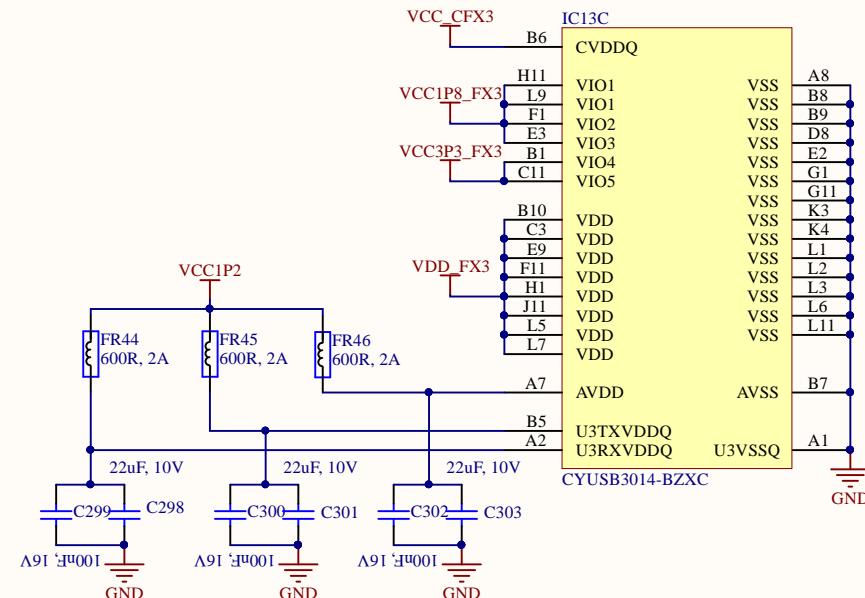
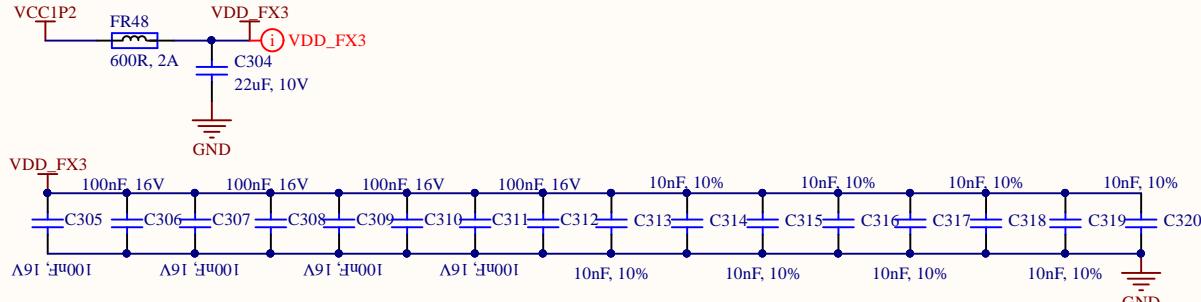
B



C



D



Project name: LimeSDR-USB_Iv4.PrjPcb

Title: USB3.0 power

Size: A4 Revision: v1.4

Date: 2020-09-30 Time: 14:08:46 Sheet 13 of 15

File: 13_USB3_0_power.SchDoc

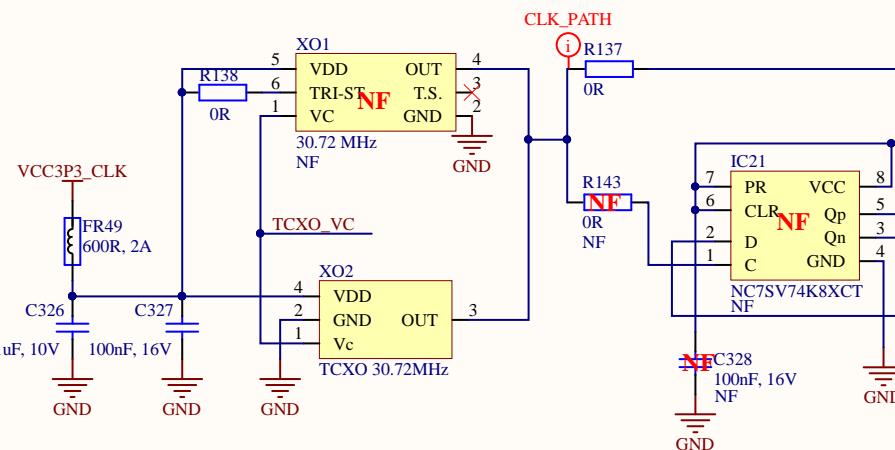
Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom



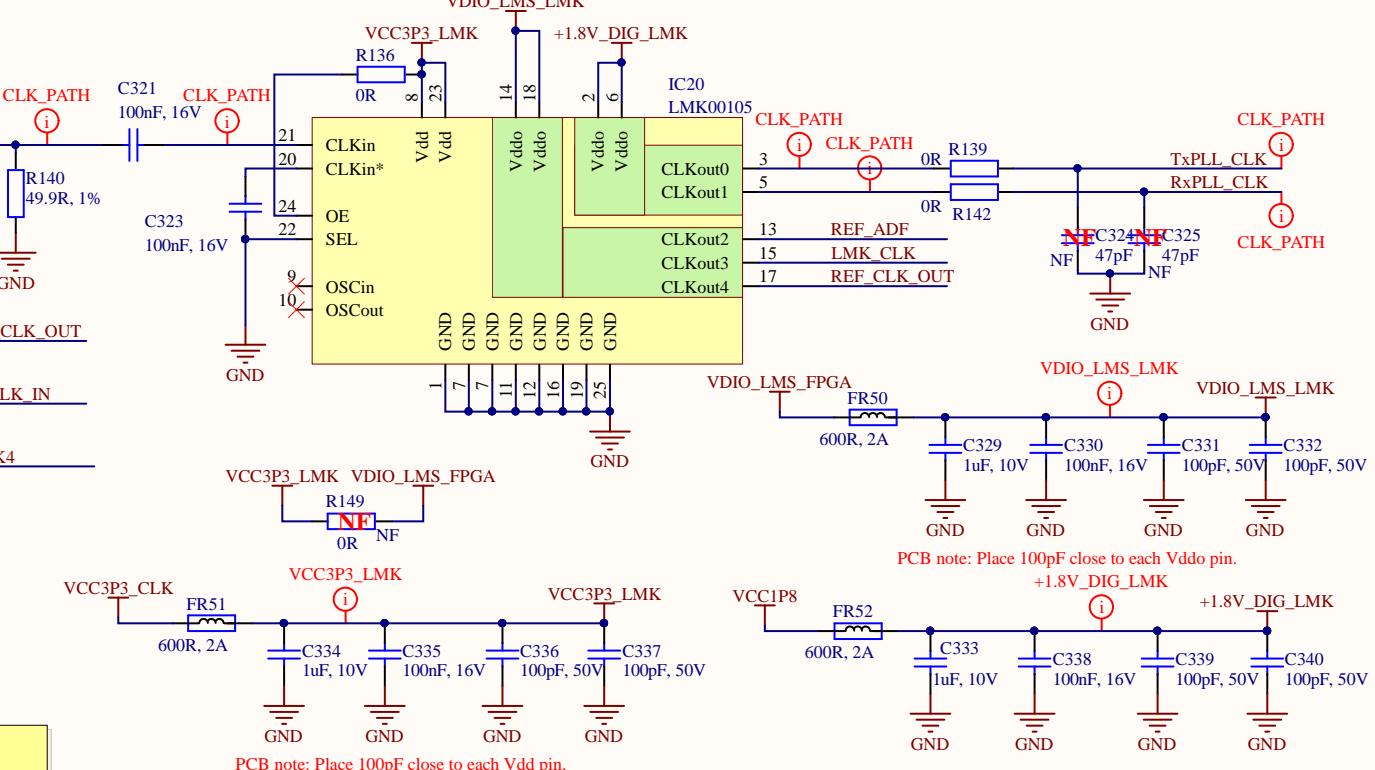
NF elements on sheet: XO1, R141, R143, R144, R145, R146, R147, R148, R149, R151, R155, C324, C325, C328, C341, IC21
Number of NF elements on sheet: 16

Clock circuits

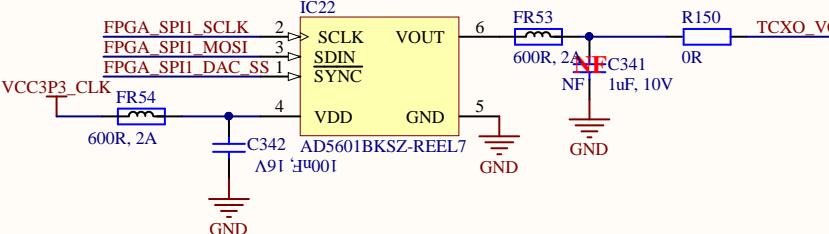
(VC)TCXO



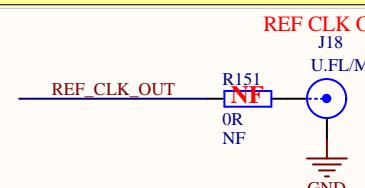
Clock buffer



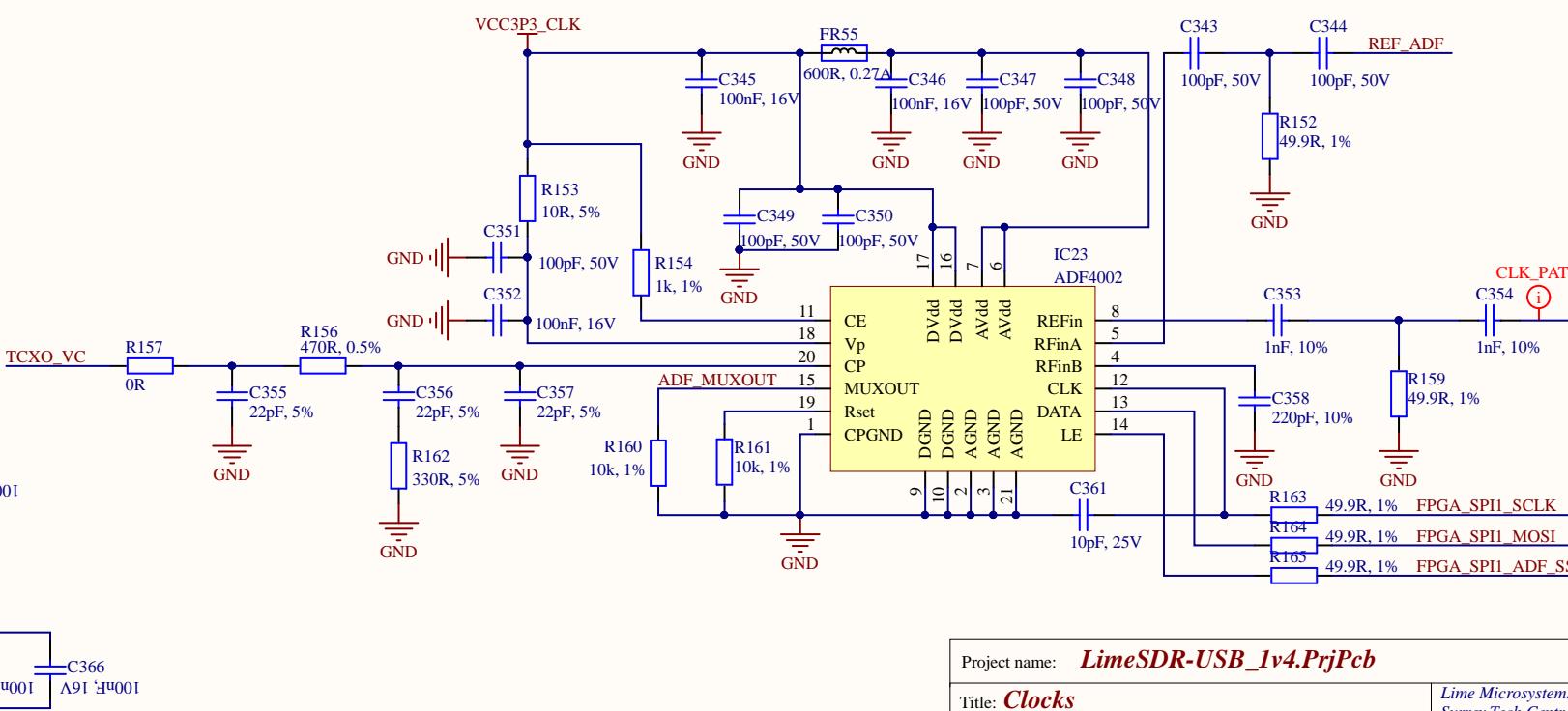
TCXO DAC



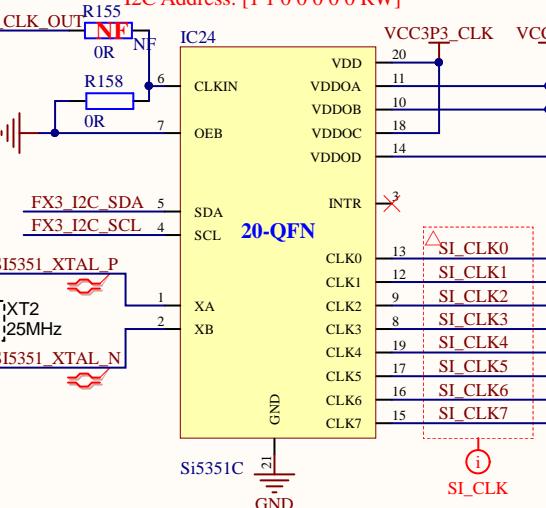
REF CLK OUT



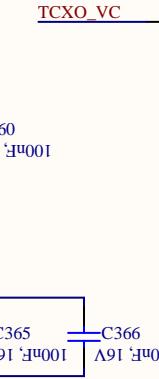
Phase detector



Clock generator



VCC3P3_CLK



Project name: LimeSDR-USB_1v4.PnjPcb

Title: Clocks

Size: A3 Revision: v1.4

Date: 2020-09-30 Time: 14:08:51 Sheet 14 of 15

File: 14_Clocks.SchDoc

Lime Microsystems
Surry Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom



NF elements on sheet: R166, R167, R172, R176, R181, R196, R212, J21, LED3, LED4, LED5, LED6, LEDS1, LEDS2
Number of NF elements on sheet: 14
Total number of NF elements on all sheets: 60

Board power circuits

