Specification and Simulation of Digital Systems

IPcore Mini-assignment

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BRIEF DESCRIPTION

The testbench has three processes: one used to retrieve the input vectors, one to load the expected results and the third to check errors by comparing the expected signal with the real output of the IPcore wrapper (and raise errors using ASSERT). The duration of the testbench is fixed at 180ns; that's because it checks five results with the `ce` signal up and three with the signal down. The test vectors are chosen in order to cover `positive - positive`, `negative - positive`, `positive - negative` and `negative - negative` cases. The latency of the IPcore is set to one, so the `check` process works on the falling edge of the clock. Furthermore, the expected signal on the initial clock cycle is manually set to `all-X` in the second process because the real output is unknown during the first clock cycle.