IoB VGA picture controller

-Electronic Systems of Computers-

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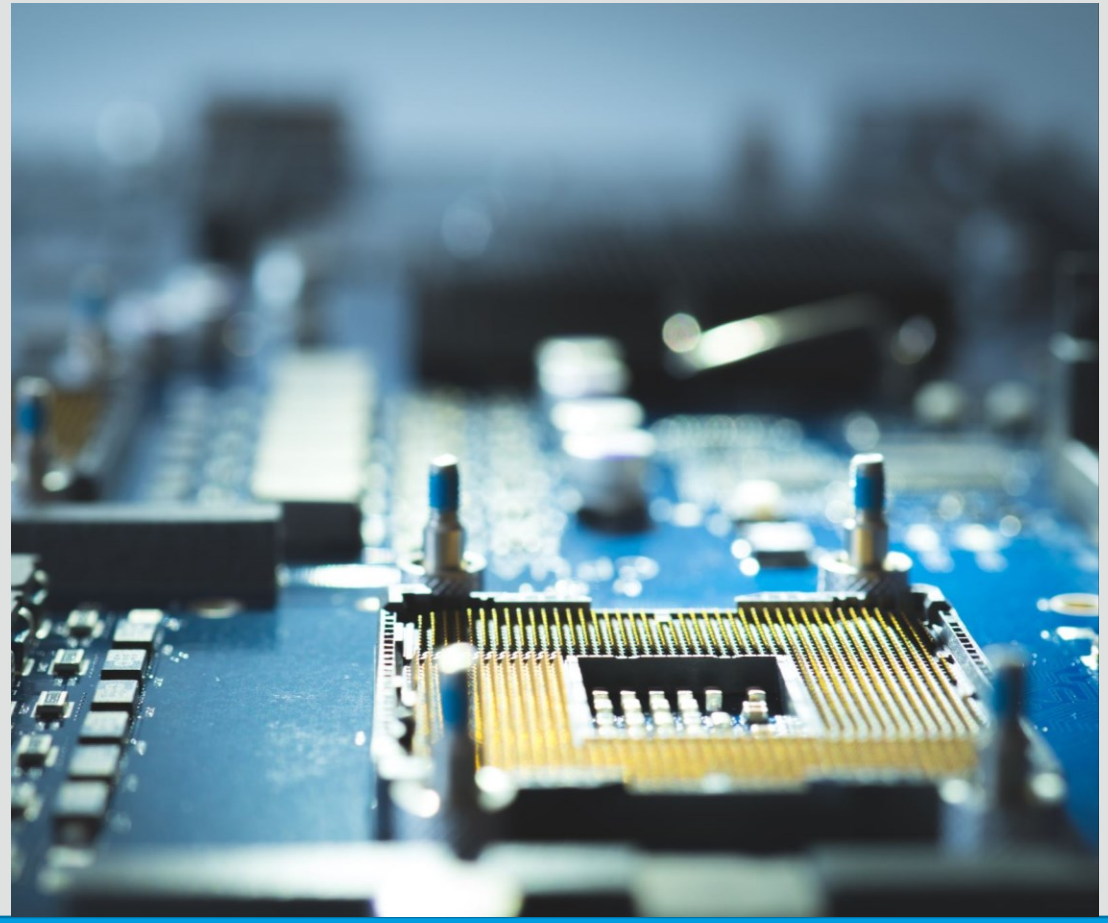
Introduction

- *Uses silicon instead of uP power*
  - *VGA driver*
  - *7-segment driver*
- *Compliant with IoB modules structure*
- *Allows the selection between 2 pre-loaded images*



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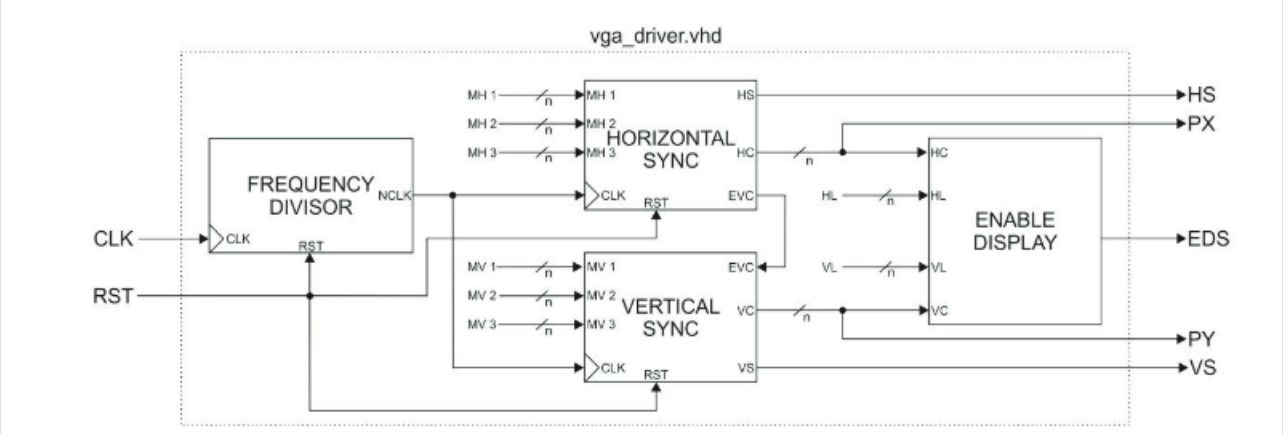
Other works

VGA on FPGA is a vastly known issue commonly used for academic purposes

Ramos-Arregu'n [1] proposes a modification to the architecture presented by Digilent for its development boards by generating the pixel coordinate and a pixel enable signal used to display it or not.

The main flaw detected is the generation of a secondary clock in the system that can cause clock domain crossing or delays.



1. Ramos-Arregu'n, C. A., Morales, J. C. M., Ramos-Arregu'n, J. M., Pedraza-Ortega, J. C., Tovar-Arriaga, S., Fernandez, M. A. A., & Rangel-Magdaleno, J. de J. (2012). FPGA Open Architecture Design for a VGA Driver. Procedia Technology, 3, 324–333. https://doi.org/10.1016/J.PROTCY.2012.03.035

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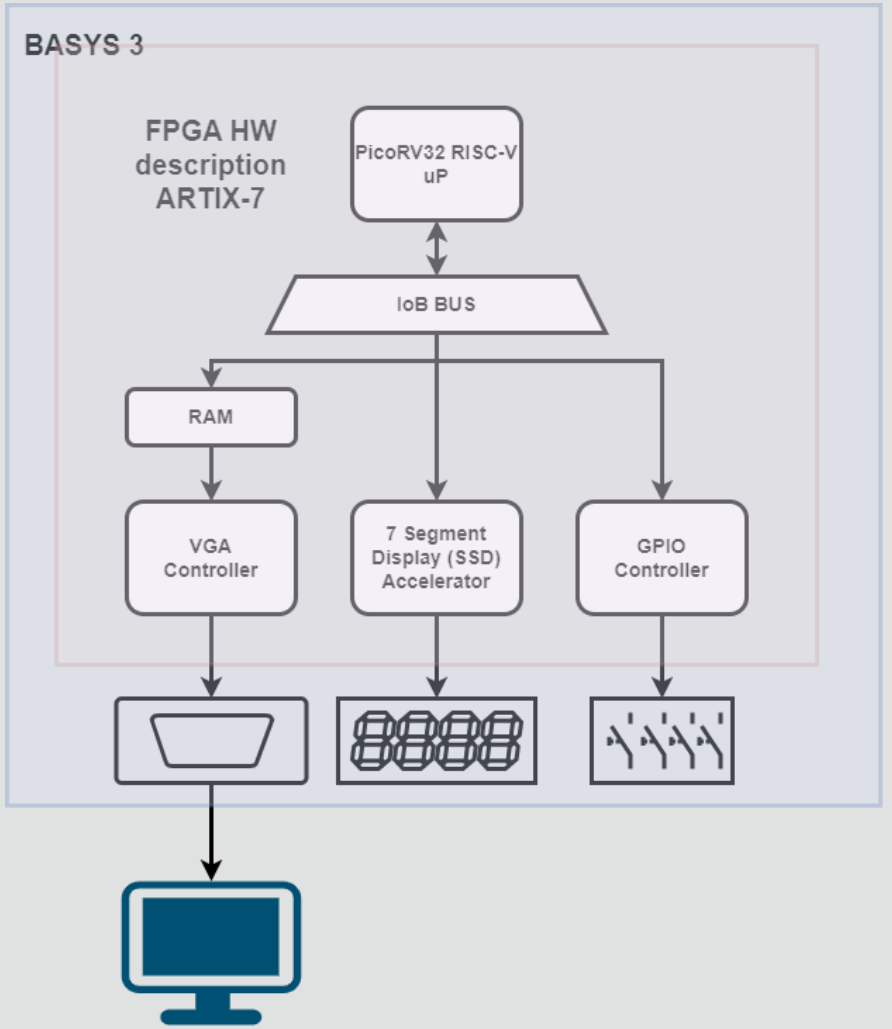
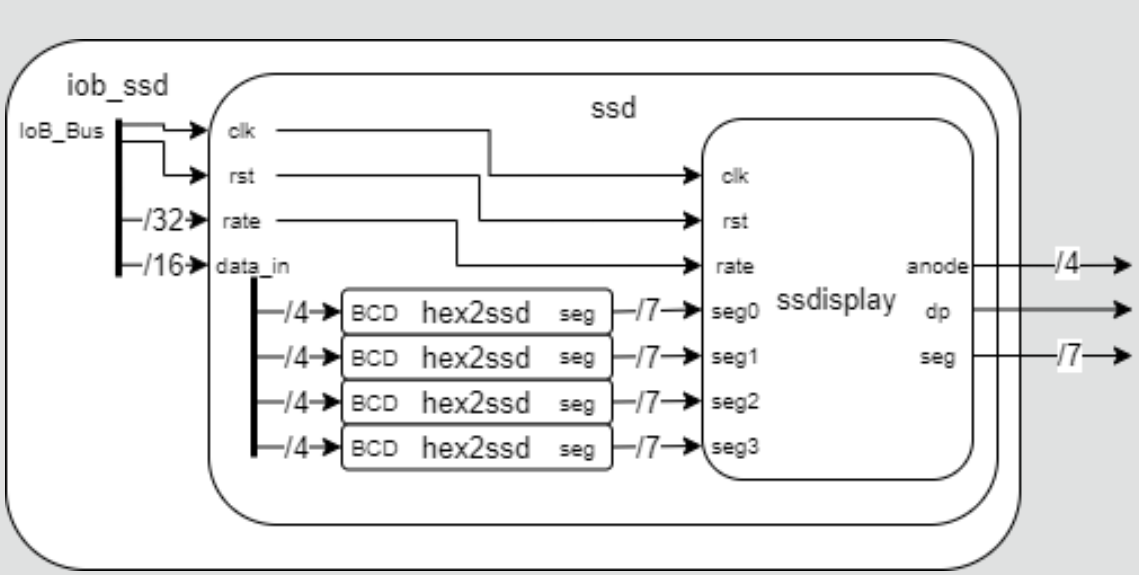
Top system organization

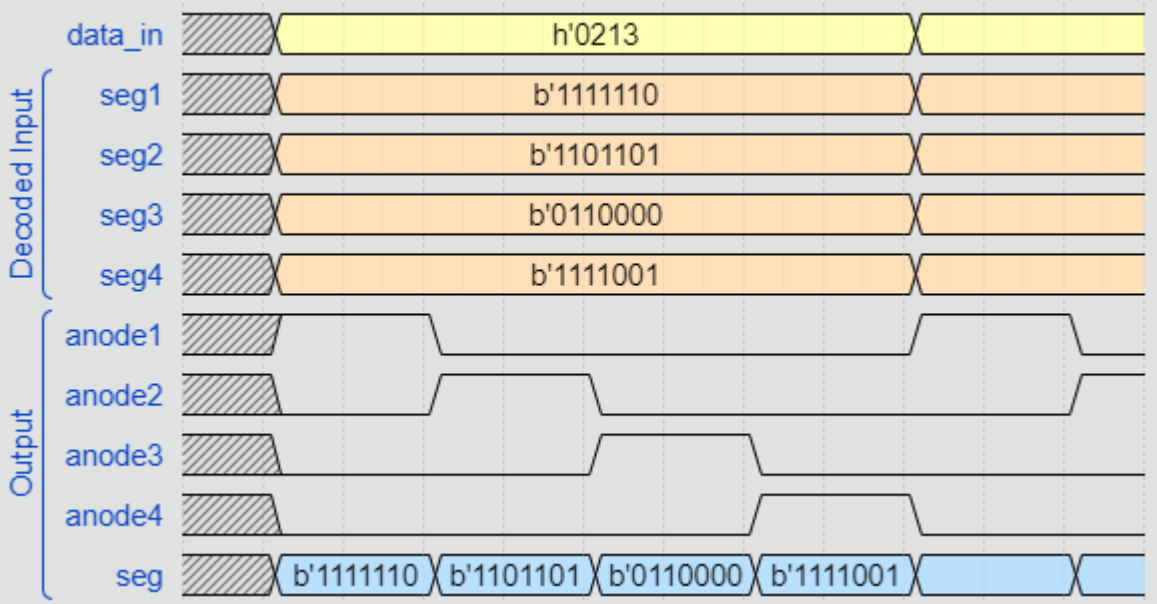
Developed submodules:

- *VGA Controller*
- *7 Segment Display Controller*
- *Image memory*



Seven Segments Controller (SSD)

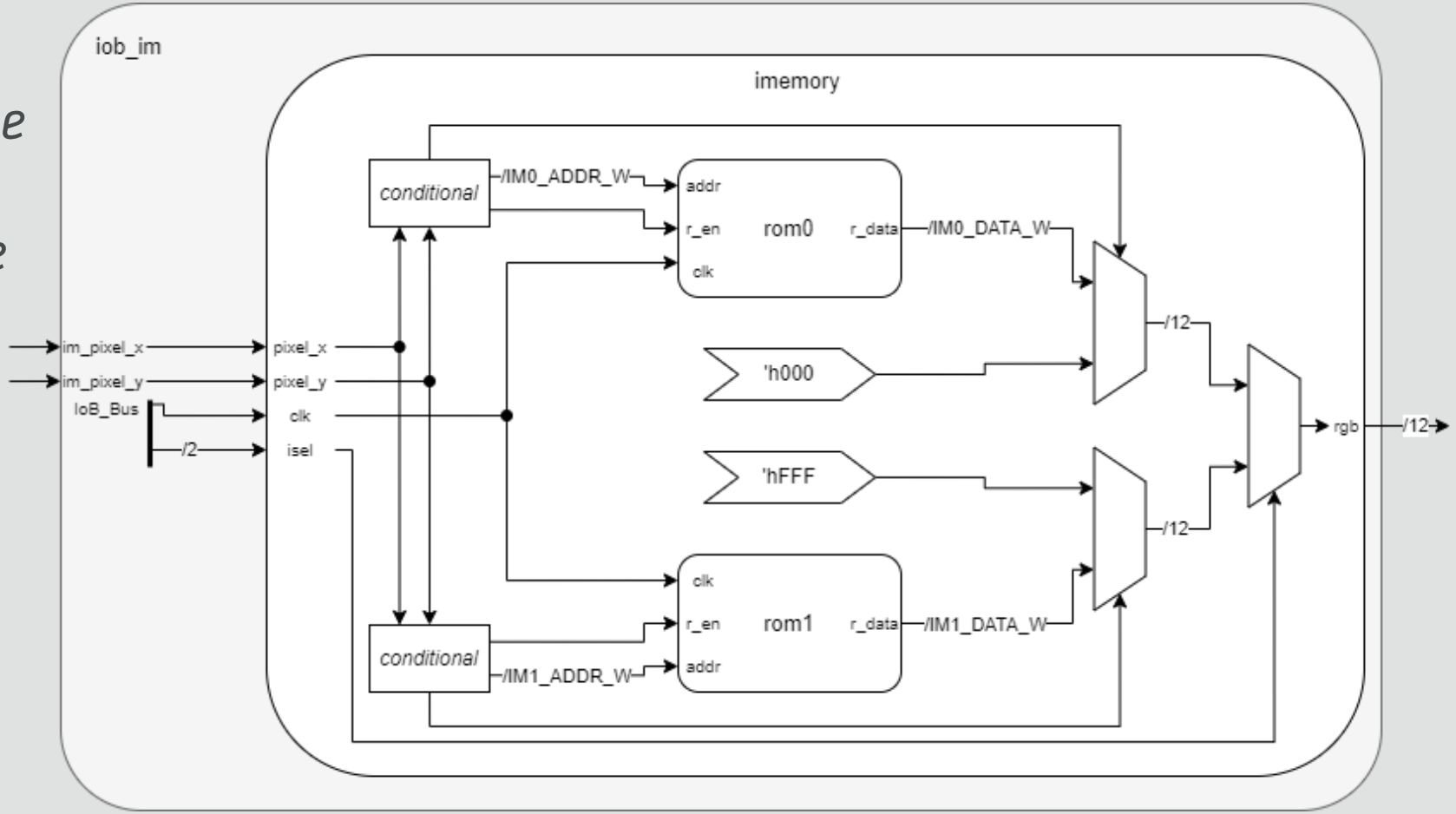




- *Software functions*
  - *ssd_init: sets the base address and the refresh frequency*
  - *ssd_set_number: writes to the software-accessible register 'data_in'*

Image Memory

- *Software functions*
  - *im_init: sets the base address*
  - *im_set: writes to the software-accessible register 'isel'*



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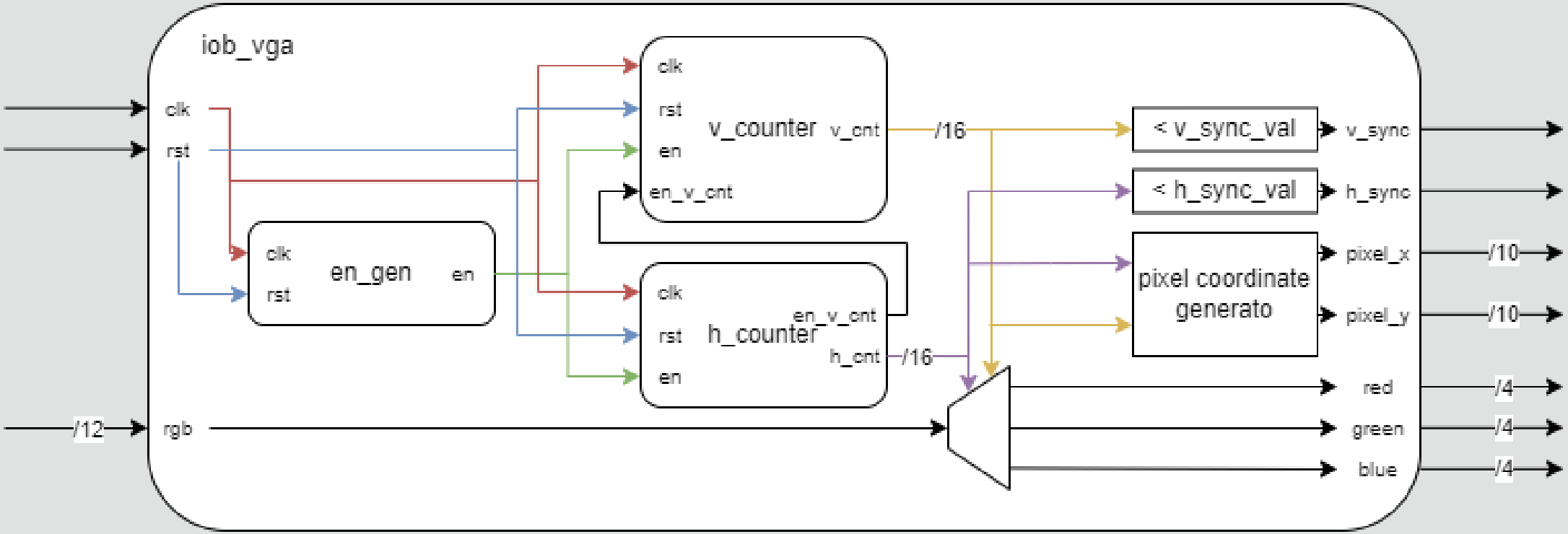
VGA



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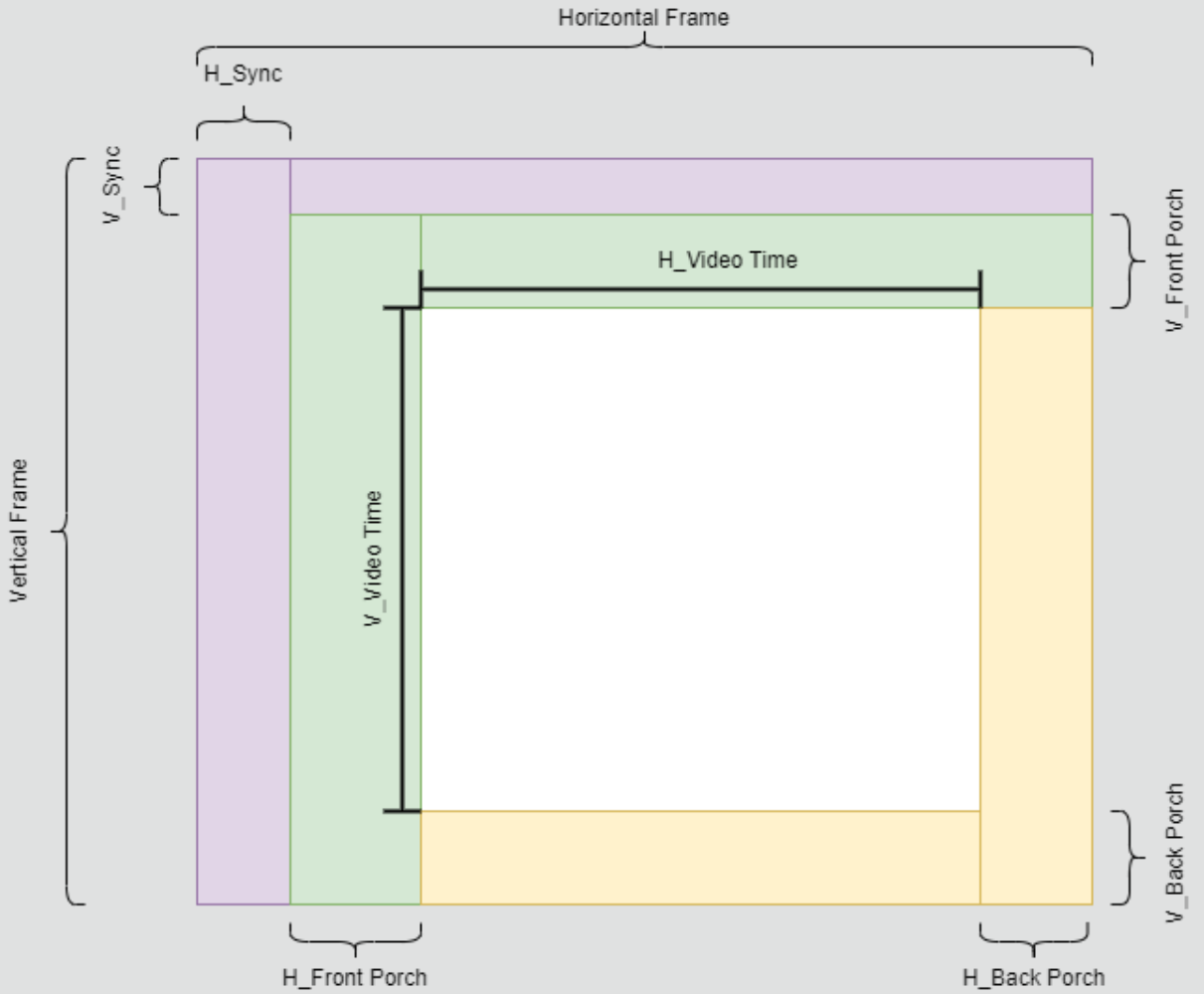
VGA

The module complies with the VESA VGA standards as follows:

Constants	Horizontal	Vertical
Refresh Rate	@60Hz	
Image Clock	@25MHz	
Total Frame	800	525
Sync Pulse	96	2
Front Porch	16	10
Visible Area	640	480
Back Porch	48	33



Software

- *Simple commuter.*
  - *Detects changes in the inputs and selects a corresponding image.*

```
while(1) {
    g_input = gpio_get();
    if(g_input != g_input_old) {
      if(g_input == 0){
           im_set(0);
           ssd_set_number(0x0001);
           printf("\nImage: 0\n");
      } else {
           im_set(1);
           ssd_set_number(0x0002);
           printf("\nImage: 1\n");
      }
      g_input_old = g_input;
    }
  }
```

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Demonstration

The system has a general testbench.

All the submodules have their own dedicated testbench.

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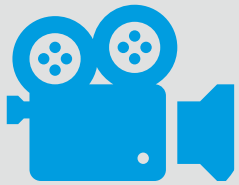
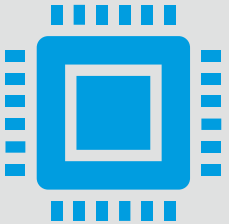
Conclusions



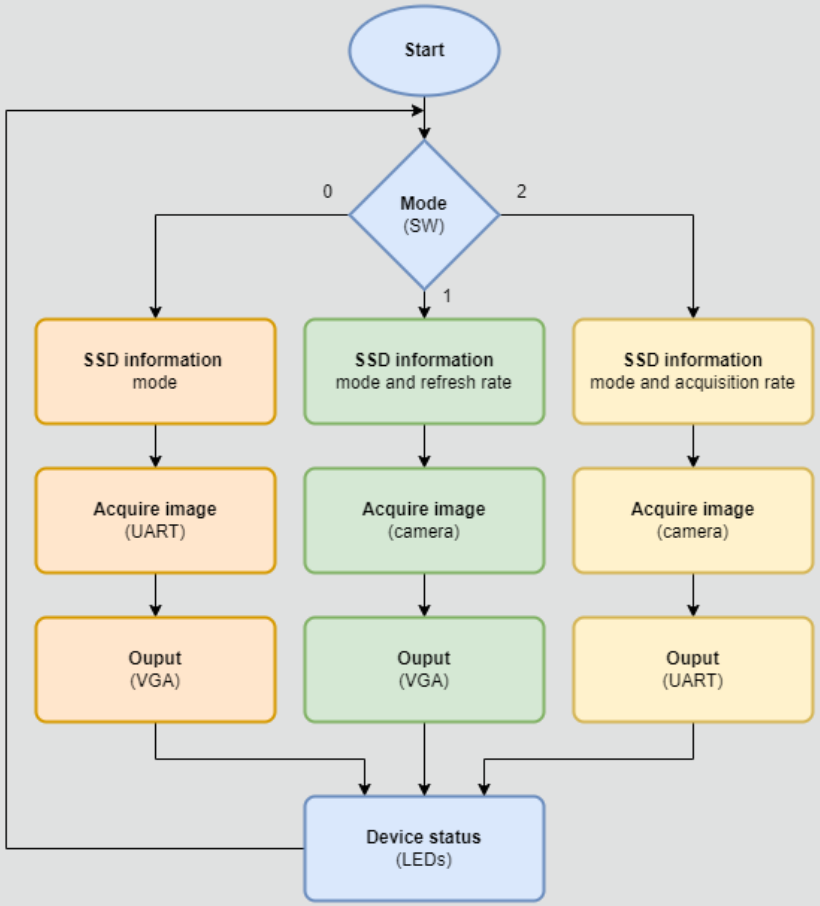
The greatest difficulty for video management in IoB_SoC is the storage space available, severely capping the system's capabilities.

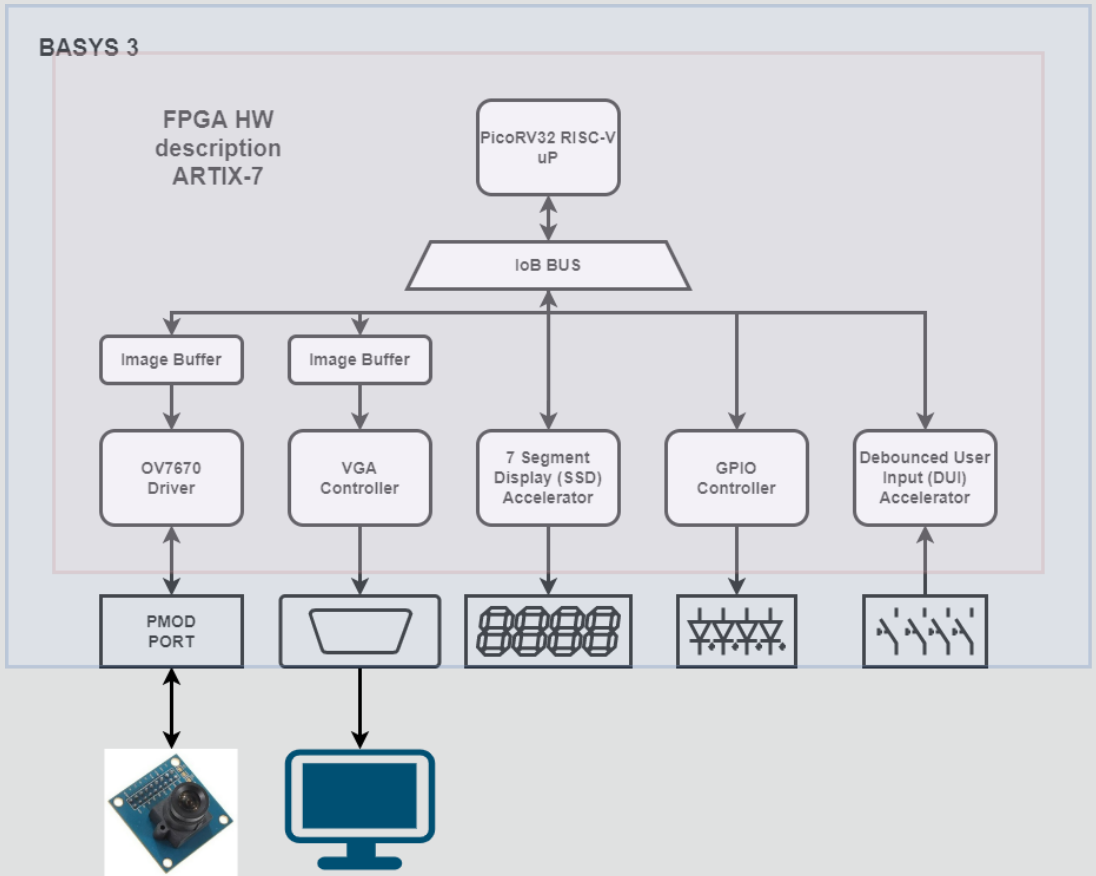
To generate video, it is suggested to use external memory or buffer a segment of the image in a dual-clock FIFO.



It is demonstrated with this application that the uC serves a better purpose in managing IP than complex computing.

Future works





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Questions?