Ex 12

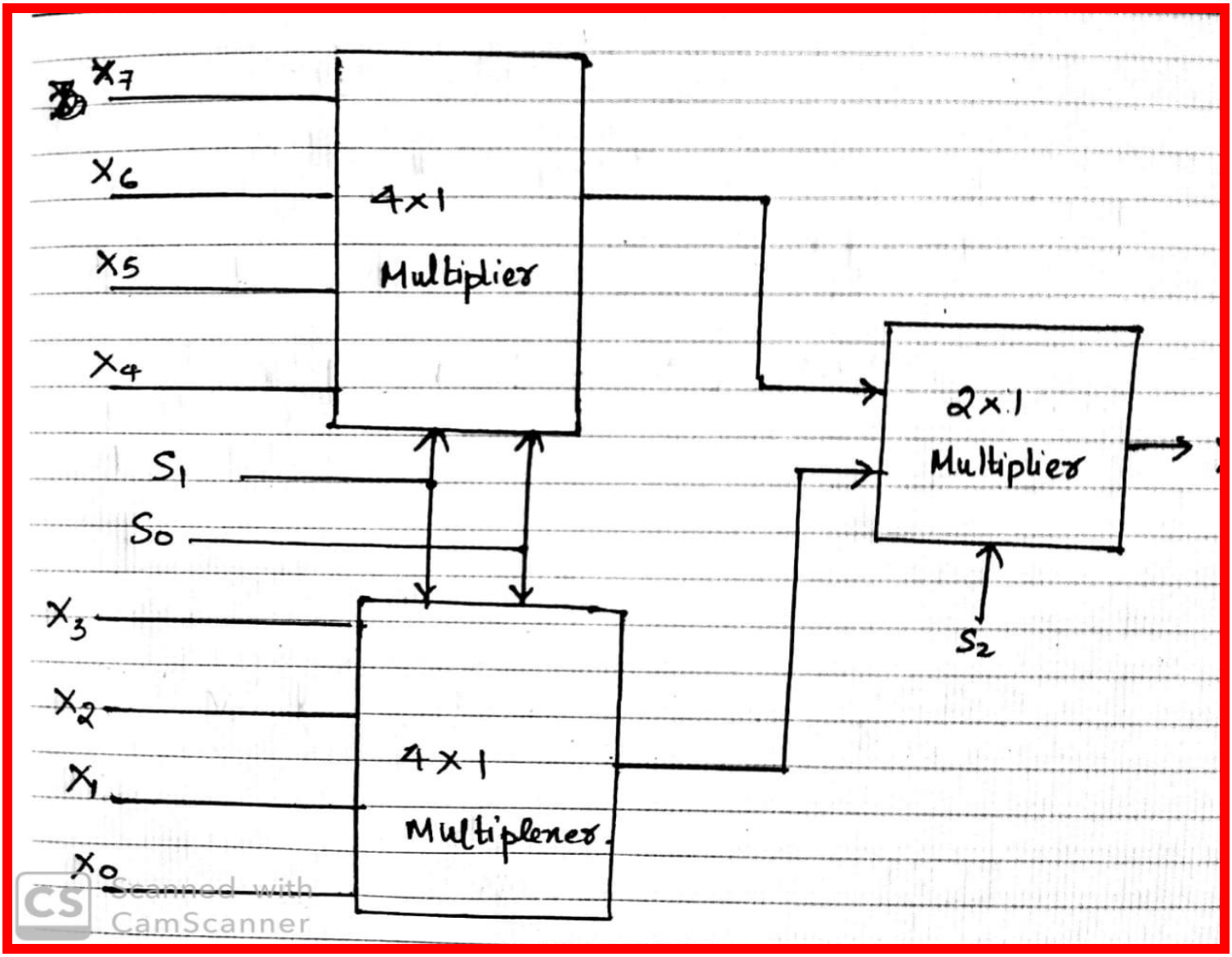
Implementation of Higher order MUX using Lower order.

Nihal Shah Parekkattil
RA1911003010868

❖ **AIM :** To implement :

1. 8:1 using 4:1
2. 16:1 using 8:1
3. 16:1 using 4:1

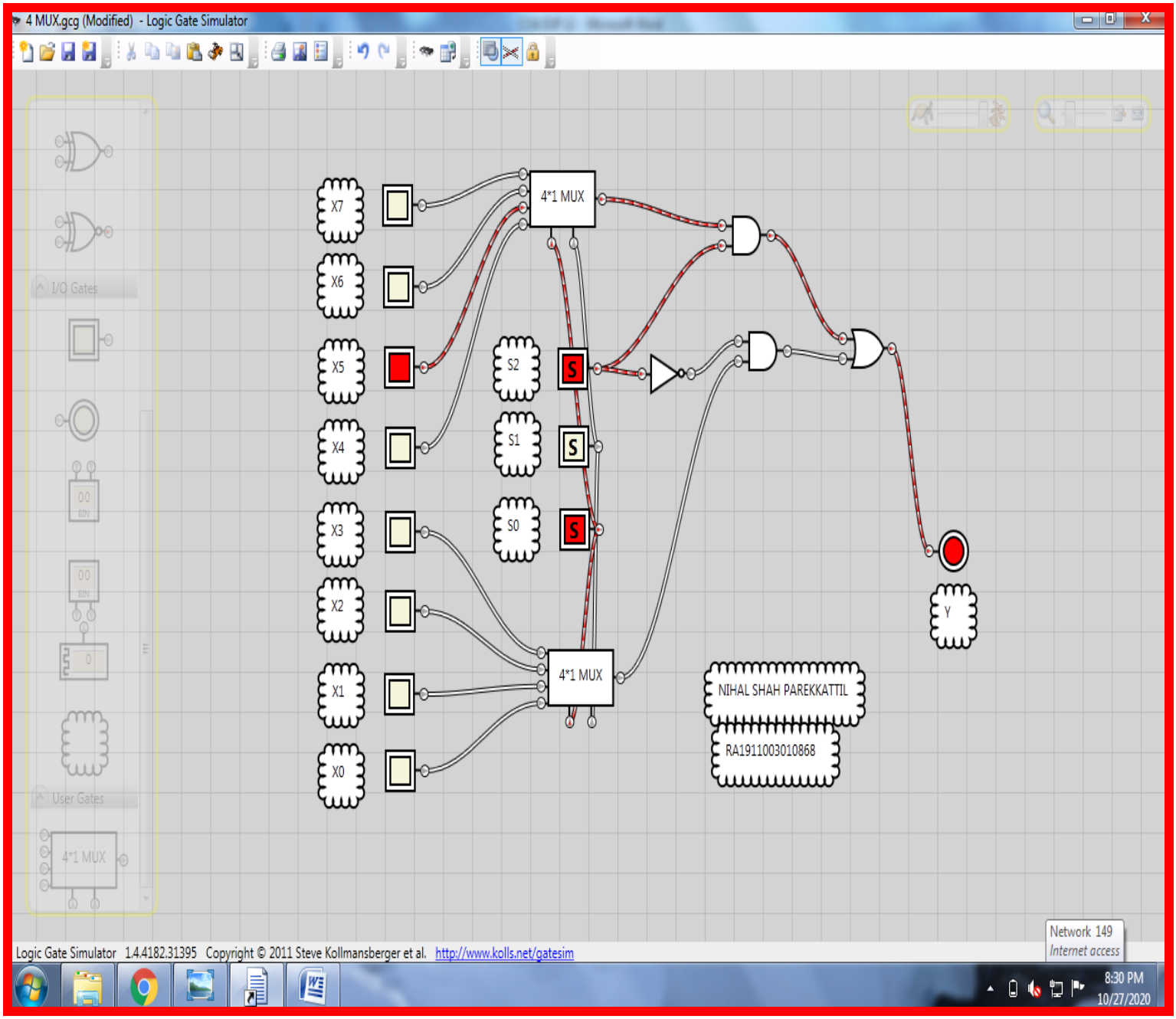
- **Implementation of 8:1 using 4:1**



Truth table

Select lines			Output
S_2	S_1	S_0	Y
0	0	0	X_0
0	0	1	X_1
0	1	0	X_2
0	1	1	X_3
1	0	0	X_4
1	0	1	X_5
1	1	0	X_6
1	1	1	X_7

Truth table of 8*1 MUX


4 MUX.gcg (Modified) - Logic Gate Simulator
I/O Gates
User Gates
4*1 MUX
X7
X6
X5
X4
X3
X2
X1
X0
S2
S1
S0
4*1 MUX
Y
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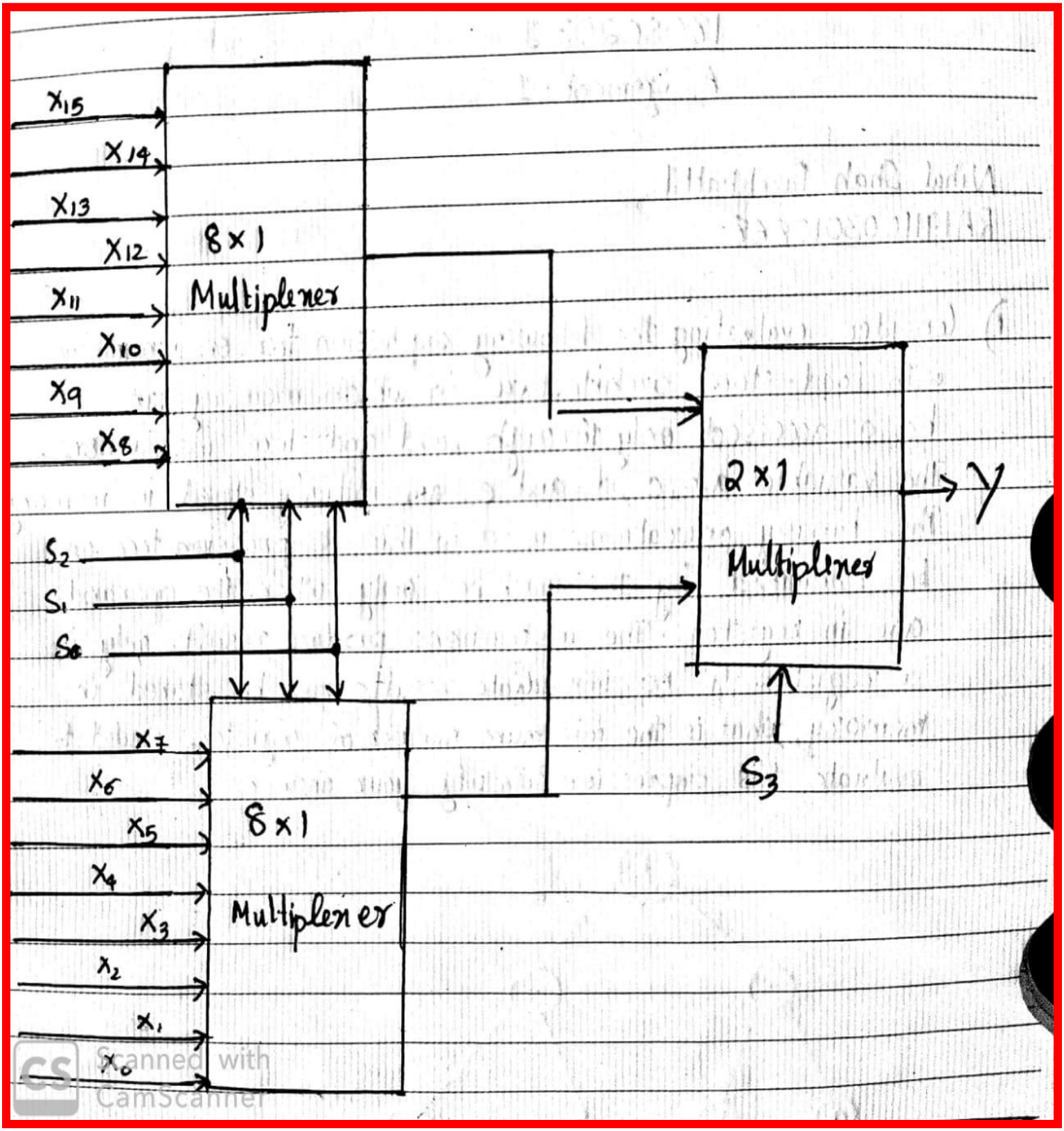
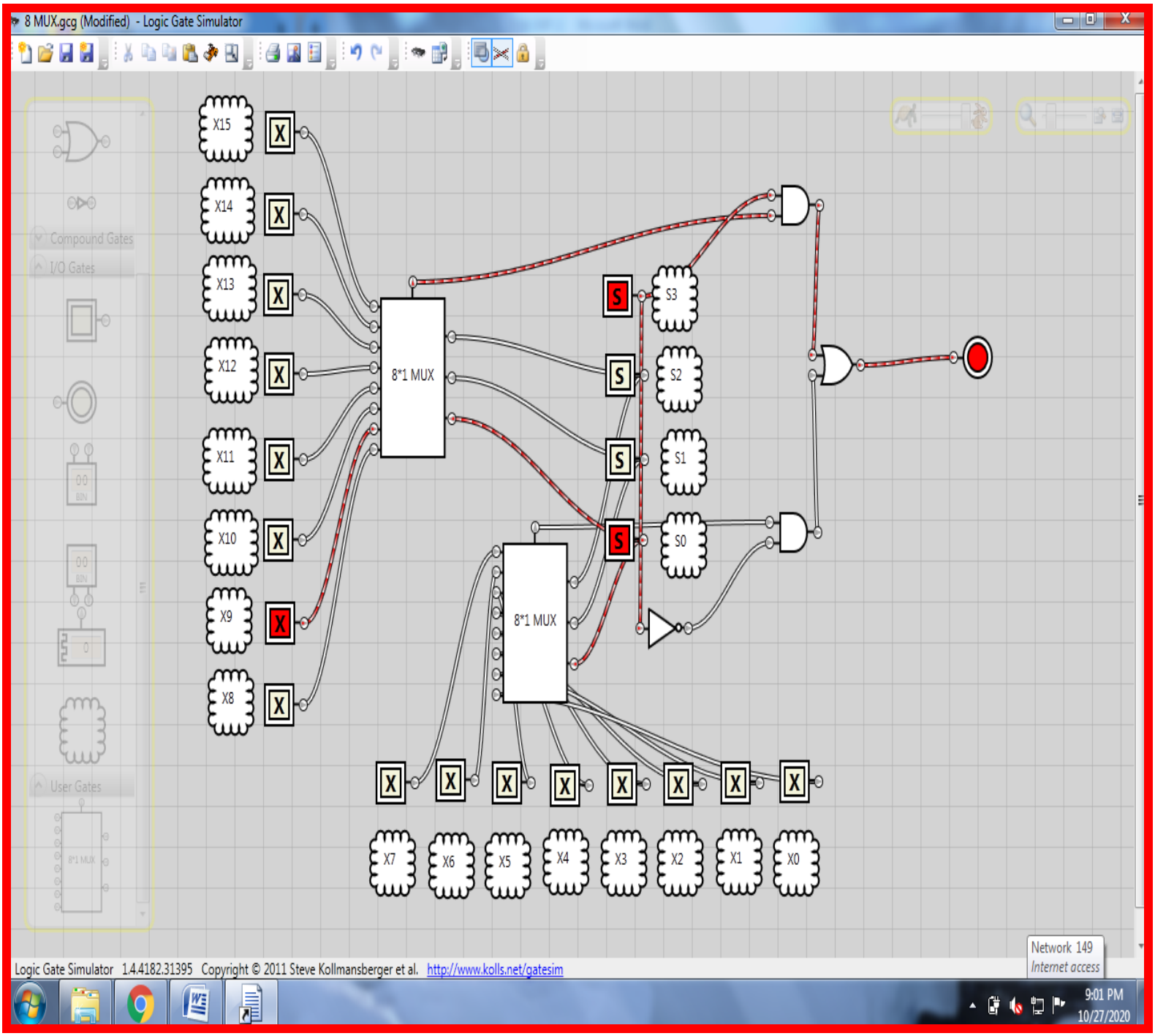
				Output
S_3	S_2	S_1	S_0	Y
0	0	0	0	X_0
0	0	0	1	X_1
0	0	1	0	X_2
0	0	1	1	X_3
0	1	0	0	X_4
0	1	0	1	X_5
0	1	1	0	X_6
0	1	1	1	X_7
1	0	0	0	X_8
1	0	0	1	X_9
1	0	1	0	X_{10}
1	0	1	1	X_{11}
1	1	0	0	X_{12}
1	1	0	1	X_{13}
1	1	1	0	X_{14}
1	1	1	1	X_{15}

Truth table of 16*1 MUX

- **Implementation of 16:1 using 8:1**




8 MUX.gcg (Modified) - Logic Gate Simulator
X15
X14
X13
X12
X11
X10
X9
X8
8*1 MUX
S3
S2
S1
S0
8*1 MUX
X7
X6
X5
X4
X3
X2
X1
X0
Compound Gates
I/O Gates
User Gates
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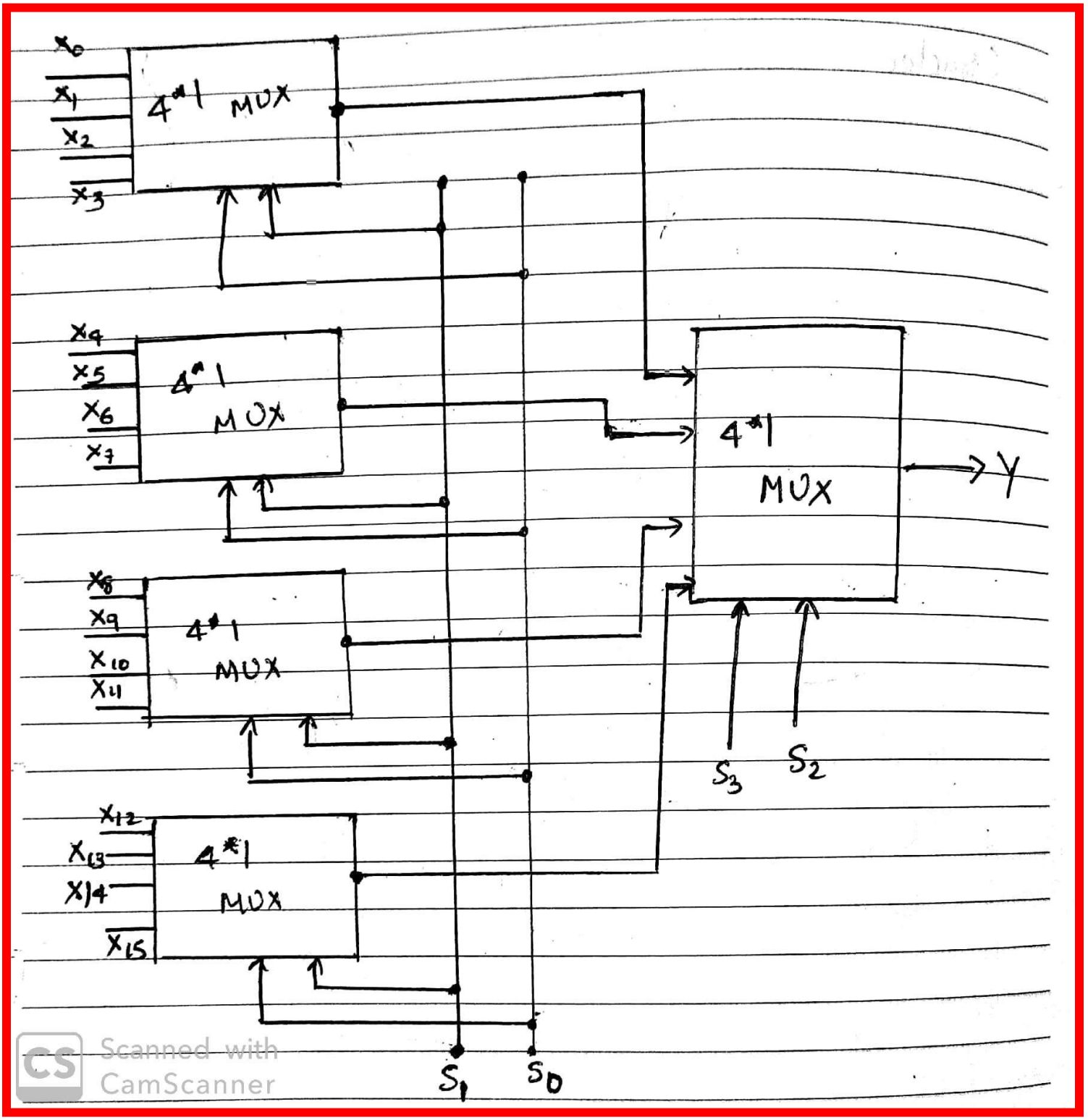
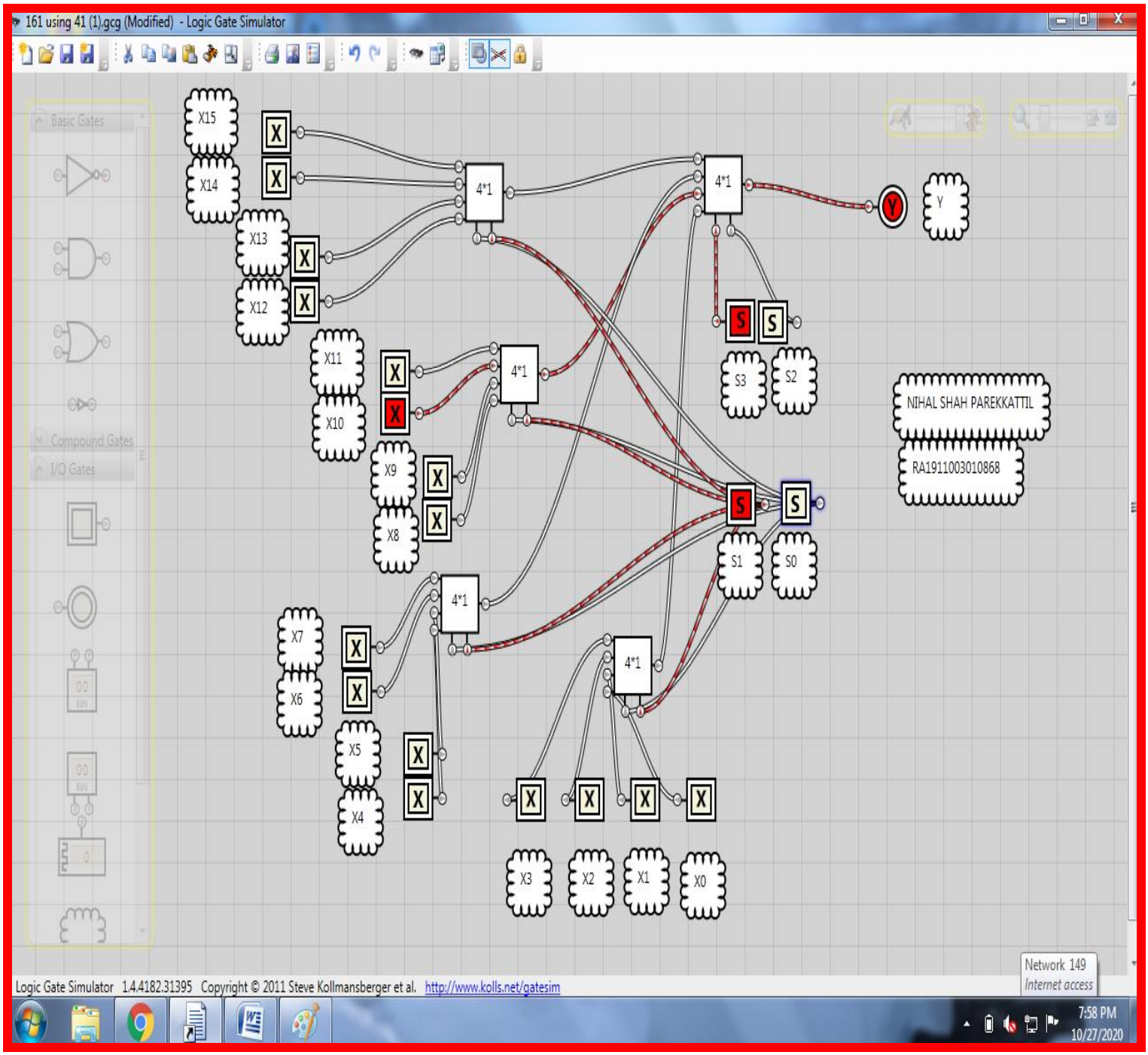
- **Implementation of 16:1 using 4:1**




161 using 41 (1).gcg (Modified) - Logic Gate Simulator
Basic Gates
Compound Gates
I/O Gates
X15
X14
X13
X12
X11
X10
X9
X8
X7
X6
X5
X4
X3
X2
X1
X0
4*1
4*1
4*1
4*1
4*1
Y
Y
S
S
S3
S2
S
S
S1
S0
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