POWER9

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POWER Systems, IBM Systems

IBM

Recent and Future
POWER Processor Roadmap

POWER7
45 nm
2010

POWER7+
32 nm
2012

POWER8 Family
22nm
2014 – 2016

POWER9 Family
14nm
2H17 – 2H18+

POWER10 Family
2020+
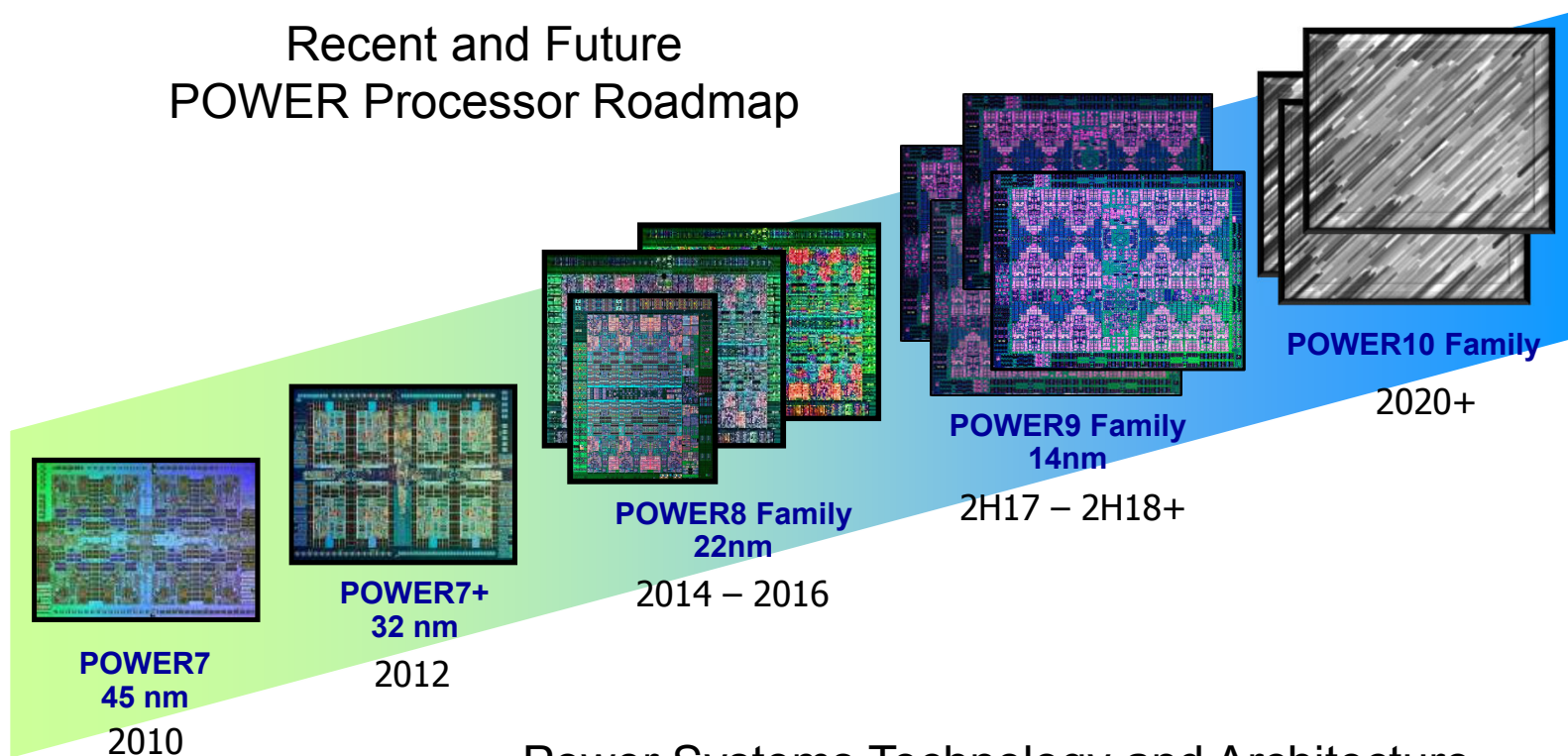
Power Systems Technology and Architecture
Leveraging the economics of the New Era

POWER9 Family – Deep Workload Optimizations

Emerging Analytics, AI, Cognitive
- New core for stronger thread performance
- Delivers 2x compute resource per socket
- Built for acceleration – OpenPOWER solution enablement

Technical / HPC
- Highest bandwidth GPU attach
- Advanced GPU/CPU interaction and memory sharing
- High bandwidth direct attach memory

Cloud / HSDC
- Power / Packaging / Cost optimizations for a range of platforms
- Superior virtualization features: security, power management, QoS, interrupt
- State of the art IO technology for network and storage performance

Enterprise
- Large, flat, Scale-Up Systems
- Buffered memory for maximum capacity
- Leading RAS
- Improved caching

New POWER9 Cores

## Optimized for Stronger Thread Performance and Efficiency

- Increased execution bandwidth efficiency for a range of workloads including commercial, cognitive and analytics
- Sophisticated instruction scheduling and branch prediction for unoptimized applications and interpretive languages
- Adaptive features for improved efficiency and performance especially in lower memory bandwidth systems

Available with SMT8 or SMT4 Cores

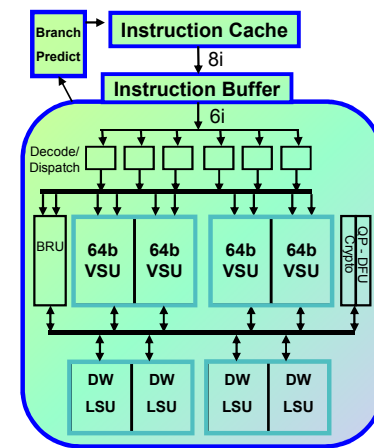8 or 4 threaded core built from modular execution slices

POWER9 SMT8 Core
- PowerVM Ecosystem Continuity
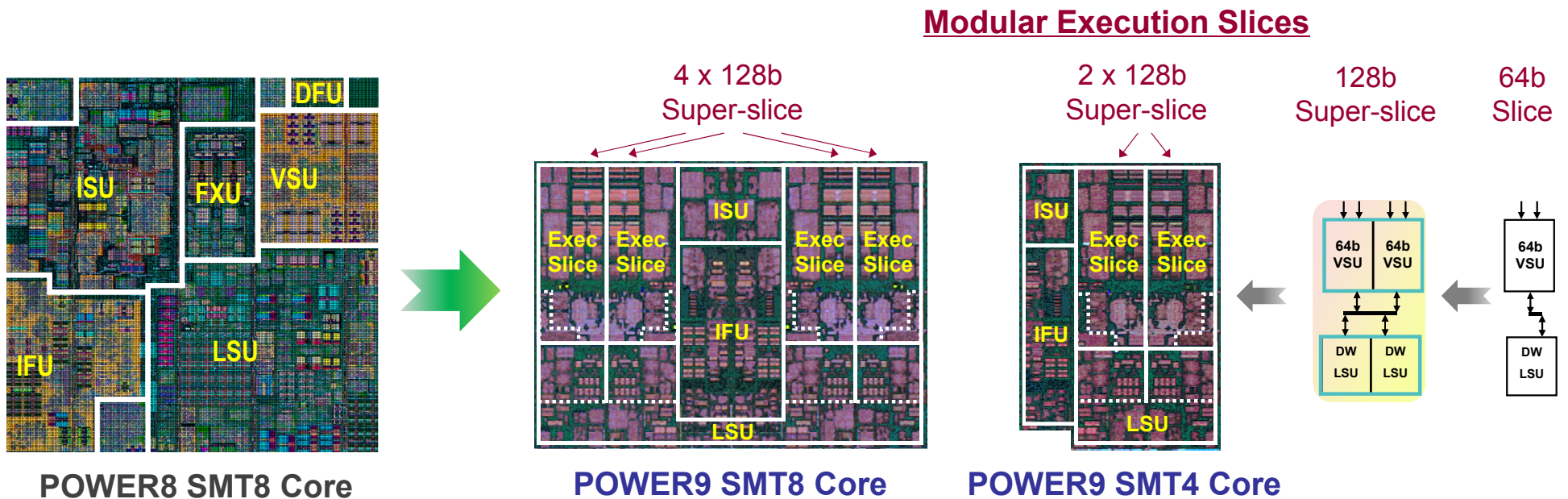- Strongest Thread
- Optimized for Large Partitions
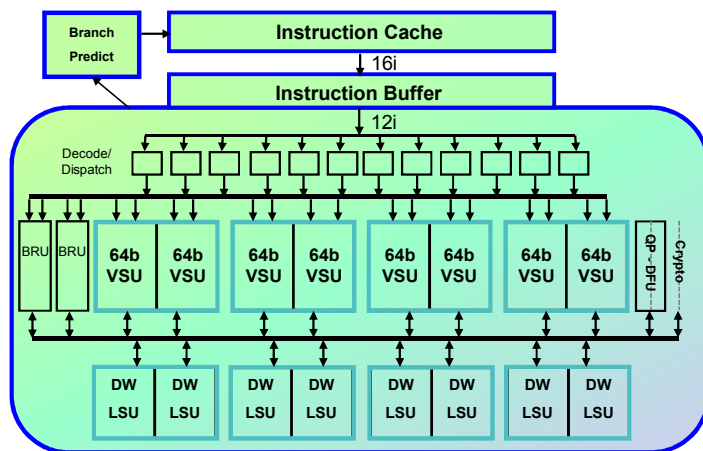
POWER9 SMT4 Core
- Linux Ecosystem Focus
- Core Count / Socket
- Virtualization Granularity

SMT8 Core

SMT4 Core

POWER9 Core Execution Slice Microarchitecture

Modular Execution Slices

4 x 128b Super-slice   2 x 128b Super-slice   128b Super-slice   64b Slice

POWER8 SMT8 Core   POWER9 SMT8 Core   POWER9 SMT4 Core

Re-factored Core Provides Improved Efficiency & Workload Alignment

- Enhanced pipeline efficiency with modular execution and intelligent pipeline control
- Increased pipeline utilization with symmetric data-type engines: Fixed, Float, 128b, SIMD
- Shared compute resource optimizes data-type interchange

POWER9 Core Pipeline Efficiency

Shorter Pipelines with Reduced Disruption

### Improved application performance for modern codes

- **Shorten fetch to compute by 5 cycles**
- **Advanced branch prediction**

Higher performance and pipeline utilization

- **Improved instruction management**
  - Removed instruction grouping and reduced cracking
  - Enhanced instruction fusion
  - Complete up to 128 (64 – SMT4 Core) instructions per cycle

Reduced latency and improved scalability

- **Local pipe control of load/store operations**
  - Improved hazard avoidance
  - Local recycles – reduced hazard disruption
  - Improved lock management

POWER8 Pipeline

Fetch to Compute Reduced by 5 cycles

POWER9 Pipeline

Reduced Hazard Disruption

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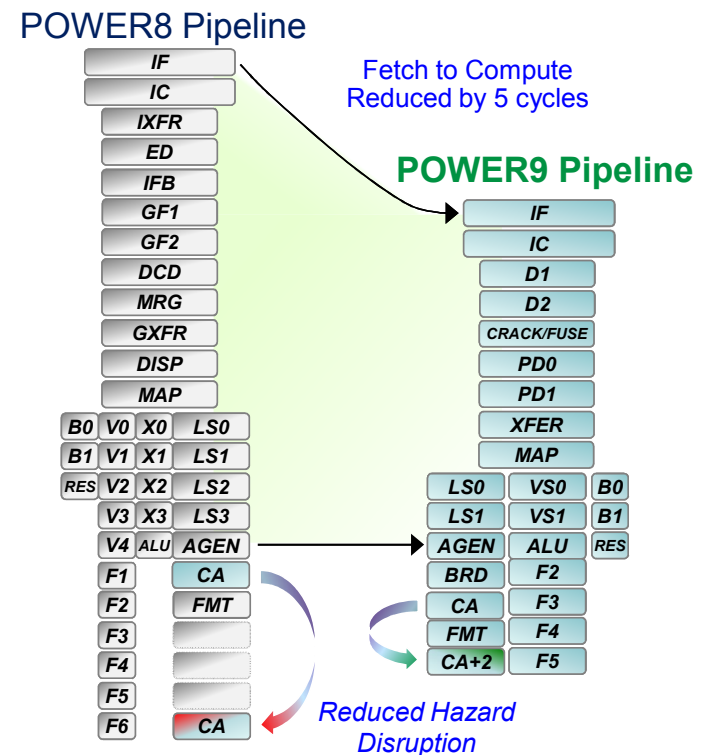
SMT4 Core Resources

Fetch / Branch
- 32kB, 8-way Instruction Cache
- 8 fetch, 6 decode
- 1x branch execution

Slices issue VSU and AGEN
- 4x scalar-64b / 2x vector-128b
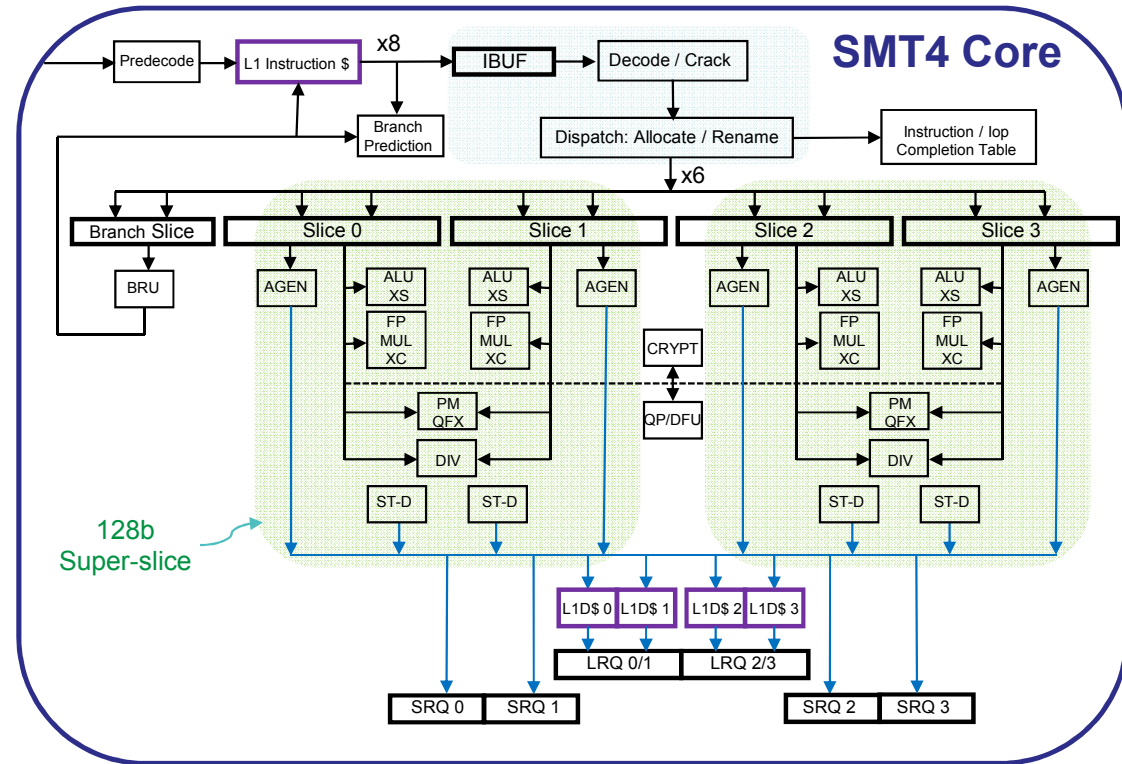- 4x load/store AGEN

Vector Scalar Unit (VSU) Pipes
- 4x ALU + Simple (64b)
- 4x FP + FX-MUL + Complex (64b)
- 2x Permute (128b)
- 2x Quad Fixed (128b)
- 2x Fixed Divide (64b)
- 1x Quad FP & Decimal FP
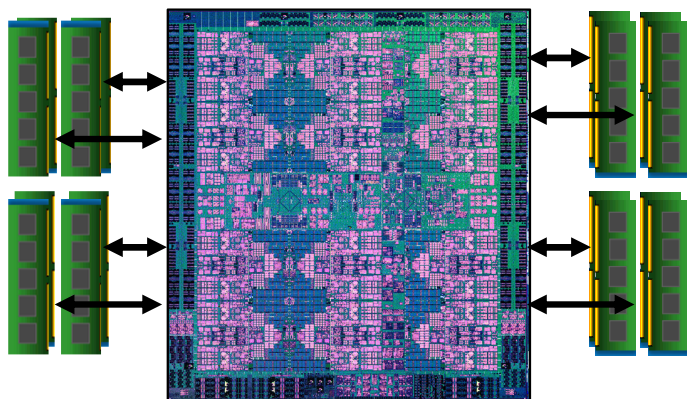- 1x Cryptography

Load Store Unit (LSU) Slices
- 32kB, 8-way Data Cache
- Up to 4 DW load or store

Symmetric Engines Per Data-Type for
Higher Performance on Diverse Workloads
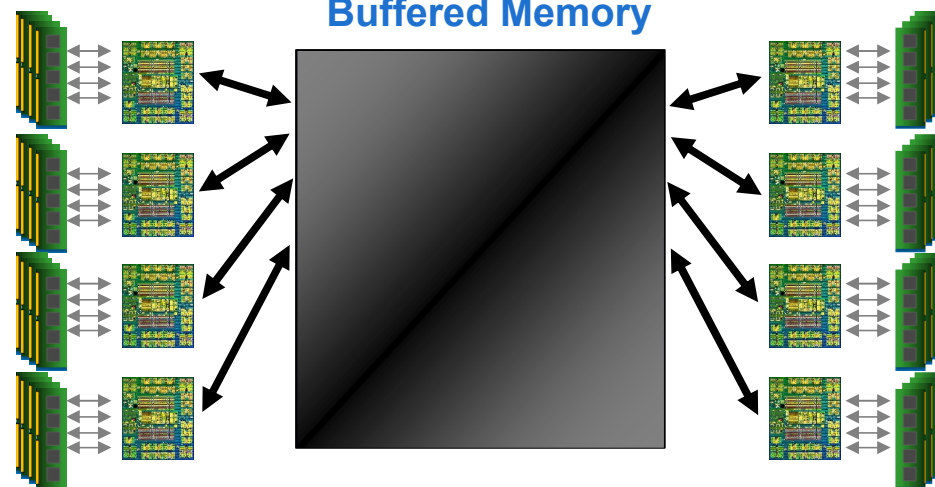

Efficient Cores Deliver 2x Compute Resource per Socket

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POWER9 – Dual Memory Subsystems

Scale Out
Direct Attach Memory

Scale Up
Buffered Memory

8 Direct DDR4 Ports

8 Buffered Channels

- Up to 120 GB/s of sustained bandwidth
- Low latency access
- Commodity packaging form factor
- Adaptive 64B / 128B reads

- Up to 230GB/s of sustained bandwidth
- Extreme capacity – up to 8TB / socket
- Superior RAS with chip kill and lane sparing
- Compatible with POWER8 system memory
- Agnostic interface for alternate memory innovations

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## New Core Microarchitecture

- Stronger thread performance
- Efficient agile pipeline
- POWER ISA v3.0

Enhanced Cache Hierarchy

- 120MB NUCA L3 architecture
- 12 x 20-way associative regions
- Advanced replacement policies
- Fed by 7 TB/s on-chip bandwidth

Cloud + Virtualization Innovation

- Quality of service assists
- New interrupt architecture
- Workload optimized frequency
- Hardware enforced trusted execution
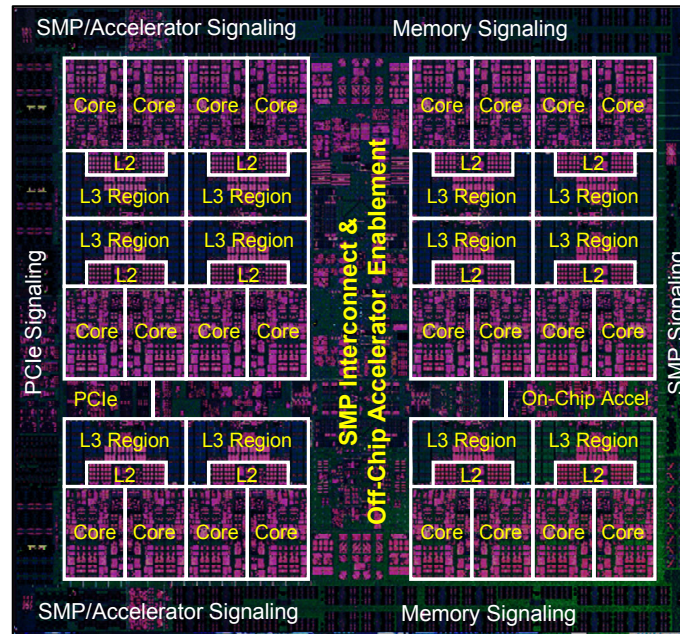
14nm finFET Semiconductor Process

- Improved device performance and reduced energy
- 17 layer metal stack and eDRAM
- 8.0 billion transistors

Leadership Hardware Acceleration Platform

- Enhanced on-chip acceleration
- Nvidia NVLink 2.0: High bandwidth and advanced new features (25G)
- CAPI 2.0: Coherent accelerator and storage attach (PCIe G4)
- New CAPI: Improved latency and bandwidth, open interface (25G)

State of the Art I/O Subsystem

- PCIe Gen4 – 48 lanes

High Bandwidth Signaling Technology

- 16 Gb/s interface
    – Local SMP
- 25 Gb/s Common Link interface
    – Accelerator, remote SMP

POWER9 Processor Family

Four targeted implementations

**SMP scalability / Memory subsystem**

Core Count / Size

|	**SMT4 Core** **24 SMT4 Cores / Chip** Linux Ecosystem Optimized	**SMT8 Core** **12 SMT8 Cores / Chip** PowerVM Ecosystem Continuity
Scale-Out – 2 Socket Optimized **Robust 2 socket SMP system** **Direct Memory Attach** • Up to 8 DDR4 ports • Commodity packaging form factor		
Scale-Up – Multi-Socket Optimized **Scalable System Topology / Capacity** • Large multi-socket **Buffered Memory Attach** • 8 Buffered channels		
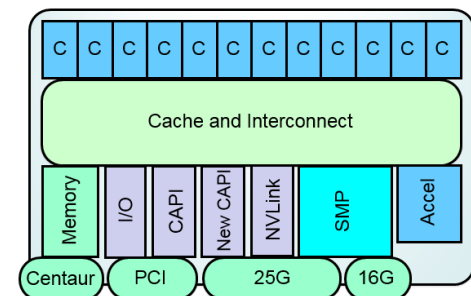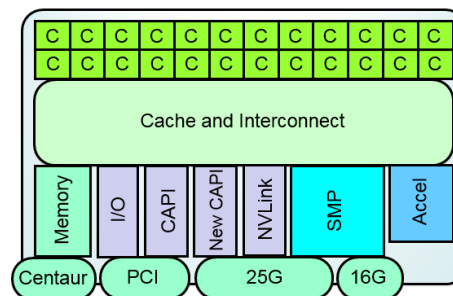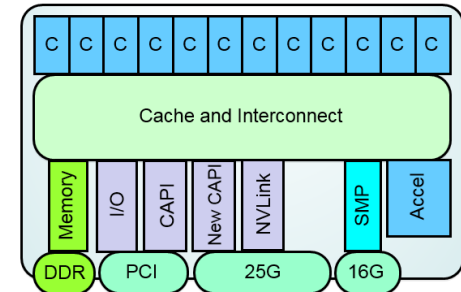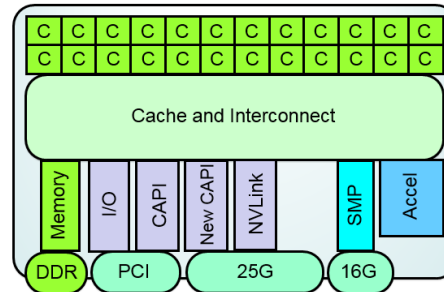
Socket Performance
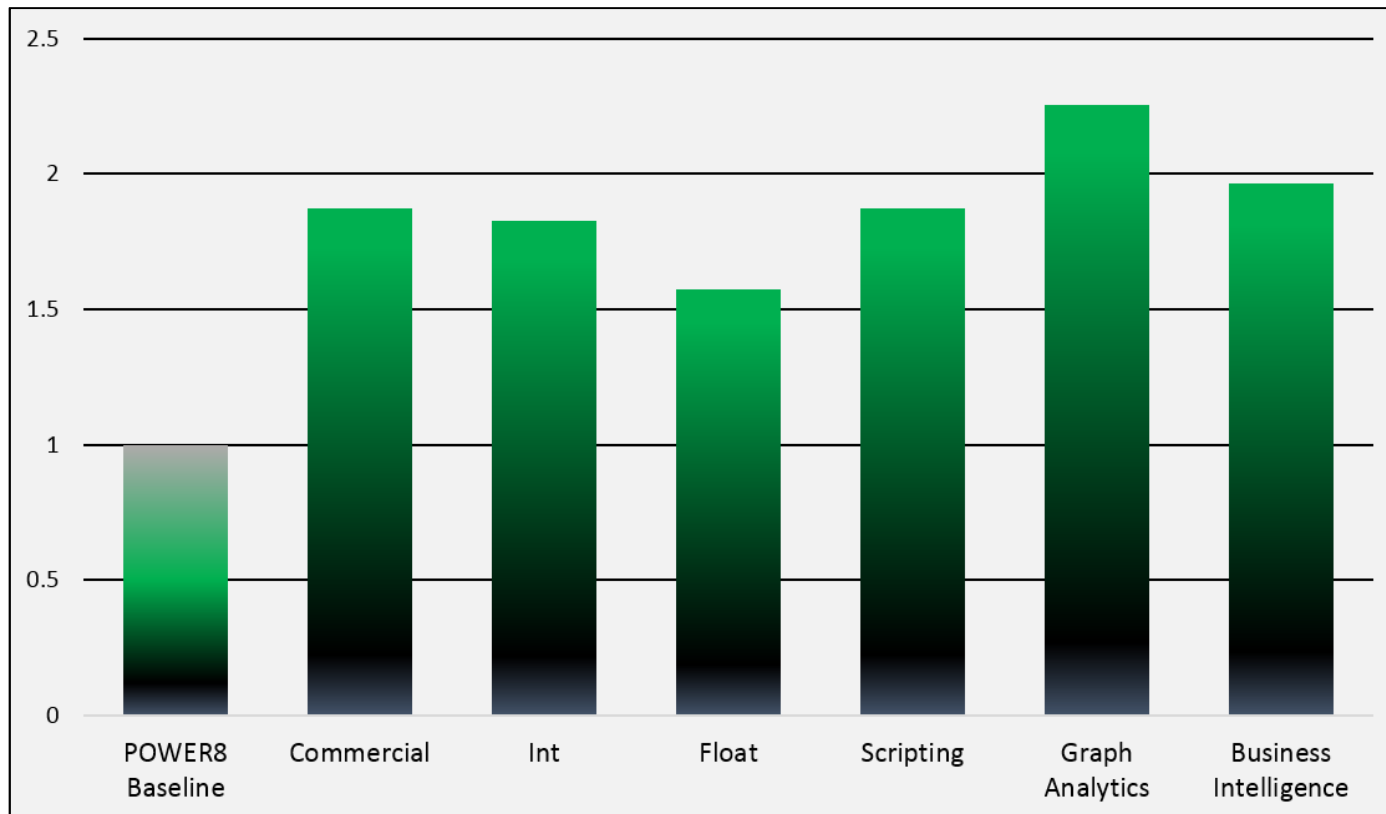
Scale-Out configuration @ constant frequency

POWER ISA v3.0

New Instruction Set Architecture Implemented on POWER9

Broader data type support
- 128-bit IEEE 754 Quad-Precision Float – Full width quad-precision for financial and security applications
- Expanded BCD and 128b Decimal Integer – For database and native analytics
- Half-Precision Float Conversion – Optimized for accelerator bandwidth and data exchange

Support Emerging Algorithms
- Enhanced Arithmetic and SIMD
- Random Number Generation Instruction

Accelerate Emerging Workloads
- Memory Atomics – For high scale data-centric applications
- Hardware Assisted Garbage Collection – Optimize response time of interpretive languages

Cloud Optimization
- Enhanced Translation Architecture – Optimized for Linux
- New Interrupt Architecture – Automated partition routing for extreme virtualization
- Enhanced Accelerator Virtualization
- Hardware Enforced Trusted Execution

Energy & Frequency Management
- POWER9 Workload Optimized Frequency – Manage energy between threads and cores with reduced wakeup latency

POWER

POWER9 – Data Capacity & Throughput

Big Caches for Massively Parallel Compute and Heterogeneous Interaction
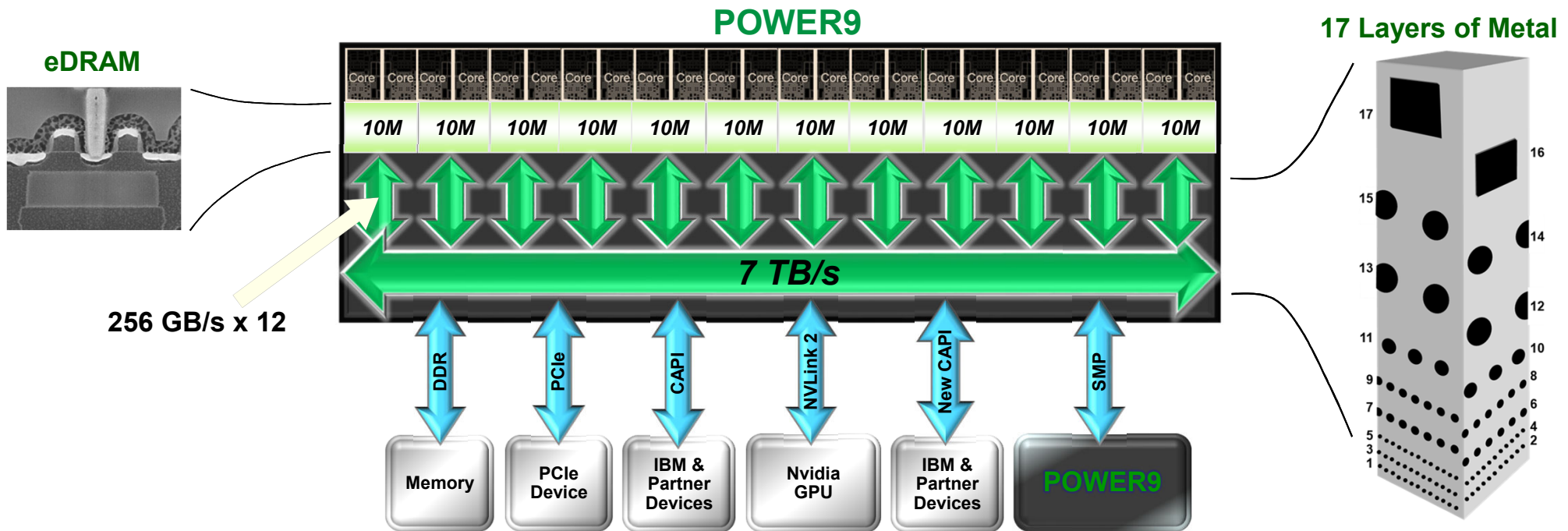
L3 Cache: 120 MB Shared Capacity NUCA Cache

- 10 MB Capacity + 512k L2 per SMT8 Core
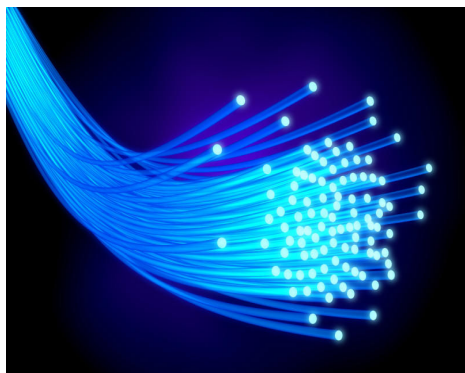- Enhanced Replacement with Reuse & Data-Type Awareness
  12 x 20 way associativity

Extreme Switching Bandwidth for the Most Demanding Compute and Accelerated Workloads

High-Throughput On-Chip Fabric

- Over 7 TB/s On-chip Switch
- Move Data in/out at 256 GB/s per SMT8 Core

POWER9

eDRAM

17 Layers of Metal

10M 10M 10M 10M 10M 10M 10M 10M 10M 10M 10M 10M

7 TB/s

256 GB/s x 12

DDR | PCIe | CAPI | NVLink 2 | New CAPI | SMP

Memory | PCIe Device | IBM & Partner Devices | Nvidia GPU | IBM & Partner Devices | POWER9

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Modular Constructs → High-speed 25 Gb/s Signaling

Utilize Best-of-Breed 25 Gb/s Optical-Style Signaling Technology

Multi-Drawer SMP Interconnect

NVLINK 2 GPU Accelerator Attach

Open CAPI Accelerator Attach
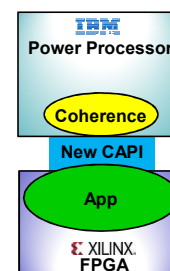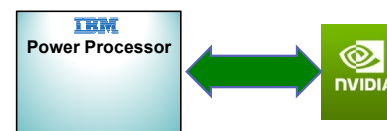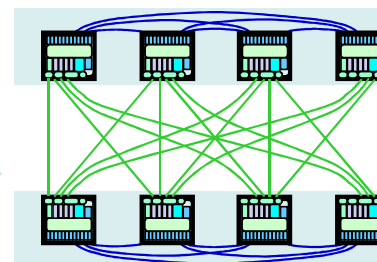
Flexible & Modular Packaging Infrastructure

IBM Power Processor

NVIDIA

IBM Power Processor

Coherence

New CAPI

App

XILINX. FPGA

16 Socket 2-Hop POWER9 Enterprise System Topology

Horizontal Full Connect

4 Socket CEC

New 25 Gb/s
SMP Cable
4X Bandwidth!!!

Vertical Full Connect
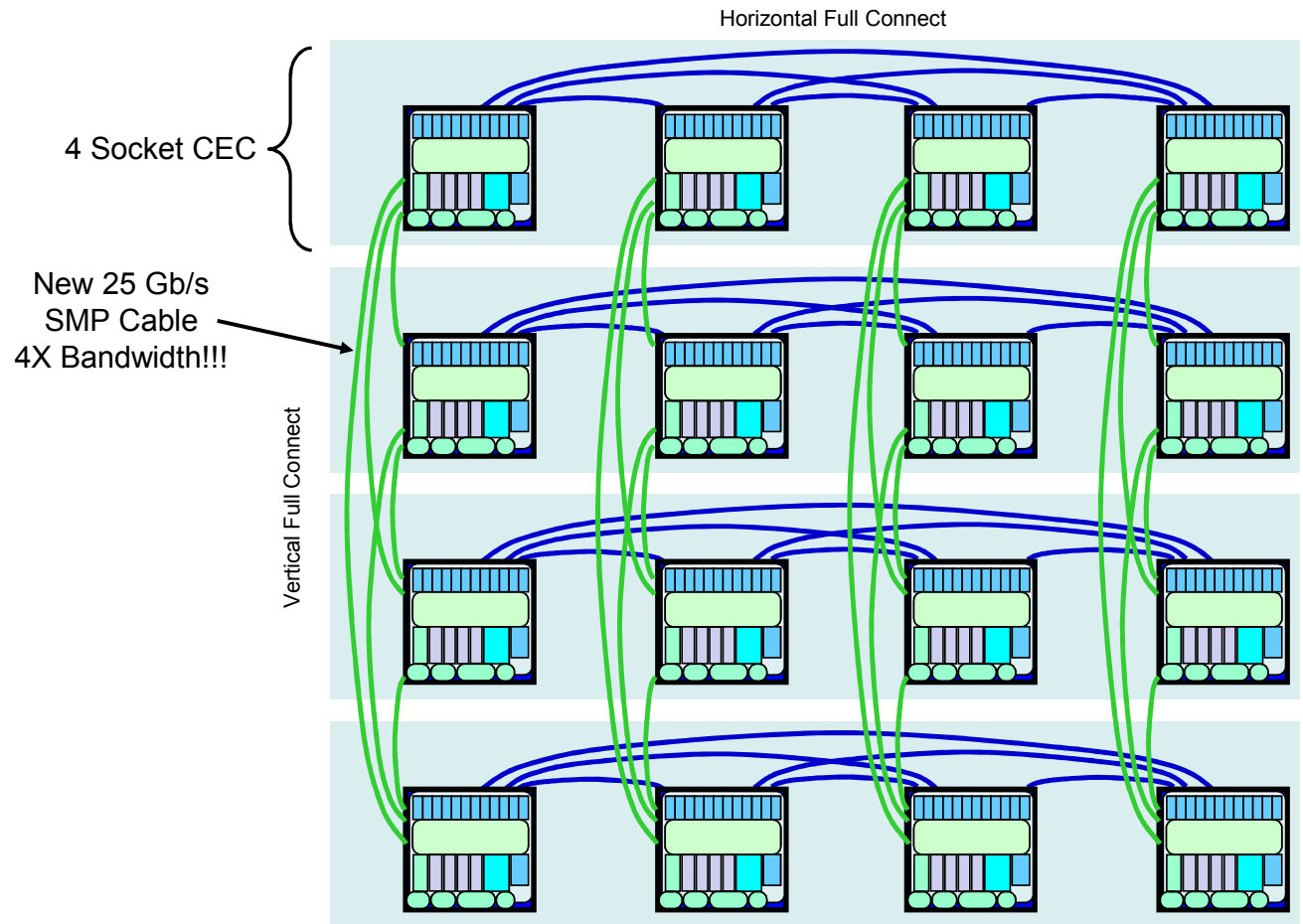
Platform Virtualization Features: Interrupts

New External Interrupt Virtualization Engine (XIVE)
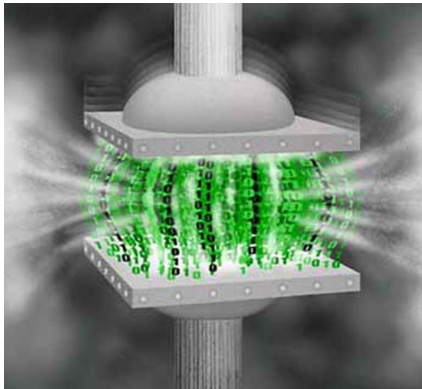
- Prior processors distributed interrupts across system
    - → Significant Software overhead to route interrupts
- New XIVE hardware routes correctly 1st time
    - → Eliminates host processor overhead
    - → Directly target guest Operating System
    - → Enable User level Interrupt

Inter. Proc Int.

Network

Interrupts

XIVE

Routing Tables in Memory

Hypervisor

LPAR1
VP
VP
VP

LPAR2
VP
VP
VP
VP

LPAR3
VP
VP
VP

Inactive Virt.Proc
VP
VP
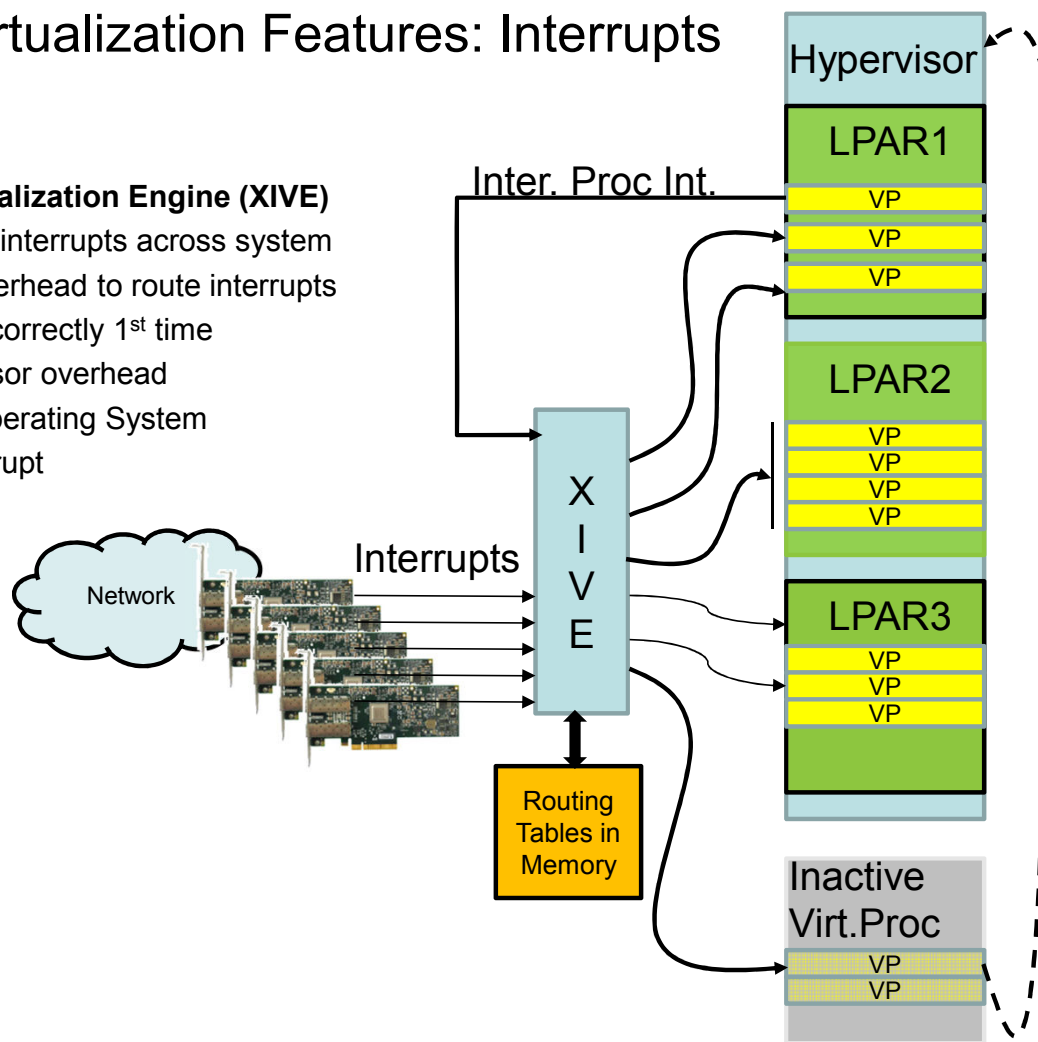
Platform Virtualization Features: Accelerators

On-Processor Accelerators

- Virtualized: User mode invocation (No Hypervisor Calls)
- Industry Standard GZIP Compression / Decompression
- AES Cryptography Support
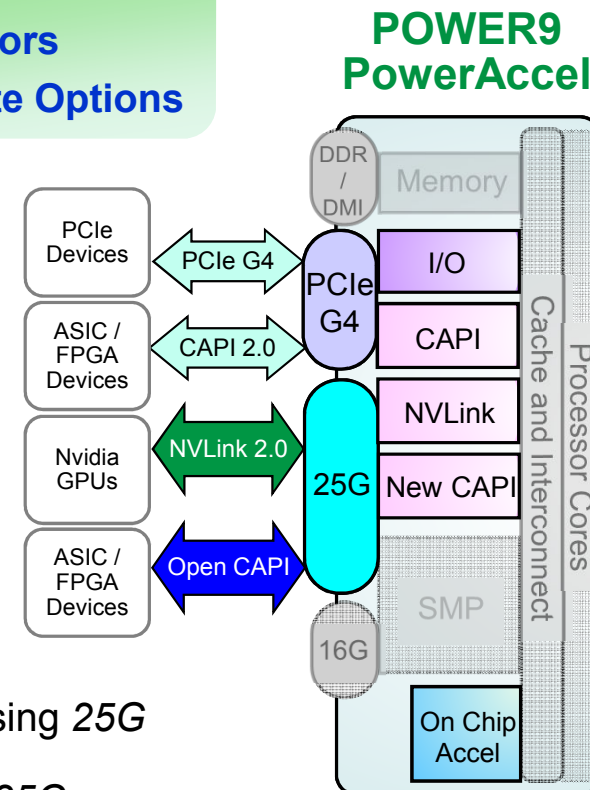- True Random Number Generation
- Data Mover

POWER9 – Premier Acceleration Platform

- **Extreme Processor / Accelerator Bandwidth and Reduced Latency**
- **Coherent Memory and Virtual Addressing Capability for all Accelerators**
- **OpenPOWER Community Enablement – Robust Accelerated Compute Options**

POWER9 PowerAccel

- **State of the Art I/O and Acceleration Attachment Signaling**
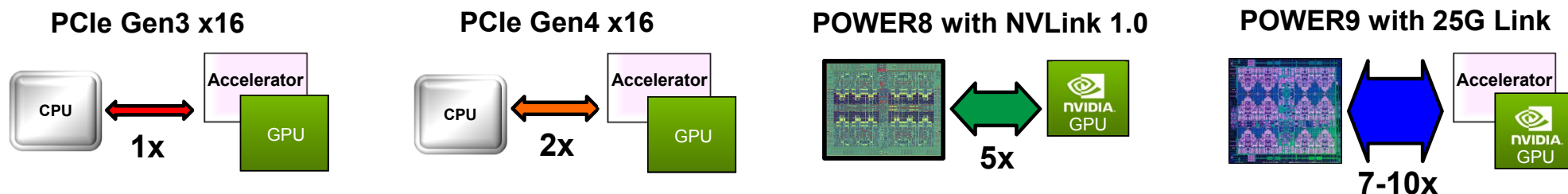
  - **PCIe Gen 4** x 48 lanes – 192 GB/s duplex bandwidth

  - **25Gb/s Common Link** x 48 lanes – 300 GB/s duplex bandwidth

- **Robust Accelerated Compute Options with OPEN standards**

  - **On-Chip Acceleration** – Gzip x1, 842 Compression x2, AES/SHA x2

  - **CAPI 2.0** – 4x bandwidth of POWER8 using *PCIe Gen 4*

  - **NVLink 2.0** – Next generation of GPU/CPU bandwidth and integration using *25G*

  - **Open CAPI 3.0** – High bandwidth, low latency and open interface using *25G*

POWER9 – Ideal for Acceleration

Extreme CPU/Accelerator Bandwidth

PCIe Gen3 x16 — **1x**

PCIe Gen4 x16 — **2x**

POWER8 with NVLink 1.0 — **5x**

POWER9 with 25G Link — **7-10x**

Increased Performance / Features / Acceleration Opportunity

Seamless CPU/Accelerator Interaction

- Coherent memory sharing
- Enhanced virtual address translation
- Data interaction with reduced SW & HW overhead

Broader Application of Heterogeneous Compute

- Designed for efficient programming models
- Accelerate complex analytic / cognitive applications

OpenPOWER™ Foundation

- Accelerating Open Innovation
- Grown from 5 to over 200 members in less than 3 years
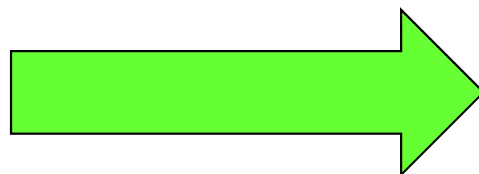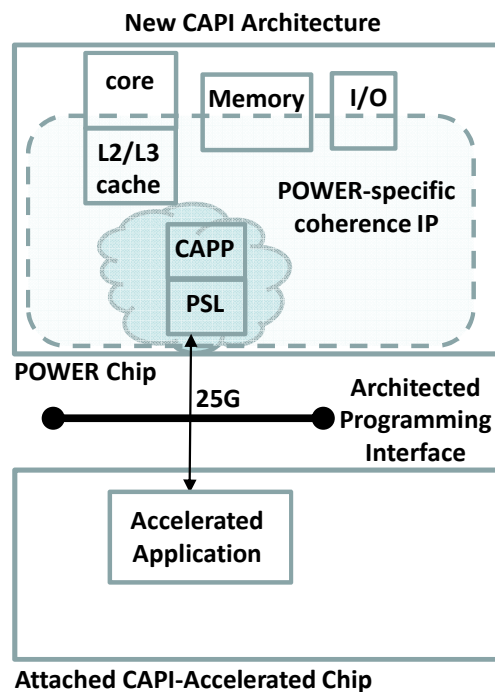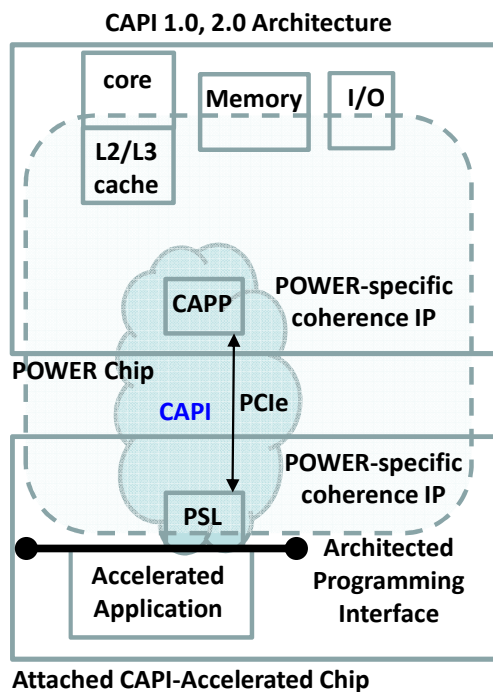
POWER9: Engineered for OpenPOWER Application

- Built for a Broad Range of Deployments and Platforms
- Open and Flexible Solutions
- Ideal for Developers

Open Innovation Interfaces: Open CAPI

CAPI 1.0, 2.0 Architecture

core | Memory | I/O

L2/L3 cache

POWER-specific coherence IP

CAPP

POWER Chip

CAPI PCIe

POWER-specific coherence IP

PSL

Accelerated Application

Architected Programming Interface

Attached CAPI-Accelerated Chip

New CAPI Architecture

core | Memory | I/O

L2/L3 cache

POWER-specific coherence IP

CAPP
PSL

POWER Chip

25G

Architected Programming Interface

Accelerated Application

Attached CAPI-Accelerated Chip

Open Industry Coherent Attach
 - Latency / Bandwidth Improvement
 - Removes Overhead from Attach Silicon
 - Eliminates "Von-Neumann Bottleneck"
 - FPGA / Parallel Compute Optimized
 - Network/Memory/Storage Innovation

IBM
Power Processor

Coherence

App

XILINX.
FPGA
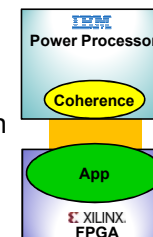
OpenCAPI Approach

- **What is OpenCAPI?**

  - OpenCAPI is an Open Interface Architecture that allows any microprocessor to attach to

    - Coherent user-level accelerators and I/O devices

    - Advanced memories accessible via read/write or user-level DMA semantics

    - Agnostic to processor architecture

- **Key Attributes of OpenCAPI**

  - High-bandwidth, low latency interface optimized to enable streamlined implementation of attached devices

    - 25Gbit/sec signaling and protocol built to enable very low latency interface on CPU and attached device

    - Complexities of coherence and virtual addressing implemented on host microprocessor to simplify attached devices and facilitate interoperability across multiple CPU architectures

  - Attached devices operate natively within an application's user space and coherently with processors

    - Allows attached device to fully participate in application without kernel involvement/overhead

  - Supports a wide range of use cases and access semantics

    - Hardware accelerators

    - High-performance I/O devices

    - Advanced memories

  - 100% Open Consortium / All company participants welcome / All ISA participants welcome

OpenCAPI 3.0 Features

Base Accelerator Support

- Accelerator Reads with no intent to cache, DMA write using Program Addresses

  - The accelerator is working in the same address domain as the host application

    - Pointer chasing, link lists are all now possible without Device Driver involvement

  - Address translation on host (processor) with error response back to the accelerator

    - Very efficient translation latency mechanism using host processor Address Translation Cache (ATC) and MMU

  - Non-posted writes only

  - Ability for Partial Read/Write DMAs

    - Write with byte enables

- Translate touch to warm up address translation caches

  - Allows accelerator to reduce translation latency when using a new page

- Wake Up host thread

  - Very efficient low latency mechanism in lieu of either interrupts or host processor polling mechanism of memory

- Atomic Memory Operations (AMO) to Host Processor Memory

  - Accelerator can now perform atomic operations in the same coherent domain just like any other host processor thread

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Virtual Addressing

- **An OpenCAPI device operates in the virtual address spaces of the applications that it supports**

  – Eliminates kernel and device driver software overhead

  – Improves accelerator performance

  – Allows device to operate directly on application memory without kernel-level data copies or pinned pages

  – Simplifies programming effort to integrate accelerators into applications

- **The Virtual-to-Physical Address Translation occurs in the host CPU**

  – Reduces design complexity of OpenCAPI-attached devices

  – Makes it easier to ensure interoperability between an OpenCAPI device and multiple CPU architectures

  – Since the OpenCAPI device never has access to a physical address, this eliminates the possibility of a defective or malicious device accessing memory locations belonging to the kernel or other applications that it is not authorized to access

OpenCAPI 3.0 Features (cont.)

Base Accelerator Support

- MMIO slave

  - Accelerators have BAR space that provide MMIO register capability

- Configuration space facility slave

  - Efficient discovery and enumeration of accelerators

- OpenCAPI attached Memory

  - High bandwidth and low latency memory home agent capability

  - Load/Store model access to OpenCAPI attached memory

  - Host Application can access memory attached to OpenCAPI endpoint as part of coherent domain

  - Data resides very close to the consumer with very low latency

  - Atomic Memory Operations (AMO) support toward OpenCAPI attached memory

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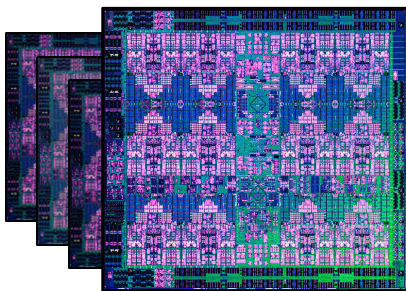
Built for the Cognitive Era

OpenPOWER™

Enhanced Core and Chip Architecture for Emerging Workloads
- New Core Optimized for Emerging Algorithms to Interpret and Reason
- Bandwidth, Scale, and Capacity, to Ingest and Analyze

Processor Family with Scale-Out and Scale-Up Optimized Silicon
- Enabling a Range of Platform Optimizations – from HSDC Clusters to Enterprise Class Systems
- Extreme Virtualization Capabilities for the Cloud

Premier Acceleration Platform
- Heterogeneous Compute Options to Enable New Application Paradigms
- State of the Art I/O
- Engineered to be Open

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