RISC-V External Debug Support Errata 5e7cb72f5b4e673c3d7baad701d7c60d4683cd08

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1 Errata to RISC-V Debug Specification 0.13

1.1 Resume ack bit is set after resuming

The third paragraph of Section 3.5 has a mistake. At the end of the process described there, the resume ack bit is *set*.

1.2 `sbdata0` Reads Order of Operations

The order of operations listed in Section 3.12.23, describing reads from `sbdata0`, is incorrect. It should read:

Reads from this register start the following:

1. "Return" the data.
2. Set sbbusy.
3. If sbreadondata is set, perform another system bus read.
4. If sbautoincrement is set, increment `sbaddress`.
5. Clear sbbusy.

1.3 mte only applies when action=0

The definition of mte in Section 5.2.6 should state that mte only applies to triggers whose action is 0.

1.4 sselect applies to svalue

In Section 5.2.13, when sselect is 0 it ignores svalue.

1.5 Last trigger example

In the last example in Section B.9, the value for `tdata2` 1 should be 0xefff8675.