SAQUIB AHMAD SIDDIQUI

480.512.2671 • sasiddi8@asu.edu • https://saquibahmad01.github.io • https://tinyurl.com/yckqpqz2

EDUCATION

Ph.D.,Computer Engineering; 2018-2023(Expected)
Arizona State University(ASU), Tempe, AZ GPA: 4.00/4.00
Advisor: Dr. Daniel Bliss
Master's Thesis: Hardware Implementation and Analysis of Temporal Interference Mitigation : A High-Level Synthesis Based Approach, **M.S.** Conferred in August 2020
B.TECH, Electronics and Communication Engineering; 2014-2018
Jamia Millia Islamia(JMI), New Delhi

TECHNICAL SKILLS

Machine Learning and Data Processing Tools: Tensorflow, Keras, Pytorch, Slurm, Bash
Design and Applications: MATLAB, High-Level Synthesis, Design Compiler, gem5, LLVM, OpenCL, Simulink, Xilinx SDx
Programming: C, C++, Python, Java, Verilog, Tcl
Relevant Coursework: Hardware Acceleration and FPGA Computation, Mobile Systems Architecture, Advanced Computer Architecture, Statistical Machine Learning, Computation Image Understanding and Pattern Analysis.
Other: Git, Linux, LaTeX

PROFESSIONAL EXPERIENCE

ASU WISCA, Graduate Research Assistant **8/2019-Present**

- Hardware mapping of communication systems algorithms to domain adaptive systolic array based processors
- Computational Precision and Dynamic Range Analysis of Interference Mitigation for Efficient Hardware Implementation onto Field-Programmable Gate Arrays(FPGAs) using High-Level Synthesis.
- Hardware mapping and acceleration of Electromagnetic Radio Frequency (RF) convergence, OFDM and Synthetic Aperture Radar(SAR) routines to FPGAs for application in Domain Specific System on Chip systems.

Information Sciences Institute(ISI)-USC, Visiting Research Assistant **6/2019- 8/2019**

- Worked with the Reconfigurable Computing group advised by Dr. Vivek Venugopalan.
- Software development and optimization of sensor fusion and image processing algorithm followed by hardware mapping to FPGA using Xilinx's SDSoC tool. Implemented an optimized streaming implementation that used high caching to give a significant performance improvement against even GPU and real time fps(50).

IIIT Delhi, Research Intern **5/2017 – 6/2017**

- Worked on image and video processing for multimedia security and forensics at Cybersecurity Education and Research Centre. Code implementation of papers like
  - "Video Super-resolution with convolutional neural networks" by A. Kappeler, IEEE Transactions [2016]
  - "Large Scale Video Classification with Convolutional Neural Networks(CNNs)" by A. Kaparthy, Fei Fei Li, et al." CVPR[2014]. Used Tensorflow for implementation.

ACADEMIC PROJECTS

ASU, FPGA Accelerator for QR factorization **Fall 2020**

- Data type optimized hardware accelerator designed for QR factorization using Modified Gram-Schmidt method. Fully feed forward architecture with throughput of 1.15 GOPS achieved.

ASU, Hardware implementation of Geometric Series **Fall 2020**

- Folded and unfolded implementation with use of interleaving with peak throughput of 1Msamples/s

ASU, Energy-Delay Characterization of 64-bit fixed point ALU in 28nm CMOS technology **Fall 2020**

- Generated RTL and HDL test bench using Simulink HDL Workflow and then performed sizing, threshold and supply voltage optimizations. Comparative study to find out the optimal optimization combinations based on energy-delay models

ASU, Text to image synthesis using Generative Adversarial Networks(GANs) **Fall 2019**

- Using existing Deep Convolution GANs(DCGANs) architecture along with matching aware discriminator and training with manifold interpolation. Implemented both using Tensorflow and Pytorch.

ASU, Cache Replacement and Branch Prediction Policy **Spring 2019**

- Implemented Signature-based Hit Predictor policy(SHiP) using SRRIP and global-history Divide-and-Conquer(gDAC) branch prediction.gem5 was used for simulation purposes.

ASU, Single and Multi-thread performance comparison **Spring 2019**

- Matrix multiplication(naive and tiled) to compare both single and multi-thread performance using OpenCL

ASU, Relay Node Placement **Spring 2019**

- Algorithmic Implementation for solving BCRP-MNCC(Budget constrained relay placement minimum number of connected components) and BCRP-MLCC(Maximum size of largest connected components) problems.

PUBLICATIONS

- O.Iqbal, **S. Siddiqui** et al. "Design and FPGA Implementation of an Adaptive Video Subsampling Algorithm for Energy-Efficient Single Object Tracking", 2020, IEEE International Conference on Image Processing
- V.Menon, **S.Siddiqui** et al. "Design and Performance Evaluation of Multispectral Sensing Algorithms on CPU, GPU and FPGA", 2021, IEEE Aerospace Conference