26-bit

In computer architecture, **26-bit** integers, memory addresses, or other data units are those that are 26 bits wide, and thus can represent values up to 64 mega (base 2). Two examples of computer processors that featured 26-bit memory addressing are certain second generation IBM System/370 mainframe computer models introduced in 1981 (and several subsequent models), which had 26-bit physical addresses but had only the same 24-bit virtual addresses as earlier models, and the first generations of ARM processors.

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IBM System/370

As data processing needs continued to grow, IBM and their customers faced challenges directly addressing larger memory sizes. In what ended up being a short-term "emergency" solution, a pair of IBM's second wave of System/370 models, the 3033 and 3081, introduced 26-bit real memory addressing, increasing the System/370's amount of physical memory that could be attached by a factor of 4 from the previous 24-bit limit of 16 MB. IBM referred to 26-bit addressing as "extended real addressing," and some subsequent models also included 26-bit support. However, only 2 years later, IBM introduced 31-bit memory addressing, expanding both physical and virtual addresses to 31 bits, with its System/370-XA models, and even the popular 3081 was upgradeable to XA standard.

Given 26-bit's brief history as the state-of-the-art in memory addressing available in IBM's model range, and given that virtual addresses were still limited to 24 bits, software exploitation of 26-bit mode was limited. The few customers that exploited 26-bit mode eventually adjusted their applications to support 31-bit addressing, and IBM dropped support for 26-bit mode after several years producing models supporting 24-bit, 26-bit, and 31-bit modes. The 26-bit mode is the only addressing mode that IBM removed from its line of mainframe computers descended from the System/360. All the other addressing modes, including now 64-bit mode, are supported in current model mainframes.

Early ARM processors

In the ARM processor architecture, 26-bit refers to the design used in the original ARM processors where the Program Counter (**PC**) and Processor Status Register (**PSR**) were combined into one 32-bit register (R15), the status flags filling the high 6 bits and the Program Counter taking up the lower 26 bits.

In fact, because the program counter is always word-aligned the lowest two bits are always zero which allowed the designers to reuse these two bits to hold the processor's mode bits too. The four modes allowed were USR26, SVC26, IRQ26, FIQ26; contrast this with the 32 possible modes available when the program status was separated from the program counter in more recent ARM architectures.

This design enabled more efficient program execution, as the Program Counter and status flags could be saved and restored with a single operation. This resulted in faster subroutine calls and interrupt response than traditional designs, which would have to do two register loads or saves when calling or returning from a subroutine.

Despite having a 32-bit ALU and word-length, processors based on ARM architecture version 1 and 2 had only a 26-bit PC and address bus, and were consequently limited to 64 MiB of addressable memory. This was still a vast amount of memory at the time, but because of this limitation, architectures since have included various steps away from the original 26-bit design.

The ARM architecture version 3 introduced a 32-bit PC and separate PSR, as well as a 32-bit address bus, allowing 4 GiB of memory to be addressed. The change in the PC/PSR layout caused incompatibility with code written for previous architectures, so the processor also included a 26-bit compatibility mode which used the old PC/PSR combination. The processor could still address 4 GB in this mode, but could not execute anything above address 0x3FFFFFC (64 MB). This mode was used by RISC OS running on the Acorn Risc PC to utilise the new processors while retaining compatibility with existing software.

ARM architecture version 4 made the support of the 26-bit addressing modes optional, and ARM architecture version 5 onwards has removed them entirely.

External links

- Differences Between ARM6 and Earlier ARM Processors
- "Using the Acorn C/C++ Development Environment to write 32-bit RISC OS software" Details on the architectural changes and converting code between 26-bit and 32-bit.
- http://www.heyrick.co.uk/assembler/32bit.html - Information on converting assembler to 32-bit