RTL Simulation in Xilinx ISE

Terminal   _ ▫ ✕

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```
------------------------
-time = 365 rqst0 = 0, rqst1 = 0,rqst2 = 0, rqst3 = 1
- time = 365 grnt0 = 0, grnt1 = 0, grnt2 = 0, grnt3 = 1
------------------------
Result is as Expected
------------------------
- [ Scoreboard ]
------------------------
-time = 365 rqst0 = 0, rqst1 = 0,rqst2 = 0, rqst3 = 1
- time = 365 grnt0 = 0, grnt1 = 0, grnt2 = 0, grnt3 = 1
------------------------
----------Accuracy Report----------
Accuracy :          80%
----------Accuracy Report Done-----
------------------------
- [ Monitor ]
------------------------
-time = 405 rqst0 = 0, rqst1 = 0,rqst2 = 0, rqst3 = 1
- time = 405 grnt0 = 0, grnt1 = 0, grnt2 = 0, grnt3 = 1
------------------------
Result is as Expected
------------------------
- [ Scoreboard ]
------------------------
-time = 405 rqst0 = 0, rqst1 = 0,rqst2 = 0, rqst3 = 1
- time = 405 grnt0 = 0, grnt1 = 0, grnt2 = 0, grnt3 = 1
------------------------
----------Accuracy Report----------
Accuracy :          90%
----------Accuracy Report Done-----
Simulation complete via $finish(1) at time 405 NS + 2
./environment.sv:63     $finish;
xcelium> exit
TOOL:   xrun    21.03-s014: Exiting on Aug 23, 2022 at 20:26:29 IST  (total: 00:00:01)
unix> ▮
```

⊡ 📄 FCFS | ▣ Terminal

Verification using VMM
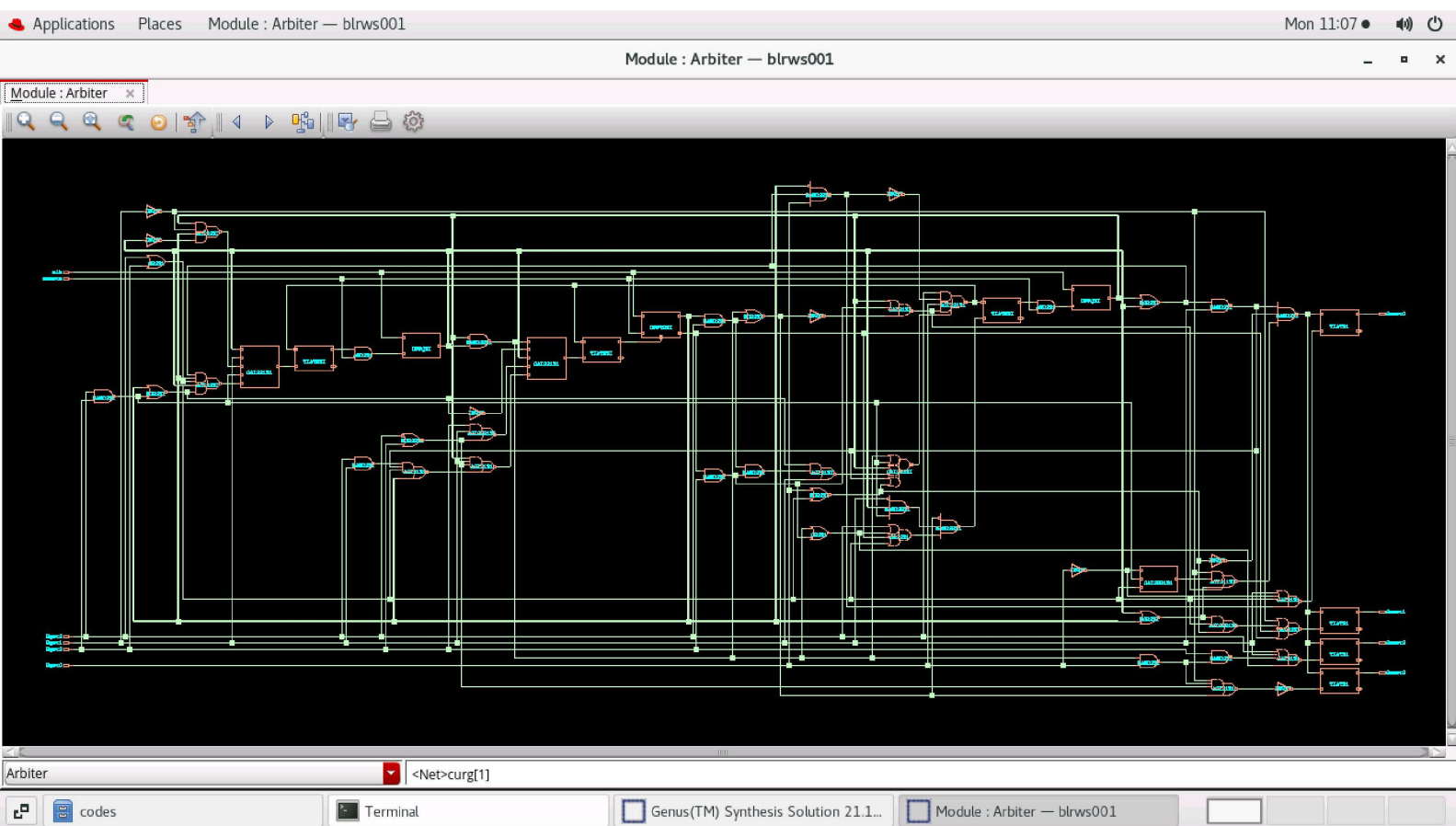
Gate Level Netlist Synthesis using Cadence Genus

Open ▾   INCREMENTAL_time.rpt
         ~/rtl2gds/codes/REPORTS

Save   ≡   ✕

```
============================================================
 Generated by:          Genus(TM) Synthesis Solution 21.12-s068_1
 Generated on:          Aug 22 2022  11:06:32 am
 Module:                Arbiter
 Library domain:        TIMING
   Domain index:        0
   Technology libraries: gpdk045bc
                        physical_cells
 Operating conditions:  slow
 Interconnect mode:     global
 Area mode:             physical library
============================================================

path   1:

        Pin                 Type       Fanout Load Slew Delay Arrival   Location
                           (Domain)          (fF) (ps) (ps)  (ps)      (x,   y)
-----------------------------------------------------------------------------
(clock clk)                launch                              0 R
(arb.sdc_line_2_4_1)       ext delay                   +500  500 R
resetn                     in port       3  9.4   0   +0   500 R
g2467__2398/B                                        +0   500
g2467__2398/Y              AND2X1(TIMING) 1  4.5  90  +126  626 R
curg_reg[1]/D              DFFQXL(TIMING)              +0   626
curg_reg[1]/CK             setup              0       +125  752 R
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
(clock clk)                capture                          10000 R
-----------------------------------------------------------------------------
Cost Group   : 'clk' (path_group 'clk')
Timing slack :    9248ps
Start-point  : resetn
End-point    : curg_reg[1]/D

path   2:
```

Plain Text ▾   Tab Width: 8 ▾   Ln 1, Col 1   ▾   INS

"INCREMENTAL_time.rpt" selected (33.3 kB)

ming_   final.rpt   INCREMENTAL_
.rpt   Arbiter.db

Timing Report with slack of +9.2ns

Terminal   _   ▫   ✕

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```
       : -frequency_scaling_factor : 1.0
       : -use_clock_freq : stim
       : -stim :/stim#0
       : -fromGenus : 1
Info   : ACTP-0001 Timing initialization started
Info   : ACTP-0001 Timing initialization ended
Info   : PWRA-0002 [PwrInfo] Skipping activity propagation due to -skip_ap
       : option....
Warning: PWRA-0302 [PwrWarn] Frequency scaling is not applicable for vectorless
       : flow. Ignoring frequency scaling.
Warning: PWRA-0304 [PwrWarn] -stim option is not applicable with vectorless mode
       : of power analysis, ignored this option.
Info   : PWRA-0002 Started 'vectorless' power computation.
Info   : PWRA-0002 Finished power computation.
Info   : PWRA-0007 [PwrInfo] Completed successfully.
       : Info=6, Warn=2, Error=0, Fatal=0
Instance: /Arbiter
Power Unit: W
PDB Frames: /stim#0/frame#0
    -----------------------------------------------------------------------
    Category       Leakage      Internal    Switching        Total    Row%
    -----------------------------------------------------------------------
      memory    0.00000e+00   0.00000e+00  0.00000e+00   0.00000e+00    0.00%
    register    6.12027e-10   2.82811e-06  9.20606e-07   3.74933e-06   28.17%
       latch    1.27968e-09   1.35493e-06  3.58952e-07   1.71516e-06   12.89%
       logic    3.13647e-09   2.01747e-06  5.61560e-07   7.63621e-06   57.37%
        bbox    0.00000e+00   0.00000e+00  0.00000e+00   0.00000e+00    0.00%
       clock    0.00000e+00   0.00000e+00  2.09952e-07   2.09952e-07    1.58%
         pad    0.00000e+00   0.00000e+00  0.00000e+00   0.00000e+00    0.00%
          pm    0.00000e+00   0.00000e+00  0.00000e+00   0.00000e+00    0.00%
    -----------------------------------------------------------------------
    Subtotal    5.02818e-09   6.20052e-06  7.10511e-06   1.33107e-05  100.01%
  Percentage          0.04%        46.58%       53.38%       100.00%  100.00%
    -----------------------------------------------------------------------
legacy_genus:/>  ▊
```

Power Report using genus
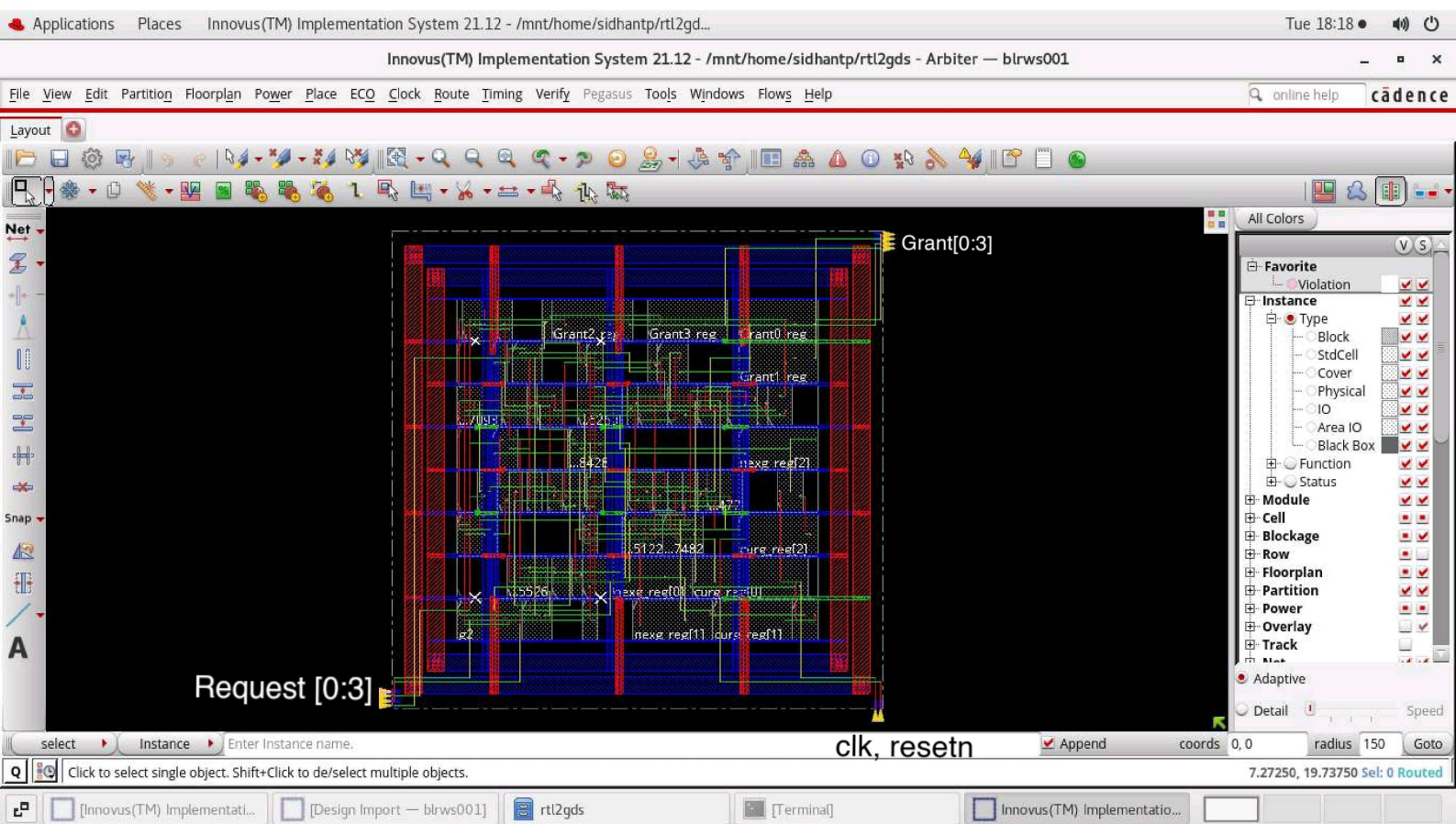
Floorplan->Powerplan->Placement->CTS->Route in Cadence Innovus