



HEXAGON

Leica
Geosystems

Lessons Learned for Reusable Firmware

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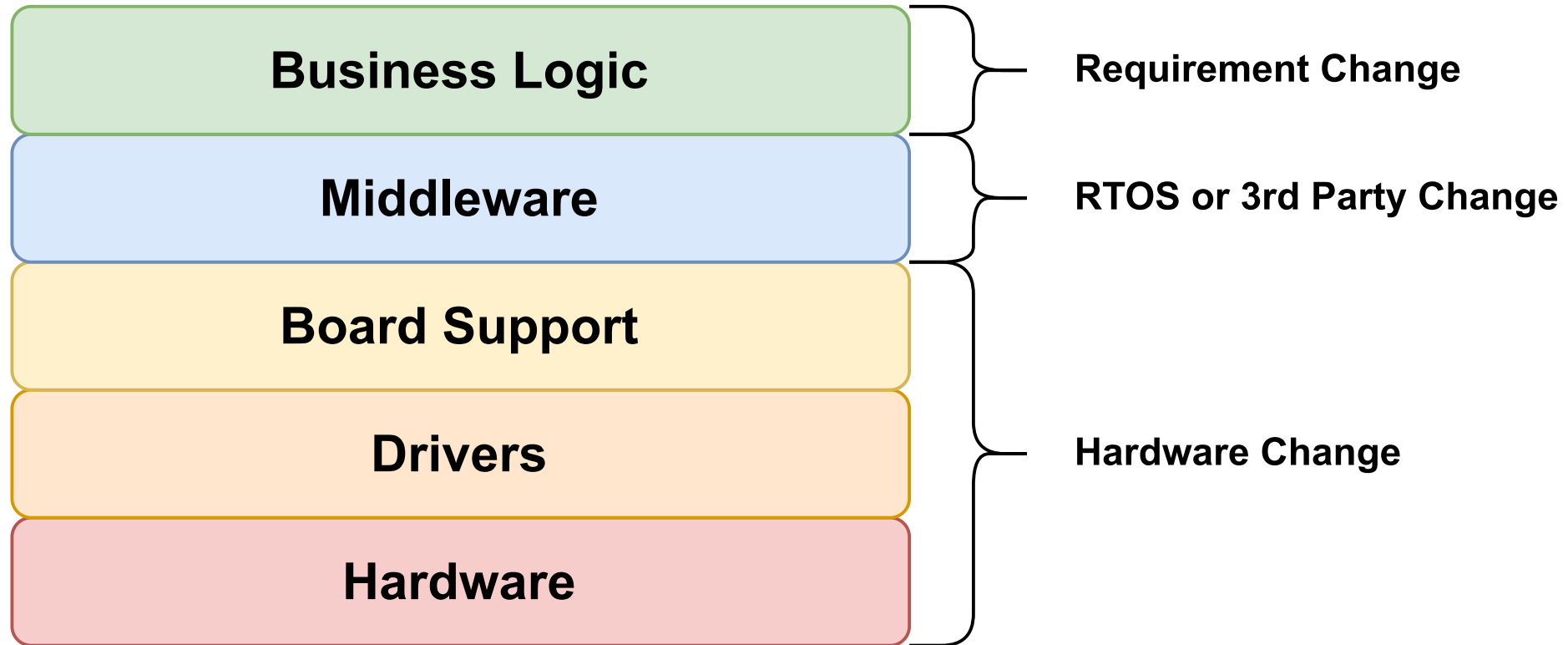


Complexity



- Complexity increases with each generation
- Collaboration necessary
- Integration necessary

Reasons for Changes



Reasons for Changes

Reuse vs. Mutation



original

```
1 /*...*/  
2 sensor::sensor(spi_driver& spi, /*...*/)  
3     : /*...*/, m_reset(gpio::port_e, 1, gpio::digital_output) {}  
4 /*...*/
```



mutation

```
1 /*...*/  
2 sensor::sensor(spi_driver& spi, /*...*/)  
3     : /*...*/, m_reset(gpio::port_e, 2, gpio::digital_output) {}  
4 /*...*/
```

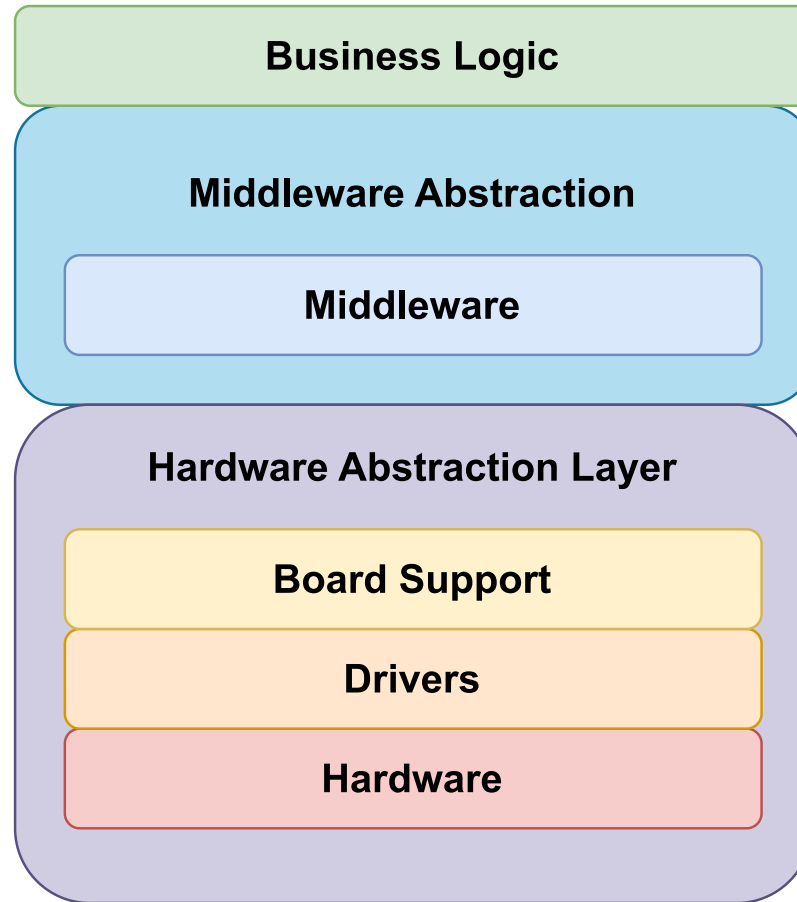
Reasons for Changes

Reuse vs. Mutation

```
1 // bsp is defined for each board configuration
2 namespace bsp {
3     static constexpr gpio_cfg sensor_reset_pin =
4         {gpio::port_e, 2, gpio::digital_output};
5 }
6
7 /*...*/
8 #include <bsp/pin_cfg.hpp>
9
10 sensor::sensor(spi_driver& spi, /*...*/)
11     : /*...*/, m_reset(bsp::sensor_reset_pin) {}
12 /*...*/
```

Reasons for Changes

taking back control



Why reusable Software?

Benefits

- Reuse of functionalities between products
- Management of system complexity
- Reduced development time
- Shorter time to the market

Drawbacks

- Higher initial development time
- Needs to consider "all" projects
 - All development restrictions apply
 - All expectations need to be handled
- Regressions would be a disaster

What needs to be done?

- Create hardware abstraction
- Create middleware abstraction
- Separate business logic components
- Enable separate integration step
- Consider testing for all layers

Hardware Abstraction Layer

Hardware Abstraction Layer

What should it do?

- provide abstraction for all higher layers
- high-level abstraction for hardware access
- provide all needed functions, **should not restrict**
- maintainable and testable
- allow mocking and simulation

Hardware Abstraction Layer

Current Situation

- Existent HALs create dependencies
 - Vendor or hardware specific
 - RTOS specific
- ***To be independent you need your own***

Abstraction & Injection

Runtime abstraction

- Interface abstraction
- Callback injection

Compile time abstraction

- Template abstraction (policies, traits, concepts)
- Header/Linker injection

Hardware Abstraction Layer

```
base_gpio.hpp

1 template <typename SOC_TYPE>
2 struct base_gpio {
3     using soc_type = SOC_TYPE;
4     using device_type = trait::soc_gpio_device_t<SOC_TYPE>;
5     using config_type = typename device_type::config_type;
6
7     constexpr base_gpio(config_type cfg) noexcept;
8     constexpr const device_type& device() const noexcept;
9
10    inline error_code init(pin_state state) noexcept;
11    inline error_code write(pin_state state) noexcept;
12    /* ... */
13 };
```

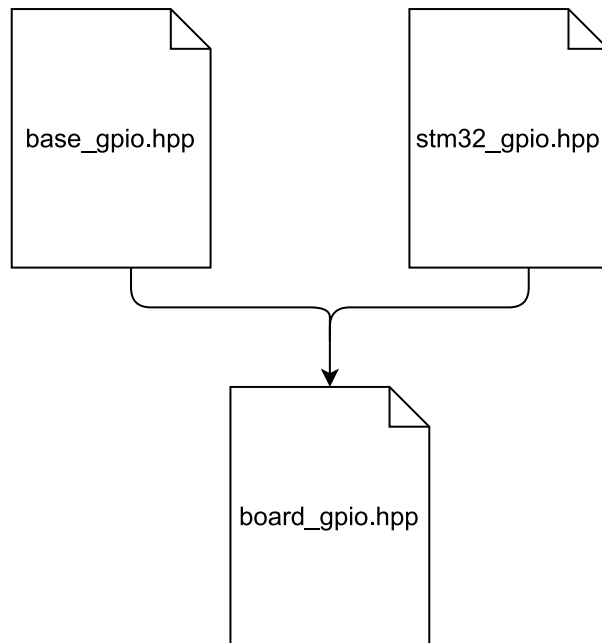
Hardware Abstraction Layer

```
gtest_gpio.hpp

1 template <>
2 struct base_gpio<tests::gtest> : tests::gtest_base_mock {
3     using soc_type = tests::gtest;
4     using device_type = trait::soc_gpio_device_t<tests::gtest>;
5     using config_type = typename device_type::config_type;
6
7     constexpr base_gpio(config_type cfg) noexcept;
8     constexpr const device_type& device() const noexcept;
9     /* ... */
10 };
```

Hardware Abstraction Layer

Board Support



```
board_gpio.hpp

1 #include <base/base_gpio.hpp>
2 #include <soc/st/stm32g4.hpp>
3
4 /*...*/
5 using gpio = base_gpio<soc::st::stm32g4>;
6
7 // using gpio = base_gpio<soc::nordic::nrf52>;
8 // using gpio = base_gpio<rtos::zephyr>;
9 // using gpio = base_gpio<tests::gtest>;
```


Hardware Abstraction Layer

Device Tree



```
1 pinctrl: pin-controller@48000000 {  
2     gpioa: gpio@48000000 {  
3         reg = < 0x48000000 0x400 >;  
4         # ...  
5     };  
6 };  
7  
8 leds {  
9     green_led: led_0 {  
10         gpios = < &gpioa 0x05 GPIO_ACTIVE_HIGH>;  
11     };  
12 };
```



```
1 using gpioa = gpio_ctrl<register<0x48000000 0x400>, /*...*/>;  
2 using green_led_cfg = gpio_cfg<gpioa, 0x05, gpio::active_high>
```

Hardware Abstraction Layer

Summary

- Consider effort
- Choose flexible abstractions
- Hide complexity for the user
- Consider tests and simulations
- Think about code generation

Middleware Abstraction

Middleware Abstraction

What should it do?

- Enable control for integration
- Needs to be interchangeable
- Needs to enable tests
- Unify APIs and error handling
- Easy to use, hard to misuse
 - ***Lead business logic design***

Middleware Abstraction

Current Situation

- Standards exist
 - Not a good fit for MCUs
- RTOS systems
 - Different APIs & Features
 - Incompatible with Host System

Middleware Abstraction

STL

- Not 3rd Party
- Can be included
 - Define what to use
 - Backporting features



```
1 namespace mwa {  
2     template<class R, class P = ::mwa::ratio<1>>  
3     using duration = std::chrono::duration<R, P>;  
4 }
```

Middleware Abstraction

Thread

Zephyr

```
1 k_tid_t k_thread_create(struct k_thread *new_thread,  
2                          k_thread_stack_t *stack,  
3                          size_t stack_size,  
4                          k_thread_entry_t entry,  
5                          void *p1, void *p2, void *p3,  
6                          int prio,  
7                          uint32_t options,  
8                          k_timeout_t delay);
```

FreeRTOS

```
1 BaseType_t xTaskCreate( TaskFunction_t pvTaskCode,  
2                          const char * const pcName,  
3                          configSTACK_DEPTH_TYPE usStackDepth,  
4                          void *pvParameters,  
5                          UBaseType_t uxPriority,  
6                          TaskHandle_t *pxCreatedTask);
```

Middleware Abstraction

Thread

```
thread_abstraction

1 // definition
2 thread::thread(const thread_cfg& cfg,
3               entry_type entry);
4 // use
5 struct component {
6     component(const thread_cfg& cfg) noexcept
7         : m_thread(cfg, /*...*/) {};
8     /*...*/
9     thread m_thread;
10 };
11 /*...*/
12 class system_setup {
13     /*...*/
14     thread_cfg m_thread_cfg{stack_cfg(addr, size), thread_prio::low};
15     component m_component{m_thread_cfg};
16 };
```


Middleware Abstraction

Summary

- Lead business logic design
- Consider Host OS from the beginning
- Take care about behavior relevant parts
 - Allow resources to be handled outside
 - Separate configuration and creation
- Provide only what is necessary

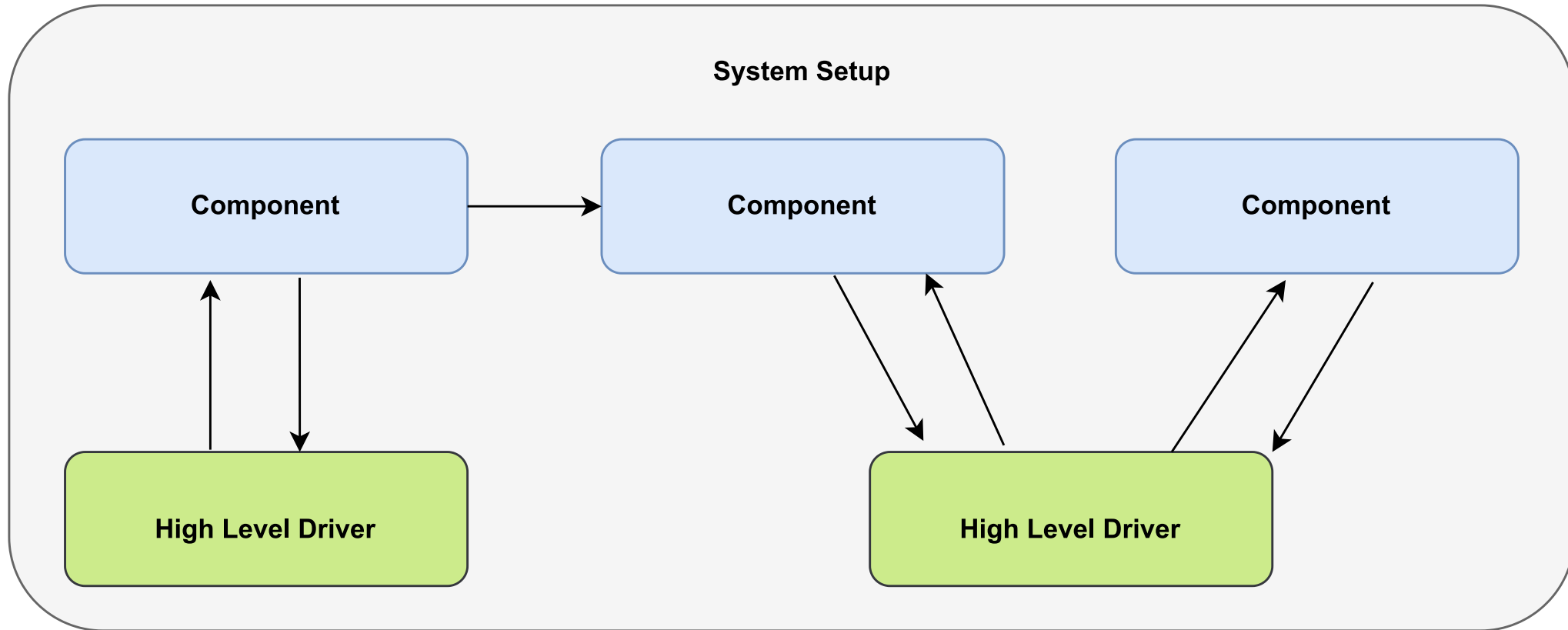
Business Logic

Business Logic

What should it do?

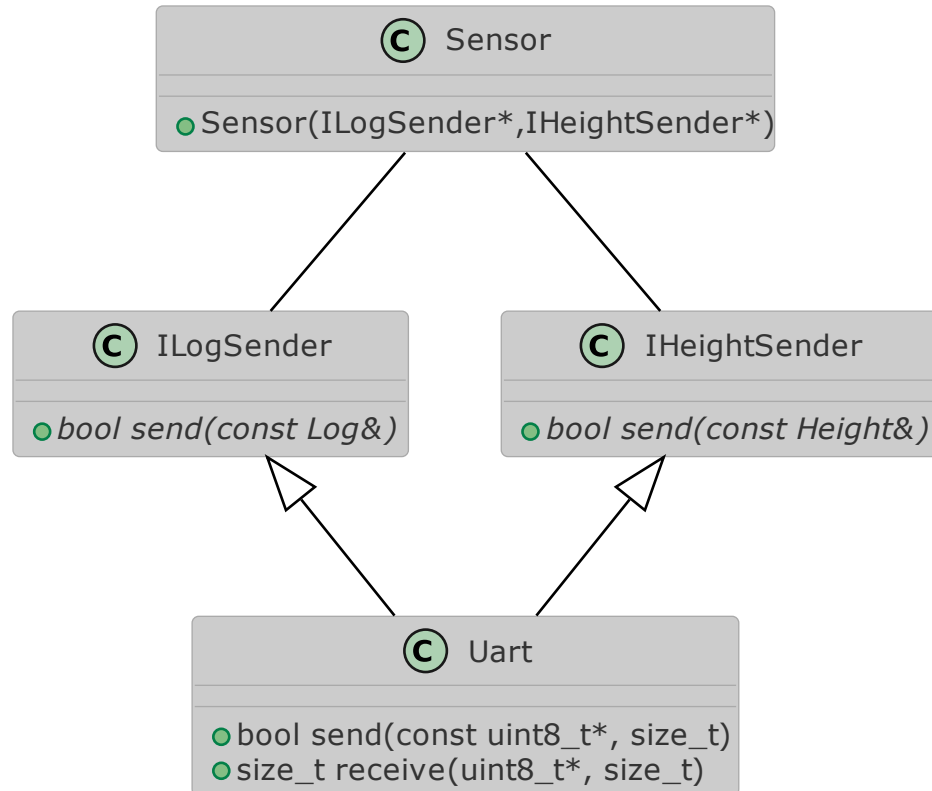
- Setup the system
 - Create and connect resources and components
- System startup and shutdown
- Allow to interchange components

Business Logic



Business Logic

Communication



Direct Interface

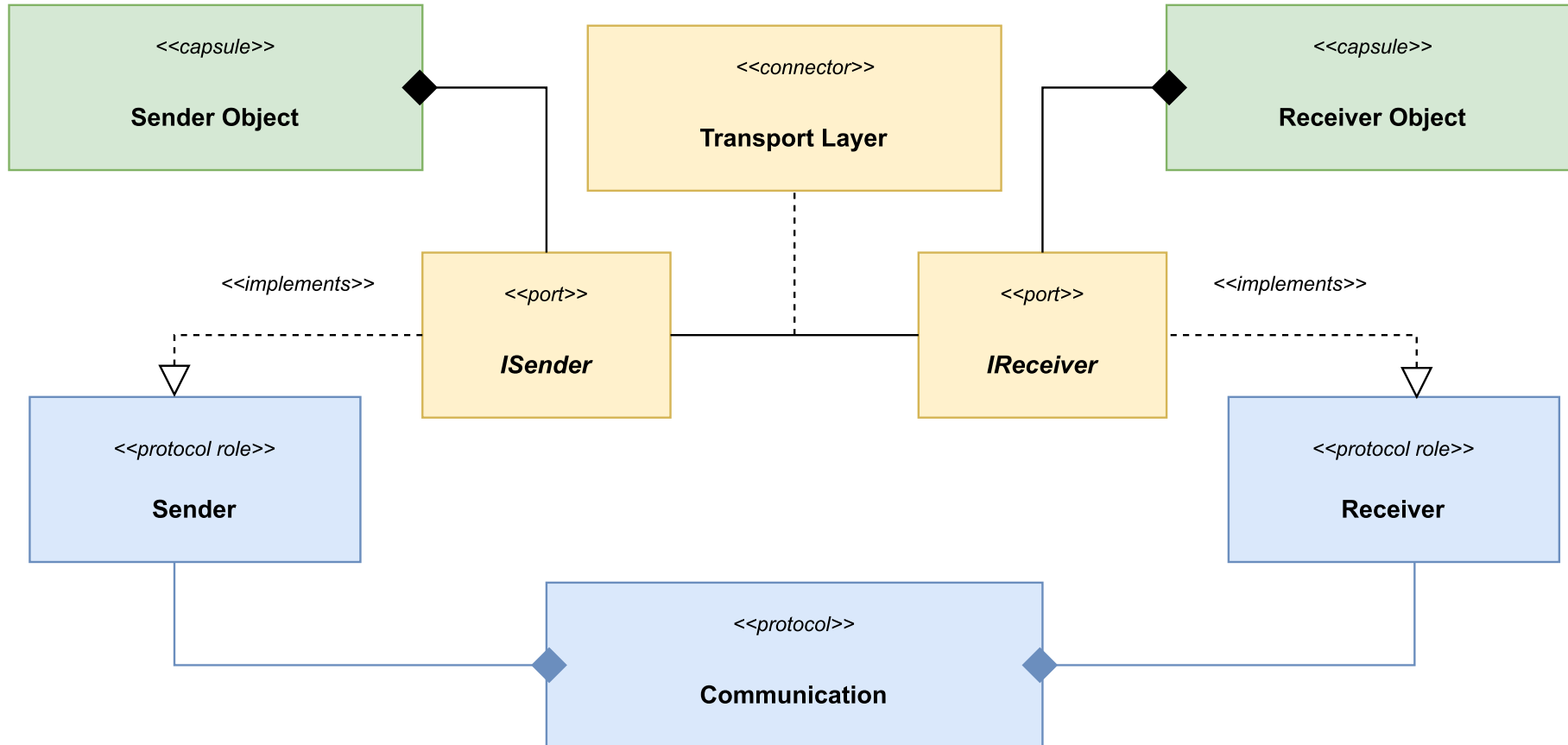
- Creates dependencies between components
- Can inject unwanted behavior

Protocol Abstraction

- Layer over the communication
- Only protocol knows messages
 - Handles decoding and dispatching
 - Handles encoding and sending
- Thread transition can be enforced

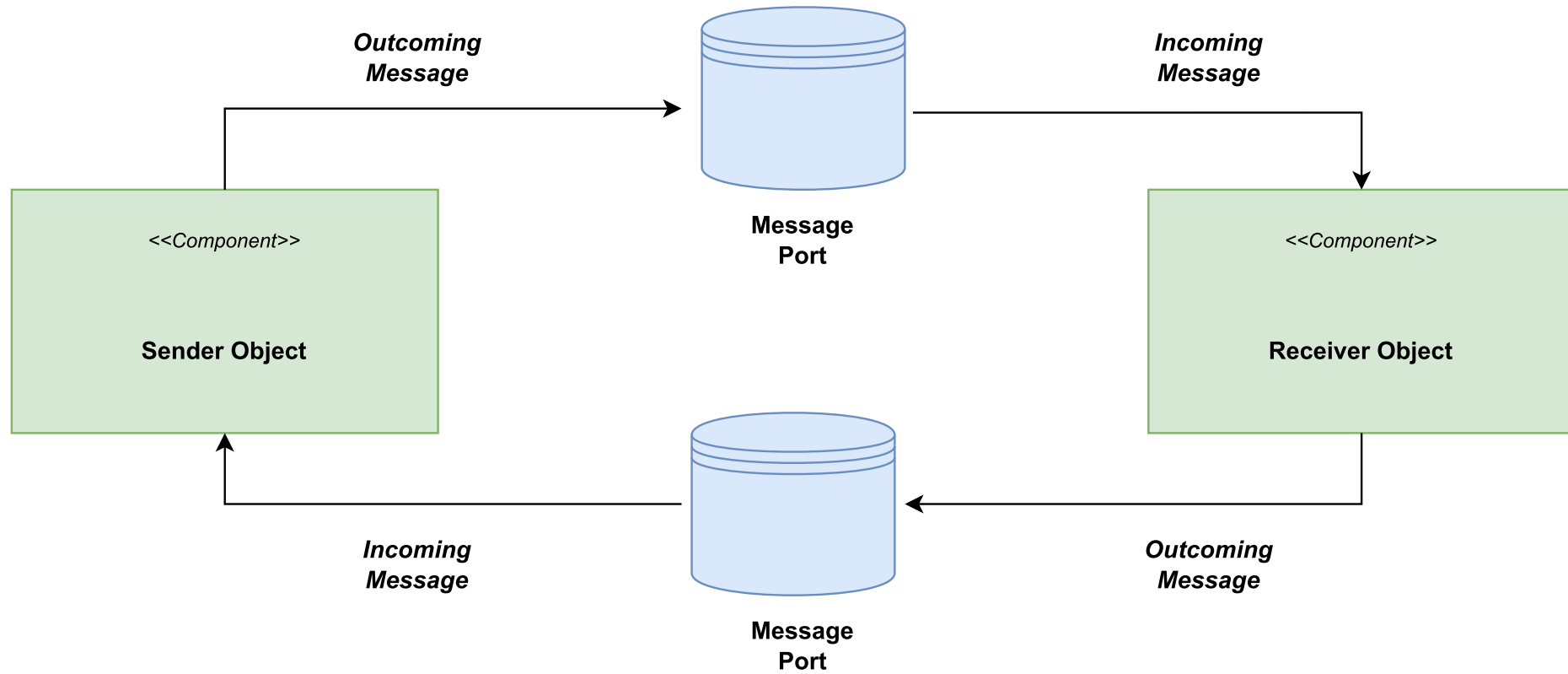
Communication

ROOM-Pattern



Communication

Microservice



Communication

Message Port

```
write_port.hpp

1 template<class RECEIVER_T, typename PROTOCOL_T>
2 struct write_port {
3     using protocol_type = PROTOCOL_T;
4     using receiver_type = RECEIVER_T;
5     using message_types = trait::incoming_messages_t<receiver_type>
6
7     write_port(receiver_type& receiver) noexcept;
8
9     template <typename MSG_T>
10    requires concepts::contains<trait::convert_t<MSG_T, protocol_type>,
11                                message_types>
12    bool write(const MSG_T& msg) noexcept {
13        const auto msg_out = convert<protocol_type>(msg);
14        return receive_message(m_receiver, msg_out);
15        // could also be dispatched over message_queue, ipc etc.
16    }
17    /*...*/
18 };
```


Communication

Receiving Messages

```
component.hpp

1 template <typename>
2 struct incoming_messages {
3     using type = ::util::sequence<>;
4 };
5
6 template <>
7 struct incoming_messages<component> {
8     using type = ::util::sequence<log_msg, ...>;
9 };
10
11 bool receive_message(component& obj, const log_msg& msg) { /*...*/ }
12 bool receive_message(component& obj, const auto& msg) { /*...*/ }
```

Communication

Sending Messages

```
i_component.hpp

1 struct i_component_write {
2     virtual bool write(const component_msg&) const noexcept = 0;
3 };
4
5 template<typename PROTOCOL_T>
6 struct component_write_port : i_component_write {
7     bool write(const component_msg& msg) const noexcept override;
8     /*...*/
9 };
10
11 struct component {
12     component(i_component_write& port) noexcept;
13 };
```

Communication

Sending Messages

```
component.hpp

1 template<typename ... Ts>
2 class write_port_ref<util::sequence<Ts...>> {
3 public:
4     using operation_types =
5         typename detail::write_port_operations<Ts...>::type;
6
7     template<typename T>
8     write_port_ref(const T& obj);
9
10    template<typename T>
11    void write(const T& msg) const noexcept;
12    /*...*/
13 };
14
15 struct component {
16     using write_port_type =
17         write_port_ref<outcoming_messages_t<component>>>;
18     component(write_port_type port) : m_port(port) {}
19 };
```

Integration

System Setup

```
system_setup.hpp

1 class system_setup {
2     /*...*/
3
4     system_setup() noexcept
5         : m_uart(uart_cfg)
6         , m_component(component::write_port_type{m_port}, thread_cfg)
7     { /*...*/ }
8
9     bool init() noexcept;
10    bool startup() noexcept;
11    bool shutdown() noexcept;
12    /*...*/
13
14    uart_driver m_uart;
15    component    m_component;
16
17    using component_port = write_port<uart_driver, protocol::inhouse>
18    component_port m_port{m_uart};
19 };
```

Summary

Keep in Mind

- Consider all possibilities for changes
- Isolate the hardware and take control
- Isolate the middleware and allow host build
- Design components independent and interchangeable
- Consider testing over all abstractions of your design

What's next?

Near future

- <https://github.com/zie87/talks>
 - Slides & Notes
 - Code Samples

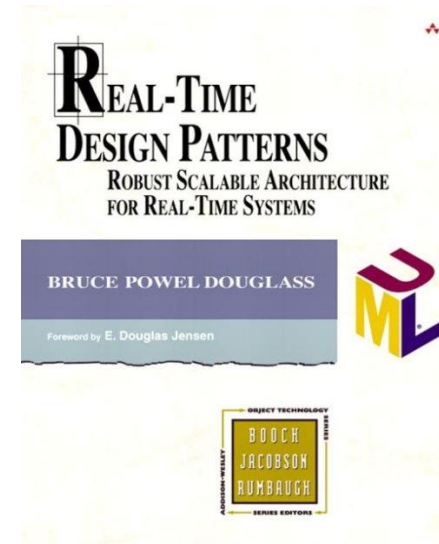
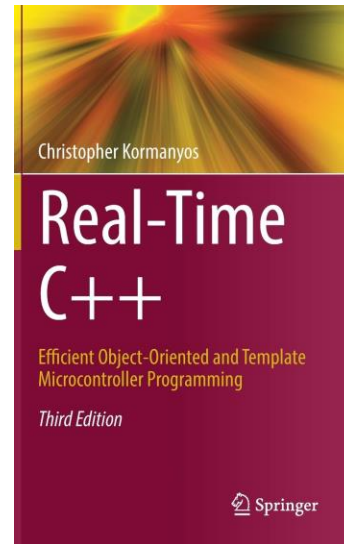
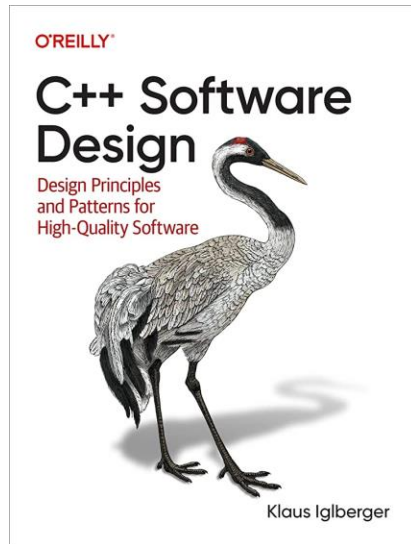
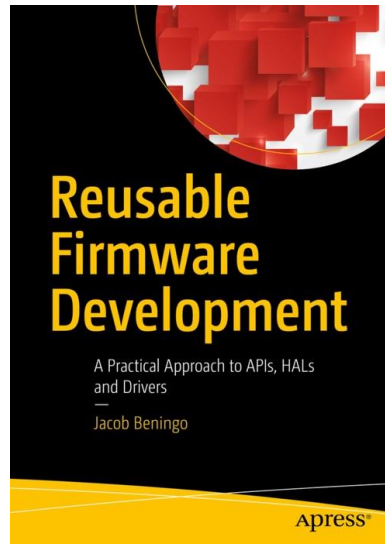
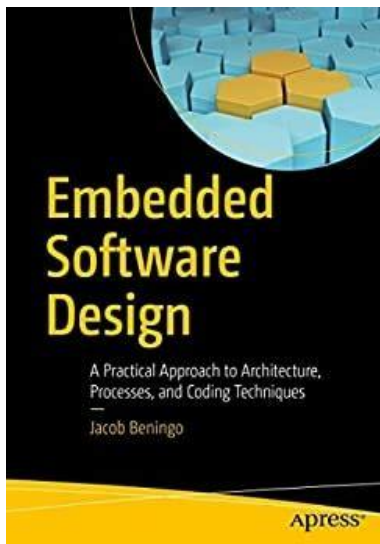


Distant future

- Hardware Abstraction Layer
- Device Tree Parser
- Generic System Setup

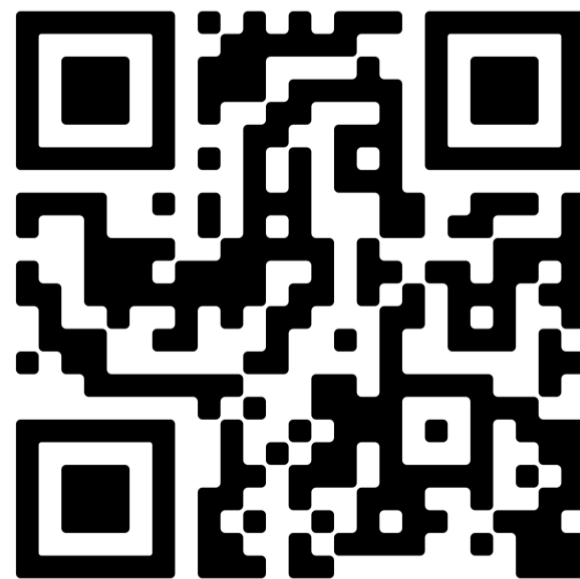
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