

Computer Organisation and Architecture Laboratory

CS39001

KGP-RISC Assignment Report

Group Number: 23

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1 Instruction set and encoding

1.1 R-format

opcode	rs	rt	shamt	don't care	func
6 bits	5 bits	5 bits	5 bits	6 bits	5 bits

Instruction	opcode	func
add rs,rt	000000	00000
comp rs,rt	000000	00001
and rs,rt	000001	00000
xor rs,rt	000001	00001
shll rs, sh	000010	00000
shrl rs, sh	000010	00001
shllv rs, rt	000010	00010
shrl rs, rt	000010	00011
shra rs, sh	000010	00100
shrav rs, rt	000010	00101
diff rs, rt	000011	00000

1.2 I-format

opcode	rs	don't care	imm
6 bits	5 bits	5 bits	16 bits
Instruction	opcode		
addi rs,imm	000011		
compi rs,imm	000100		

1.3 Memory-access

opcode	rs	rt	imm
6 bits	5 bits	5 bits	16 bits
Instruction	opcode		
lw rt, imm(rs)	000101		
sw rt, imm(rs)	000110		

1.4 branch format

opcode	rs	don't care	L
6 bits	5 bits	5 bits	16 bits
Instruction	opcode		
bltz rs,L	000111		
bz rs,L	001000		
bnz rs,L	001001		

1.5 jump to register format

opcode	rs	don't care
6 bits	5 bits	21 bits

Instruction	opcode
br rs	001010

1.6 unconditional jump -format

opcode	L
6 bits	26 bits

Instruction	opcode
b L	001011
bl L	001100
bcy L	001101
bncy L	001110

2 Control signals

Control signal is a 17 bit binary stream where-

- control_sig[16]: whether PC needs to unconditionally jump to a label or not
- control_sig[15]: 1 in case of br instruction
- control_sig[14]: 1 in case of all branch instructions
- control_sig[13]: 1 in case of complement operation
- control_sig[12:8]: type of operation in the ALU
- control_sig[7]: 1 in case of I type instructions
- control_sig[6]: If data need to be written to memory from register (and which register)

- control_sig[5:4]: 1 in case of something needs to be written to memory
- control_sig[3]: 1 in case of something needs to be read from memory
- control_sig[2]: 1 in case of something needs to be written to the registerfile
- control_sig[1:0]: Determines the register to which something needs to be written

Instr	opcode	func	value
add	000000	00000	00000000101000100
comp	000000	00001	00010010101000100
and	000001	00000	00000001001000100
xor	000001	00001	00000001101000100
shll	000010	00000	00000101011000100
shrl	000010	00001	00000100011000100
shllv	000010	00010	00000101001000100
shrl	000010	00011	00000100001000100
shra	000010	00100	00000100111000100
shrav	000010	00101	00000100101000100
addi	000011	NA	00000000111000100
compi	000100	NA	00010010111000100
lw	000101	NA	00001010110101101
sw	000110	NA	00001010110010000
bltz	000111	NA	10100000000000000
bz	001000	NA	10100000000000000
bnz	001001	NA	10100000000000000
br	001010	NA	01100000000000000
b	001011	NA	00100000000000000
bl	001100	NA	00100000000000110
bcy	001101	NA	00100000000000000
bncy	001110	NA	00100000000000000

2.1 Datapath

