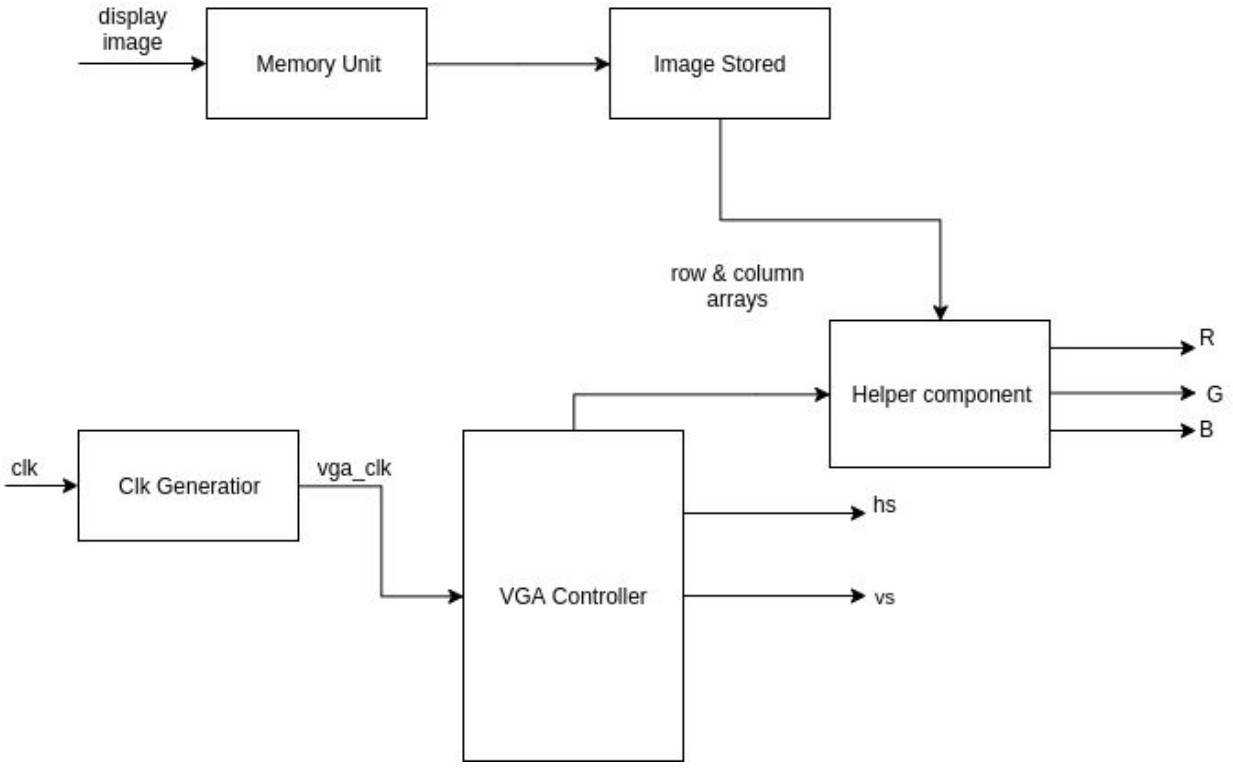
COL215 Mini Project
Progress Report 1

Title: Bus/metro route display

Revised Aim: 1. Display bus/metro routes on the computer screen using VGA interface.
2. Find the shortest path between any two given stations and display it on Screen.

Progress:

- Completed Clk generation unit: Generate 25 Mhz pixel clock
- Completed VGA Controller Unit: used to generate VS and HS signal
- Memory Unit: Used IP core catalog in Vivado to create a block RAM and initialized it using coe file generated
- Image generation unit : added functions to draw line on monitor given two points (x1, y1) and (x2, y2) and tested it on monitor.
- Made VHDL compatible algorithm for finding shortest path between source and destination.



Block diagram

Current difficulties: creating a valid coe file with all information(stations, distance etc.), correctly implementing dijkstra's algo on fpga.