Advanced Digital Electronics Laboratory 6

Analysing structural logic circuits in Vivado.

Task:

Design a FPGA that adds two 3-bit unsigned numbers. For this first write a 1-bit full adder. Then using structural VHDL design connect this adder to build a 2 input 3-bit adder having no carry output.

Method:

1) Implement the circuit using the Xilinx Vivado design suite following the steps of the previous laboratory. Explain your code using remarks in your VHDL description.
2) Simulate your design using an appropriate simulation strategy. To carry out this simulation develop your own testbench. Explain your code using remarks in your VHDL description.
3) Test your circuit on the Basys 3 board. Document that your circuit is working correctly using photographs.
4) Analyse and document the slice logic of your circuit. Give a brief overview of the results of the other nine sections of this report.
5) Draw conclusions