**Programme: DT021A**
**Laboratory Technical Report**

| | Name | Student Number |
|---|---|---|
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| **Collaborator 1:** | | |
| **Collaborator 2:** | | |
| **Collaborator 3:** | | |

| | |
|---|---|
| **Laboratory Number:** | **1** |
| **Semester Week Number:** | **1** |
| **Date:** | **01/26/2022** |

**Submission Checklist and Declaration**

To ensure that the focus of the assessment of your laboratory report can include the development of higher-order skills and competencies associated with a Level 8 qualification, please complete the checklist and declaration below.

| **I declare that the report that I am submitting:** | **Tick Boxes** |
|---|---|
| • is my original work, with secondary sources acknowledged;<br>• was proofread thoroughly for typographical errors;<br>• contains citations with references formatted in the IEEE reference citation style.<br>I understand that my work can be returned uncorrected if the criteria are unfulfilled. | ☑<br>☑<br>☑ |

**By submitting this report I declare that the above conditions are fully met.**

## 1.0 Laboratory Aim

- Purpose of the experiment

This laboratory aims to get familiar with the Vivado application and utilize the Vivado Design Environment to design simulate and synthesise a digital comparator circuit.

In this lab, the crucial task is to program BASYS 3 board using Xilinx software known as the Vivado to perform an XNOR gate logic. The functionality of the finished design will be tested by implementing and programming it onto the Artix-7 FPGA of the Digilent Basys 3 board.

## 2.0 Laboratory Procedure

- Actions are taken during the work

The lab action that was taken during the lab, was to create the VHDL design source code and to create a VHDL simulate code to test the design.

Implementing the design on the Basys 3 development board on Artix-7 FPGA and applying signals to the board via the switches to confirm that the design works as planned.

The comparator that is used in this circuit is an XNOR logic gate which means it depends on the 2 inputs A and B to determine the output signal, as shown in the diagram below.


| A | B | EQ |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

*Figure 1 - A 1-bit digital Comparator [2]*

The output of the analogue comparator is high when the input of a signal equals or exceeds the reference signal.

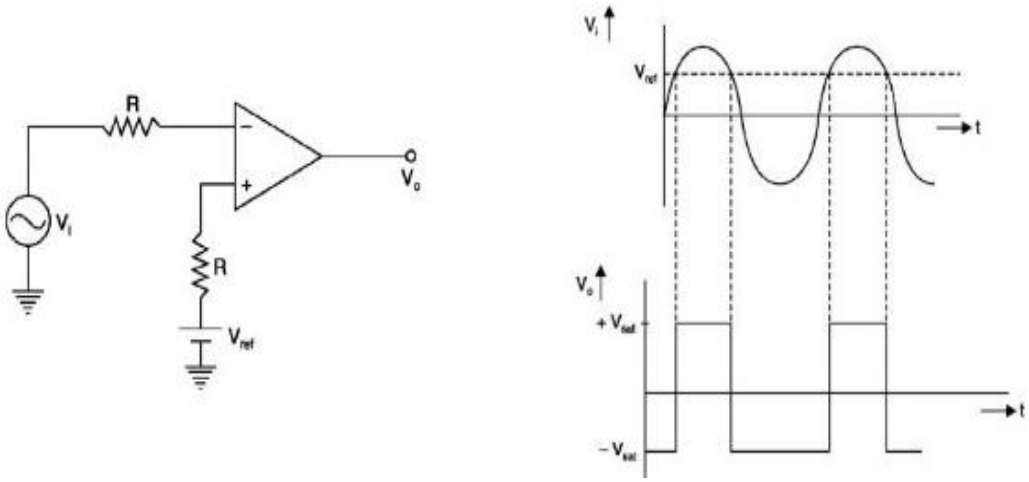



*Figure 2 - Output of an Analogue Comparator [2]*

The new project was created to program the board and simulate it. The test bench source file was created "Compared_TB" to set the I/O ports, then the following link was used to generate VHDL code with the help of source code.

https://www.doulos.com/knowhow/perl/testbench_creation/ [1]

After editing the test bench VHDL Code the runtime on the simulation settings was set to 100 ns to run the behavioural simulation. The behavioural simulations are recorded in the results section.

## 3.0 Results

- Present the results recorded from the investigation.

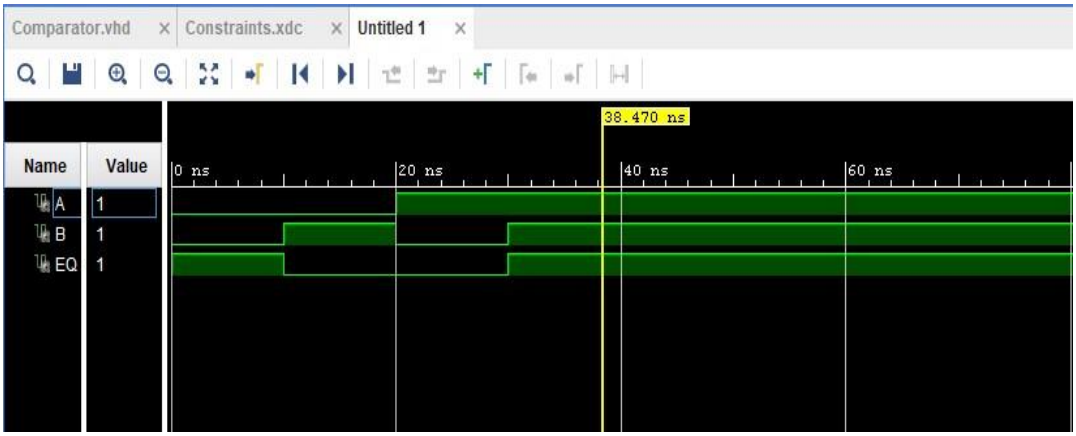



*Figure 3 - Behavioural Simulation results*

After checking the simulation with a marker, the result of the simulation shows that if we receive 1 in both inputs then we will receive 1 in the output.

| A | B | EQ |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

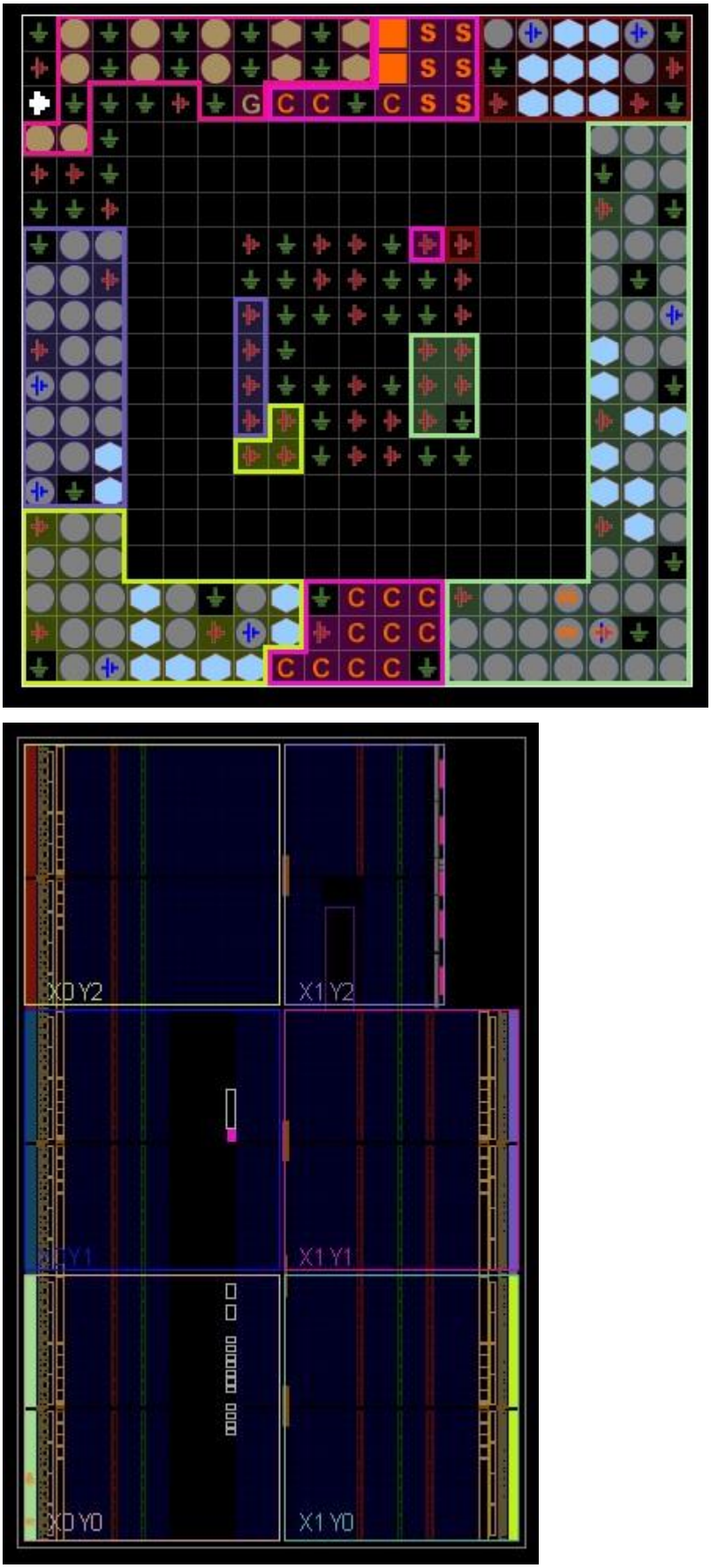



Figure 4 – Results of the Elaborated Design package & Synthesized design device layout

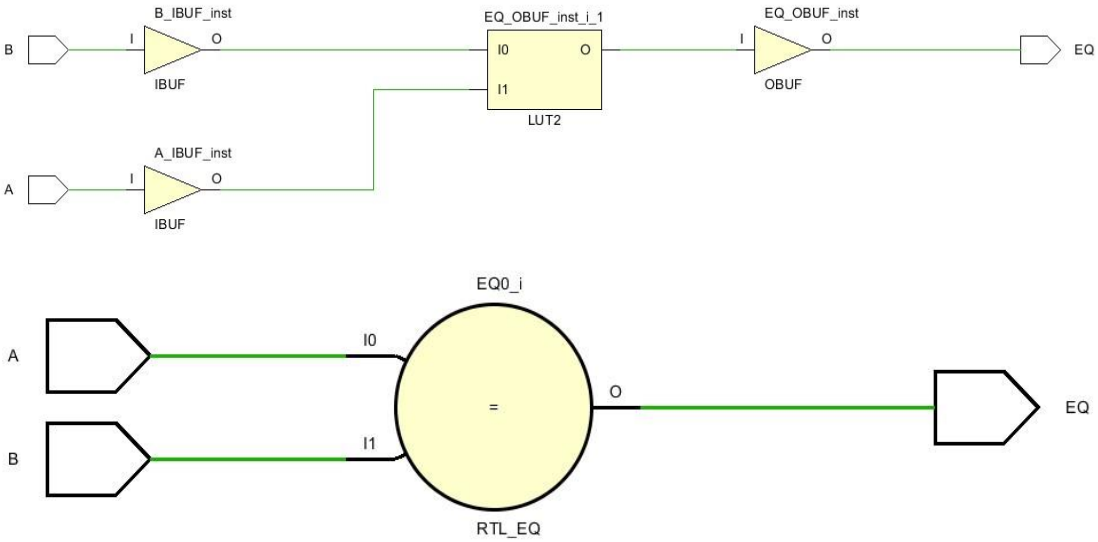



*Figure 5 - Comparison of the Synthesis Schematics and RTL*

- Testing

The result of the comparator can be seen on the BASYS 3 board, shown below in the photo. The board shows the logic when both switches are ON, the light turn as shown on the bottom right corner of the board.

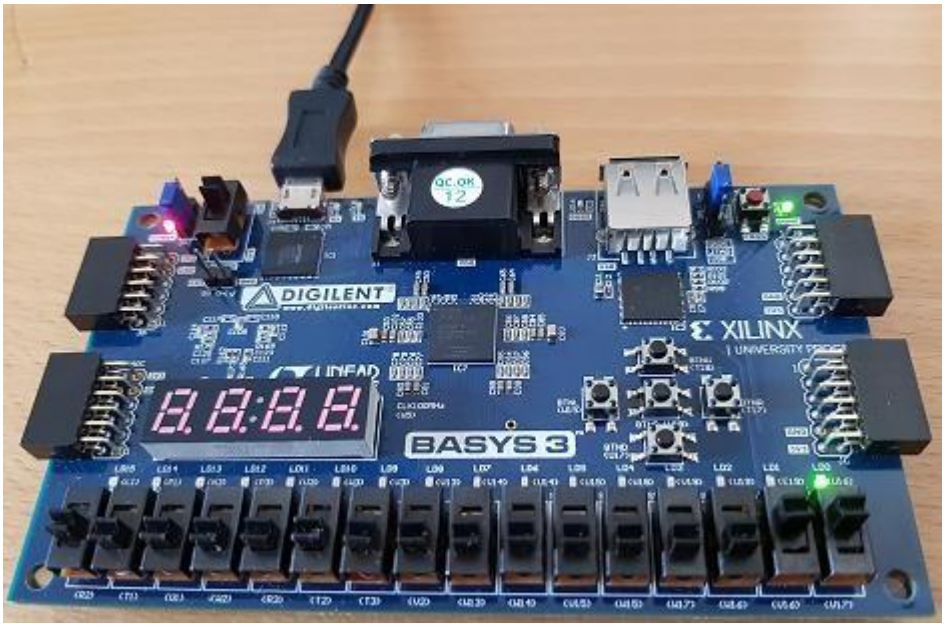


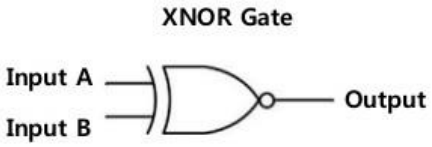

*Figure 6 - Implemented XNOR logic gate on the BASYS 3 Board*

The XNOR gate is a digital logic gate whose function is the logical complement of the exclusive OR gate.

## 4.0 Analysis

- Comments on the results

The result proves that the logic XNOR gate works flawlessly on the board as well as on the Vivado software. The two-input version implements logical equality, behaving according to the truth table.




| Input A | Input B | Output |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

A ⊙ B = Y

*Figure 7 - XNOR Logic Gate*

The result shows that if input A and input B are high (1) then the output will be high (1) and if input A and input B are low (0) then the output will be high.

However, if the comparator receives high input A (1) but low Input B then the logic outputs low (0). If the comparator receives high input B (1) but low Input A (0) then the logic outputs low (0).

## 5.0 Conclusions

- Learning from the results and the research findings

This lab helped me to learn how to write the Verilog HDL code for a 1-bit comparator and learned how to program the BASYS 3 board and simulate it in the Vivado software. My knowledge about the FPGAS has gained.

- FPGA can execute a function faster than a CPU as FPGA can perform parallel processing at a faster rate.
- FPGA is reprogrammable even after the circuit has been designed and implemented meaning they are reprogrammable and reusable.
- No expensive tools are required to design or configure an FPGA chip.
- FPGAs are designed in a higher description language called HDL which is a modular programming code. Using HDL code, such as VHDL or Verilog makes the design process extremely fast and efficient. Thus, it has a faster time to market.
- FPGAs are ideal for real-time applications.

The most things learned while watching a few videos during the lab about the Basys 3 board. This board has a lot of good capabilities such as, 20,800 6-input Look Up Tables, 41,600 flipflops, 1800 Kbits of fast block Ram, 90 DSP slices, and an On-chip analogue/digital converter.

- Suggestions on improving the laboratory exercise

The laboratory exercise can be improved by involving practical work in labs face-face where students can ask questions freely. As we learn more from the questions we ask and the mistakes we make. It is crucial to get experience from practical hands-on exercises to be able to gain practical skills which help to gain knowledge effectively.

## 6.0 References

[1] "Doulos", Doulos.com, 2022. [Online]. Available: https://www.doulos.com/knowhow/perl/testbench_creation/. [Accessed: 08- Feb- 2022]

[2] D. Schwarzbacher, Laboratory 1. TUDUBLIN, 2022, p. 32 [Online]. Available: https://brightspace.tudublin.ie/d2l/le/content/189139/viewContent/1380826/View. [Accessed: 06- Feb- 2022]

[3] "Implementation of VHDL Design in Vivado and IO Pin Planning in Vivado", Youtube.com, 2022. [Online]. Available: https://www.youtube.com/watch?v=JtixlupNSOQ. [Accessed: 06- Feb- 2022]

Submission Checklist

1. The cover page is appropriately complete. ☑
2. The six sections in the body of the report are complete. ☑
3. The constructive feedback from a collaborator is addressed. ☑
4. A final spell-check is completed. ☑
5. A backup copy of the report is online. ☑