SCHOOL OF
ELECTRICAL AND
ELECTRONIC
ENGINEERING

Laboratory 1

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Laboratory: Basic Design Flow

September 2018

Comparator

- In this laboratory, the Vivado Design Environment will be used to design, simulate and synthesise a digital comparator circuit
- Finally, the functionality of the finished design will be tested by implementing it and programming it onto the Artix-7 FPGA of the Digilent Basys3 board

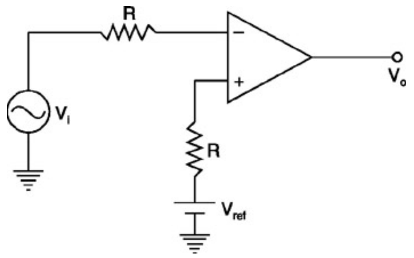
Learning Objectives

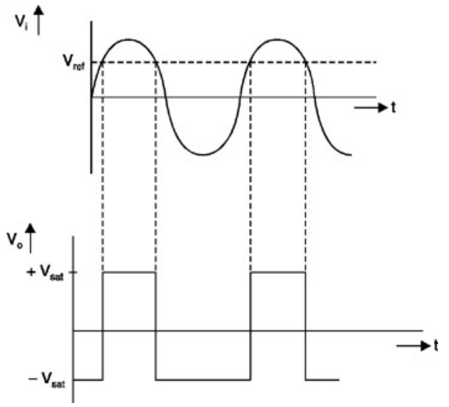
In this laboratory, you will:

- Create VHDL design source code
- Create a VHDL simulation code to test the design
- Implement the design on the Basys 3 development board based on Artix-7 FPGA
- Apply signals to the board via the switches to confirm that the design works as planned

An Analogue Comparator

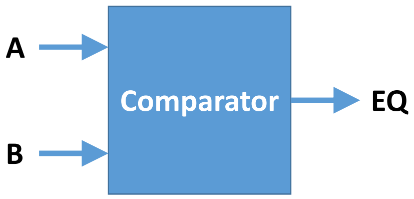
- The output of an analogue comparator is high when the input signal equals or exceeds the reference signal





A Digital Comparator

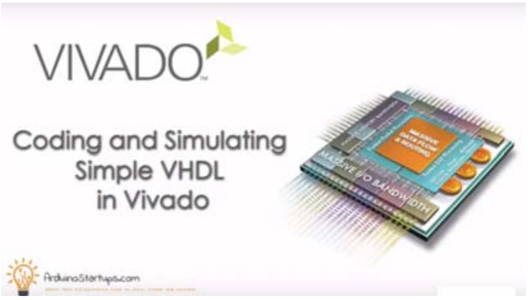
- A 1-bit digital comparator provides an “1” output when inputs A and B are equal i.e. two “1’s” or two “0’s”



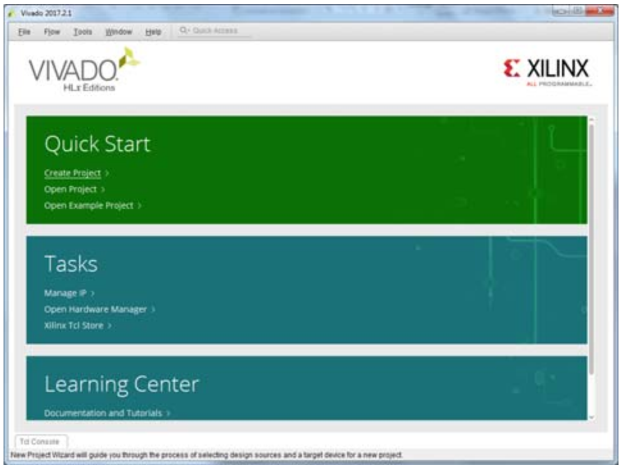
A	B	EQ
0	0	1
0	1	0
1	0	0
1	1	1

YouTube – Look at old work flow (ver. 2016.2)

- Take a look at the following video to get oriented on the work flow.
- http://www.youtube.com/watch?v=ShjXQdKdxsE



Create a new project



New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

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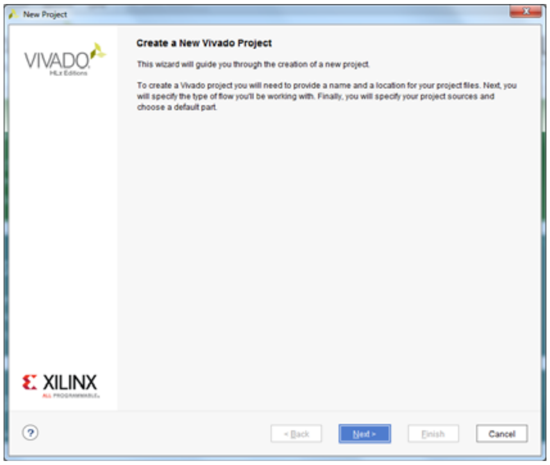
Create a new project



Create a New Vivado Project

This wizard will guide you through the creation of a new project.

To create a Vivado project you will need to provide a name and a location for your project files. Next, you will specify the type of flow you'll be working with. Finally, you will specify your project sources and choose a default part.

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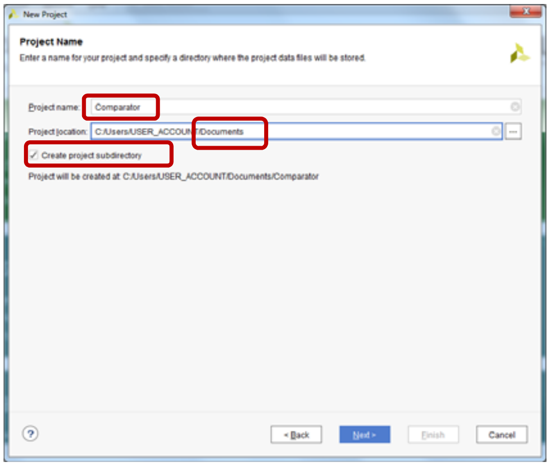
Select a project name and location



New Project

Project Name

Enter a name for your project and specify a directory where the project data files will be stored.

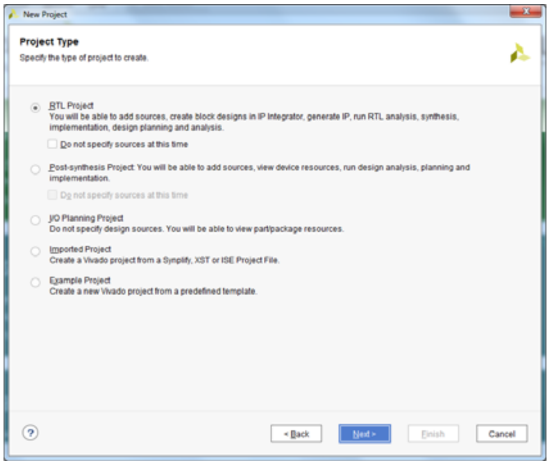
Project name: Comparator

Project location: C:/Users/USER_ACCOUNT/Documents

☑ Create project subdirectory

Project will be created at: C:/Users/USER_ACCOUNT/Documents/Comparator

Select Register-Transfer Level (RTL) project



New Project

Project Type

Specify the type of project to create.

● RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.

□ Do not specify sources at this time

○ Post-synthesis Project: You will be able to add sources, view device resources, run design analysis, planning and implementation.

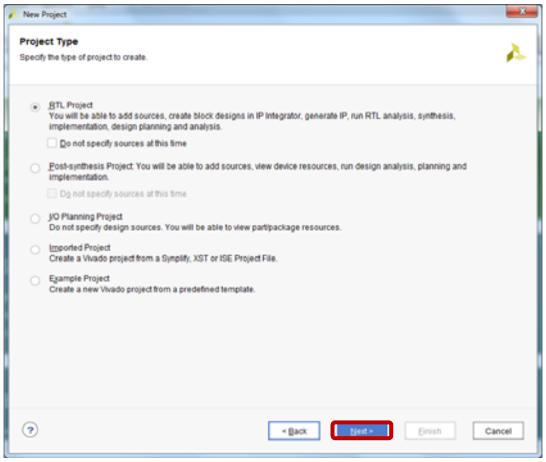
□ Do not specify sources at this time

○ I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.

○ Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.

○ Example Project
Create a new Vivado project from a predefined template.

Create a source file

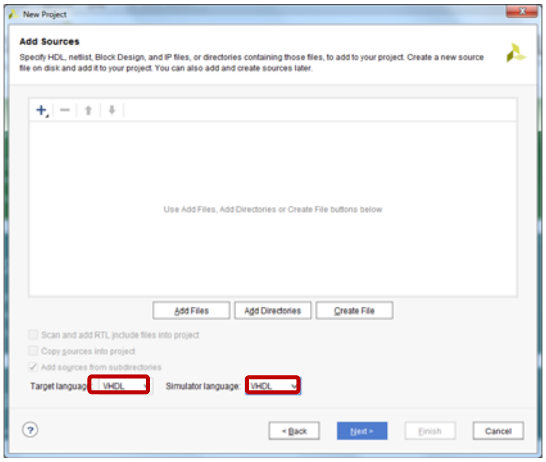


New Project

Project Type

Specify the type of project to create.

- ● RTL Project
  You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
  - □ Do not specify sources at this time
- ○ Post-synthesis Project: You will be able to add sources, view device resources, run design analysis, planning and implementation.
  - □ Do not specify sources at this time
- ○ I/O Planning Project
  Do not specify design sources. You will be able to view part/package resources.
- ○ Imported Project
  Create a Vivado project from a Synplify, XST or ISE Project File.
- ○ Example Project
  Create a new Vivado project from a predefined template.



New Project

Add Sources

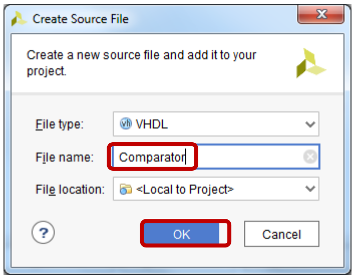
Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.

Use Add Files, Add Directories or Create File buttons below

- □ Scan and add RTL include files into project
- □ Copy sources into project
- ☑ Add sources from subdirectories

Target language: VHDL   Simulator language: VHDL

Create a source file



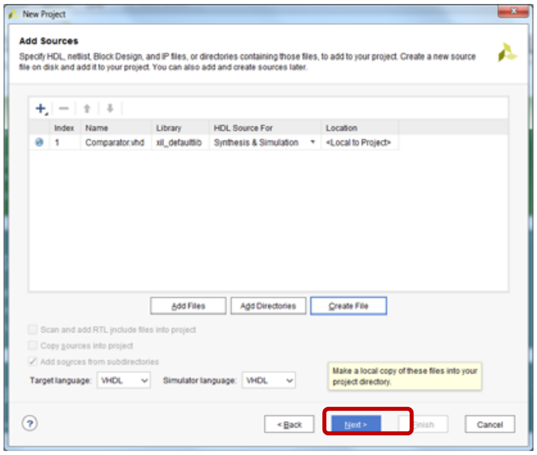
Create Source File

Create a new source file and add it to your project.

File type: VHDL

File name: Comparator

File location: <Local to Project>



New Project

Add Sources

Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.

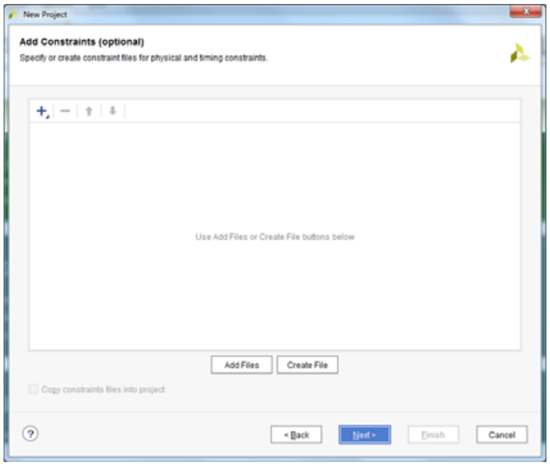
Index	Name	Library	HDL Source For	Location
1	Comparator.vhd	xil_defaultlib	Synthesis & Simulation	<Local to Project>

- □ Scan and add RTL include files into project
- □ Copy sources into project
- ☑ Add sources from subdirectories

Target language: VHDL   Simulator language: VHDL

Make a local copy of these files into your project directory.

A constraints (.cdx) file will be created later



New Project

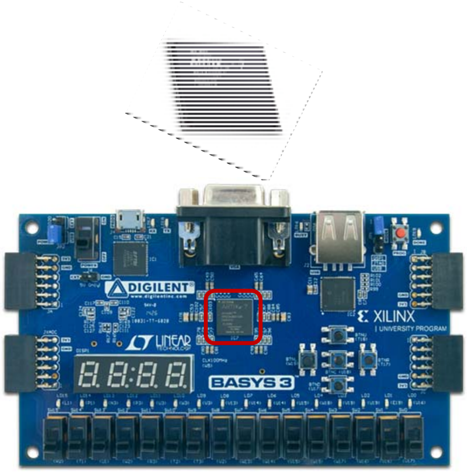
Add Constraints (optional)

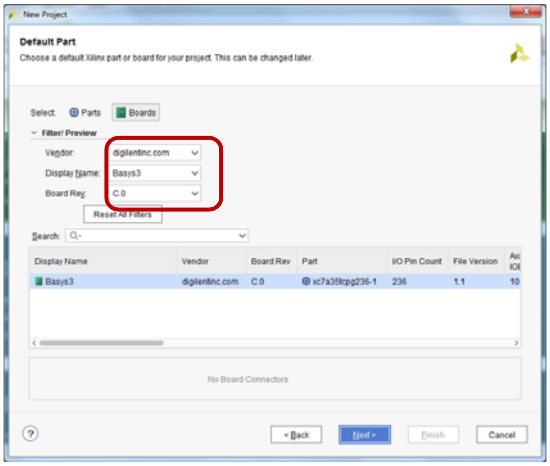
Specify or create constraint files for physical and timing constraints.

Use Add Files or Create File buttons below

☐ Copy constraints files into project

Select the Basys3 board type





New Project

Default Part

Choose a default Xilinx part or board for your project. This can be changed later.

Select: ○ Parts ● Boards

Filter/ Preview

Vendor: digilentinc.com

Display Name: Basys3

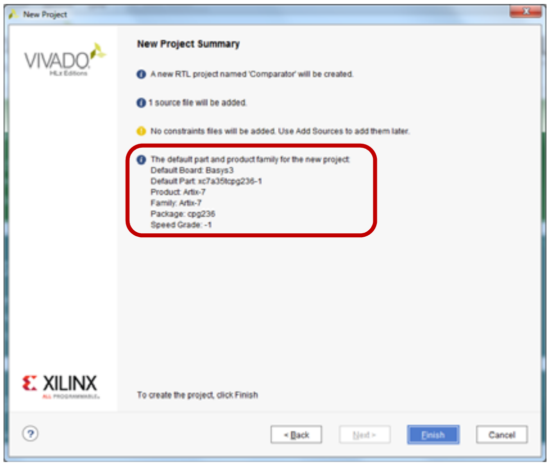
Board Rev: C.0

Search: Q-

Display Name	Vendor	Board Rev	Part	I/O Pin Count	File Version	Av IOE
Basys3	digilentinc.com	C.0	xc7a35tcpg236-1	236	1.1	10

No Board Connectors

Note project summary



New Project

New Project Summary

A new RTL project named 'Comparator' will be created.

1 source file will be added.

No constraints files will be added. Use Add Sources to add them later.

The default part and product family for the new project:
Default Board: Basys3
Default Part: xc7a35tcpg236-1
Product: Artix-7
Family: Artix-7
Package: cpg236
Speed Grade: -1

To create the project, click Finish

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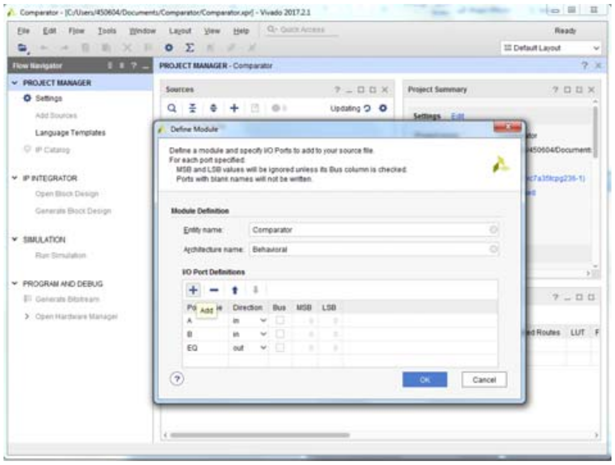
Set the port names and directions



Comparator - [C:/Users/450604/Documents/Comparator/Comparator.xpr] - Vivado 2017.2.1

Define Module

Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.

Module Definition

Entity name: Comparator

Architecture name: Behavioral

I/O Port Definitions

Po Add e	Direction	Bus	MSB	LSB
A	in	□	0	0
B	in	□	0	0
EQ	out	□	0	0

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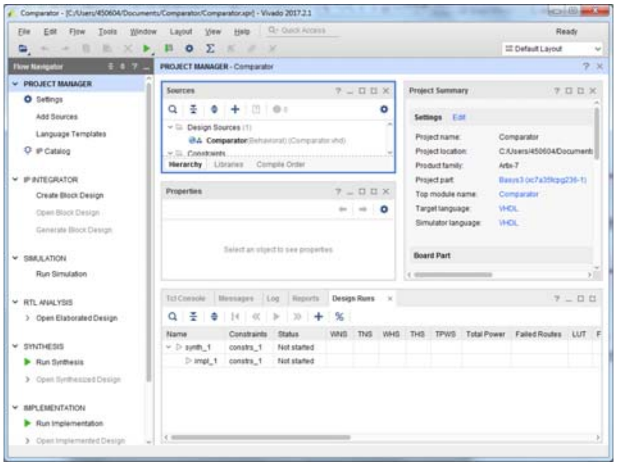
Design environment

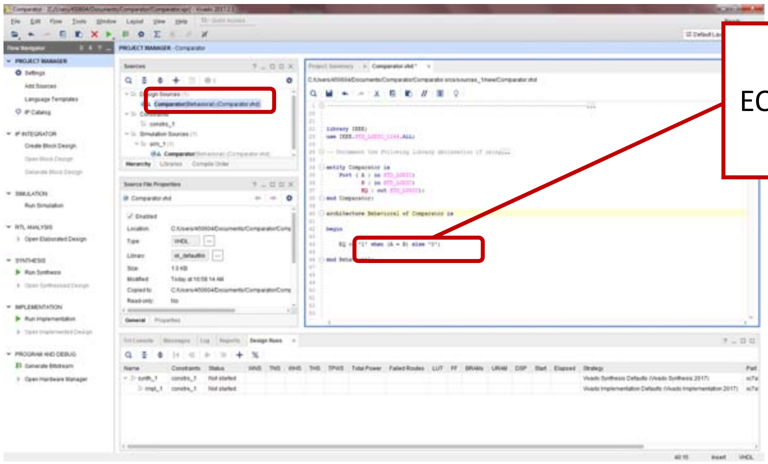


Comparator - [C:/Users/450604/Documents/Comparator/Comparator.xpr] - Vivado 2017.2.1

Project name: Comparator
Project location: C:/Users/450604/Documents
Product family: Artix-7
Project part: Basys3 (xc7a35tcpg236-1)
Top module name: Comparator
Target language: VHDL
Simulator language: VHDL

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	F
synth_1	constrs_1	Not started									
impl_1	constrs_1	Not started									

Define comparator behaviour



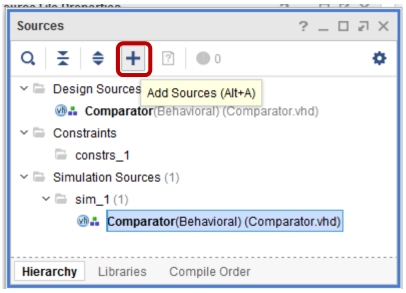
C:/Users/450604/Documents/Comparator/Comparator.srcs/sources_1/new/Comparator.vhd

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using...

entity Comparator is
    Port ( A : in STD_LOGIC;
           B : in STD_LOGIC;
           EQ : out STD_LOGIC);
end Comparator;

architecture Behavioral of Comparator is

begin

    EQ <= '1' when (A = B) else '0';

end Behavioral;
```

EQ <= '1' when (A = B) else '0';

Press “Ctrl” + “s” to save the edits and to verify the syntax of the VHDL code.

Create a “testbench” simulation source file



Sources

Design Sources

Add Sources (Alt+A)

Comparator(Behavioral) (Comparator.vhd)

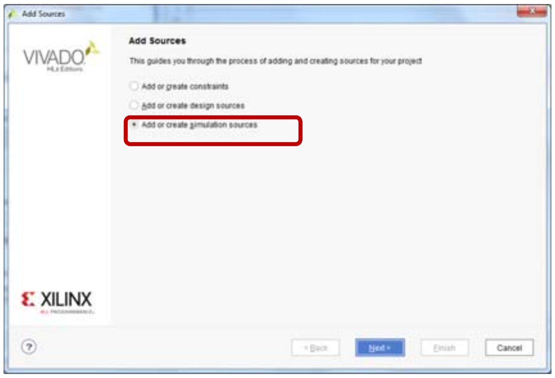
Constraints

constrs_1

Simulation Sources (1)

sim_1 (1)

Comparator(Behavioral) (Comparator.vhd)



Add Sources

Add Sources

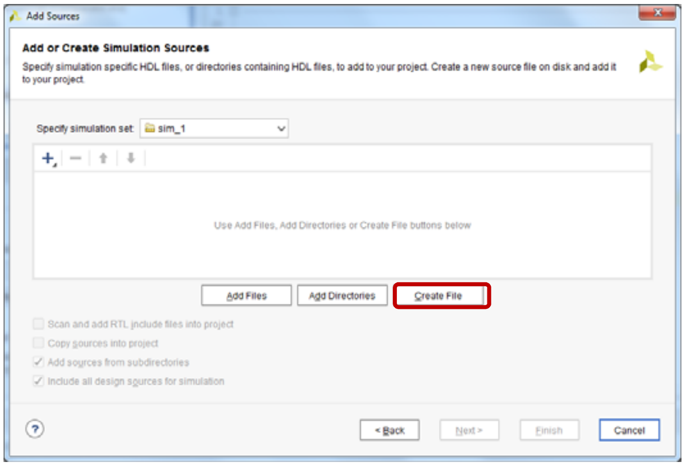
This guides you through the process of adding and creating sources for your project

○ Add or create constraints

○ Add or create design sources

● Add or create simulation sources

Create testbench source file: “Compare_TB”



Add Sources

Add or Create Simulation Sources

Specify simulation specific HDL files, or directories containing HDL files, to add to your project. Create a new source file on disk and add it to your project.

Specify simulation set: sim_1

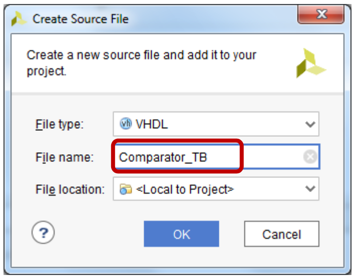
Use Add Files, Add Directories or Create File buttons below

□ Scan and add RTL include files into project

□ Copy sources into project

☑ Add sources from subdirectories

☑ Include all design sources for simulation



Create Source File

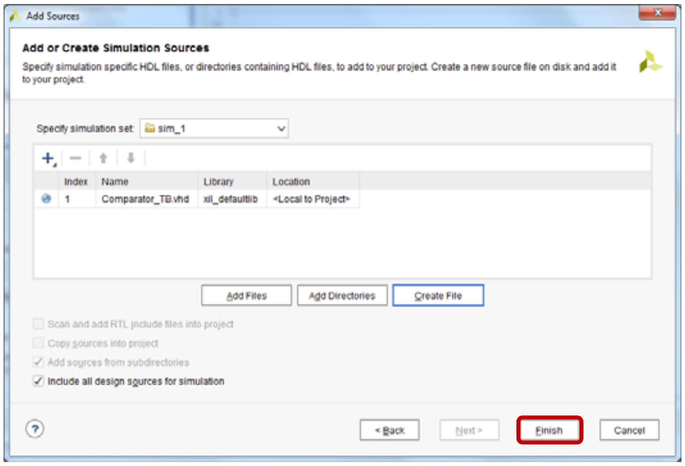
Create a new source file and add it to your project.

File type: VHDL

File name: Comparator_TB

File location: <Local to Project>

Create testbench source file: “Compare_TB”



Add or Create Simulation Sources

Specify simulation specific HDL files, or directories containing HDL files, to add to your project. Create a new source file on disk and add it to your project.

Specify simulation set: sim_1

Index	Name	Library	Location
1	Comparator_TB.vhd	xil_defaultlib	<Local to Project>

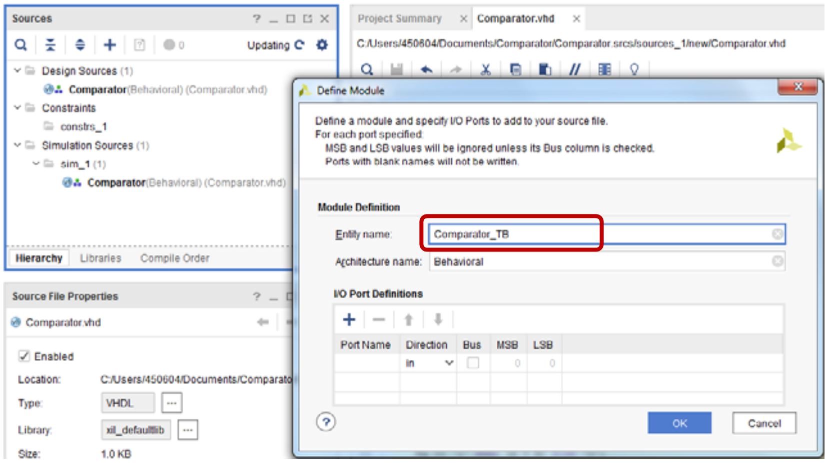
□ Scan and add RTL include files into project

□ Copy sources into project

☑ Add sources from subdirectories

☑ Include all design sources for simulation

Set I/O Ports of the testbench



C:/Users/450604/Documents/Comparator/Comparator.srcs/sources_1/new/Comparator.vhd

☑ Enabled

Location: C:/Users/450604/Documents/Comparato

Type: VHDL

Library: xil_defaultlib

Size: 1.0 KB

Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.

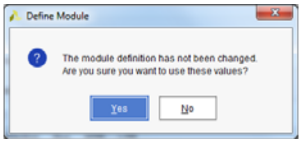
Module Definition

Entity name: Comparator_TB

Architecture name: Behavioral

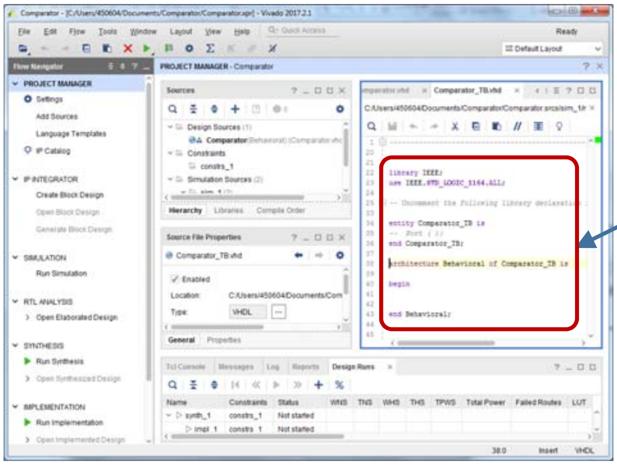
I/O Port Definitions

Port Name	Direction	Bus	MSB	LSB
	in	□	0	0



The module definition has not been changed.
Are you sure you want to use these values?

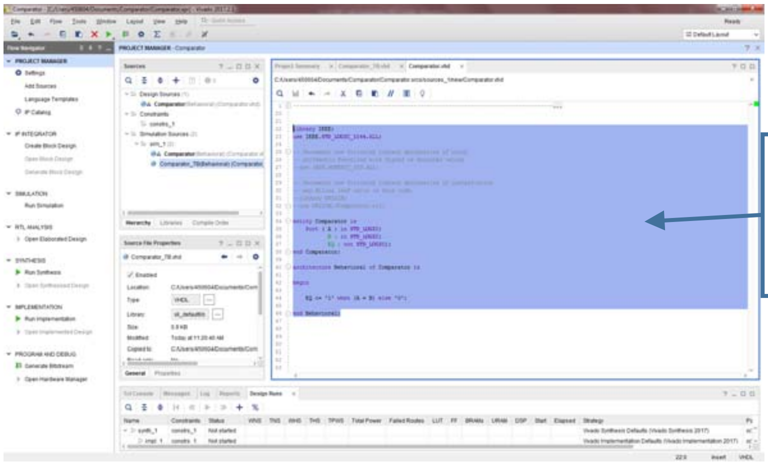
Testbench code



```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration :

entity Comparator_TB is
--  Port ( );
end Comparator_TB;

architecture Behavioral of Comparator_TB is

begin


end Behavioral;
```

Use following steps to **replace** this VHDL simulation code

Copy design source code to clipboard



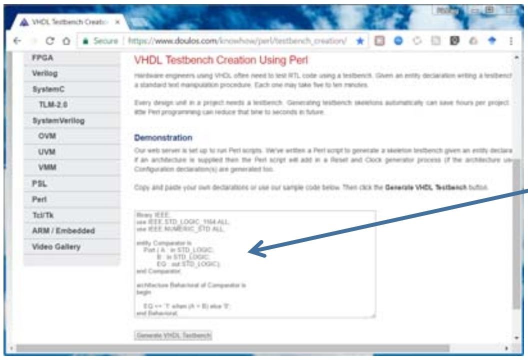
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

[illegible]

entity Comparator is
    Port ( A : in STD_LOGIC;
           B : in STD_LOGIC;
           EQ : out STD_LOGIC);
end Comparator;

architecture Behavioral of Comparator is

begin

    EQ <= '1' when (A = B) else '0';

end Behavioral;
```

Copy design source code from Compare.vhd file

Generate testbench VHDL code

Use online VHDL Testbench Editor to generate code

- https://www.doulos.com/knowhow/perl/testbench_creation/



VHDL Testbench Creation Using Perl

Hardware engineers using VHDL often need to test RTL code using a testbench. Given an entity declaration writing a testbench a standard text manipulation procedure. Each one may take five to ten minutes.

Every design unit in a project needs a testbench. Generating testbench skeletons automatically can save hours per project little Perl programming can reduce that time to seconds in future.

Demonstration

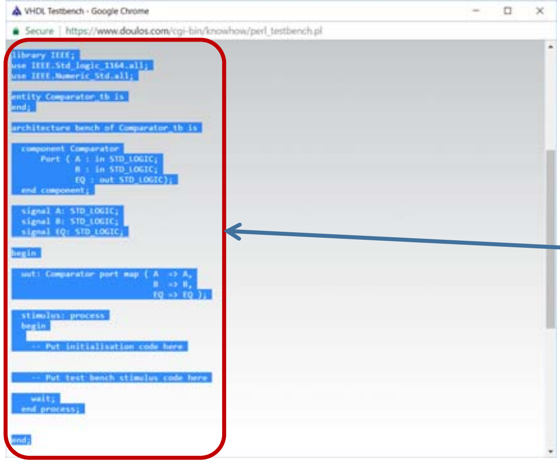
Our web server is set up to run Perl scripts. We've written a Perl script to generate a skeleton testbench given an entity declara If an architecture is supplied then the Perl script will add in a Reset and Clock generator process (if the architecture us Configuration declaration(s) are generated too.

Copy and paste your own declarations or use our sample code below. Then click the **Generate VHDL Testbench** button.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity Comparator is
   Port ( A : in STD_LOGIC;
          B : in STD_LOGIC;
          EQ : out STD_LOGIC);
end Comparator;

architecture Behavioral of Comparator is
begin

   EQ <= '1' when (A = B) else '0';
end Behavioral;
```

Paste the design source code (Compare.vhd) into the online editor. Generate new VHDL simulator code for testing the design.

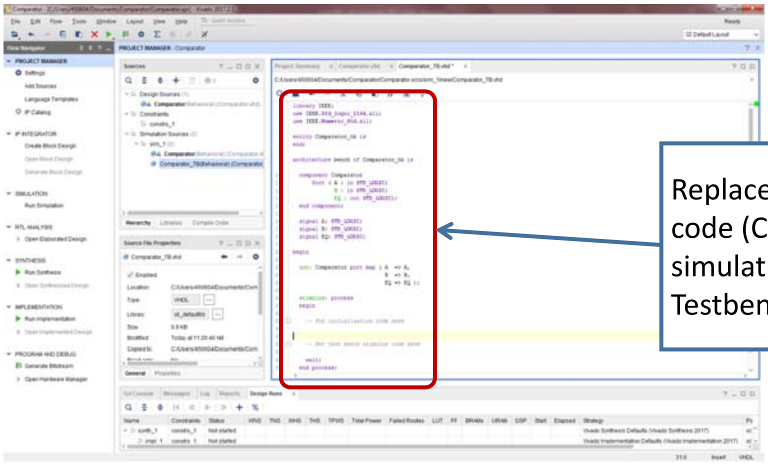
Copy testbench VHDL code


VHDL Testbench - Google Chrome
Secure
https://www.doulos.com/cgi-bin/knowhow/perl_testbench.pl

```
library IEEE;
use IEEE.Std_logic_1164.all;
use IEEE.Numeric_Std.all;

entity Comparator_tb is
end;

architecture bench of Comparator_tb is

  component Comparator
      Port ( A : in STD_LOGIC;
             B : in STD_LOGIC;
             EQ : out STD_LOGIC);
  end component;

  signal A: STD_LOGIC;
  signal B: STD_LOGIC;
  signal EQ: STD_LOGIC;

begin

  uut: Comparator port map ( A  => A,
                             B  => B,
                             EQ => EQ );

  stimulus: process
  begin

    -- Put initialisation code here


    -- Put test bench stimulus code here

    wait;
  end process;


end;
```

Highlight and copy this sub-section of the VHDL simulator code from the online Testbench generator

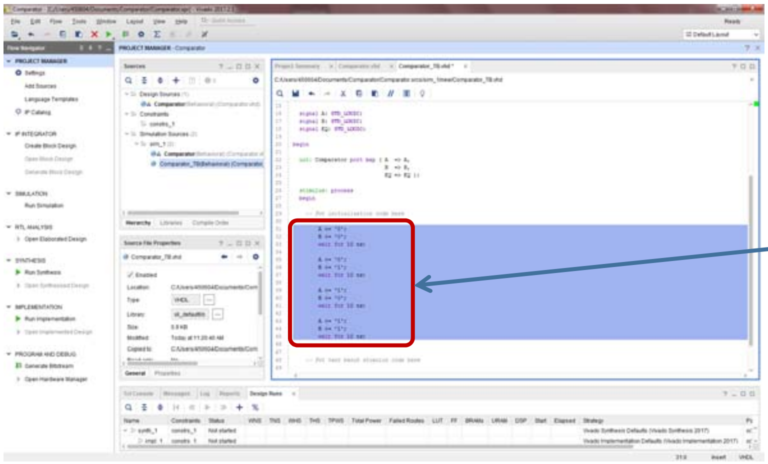
Paste testbench VHDL code



```
library IEEE;
use IEEE.Std_logic_1164.all;
use IEEE.Numeric_Std.all;

entity Comparator_tb is
end;

architecture bench of Comparator_tb is

  component Comparator
      Port ( A : in STD_LOGIC;
             B : in STD_LOGIC;
             EQ : out STD_LOGIC);
  end component;

  signal A: STD_LOGIC;
  signal B: STD_LOGIC;
  signal EQ: STD_LOGIC;

begin

  uut: Comparator port map ( A  => A,
                             B  => B,
                             EQ => EQ );

  stimulus: process
  begin

    -- Put initialization code here

    -- Put test bench stimulus code here

    wait;
  end process;
```

Replace Vivado VHDL simulator code (Compare_TB.vhd) with simulation code from the online Testbench generator

Edit testbench VHDL code



```
  signal A: STD_LOGIC;
  signal B: STD_LOGIC;
  signal EQ: STD_LOGIC;

begin

  uut: Comparator port map ( A  => A,
                             B  => B,
                             EQ => EQ );

  stimulus: process
  begin

    -- Put initialization code here

      A <= '0';
      B <= '0';
      wait for 10 ns;

      A <= '0';
      B <= '1';
      wait for 10 ns;

      A <= '1';
      B <= '0';
      wait for 10 ns;

      A <= '1';
      B <= '1';
      wait for 10 ns;

    -- Put test bench stimulus code here
```

Add the following stimulus code into the Compare_TB.vhd source:

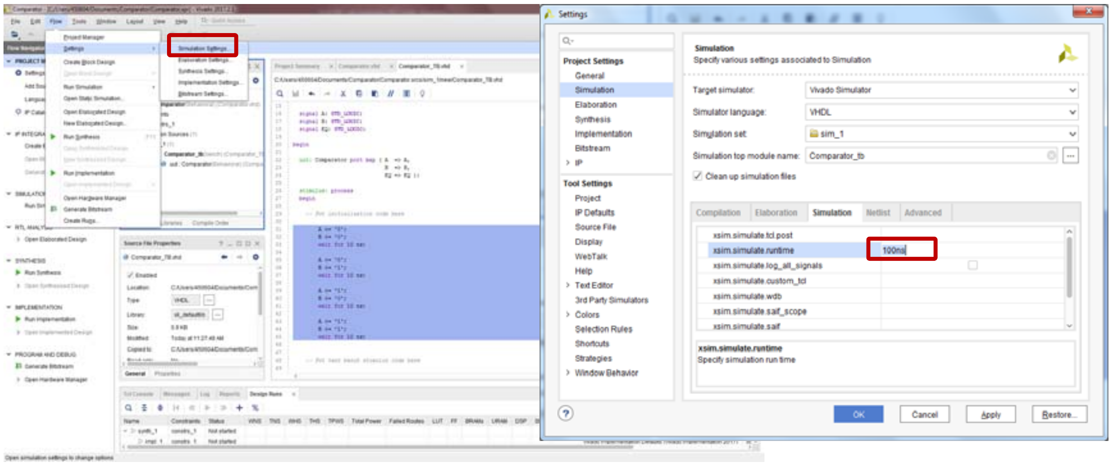
A <= '0';
B <= '0';
wait for 10 ns;

A <= '0';
B <= '1';
wait for 10 ns;

A <= '1';
B <= '0';
wait for 10 ns;

A <= '1';
B <= '1';
wait for 10 ns;

Simulation settings: runtime 100 ns



```
signal A: STD_LOGIC;
signal B: STD_LOGIC;
signal EQ: STD_LOGIC;

begin

  uut: Comparator port map ( A  => A,
                             B  => B,
                             EQ => EQ );

  stimulus: process
  begin

    -- Put initialization code here

      A <= '0';
      B <= '0';
      wait for 10 ns;

      A <= '0';
      B <= '1';
      wait for 10 ns;

      A <= '1';
      B <= '0';
      wait for 10 ns;

      A <= '1';
      B <= '1';
      wait for 10 ns;


    -- Put test bench stimulus code here
```

Settings

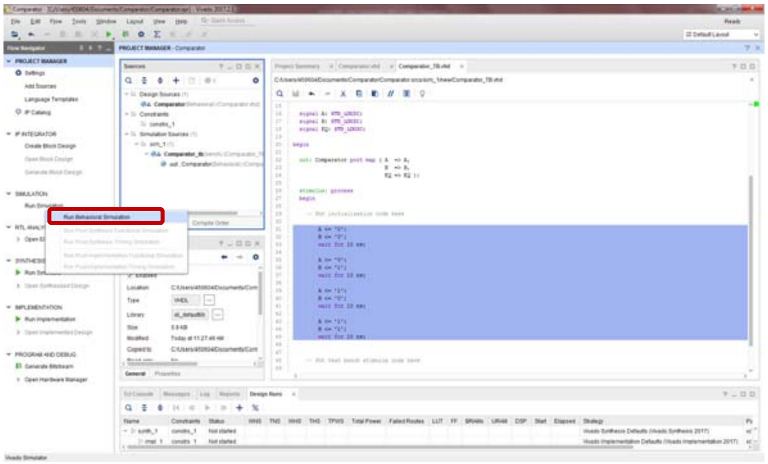
Simulation
Specify various settings associated to Simulation

Target simulator: Vivado Simulator
Simulator language: VHDL
Simulation set: sim_1
Simulation top module name: Comparator_tb
☑ Clean up simulation files

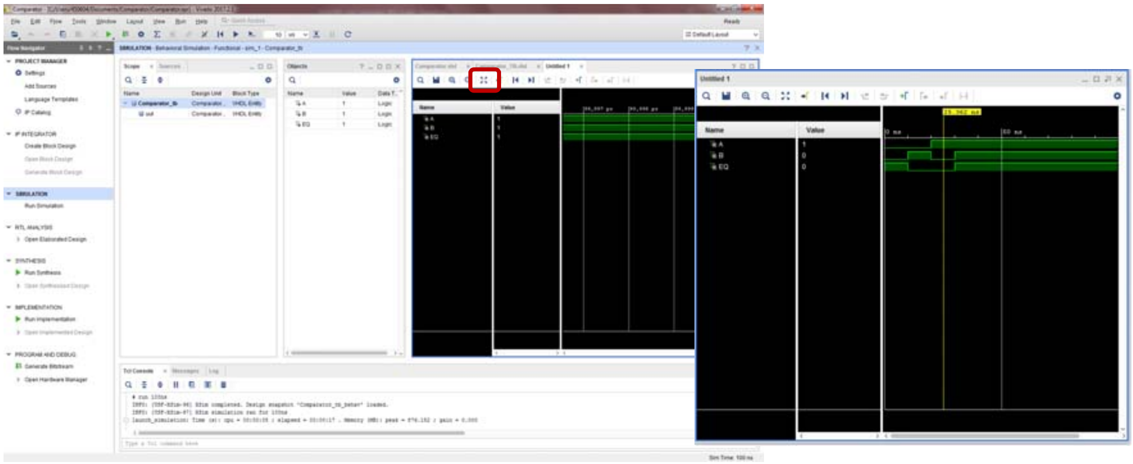
xsim.simulate.tcl.post
xsim.simulate.runtime 100ns
xsim.simulate.log_all_signals □
xsim.simulate.custom_tcl
xsim.simulate.wdb
xsim.simulate.saif_scope
xsim.simulate.saif

xsim.simulate.runtime
Specify simulation run time

Run behavioural simulation

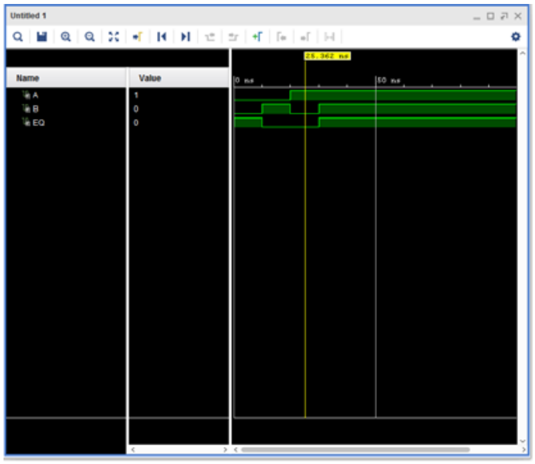


Zoom-fit the simulation results



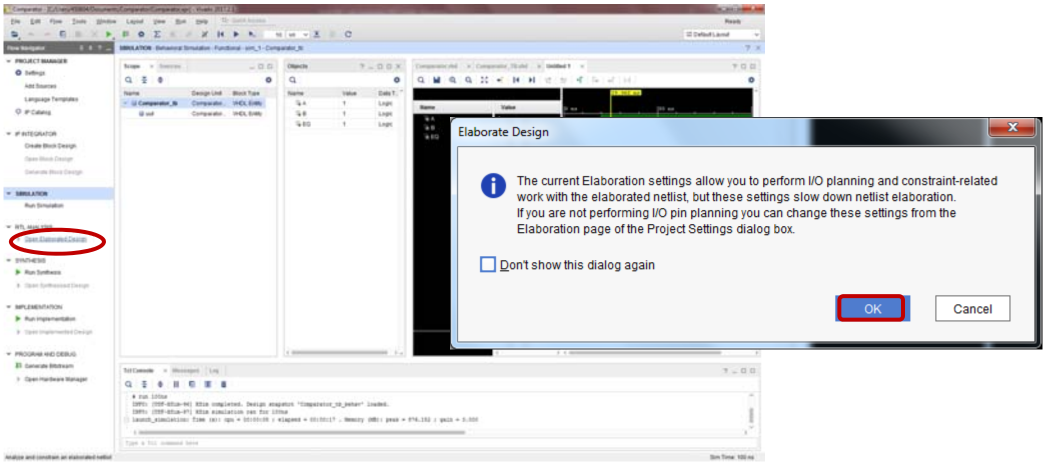
```
# run 100ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'Comparator_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 100ns
launch_simulation: Time (s): cpu = 00:00:08 ; elapsed = 00:00:17 . Memory (MB): peak = 876.152 ; gain = 0.000
```

Check the simulation with a marker



A	B	EQ
0	0	1
0	1	0
1	0	0
1	1	1

Open elaborated design



Elaborate Design

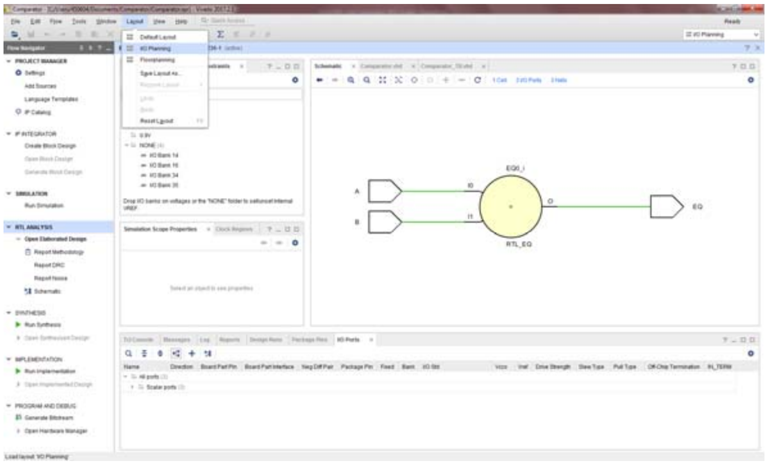
The current Elaboration settings allow you to perform I/O planning and constraint-related work with the elaborated netlist, but these settings slow down netlist elaboration.
If you are not performing I/O pin planning you can change these settings from the Elaboration page of the Project Settings dialog box.

□ Don't show this dialog again

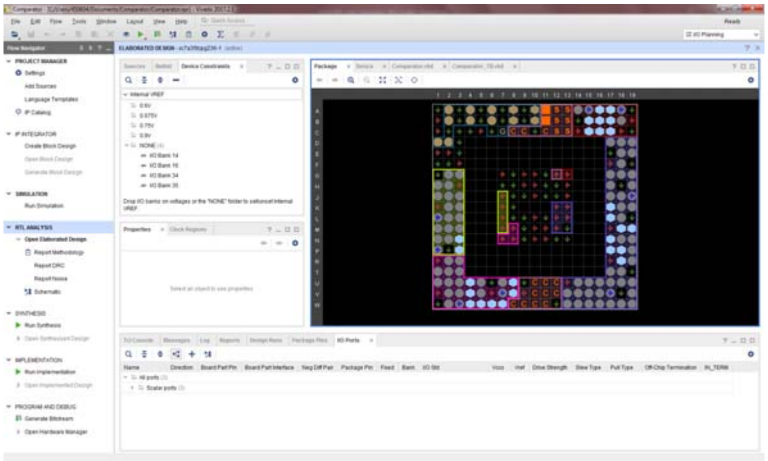
OK Cancel

```
# run 100ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'Comparator_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 100ns
launch_simulation: Time (s): cpu = 00:00:08 ; elapsed = 00:00:17 . Memory (MB): peak = 876.152 ; gain = 0.000
```

Elaborated design – RTL view

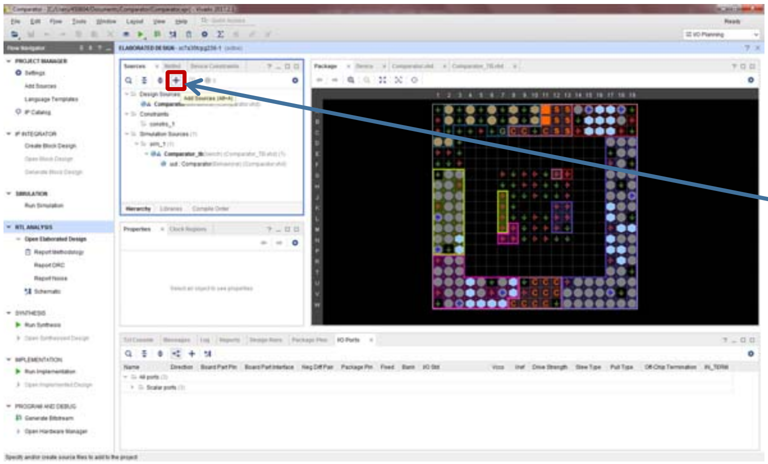


Elaborated design package



35

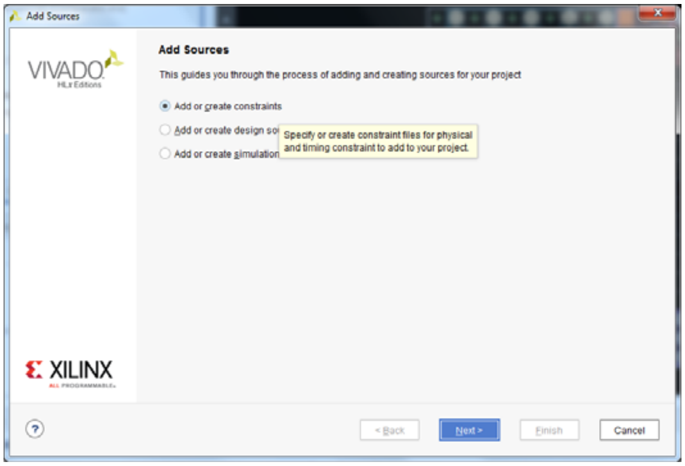
Create a constraints file



Add a source file

36

Create a constraints file



Add Sources

This guides you through the process of adding and creating sources for your project

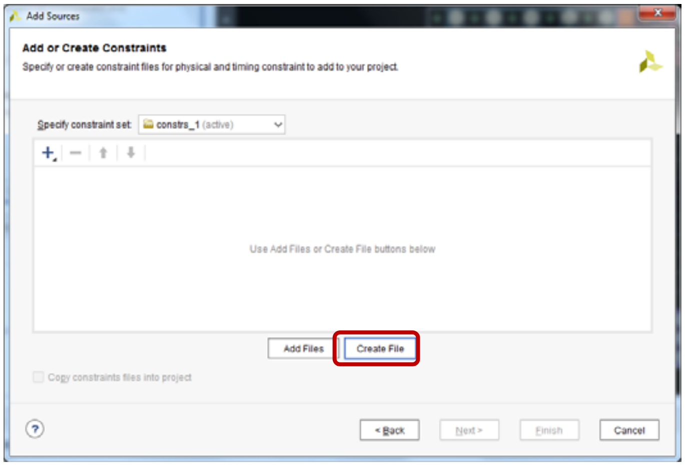
● Add or create constraints

○ Add or create design so

○ Add or create simulation

Specify or create constraint files for physical and timing constraint to add to your project.

Create a constraints file



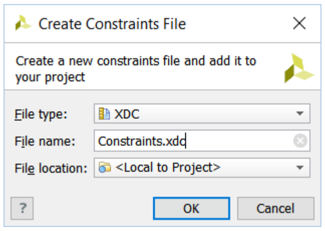
Add or Create Constraints

Specify or create constraint files for physical and timing constraint to add to your project.

Specify constraint set: constrs_1 (active)

Use Add Files or Create File buttons below

□ Copy constraints files into project



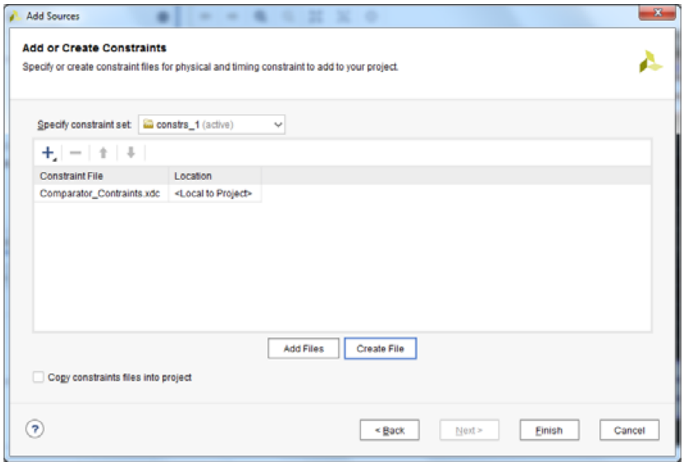
Create a new constraints file and add it to your project

File type: XDC

File name: Constraints.xdc

File location: <Local to Project>

Create a constraints file



Add Sources

Add or Create Constraints

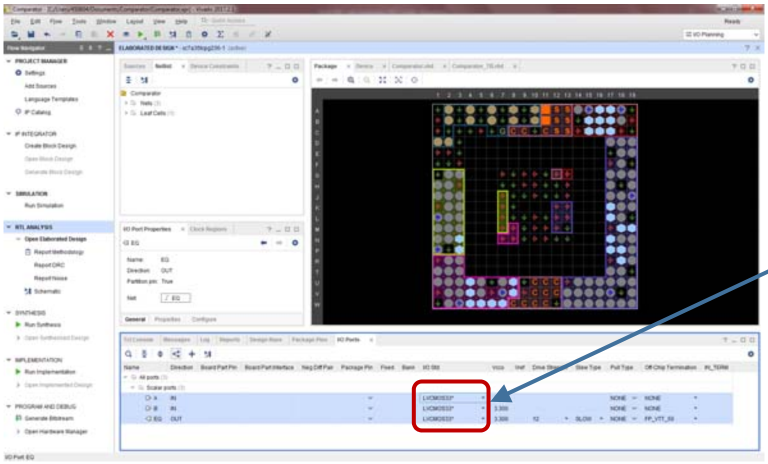
Specify or create constraint files for physical and timing constraint to add to your project.

Specify constraint set: constrs_1 (active)

Constraint File	Location
Comparator_Contraints.xdc	<Local to Project>

□ Copy constraints files into project

Set IO pin voltage levels to LV CMOS 3.3 V



IO Port Properties

EQ

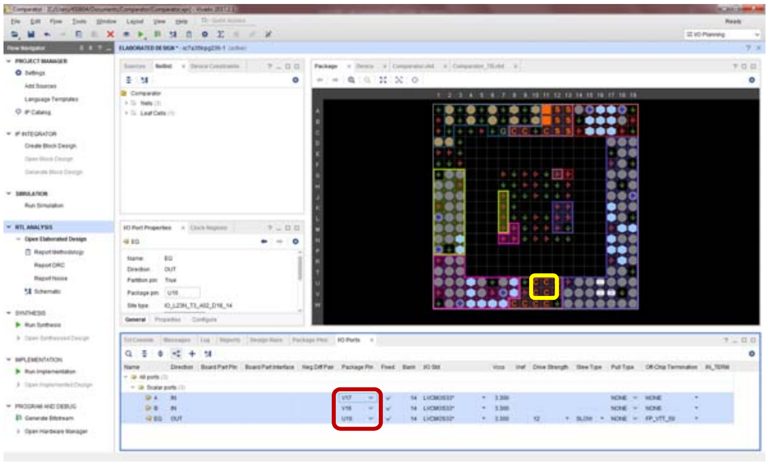
Name: EQ
Direction: OUT
Partition pin: True
Net: EQ

IO Ports

Name	Direction	Board Part Pin	Board Part Interface	Neg Diff Pair	Package Pin	Fixed	Bank	IO Std	Vcco	Vref	Drive Strength	Slew Type	Pull Type	Off Chip Termination	IN_TERM
All ports (3)															
Scalar ports (3)															
A	IN							LVCMOS33*					NONE	NONE	
B	IN							LVCMOS33*	3.300				NONE	NONE	
EQ	OUT							LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_50	

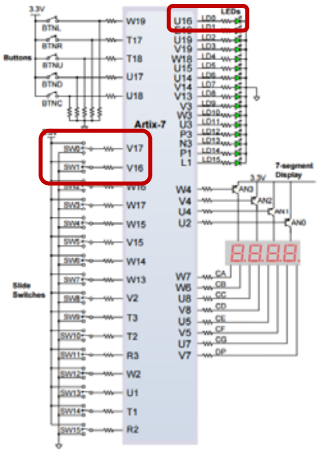
Select LVCMOS33 for the 3.3 V level of the Basys3 IO Pins

Select I/O Planning view and I/O Pins

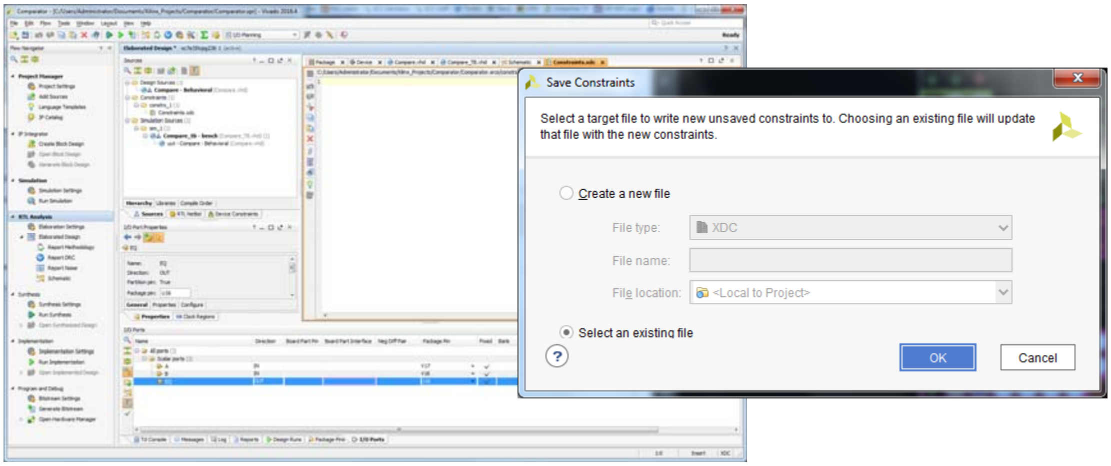


Name: EQ
Direction: OUT
Partition pin: True
Package pin: U16
Site type: IO_L23N_T3_A02_D18_14

Name	Direction	Board Part Pin	Board Part Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Pull Type	Off-Chip Termination	IN_TERM
All ports (3)															
Scalar ports (3)															
A	IN				V17	✓	14	LVCMOS33*	3.300				NONE	NONE	
B	IN				V16	✓	14	LVCMOS33*	3.300				NONE	NONE	
EQ	OUT				U16	✓	14	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_50	



Update Contraints.xdc file with Cntl + “s”



Save Constraints

Select a target file to write new unsaved constraints to. Choosing an existing file will update that file with the new constraints.

○ Create a new file

File type: XDC

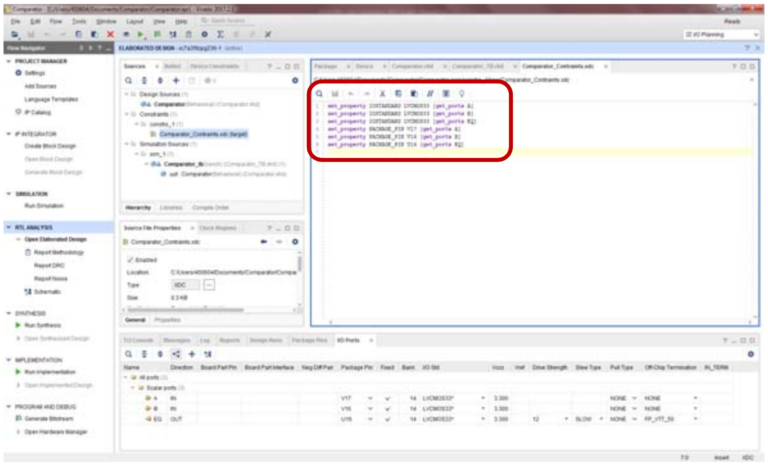
File name:

File location: <Local to Project>

● Select an existing file

OK Cancel

Inspect the updated Constraints.xdc file



```
set_property IOSTANDARD LVCMOS33 [get_ports A]
set_property IOSTANDARD LVCMOS33 [get_ports B]
set_property IOSTANDARD LVCMOS33 [get_ports EQ]
set_property PACKAGE_PIN V17 [get_ports A]
set_property PACKAGE_PIN V16 [get_ports B]
set_property PACKAGE_PIN U16 [get_ports EQ]
```

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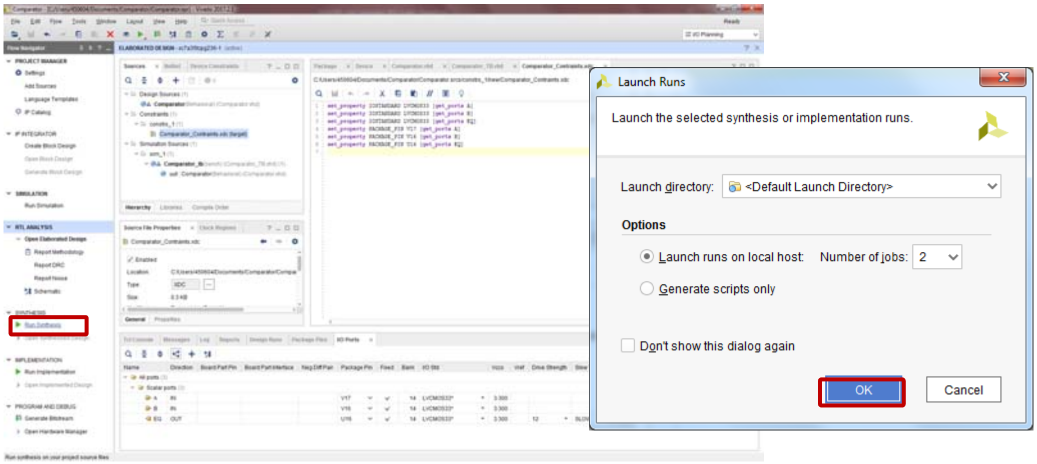
Run synthesis



Launch Runs

Launch the selected synthesis or implementation runs.

Launch directory: <Default Launch Directory>

Options

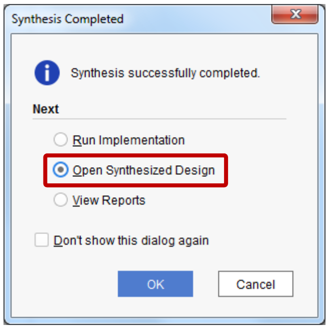
● Launch runs on local host: Number of jobs: 2

○ Generate scripts only

□ Don't show this dialog again

44

Open synthesized design device layout



Synthesis Completed

Synthesis successfully completed.

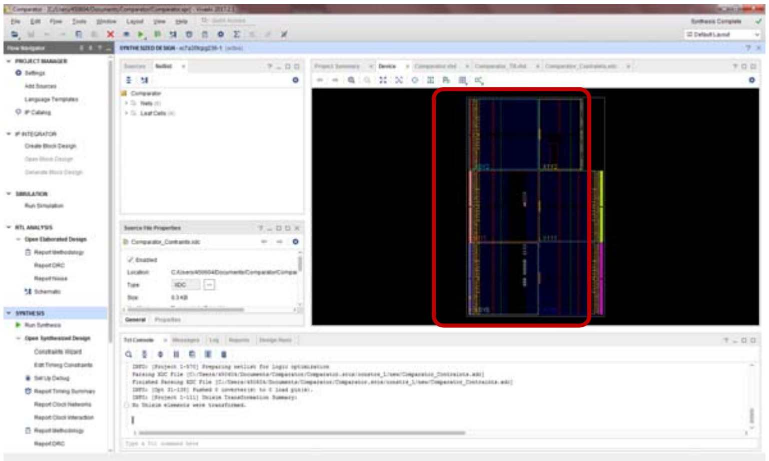
Next

○ Run Implementation

● Open Synthesized Design

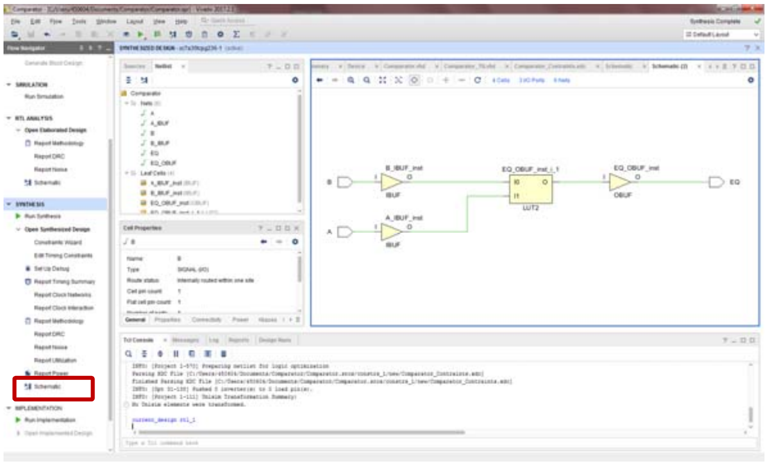
○ View Reports

□ Don't show this dialog again



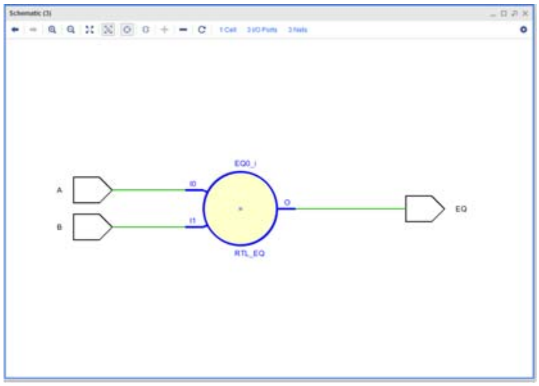
```
INFO: [Project 1-570] Preparing netlist for logic optimization
Parsing XDC File [C:/Users/450604/Documents/Comparator/Comparator.srcs/constrs_1/new/Comparator_Contraints.xdc]
Finished Parsing XDC File [C:/Users/450604/Documents/Comparator/Comparator.srcs/constrs_1/new/Comparator_Contraints.xdc]
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
```

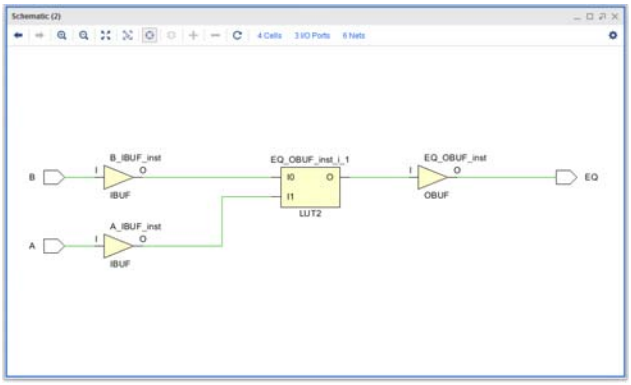
Open synthesized design schematic



```
INFO: [Project 1-570] Preparing netlist for logic optimization
Parsing XDC File [C:/Users/450604/Documents/Comparator/Comparator.srcs/constrs_1/new/Comparator_Contraints.xdc]
Finished Parsing XDC File [C:/Users/450604/Documents/Comparator/Comparator.srcs/constrs_1/new/Comparator_Contraints.xdc]
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

current_design rtl_1
```

Compare RTL and Synthesis Schematics



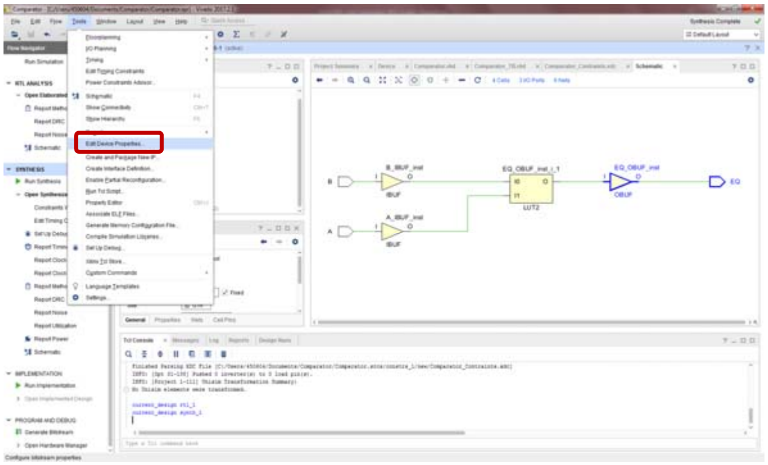


Design reports

- Look at the Synthesis report:
  - Copy of the following table and complete it in your report

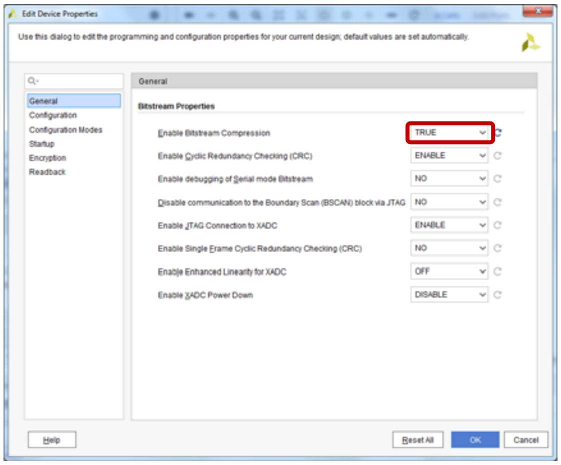
Cell Type Label	Functional Category	What is it used for?
LUT2		
IBUF		
OBUF		

Tools menu: Edit device properties



```
Finished Parsing XDC file [C:/Users/450604/Documents/Comparator/Comparator.srcs/constrs_1/new/Comparator_Contraints.xdc]
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

current_design rtl_1
current_design synth_1
```

Tools menu: Edit device properties

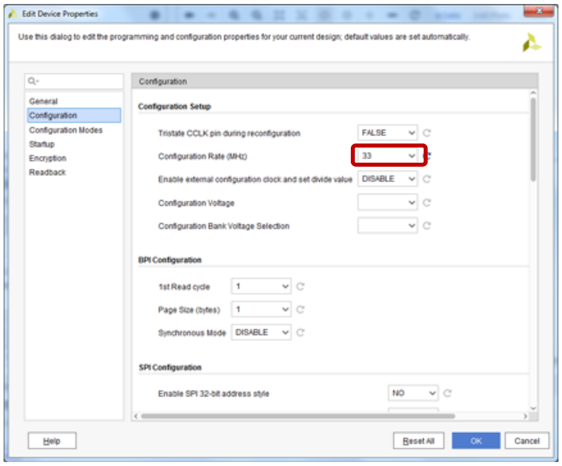


Use this dialog to edit the programming and configuration properties for your current design; default values are set automatically.

General

Bitstream Properties

Enable Bitstream Compression	TRUE
Enable Cyclic Redundancy Checking (CRC)	ENABLE
Enable debugging of Serial mode Bitstream	NO
Disable communication to the Boundary Scan (BSCAN) block via JTAG	NO
Enable JTAG Connection to XADC	ENABLE
Enable Single Frame Cyclic Redundancy Checking (CRC)	NO
Enable Enhanced Linearity for XADC	OFF
Enable XADC Power Down	DISABLE



Use this dialog to edit the programming and configuration properties for your current design; default values are set automatically.

Configuration

Configuration Setup

Tristate CCLK pin during reconfiguration	FALSE
Configuration Rate (MHz)	33
Enable external configuration clock and set divide value	DISABLE
Configuration Voltage	
Configuration Bank Voltage Selection	

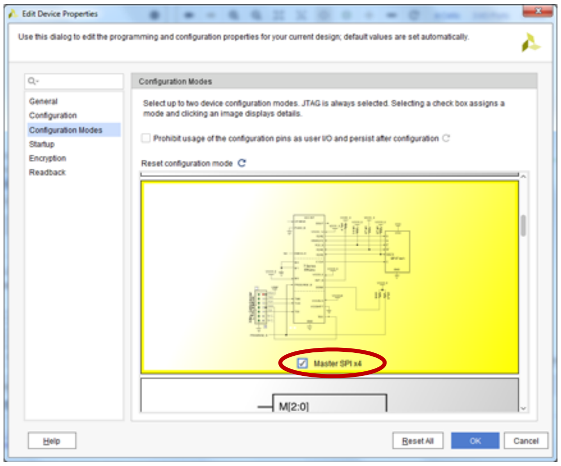
BPI Configuration

1st Read cycle	1
Page Size (bytes)	1
Synchronous Mode	DISABLE

SPI Configuration

Enable SPI 32-bit address style	NO

Edit device properties



Edit Device Properties

Use this dialog to edit the programming and configuration properties for your current design; default values are set automatically.

Configuration Modes

Select up to two device configuration modes. JTAG is always selected. Selecting a check box assigns a mode and clicking an image displays details.

□ Prohibit usage of the configuration pins as user I/O and persist after configuration

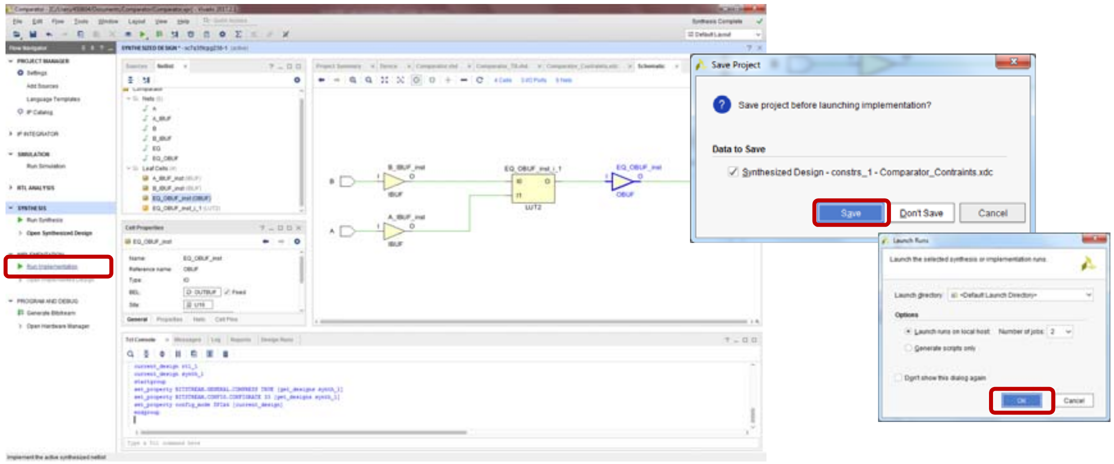
Reset configuration mode

☑ Master SPI x4

Select Serial Peripheral Interface BUS – quad

Examine the Master SPI x4 Configuration Mode Details by doubling clicking SPI image.

Run implementation



Name: EQ_OBUF_inst
Reference name: OBUF
Type: IO
BEL: OUTBUF ✓ Fixed
Site: U16

```
current_design rtl_1
current_design synth_1
startgroup
set_property BITSTREAM.GENERAL.COMPRESS TRUE [get_designs synth_1]
set_property BITSTREAM.CONFIG.CONFIGRATE 33 [get_designs synth_1]
set_property config_mode SPIx4 [current_design]
endgroup
```

Save Project

Save project before launching implementation?

Data to Save

☑ Synthesized Design - constrs_1 - Comparator_Contraints.xdc

Launch Runs

Launch the selected synthesis or implementation runs.

Launch directory: <Default Launch Directory>

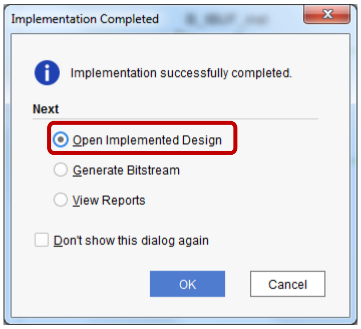
Options

● Launch runs on local host Number of jobs: 2

○ Generate scripts only

□ Don't show this dialog again

Examine leaf cells in the implemented design



Implementation Completed

Implementation successfully completed.

Next

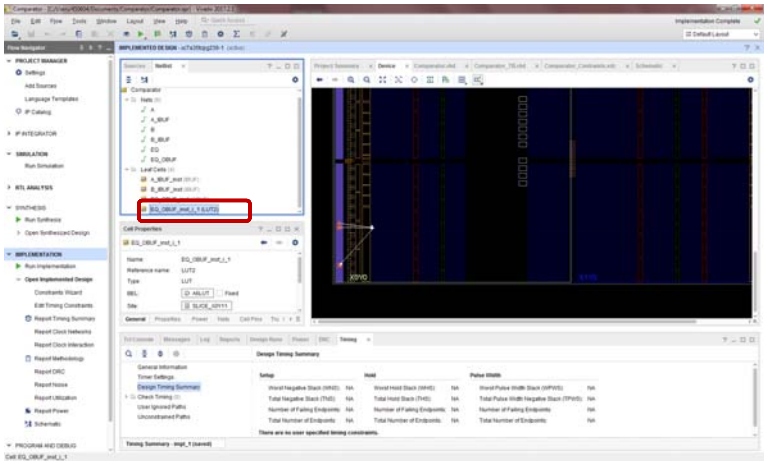
● Open Implemented Design

○ Generate Bitstream

○ View Reports

□ Don't show this dialog again

OK Cancel



IMPLEMENTED DESIGN - xc7a35tcpg236-1 (active)

Netlist

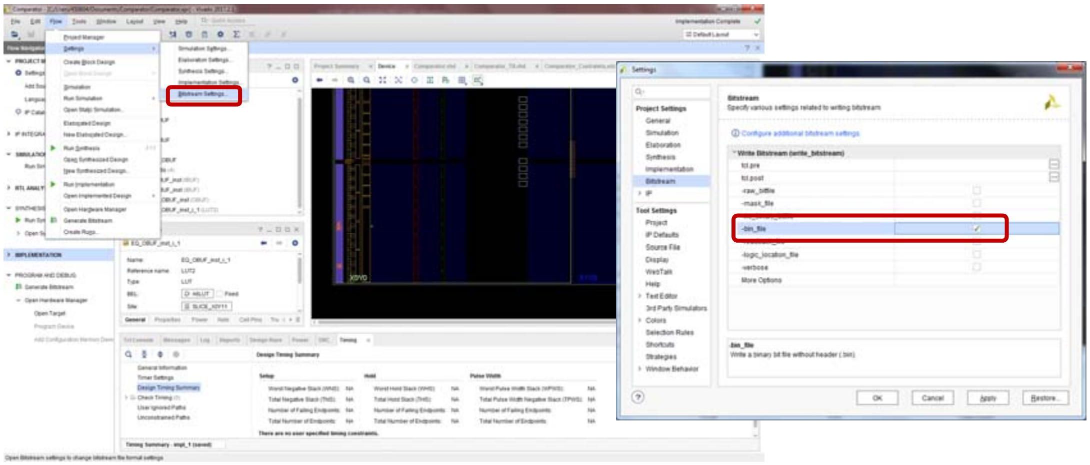
- Comparator
  - Nets
    - A
    - A_IBUF
    - B
    - B_IBUF
    - EQ
    - EQ_OBUF
  - Leaf Cells
    - A_IBUF_inst (IBUF)
    - B_IBUF_inst (IBUF)
    - EQ_OBUF_inst_i_1 (LUT2)

Cell Properties

EQ_OBUF_inst_i_1

Name	EQ_OBUF_inst_i_1
Reference name	LUT2
Type	LUT
BEL	A6LUT □ Fixed
Site	SLICE_X0Y11

Bitstream settings



Settings

Bitstream
Specify various settings related to writing bitstream

Configure additional bitstream settings

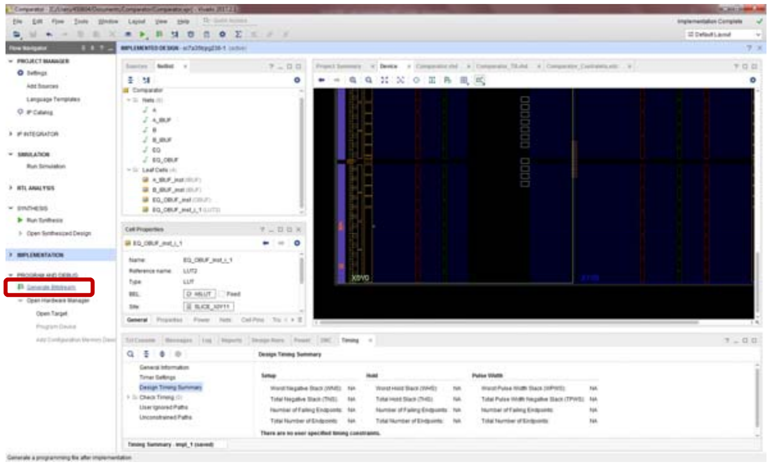
Write Bitstream (write_bitstream)

tcl.pre	
tcl.post	
-raw_bitfile	□
-mask_file	□
-bin_file	☑
-logic_location_file	□
-verbose	□
More Options	

-bin_file
Write a binary bit file without header (.bin)

OK Cancel Apply Restore...

Generate bitstream



EQ_OBUF_inst_i_1

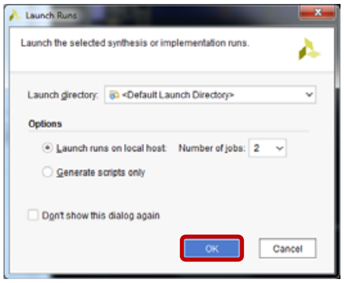
Name: EQ_OBUF_inst_i_1
Reference name: LUT2
Type: LUT
BEL: D6LUT □ Fixed
Site: SLICE_X0Y11

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	NA	Worst Hold Slack (WHS):	NA	Worst Pulse Width Slack (WPWS):	NA
Total Negative Slack (TNS):	NA	Total Hold Slack (THS):	NA	Total Pulse Width Negative Slack (TPWS):	NA
Number of Failing Endpoints:	NA	Number of Failing Endpoints:	NA	Number of Failing Endpoints:	NA
Total Number of Endpoints:	NA	Total Number of Endpoints:	NA	Total Number of Endpoints:	NA

There are no user specified timing constraints.

Generate a programming file after implementation



Launch the selected synthesis or implementation runs.

Launch directory: <Default Launch Directory>

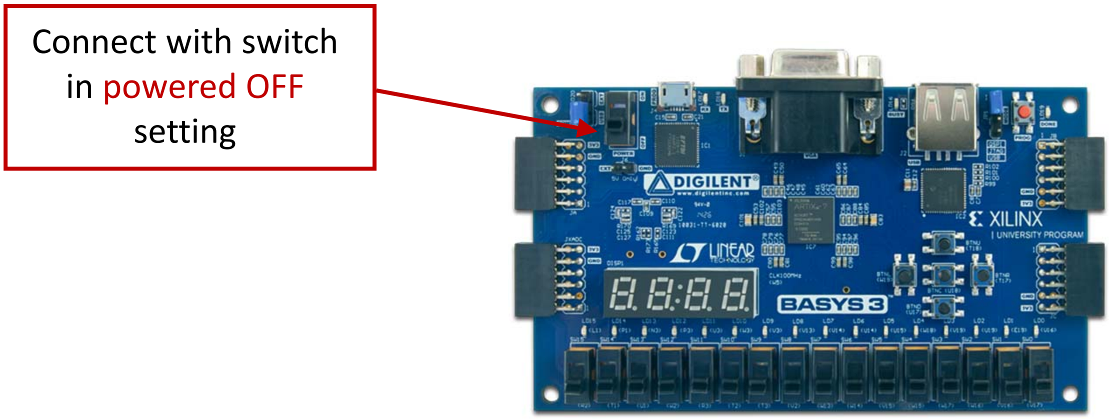
Options

● Launch runs on local host: Number of jobs: 2

○ Generate scripts only

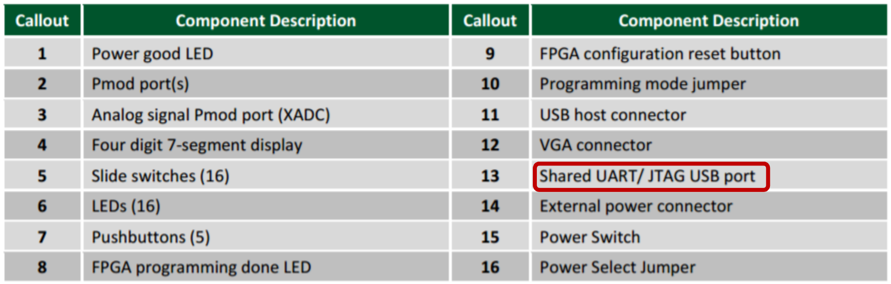
□ Don't show this dialog again

Connect Basys 3 to PC with USB cable



Connect with switch in powered OFF setting

Basys3 board: configure pins



Callout	Component Description	Callout	Component Description
1	Power good LED	9	FPGA configuration reset button
2	Pmod port(s)	10	Programming mode jumper
3	Analog signal Pmod port (XADC)	11	USB host connector
4	Four digit 7-segment display	12	VGA connector
5	Slide switches (16)	13	Shared UART/ JTAG USB port
6	LEDs (16)	14	External power connector
7	Pushbuttons (5)	15	Power Switch
8	FPGA programming done LED	16	Power Select Jumper

Table 1. Basys 3 Callouts and component descriptions.

Basys3 board: Pin configurations

Figure 3 shows the different options available for configuring the FPGA. An on-board "mode" jumper (JP1) selects between the programming modes.

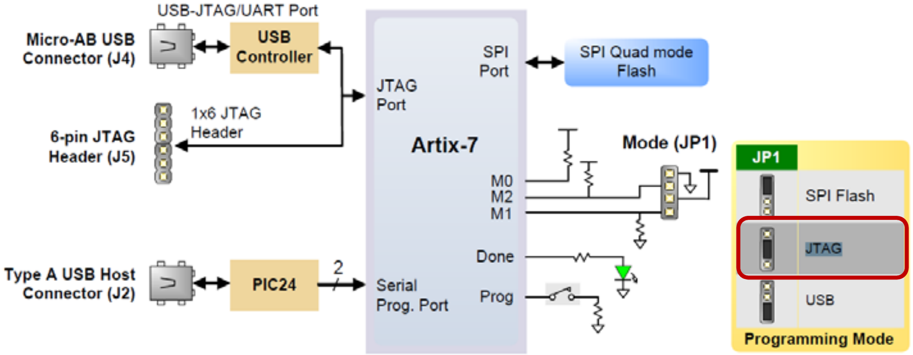


Figure 3. Basys 3 configuration options.

Basys3 board: configure pin 10 and **power on**

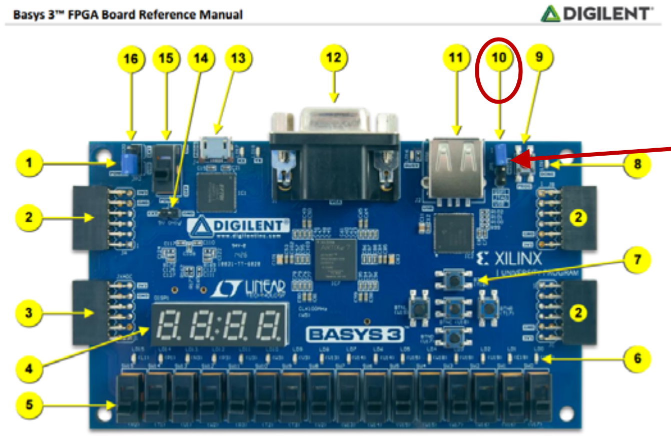
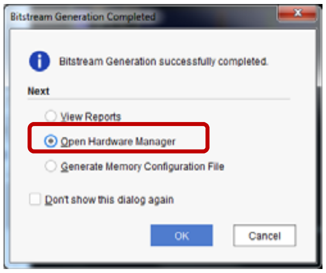


Figure 1. Basys 3 FPGA board with callouts.

To select the JTAG setting, place jumper on middle pair of the four pins.
(Note: QSPI setting is illustrated)

Open hardware manager



Bitstream Generation Completed

Bitstream Generation successfully completed.

Next

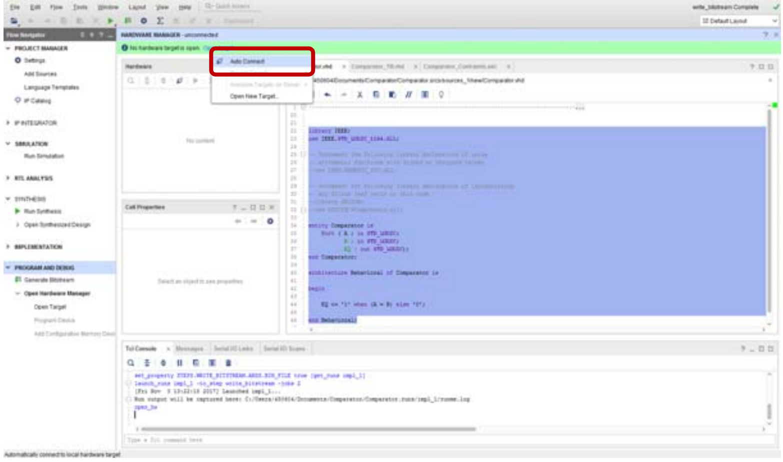
○ View Reports

● Open Hardware Manager

○ Generate Memory Configuration File

□ Don't show this dialog again

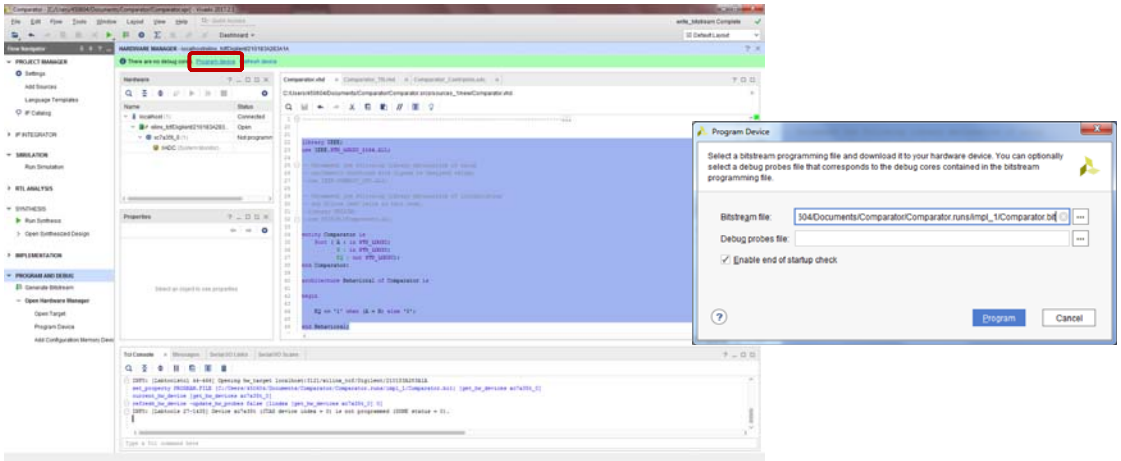
OK Cancel



```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity Comparator is
    Port ( A : in STD_LOGIC;
           B : in STD_LOGIC;
           EQ : out STD_LOGIC);
end Comparator;

architecture Behavioral of Comparator is

begin

    EQ <= '1' when (A = B) else '0';

end Behavioral;
```

```
set_property STEPS.WRITE_BITSTREAM.ARGS.BIN_FILE true [get_runs impl_1]
launch_runs impl_1 -to_step write_bitstream -jobs 2
[Fri Nov  3 13:22:18 2017] Launched impl_1...
Run output will be captured here: C:/Users/450404/Documents/Comparator/Comparator.runs/impl_1/runme.log
open_hw
```

Program device



Program Device

Select a bitstream programming file and download it to your hardware device. You can optionally select a debug probes file that corresponds to the debug cores contained in the bitstream programming file.

Bitstream file: 304/Documents/Comparator/Comparator.runs/impl_1/Comparator.bit

Debug probes file:

☑ Enable end of startup check

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Comparator is
    Port ( A : in STD_LOGIC;
           B : in STD_LOGIC;
           EQ : out STD_LOGIC);
end Comparator;

architecture Behavioral of Comparator is

begin

    EQ <= '1' when (A = B) else '0';

end Behavioral;
```

```
INFO: [Labtoolstcl 44-466] Opening hw_target localhost:3121/xilinx_tcf/Digilent/210183A2E3A1A
set_property PROGRAM.FILE {C:/Users/450804/Documents/Comparator/Comparator.runs/impl_1/Comparator.bit} [get_hw_devices xc7a35t_0]
current_hw_device [get_hw_devices xc7a35t_0]
refresh_hw_device -update_hw_probes false [lindex [get_hw_devices xc7a35t_0] 0]
INFO: [Labtools 27-1435] Device xc7a35t (JTAG device index = 0) is not programmed (DONE status = 0).
```

Does the programme work properly?

Report:

- Apply signals to the board via the switches to confirm that the design works as planned
- Show that the programme worked using photographs of the Basys 3 to show the LEDs and the different switch states.

YouTube - Advice

- Take a look at the following video to get oriented on the work flow.
- https://www.youtube.com/watch?v=JtixlupNSOQ

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