

Sistemas Digitales Laboratorio

Semestre 2020-2
Sesión Laboratorio Semana 9
Profesor: Kalun José Lau Gan

1

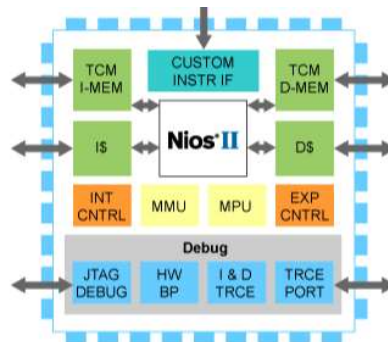
Preguntas previas:

- ¿Alguna consulta antes de empezar?

2

Agenda:

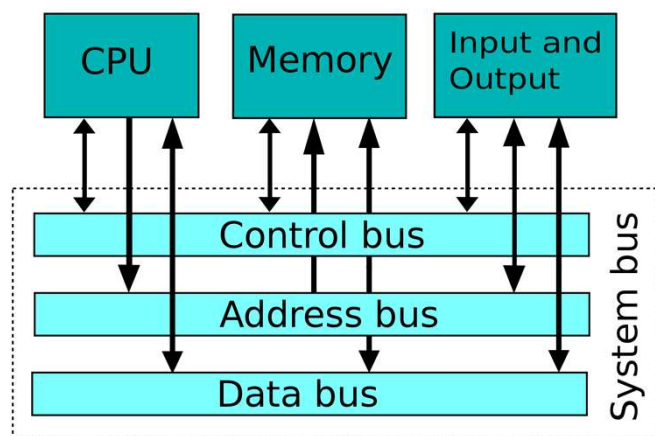
- Esquema general de un computador
- El procesador Intel (ex. Altera) NIOS II
- El Qsys: Implementación de un procesador NIOS II



3

Esquema general de un computador (arquitectura Von Neumann)

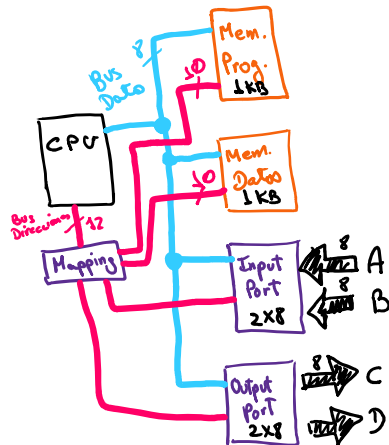
- No pueden faltar ninguno de los componentes.
- Dualidad hardware/software
- Buses interconectan los componentes
- Direcciones únicas tanto en memoria como en E/S



4

Mapecto de direcciones:

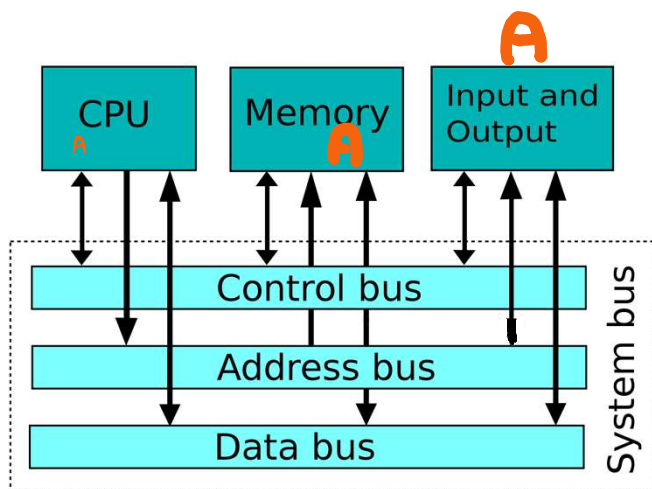
- Los recursos de un computador deben de estar en direcciones únicas, no puede haber conflicto entre los recursos.



		A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	HEX
Mem Instr. (1KB)	Inicio	0	0	0	0	0	0	0	0	0	0	0	0	000H
	Fin	0	0	1	1	1	1	1	1	1	1	1	1	3FFH
Mem Data (1KB)	Inicio	0	1	0	0	0	0	0	0	0	0	0	0	400H
	Fin	0	1	1	1	1	1	1	1	1	1	1	1	4FFH
Input 2x8	Inicio	1	0	0	0	0	0	0	0	0	0	0	0	800H
	Fin	1	0	0	0	0	0	0	0	0	0	0	1	801H
Output 2x8	Inicio	1	1	0	0	0	0	0	0	0	0	0	0	C00H
	Fin	1	1	0	0	0	0	0	0	0	0	0	1	C01H

5

Proceso para grabar un dato "A" del puerto a la memoria:

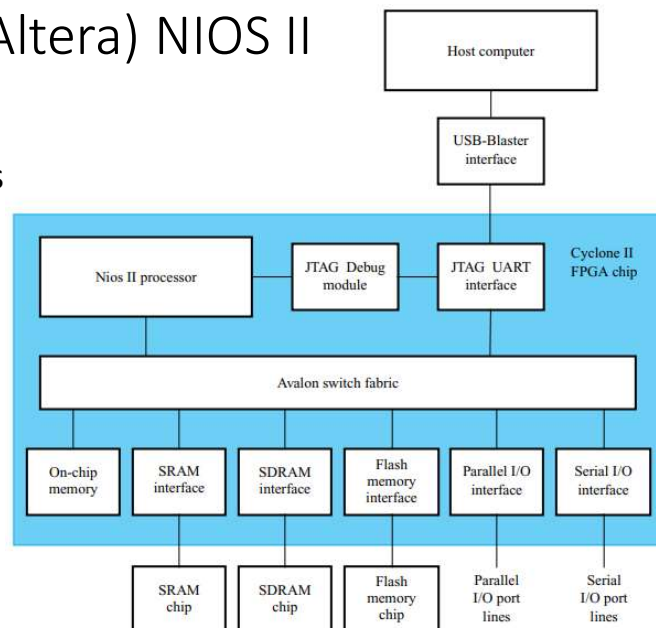


- CPU selecciona el recurso de E/S donde se encuentra "A" (bus de direcciones)
- CPU hace acción de lectura a E/S (bus de control)
- El dato "A" para a un registro temporal del CPU a través del bus de datos
- CPU selecciona el recurso de memoria donde va a alojarse la "A" (bus de direcciones)
- CPU coloca la "A" en el bus de datos
- CPU hace acción de escritura a la memoria (bus de control)

6

El softcore Intel (ex. Altera) NIOS II

- Procesador softcore de 32 bits
- ¿Cuál es la diferencia entre softcore y hardcore?
 - Softcore: Implementado lógicamente (en un FPGA)
 - Hardcore: Implementado físicamente



7

El softcore Intel (ex. Altera) NIOS II

- Documentación:
 - NIOS II Classic Processor Reference Guide (28/10/2016):
https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/hb/nios2/n2cpu_nii5v1.pdf
 - NIOS II Processor Reference Guide (24/04/2020):
<https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/hb/nios2/n2cpu-nii5v1gen2.pdf>
 - My First Nios II Software Tutorial:
http://www.ee.nmt.edu/~erives/554_11/Altera_NIOSII_SW.pdf
 - James O. Hamblen. Rapid Prototyping of Digital Systems SOPC Edition:
<http://dl.icdst.org/pdfs/files3/edddd8fa848a6ff8f0353f0b4be07d11.pdf>

8

Implementando el NIOS II con Qsys:

System Contents Address Map Clock Settings Project Settings Instance Parameters System Inspector HDL Example Generation								
Use	Connections	Name	Description	Export	Clock	Base	End	IRQ
		clk_0	Clock Source	clk	clk_0			
		clk_in	Clock Input	Double-click to export				
		clk_in_reset	Reset Input	Double-click to export				
		clk_reset	Reset Output	Double-click to export				
		nios2_qsys_0	Nios II Processor					
		clk	Clock Input	Double-click to export	clk_0			
		reset_n	Reset Input	Double-click to export	[clk]			
		data_master	Avalon Memory Mapped Master	Double-click to export	[clk]			
		instruction_master	Avalon Memory Mapped Master	Double-click to export	[clk]			
		jtag_debug_module_re...	Reset Output	Double-click to export	[clk]			
		jtag_debug_module	Avalon Memory Mapped Slave	Double-click to export	[clk]	# 0x2800	0x2fff	
		custom_instruction_m...	Custom Instruction Master	Double-click to export				
		onchip_memory2_0	On-Chip Memory (RAM or ROM)					
		clk1	Clock Input	Double-click to export	clk_0			
		s1	Avalon Memory Mapped Slave	Double-click to export	[clk1]	# 0x1000	0x1fff	
		reset1	Reset Input	Double-click to export				
		jtag_uart_0	JTAG UART					
		clk	Clock Input	Double-click to export	clk_0			
		reset	Reset Input	Double-click to export	[clk]			
		avalon_jtag_slave	Avalon Memory Mapped Slave	Double-click to export	[clk]	# 0x0000	0x0007	

9

Implementación del NIOS II con Qsys

System Contents Address Map Clock Settings Project Settings Instance Parameters System Inspector HDL Example Generation								
Use	Connections	Name	Description	Export	Clock	Base	End	IRQ
		clk_0	Clock Source	clk	clk_0			
		clk_in	Clock Input	Double-click to export				
		clk_in_reset	Reset Input	Double-click to export				
		clk_reset	Reset Output	Double-click to export				
		nios2_qsys_0	Nios II Processor					
		clk	Clock Input	Double-click to export	clk_0			
		reset_n	Reset Input	Double-click to export	[clk]			
		data_master	Avalon Memory Mapped Master	Double-click to export	[clk]			
		instruction_master	Avalon Memory Mapped Master	Double-click to export	[clk]			
		jtag_debug_module_re...	Reset Output	Double-click to export	[clk]			
		jtag_debug_module	Avalon Memory Mapped Slave	Double-click to export	[clk]	# 0x2800	0x2fff	
		custom_instruction_m...	Custom Instruction Master	Double-click to export				
		onchip_memory2_0	On-Chip Memory (RAM or ROM)					
		clk1	Clock Input	Double-click to export	clk_0			
		s1	Avalon Memory Mapped Slave	Double-click to export	[clk1]	# 0x1000	0x1fff	
		reset1	Reset Input	Double-click to export				
		jtag_uart_0	JTAG UART					
		clk	Clock Input	Double-click to export	clk_0			
		reset	Reset Input	Double-click to export	[clk]			
		avalon_jtag_slave	Avalon Memory Mapped Slave	Double-click to export	[clk]	# 0x0000	0x0007	
		pio_0	PIO (Parallel IO)					
		clk	Clock Input	Double-click to export	clk_0			
		reset	Reset Input	Double-click to export	[clk]			
		pio_1	PIO (Parallel IO)					
		clk	Clock Input	Double-click to export	clk_0			
		reset	Reset Input	Double-click to export	[clk]			
		external_connection	Conduit					
		clk	Clock Input	Double-click to export	clk_0			
		reset	Reset Input	Double-click to export	[clk]			
		external_connection	Conduit					
		clk	Clock Input	Double-click to export	clk_0			
		reset	Reset Input	Double-click to export	[clk]			

Messages

Description	Path
3 Warnings	
pio_0_external_connection must be exported, or connected to a matching conduit.	System.pio_0
pio_1_external_connection must be exported, or connected to a matching conduit.	System.pio_1
Interrupt sender jtag_uart_0_irq is not connected to an interrupt receiver	System.jtag_uart_0
1 Info Message	
0 Errors, 3 Warnings	

10

Cuestionario

11

Fin de la sesión

12