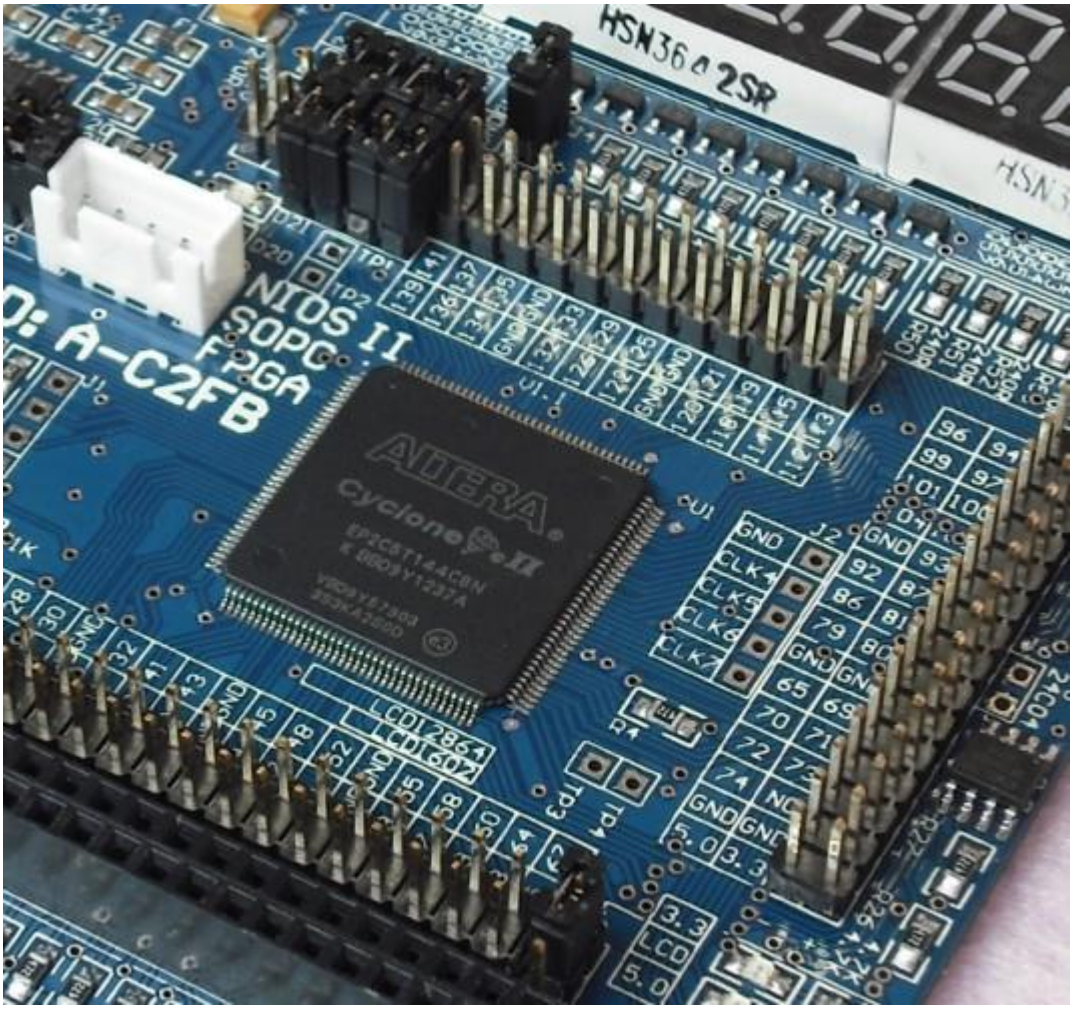
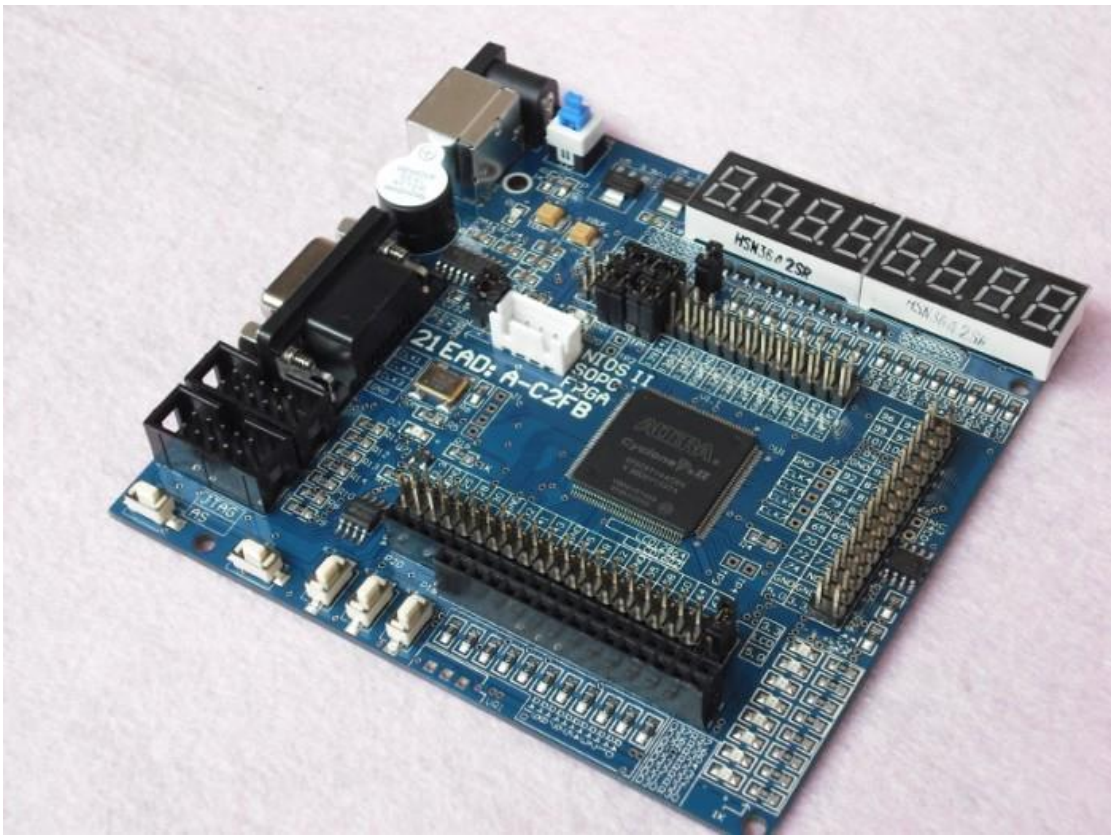
Altera FPGA Development Board User Manual

Model： A-C2FB

CycloneII :EP2C5T144C8




EAD: A-C2FB
JTAG
AS


21EAD: A-C2FB
NIOS II
SOPC
FPGA
JTAG
AS

Contents

1: The introduction of development board

This development board using Altera Cyclone II EP2C5T144C8. To help customers reduce learning cost. The user quick access to the design and development of field programmable logic device. Provides a user quickly learn the programmable logic device hardware platform.

The FPGA platform provides rich hardware resources and a large number of experimental routines. Development board using JTAG interface programming on the chip, JTAG download, power-down missing. You can use the AS interface to download. AS is used for curing power-down without loss of program. Distribution of ByteBlasterII download cable can all FPGA /CPLD chip of Altera company, download.

Development board all I/O are brought forth by needles, plates.. Convenient for users to develop their own products. The maximum for users to save development cost.

2: Development board hardware introduction

1 ）CycloneII U1 EP2C5T144C8

2 ）I2C U3 AT24C04

3 ）AS U2 EPCS4

4 ）UART U4 MAX232

5 ）PS/2 A

6 ）8 digital tube display

7 ）8 LED

8 ）BELL

9 ）LCD12864 / LCD1602 interface

10）4 KEYS

11）ONE FPGA RE-CONFIG KEY

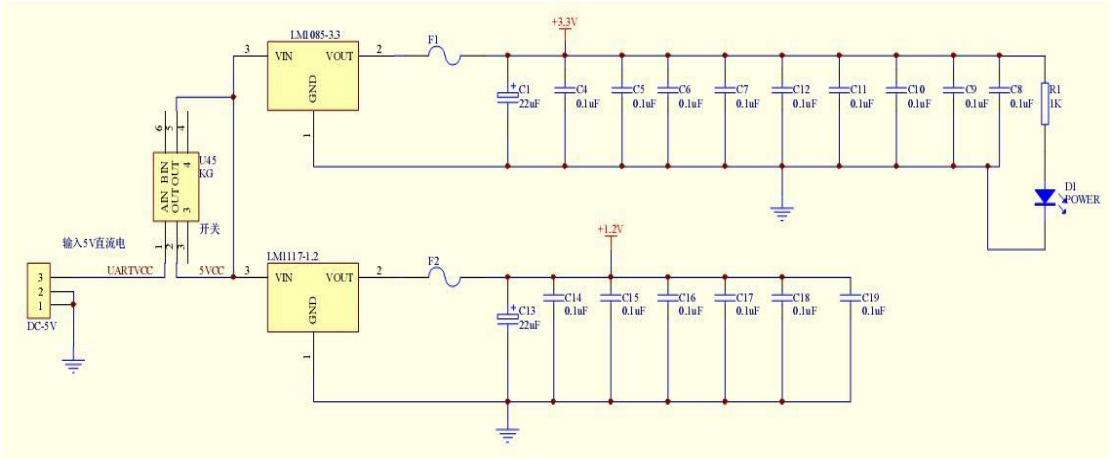
12）JTAG , AS Download mode

13）5V DC POWER INPUT

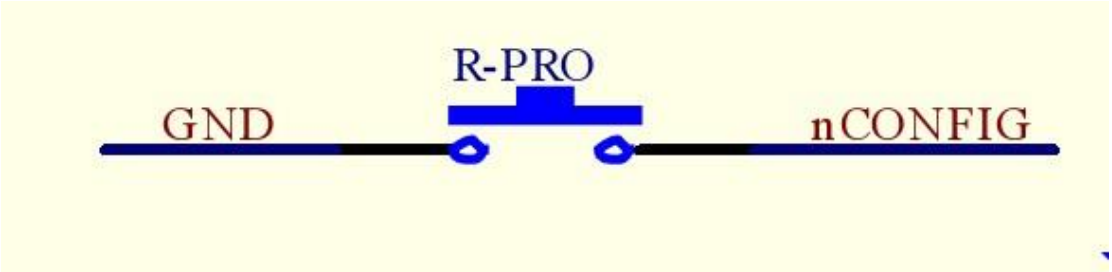
14）50M HZ CLK INPUT

3: Hardware circuit description

1: POWER, DC 5V INPUT.

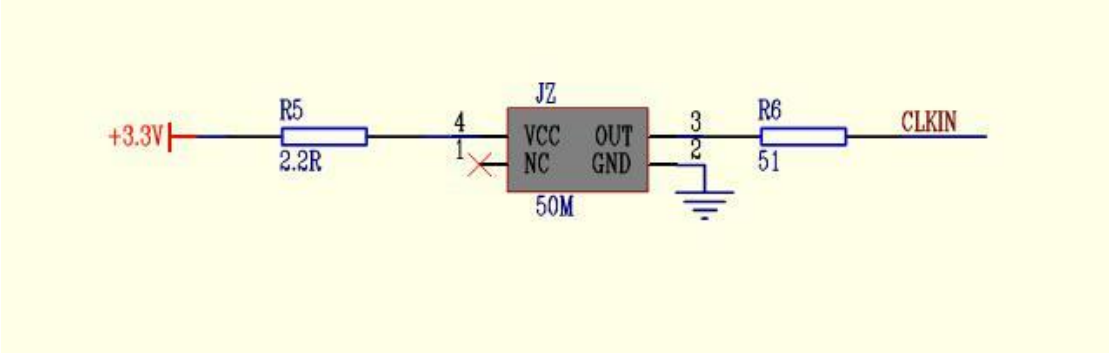


2 FPGA Re-config key



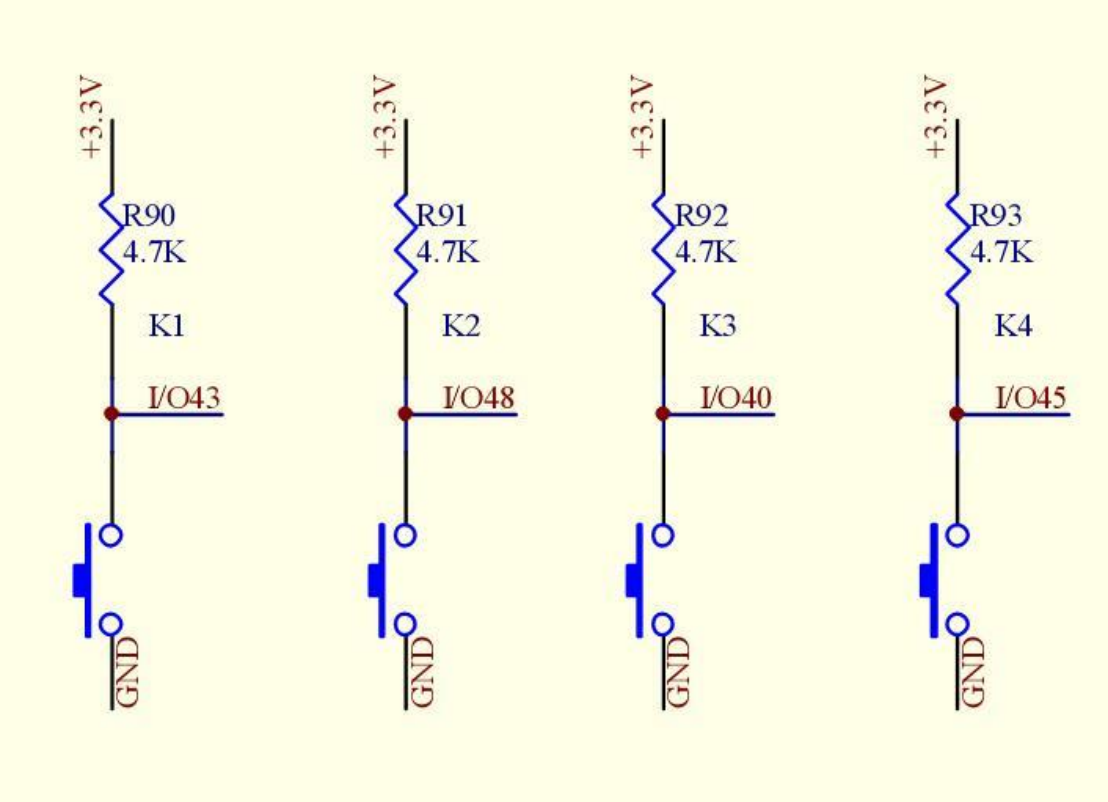
FPGA reconfiguration function keys, when you press this button. FPGA will return to the serial configuration chip to configure FPGA, the board of D2 exhibit of lanterns lit. Configuration data, D2 lights. Successful configuration.

3 Clock input



The active crystal, frequency of 50M Hz to FPGA P17 provides clock.

4 Four independent keys



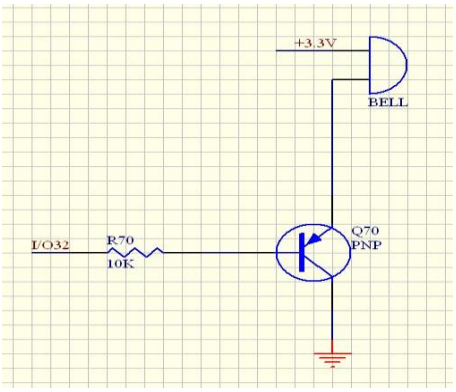
I/O distribution independent key:

KEY1: PIN 43 KEY2: PIN 48

KEY3: PIN 40 KEY4: PIN 45

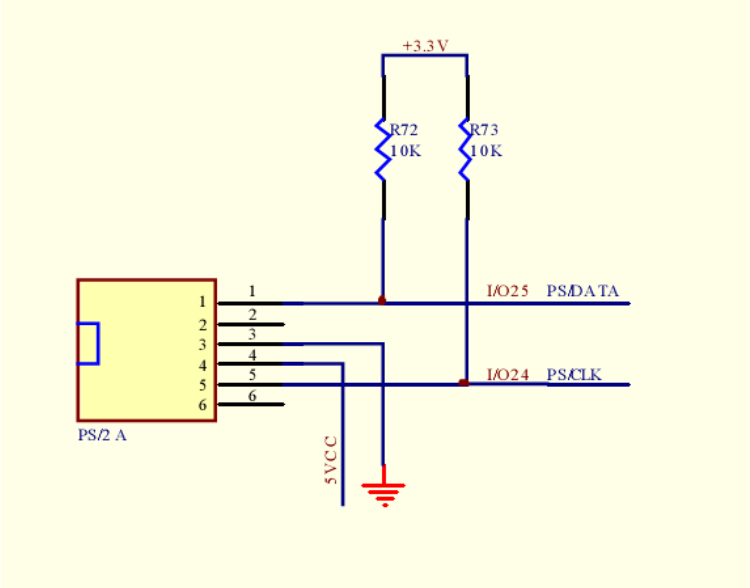
When you press KEY, the IO is a low level.

5 BELL



Buzzer (BELL), when PIN is 32 to 0, BELL beep sound.

6 PS/2 接口

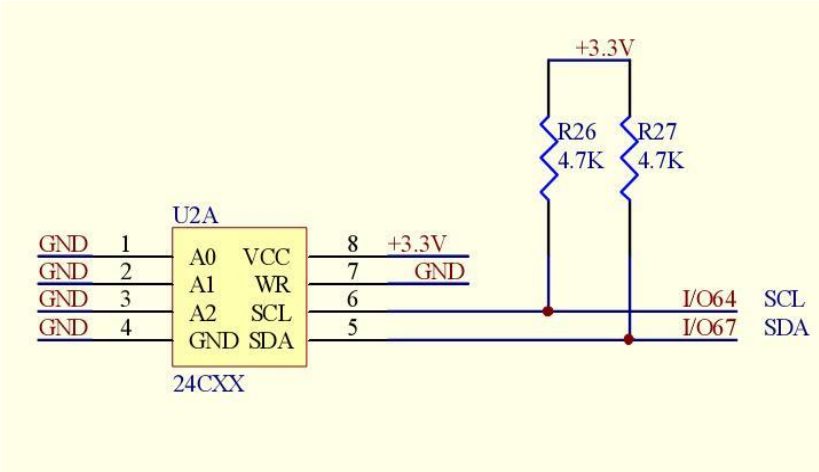


PS/2 A

PS/DATA: PIN 25

PS/CLK : PIN 24

7 I2C AT24C04

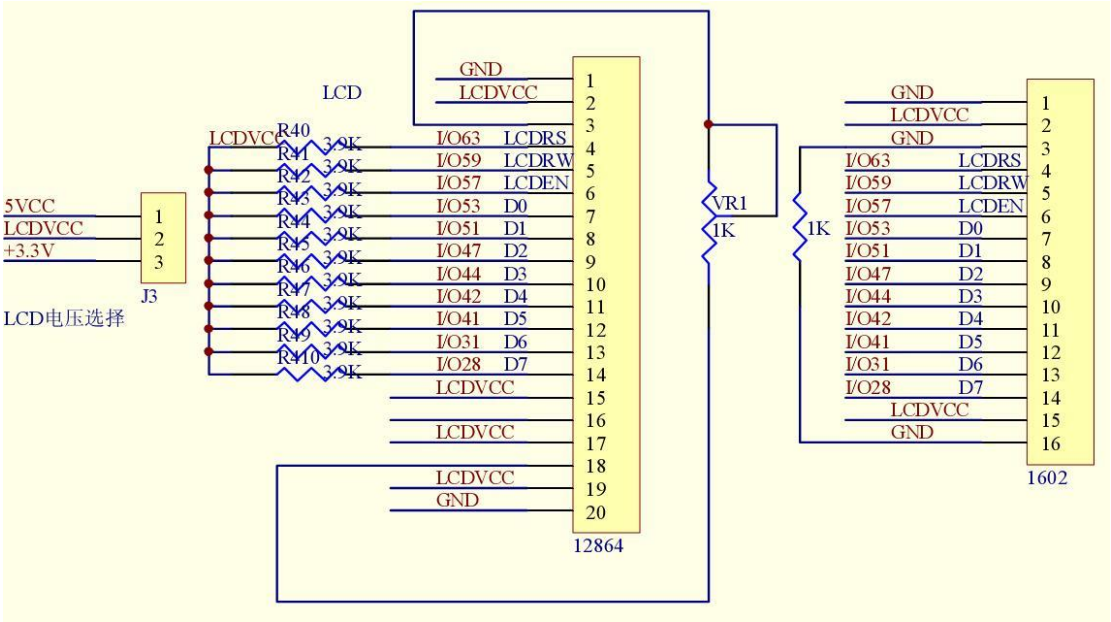


AT24C04 EEPROM：

SCL: PIN64

SDA: PIN67

8 LCD interface



LCD12864/LCD1602 standard interface (LCD with font):

LCD工作电压选择(J3)3.3V或者5.0V。

The working voltage of LCD selection (J3) 3.3V or 5.0V.

LCD control I/O

LCD RS：PIN63

LCD WR：PIN59

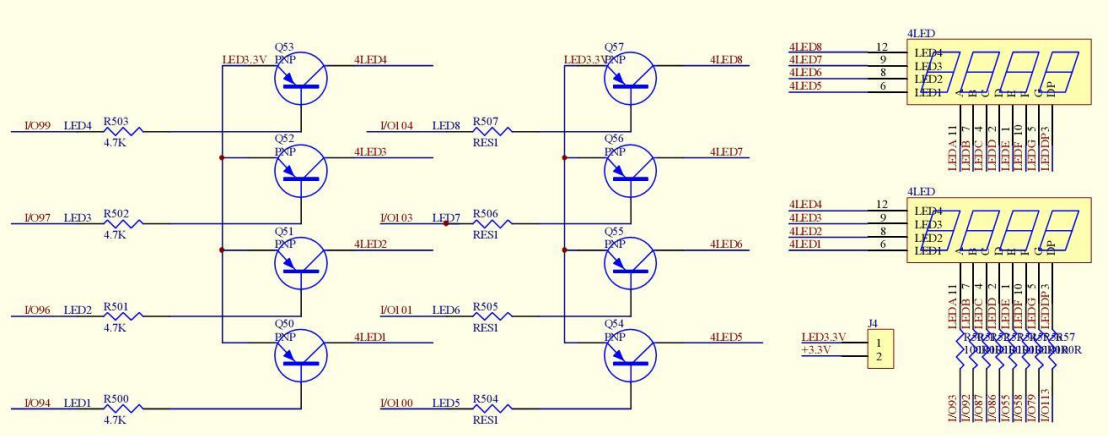
LCD EN：PIN57

LCD 8BIT DATA IO

D0：PIN53 D1：PIN51 D2：PIN47 D3：PIN44

D4：PIN42 D5：PIN41 D6：PIN31 D7：PIN28

9 8 digital tube display



8 digital tube display ， Driven by the PNP triode.

I/O:

LED1:PIN94 。the right one

LED2:PIN96

LED3:PIN97

LED4:PIN99

LED5:PIN100

LED6:PIN101

LED7:PIN103

LED8:PIN104 。The left one,

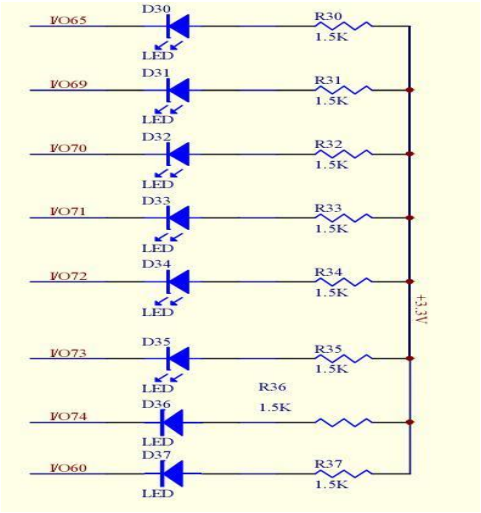
A-》H，8 segment code

LEDA : PIN93 LEDB : PIN92 LEDC : PIN87

LEDD : PIN86 LEDE : PIN55 LEDF : PIN58

LEDG : PIN79 LEDH : PIN113

10 8 leds



I/O pin:

D30 : PIN65

D31 : PIN69

D32 : PIN70

D33 : PIN71

D34 : PIN72

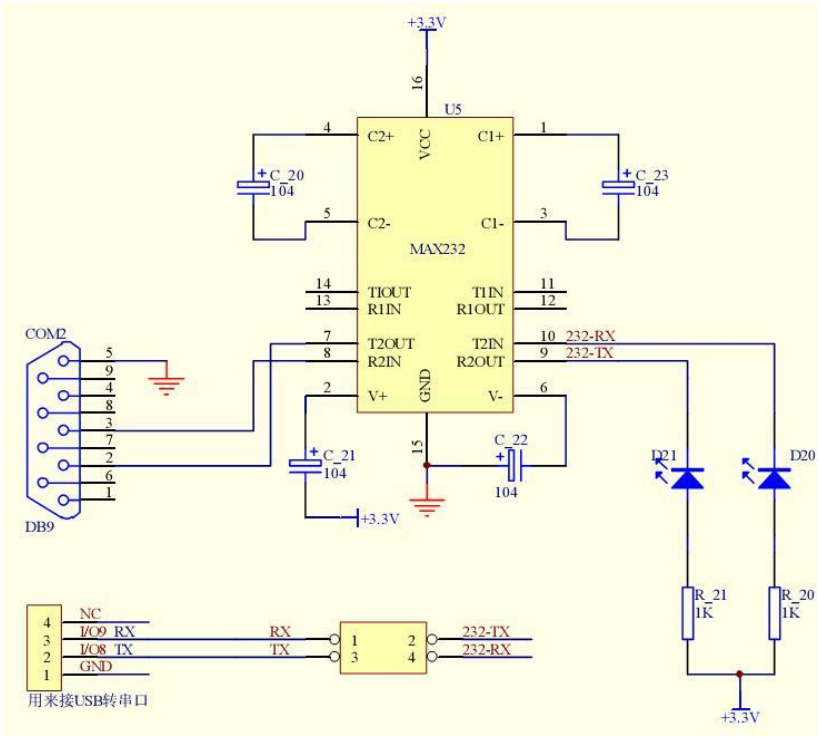
D35 : PIN73

D36 : PIN74

D37 : PIN60

When I/O is low, LED light.

11 UART

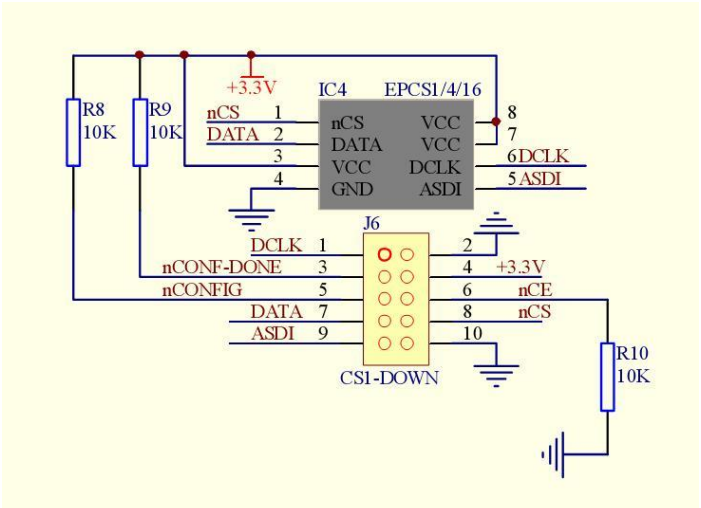


UART：

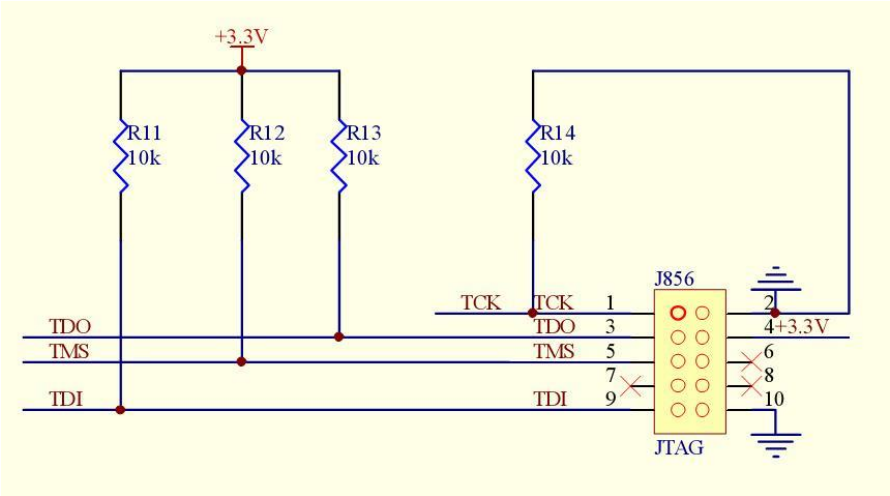
TX : PIN 8

RX : PIN 9

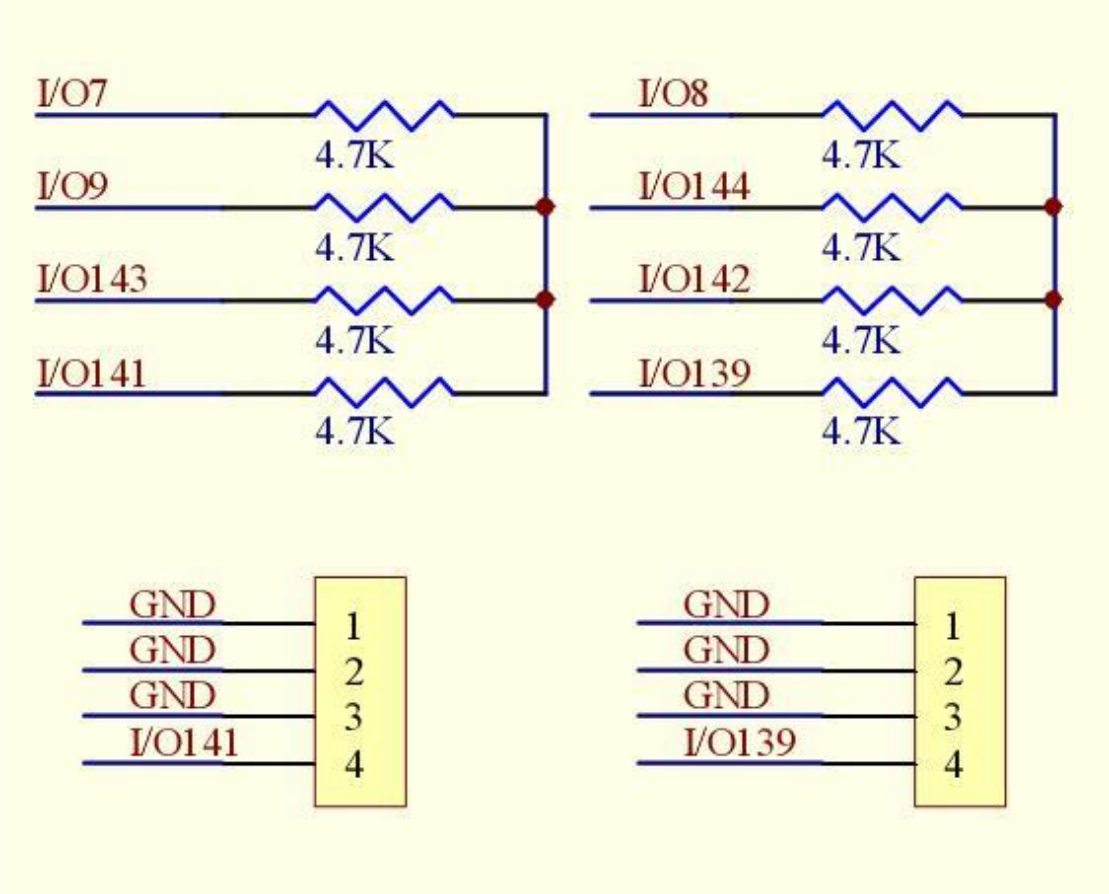
12:AS



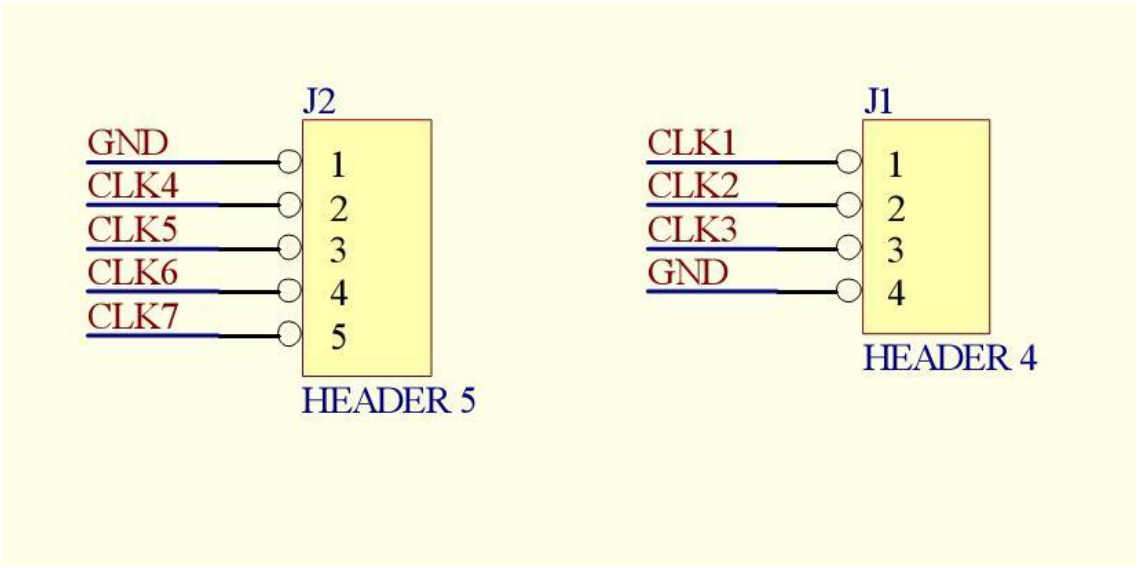
13 JTAG



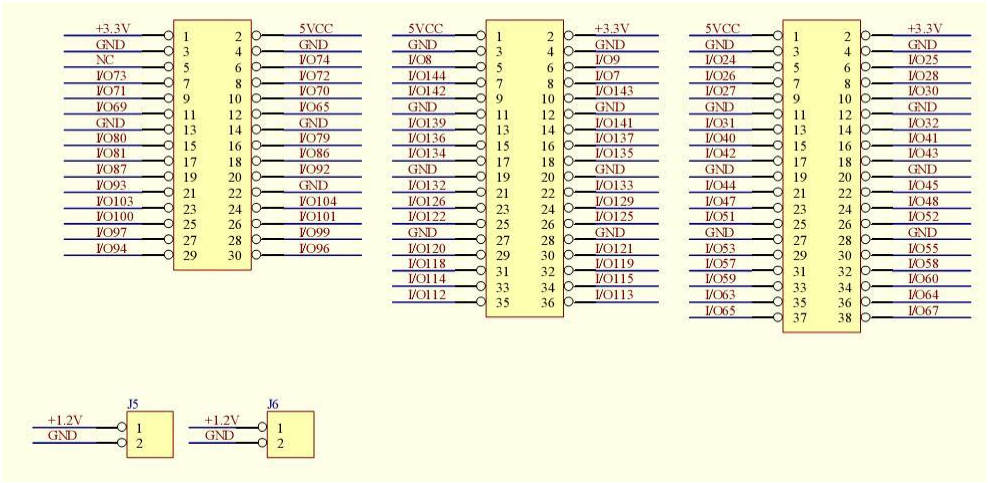
14 The 8 IO, you can set up 1 or 0

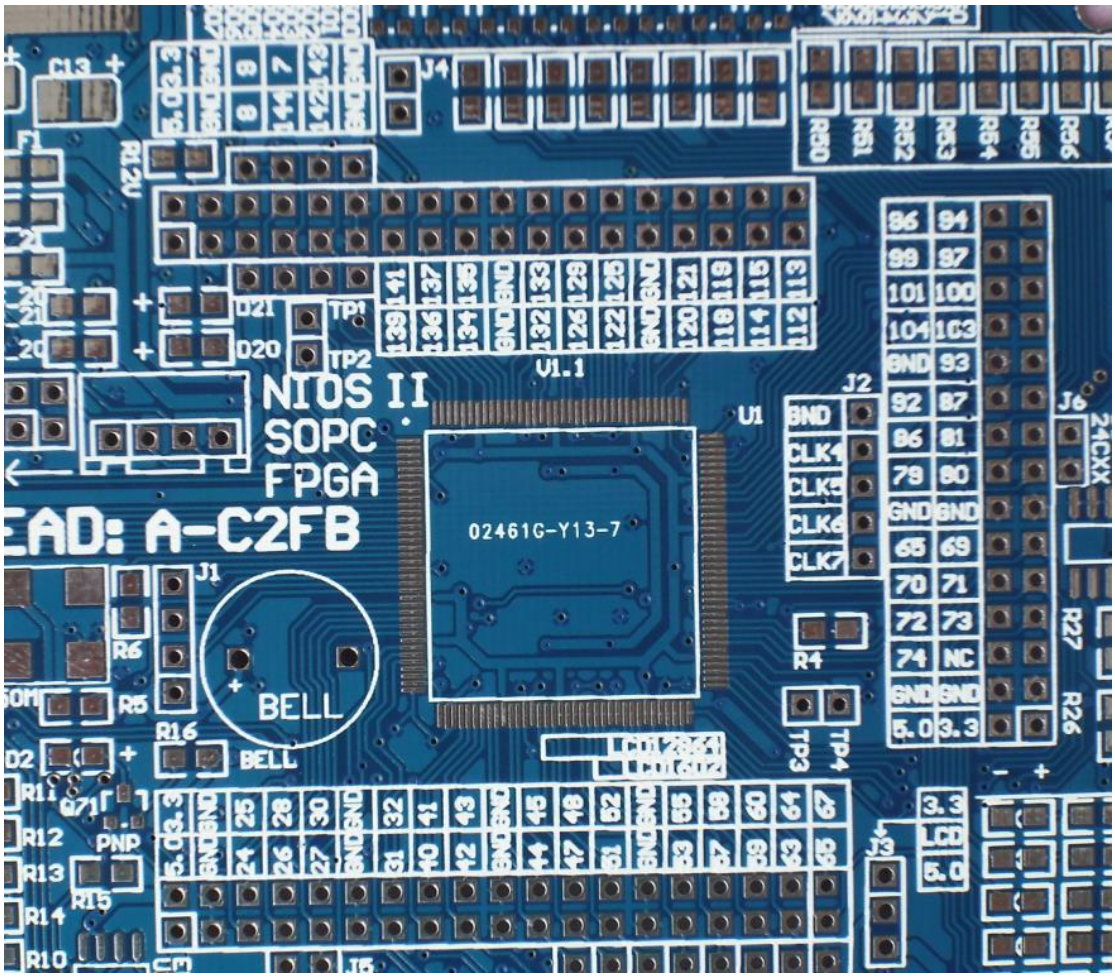


15 The global clock input



16 Users of other I/O available, see the specific sign board.




NIOS II
SOPC
FPGA
EAD: A-C2FB
02461G-Y13-7
V1.1
U1
J1
J2
J3
J4
J6
BELL
BELL
PNP
24CXX
TP1
TP2
TP3
TP4
D20
D21
R4
R5
R6
R12
R13
R14
R15
R16
R26
R27
Q71
C13
GND
CLK4
CLK5
CLK6
CLK7
NC
3.3
5.0