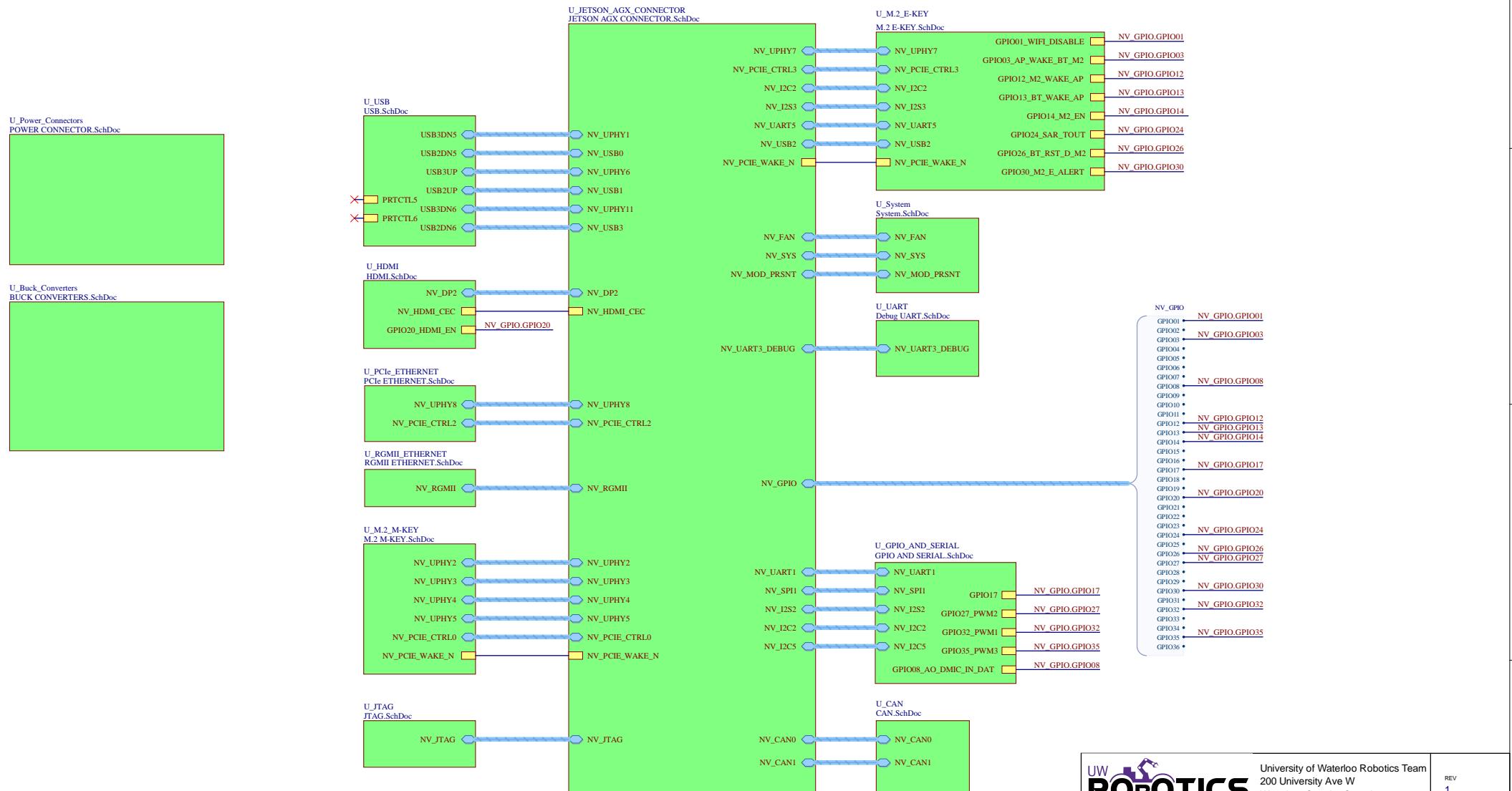


Block Diagram



| | | |
|---|---------------------------|------------------------|
| University of Waterloo Robotics Team 200 University Ave W Waterloo, Ontario, Canada N2L 3G1 | | REV 1 |
| PROJECT Jetson AGX Xavier Carrier Board.PrjPcb, [No Variations] | | |
| DOCUMENT BLOCK DIAGRAM.SchDoc | | MODIFIED 2021-08-24 |
| ENGINEER Cindy Li, Chealsie Bains | REVIEWER Lance Bantoto | SHEET 1 OF 23 |

Power Connector

A

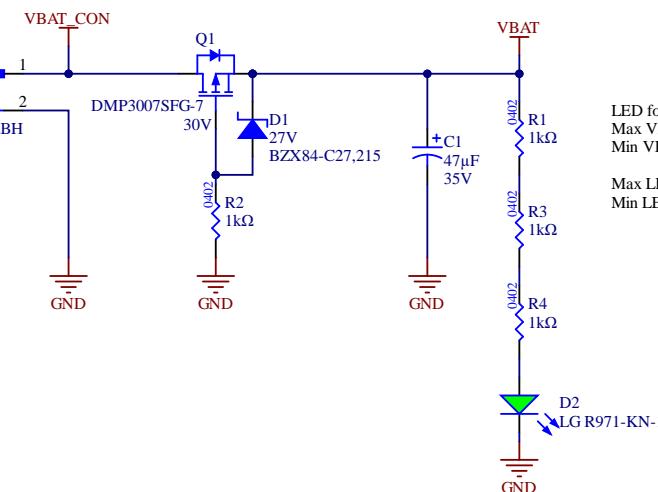
A

Power Jack

Input voltage range: 9V - 20V
 Max current draw at 20V input: 9.5A
 Max current draw at 17V input: 10.2A
 Max current draw at 9V input: 14.5A

[△] TODO: Power Jack rated for 10A, may need to spec a new one

Reverse Polarity Protection



LED forward drop = 2.2V
 Max VBAT = 20V
 Min VBAT = 9V

Max LED current = $(20-2.2)/3000 = 6\text{mA}$
 Min LED current = $(9-2.2)/3000 = 2.3\text{mA}$

B

B



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PROJECT
 Jetson AGX Xavier Carrier Board.PrjPcb, [No Variations]

DOCUMENT
 POWER CONNECTOR.SchDoc

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 2021-08-24

ENGINEER
 Cindy Li

REVIEWER
 Lance Bantoto

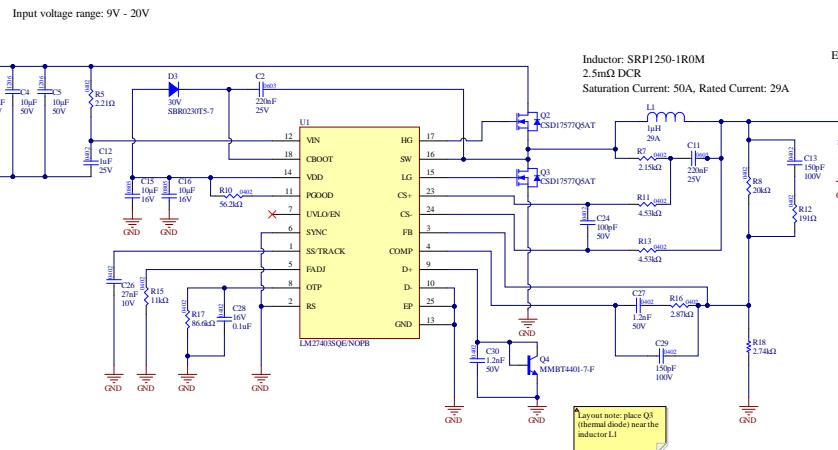
SHEET 2 OF 23

C

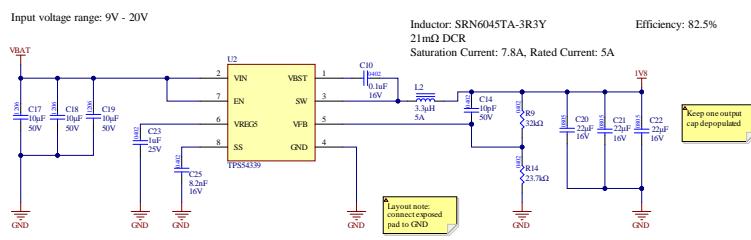
C

Buck Converters

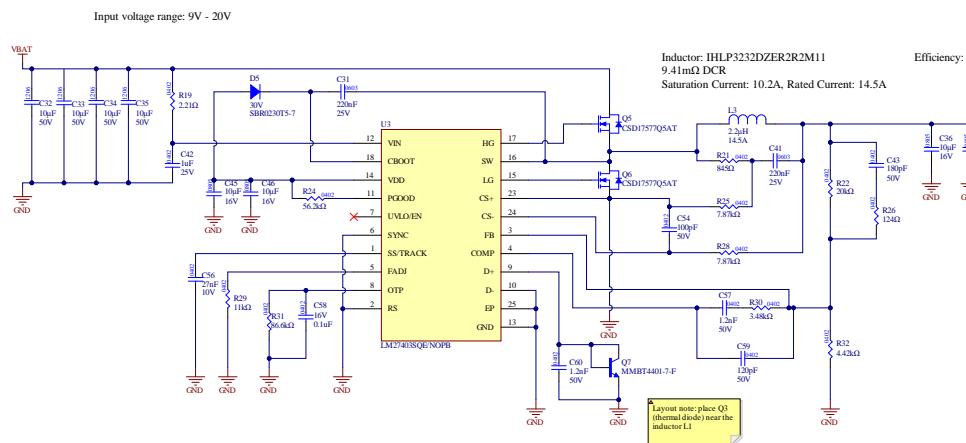
5V Buck Converter @ 16A



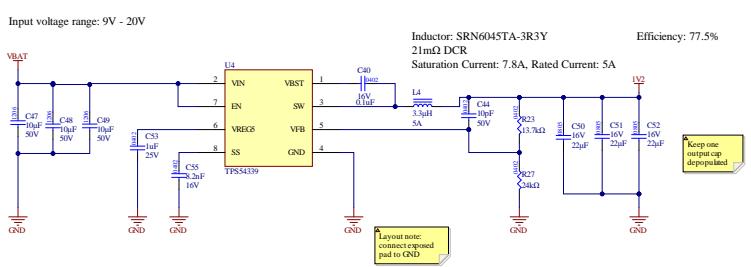
1.8V Buck Converter @ 2A



3.3V Buck Converter @ 6A



1.2V Buck Converter @ 2A



Jetson AGX Connector



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PROJECT
Jetson AGX Xavier Carrier Board.PnjPcb, [No Variations]

DOCUMENT
JETSON AGX CONNECTOR.SchDoc

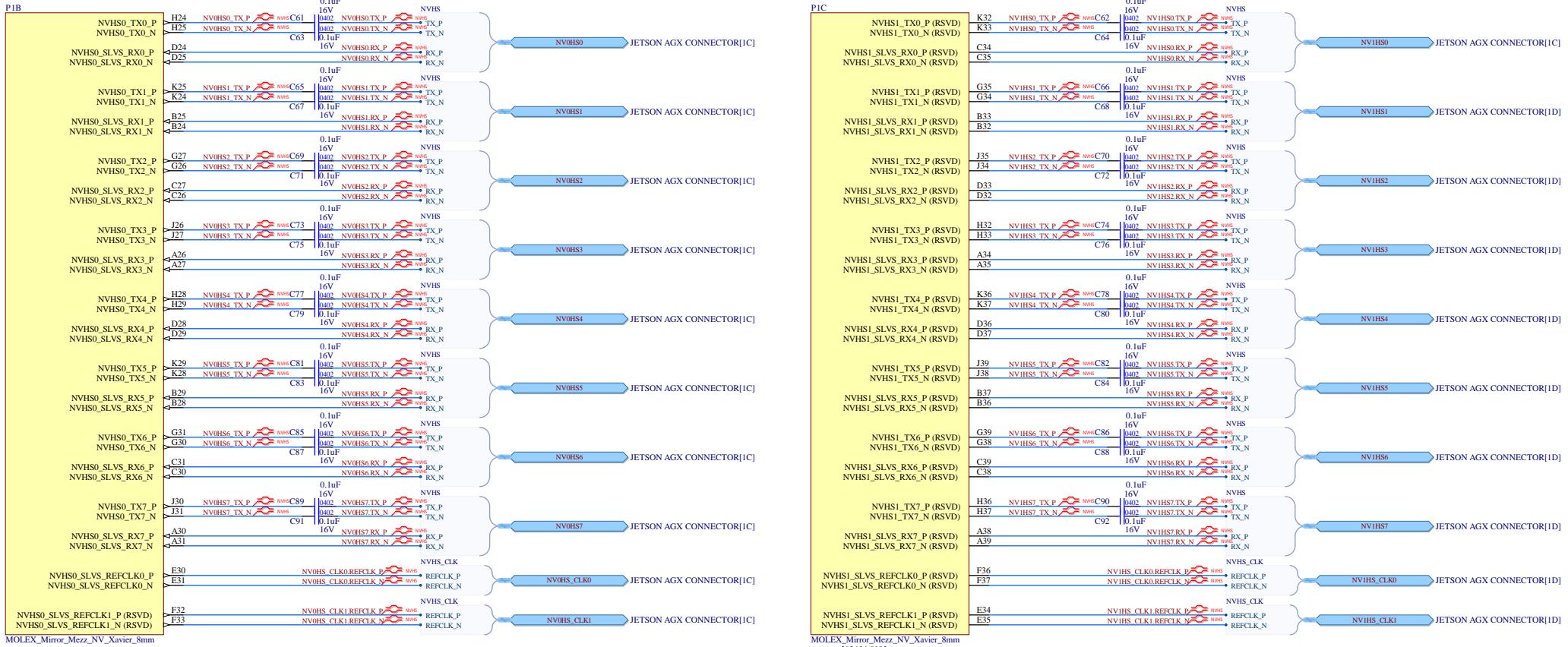
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2021-08-18

ENGINEER
Cindy Li, Chealsie Bains

REVIEWER
Lance Bantoto

SHEET 4 OF 23

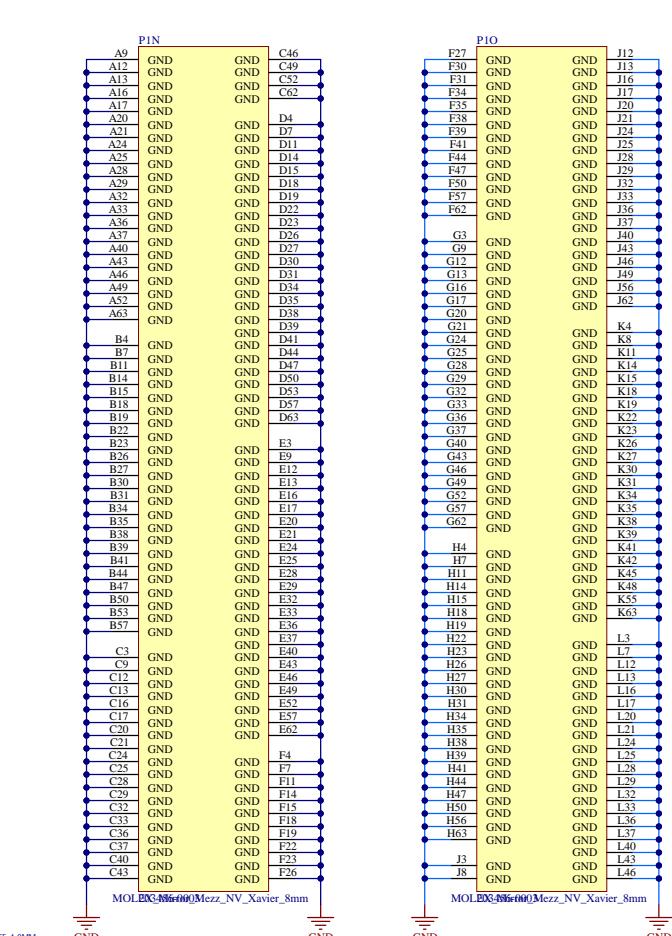
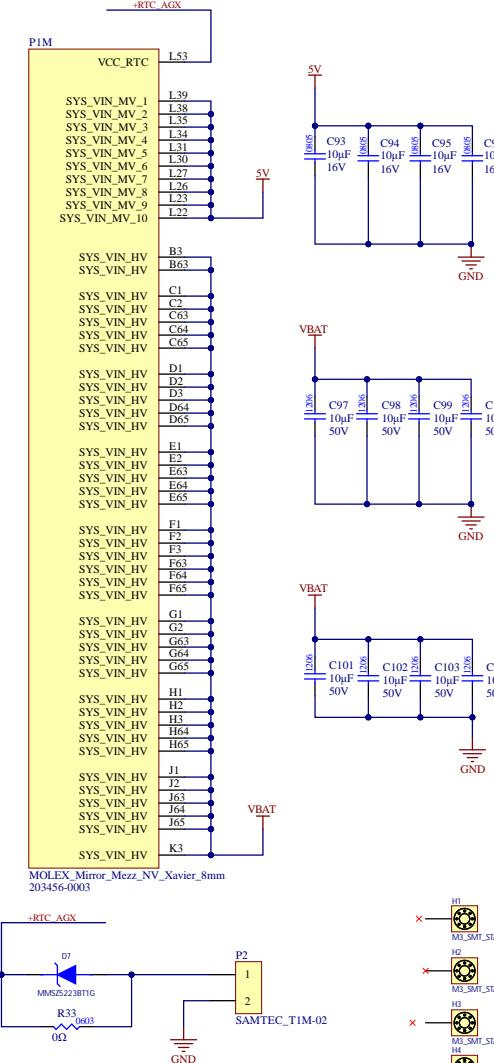
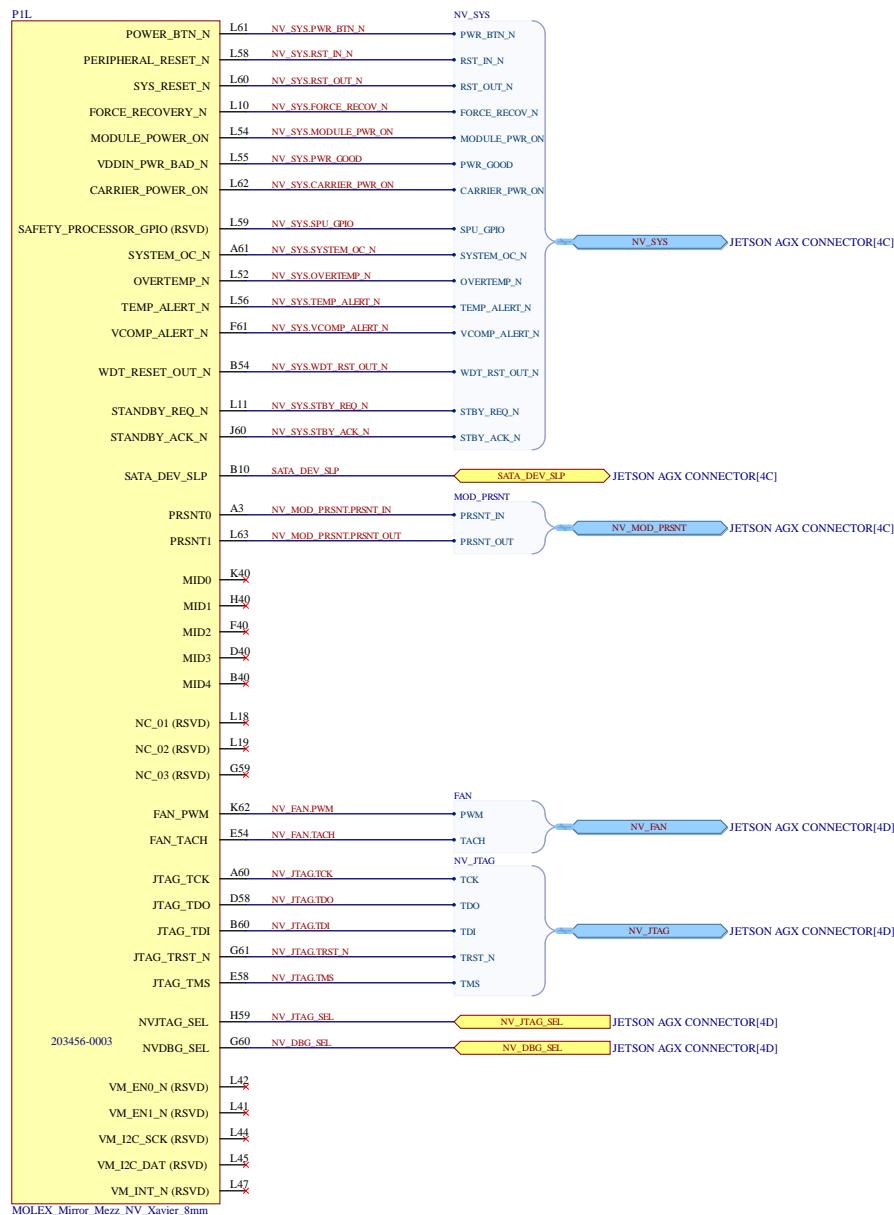
Jetson AGX -NVHS



| | | |
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| PROJECT , [No Variations] | | |
| DOCUMENT | JETSON AGX NVHS.SchDoc | MODIFIED 2021-08-24 |
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Jetson AGX SYS-PWR-GND

A



| | | |
|--|-------------------------------|--|
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| PROJECT | | REV 1 |
| Jetson AGX Xavier Carrier Board.PjPcb, [No Variations] | | |
| DOCUMENT | JETSON AGX SYS-PWR-GND.SchDoc | MODIFIED 2021-08-24 |
| ENGINEER | Cindy Li, Chealsie Bains | REVIEWER Lance Bantoto |
| | | SHEET 6 OF 23 |

Jetson AGX SDIO-SPI-UART-CAN-GPIO



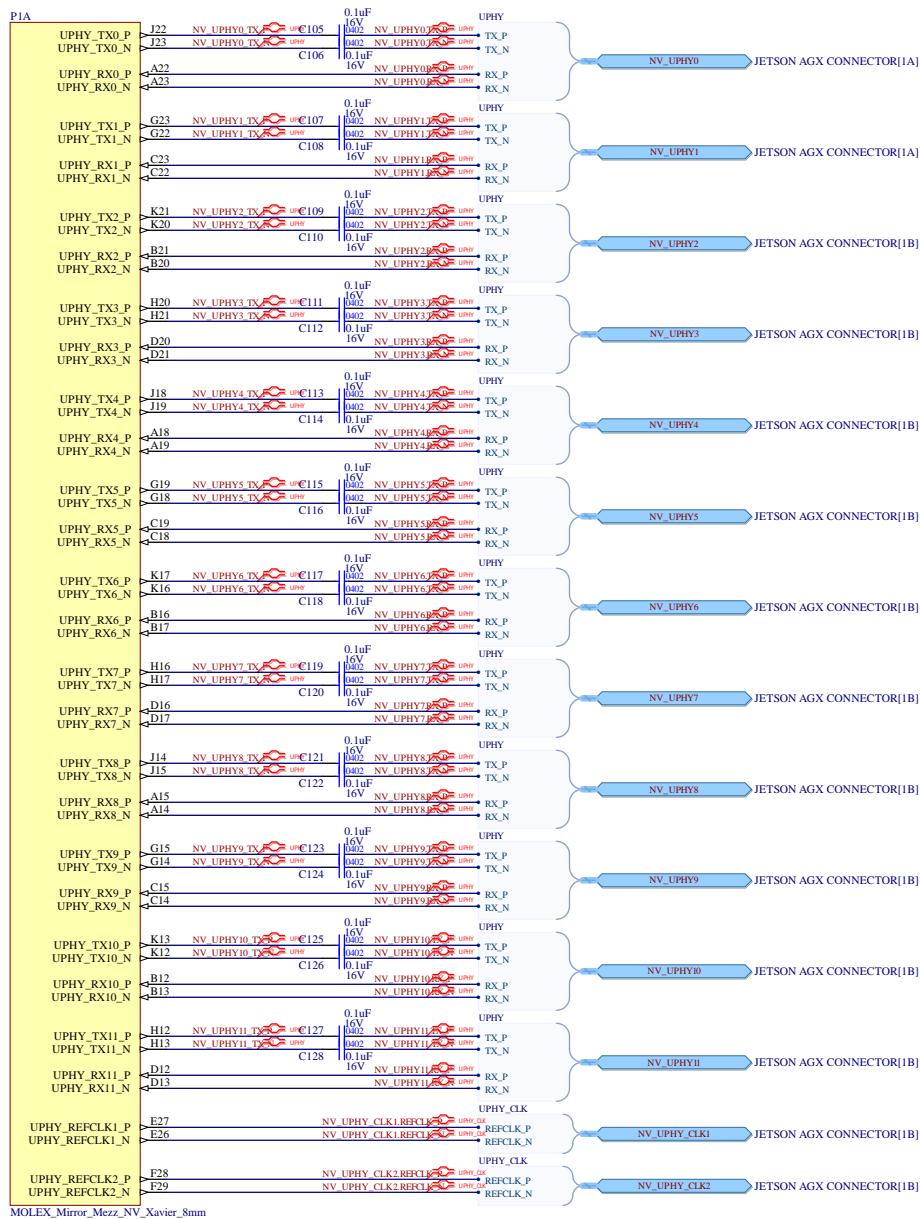
Jetson AGX CSI-I2C-I2S



| NVIDIA Jetson AGX Dev Kit Configuration | | |
|---|--------------------|-------------------|
| CSI | I2C | I2S |
| 0 CAM Expansion | - | - |
| 1 CAM Expansion | ID EEPROM / Debug | - |
| 2 CAM Expansion | PClx16 / M.2-E-Key | 40 Pin Expansion |
| 3 CAM Expansion | CAM Expansion | M.2 E-Key WiFi/BT |
| 4 CAM Expansion | M.2 M.2KEY NVMe | - |
| 5 CAM Expansion | 40 Pin Expansion | - |
| 6 CAM Expansion | - | - |
| 7 CAM Expansion | - | - |

| NVIDIA Jetson AGX Design Configuration | | |
|--|-----|-------------------|
| CSI | I2C | I2S |
| 0 - | - | - |
| 1 - | - | - |
| 2 - | - | M.2 E-Key + GPIO |
| 3 - | - | GPIO |
| 4 - | - | M.2 E-Key WiFi/BT |
| 5 - | - | M.2 M.2KEY NVMe |
| 6 - | - | GPIO |
| 7 - | - | - |

Jetson AGX - UPHY



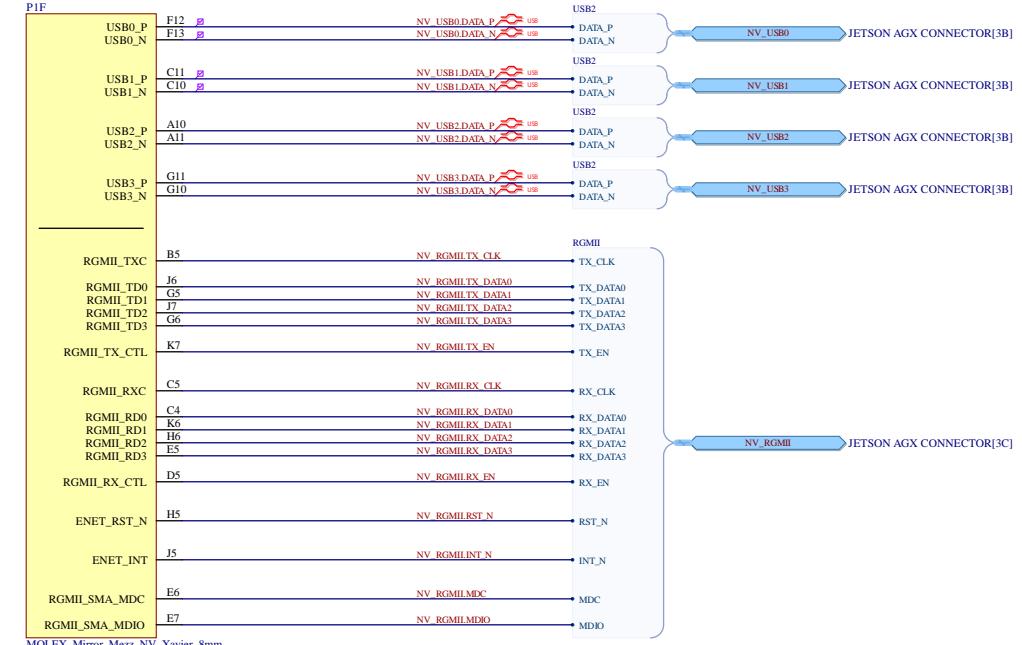
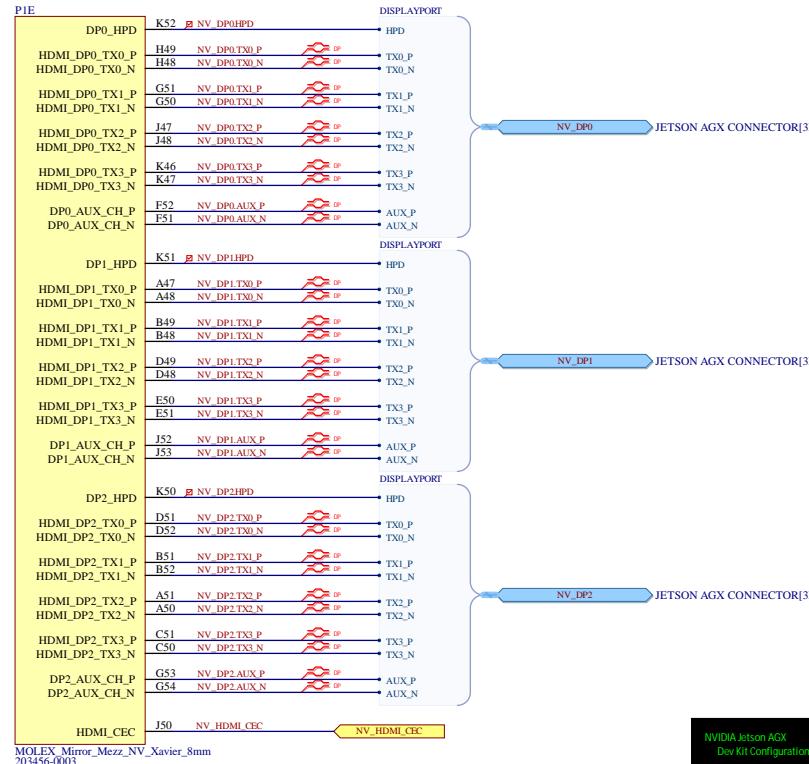
| NVIDIA Jetson AGX Dev Kit Configuration | | | |
|---|----------|-------|-------------------|
| UPHY | NVHS0 | NVHS1 | PCIE_CTRL |
| 0 PCIE/eSATA | PCIe x16 | - | M.2 M-Key NVMe |
| 1 USB Type C | PCIe x16 | - | PCIe/eSATA |
| 2 M.2 M-Key NVMe | PCIe x16 | - | - |
| 3 M.2 M-Key NVMe | PCIe x16 | - | M.2 E-Key WiFi/BT |
| 4 M.2 M-Key NVMe | PCIe x16 | - | - |
| 5 M.2 M-Key NVMe | PCIe x16 | - | PCIe x16 |
| 6 USB Type C | PCIe x16 | - | - |
| 7 M.2 E-Key WiFi/BT | PCIe x16 | - | - |
| 8 - | - | - | - |
| 9 - | - | - | - |
| 10 UFS/MicroSD | - | - | - |
| 11 PCIE/eSATA | - | - | - |

| NVIDIA Jetson AGX Design Configuration | | | |
|--|-------|-------|-----------------------|
| UPHY | NVHS0 | NVHS1 | PCIE_CTRL |
| 0 - | - | - | M.2 M-Key Storage |
| 1 USB 3.0 Type A | - | - | - |
| 2 M.2 M-Key Lane 0 | - | - | PCIe Gigabit Ethernet |
| 3 M.2 M-Key Lane 1 | - | - | M.2 E-Key WiFi/BT |
| 4 M.2 M-Key Lane 2 | - | - | - |
| 5 M.2 M-Key Lane 3 | - | - | - |
| 6 USB 3.0 Type A | - | - | - |
| 7 M.2 E-Key WiFi/BT | - | - | - |
| 8 PCIe Gigabit Ethernet | - | - | - |
| 9 - | - | - | - |
| 10 - | - | - | - |
| 11 USB 3.0 Type A | - | - | - |

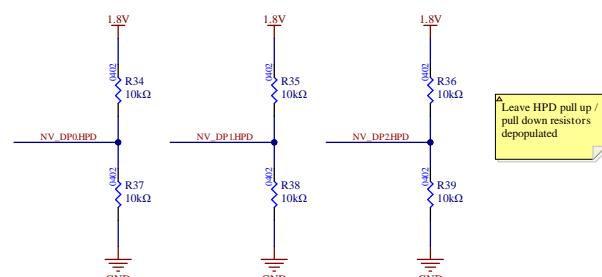
REV 1

| | |
|--|--|
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| PROJECT | |
| Jetson AGX Xavier Carrier Board.Pnjcb, [No Variations] | |
| DOCUMENT | JETSON AGX UPHY.SchDoc |
| ENGINEER | Cindy Li, Chealsie Bains |
| REVIEWER | Lance Bantoto |
| SHEET | 9 OF 23 |

Jetson AGX DP-HDMI-USB-GBE



↔ NVIDIA Jetson AGX Module Headless Operation ↔
The NVIDIA Jetson Module expects to have a Display present. When designing the system for a Headless Operation Mode, the Hot Plug Detect Lines need to be Pulled High, otherwise the Module will report Display Issues Constantly.



↔ NVIDIA Jetson AGX Module DisplayPort / HDMI Routing ↔
The NVIDIA Jetson AGX Module requires 100nF Capacitors to be placed on the DisplayPort TXD and HDMI TXD Lines. These are taken care of on the DisplayPort/HDMI Sheets and should not be duplicated here.

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PROJECT: Jetson AGX Xavier Carrier Board.PnjPcb, [No Variations]

DOCUMENT: JETSON AGX DP-HDMI-USB-GBE.SchDoc

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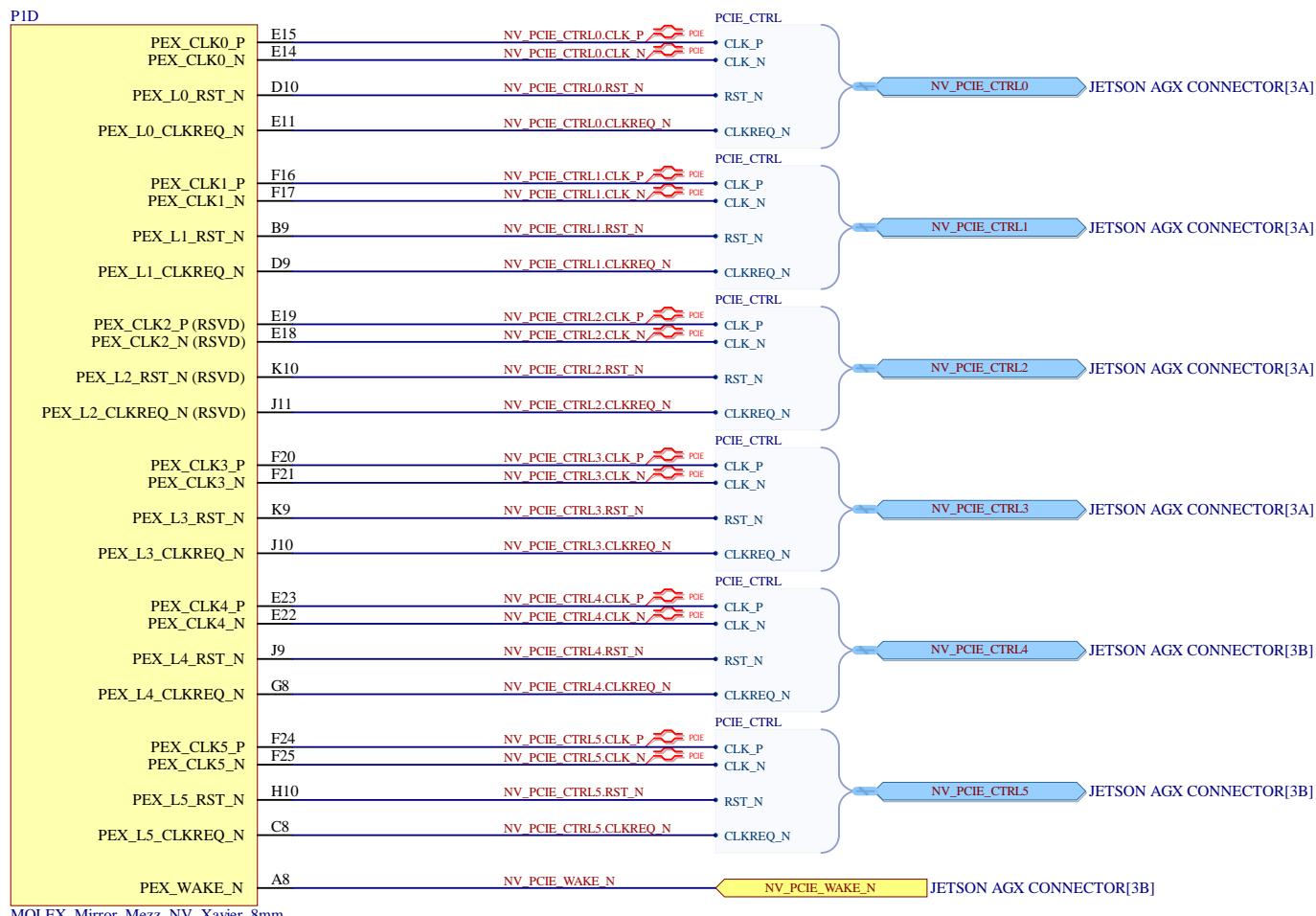
ENGINEER: Cindy Li, Chealsie Bains

REVIEWER: Lance Bantoto

SHEET 10 OF 23

Jetson AGX PCIe

A



A

B

B

C

C

203456-0003



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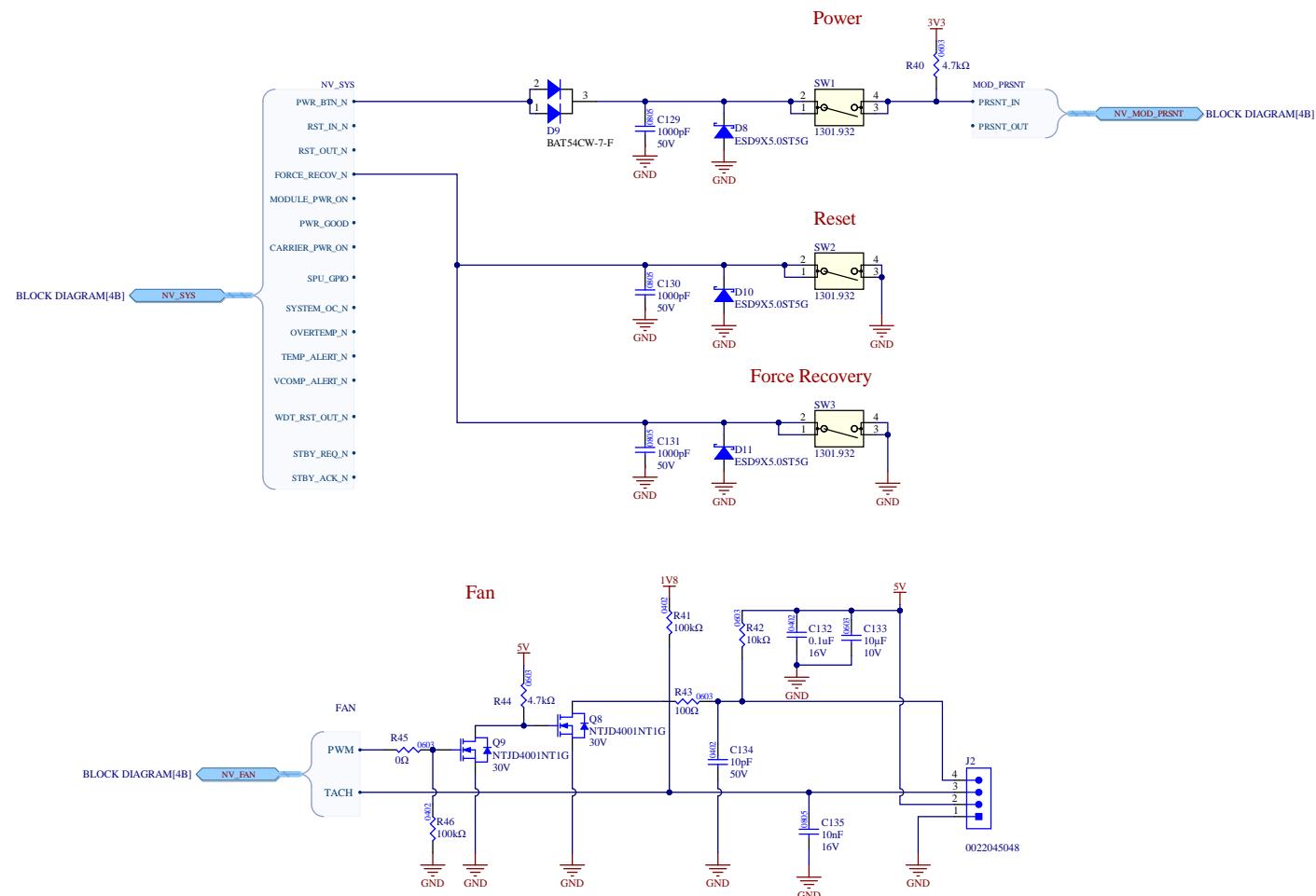
DOCUMENT
JETSON AGX PCIe.SchDoc

ENGINEER
Cindy Li, Chealsie Bains

REVIEWER
Lance Bantoto

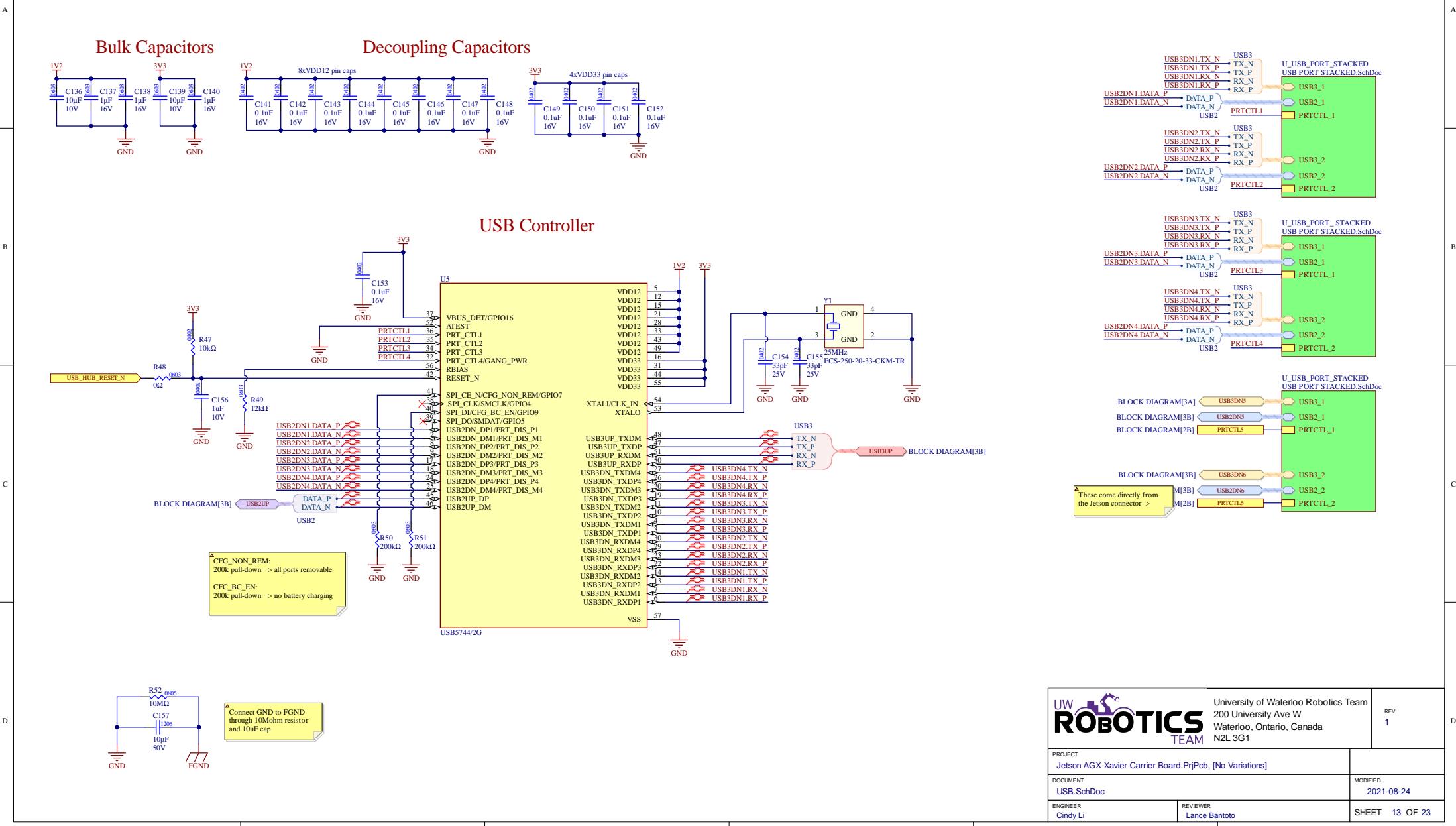
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System



| | | |
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| DOCUMENT System.SchDoc | | MODIFIED 2021-08-24 |
| ENGINEER Chealsie Bains | REVIEWER Lance Bantoto | SHEET 12 OF 23 |

USB

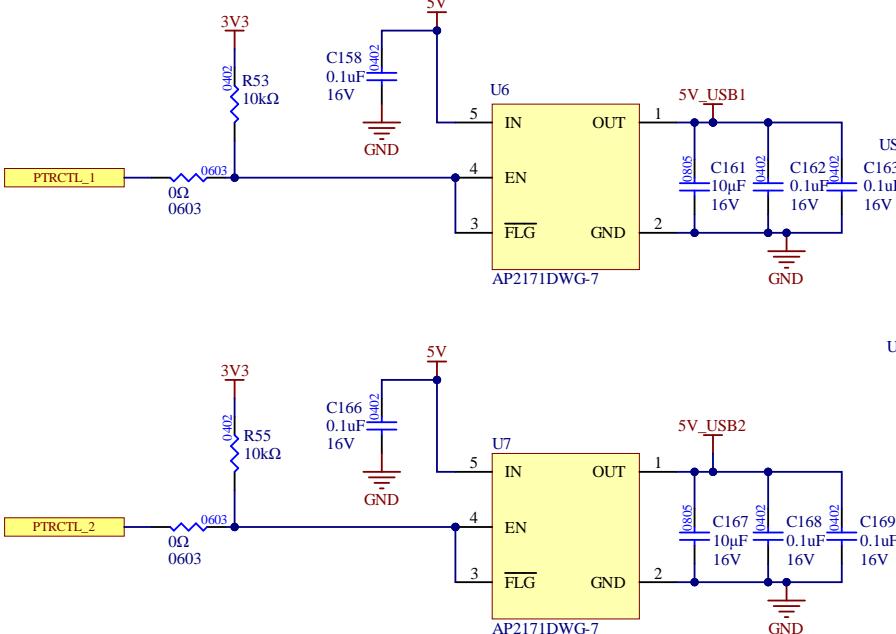


USB Port

A

A

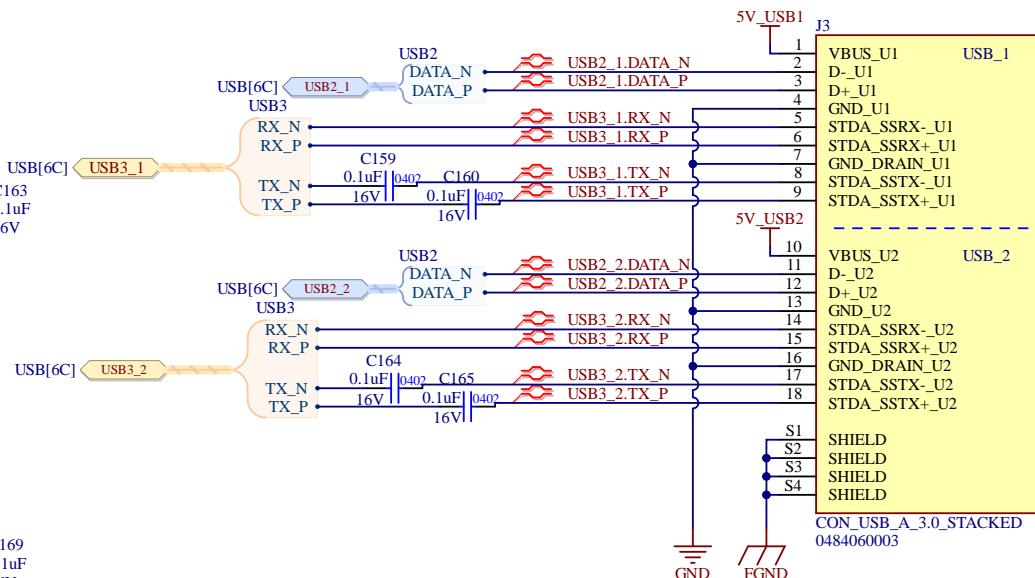
Power Switches



B

B

USB Connector



C

C



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PROJECT

Jetson AGX Xavier Carrier Board.PrjPcb, [No Variations]

DOCUMENT

USB PORT STACKED.SchDoc

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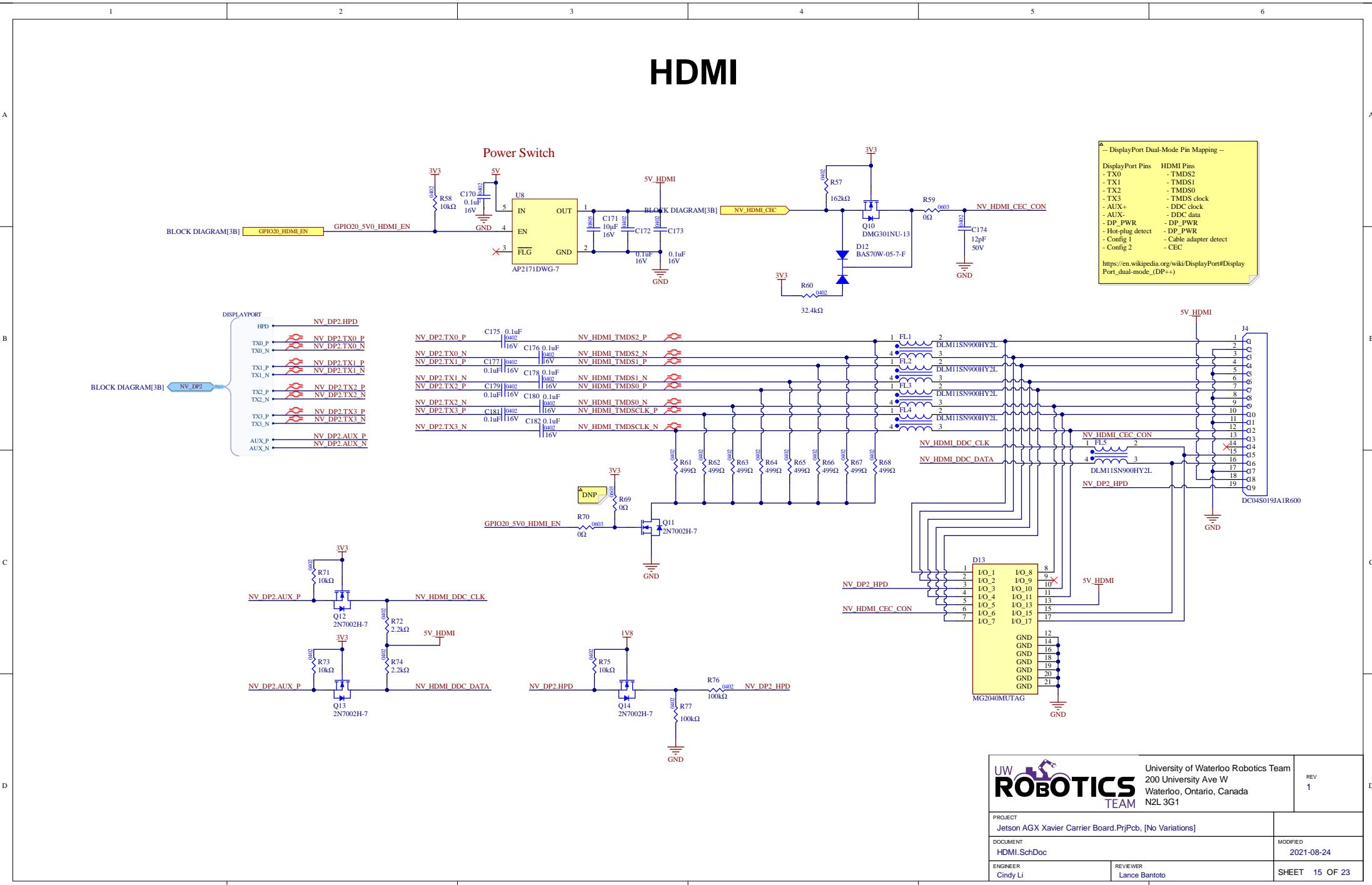
ENGINEER

Cindy Li

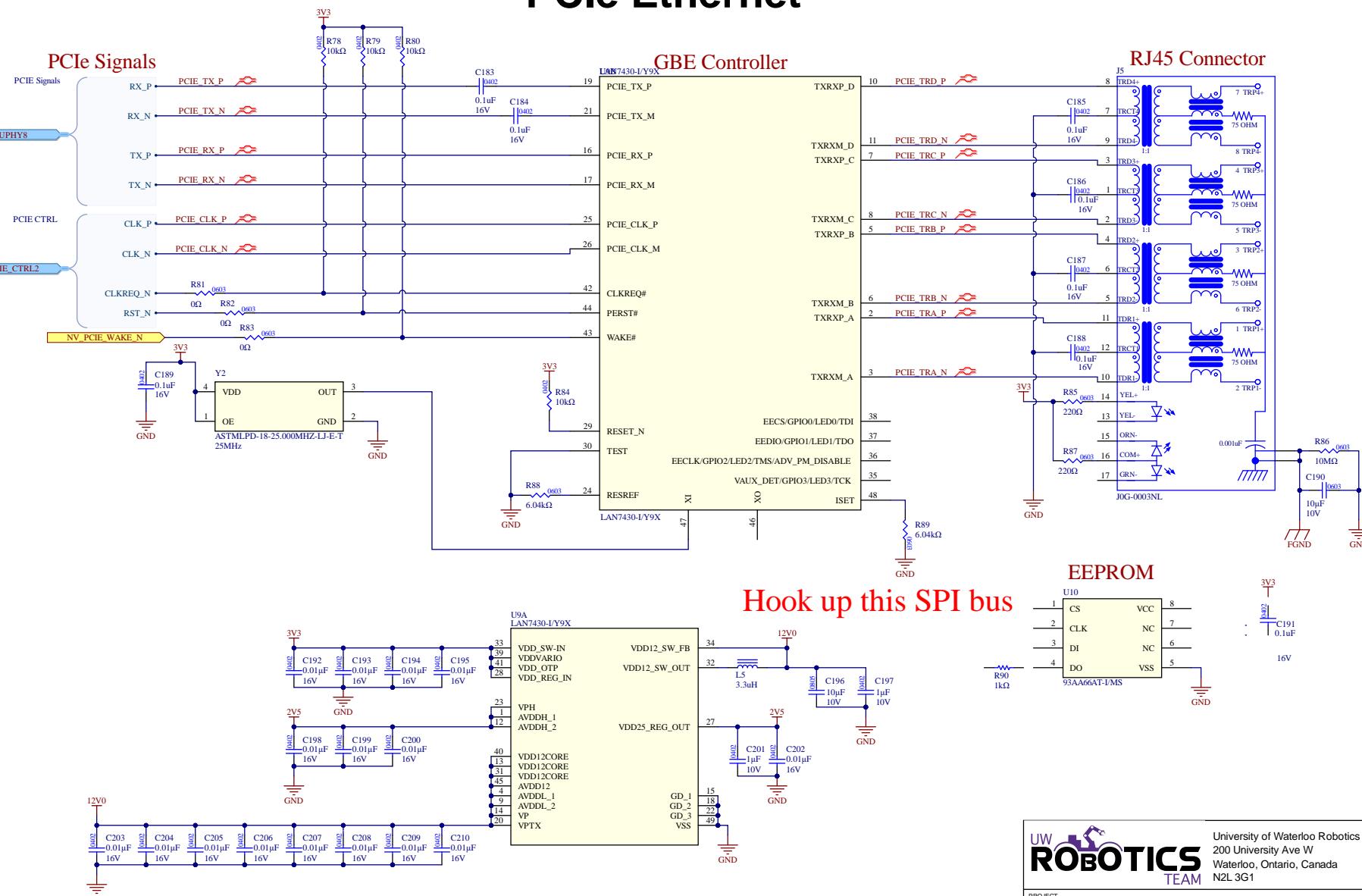
REVIEWER

Lance Bantoto

SHEET 14 OF 23



PCIe Ethernet



Hook up this SPI bus



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DOCUMENT
PCIe ETHERNET.SchDoc

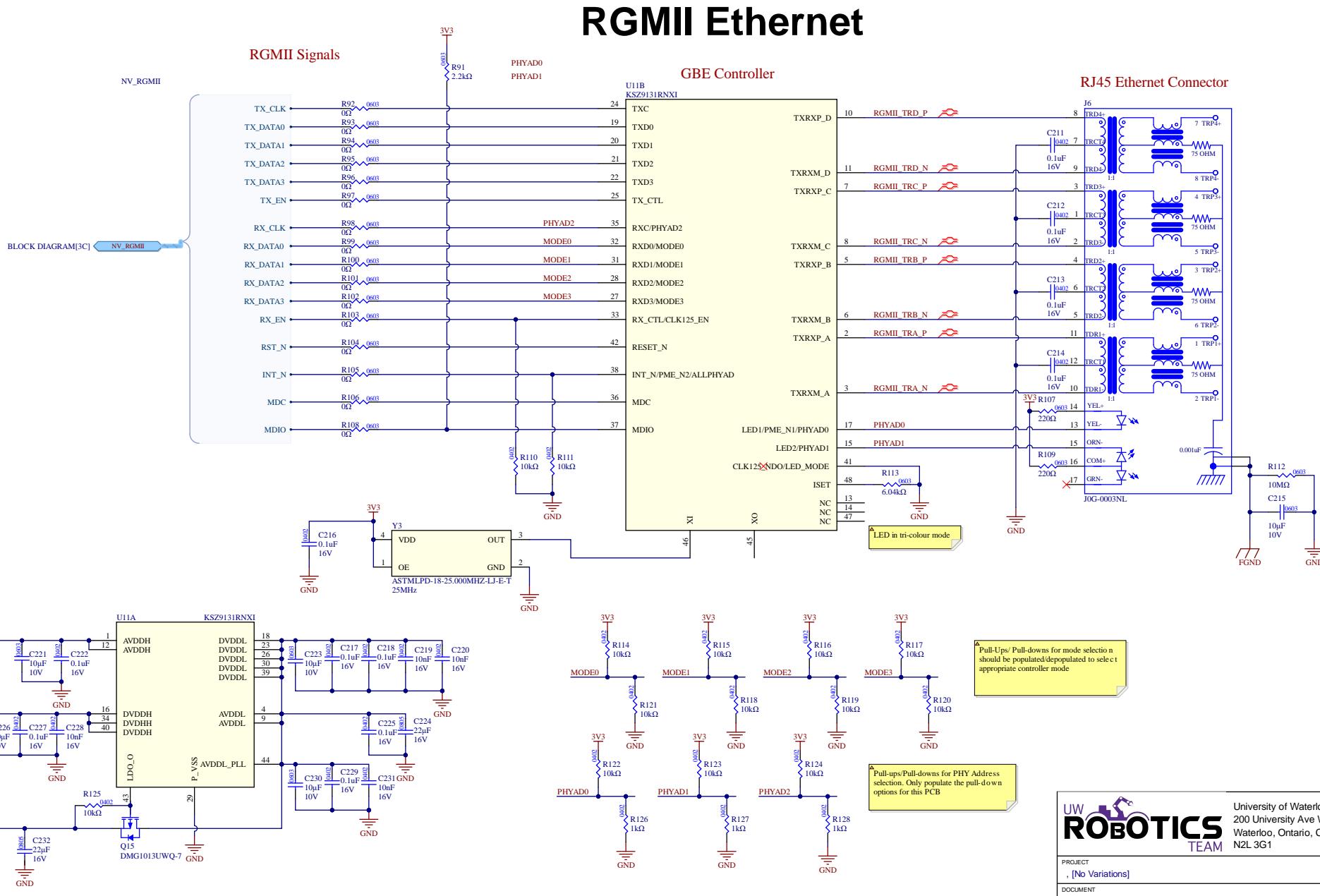
2021-08-24

ENGINEER
Chealsie Bains

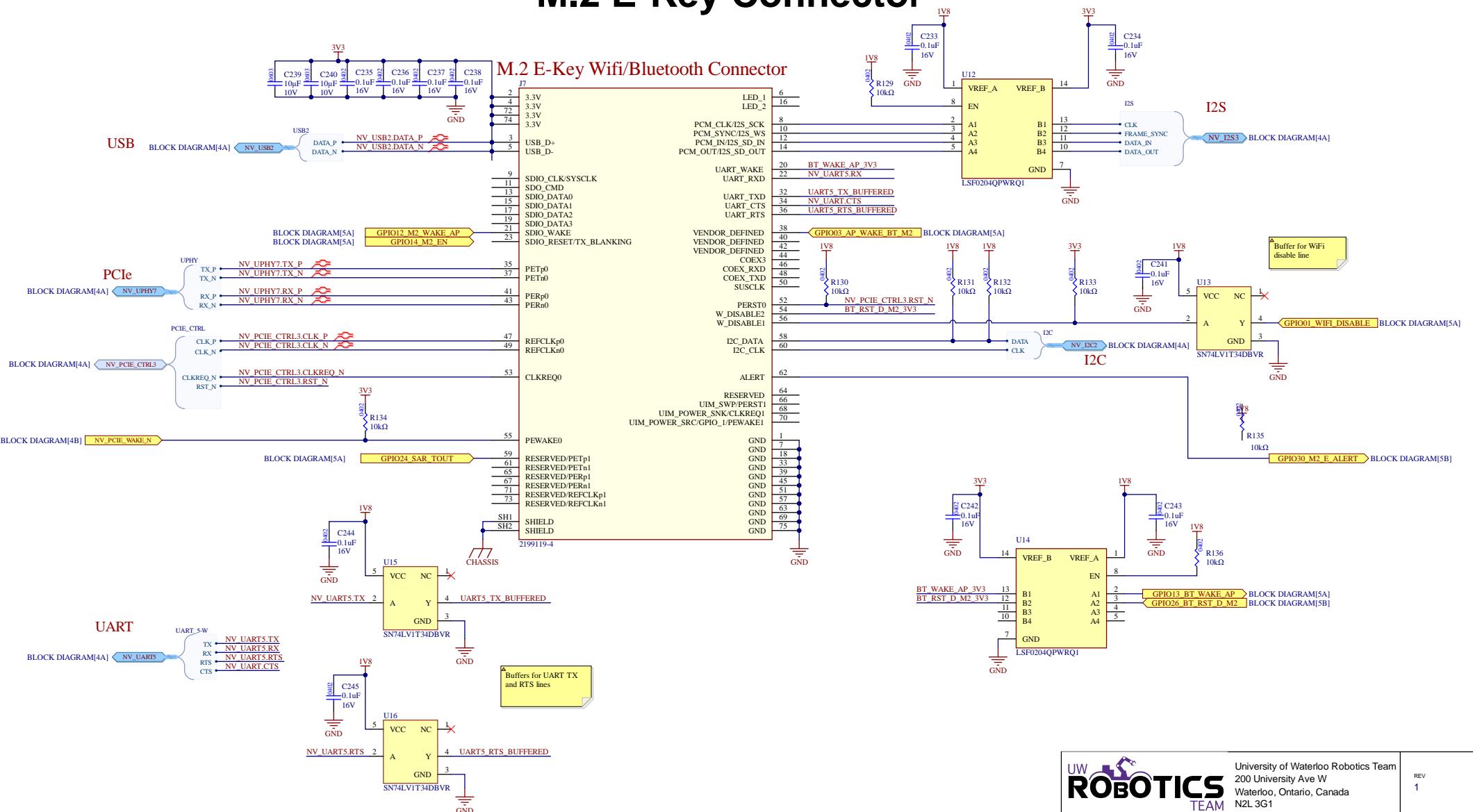
REVIEWER
Lance Bantoto

SHEET 16 OF 23

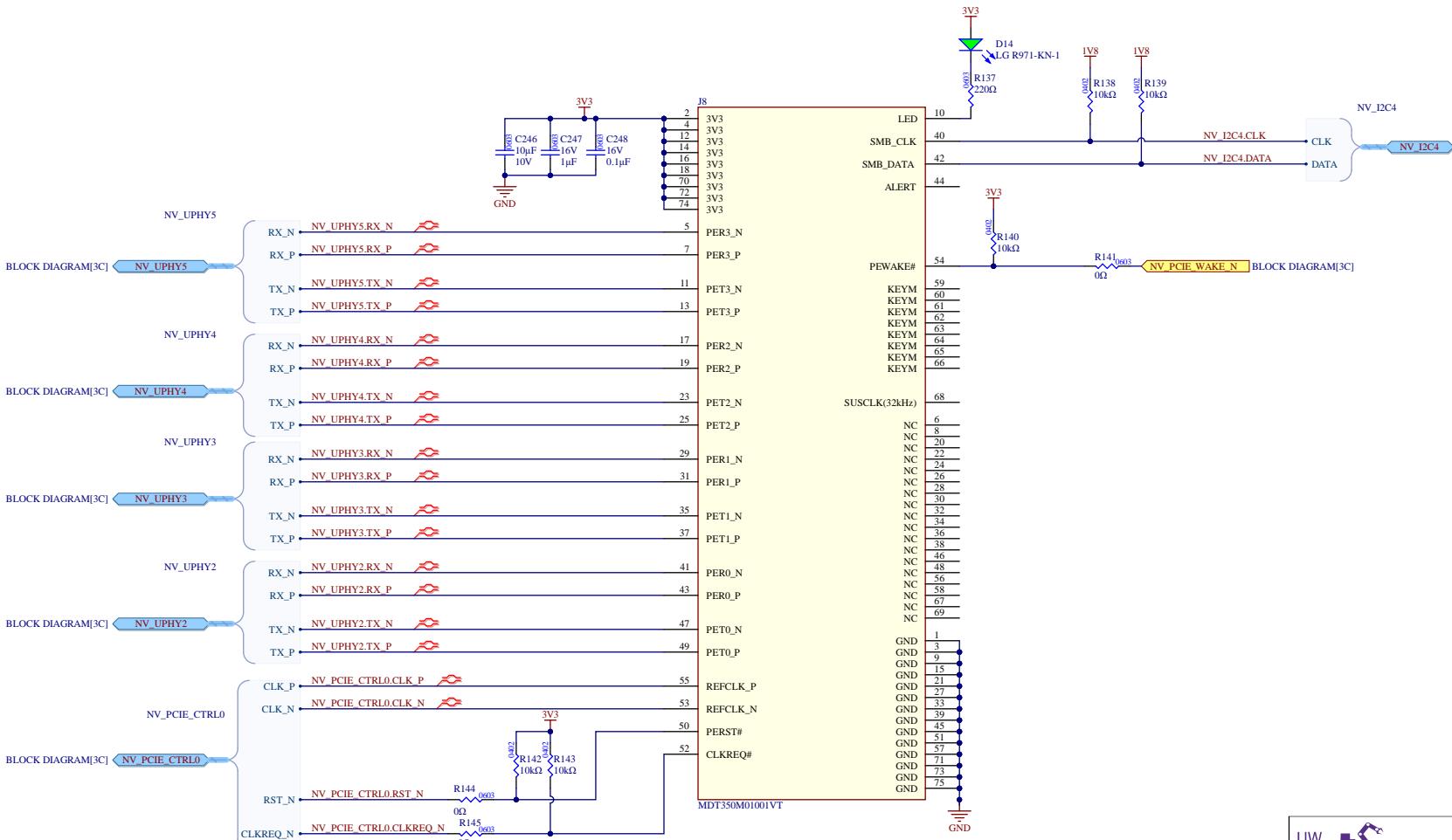
RGMII Ethernet



M.2 E-Key Connector



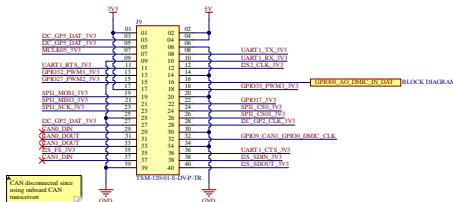
M.2 M-KEY Connector



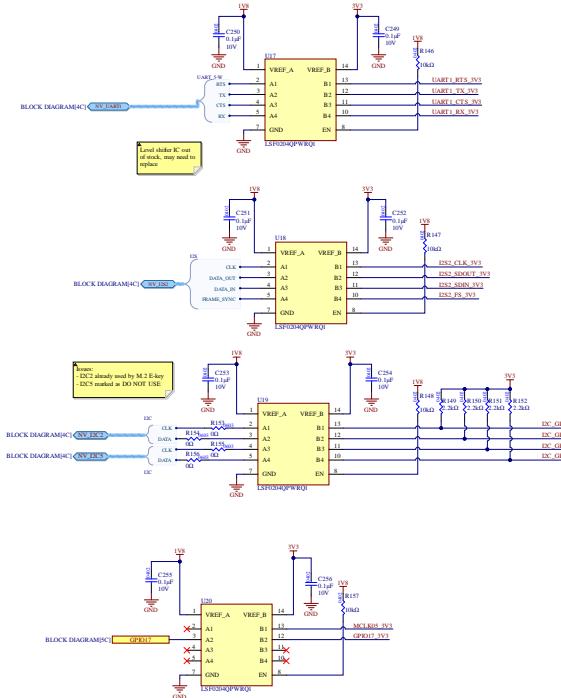
| | | |
|---|---------------------------|------------------------|
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| PROJECT Jetson AGX Xavier Carrier Board.PrjPcb, [No Variations] | | |
| DOCUMENT M.2 M-KEY.SchDoc | | MODIFIED 2021-08-24 |
| ENGINEER Chealsie Bains | REVIEWER Lance Bantoto | SHEET 19 OF 23 |

GPIO and Serial

GPIO Expansion



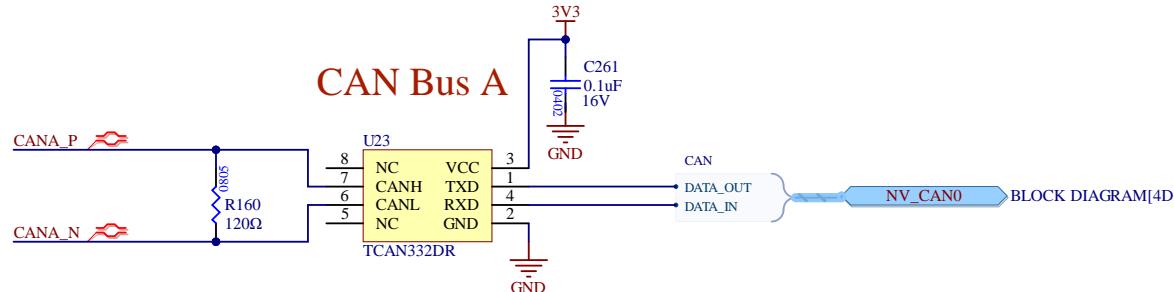
Level Shifters



CAN

A

A

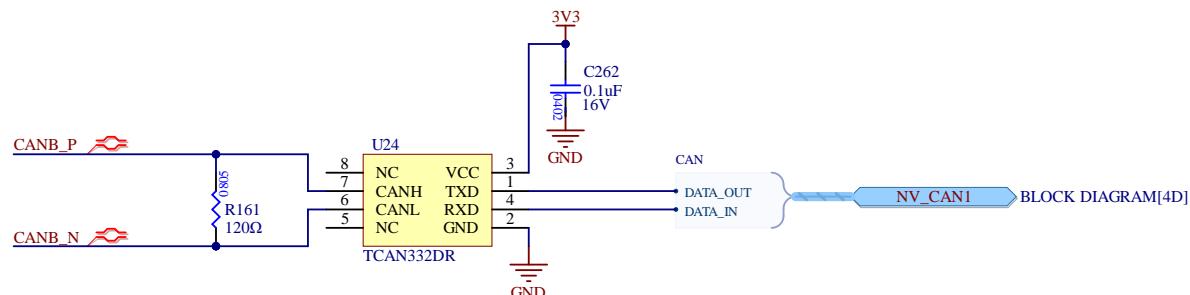


Select 8 pin connector

CAN Bus B

B

B



C

C

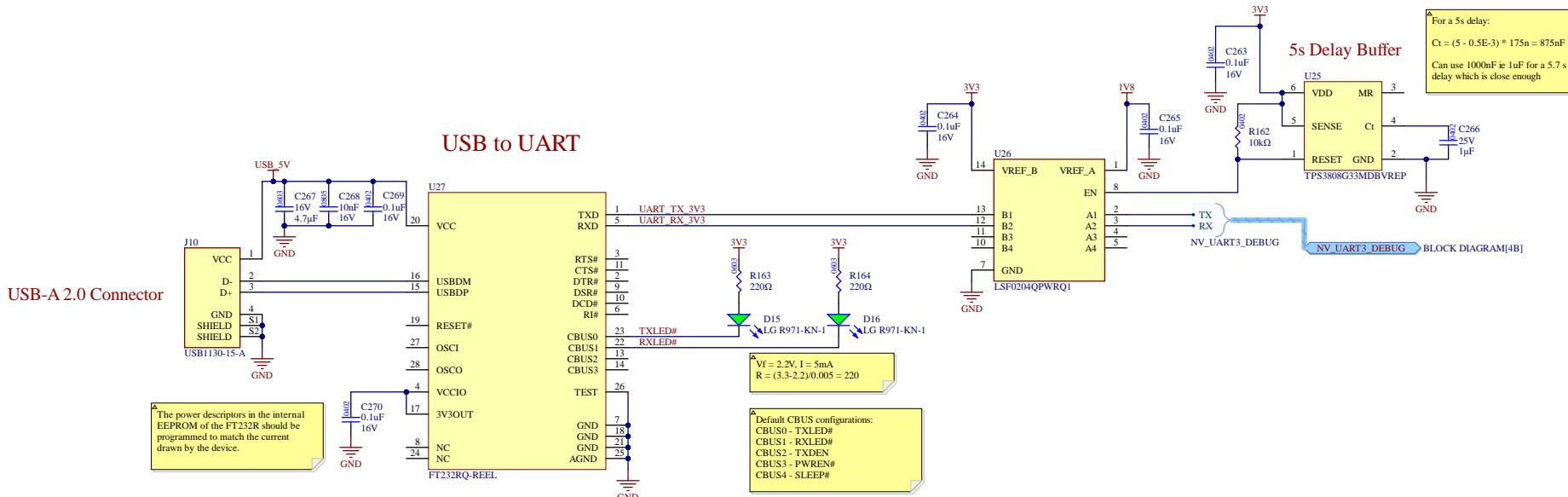


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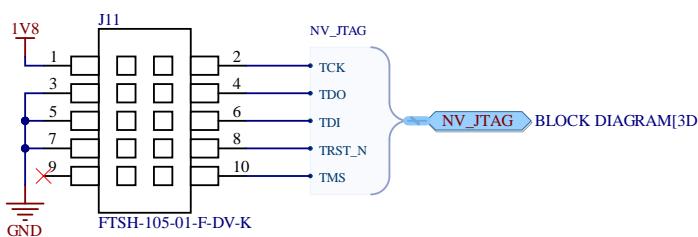
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|--|---------------------------|
| PROJECT Jetson AGX Xavier Carrier Board.PrjPcb, [No Variations] | |
| DOCUMENT CAN.SchDoc | MODIFIED 2021-08-24 |
| ENGINEER Cindy Li | REVIEWER Lance Bantoto |
| | SHEET 21 OF 23 |

Debug UART

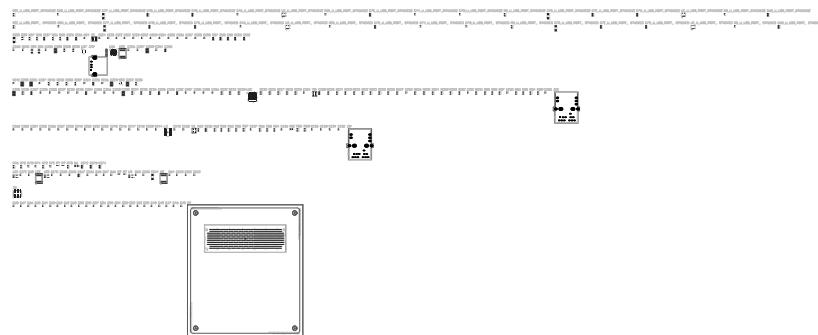


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|-------------------------|--|----------|---------------|-------|----------|
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| PROJECT | Jetson AGX Xavier Carrier Board.PrjPcb, [No Variations] | | | | |
| DOCUMENT | Debug UART.SchDoc | | | | |
| ENGINEER | Chealsie Bains | REVIEWER | Lance Bantoto | SHEET | 22 OF 23 |

JTAG



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| ROBOTICS TEAM | University of Waterloo Robotics Team 200 University Ave W Waterloo, Ontario, Canada N2L 3G1 | |
| | REV 1 | |
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| DOCUMENT JTAG.SchDoc | | |
| ENGINEER Cindy Li | REVIEWER Lance Bantoto | SHEET 23 OF 23 |



20'0"

