JX1 Pin	MicroZed Net Name	Zynq Pin	Zynq Name	VCCO Bank	Carrier board port name	Carrier board port impedance	Comment
1	JTAG_TCK	F9	TCK_0		(not connected)		
2	JTAG_TMS	J6	TMS_0		(not connected)		
3	JTAG_TDO	F6	TDO_0		(not connected)		
4	JTAG_TDI	G6	TDI_0		(not connected)		
5	NetJX1_5		PWR_EN		PWR_EN (TP5)		
6	NetJX1_6		CARRIER_SRST#		(not connected)		
7	FPGA_VBATT	F11	VCCBATT_0		VCCBAT (TP11)		
8	FPGA_DONE	R11	DONE_0		DONE (TP12)		
9	JX1_SE_0	R19	IO_0_34	34	J3_02	single-ended 50Ω	
10	JX1_SE_1	T19	IO_25_34	34	J3_01	single-ended 50Ω	
11	JX1_LVDS_0_P	T11	IO_L1P_T0_34	34	J3_03	single-ended 50Ω	
12	JX1_LVDS_1_P	T12	IO_L2P_T0_34	34	J3_05	single-ended 50Ω	
13	JX1_LVDS_0_N	T10	IO_L1N_T0_34	34	J3_04	single-ended 50Ω	
14	JX1_LVDS_1_N	U12	IO_L2N_T0_34	34	J3_06	single-ended 50Ω	
15	GND	A8	GND				
16	GND	A8	GND				
17	JX1_LVDS_2_P	U13	IO_L3P_T0_DQS_PUDC_B_34	34	JP2 PUDC	(uncontrolled)	JP2 controlls PUDC
18	JX1_LVDS_3_P	V12	IO_L4P_T0_34	34	J3_07	single-ended 50Ω	
19	JX1_LVDS_2_N	V13	IO_L3N_T0_DQS_34	34	J3_27	single-ended 50Ω	
20	JX1_LVDS_3_N	W13	IO_L4N_T0_34	34	J3_08	single-ended 50Ω	
21	GND	A8	GND				
22	GND	A8	GND				
23	JX1_LVDS_4_P	T14	IO_L5P_T0_34	34	J3_28	single-ended 50Ω	
24	JX1_LVDS_5_P	P14	IO_L6P_T0_34	34	J3_11	single-ended 50Ω	
25	JX1_LVDS_4_N	T15	IO_L5N_T0_34	34	J3_29	single-ended 50Ω	
26	JX1_LVDS_5_N	R14	IO_L6N_T0_VREF_34	34	J3_12	single-ended 50Ω	
27	GND	A8	GND				
28	GND	A8	GND				
29	JX1_LVDS_6_P	Y16	IO_L7P_T1_34	34	J3_30	single-ended 50Ω	
30	JX1_LVDS_7_P	W14	IO_L8P_T1_34	34	J3_13	(uncontrolled)	
31	JX1_LVDS_6_N	Y17	IO_L7N_T1_34	34	J3_31	single-ended 50Ω	
32	JX1_LVDS_7_N	Y14	IO_L8N_T1_34	34	J3_14	(uncontrolled)	
33	GND	A8	GND				
34	GND	A8	GND				
35	JX1_LVDS_8_P	T16	IO_L9P_T1_DQS_34	34	J3_09	single-ended 50Ω	
36	JX1_LVDS_9_P	V15	IO_L10P_T1_34	34	J3_17	(uncontrolled)	
37	JX1_LVDS_8_N	U17	IO_L9N_T1_DQS_34	34	J3_10	single-ended 50Ω	
38	JX1_LVDS_9_N	W15	IO_L10N_T1_34	34	J3_18	(uncontrolled)	
39	GND	A8	GND				
40	GND	A8	GND				
41	JX1_LVDS_10_P	U14	IO_L11P_T1_SRCC_34	34	J3_15	(uncontrolled)	
42	JX1_LVDS_11_P	U18	IO_L12P_T1_MRCC_34	34	J3_19	(uncontrolled)	
43	JX1_LVDS_10_N	U15	IO_L11N_T1_SRCC_34	34	J3_16	(uncontrolled)	
44	JX1_LVDS_11_N	U19	IO_L12N_T1_MRCC_34	34	J3_20	(uncontrolled)	
45	GND	A8	GND				
46	GND	A8	GND				
47	JX1_LVDS_12_P	N18	IO_L13P_T2_MRCC_34	34	OSC_50MHZ	single-ended 50Ω	input from oscillator X1, 50 MHz ±0.5ppm
48	JX1_LVDS_13_P	N20	IO_L14P_T2_SRCC_34	34	J3_21	(uncontrolled)	
49	JX1_LVDS_12_N	P19	IO_L13N_T2_MRCC_34	34	(not connected)		
50	JX1_LVDS_13_N	P20	IO_L14N_T2_SRCC_34	34	J3_22	(uncontrolled)	
51	GND	A8	GND				
52	GND	A8	GND				
53	JX1_LVDS_14_P	T20	IO_L15P_T2_DQS_34	34	J3_32_UART_RX	single-ended 50Ω	input from onboard USB to UART convert chip U5
54	JX1_LVDS_15_P	V20	IO_L16P_T2_34	34	J3_23	(uncontrolled)	
55	JX1_LVDS_14_N	U20	IO_L15N_T2_DQS_34	34	J3_33_UART_TX	single-ended 50Ω	output to onboard USB to UART convert chip U5
56	JX1_LVDS_15_N	W20	IO_L16N_T2_34	34	J3_24	(uncontrolled)	
57	VIN_HDR		VIN				
58	VIN_HDR		VIN				
59	VIN_HDR		VIN				
60	VIN_HDR		VIN				
61	JX1_LVDS_16_P	Y18	IO_L17P_T2_34	34	J3_34	single-ended 50Ω	
62	JX1_LVDS_17_P	V16	IO_L18P_T2_34	34	PMOD3_8	single-ended 50Ω	
63	JX1_LVDS_16_N	Y19	IO_L17N_T2_34	34	J3_35	single-ended 50Ω	
64	JX1_LVDS_17_N	W16	IO_L18N_T2_34	34	PMOD3_7	single-ended 50Ω	
65	GND	A8	GND				
66	GND	A8	GND				
67	JX1_LVDS_18_P	R16	IO_L19P_T3_34	34	J3_36	single-ended 50Ω	
68	JX1_LVDS_19_P	T17	IO_L20P_T3_34	34	PMOD3_6	single-ended 50Ω	
69	JX1_LVDS_18_N	R17	IO_L19N_T3_VREF_34	34	J3_37	single-ended 50Ω	
70	JX1_LVDS_19_N	R18	IO_L20N_T3_34	34	PMOD3_5	single-ended 50Ω	
71	GND	A8	GND				
72	GND	A8	GND				
73	JX1_LVDS_20_P	V17	IO_L21P_T3_DQS_34	34	J3_38	single-ended 50Ω	
74	JX1_LVDS_21_P	W18	IO_L22P_T3_34	34	PMOD3_4	single-ended 50Ω	
75	JX1_LVDS_20_N	V18	IO_L21N_T3_DQS_34	34	J3_39	single-ended 50Ω	
76	JX1_LVDS_21_N	W19	IO_L22N_T3_34	34	PMOD3_3	single-ended 50Ω	
77	GND	A8	GND				
78	VCCO_34	N19	VCCIO	34			
79	VCCO_34	N19	VCCIO	34			
80	VCCO_34	N19	VCCIO	34			

JX1 Pin	MicroZed Net Name	Zynq Pin	Zynq Name	VCCO Bank	Carrier board port name	Carrier board port impedance	Comment
81	JX1_LVDS_22_P	N17	IO_L23P_T3_34	34	J3_40	single-ended 50Ω	
82	JX1_LVDS_23_P	P15	IO_L24P_T3_34	34	PMOD3_2	single-ended 50Ω	
83	JX1_LVDS_22_N	P18	IO_L23N_T3_34	34	J3_41	single-ended 50Ω	
84	JX1_LVDS_23_N	P16	IO_L24N_T3_34	34	PMOD3_1	single-ended 50Ω	
85	GND	A8	GND				
86	GND	A8	GND				
87	BANK13_LVDS_0_P	U7	IO_L11P_T1_SRCC_13	13	J3_42	single-ended 50Ω	MicroZed 70**20** only
88	BANK13_LVDS_1_P	T9	IO_L12P_T1_MRCC_13	13	J3_26	single-ended 50Ω	MicroZed 70**20** only
89	BANK13_LVDS_0_N	V7	IO_L11N_T1_SRCC_13	13	J3_43	single-ended 50Ω	MicroZed 70**20** only
90	BANK13_LVDS_1_N	U10	IO_L12N_T1_MRCC_13	13	J3_48	single-ended 50Ω	MicroZed 70**20** only
91	BANK13_LVDS_2_P	V8	IO_L15P_T2_DQS_13	13	J3_44	single-ended 50Ω	MicroZed 70**20** only
92	BANK13_LVDS_3_P	T5	IO_L19P_T3_13	13	J3_49	single-ended 50Ω	MicroZed 70**20** only
93	BANK13_LVDS_2_N	W8	IO_L15N_T2_DQS_13	13	J3_45	single-ended 50Ω	MicroZed 70**20** only
94	BANK13_LVDS_3_N	U5	IO_L19N_T3_VREF_13	13	J3_52	single-ended 50Ω	MicroZed 70**20** only
95	GND	A8	GND				
96	GND	A8	GND				
97	NetJX1_97	K9	XADC_VP		J3_46	diff. pair 100Ω	analog input
98	NetJX1_98	M9	XADC_DXP		J3_51	diff. pair 100Ω	temperature-sensing diode pin (see UG475, Table1-12)
99	NetJX1_99	L10	XADC_VN		J3_47	diff. pair 100Ω	analog input
100	NetJX1_100	M10	XADC_DXN		J3_50	diff. pair 100Ω	temperature-sensing diode pin (see UG475, Table1-12)

JX2 Pin	MicroZed Net Name	Zynq Pin	Zynq Name	VCCO Bank	Carrier board port name	Carrier board port impedance	Comment
1	PMOD_D0	E8	PS_MIO13_500		(not connected)		
2	PMOD_D1	E9	PS_MIO10_500		(not connected)		
3	PMOD_D2	C6	PS_MIO11_500		(not connected)		
4	PMOD_D3	D9	PS_MIO12_500		(not connected)		
5	PMOD_D4	E6	PS_MIO0_500		(not connected)		
6	PMOD_D5	B5	PS_MIO9_500		(not connected)		
7	PMOD_D6	C5	PS_MIO14_500		(not connected)		
8	PMOD_D7	C8	PS_MIO15_500		(not connected)		
9	NetJX2_9	R10	INIT_B		(not connected)		
10	NetJX2_10	L6	VCCIO_EN		VCCIO_EN (TP7)		
11	PG_MODULE	C7	PG_CARRIER		PG_CARRIER (TP10)		
12	VIN_HDR		VIN				
13	JX2_SE_0	G14	IO_0_35	35	SWITCH2		
14	JX2_SE_1	J15	IO_25_35	35	LED2		
15	GND	A8	GND				
16	GND	A8	GND				
17	JX2_LVDS_0_P	C20	IO_L1P_T0_AD0P_35	35	LED1		
18	JX2_LVDS_1_P	B19	IO_L2P_T0_AD8P_35	35	J4_10	diff. pair 100Ω	
19	JX2_LVDS_0_N	B20	IO_L1N_T0_AD0N_35	35	SWITCH1		
20	JX2_LVDS_1_N	A20	IO_L2N_T0_AD8N_35	35	J4_09	diff. pair 100Ω	
21	GND	A8	GND				
22	GND	A8	GND				
23	JX2_LVDS_2_P	E17	IO_L3P_T0_DQS_AD1P_35	35	J4_14	diff. pair 100Ω	
24	JX2_LVDS_3_P	D19	IO_L4P_T0_35	35	J4_08	diff. pair 100Ω	
25	JX2_LVDS_2_N	D18	IO_L3N_T0_DQS_AD1N_35	35	J4_13	diff. pair 100Ω	
26	JX2_LVDS_3_N	D20	IO_L4N_T0_35	35	J4_07	diff. pair 100Ω	
27	GND	A8	GND				
28	GND	A8	GND				
29	JX2_LVDS_4_P	E18	IO_L5P_T0_AD9P_35	35	J4_12	diff. pair 100Ω	
30	JX2_LVDS_5_P	F16	IO_L6P_T0_35	35	J4_06	diff. pair 100Ω	
31	JX2_LVDS_4_N	E19	IO_L5N_T0_AD9N_35	35	J4_11	diff. pair 100Ω	
32	JX2_LVDS_5_N	F17	IO_L6N_T0_VREF_35	35	J4_05	diff. pair 100Ω	
33	GND	A8	GND				
34	GND	A8	GND				
35	JX2_LVDS_6_P	L19	IO_L9P_T1_DQS_AD3P_35	35	J4_17	diff. pair 100Ω	
36	JX2_LVDS_7_P	M19	IO_L7P_T1_AD2P_35	35	J4_04	diff. pair 100Ω	
37	JX2_LVDS_6_N	L20	IO_L9N_T1_DQS_AD3N_35	35	J4_16	diff. pair 100Ω	
38	JX2_LVDS_7_N	M20	IO_L7N_T1_AD2N_35	35	J4_03	diff. pair 100Ω	
39	GND	A8	GND				
40	GND	A8	GND				
41	JX2_LVDS_8_P	M17	IO_L8P_T1_AD10P_35	35	PMOD2_1	single-ended 50Ω	Output shifted to 5V
42	JX2_LVDS_9_P	K19	IO_L10P_T1_AD11P_35	35	J4_02	diff. pair 100Ω	
43	JX2_LVDS_8_N	M18	IO_L8N_T1_AD10N_35	35	PMOD2_2	single-ended 50Ω	Output shifted to 5V
44	JX2_LVDS_9_N	J19	IO_L10N_T1_AD11N_35	35	J4_01	diff. pair 100Ω	
45	GND	A8	GND				
46	GND	A8	GND				
47	JX2_LVDS_10_P	L16	IO_L11P_T1_SRCC_35	35	PMOD2_3	single-ended 50Ω	Output shifted to 5V
48	JX2_LVDS_11_P	K17	IO_L12P_T1_MRCC_35	35	J4_20	diff. pair 100Ω	
49	JX2_LVDS_10_N	L17	IO_L11N_T1_SRCC_35	35	PMOD2_4	single-ended 50Ω	Output shifted to 5V
50	JX2_LVDS_11_N	K18	IO_L12N_T1_MRCC_35	35	J4_21	diff. pair 100Ω	
51	GND	A8	GND				
52	GND	A8	GND				
53	JX2_LVDS_12_P	H16	IO_L13P_T2_MRCC_35	35	PMOD2_5	single-ended 50Ω	Output shifted to 5V
54	JX2_LVDS_13_P	J18	IO_L14P_T2_AD4P_SRCC_35	35	J4_22	diff. pair 100Ω	
55	JX2_LVDS_12_N	H17	IO_L13N_T2_MRCC_35	35	PMOD2_6	single-ended 50Ω	Output shifted to 5V
56	JX2_LVDS_13_N	H18	IO_L14N_T2_AD4N_SRCC_35	35	J4_23	diff. pair 100Ω	
57	VIN_HDR		VIN				
58	VIN_HDR		VIN				
59	VIN_HDR		VIN				
60	VIN_HDR		VIN				
61	JX2_LVDS_14_P	G17	IO_L16P_T2_35	35	PMOD2_7	single-ended 50Ω	Output shifted to 5V
62	JX2_LVDS_15_P	F19	IO_L15P_T2_DQS_AD12P_35	35	J4_24	diff. pair 100Ω	
63	JX2_LVDS_14_N	G18	IO_L16N_T2_35	35	PMOD2_8	single-ended 50Ω	Output shifted to 5V
64	JX2_LVDS_15_N	F20	IO_L15N_T2_DQS_AD12N_35	35	J4_25	diff. pair 100Ω	
65	GND	A8	GND				
66	GND	A8	GND				
67	JX2_LVDS_16_P	G19	IO_L18P_T2_AD13P_35	35	PMOD1_1	diff. pair 100Ω	Output shifted to 5V
68	JX2_LVDS_17_P	J20	IO_L17P_T2_AD5P_35	35	J4_26	diff. pair 100Ω	
69	JX2_LVDS_16_N	G20	IO_L18N_T2_AD13N_35	35	PMOD1_2	diff. pair 100Ω	Output shifted to 5V
70	JX2_LVDS_17_N	H20	IO_L17N_T2_AD5N_35	35	J4_27	diff. pair 100Ω	
71	GND	A8	GND				
72	GND	A8	GND				

JX2 Pin	MicroZed Net Name	Zynq Pin	Zynq Name	VCCO Bank	Carrier board port name	Carrier board port impedance	Comment
73	JX2_LVDS_18_P	K14	IO_L20P_T3_AD6P_35	35	PMOD1_3	diff. pair 100Ω	Output shifted to 5V
74	JX2_LVDS_19_P	H15	IO_L19P_T3_35	35	J4_28	diff. pair 100Ω	
75	JX2_LVDS_18_N	J14	IO_L20N_T3_AD6N_35	35	PMOD1_4	diff. pair 100Ω	Output shifted to 5V
76	JX2_LVDS_19_N	G15	IO_L19N_T3_VREF_35	35	J4_29	diff. pair 100Ω	
77	GND	A8	GND				
78	VCCO_35	C19	VCCIO	35			
79	VCCO_35	C19	VCCIO	35			
80	VCCO_35	C19	VCCIO	35			
81	JX2_LVDS_20_P	N15	IO_L21P_T3_DQS_AD14P_35	35	PMOD1_5	diff. pair 100Ω	Output shifted to 5V
82	JX2_LVDS_21_P	L14	IO_L22P_T3_AD7P_35	35	J4_30	diff. pair 100Ω	
83	JX2_LVDS_20_N	N16	IO_L21N_T3_DQS_AD14N_35	35	PMOD1_6	diff. pair 100Ω	Output shifted to 5V
84	JX2_LVDS_21_N	L15	IO_L22N_T3_AD7N_35	35	J4_31	diff. pair 100Ω	
85	GND	A8	GND				
86	GND	A8	GND				
87	JX2_LVDS_22_P	M14	IO_L23P_T3_35	35	PMOD1_7	diff. pair 100Ω	Output shifted to 5V
88	JX2_LVDS_23_P	K16	IO_L24P_T3_AD15P_35	35	J4_32	diff. pair 100Ω	
89	JX2_LVDS_22_N	M15	IO_L23N_T3_35	35	PMOD1_8	diff. pair 100Ω	Output shifted to 5V
90	JX2_LVDS_23_N	J16	IO_L24N_T3_AD15N_35	35	J4_33	diff. pair 100Ω	
91	GND	A8	GND				
92	GND	A8	GND				
93	BANK13_LVDS_4_P	Y12	IO_L20P_T3_13	13	J4_18	diff. pair 100Ω	MicroZed 70**20** only
94	BANK13_LVDS_5_P	V11	IO_L21P_T3_DQS_13	13	J4_34	diff. pair 100Ω	MicroZed 70**20** only
95	BANK13_LVDS_4_N	Y13	IO_L20N_T3_13	13	J4_19	diff. pair 100Ω	MicroZed 70**20** only
96	BANK13_LVDS_5_N	V10	IO_L21N_T3_DQS_13	13	J4_35	diff. pair 100Ω	MicroZed 70**20** only
97	BANK13_LVDS_6_P	V6	IO_L22P_T3_13	13	J4_38	diff. pair 100Ω	MicroZed 70**20** only
98	VCCO_13	T8	VCCIO	13			MicroZed 70**20** only
99	BANK13_LVDS_6_N	W6	IO_L22N_T3_13	13	J4_37	diff. pair 100Ω	MicroZed 70**20** only
100	BANK13_SE_0	V5	IO_L6N_T0_VREF_13	13	J4_36	single-ended 50Ω	MicroZed 70**20** only