

Buskerud and Vestfold University College

Compulsory Coursework

Part 2: Music box

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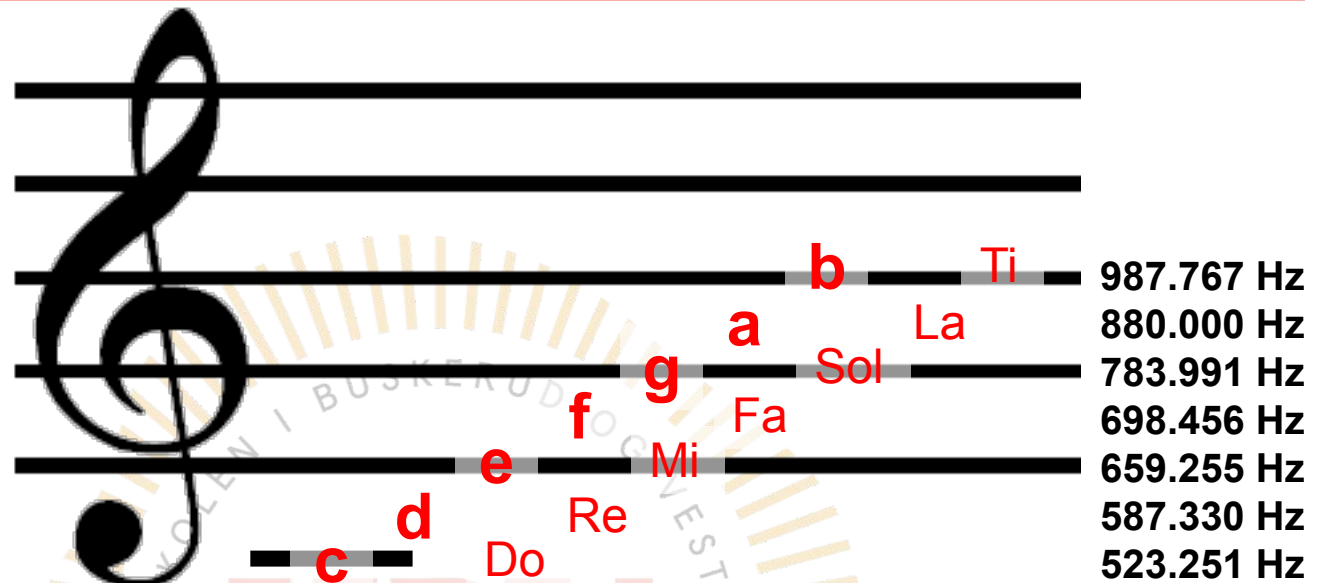
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Learning outcomes

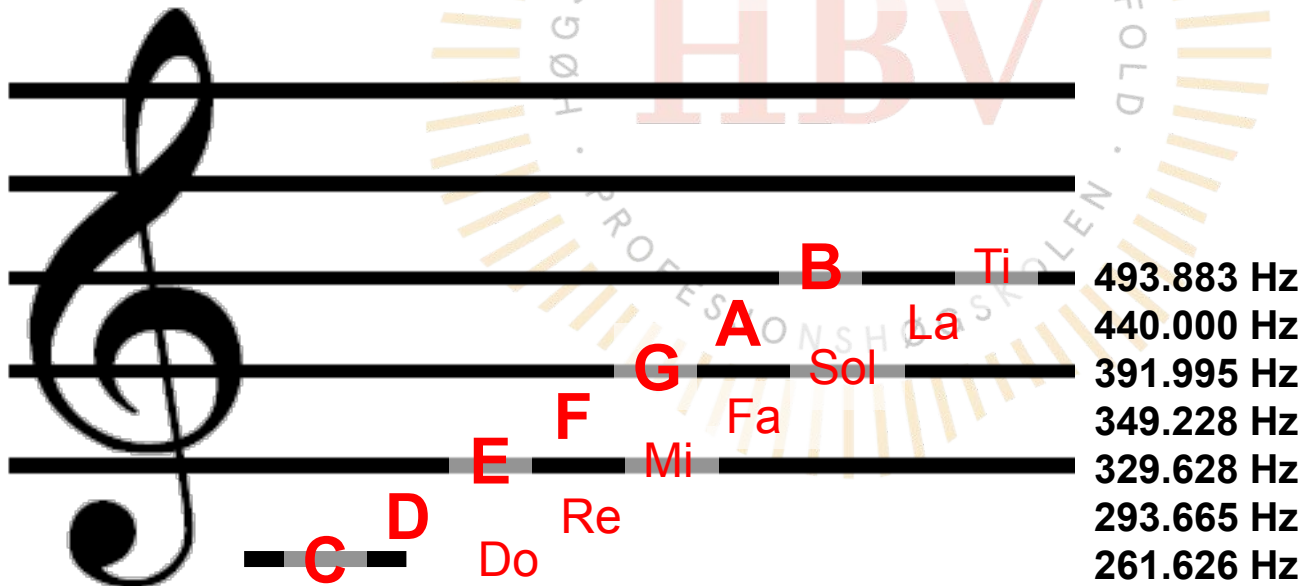
You'll be able to:

- Work with the very basics of music notation
- Explain the functional specification of the required music box
- Identify the main design tasks and divide them among the group members
- Set up a plan for the development work

Octave 5
frequencies



Octave 4
frequencies



(for the full range corresponding to an 88-key piano, see Wikipedia at <https://goo.gl/P9FG0u>)

Beethoven's "Ode to Joy" sound-alike melody using octaves 4 and 5

Ode to Joy

L. Van Beethoven

The image displays a musical score for the 'Ode to Joy' melody, arranged in four staves. Each staff begins with a treble clef, a key signature of one sharp (F#), and a 4/4 time signature. The notes are represented by black dots on the staff lines, with letter names (B, A, G, F, E, D, C, B) placed below them. The melody is written in a simplified, sound-alike style using only octaves 4 and 5. The first staff contains 14 notes: B, B, c, d, d, c, B, A, G, G, A, B, B, A, A, A. The second staff contains 14 notes: B, B, c, d, d, c, B, A, G, G, A, B, A, G, G, G. The third staff contains 14 notes: A, A, B, G, A, B, c, B, G, A, B, c, B, A, G, A, D. The fourth staff contains 14 notes: B, B, c, d, d, c, B, A, G, G, A, B, A, G, G, G. The score is watermarked with 'L. Van Beethoven' and 'Ode to Joy'.

B B c d d c B A G G A B B A A A

B B c d d c B A G G A B A G G G

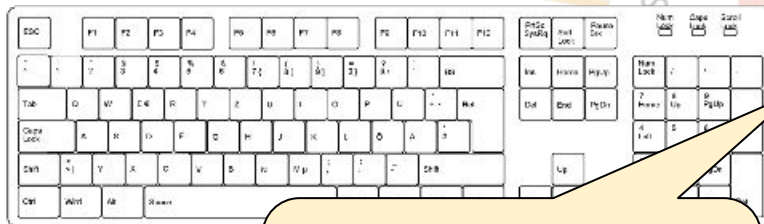
A A B G A B c B G A B c B A G A D

B B c d d c B A G G A B A G G G

Overview of the music box

Check section 11.4 of P. Chu's book

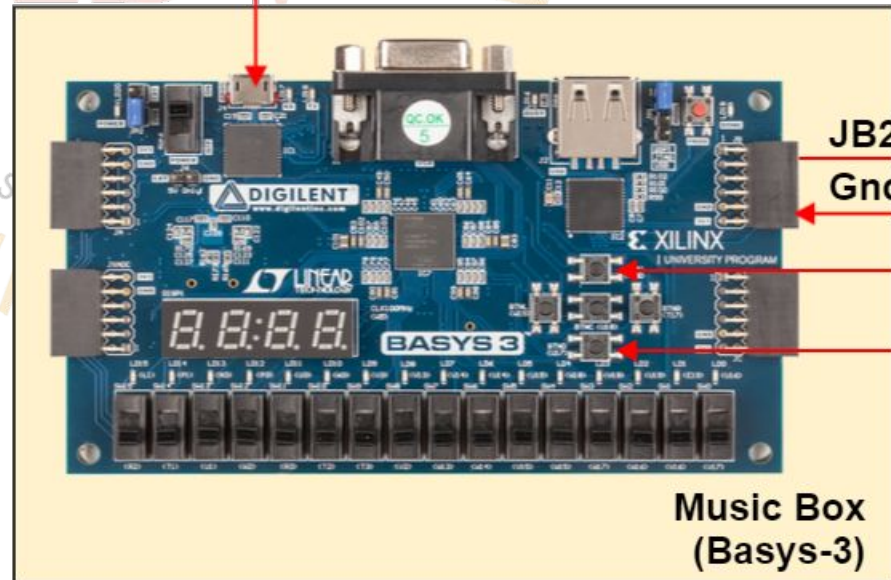
- Store the melody a local RAM as a sequence of ASCII characters typed in the computer keyboard
- Press “Play” to listen



e.g. PuTTY or Hyperterminal

(RS232)

Rx



Reset

Play

Music Box
(Basys-3)

Simplifying assumptions

- Octaves 4 and 5 only (frequency range from 261.626 Hz to 987.767 Hz)
- Fixed duration for all notes (e.g. double duration will be achieved by repeating the note)

Recommended approach

- Define the architecture of the **FSMD datapath** (what blocks need to be present)
- Design the **ASMD chart**
- Build the **VHDL description**, simulate, and try it out in the Basys-3 board

Proposed roadmap

- Group: Define FSMD architecture and design ASMD chart
- Individual: Build the VHDL description from the chart
- Group: Design verification (simulation) in Vivado
- Individual: Allocate FPGA pins, generate .bit file, program the FPGA and check operation in the Basys-3 board

Deliverables (deadline is 23:59, Sunday March 18th):

- A presentation (5~10 min.) explaining your work and results, including simulation waveforms and experimental demo (video)
- The Vivado project folder