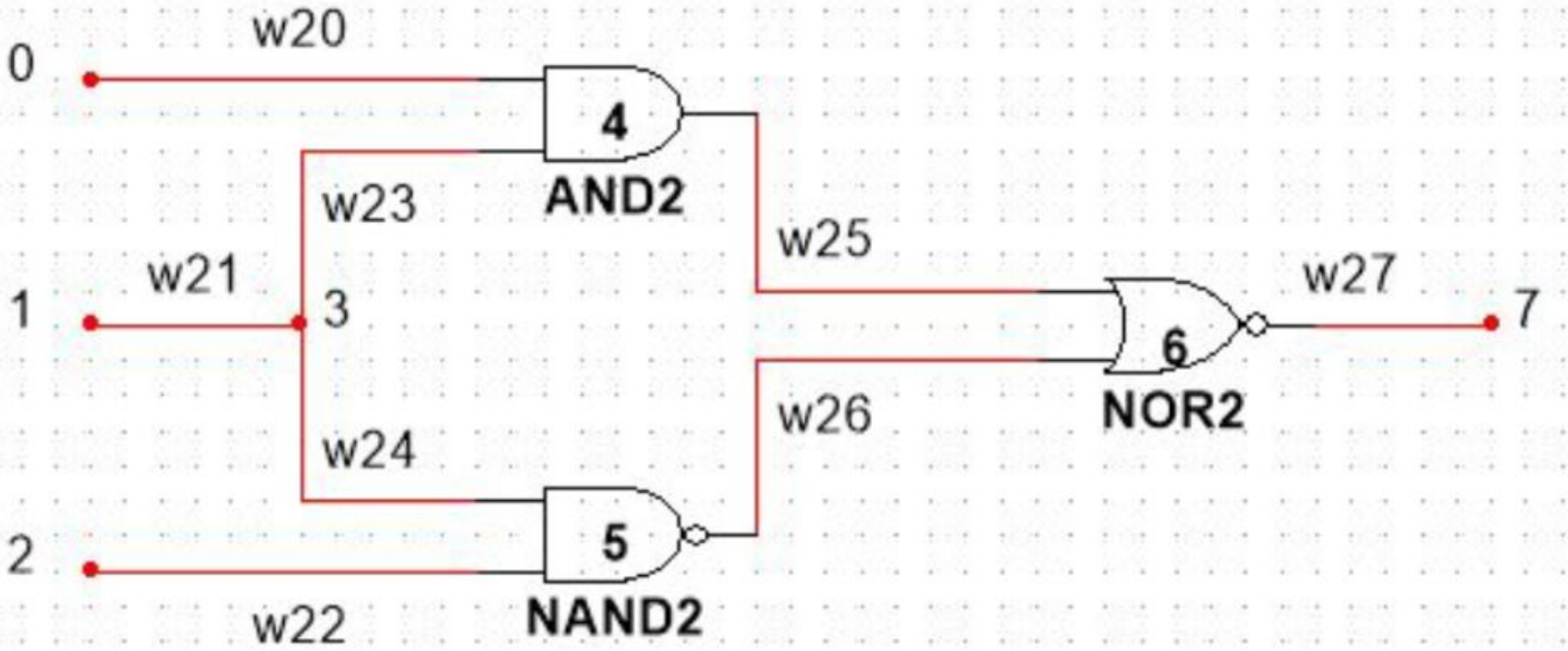
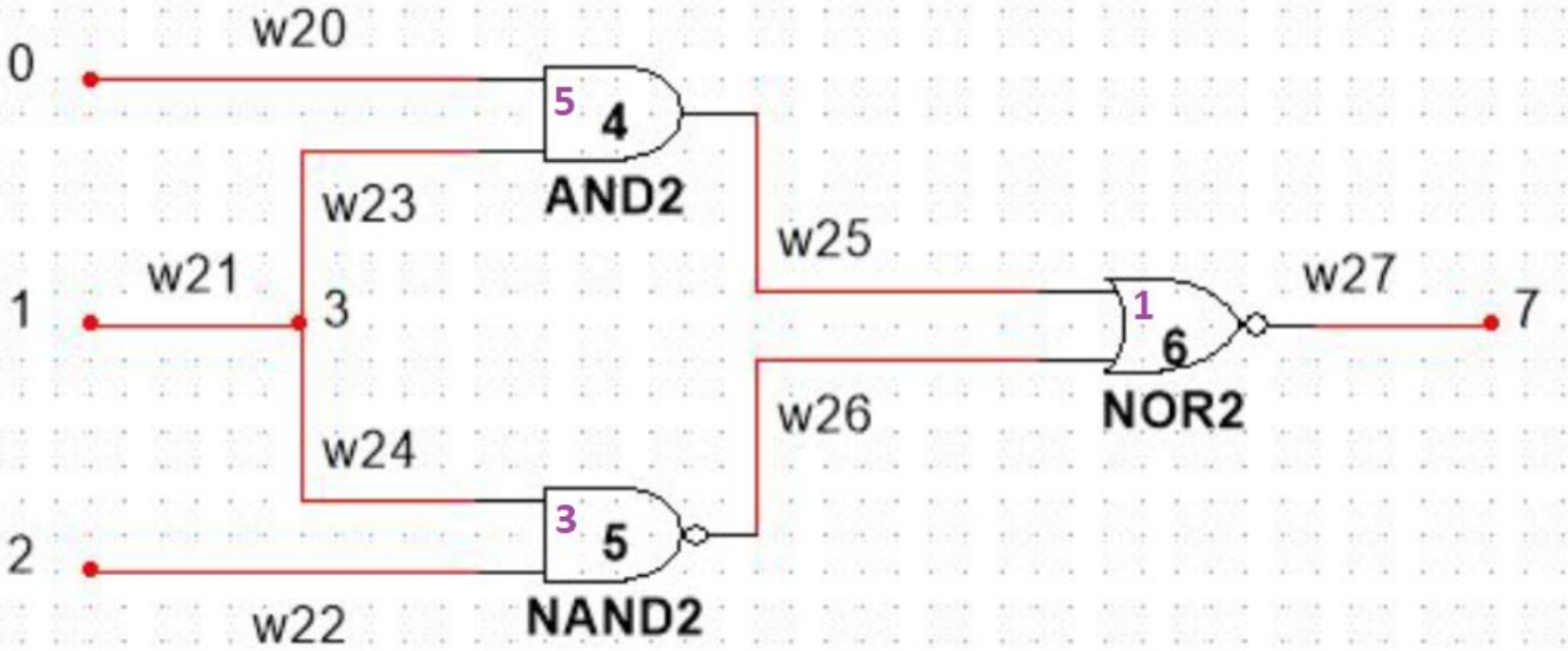
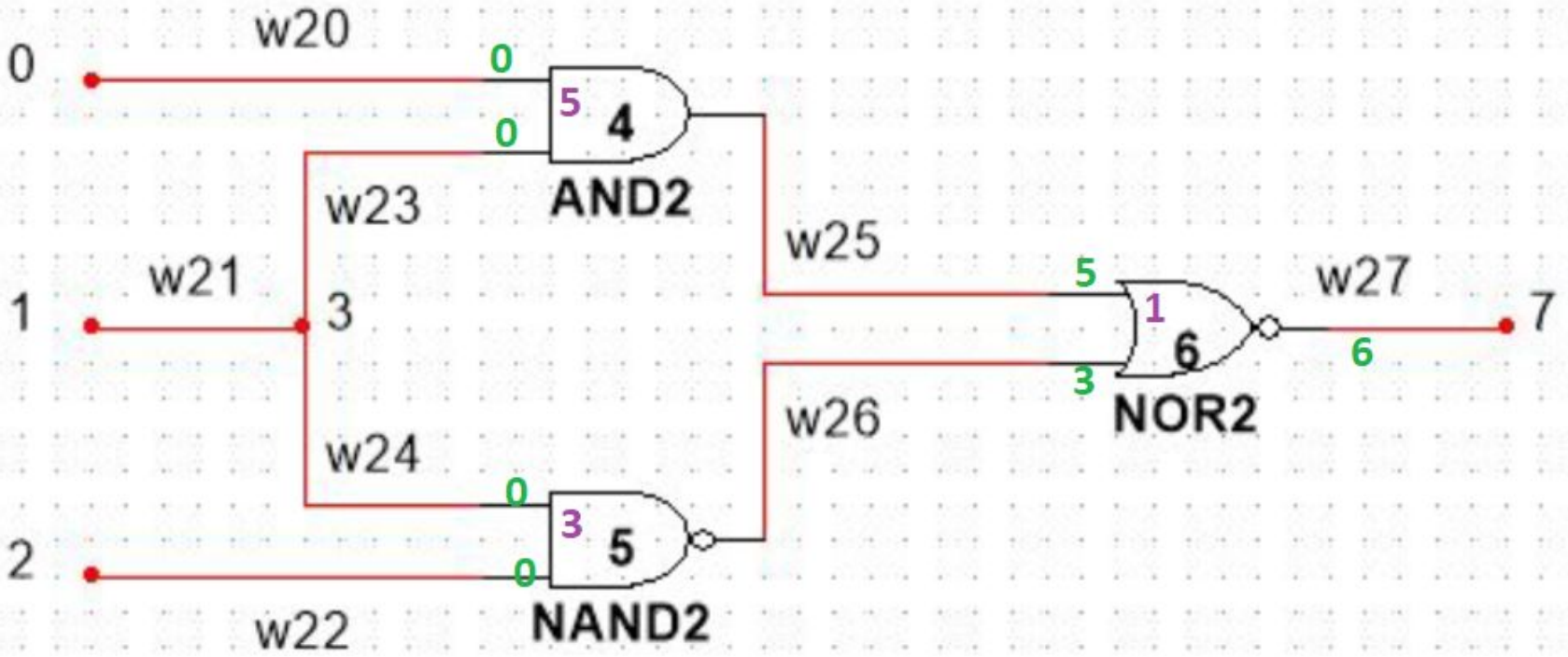
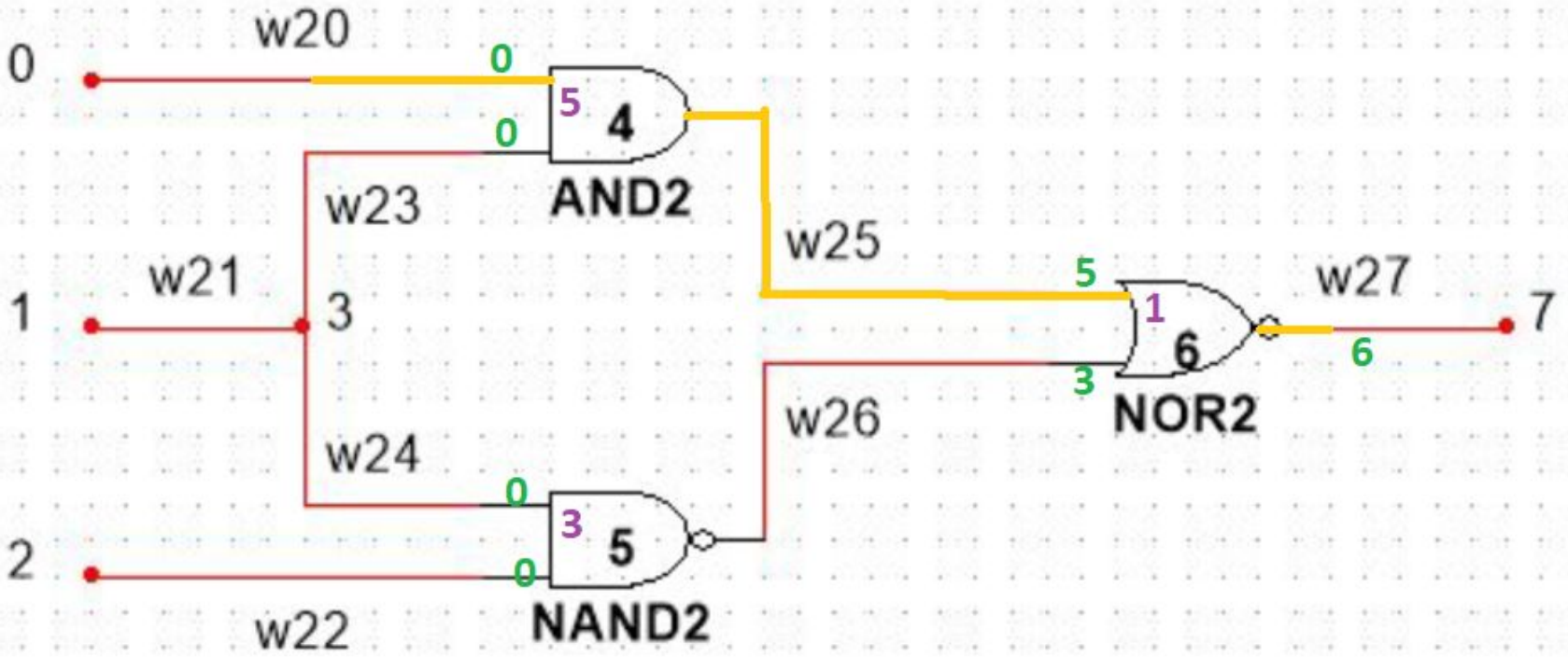


Circuit

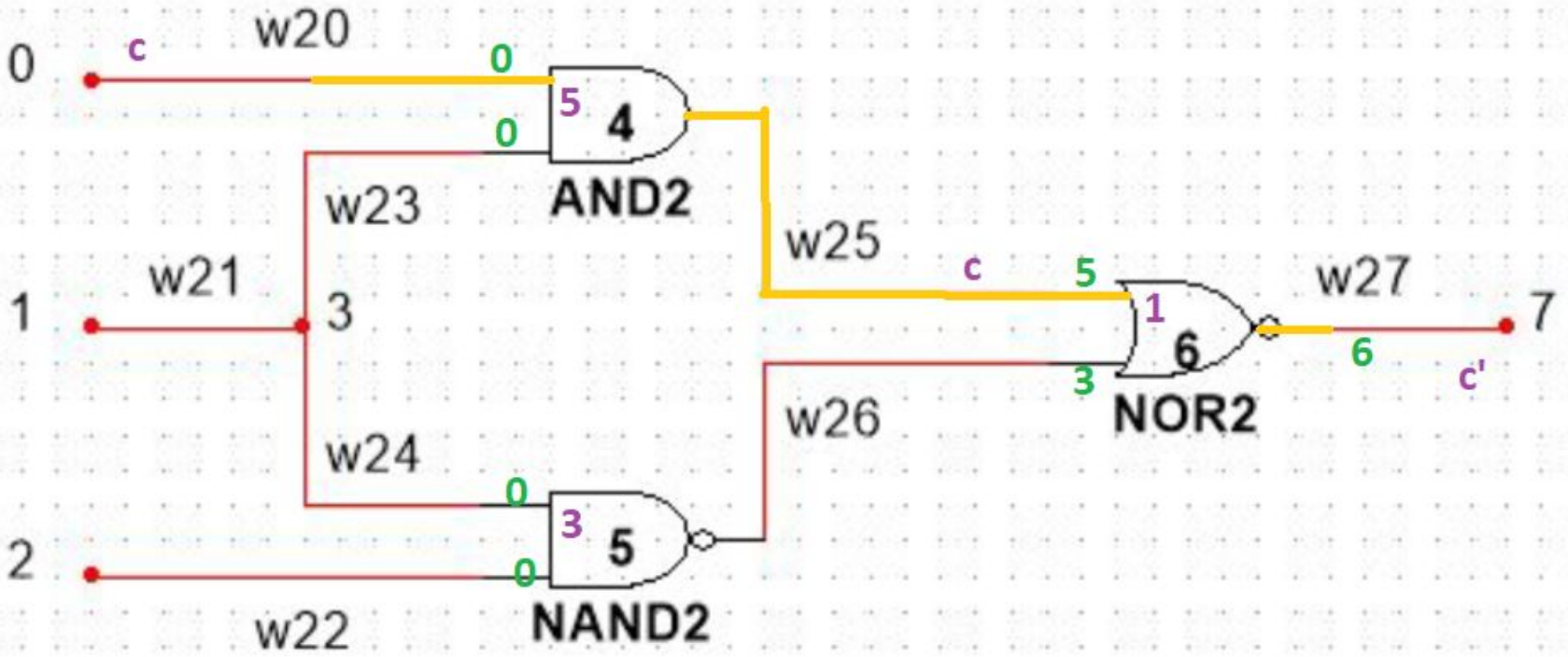


Read Delay File

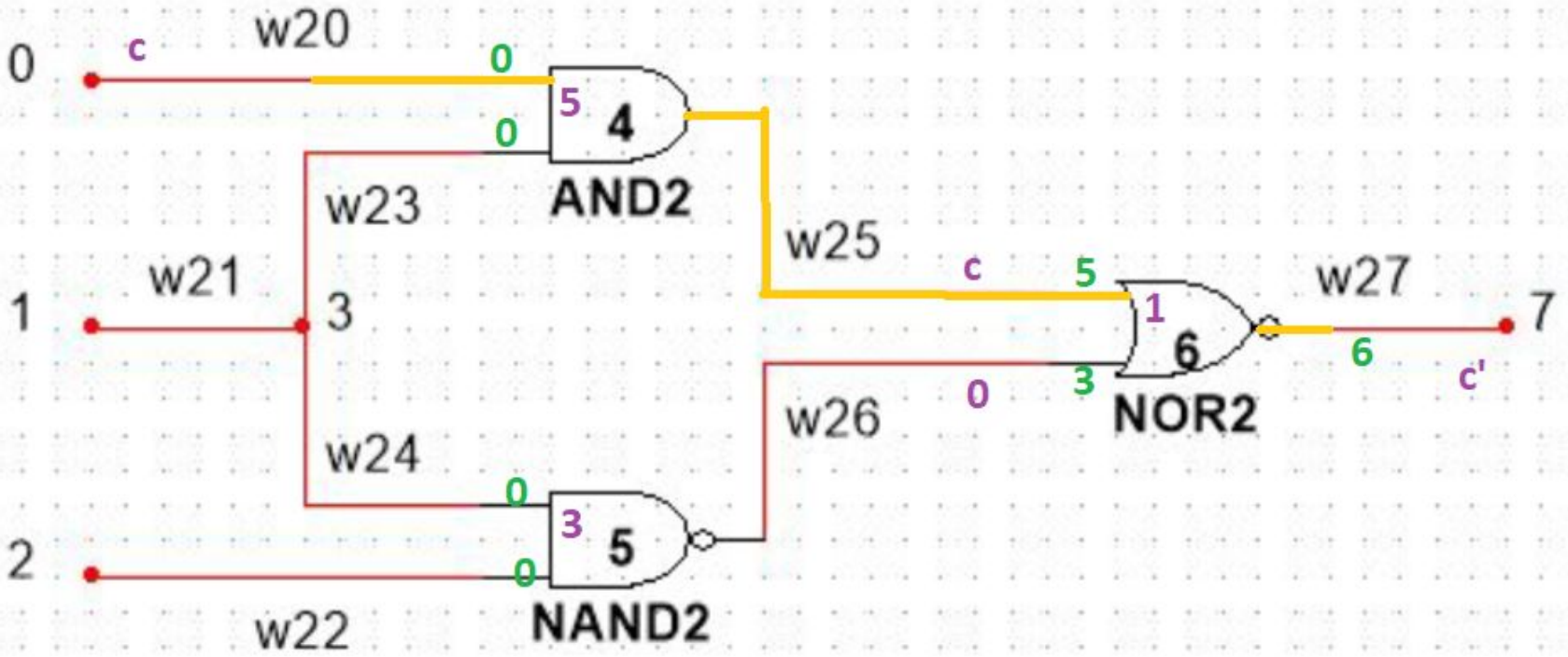

0
w20
0
5
4
0
AND2
w23
w21
1
3
w25
5
1
6
3
NOR2
w27
6
7
w26
w24
0
3
5
0
2
w22
NAND2



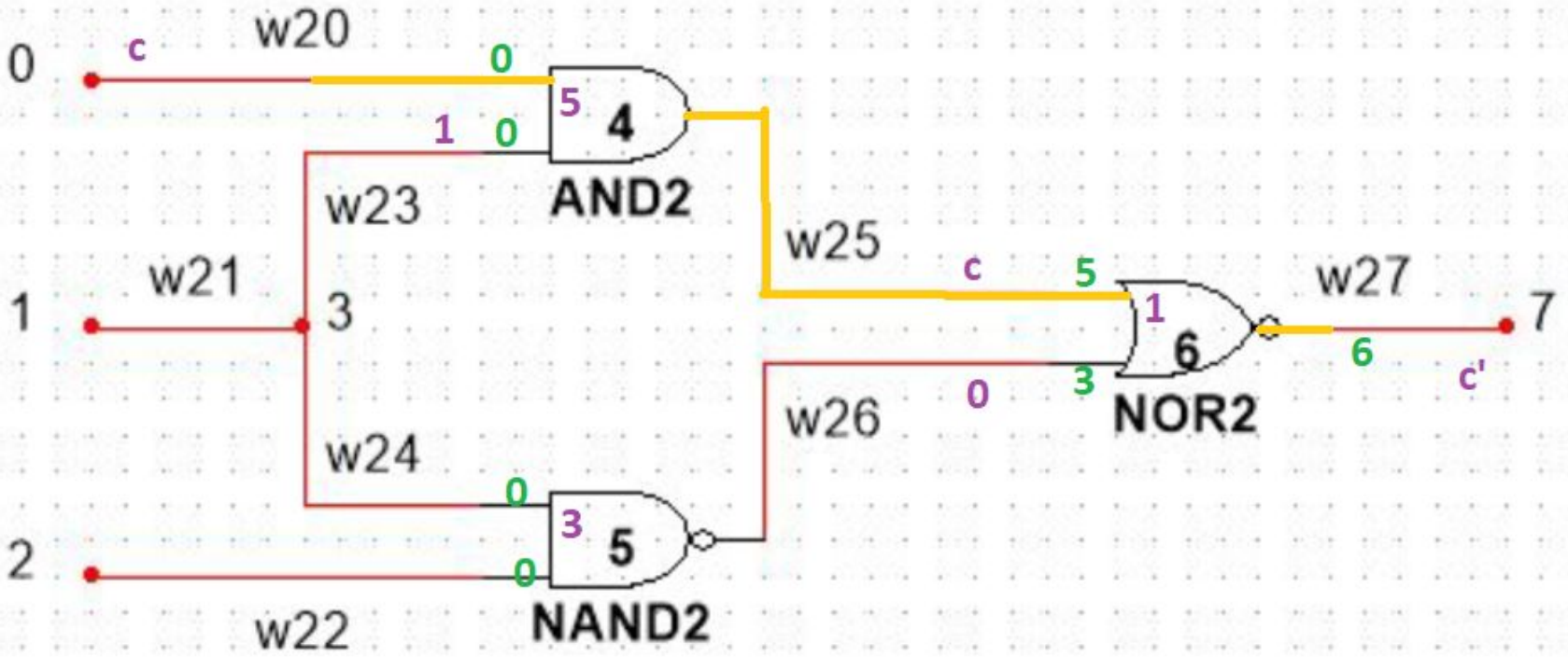
Backtracing



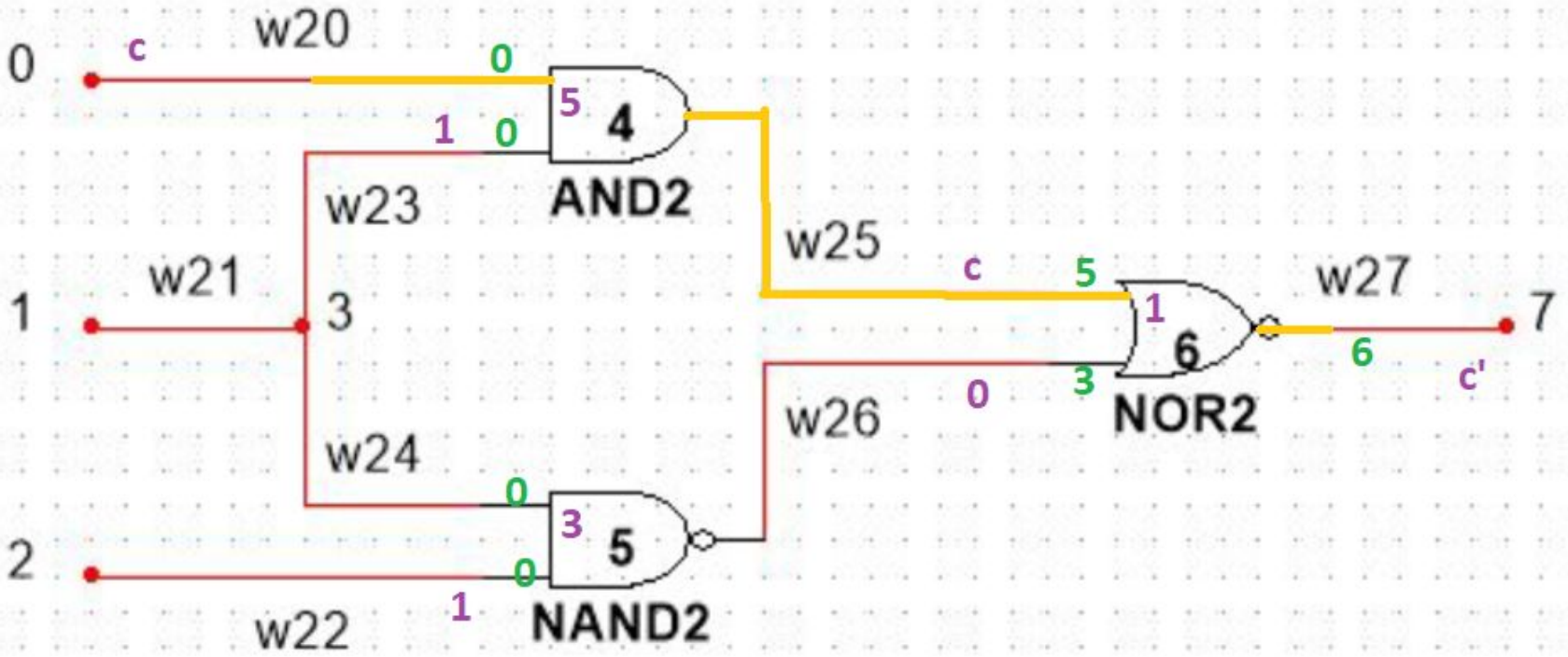
Path Sensitization for path N0 AND2__4 N25 NOR2__6 N27, marked path



Backtrace from PO to PI on path



Backtrace from PO to PI on path



Justify NAND2_5, Implication Occurs, Done