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Test Benches

In VHDL, or any HDL for that matter, testing is almost everything! Your VHDL components have no value unless you can evidence that they perform the desired function.

As a general rule, for each component you develop, there should be at least one test bench.

In this series of articles we look at how we use VHDL test benches to test our components.

Part 1 – Testing a Single Architecture Component < https://blogs.plymouth.ac.uk/embedded-systems/fpga-and-vhdl/test-benches/part-1-single-architecture-test/>

Part 2 – Multiple Architectures < https://blogs.plymouth.ac.uk/embedded-systems/fpga-and-vhdl/test-benches/part-2-multiple-architectures/>

Part 3 – Automatic Testing with Assert < https://blogs.plymouth.ac.uk/embedded-systems/fpga-and-vhdl/test-benches/part-3-automatic-testing-with-assert/>

Part 4 – Testing with Simulated Timing < https://blogs.plymouth.ac.uk/embedded-systems/fpga-and-vhdl/test-benches/part-4-testing-with-simulated-timing/>

Part 5 – Timing Checks < https://blogs.plymouth.ac.uk/embedded-systems/fpga-and-vhdl/test-benches/part-5-timing-checks/>

Part 6 – Modelling and Testing Synchronous Systems < https://blogs.plymouth.ac.uk/embedded-systems/fpga-and-vhdl/test-benches/part-6-modelling-and-testing-synchronous-systems/>

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