Grundy NewBrain Expansion Connector

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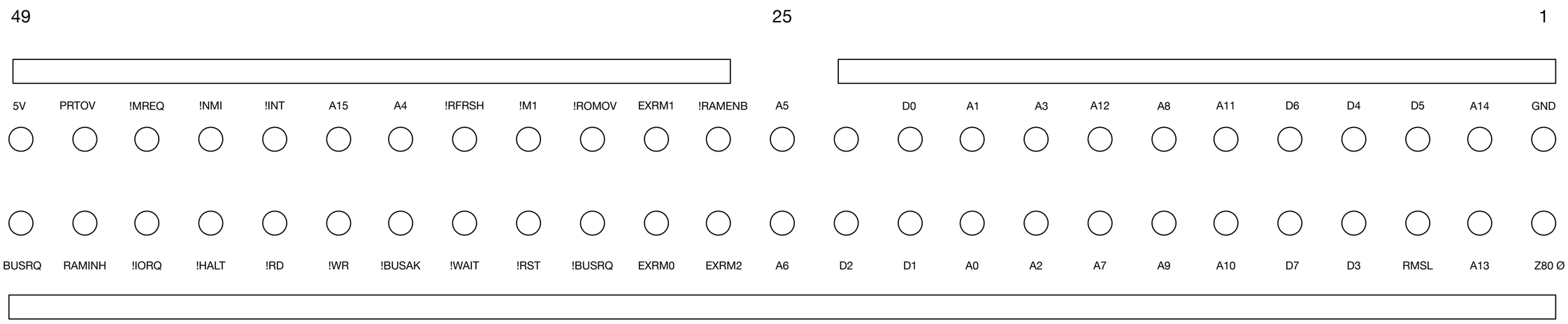

Exp Port	Signal Type	Signal	Description
1		GND	Ground
2	OUT	Ø	1/8C, 4MHz clock
3	TRI	A14	A14 from Z80
4	TRI	A13	A13 from Z80
5	TRI	D5	D5 from Z80
6		RMSL	RAM select, address modifier, unused
7	TRI	D4	D4 from Z80
8	TRI	D3	D3 from Z80
9	TRI	D6	D6 from Z80
10	TRI	D7	D7 from Z80
11	TRI	A11	A11 from Z80
12	TRI	A10	A10 from Z80
13	TRI	A8	A8 from Z80
14	TRI	A9	A9 from Z80
15	TRI	A12	A12 from Z80
16	TRI	A7	A7 from Z80
17	TRI	A3	A3 from Z80
18	TRI	A2	A2 from Z80
19	TRI	A1	A1 from Z80
20	TRI	A0	A0 from Z80
21	TRI	D0	D0 from Z80
22	TRI	D1	D1 from Z80
23			Unused, early machines have a signal connected, connect 10Ω pullup to 5V
24	TRI	D2	D2 from Z80
25	TRI	A5	A5 from Z80

Exp Port	Signal Type	Signal	Description
26	TRI	A6	A6 from Z80
27	IN	!RAMENB	RAM enable, logic 0 routes Z80 memory request to RAM, dependent on pin 48 RAMINH
28	IN	EXRM2	External A15 signal, used by paging circuits in expansion interface
29	IN	EXRM1	External A14 signal, used by paging circuits in expansion interface
30	IN	EXRM0	External A13 signal, used by paging circuits in expansion interface
31	IN	!ROMOV	Address override, logic 0 causes A13/14/15 to be replaced by external A13/14/15
32	OC	!BUSRQ	Bus request as supplied to Z80
33	OUT	!M1	Machine cycle 1 from Z80
34	OUT	!RST	Reset as supplied to Z80
35	OUT	!RFRSH	Refresh from Z80
36	IN	!WAIT	Wait as supplied to Z80
37	TRI	A4	A4 from Z80
38	OUT	!BUSAK	Bus acknowledge from Z80
39	TRI	A15	A15 from Z80
40	TRI	!WR	Write from Z80
41	OC	!INT	Interrupt supplied to Z80
42	TRI	!RD	Read from Z80
43	IN	!NMI	Non-maskable interrupt supplied to Z80
44	OUT	!HALT	Halt from Z80
45	TRI	!MREQ	Memory request from Z80
46	TRI	!IORQ	I/O request from Z80
47	IN	PRTOV	Logic 1 inhibits internal I/O port decode, unconnected state biased to logic 0
48	IN	RAMINH	Logic 1 inhibits Z80 request to internal RAM
49	OUT	+5V	up to 200mA
50	OUT	BUSRQ	Bus request as generated by video circuit