Lecture-14

1. What is partitioning? Why do we need it?
2. What are the different levels of partitioning?
3. How VLSI layout are covert into a graph?
4. What is hypergraph? What is the problem of it in designing algorithms for VLSI design.
5. How can you convert a hypergraph to graph.
6. Consider a hypergraph H, where each hyperedge interconnects at most three vertices. We model each hyperedge of degree-3 with three edges of weight ½, on the same set of vertices, to obtain a weighted graph G. Prove that an optimal balanced partitioning of G corresponds to an optimal balanced partitioning of H.
7. In refer to Question 6, prove that optimal balanced partitioning of G cannot be done if each edge of H interconnects at most four vertices (i.e., give a counter example).
8. Give formal definition of partitioning.

Lecture-15

1. Explain Kernighan-Lin algorithm for partitioning a graph.
2. Consider a path graph $v_1, v_2, \ldots, v_n$. That is, v_1 is connected to v_{i+1}, for $1 \leq i \leq n-1$. Apply the Kernighan-Lin algorithm to this graph. As the initial partition, let v_a, for all odd values of a be in one set , and v_b, for all even values of b, be in the other set.
3. Consider a complete binary tree with n nodes. Apply Kernighan-Lin algorithm to this graph. As the initial partition, let v_a, for all internal vertices, be in one set and v_b, for all leaves, be in the other set.
4. Show how the Kernighan-Lin Heuristic works on the ladder graph with 2n vertices, starting with initial partition of V_1= {1,2,3,……,n}, and V_2={n+1,n+2,n+3,…..,2n}.

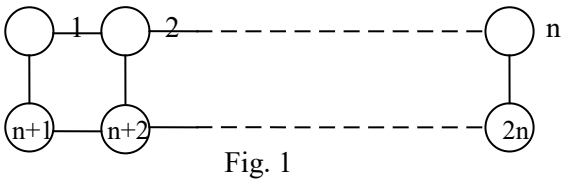

Fig. 1

5. Find the time complexity of Kernighan-Lin algorithm.
6. What are the drawbacks of Kernighan-Lin algorithm?
7. The following matrix provides 4 modules a,b,c,d with their entries representing the number of connections between the two modules. Apply Kernighan-Lin heuristic to obtain the partitioning.

	a	b	c	d
a	0	1	2	3
b	1	0	1	4
c	2	1	0	3
d	3	4	3	0

Fig.2

Lecture-16

1. What are the advantages of Fiduccia-Mattheyses algorithm over Kernighan-Lin algorithm?
2. What are the similarities between Fiduccia-Mattheyses algorithm and Kernighan-Lin algorithm?
3. Present the Fiduccia-Mattheyses Algorithm.
4. Consider a path graph $v_1, v_2, \ldots, v_n$. That is, v_1 is connected to v_{i+1}, for $1 \leq i \leq n-1$. Each Apply the Fiduccia-Mattheyses Algorithm to this graph. Each v_i has the weight i.
5. Apply Fiduccia-Mattheyses Algorithm for the the problem of question 3 of lecture 15 considering weighted vertices.
6. Apply Fiduccia-Mattheyses Algorithm for the the problem of question 4 of lecture 15 considering weighted vertices.
8. Apply Fiduccia-Mattheyses Algorithm for the the problem of question 7 of lecture 15 considering weighted vertices.

Lecture-17

1. Find out the time complexity of Fiduccia-Mattheyses Algorithm.
2. “There is a trade off associated for partitioning with replication.” Is it true or false? Justify.
3. Discuss how Partitioning is affecting overall delay.
4. What do you understand by performance driven partitioning?
5. Discuss the approach of clustering in case of partitioning.

Lecture-18

1. Define Floorplanning. Define sliceable and non-sliceable floorplan with examples. What are the advantages of sliceable floorplan?
2. State with an example how a sliceable floorplan can be represented by a binary tree.
3. Goven a binary tree , how can you obtain the floor plan for it?
4. When an adjacency graph cannot admit a rectangular dual?
5. Obtain the hierarchical floorplan tree for the floorplan given in Fig.1.

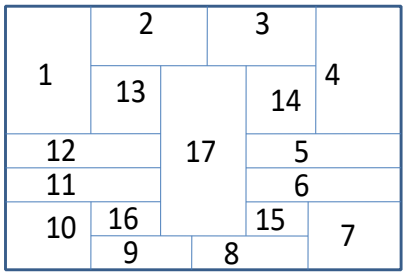

Fig. 1

6. Illustrate the steps of rectangular dualization on an inherently non-sliceable graph of n vertices.
7. Obtain a rectangular dual of the following adjacency graph. Is it sliceable?

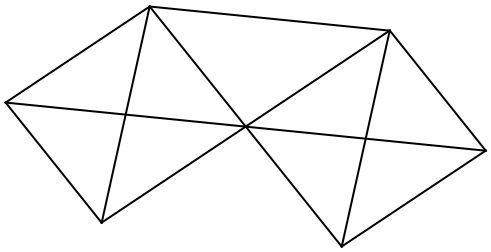

Fig. 2

8. Obtain the rectangular dual of the following adjacency graph below of Fig. 3.
9. What is extended dual.
10. Prove that if the adjacency graph does not contain any complex triangle, then it is possible to obtain a sliceable flooeplan for it.
11. Give the adjacency graph for the floorplan of Fig.1.

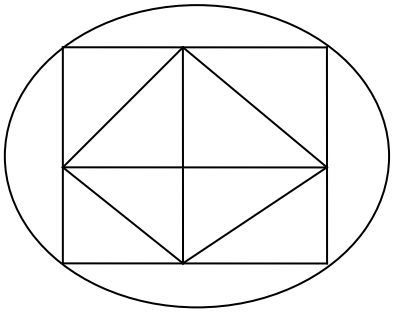

Fig. 3

Lecture-19

1. Explain Bottom-up and Top-down approach in Floorplan.
2. Show with the example that the number of possible sliceable floorplan increases exponentially with the number of modules.

3. What are the different types of internal nodes for a hierarchical floorplan.
4. Explain Hierarchical floorplan with some Greedy procedure for a sliceable floorplan. Explain how the procedure may lead to wastage of space. What is the solution for it?
Prove that there is a one-to-one correspondence between a sliceable floorplan and a normalized Polish expression.
5. State the steps in the Hierarchical floorplan with Bottom up Greedy procedure for the following adjacency graph, where edges have some weights.

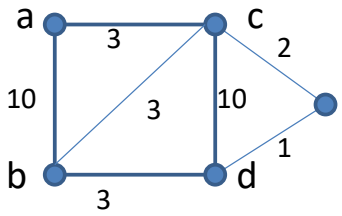

Fig. 1

6.. Explain how the procedure in previous question may lead to wastage of space. What is the solution for it?
7. How do you estimate the cost of floorplan.
8. Consider the following adjacency graph where the edge weights are providing the distance between two vertices. Estimate the routing cost in different sliceable florplans for it.

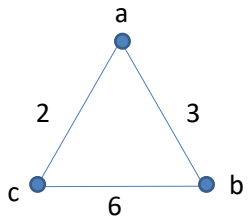

Fig.2

9. Explain Hierarchical top down approach in floorplanning.
10. Prove that there is a one-to-one correspondence between a sliceable floorplan and a normalized Polish expression.
11. What is simulated annealing?
12. How simulated annealing approach can be applied in Floorplanning of VLSI design.
13. State the three different operations in simulated annealing approach in Floorplanning. How they will be applied in a given floorplan.
14. Given a Polish expression corresponding to a given slicing floorplan. Show that the expression 12+3+4+……. +n+ can be reached, and vice versa, using three operations in simulated annealing approach of floorplan. (+ and * represent horizontal and vertical bisection respectively.)

Lecture-20

1. State Floorplan sizing problem.
2. Considering hierarchical nature of floorplan, discuss how to deal with the sizing problem.
3. In a hierarchical florrplan sizing problem, there are given two subfloorplans corresponding to two subtrees of a node v, one with t and other with s nonredundant implementations, prove that v has at most s+t-1 nonredundant realizations.
4. Given a fllorplan with fixed cell environment, what are the significance of horizontal dependency graph and vertical dependency graph.
5. Draw the horizontal and vertical dependency graph of the floorplan given in Fig. 1 of Lecture 19.
6. State an algorithm for hierarchical floorplan sizing problem. What is its time complexity?
7. Considering no restriction on the organization of the modules, formulate the floorplan sizing problem as an Integer Linear Programming (ILP).
8. What are the advantages of integer linear programming technique in case in floorplanning.

Lecture-21

1. State the consequences of placement in VLSI Design.
2. What are the consequences of placement problem?
3. State the importance of Placement problem.
3. How do we estimate the wirelength in the placement? Explain.

4. Show with an example that the placement of logic blocks in different ways may affect the wirelength.
5. Show with an example that the placement of logic blocks in different ways may affect the routability.
6. What are constrained and unconstrained placement?
7. Give a brief discussion on the objective functions and routing estimation in placement.
8. Formulate the placement problem.
9. Discuss the cost components in Placement.
10. What are global and detailed placement?
11. What are user constraints in placement problem?
12. State the various approaches for placement problem- Top-down, iterative, constructive?
13. Explain the Force directed Placement algorithm.
14. Compare the constructive and iterative algorithm in Placement problem.
15. State two different approaches in Force directed algorithm.
16. What are pros and cons of Force directed algorithm?

Lecture-22

1. Explain congestion problem in time of placement.
2. State partitioning technique in placement approach with goal and objectives.
3. Explain the different procedures for Breuer's Algorithm.
4. What are pros and cons of Breuer's algorithm?
5. Explain simulated annealing algorithm in case of placement problem.
6. Explain the quadratic placement approach.
7. What is analytical placement? What is the advantage of doing this type of placement?
8. State the pros and cons of quadratic placement approach.
9. State the clustering approach in case of placement.