VLSI
Assignment 3 Annexure

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1 Describtion

- Design a 4x16 decoder by only behavioral modelling
  - by using function of 2x4 decoders only
  - by using procedures of 2x4 decoders only

2 Block Diagram

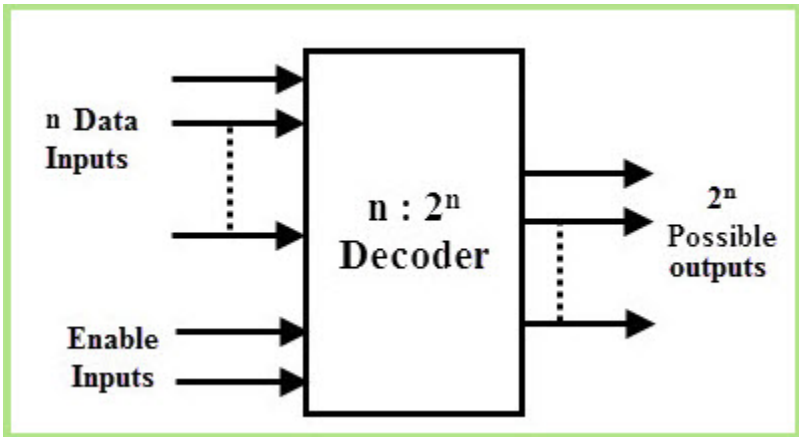

Figure 1: Decoder block diagram

3 Truth Table

X(3 - 0)	Y(15 - 0)
0000	0000000000000001
0001	0000000000000010
0010	0000000000000100
0011	0000000000001000
0100	0000000000010000
0101	0000000000100000
0110	0000000001000000
0111	0000000010000000
1000	0000000100000000
1001	0000001000000000
1010	0000010000000000
1011	0000100000000000
1100	0001000000000000
1101	0010000000000000
1110	0100000000000000
1111	1000000000000000

4 Circuit Diagram

5 Code

5.1 Using function of 2x4 decoders only

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity ass3_annex2a is
    Port ( X : in  STD_LOGIC_VECTOR (3 downto 0);
```

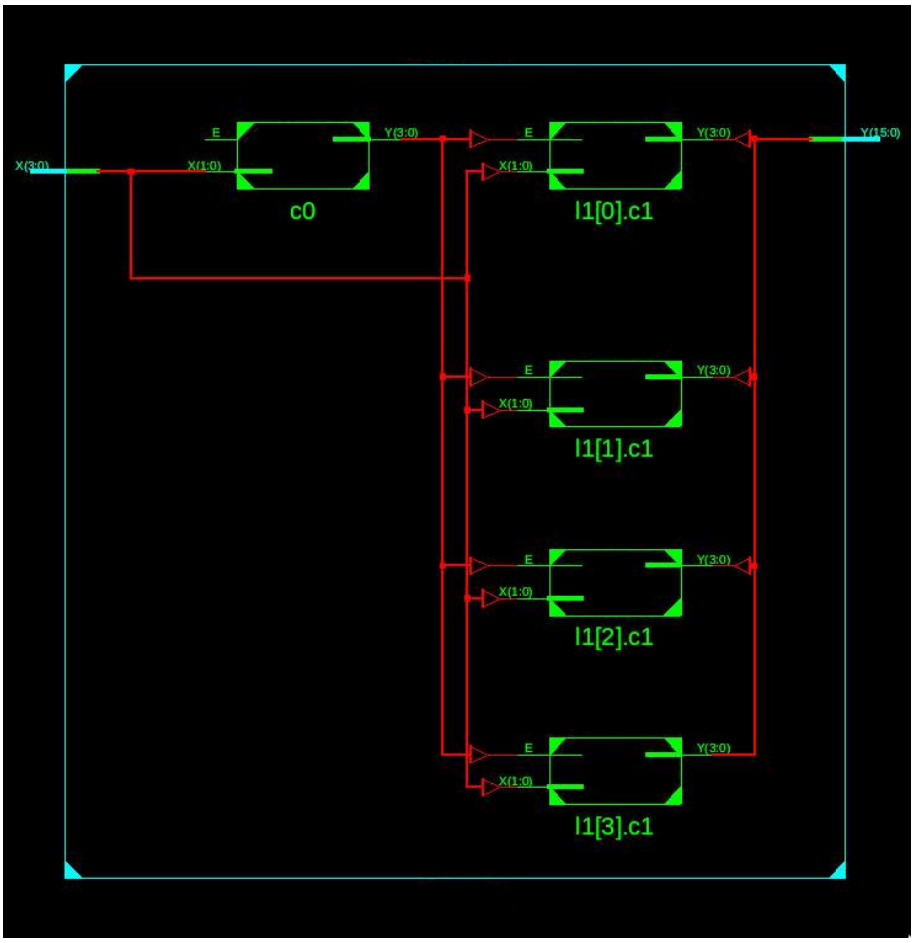

Figure 2: 4x16 circuit diagram

```
        Y : out  STD_LOGIC_VECTOR (15 downto 0));
end ass3_annex2a;

architecture Behavioral of ass3_annex2a is
        function demux2x4(x: in std_logic_vector) return std_logic_vector is
        variable a: std_logic_vector(3 downto 0);
        begin
                if x = "00" then
                        a := "0001";
                elsif x = "01" then
                        a := "0010";
                elsif x = "10" then
                        a := "0100";
                elsif x = "11" then
                        a := "1000";
                else
                        a := "ZZZZ";
                end if;
        return a;
        end function;

begin
        p1: process(X)
        variable a: std_logic_vector(3 downto 0);
        variable b: std_logic_vector(3 downto 0);
        begin
                a := demux2x4(X(3 downto 2));
```

```
                b := demux2x4(X(1 downto 0));
                for k in 0 to 3 loop
                        if a(k) = '1' then
                                Y(4*k+3 downto 4*k) <= b;
                        else
                                Y(4*k+3 downto 4*k) <= "0000";
                        end if;
                end loop;
        end process;
end Behavioral;
```

5.2 Using procedures of 2x4 decoders only

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity ass3_annex2b is
    Port ( X : in  STD_LOGIC_VECTOR (3 downto 0);
           Y : out  STD_LOGIC_VECTOR (15 downto 0));
end ass3_annex2b;

architecture Behavioral of ass3_annex2b is
        procedure demux2x4(x: in std_logic_vector; y: out std_logic_vector) is
        variable a: std_logic_vector(3 downto 0);
        begin
                if x = "00" then
                        y := "0001";
                elsif x = "01" then
                        y := "0010";
                elsif x = "10" then
                        y := "0100";
                elsif x = "11" then
                        y := "1000";
                else
                        y := "ZZZZ";
                end if;
        end procedure;
begin
        p1: process(X)
        variable a: std_logic_vector(3 downto 0);
        variable b: std_logic_vector(3 downto 0);
        begin
                proc1: demux2x4(X(3 downto 2), a);
                proc2: demux2x4(X(1 downto 0), b);
                for k in 0 to 3 loop
                        if a(k) = '1' then
                                Y(4*k+3 downto 4*k) <= b;
                        else
                                Y(4*k+3 downto 4*k) <= "0000";
                        end if;
                end loop;
        end process;

end Behavioral;
```

6 Test Bench

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
```

```
ENTITY tb_a3_ax1 IS
END tb_a3_ax1;

ARCHITECTURE behavior OF tb_a3_ax1 IS

    -- Component Declaration for the Unit Under Test (UUT)

    COMPONENT a3_ax1
    PORT(
         X : IN  std_logic_vector(3 downto 0);
         Y : OUT  std_logic_vector(15 downto 0)
        );
    END COMPONENT;


   --Inputs
   signal X : std_logic_vector(3 downto 0) := (others => '0');

         --Outputs
   signal Y : std_logic_vector(15 downto 0);
   -- No clocks detected in port list. Replace <clock> below with
   -- appropriate port name

BEGIN

         -- Instantiate the Unit Under Test (UUT)
   uut: a3_ax1 PORT MAP (
          X => X,
          Y => Y
        );


   -- Stimulus process
   stim_proc: process
   begin

                                X <= "0000";
                wait for 1 ps;
                X <= "0001";
                wait for 1 ps;
                X <= "0010";
                wait for 1 ps;
                X <= "0011";
                wait for 1 ps;
                X <= "0100";
                wait for 1 ps;
                X <= "0101";
                wait for 1 ps;
                X <= "0110";
                wait for 1 ps;
                X <= "0111";
                wait for 1 ps;

                X <= "1000";
                wait for 1 ps;
                X <= "1001";
                wait for 1 ps;
                X <= "1010";
                wait for 1 ps;
```

```
                X <= "1011";
                wait for 1 ps;
                X <= "1100";
                wait for 1 ps;
                X <= "1101";
                wait for 1 ps;
                X <= "1110";
                wait for 1 ps;
                X <= "1111";
                wait for 1 ps;

    end process;

END;
```

7 Timing diagram