Ref. No.: EX/IEBT/ET/T/122/2018

B. TECH. INSTRUMENTATION AND ELECTRONICS ENGINEERING
FIRST YEAR SECOND SEMESTER - 2018

Subject: ELECTRONIC CIRCUITS-I **Time: Three Hours** **Full Marks: 100**

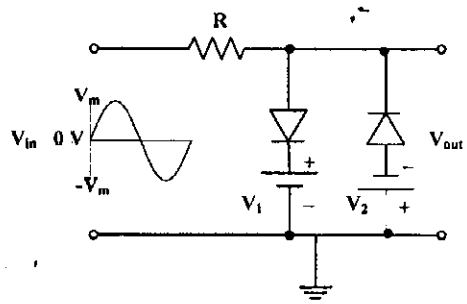
Answer any **FIVE** questions. 5x20

(Questions must be answered serially and
All parts of the same question must be answered at one place only)

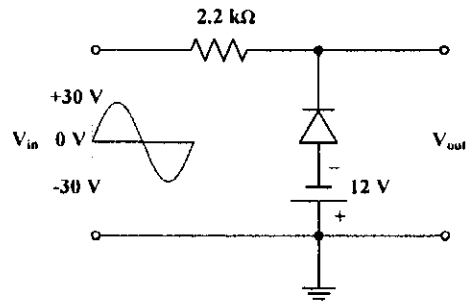
1. (a) Define the performance parameters of a filter circuit. Derive their expressions. Evaluate them for half wave and full wave rectifiers and compare.
(b) What does the regulation characteristic curve of a filter circuit tell us? What is the fundamental source of its non-zero resistance?
(c) Prove that the maximum dc output power occurs in a half-wave rectifier when the load resistance is equal to the diode resistance. (3+4+6)+3+4=20

2. (a) Explain the performance of an inductor filter when applied to a full-wave rectifier circuit. Derive the expression for the corresponding ripple factor. Qualitatively compare it with the ripple factor for a capacitor filter.
(b) Derive and compare the ripple factors of a capacitor filter when connected across a half-wave and a full-wave rectifier circuit. The component values are assumed to be same.
(c) The output voltage across a load resistance $R_L = 100\Omega$ of a capacitor filter with $C = 1100\mu F$ connected to a full-wave rectifier supplied with a line frequency of 50 Hz has a dc value of 9 V and a peak-to-peak ripple voltage of 0.8 V. Calculate the ripple factor from the voltage values, and compare it with the theoretical value expected from the filter components. (5+3)+6+6=20

3. (a) What are series and parallel clipper circuits?
(b) Sketch and describe the output waveforms for the following circuits. In (i), we can assume, $V_m > |V_1| > |V_2|$.

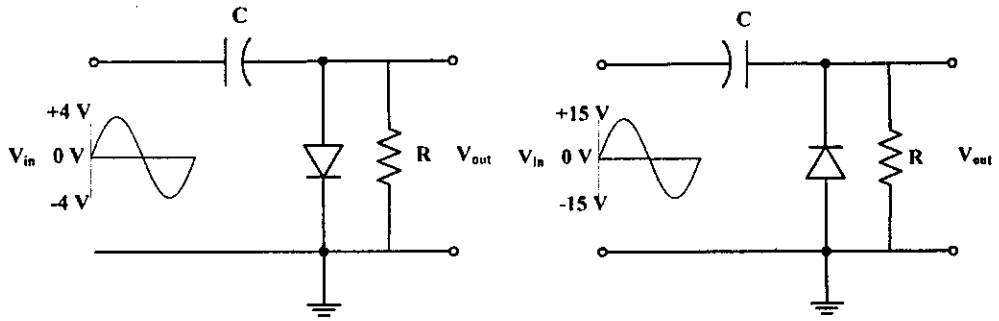


(i)



(ii)

(c) Sketch and describe the output waveforms for the following circuits. Assume that the RC time constant is much greater than the period of the input.



(i) (ii)

(d) Define critical inductance and bleeder resistance with reference to an LC filter circuit.

4+6+6+4=20

4. (a) State and prove Miller's theorem.
(b) Explain self-biasing arrangement for a BJT. Why is it so named? Derive the stability factors.
(c) A Ge transistor with $\beta = 49$ has a self-biasing arrangement in CE configuration. The supply voltage is 10 V, the load resistance is $1k\Omega$, $V_{CE} = 5V$, $I_C = 4.9mA$ and $V_{BE} = 0.2V$. The stability factor S is desired to be 10. Obtain the values of R_1, R_2 and R_e. (2+2)+(3+1+3x2)+6=20

5. (a) A CE transistor amplifier is characterized by $h_{ie} = 2k\Omega, h_{re} = 2\times10^{-4}, h_{fe} = 50$ and $h_{re} = 20\times10^{-6} A/V$. If the load resistance is $4k\Omega$ and the source resistance is 200Ω, determine the input resistance, the output resistance and the voltage, current and power gains. Derive the formula you use.
(b) Explain the working principle of a Darlington pair. Quantitatively show the improvements of input and output resistances. 15+5=20

6. (a) From the gain analysis of an RC coupled CE amplifier, define lower and upper-off frequencies.
(b) If the lower and upper half-power frequencies of an RC-coupled amplifier are 30 Hz and 300 kHz, respectively, find the gain relative to the mid frequency gain at 60 Hz and 600 kHz. Find both magnitude and phase.
(c) Analyze the phase response curve of a two-stage RC coupled amplifier circuit.
(d) Explain the working principle of an emitter follower circuit. 4+6+6+4=20

7. (a) Define FET parameters μ, r_d and g_m. How are they related? Derive and draw the small signal a.c. equivalent circuit of a FET.
(b) Derive the expression for voltage gain of a common-source FET amplifier.
(c) A FET amplifier in the common-source configuration uses a load resistance of 250 kΩ. The a.c. drain resistance of the device is 100 kΩ and the trans-conductance is 0.5 mA/V. What is the voltage gain of the amplifier?
(d) Derive the relation between trans-conductance and gate shorted trans-conductance of a JFET.

(3x1+2+3+1)+4+4+3=20

8. (a) A certain differential amplifier has a differential voltage gain of 2000 and a common-mode gain of 0.2. Determine the CMRR and express it in decibels.
(b) Derive and draw the trans-conductance curve of a CMOS differential amplifier. Clearly mention the assumptions.
(c) Derive the expressions for the differential and common-mode voltage gains using small signal ac analysis of a single ended output CMOS differential amplifier and hence find the CMRR. Extend the expressions for differential output. 2+6+(10+2)=20