Ex/CSE/T/214/18/2011

BACHELOR OF COMPUTER Sc. & ENGG. EXAMINATION, 2011

(2nd Year, 1st Semester)

DIGITAL CIRCUITS

Time : Three hours Full Marks :100

Answer any ***five*** questions

1. a) With the help of a circuit diagram explain the operations of a DTL gate. 12

   b) Draw the transfer characteristics of the same at 25^0C. 4

   c) Estimate the steady state power dissipation at no load, assuming power supply voltage of 5V. 4

2. a) Explain the operations of a standard TTL gate. 8

   b) What are the modifications required for wired–OR Connection? 4

   c) An wired -OR circuit has fan-in and fan-out of 3 and 4 respectively. Estimate the value of the pull-up resistor with the following parameters : V_{OHmin} = 2.4V; V_{OLmax} = 0.4; I_{IH} = 40 μ A; I_{OHmax} = 250 μ A; I_{ILmax} = 1.6mA and I_{OLmax} = 16mA. 8

[Turn Over]

3. a) sExplain the operations of an nMOS inverter. 8

   b) Estimate the voltage rise time of an nMOS inverter interms of its circuit Parameters. 8

   c) Calculate t_r when C_L = 6pf; K_L = 16 m A/ V^2 and V_f = 12V. 4

4. a) Explain the operations of a clock generator using an 555 IC timer. 8

   b) Deduce the Expressions for the frequency and duty cycle. 6+2

   c) Design a clock working at 1KHz with 30% duty cycle using a.01 m f capacitor. 4

5. a) With the help of a circuit diagram explain the operations of a static MOS memory cell. 12

   b) How can the stored information be retained even when the power supply is switched off? 8

6. a) Explain the operation of a R-2R Ladder type DAC. 12

   b) What are the basic differences in the working principles of weighted resistor type DAC's with that of R-2R Ladder type DAC's? 4

   c) What are their relative merits and demerits? 4

7. a) Explain the operation of a Successive Aproximation type ADC. 12

   b) What are its relative merits and demerits? 2

   c) Explain the functions of the interfacing signals associated with same. 6

8. Write notes on any ***four*** of the following : 5x4

   a) Current hogging in DCTL;

   b) RTL NOR gates;

   c) ECL;

   d) Realise $X = \overline{A.B. + (C+D).E}$ using a single nMOS gate;

   e) EAPROM's;

   f) Frequency Multiplications;

   g) Sample & Hold circuits;

   h) Analog Multiplexers.

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