Ref. No.: Ex/MECE 617/2018

Department of Electronics and Telecommunication Engineering, Jadavpur University
M.Tech in VLSI Design and Microelectronics Technology 1st year 2nd Semester Examination 2018.
Attempt any five questions and all question carry equal mark. The figures in the right hand margin indicate marks. *Symbols carry usual meaning.*

Time: Three hours **Subject: Advanced Digital IC Design** **Full Marks: 100**

Q1(a). Why low power has become an important issue in the presentday VLSI circuit realization? What is the threshold voltage of a MOS transistor? How it varies with the body bias? What is body effect?
Q1(b). What is channel length modulation effect? How the voltage current characteristics are affected because of this effect?
Q1(c).What is noise margin? Find out the noise margin from the actual characteristics of an inverter. 9+5+6=20

Q2(a). What effect has velocity saturation in the drain current?
Q2(b). Distinguish between constant field and constant voltage feature size scaling? Compare their advantages and disadvantages.
Q2(c). As you move to a new process technology with a scaling factor S = 1.4, how the drain current, power density, delay and energy requirement changes for the constant field scaling? 3+ 7+10 = 20

Q3(a). How one nMOS and one pMOS transistor are combined to behave like an ideal switch?
Q3(b) Why leakage power is an important in the deep sub micron technology?
Q3(c). List various sources of leakage currents.
Q3(d). Briefly discuss various mechanisms responsible for this leakage current? 4+4 +4 + 8 = 20

Q4(a). What is glitching power dissipation? Explain how can it be minimized?
Q4(b). With the help of an example explain how gray coding helps to reduce power dissipation?
Q4(c). Explain how the ordering of input signal does affect the dynamic power dissipation.
Q4(d). Prove that the charging of a capacitor C in *n* steps to a voltage Vdd instead of a conventional single-step charging reduces the power dissipation by a factor of *n*. 6+6+ 4+ 4=20

Q5.(a). Define the symmetric and asymmetric logic gates with an example for each. Explain why the input ordering of a logic gate may affect propagation delays.
Q5(b). Using equivalent NOT gate, drive the threshold voltage of an n-input NAND gate.
Q5(c). Describe single-rail and dual –rail logic circuits 8+8+4 = 20

Q6(a). How is a CMOS inverter different from a resistive load inverter? Which is preferred and why?
Q6(b). For inverter design, why depletion load n-MOS inverter is preferred?
Q6(c). What is pass transistor? Write its advantages and disadvantages. Realize a NAND and a XOR Gates using Pass transistors and explain their operation. 4+ 2 + 14 = 20

Q7(a).What are high and low –skewed logic gates? Explain GDI logic with an example.
Q7(b). Implement two-input (i) XOR and (ii) NOR gates with GDI logic. Explain their operations.
Q7(c). Explain pseudo and Ganged CMOS logic with an example for each. 6+ 8 + 6 =20

Q8 Write notes on any four **5x4 = 20**
(a)Short channel effects (b) limitation of contemporary CAD tools (c) an area optimized transmission Gate based full adder (d) Fan- in and Fan- out of Logic Gates. (e) Non-threshold Logic (f) pipelining and parallelism in Low power VLSI Design