VLSI
Assignment 3 Annexure

Priyank Lohariwal
BCSE IV
Roll-001710501055

1 Describtion

- Design a 4x16 decoder using 2x4 decoders with generate statement. Write test bench using behavioural modelling

2 Block Diagram

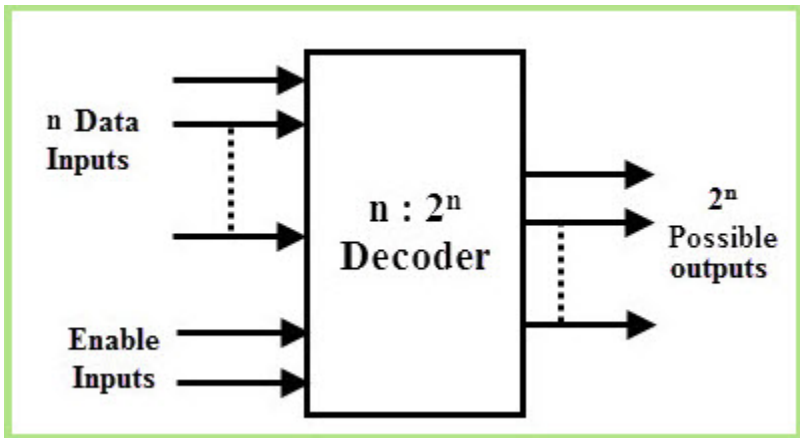

Figure 1: Decoder block diagram

3 Truth Table

X(3 - 0)	Y(15 - 0)
0000	0000000000000001
0001	0000000000000010
0010	0000000000000100
0011	0000000000001000
0100	0000000000010000
0101	0000000000100000
0110	0000000001000000
0111	0000000010000000
1000	0000000100000000
1001	0000001000000000
1010	0000010000000000
1011	0000100000000000
1100	0001000000000000
1101	0010000000000000
1110	0100000000000000
1111	1000000000000000

4 Circuit Diagram

5 Code

5.1 Using 2x4 decoders with generate statement

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity a3_ax1 is
    Port ( X : in  STD_LOGIC_VECTOR (3 downto 0);
           Y : out  STD_LOGIC_VECTOR (15 downto 0));
end a3_ax1;
```

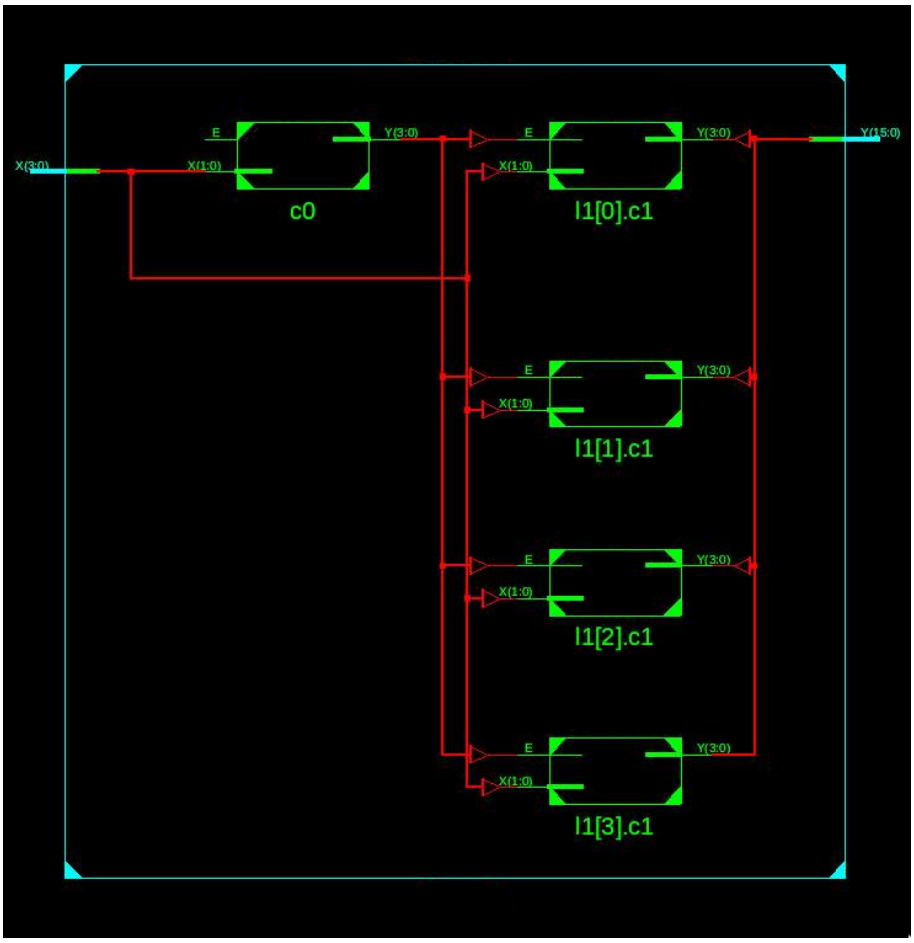

Figure 2: 4x16 circuit diagram

```
architecture Behavioral of a3_ax1 is

component a3_2_1a is
    Port ( X : in  STD_LOGIC_VECTOR (1 downto 0);
                   E : in STD_LOGIC;
           Y : out  STD_LOGIC_VECTOR (3 downto 0));
end component;

signal e1: std_logic_vector(3 downto 0);

begin

                c0 : a3_2_1a port map(X(3 downto 2), '1', e1);
                l1: for i in 0 to 3 generate
                        c1 : a3_2_1a port map(X(1 downto 0), e1(i), Y(4*i+3 downto 4*i));
                end generate;

end Behavioral;
```

6 Test Bench

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;


ENTITY tb_a3_ax1 IS
```

```
END tb_a3_ax1;

ARCHITECTURE behavior OF tb_a3_ax1 IS

    -- Component Declaration for the Unit Under Test (UUT)

    COMPONENT a3_ax1
    PORT(
         X : IN  std_logic_vector(3 downto 0);
         Y : OUT  std_logic_vector(15 downto 0)
        );
    END COMPONENT;


   --Inputs
   signal X : std_logic_vector(3 downto 0) := (others => '0');

         --Outputs
   signal Y : std_logic_vector(15 downto 0);
   -- No clocks detected in port list. Replace <clock> below with
   -- appropriate port name

BEGIN

         -- Instantiate the Unit Under Test (UUT)
   uut: a3_ax1 PORT MAP (
          X => X,
          Y => Y
        );


   -- Stimulus process
   stim_proc: process
   begin

                                X <= "0000";
                wait for 1 ps;
                X <= "0001";
                wait for 1 ps;
                X <= "0010";
                wait for 1 ps;
                X <= "0011";
                wait for 1 ps;
                X <= "0100";
                wait for 1 ps;
                X <= "0101";
                wait for 1 ps;
                X <= "0110";
                wait for 1 ps;
                X <= "0111";
                wait for 1 ps;

                X <= "1000";
                wait for 1 ps;
                X <= "1001";
                wait for 1 ps;
                X <= "1010";
                wait for 1 ps;
                X <= "1011";
                wait for 1 ps;
```

```
                X <= "1100";
                wait for 1 ps;
                X <= "1101";
                wait for 1 ps;
                X <= "1110";
                wait for 1 ps;
                X <= "1111";
                wait for 1 ps;

   end process;

END;
```

7 Timing diagram