M.Tech. VLSI DESIGN AND MICROELECTRONICS

FIRST YEAR 2nd SEM EXAM- 2018

Low Power VLSI Design

(Paper Code MECE-634)

Time: Three hours | Full Marks: 100

(50 marks for each Part)

Use a separate Answer Script for each Part

PART-I

Answer any five questions [5x10=50]

1. Why Leakage power is so important in VLSI circuit realization? Write the advantages & disadvantages of CMOS in VLSI circuit designing approach. [4+6=10]
2. (a) Proof that the power dissipation of a CMOS is proportional to the supply voltage and frequency? Discuss about the propagation delay of CMOS inverter.
   (b) Discuss about the Power versus Energy. [(4+4)+(2)=10]
3. (a) Explain the Glitching Power Dissipation in a logic circuit and how it can be minimized.
   (b) Design a NAND Gate using CMOS inverter and realize the same. Draw the circuits with CMOS inverter of the expression $Y=\overline{AB+C}$ [4+(3+3)=10]
4. (a) Explain the Short Circuit Current in CMOS Inverter with necessary sketch.
   (b). A 64 bit off Chip Bus operating at 6V and 66MHz clock rate is driving a capacitance of 20 pF/bit. Each bit is estimated to have a toggling probability of 0.20 at each clock cycle. What is the Power dissipation in operating the bus? [5+5=10]
5. (a) Derive the Logic Threshold Voltage of CMOS Inverter and the desirable noise margin.
   (b) One 3 watt electronic gadget with 7.8wh battery capacity is designed. How much times the device can run? If 85mW and 300 mW required for music and slide show respectively, then how much times the system can run for music and slides. [5+5=10]
6. (a) Describe the fabrication process of CMOS inverter circuit.
   (b) Compare the toggles of Binary and Gray code counter and which one is more preferable for low power VLSI circuit. [7+3=10]
7. Write a short note on any of two: [5x2=10]
   (a). Latch up in C-MOS (b). DIBLE Effect (c). Switching activity of Static CMOS gates (d). Sub threshold leakage current.

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PART-II

(Use separate answer scripts for each part)

Answer any five questions. Each question carries equal marks. Answers must be brief and to the point. Answer to one question should be at one place.

1. What is meant by process technology? Describe the different types of process technology. 2+8=10
2. Describe in brief the working principle of the multi-threshold CMOS circuit. What is CMOS technology? 7+3=10
3. Derive the expression of the dissipated energy for the adiabatic switching. Find out the value of load capacitance (C_L) of the CMOS inverter. Plot the delay versus load capacitance for conventional CMOS and BiCMOS buffers. 5+3+2=10
4. What is P-well process technology? Discuss in brief the N-well process technology and P-well process technology. 2+8=10
5. What is meant by BiCMOS technology? Describe in brief the working principle of a typical BiCMOS inverter circuit. 2+8=10
6. State the advantages of BiCMOS technology over CMOS technology. Explain the principle of operation of the BiCMOS NAND gate. 3+7=10
7. Consider a logic gate for the Boolean function $Z=\overline{(ABD + CEF)}$. Design a BiCMOS circuit to implement the Boolean function Z. 10