Ex./PE/T/424A/2018

Jadavpur University
B.Power Engg. 4th Year 2nd Semester Examination 2018
Elective II (Microcomputers and Digital Systems)

Time: 3hours **Full Marks : 100**

Answer any Five

1. Represent the Timing Diagram for a memory read in a 8086 based system with 0 wait states. If the memory has a latency of 600 ns. calculate the number of wait-states that need to inserted in your Timing Diagram and re-draw the same with the wait-states inserted. 10+10

2. The data segment for a code on a 8086/8088 based system is initialized to 0x7200. The data consists of 64 double words (16 bits) starting with an offset 0x0001. Calculate the number of memory reads (RD cycles) required to read the data. Now assuming that the computation results are stored in 8 double words, calculate the physical address of the last word. 5+5

   Enumerate the different segment registers in a 8086 micro-processor and state their use. 10

3. Distinguish between memory mapped and I/O mapped I/O. With a neat schematic represent the general interaction between the processor memory and I/O ports through a Data bus, Control Bus and an Address Bus. What do you mean by Programmed I/O, Interrupt I/O and Block Transfers. 6+8+6
4. Define the terms *bus cycle* and *cycle stealing* . Enumerate the sequence involved in transferring a single byte from the peripheral to the memory using DMA. Explain the sequence with a neat schematic. 6+6+8
5. Draw the block diagram of a 8255. Enumerate its modes of operation
   Representing the Control Word Register for a 8255 compute the control word to initialize the 5255 in active mode, Mode 0 for Group A and Group B with port A as input and ports B and C as outputs. 6+4+10

6. Calculate the time taken to transmit 2KB of data over an asynchronous serial link using 8 bit , no parity, 2 stop bits format for a transmission speed of 19.2kbps. What will be the worst case transmission time for the same data if synchronous communication is used with the same communication speed with NRZ coding. Represent the bit sequence 11001011 in Manchester coded form. 7+7+6
7. Enumerate the interrupt sequence in a 8086 micro-processor.
   If the interrupt table starts at the physical memory location 0x00010 where would you place the [CS,IP] for the Interrupt Service Routine associated with IRQ5?
   With a neat schematic represent the timing diagram for identification of the IRQ type with a 8259 for a 8086 microprocessor. 4+6+10
8. With a neat schematic represent the Timing Diagram of an ADC 0808.
   Write a small assembly level program to read an analog input from IP_2 of an ADC through Port A and the upper 4 bits of the Port C to receive the EOC signal and the lower 4 bits of port C to send the SOC signal to the ADC. 8+12