Ex./MECE 619/2018

M.TECH. VLSI AND MICRO ELECTRONICS SECOND YEAR SECOND SEMESTER-2018

VLSI ARCHITECTURE AND SYSTEM DESIGN

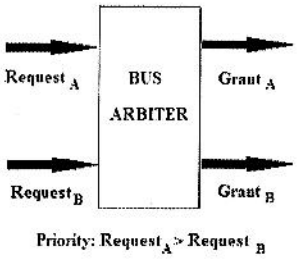
Time : 1 hr 30 mins **PART - I** Full Marks : 50

(Use Separate Answer scripts for each part)
Answer any five questions.

1. Compare PLA and PAL architecture. Implement the following Input functions using PLA based architecture.
   $F_1 = x`+z+y`z$; $F_2 = y`+x`z+ z$; $F_3 = x`+x`z$ 4+6

2. Design a pattern identifier (1 input-1 output) which can identify a bit pattern 1001 (considering non overlapping pattern) from a bit streams using state graph and show corresponding implementation in MUX based and PAL based architecture. 10

3. Explain VLSI system Design using Algorithmic State Machine chart. Design a ASM chart for priority based Bus Arbiter given below.



Priority: Request $_A$ > Request $_B$

4+6

4. What is a FPGA slice? What is LUT based logic realization? How to get a 6-input LUT from 2-input LUT on a Virtex CLB? 3+2+5

5. What is the role of verification in VLSI design? Explain Xilinx FPGA design development flow.
   3+7

6. State different technologies of programmable logic switches in FPGA and explain their operational principles. Compare Full custom ASIC and Semi-custom ASIC with examples? 7+3

7. Explain the methods to optimize the FPGA resource usage? Define FPGA placement and routing problem and describe optimization solution. 4+6

[Turn over

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VLSI ARCHITECTURE AND SYSTEM DESIGN

Time : 1 hr 30 mins **PART - II** Full Marks : 50

(Use Separate Answer scripts for each part)
Answer any five questions.

1. a. Compare RISC and CISC Architectures.
   b. State any two different performance parameters of a computing system.
   c. State Amdahl's law. Give the expression of speed up. 3+3+4

2. a. The performance of a processor and for web serving has to be enhanced. The new processor is 10 times faster in computation than the original processor. Assuming that the original processor is busy with computing 40% of the time & is waiting for I/O for 60% of the time. Define fractional enhancement. What is the overall speed up gained by incorporating the enhancement?
   b. Explain the key parameters which determines the throughput of a processor in terms of instruction execution. 6+4

3. Explain the full Data Path of Single Cycle MIPS Processor with proper illustration. 10

4. Discuss the concept of Pipelining. Derive the expression for maximum speed up in case of pipelining. State any one limitation of pipelined architecture. 5+4+1

5. a. What do you mean by Data Hazards in Pipeline?
   b. Resolve a RAW Data Hazard by: (i.) Code Reordering (ii.) Register Renaming. (iii.) Hardware Technique. 4+6

6. a. Describe with suitable examples the occurrence of Control Hazard in 32 bit MIPS processor.
   b. State any one technique of handling Control Hazard. 5+5

7. Write short notes on (any two) 5+5
   i. Non-Linear Pipeline
   ii. Structural Hazards in Pipeline
   iii. 32 bit MIPS Instruction Set.