

RESISTOR-TRANSISTOR LOGIC (RTL) AND INTEGRATED-INJECTION LOGIC (IIL)

We begin our discussion of logic gates (Chaps. 4 to 8) by considering the *resistor-transistor-logic* (RTL) gate. This type of gate is no longer used in new design, but for a number of reasons the RTL gate is a useful starting point. On the one hand, this gate is elegantly simple and hence may be used conveniently to develop concepts useful in connection with all types of gates. Further, the RTL gate is historically the first gate to have been used extensively, and many installations employing this type of gate are still in operation. Finally, topologically at least, RTL is a forerunner of *integrated-injection-logic* (IIL) which, at the present writing, is one of the newest of the commercially available LSI logic families.

4.1 THE RESISTOR-TRANSISTOR-LOGIC (RTL) GATE

An N -input RTL gate (Fig. 4.1-1) consists of N transistors all of whose emitters are connected to a common ground and all of whose collectors are tied through a common collector resistor R_c to a supply voltage V_{cc} . Input voltages V_i , ($i = 1, 2, \dots, N$) representing logic levels, are applied to the bases through

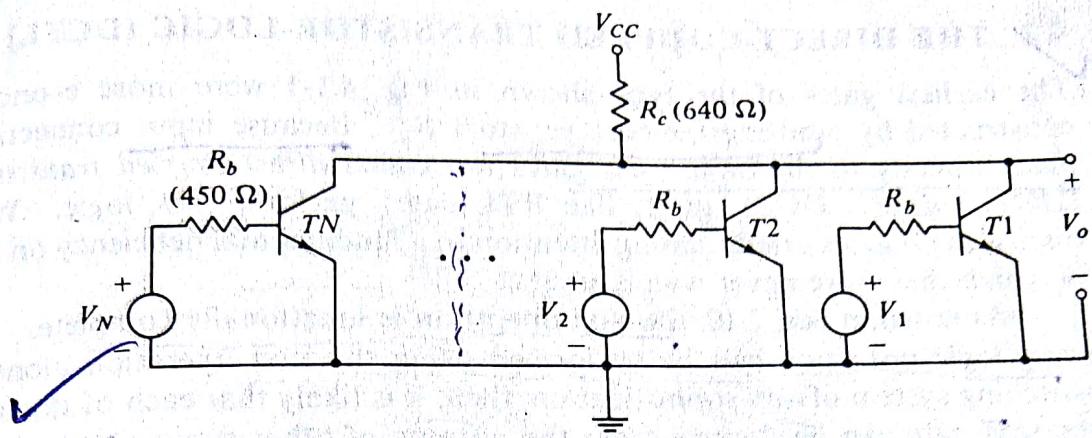


FIGURE 4.1-1

An N -input RTL gate. A medium-power commercial gate has the component values indicated in parentheses.

resistors R_b . If we adopt the convention of *positive logic*, then, as we can now verify, the gate performs NOR logic.

Let V_L and V_H be the voltages representing the two possible values of a logical variable. The subscripts L and H stand for "low" and "high." That is, $V_L < V_H$. In positive logic V_L corresponds to the case where the logical variable is "false," i.e., to logic level 0. The voltage is V_H when the variable is "true," i.e., at logic level 1. In the RTL gate V_L is required to be low enough for the corresponding transistor to be cut off when V_L is applied at a gate input. The voltage V_H is a voltage which, applied at an input, will drive the corresponding transistor to saturation. Note that V_L and V_H are not unique voltages but are characterized by the fact that V_L must be *less than* some unique voltage and V_H must be *greater than* some unique voltage. In the present case it is necessary that $V_L < V_\gamma$, the cut-in voltage, and V_H be equal to or higher than the voltage which when applied through R_b will bring the transistor to saturation.

The truth table for a two-input gate is given in Table 4.1-1. In one truth table we have used the logical values LOW and HIGH in the other 0 and 1. Both types of tables are common.

Table 4.1-1

V_1	V_2	V_o	V_1	V_2	V_o
L	L	H	0	0	1
L	H	L	0	1	0
H	L	L	1	0	0
H	H	L	1	1	0

4.2 THE DIRECT-COUPLED TRANSISTOR-LOGIC (DCTL) GATE

The earliest gates of the type shown in Fig. 4.1-1 were more economically constructed by omitting the base resistors R_b . Because input connections are made directly to the base, such gates are called direct-coupled transistor-logic (DCTL) gates. DCTL gates, like RTL gates, perform NOR logic. We shall discuss these gates briefly calling attention to a fundamental deficiency on account of which they were never widely used.

As noted in Sec. 3.10, the NOR operation is functionally complete. That is, every logic operation can be performed using the NOR operation alone. In a switching system of any sophistication, then, it is likely that each of the inputs to the NOR gate can be derived from the outputs of other similar NOR gates, and, in turn, each NOR gate may be required to furnish input logic levels to other NOR gates. Hence the situation of the DCTL gate G_{11} , shown in the dashed box of Fig. 4.2-1 is representative of the milieu in which a typical gate may have to function.

Let us focus our attention on gate G_{11} . It receives input V_i from gate G_0 , which is also required to furnish a signal to one input of $N - 1$ other gates G_{1N} through G_{2N} . Similarly, gate G_{11} must furnish signals to one input of N other gates G_{21} through G_{2N} . The other gate input terminals, not shown connected in Fig. 4.2-1, will derive their inputs from sources not specified here. If any of these gates has more inputs than required for its function, the unused gate input terminals are to be grounded. The corresponding transistor will then be at cutoff and will have no effect on the operation of that gate.

We now determine the voltage levels present at the input and output of the DCTL gates shown in Fig. 4.2-1. Suppose that all inputs of G_0 are low enough to keep all transistors in G_0 cut off. Then the common collector of G_0 will rise, driving transistors T_1, T_2, \dots, T_N to saturation. As noted earlier (Sec. 1.1), at room temperature the base-emitter voltage V_o of a saturated transistor is 0.75 V. Thus the gate voltage level corresponding to the 1 state at the output of gate G_0 is $V_o = 0.75$ V. The current supplied to the bases of each of the transistors T_1, T_2, \dots, T_N is supplied from the source V_{CC} through the resistor R_c . In this discussion we are assuming that R_c is small enough for adequate current to be available to drive all the transistors T_1, T_2, \dots, T_N to saturation. That is, the current in R_c is equal to

$$\frac{V_{CC} - V_o}{R_c} = \frac{V_{CC} - 0.75}{R_c}$$

Hence, each base current in T_1, \dots, T_N is $I_B = (V_{CC} - 0.75)/NR_c$ if T_1, \dots, T_N are identical. We are assuming that the current is adequate to saturate T_1, \dots, T_N . Note that the collectors of gate G_0 rise no higher than $V_o = 0.75$ V.

With at least one input of G_{11} at the logical level 1, the logic level at the output of G_{11} is 0, since $V_{CE} = V_{CE}(\text{sat})$. This voltage level, $V_{CE}(\text{sat})$, is typically between 0.1 and 0.2 V, depending on the current flowing in resistor R_c .

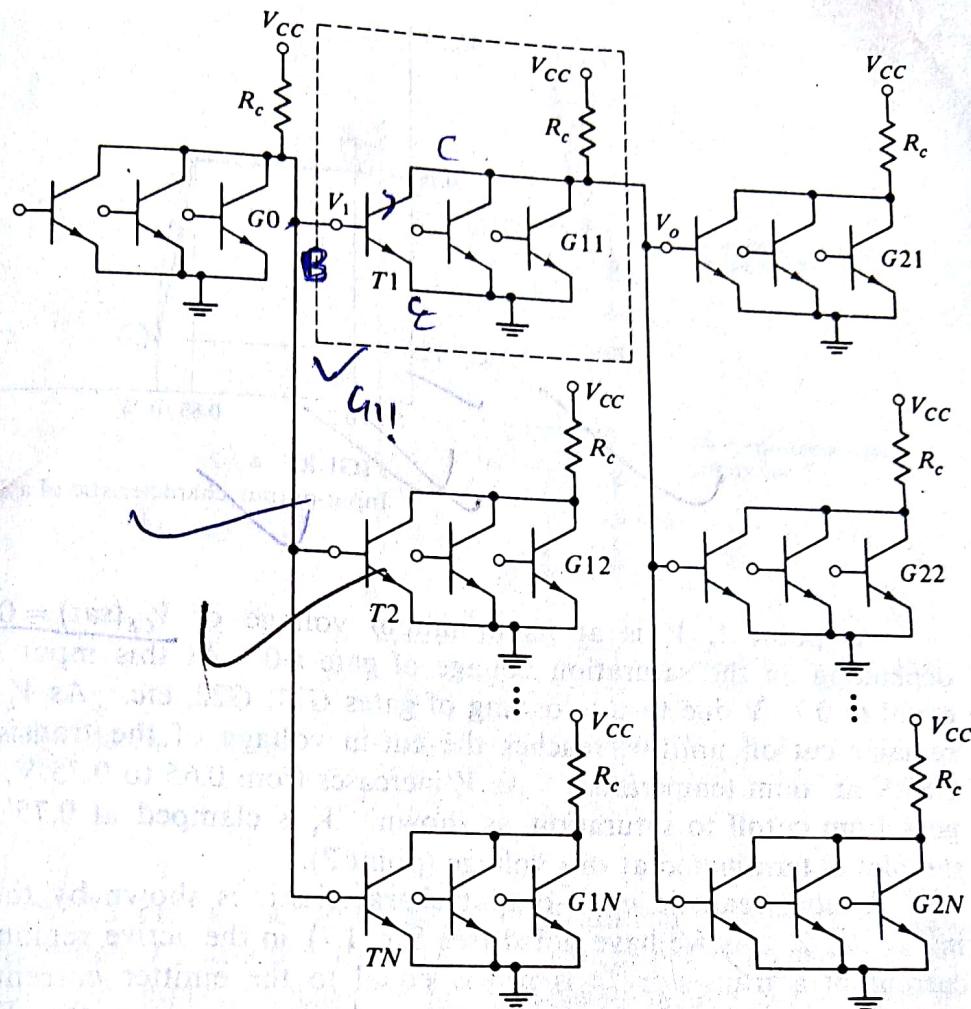


FIGURE 4.2-1
DCTL NOR gate with a fan-out of N .

of the gate. Since, as we have seen, the cut-in point of a silicon transistor occurs at a base-emitter voltage of about 0.65 V, the saturation voltage $V_{CE}(\text{sat}) = 0.1$ or 0.2 V, applied to an input of a succeeding gate is low enough to keep the corresponding transistor cut off.

It is to be observed that the total voltage separation, referred to as the logic swing between the voltages corresponding to the logic levels 1 and 0, is of the order of $0.75 - 0.1 = 0.65$ V.

Input-output characteristic of DCTL The above results are neatly summarized by the (idealized) *input-output characteristic* shown as the solid plot in Fig. 4.2-2. This figure plots the output V_o of gate $G11$ as a function of an input voltage V_i applied to one of the transistors in the gate. The other remaining transistors in the gate are assumed to be cut off; i.e., the other inputs are in the low state.

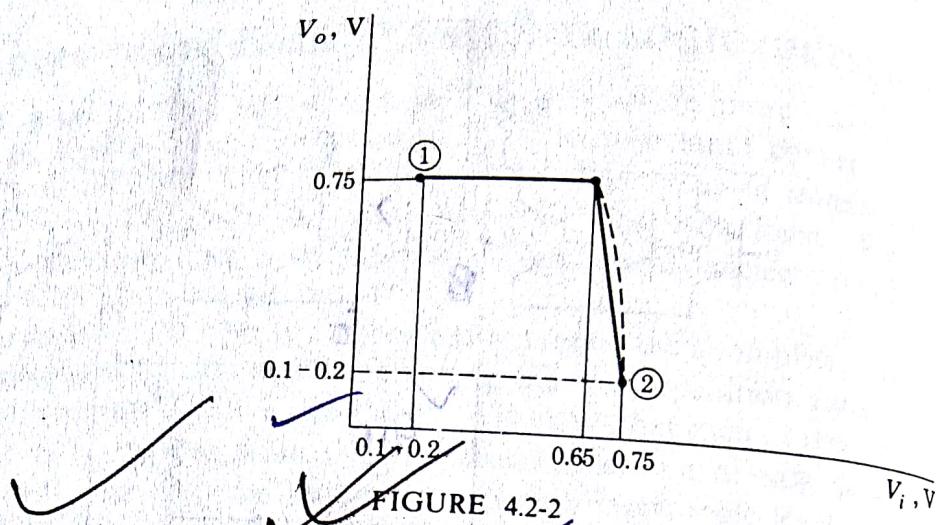


FIGURE 4.2-2
Input-output characteristic of a DCTL NOR gate.

At point 1, V_i is at its minimum voltage of $V_{CE(\text{sat})} = 0.1$ to 0.2 V, depending on the saturation voltage of gate G_0 . At this input voltage, V_o is equal to 0.75 V due to the loading of gates G_{21} , G_{22} , etc. As V_i increases, T_1 remains cut off until V_i reaches the cut-in voltage of the transistor, which is 0.65 V at room temperature. As V_i increases from 0.65 to 0.75 V, transistor T_1 goes from cutoff to saturation, as shown. V_i is clamped at 0.75 V, and hence the plot is terminated at this voltage (point 2).

A more realistic input-output characteristic is shown by the dashed plot in Fig. 4.2-2. As we have noted (see Sec. 1.7), in the active region the collector current of a transistor I_C is nearly equal to the emitter current I_E , and the emitter current is related to the emitter-base voltage by the diode equation [Eq. (1.7-3)]. Hence, since $V_{BE} = V_i$, we have

$$I_C \approx I_E \approx I_{E0} e^{V_i/V_T} \quad (4.2-1)$$

For values of V_o less than 0.65 the base currents of the transistors being driven by G_{11} fall to zero and we may write

$$V_o = V_{cc} - R_c I_C = V_{cc} - R_c I_{E0} e^{V_i/V_T} \quad (4.2-2)$$

Hence the input-output characteristic is a falling exponential with ever increasing magnitude of slope. In the range $0.65 \leq V_o \leq 0.75$ V, Eq. (4.2-2) is less exact since it does not take account of the volt-ampere characteristic of the base-collector circuits of the driven transistors.

4.3 CURRENT HOGGING IN DCTL GATES

DCTL gates suffer from a difficulty referred to as *current hogging*. To appreciate this problem we need only recognize that while transistors of similar manufacture are generally quite similar in performance, they are not precisely identical. Thus, referring to Fig. 4.2-1, suppose that the output of gate G_0 is at logic

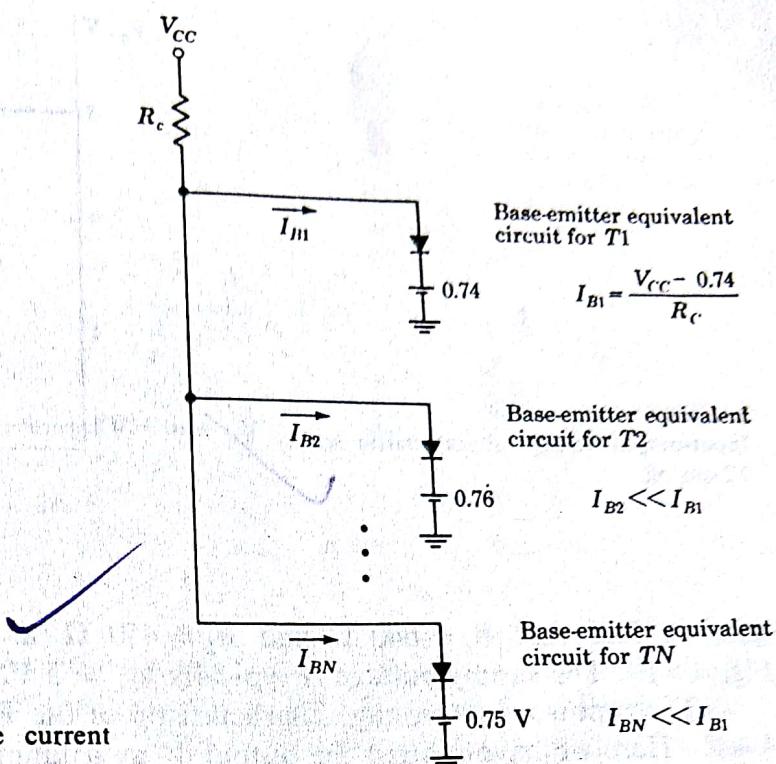


FIGURE 4.3-1
Equivalent circuit to illustrate current hogging in DCTL.

level 1, so that T_1 , T_2 , etc., are all to be driven to saturation. Suppose, by way of example, that when T_1 attains saturation, its base-emitter voltage is 0.74 V. But suppose that T_2 requires a base-emitter voltage of 0.76 V for saturation while 0.74 V leaves it in the active region. This difference may be due not only to the fact that the transistors are different but also to the fact that T_1 and T_2 may be in different integrated-circuit packages and hence operating at different temperatures. The temperature difference, in turn, may be due to the different physical location of the two units and possibly a difference in power dissipation in the two integrated circuit packages.

In any event, as seen from Fig. 4.3-1, which shows the output circuit of G_0 and the base-emitter equivalent circuits of T_1 , T_2 , ..., T_N , T_1 will hog much of the available current furnished by V_{CC} through R_c , and other transistors having base-emitter voltages greater than 0.74 V, such as T_2 , will be starved for base current and not be able to attain saturation as required. This current-hogging phenomenon, which is characteristic of DCTL, explains why this type of logic is not presently in wide use, and we shall not consider it further.

4.4 RESISTOR-TRANSISTOR LOGIC (RTL)

The current-hogging difficulty of the DCTL gate can be largely eliminated by introducing resistors in series with the base of each transistor as has been done in the RTL gate of Fig. 4.1-1 (see Prob. 4.4-1). In a medium-power commercial

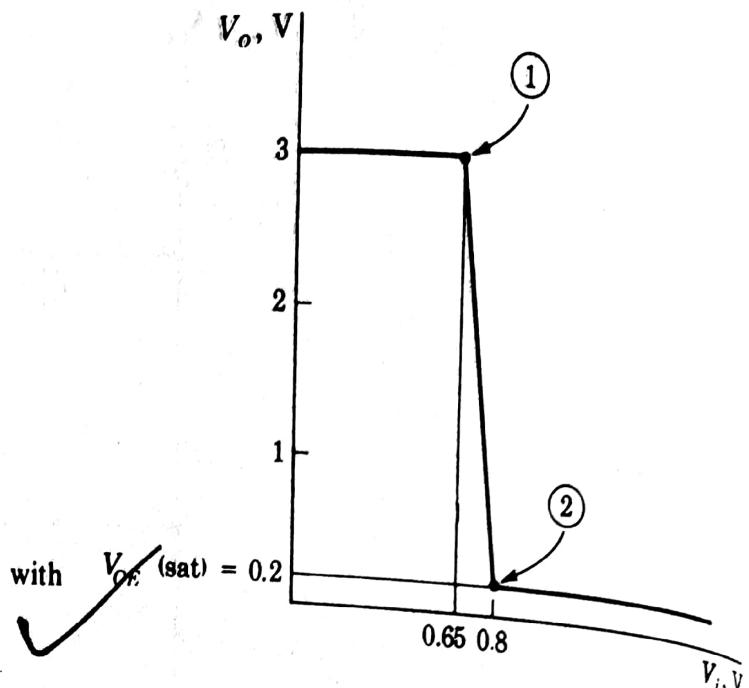


FIGURE 4.4-1

Input-output voltage characteristic with $V_{CE}(\text{sat}) = 0.2$
 T_2 cut off.

gate we find that $R_c = 640 \Omega$ and $R_b = 450 \Omega$, as noted in parentheses in Fig. 4.1-1. The supply voltage is typically $V_{CC} = 3$ V.

The input-output voltage characteristic of the RTL gate is shown in Fig. 4.4-1. Here we have plotted the output V_o as a function of one input V_i under the condition that all other input signals are at voltages which ensure that the corresponding transistor is cut off. Referring to Fig. 4.4-1, we note that if V_i is less than the cut-in voltage, which is 0.65 V at room temperature, T_1 is cut off and $V_o = V_{CC} = 3$ V.

When V_i exceeds 0.65 V, T_1 enters the active region and V_o decreases until T_1 saturates. It is useful to calculate the minimum value of V_i needed to bring T_1 into saturation. For the purpose of illustration let us assume that $V_{CE}(\text{sat}) = 0.2$ V, $h_{FE} = 50$, and $h_{FC} = 0.1$. Then from Fig. 1.10-1 we find that $\sigma \equiv I_C/50I_B = 0.85$. Using $R_c = 640 \Omega$, the collector current of T_1 is found from Fig. 4.1-1 to be

$$I_C = \frac{3 - 0.2}{640} = 4.4 \text{ mA} \quad (4.4-1)$$

and hence

$$I_B = \frac{4.4 \times 10^{-3}}{50(0.85)} \approx 0.1 \text{ mA} \quad (4.4-2)$$

Knowing I_B and assuming that $V_{BE}(T_1) = V_o = 0.75$ V since T_1 is saturated, we can calculate V_i . Referring to Fig. 4.1-1, we have

$$V_i = 450I_B + V_{BE} = 450(0.1 \times 10^{-3}) + 0.75 \approx 0.8 \text{ V} \quad (4.4-3)$$

Further increases in V_i produce only a small change in $V_o = V_{CE}$ since in saturation V_{CE} is typically between 0.1 and 0.2 V. Thus, as seen in Fig. 4.4-1, V_o has dropped to 0.2 V at $V_i = 0.8$ V, and we have idealized the plot by ignoring any further small change in V_o for $V_i > 0.8$ V. The plot is further idealized in that the plot from point 1 to point 2, which should be exponential in character, is drawn as a straight line.

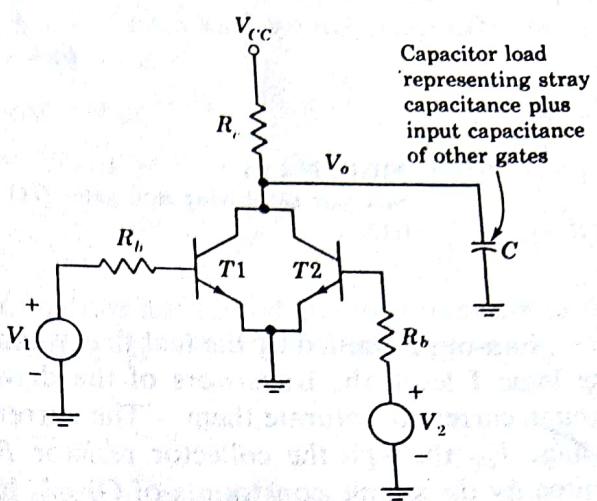


FIGURE 4.4-2
A two-input RTL gate with a capacitive load.

Types of RTL NOR gates As noted, commercially available integrated-circuit RTL NOR gates typically have the collector resistor $R_c = 640 \Omega$ while the base resistors $R_b = 450 \Omega$. A low-power RTL NOR gate is also available having $R_c = 3.6 \text{ k}\Omega$ while $R_b = 1.5 \text{ k}\Omega$. A disadvantage of this low-power gate is that the larger resistors result in slower operation: i.e., the propagation delay time is longer. The reason for this longer delay is that all stray capacitors and capacitors inherent in the active devices must charge and discharge through these larger resistors.

Pull-up resistors The collector resistor R_c in the RTL gate is often called a *passive pull-up resistor*. The reason for this terminology is to be seen in connection with Fig. 4.4-2, where an RTL gate drives a capacitive load C . This capacitance is due in part to stray capacitance and in part to the capacitance associated with the base-emitter junctions of gates driven by the gate shown.

Assume, initially that V_1 is high and V_2 low, so that $T1$ is saturated, $T2$ cut off, and V_o in the 0 state. Now let V_1 fall to the 0 state. $T1$ now cuts off, and V_o rises toward V_{cc} with a time constant $\tau = R_c C$. We say that V_o is pulled up to V_{cc} by the *pull-up resistor* R_c . Since R_c is passive, we say that the gate shown employs *passive pull-up*. Active pull-up is also available for RTL and many of the other gates to be discussed subsequently. The operation of active pull-up is postponed until Sec. 4.7, where we discuss the RTL buffer.

4.5 FAN-OUT

It will generally be necessary, in a physical switching system, for one NOR gate to provide the input logic levels to a number of other such gates. The number of gates driven by a single gate is referred to as the *fan-out* of that driving gate.

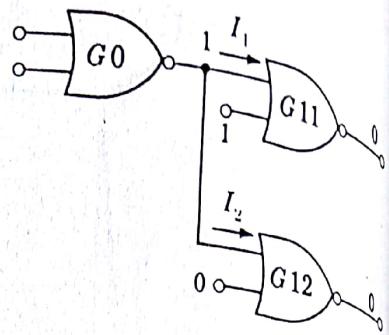


FIGURE 4.5-1
NOR gate G_0 driving NOR gates G_{11} and G_{12} .

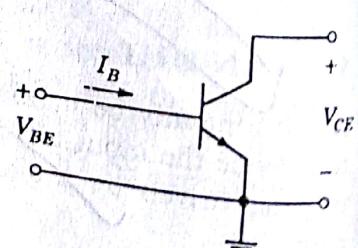
Fan-out is limited by the fact that when the output of the driving gate is at the logic 1 level, the transistors of the driven gate must all be furnished with enough current to saturate them. The current required is supplied by the supply voltage V_{CC} through the collector resistor R_c of the driving gate and hence is limited by the simple constraints of Ohm's law.

It is of some interest to note that when a driving gate, with its limited available driving current, is fanned out to a number of gates, those driven gates which make the greatest drain on the available current are precisely the gates which do not make effective use of the current. This point is made clearer by considering the situation indicated in Fig. 4.5-1. Here a driving gate G_0 has its output at logic level 1 and is driving two gates G_{11} and G_{12} . Gate G_0 will provide a current I_1 to the base of a transistor in G_{11} and a current I_2 to the base of a transistor in G_{12} . In gate G_{11} the other input is at logic level 1; hence the output of G_{11} would be logic level 0 even if it were not furnished with current I_1 . In this sense the current I_1 is "wasted." On the other hand, the second input of gate G_{12} is at logic level 0, and hence the current I_2 is essential to keep the output of G_{12} at level 0. It is therefore somewhat disconcerting to note that the "wasted" current I_1 is larger than the current I_2 .

To explore this point we need to consider the volt-ampere characteristic seen looking into the base of a transistor operating in the common-emitter configuration. This volt-ampere characteristic is a plot of I_B , the base current, as a function the base-emitter voltage V_{BE} . This current and voltage are indicated in Fig. 4.5-2. From the Ebers-Moll equations (1.7-3) and (1.7-4) we find that if the transistor is in the active region, the base current $I_B = I_E - I_C$ is related to V_{BE} approximately by

$$I_B = \frac{I_{E0}(1 - \alpha_N)}{1 - \alpha_N \alpha_I} e^{V_{BE}/V_T} \quad (4.5-1)$$

FIGURE 4.5-2
The current I_B and voltage V_{BE} defined.



In arriving at this equation we have taken account of the fact that $e^{V_{BE}/V_T} \gg 1$ and $e^{V_{BC}/V_T} \ll 1$. Since α_i is small ($\alpha_i \approx 0.1$ or even less), we may reasonably carry the approximation somewhat further and write

$$I_B = I_{E0}(1 - \alpha_N)e^{V_{BE}/V_T} \quad (4.5-2)$$

Finally, since $1 - \alpha_N = 1/(h_{FE} + 1) \approx 1/h_{FE}$, we have in the active region

$$I_B = \frac{I_{E0}}{h_{FE}} e^{V_{BE}/V_T} \quad (4.5-3)$$

Next, let us consider that the transistor has been driven to saturation to the maximum extent possible with $\sigma \equiv I_C/h_{EA}, I_M = 0$. We then verify, using Eqs. (1.7-3) and (1.7-4), that

$$I_B = I_{E0} e^{V_{BE}/V_T} \quad (4.5-4)$$

Equations (4.5-3) and (4.5-4) appear eminently reasonable. When the transistor is driven to the point where $\sigma = 0$, the collector current may be ignored in comparison with the base current. If we ignore the collector current, we may equivalently consider that the collector terminal of the transistor is floating unconnected. In this case looking into the transistor between base and emitter, we see a simple diode, i.e., the base-emitter junction. The volt-ampere characteristic is then given straightforwardly by the diode equation (4.5-4). However, in the active region, the fraction $h_{FE}/(1 + h_{FE})$ of the emitter-junction current continues on to the collector junction, while the remaining fraction $1/(1 + h_{FE}) \approx 1/h_{FE}$ becomes base current. The base current I_B is again of the form of the diode equation except smaller by the factor h_{FE} , as given by Eq. (4.5-3).

We have referred to the cut-in voltage V_y of a diode as the voltage at which the diode current just becomes large enough to be of significance. It is apparent that the cut-in point of the diode described by Eq. (4.5-3) is higher than the cut-in point of the diode described by Eq. (4.5-4), since in the first case the base current is always smaller by the factor h_{FE} . Since

$$\frac{1}{h_{FE}} \leq \exp\left(\ln \frac{1}{h_{FE}}\right) = \exp(-\ln h_{FE}) \quad (4.5-5)$$

we may write Eq. (4.5-3) in the form

$$I_B = I_{E0} \exp\left[\frac{V_{BE} - V_T \ln h_{FE}}{V_T}\right] \quad (4.5-6)$$

A plot of Eq. (4.5-6) would be identical to a plot of Eq. (4.5-4) except that the plot for Eq. (4.5-6) would be shifted in the positive V_{BE} direction by amount $V_T \ln h_{FE} = 0.1$ V for $V_T = 25$ mV and $h_{FE} = 55$. Thus, in a typical case the cut-in point of the active-transistor base input circuit will be about 0.1 V higher than for a transistor driven to the limit of saturation.

Now consider the situation represented in Fig. 4.5-3, where two transistors are paralleled like a two-input NOR gate. Suppose that T_2 is cut off. Then

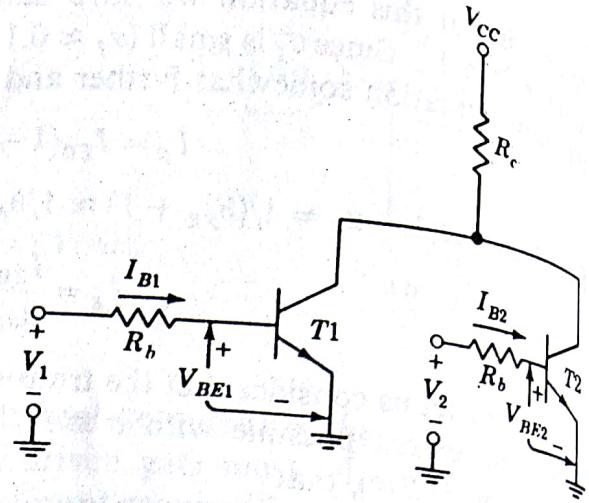


FIGURE 4.5-3

The input volt-ampere characteristic of T_1 depends on the operating condition of T_2 .

the volt-ampere input characteristic at the base of T_1 is given by Eq. (4.5-3), the presence of T_2 having no effect. But suppose, on the other hand, that V_1 is in saturation with V_{CE} , as usual, in the range 0.2 to 0.1 V. In this case when V_1 rises to bring T_1 out of cutoff ($V_{BE1} = 0.65$ V), the collector junction will also find itself forward-biased. That is, with $V_{BE1} = 0.65$ V and, say, $V_{CE} = 0.2$ V, $V_{BC} = 0.65 - 0.2 = +0.45$ V. Hence, T_1 is either cut off or in saturation and is never in the active region. Hence, when T_1 is ON, the input volt-ampere characteristic at the base of T_1 is given by Eq. (4.5-4).

Next, let us consider the worst-case situation represented in Fig. 4.5-4. Here a gate G_0 drives one input of N different gates. In every case except one, the transistor paralleling the driven transistor is in saturation. The transistors $T_{12}, T_{13}, \dots, T_{1N}$ are in saturation if they are not cut off. The transistor T_{11} may operate in the active region. Allowing for this worst-case condition, we now estimate the allowable fan-out.

As we have seen, the base current I_{B1} required to drive T_{11} is given by Eq. (4.4-2) as $100 \mu\text{A}$. We can make a rough estimate of the currents I_{B2}, \dots, I_{BN} by considering that the base voltages of $T_{12}, T_{13}, \dots, T_{1N}$ are lower by 0.1 V than the base voltage of T_{11} . Since V_o is common to all transistors, each current I_{B2}, \dots, I_{BN} is larger than I_{B1} by $0.1/R_b = 0.1/450 = 220 \mu\text{A}$. Therefore I_{B2}, \dots is

$$I_{B2} = 100 + 220 = 320 \mu\text{A} \quad (4.5-7)$$

We have also calculated, as given by Eq. (4.4-3), that at room temperature V_o [referred to as V_i in Eq. (4.4-3)] is 0.8 V. The maximum available current from the driver is I_o , given by

$$I_o = \frac{V_{cc} - V_o}{R_c} = \frac{3 - 0.8}{640} = 3.4 \text{ mA} \quad (4.5-8)$$

If the fan-out is to be N , we require that

$$I_o = I_{B1} + I_{B2} + \dots + I_{BN} \quad (4.5-9a)$$

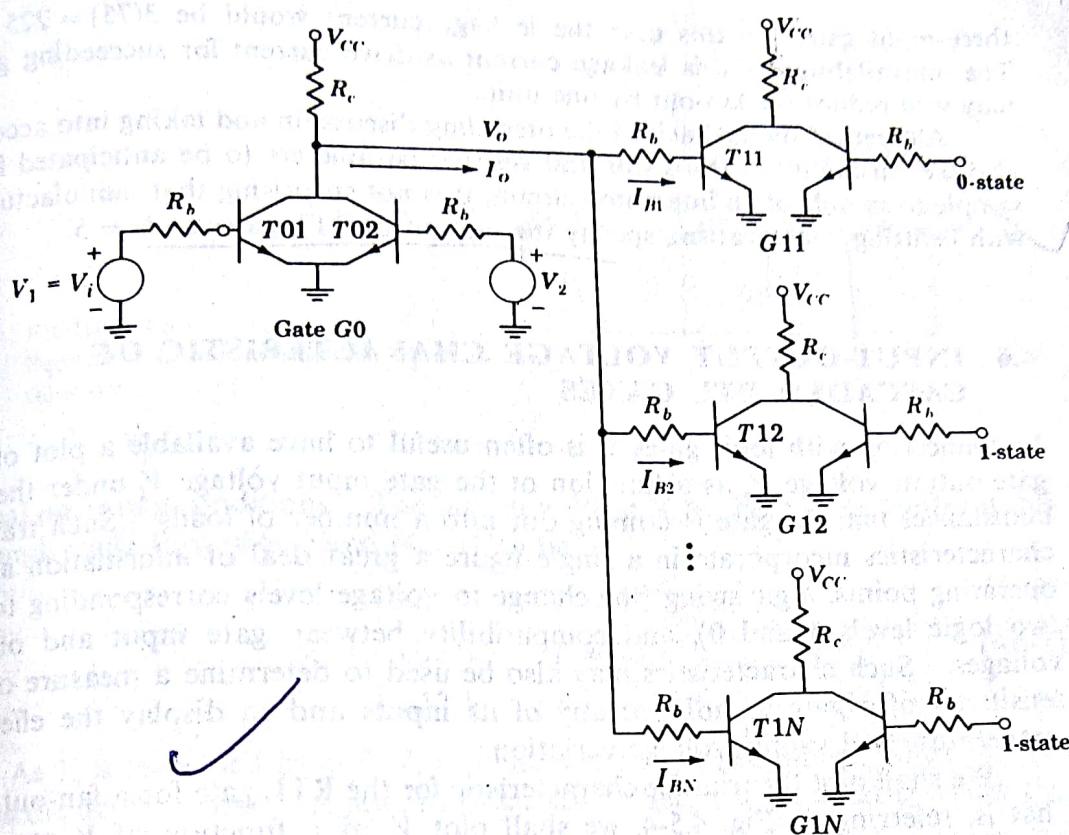


FIGURE 4.5-4

Gate G_0 drives N two-input gates. In all cases except one, the transistor paralleling the driven gate is in saturation.

and

$$3,400 = 100 + (N - 1)320 \quad (4.5-9b)$$

Thus we find that at room temperature

$$N = 11 \quad (4.5-10)$$

At lower temperatures the allowable fan-out would be reduced. This situation results from the temperature sensitivity of the base-emitter voltage V_{BE} ($-2 \text{ mV}/^\circ\text{C}$) and because h_{FE} decreases with decreasing temperature. At -55°C we would find that h_{FE} has fallen to about half its value at room temperature. With h_{FE} reduced to so low a value, it is easy to verify that at -55°C the fan-out must be reduced to about $N = 7$.

A further possibility may make it necessary to restrict the fan-out even slightly more than indicated by the preceding discussion. Referring to Fig. 4.5-4, we have assumed that when V_o is at logic 1, transistors T_{01} and T_{02} , being cut off, are drawing no current. As a matter of practice it turns out that when these transistors are cut off, each may, in a worst case, draw as much as $75 \mu\text{A}$ each of leakage current (see Sec. 4.9). Suppose then, for example, that gate G_0 is a

three-input gate. In this case the leakage current would be $3(75) = 225 \text{ nA}$. The unavailability of this leakage current as drive current for succeeding gates may well reduce the fan-out by one unit.

Altogether, on the basis of the preceding discussion and taking into account also the variability of transistor and resistor parameters to be anticipated from sample to sample of an integrated circuit, it is not surprising that manufacturers, with befitting conservatism, specify the fan-out of RTL gates at $N = 5$.

4.6 INPUT-OUTPUT VOLTAGE CHARACTERISTIC OF CASCADED RTL GATES

In connection with logic gates it is often useful to have available a plot of the gate output voltage V_o as a function of the gate input voltage V_i under the circumstances that the gate is fanning out into a number of loads. Such transfer characteristics incorporate in a single figure a great deal of information about operating points, logic swing (the change in voltage levels corresponding to the two logic levels 1 and 0), and compatibility between gate input and output voltages. Such characteristics may also be used to determine a measure of the sensitivity of a gate to noise at any of its inputs and to display the effect of temperature and supply-voltage variation.

We shall plot the transfer characteristic for the RTL gate for a fan-out of 5. That is, referring to Fig. 4.5-4, we shall plot V_o as a function of V_i assuming $N = 5$ and that $T02$ is cut off. We shall also assume that in each of the driven gates all transistors, other than the transistors connected to $G0$, are cut off. Note that in the present situation the base of each right-hand transistor $G1I-G1N$ is to be in the 0-state and not, as appears in the figure, in the 1-state.

When the voltage $V_i = 0 \text{ V}$, the output V_o of gate $G0$ is in the 1 state. All the driven gates, to which the driving-gate fans out, are in saturation. As we have discussed in Sec. 1.9, we shall assume that looking into the base, i.e., between base and emitter, a saturated transistor appears as a voltage source $V_s = 0.75 \text{ V}$ (at room temperature) or more generally [see Eq. (1.2-1)] as a source

$$V_s = 0.75 - (2 \times 10^{-3})(T - 25^\circ\text{C}) \quad (4.6-1)$$

The equivalent circuit needed to calculate the collector voltage V_o of gate $G0$ is as given in Fig. 4.6-1. In this circuit we have implicitly assumed that all driven transistors are identical. Applying Kirchhoff's laws to the circuit of Fig. 4.6-1, we find that (since $450/5 = 90 \Omega$)

$$V_o = \frac{3}{640 + 90} 90 + \frac{V_o}{640 + 90} 640 \quad (4.6-2)$$

Transistor specifications are usually presented at three temperatures, -55°C , room temperature $T = 25^\circ\text{C}$, and $+125^\circ\text{C}$. The low and high temperatures represent the extreme operating temperatures, while room temperature represents

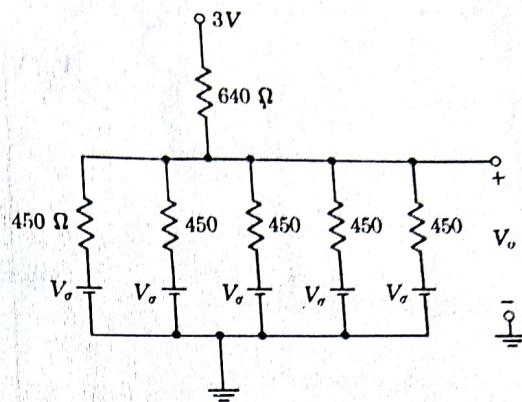


FIGURE 4.6-1
Equivalent circuit to calculate V_o when G0 is OFF.

typical operating conditions. The output voltage V_o at these three temperatures is found, using Eqs. (4.6-1) and (4.6-2), to be

$$V_o = \begin{cases} 0.85 \text{ V} & T = 125^\circ\text{C} \\ 1.03 \text{ V} & T = 25^\circ\text{C} \\ 1.17 \text{ V} & T = -55^\circ\text{C} \end{cases} \quad (4.6-3)$$

As V_i is increased from 0 V, a point will be reached where transistor T01 enters the active region. Again, as discussed in Sec. 1.2, we shall consider that this cut-in point occurs at

$$\begin{aligned} V_{BE} &= V_i = 0.65 - (2 \times 10^{-3})(T - 25^\circ) \\ &= \begin{cases} 0.45 & T = 125^\circ\text{C} \\ 0.65 & T = 25^\circ\text{C} \\ 0.81 & T = -55^\circ\text{C} \end{cases} \end{aligned} \quad (4.6-4)$$

Increasing V_i farther, we find that V_o decreases and eventually will drop to $V_{CE(\text{sat})}$, which we shall again assume to be in the range 0.2 to 0.1 V. The base-emitter voltage of the driving-gate transistors will again be $V_{BE} = V_o$ at saturation.

The input voltage at the point where T01 in gate G0 reaches saturation has already been calculated in Eq. (4.4-3) to be $V_i = 0.8$ V at room temperature. Using Eq. (4.6-1), we can similarly find V_i at other temperatures:

$$V_i = \begin{cases} 0.6 \text{ V} & T = 125^\circ\text{C} \\ 0.8 \text{ V} & T = 25^\circ\text{C} \\ 0.96 \text{ V} & T = -55^\circ\text{C} \end{cases} \quad (4.6-5)$$

Using the results given in Eqs. (4.6-3) to (4.6-5), we can construct the plots shown in Fig. 4.6-2. To see how these plots are obtained consider $T = 25^\circ\text{C}$. Then for $V_i \leq 0.65$ V (cut-in), $V_o = 1.03$ [Eq. (4.6-3)]. The value of cut-in is given in Eq. (4.6-4). The value of V_i needed to have $V_o = 0.2$ V (saturation) is $V_i = 0.8$, which is obtained from Eq. (4.6-5). The maximum value of V_i is 1.03 V

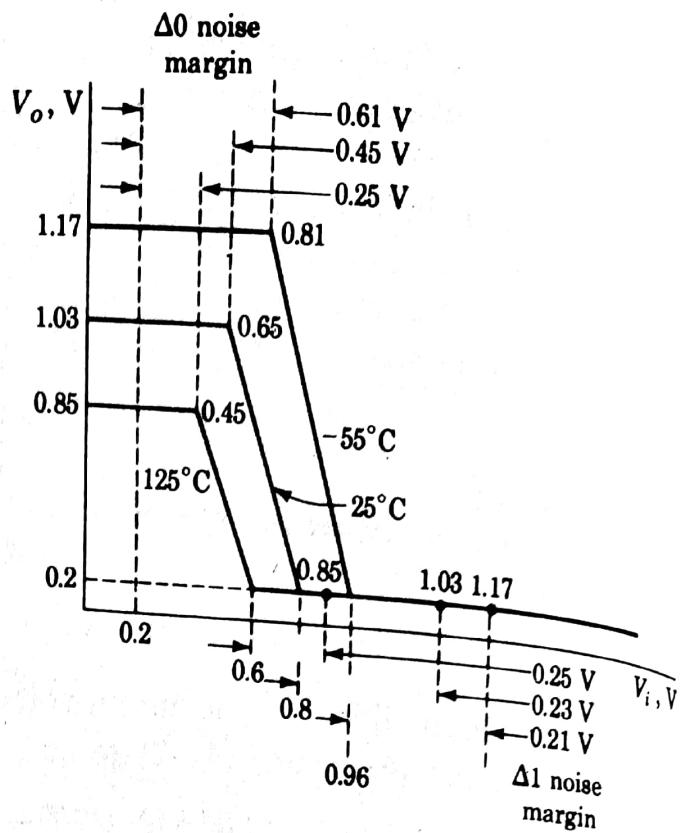


FIGURE 4.6-2
Input-output characteristic.

and is obtained by assuming that gate G0 is driven from another gate (not shown) having the same values of V_o that G0 has. Using a similar argument, we find that V_i cannot be less than 0.2 V, which occurs when the gate driving G0 saturates.

These plots are, of course, idealized and representative rather than real and exact. However, they are close enough to the actual plots that would be obtained in a representative real situation to be of great value. By way of comparison we compare the plots of Fig. 4.6-2 with the plots of Fig. 4.6-3 determined experimentally for typical gates. The real plots indicate some dependence of the temperature on the transistor saturation collector-emitter voltage. This, of course, should be expected, since, referring to Eq. (1.10-3), we see that $V_{CE}(\text{sat})$ is proportional to $V_T = kT/q$ and therefore $V_{CE}(\text{sat})$ increases with an increase in temperature. Our idealized plots have ignored this temperature dependence since the variation is small. We also note that while we have assumed that $V_o(\text{sat}) = 0.2$ V at room temperature, the characteristic shown in Fig. 4.6-3 has a value of 0.16 V. Starting with $V_{CE}(\text{sat}) = 0.16$ V at room temperature and since $0^\circ\text{C} = 273^\circ\text{K}$, we then have

$$V_{CE}(\text{sat}, 125^\circ\text{C}) = \left[\frac{273 + 125}{273 + 25} \right] 0.16 = 0.21 \text{ V} \quad (4.6-6)$$

and we correspondingly find $V_{CE}(\text{sat}, -55^\circ\text{C}) = 0.12$ V. These results agree with Fig. 4.6-3.

Noise margin The plots of Fig. 4.6-2 are useful because they provide the input and output voltage ranges corresponding to the two logic levels 1 and 0. We keep in mind that generally the input of one gate is the output of a preceding gate. Thus, when the logic level 0 appears at the output of a driving gate and

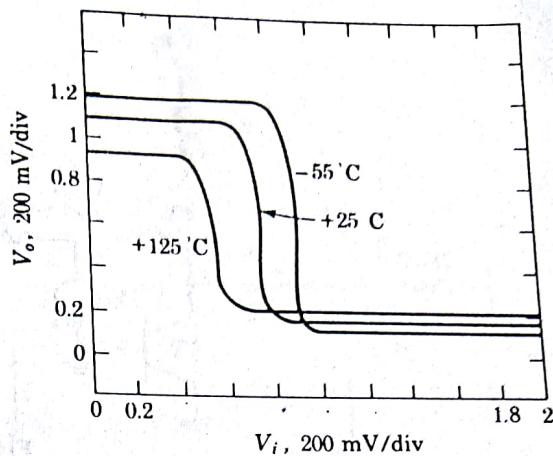


FIGURE 4.6-3

Typical RTL-gate transfer characteristic for three temperatures at fan-out = 5.

hence at the input to a driven gate, this logic level will correspond to the voltage $V_{CE}(\text{sat}) \approx 0.2 \text{ V}$. We now note from Fig. 4.6-2 that such a voltage, 0.2 V, is low enough to represent properly the logic level 0. For over the entire range of temperature contemplated in Fig. 4.6-2, the driven gate transistor will be cut off and the output of the driven gate will therefore be at a high voltage. Further, we note that this voltage $V_{CE}(\text{sat}) = 0.2 \text{ V}$ provides a *margin of safety* in assuring cutoff. For even in the least assured case, which occurs at $T = 125^{\circ}\text{C}$, there is a voltage difference $0.45 - 0.20 = 0.25 \text{ V}$ between $V_i = V_{CE}(\text{sat})$ and the minimum input voltages which would allow the driven transistor to enter its active region, $V_i = 0.45 \text{ V}$. Having marked off the voltage $V_{CE}(\text{sat}) = 0.2 \text{ V}$ on the abscissa of Fig. 4.6-2, we can indicate the margins of safety for the three temperatures in the manner shown in the figure. This margin of safety is also referred to as the *noise margin for an input corresponding to logic level 0* and is represented by $\Delta 0$. We have that

$$\Delta 0 = 0.65 - k(T - 25^{\circ}\text{C}) - V_{CE}(\text{sat}) = 0.45 - k(T - 25^{\circ}\text{C}) \quad (4.6-7)$$

where k , as noted, is $k = 2 \text{ mV}/^{\circ}\text{C}$. We note the decrease of $\Delta 0$ with increasing temperature.

The sensitivity to temperature of $\Delta 0$ is actually somewhat larger than indicated in Eq. (4.6-7), for we see in Fig. 4.6-3 that $V_o = V_{CE}(\text{sat})$ increases somewhat with temperature. Thus, the single dashed line erected vertically from the abscissa at $V_i = V_{CE}(\text{sat}) = 0.2 \text{ V}$ in Fig. 4.6-2 should be replaced by three lines, corresponding to the three temperatures. The reduction in $\Delta 0$ below the values given in Fig. 4.6-2 would be greatest for $\Delta 0$ at 125°C , the case where there is already the smallest noise margin. We may, as a matter of fact, observe that this limited $\Delta 0$ encountered with increasing temperature constitutes a disadvantage of consequence in RTL circuitry.

Now let us turn our attention to the case in Fig. 4.5-4, where V_i has increased sufficiently for $T01$ to be driven into saturation. In this case, of course, the higher the voltage V_i the more assurance we have of saturating transistor $T01$.

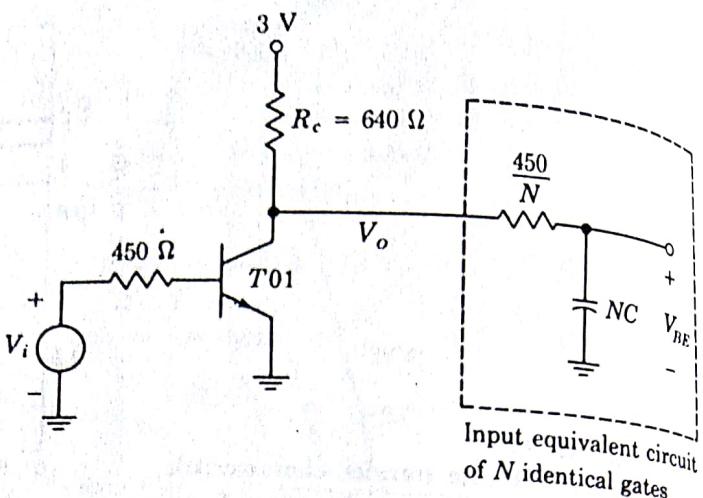


FIGURE 4.6-4
Equivalent circuit to determine the rise time of V_{BE} .

We note from Sec. 4.5 that the fan-out of the gate driving G_0 limits the extent to which V_i can rise, just as the fan-out of G_0 limits the maximum value of V_o . The greater the fan-out the lower the available voltage. Hence, we must consider that the maximum available input voltage to drive a gate is not the unloaded output voltage of a driving gate but the output voltage which is loaded by a maximum fan-out. We have drawn Fig. 4.6-2 for a fan-out of 5 precisely because this fan-out is nominally the maximum intended with RTL gates. The output voltages (1.17, 1.03, and 0.85 V) for the fan-out of 5 are, of course, the input voltages available to drive succeeding transistors to saturation.

We can now mark off on the abscissa of Fig. 4.6-2 these output voltages corresponding to a fan-out of 5. The noise margins $\Delta 1$ for an input corresponding to logic level 1 can be read off as indicated in the figure. Thus, at $T = -55^\circ$ the output is 1.17 V, and the minimum output which will keep a driven transistor in saturation is 0.96 V. The noise margin is therefore $\Delta 1 = 1.17 - 0.96 = 0.21$ V. We note from Fig. 4.6-2, that the $\Delta 1$ noise margins are not sensitively dependent on temperature.

Rise time The rise time of gate G_0 is affected by the number of gates it drives. To illustrate this consider that in Fig. 4.5-4 V_i is in the 1 state and V_o is in the 0 state. Then T_{11} to T_{1N} are cut off, and the base-emitter junction of each of these transistors appears to be a capacitor. Let us approximate this capacitor as a real constant capacitor C . Then the equivalent circuit of G_0 and the driven gates in the region where V_i changes from its 1 state to its 0 state (with V_o remaining in the 0 state) is shown in Fig. 4.6-4. Here we have assumed that each of the $N = 5$ driven gates is identical.

Now let V_i fall instantaneously from its 1 state to its 0 state. T_{01} cuts off, and the base-emitter voltage of T_{11} to T_{1N} rises with a time constant

$$\tau = \left(R_c + \frac{450}{N} \right) NC = (640N + 450)C \quad (4.6-8)$$

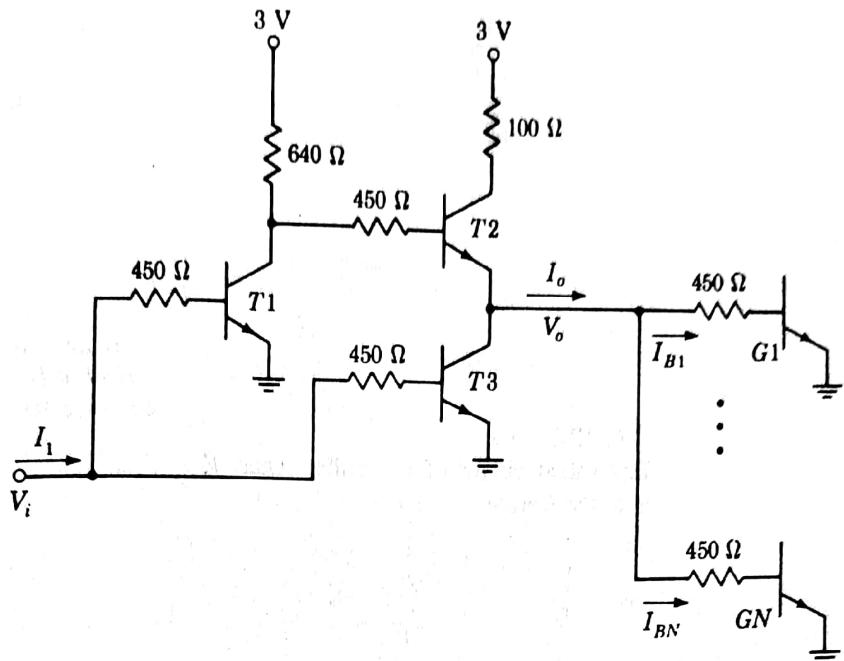


FIGURE 4.7-1
An RTL buffer inverter driving N gates.

The manufacturer generally specifies that $C \approx 5 \text{ pF}$; thus with $N = 5$, $\tau = 18 \text{ ns}$. In the next section we shall see that an RTL gate using an active pull-up can have the same value for τ and a significantly larger fan-out.

It should be kept in mind that the input capacitance to a transistor is not constant and is a function of the current in the base. Thus, the time constant indicated here is of only qualitative rather than quantitative value.

4.7 AN RTL BUFFER

The RTL gates discussed in the previous sections employed a *passive pull-up* R_c . This limited the output current, available to drive other gates, to a value less than V_{cc}/R_c . The *buffer* is an RTL gate using an *active pull-up* to achieve a very low output impedance. Thus, the output-current capability of the buffer is significantly greater than that of the ordinary gate. As a result, while the ordinary RTL gate has a fan-out of 5, the buffer has a fan-out of 25. In addition, since the buffer has a low output impedance, the *rise time* when driving a capacitive load is significantly less than that obtained when using a passive pull-up.

A typical RTL buffer is shown in Fig. 4.7-1. The transistor T_2 is the active pull-up which replaces the passive pull-up resistor R_c in the ordinary NOR gate. The transistor T_1 serves as a logic inverter. When V_i is at logic 0, the output of T_1 is at logic 1 and vice versa. Thus, the logic levels at the bases of T_2 and T_3 are always different, and when one of these transistors is conducting, the other is cut off. When T_2 is OFF, its collector current is zero; T_3 is saturated

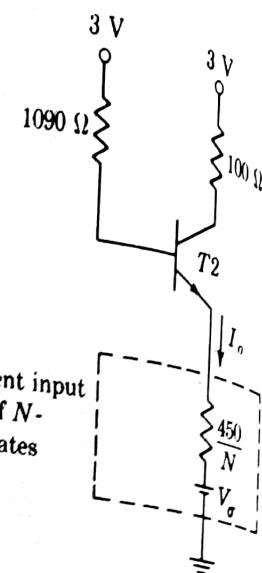


FIGURE 4.7-2
Equivalent circuit of the buffer when V_i is in the 0 state.

in the extreme with $\sigma = I_C/h_{FE} I_B = 0$, and (as can be seen in Fig. 1.10-1) its voltage $V_{CE}(\text{sat}) = 60 \text{ mV}$.

When T_3 is OFF and T_2 is ON and driving N gates, its output current I_o can be calculated from the circuit of Fig. 4.7-2. Assume first that T_2 is in its active region with $V_{BE}(T_2) = 0.7 \text{ V}$ and assume also $h_{FE} = 50$. At room temperature, as usual, we take $V_o = 0.75 \text{ V}$. Applying Kirchhoff's voltage law to the loop which includes the base-emitter junction of T_2 , we find

$$I_o = \frac{3 - 0.7 - 0.75}{1090/50 + 450/N} = \frac{7.1 \times 10^{-2}}{1 + 20.6/N} \quad (4.7-1)$$

If, instead, we assume that T_2 is saturated, we have $V_{BE} = 0.75 \text{ V}$ and $V_{CE} = 0.2 \text{ V}$. In this case we find (Prob. 4.7-4) that

$$I_o(\text{sat}) = \frac{21.8 \times 10^{-3}}{1 + 4.9/N} \quad (4.7-2)$$

To tell whether or not T_2 is saturated we need only compare the two currents. For if $I_o(\text{sat}) > I_o$, the transistor is not saturated, while if $I_o(\text{sat}) < I_o$, the transistor is saturated. It can be verified that the transistor is not saturated for $N = 1$ and is saturated for $N \geq 2$.

The buffer is ordinarily employed to drive a large number of gates. We shall therefore assume that $N \geq 2$ and that the transistor T_2 is saturated. Since $I_o(\text{sat})$ is supplied to all N gates, the current supplied to each gate is $I_{B1} = I_{B2} = I_{BN} = I_B$, where

$$I_B = \frac{I_o(\text{sat})}{N} = \frac{21.8 \times 10^{-3}}{N + 4.9} \quad (4.7-3)$$

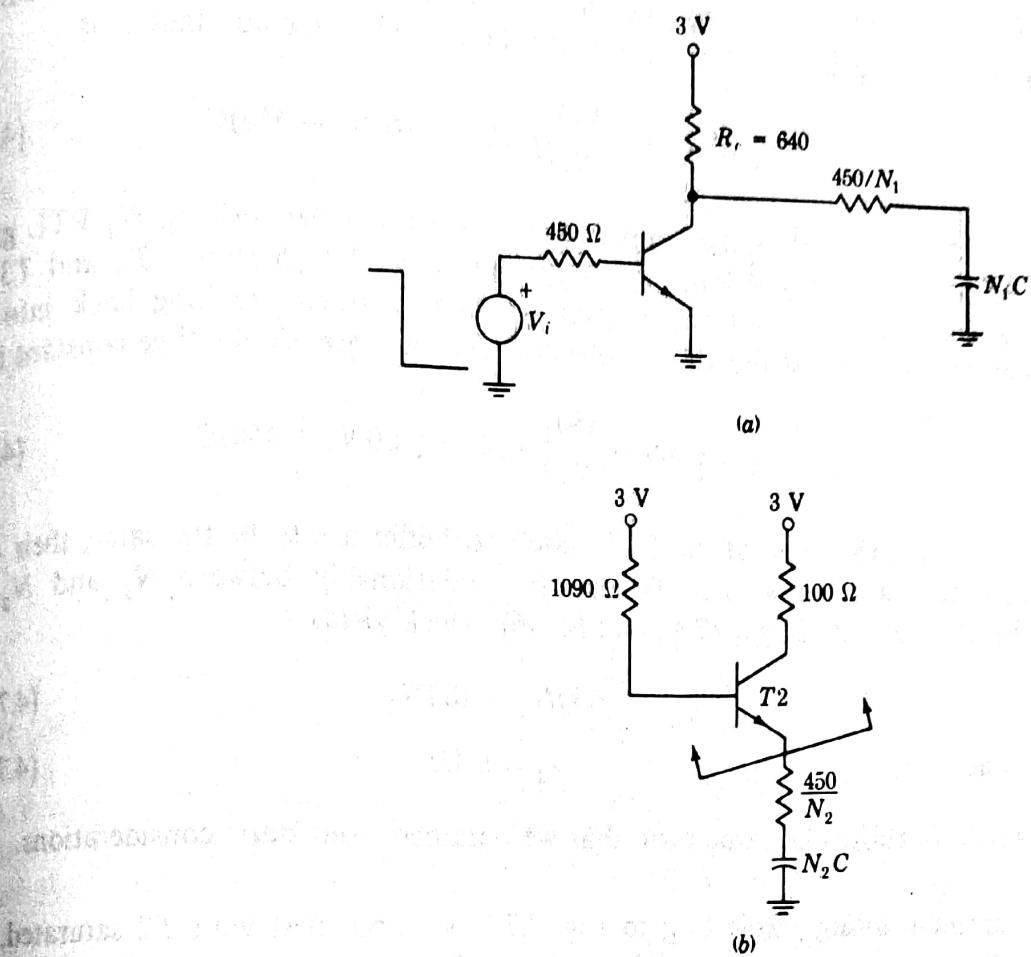


FIGURE 4.7-3
 (a) RTL gate circuit to determine time constant τ_i . (b) Equivalent circuit of buffer just after T1 and T3 cut off.

For the purpose of comparing the fan-out of the buffer to the fan-out of the ordinary RTL gate we assume that $I_B = 320 \mu\text{A}$, as in Eq. (4.5-7). Then

$$\frac{21.8 \times 10^{-3}}{N + 4.9} \geq 0.32 \times 10^{-3} \quad (4.7-4a)$$

and $N \leq 65 \quad (4.7-4b)$

Note that in Eq. 4.5-10 we found $N = 11$. Thus, we have improved the fan-out by a factor of 6. Manufacturer's specifications, typically conservative, state that the maximum fan-out of a buffer is $N = 25$, which is a factor of 5 greater than the specification of fan-out for an RTL gate.

We compare now the rise times of a buffer with a passive pull-up NOR gate. The rise time of a gate is proportional to the RC time constant of the gate and load. In Fig. 4.7-3a we have the equivalent circuit of an RTL gate driving N_1

identical RTL gates (see Sec. 4.6). We have represented the base-emitter junction of each transistor by a capacitor C . The time constant τ_1 is

$$\tau_1 = \left(640 + \frac{450}{N_1} \right) N_1 C = (640N_1 + 450)C \quad (4.7-5)$$

Figure 4.7-3b is the equivalent circuit of a buffer, driving N_2 RTL gates, just after the input voltage V_i dropped from its 1 to 0 state. T_1 and T_3 are cut off and T_2 is saturated. Since T_2 is saturated, looking back into the emitter, we see just the 100- Ω collector resistor. Hence, the time constant is

$$\tau_2 \approx \left(100 + \frac{450}{N_2} \right) N_2 C = (100N_2 + 450)C \quad (4.7-6)$$

If the rise time of the RTL gate and buffer are to be the same, their time constants are the same. To obtain a relationship between N_1 and N_2 we therefore equate Eqs. (4.7-5) and (4.7-6), which yields

$$640N_1 = 100N_2 \quad (4.7-7a)$$

Thus

$$N_2 = 6.4N_1 \quad (4.7-7b)$$

which is about the same ratio that we obtained from static considerations.

Current-limiting Referring to Fig. 4.7-2, we note that with T_2 saturated, the collector current is limited by the 100- Ω collector resistor. This resistor is designed to allow T_2 to saturate and yet limit its power dissipation.

To illustrate, let T_2 be saturated so that $V_{CE} \approx 0.2$ V. Then with $N = 25$, $I_o(\text{sat}) = 18$ mA. We can show (see Prob. 4.7-3) that $I_B = 1$ mA, so that $I_C = 17$ mA. Thus, the collector dissipation in T_2 is $P_C = 3.4$ mW. However, if the 100- Ω resistor were short-circuited, T_2 would not saturate, since $V_{CB} > 0$. Then from Eq. (4.7-1), $I_o(N = 25) = 39$ mA, and from Fig. 4.7-2,

$$V_{CE} = 3 - (450/25)(39 \times 10^{-3}) - V_o = 1.55 \text{ V} \quad (4.7-8)$$

The dissipation is now 60 mW, a considerable increase and a sizable dissipation for an integrated-circuit transistor.

4.8 AN RTL EXCLUSIVE-OR GATE

The EXCLUSIVE-OR gate was introduced in Sec. 3.10, where it was defined as a device which performs the operation

$$Z = \overline{A} \cdot B + A \cdot \overline{B} \equiv A \oplus B \quad (4.8-1)$$

An RTL circuit capable of performing this logic operation is shown in Fig. 4.8-1a. The operation of this circuit is as follows. Consider that B is in the

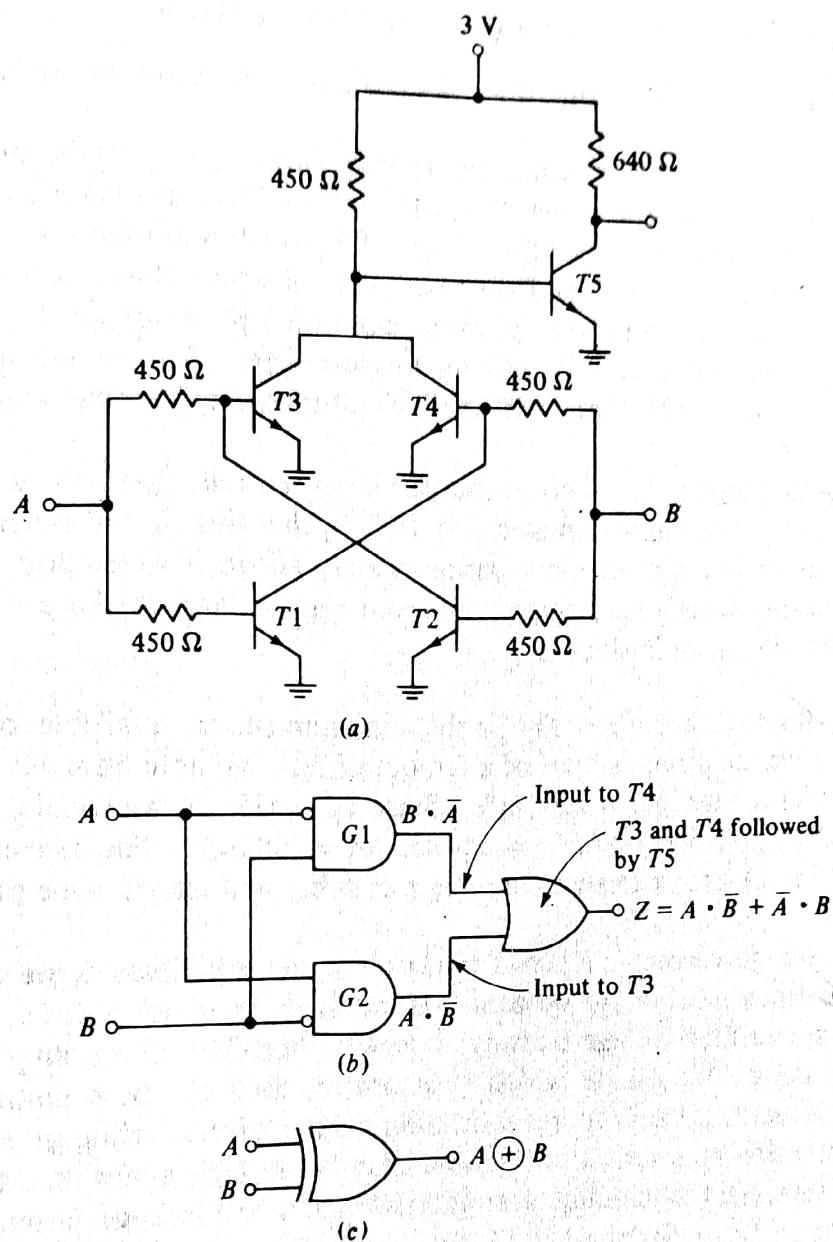


FIGURE 4.8-1
(a) An EXCLUSIVE-OR circuit using RTL. (b) Logic-gate representation and (c) symbol for EXCLUSIVE-OR circuit.

Referring to Fig. 4.8-1a, we see that transistors T_3 and T_4 represent a NOR operation. Transistor T_5 inverts the NOR output, producing an OR gate. This is shown in Fig. 4.8-1b. Thus, the output of T_5 is $Z = A \cdot \bar{B} + \bar{A} \cdot B$, as required.

Referring to Fig. 4.8-1a, we see that transistors T_3 and T_4 represent a NOR operation. Transistor T_5 inverts the NOR output, producing an OR gate. This is shown in Fig. 4.8-1b. Thus, the output of T_5 is $Z = A \cdot \bar{B} + \bar{A} \cdot B$, as required.

4.9 MANUFACTURER'S SPECIFICATIONS

This section is devoted to a discussion of the manufacturer's specifications of RTL gates.

There are four basic types of RTL gates. They are the medium-power gate (MRTL), where $R_c = 640 \Omega$ and $R_b = 450 \Omega$; the low-power gate (LRTL), where $R_c = 3.6 \text{ k}\Omega$ and $R_b = 1.5 \text{ k}\Omega$; the buffer, which is available in either the medium- or low-power class; and the EXCLUSIVE-OR gate. Some of the more important characteristics of each of these gates are presented in Fig. 4.9-1 for room temperature, $T = 25^\circ\text{C}$, and for a typical gate. Corresponding specifications at -55 and $+125^\circ\text{C}$ are also available in manufacturer's literature.

Input current, I_{in} This is the maximum current that will be drawn by a gate input. We have estimated [Eq. (4.5-7)] that this current is about $320 \mu\text{A}$. The manufacturer even more conservatively allows a worst case of $435 \mu\text{A}$. This manufacturer's specification is about right to account for his specification that the allowable fan-out is 5.

Output current, I_{out} This is the minimum current available to drive other gates under the circumstance of a fan-out of N . We note from Fig. 4.9-1 that for an MRTL gate, $I_{45} = 2.54 \text{ mA}$. Since $I_{in} = 435 \mu\text{A}$, we should expect that $I_{45} = 5I_{in}$. We find that $5I_{in} = 5 \times 435 \mu\text{A} = 218 \text{ mA}$. The difference $2.54 - 2.18 = 0.36 \text{ mA}$ provides an extra margin of safety and allows some current for leakage.

Leakage current When a transistor input is at logic 0, we would expect the collector current to be zero. However, such is not always the case since the base-emitter voltage is always somewhat positive. For example, if the transistor is driven by a gate which is saturated, then the base-emitter voltage of the transistor is equal to the saturation voltage of the driving gate. In a worst-case situation this saturation voltage may be as high as 0.4 V . As can be seen in Fig. 4.9-1, the manufacturer guarantees that the leakage current I_L is always less than $218 \mu\text{A}$ for the MRTL gate and buffer and $100 \mu\text{A}$ for the LRTL gate and buffer.

Input and output loading factors To provide guidance concerning allowable fan-out of gates, buffers, etc., manufacturers often assign numbers to the input and output terminals. These numbers, called input and output *loading factors*, are proportional (to the nearest integer on the conservative side) to the current required by an input or available from an output. Thus, as appears in Fig. 4.9-1, the input loading factor of an MRTL gate is 1, and the output loading factor N_G is 5. These numbers are interpreted to mean that the available output current is at least 5 times (but less than 6 times) the required input current. Consequently, when a gate drives a gate, the allowable fan-out is 5. We note that a buffer has an input loading factor of 2. Hence, a gate may be fanned out to two buffers but not three. The allowable fan-out of an LRTL gate is 4, and hence the input and output loading factors are 1 and 4, respectively.

	MRTL			LRTL	
	Gate	Buffer	Exclusive-or	Gate	Buffer
Fan out $\begin{pmatrix} N_G \\ N_B \end{pmatrix}$	5		5	4	
Propagation delay time, t_{pd}	12 ns	20 ns	12 ns	27 ns	57 ns
Power dissipation, P_d					
Inputs high	19 mW	16 mW	72 mW	4.8 mW	5.5 mW
Inputs low	5 mW	45 mW	72 mW	0.5 mW	16 mW
Input current, I_{in}	435 μ A	870 μ A	870 μ A	130 μ A	260 μ A
Output current, I_{A5}	2.54 mA	12.7 mA	2.54 mA	815 μ A	4 mA
Output leakage current, I_L	218 μ A	218 μ A	218 μ A	100 μ A	100 μ A
Saturation voltage	210 mV	210 mV	210 mV	220 mV	220 mV

FIGURE 4.9-1
Manufacturer's specifications.

The loading factors are modified when MRTL and LRTL gate families are used together. The loading factors of the LRTL gate remains 1 and 4, but the loading factors of the MRTL gate become 3 and 16. These numbers indicate that an MRTL gate is able not only to drive five other MRTL gates but can simultaneously drive an LRTL gate, that is, $16 = 5 \times 3 + 1$. In general, in fanning gates out we need only observe the rule that the output loading factor of the driving gate must be equal to or less than the sum of the input loading factors of the driven gates.

4.10 PARALLELING RTL GATES

To increase the number of inputs available in an RTL gate we can operate these gates in parallel. We consider now how the input and the output loading factors are affected by such paralleling.

One way of paralleling is shown in Fig. 4.10-1, where we have connected the output terminals of the two gates A and B and in each case have connected the top end of the collector resistor R_c to the supply voltage V_{cc} . As a consequence, the composite gate operates with a collector resistor $R_c/2$. It will be recalled that the output loading allowed on an RTL gate is limited by the fact that the output current required to drive other gates must be furnished from V_{cc} through the collector resistor. Since the paralleling has reduced the collector

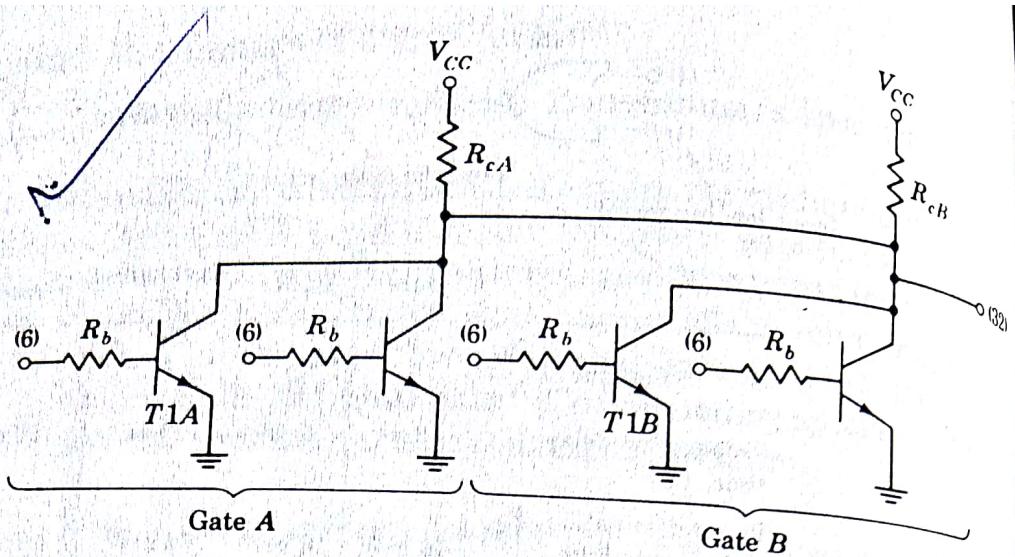


FIGURE 4.10-1
Paralleling two gates on the same chip.

resistor by a factor of 2, the effect of the paralleling is to increase the output loading factor by this same factor of 2. If MRTL gates are involved which individually have an output loading factor of 16, then, as indicated in Fig. 4.10-1, the paralleling has increased the output loading factor to 32. Altogether, then, the paralleling has doubled the output loading factor and has doubled as well the number of available input terminals to the gate.

The price to be paid for these advantages, as noted in Fig. 4.10-1, is that the input loading factor must also be increased by a factor of 2, increasing it to 6, while for a single gate the input loading factor is 3. This increased input load results from the fact that the collector resistance is $R_c/2$ rather than R_c . For with $R_c/2$ the collector saturation current increases by a factor of 2, and the base current required to drive a transistor to saturation must increase correspondingly by 2 (for the same σ and the same saturation voltage). Similarly if N gates are paralleled, the output loading factor becomes $16N$ and the input loading factor becomes $3N$.

These results for paralleling apply when the individual gates involved are part of the same integrated circuit, i.e., are on the same chip. When the individual gates are on different chips, the input loading factor must be increased beyond $3N$ for a reason now to be discussed.

A characteristic of integrated circuits is that there may be considerable variability in the values of resistors in any given circuit. Thus, from sample to sample, in an RTL gate, R_c and R_b may vary widely. On the other hand, there is substantially less variability in the ratio of resistors R_c/R_b . This greater uniformity of the resistor ratio serves to provide a measure of compensation in the operation of a gate operating individually. For suppose, in a particular gate, that R_b is considerably larger than average. Then in a typical operating situation the base current of a transistor in such a gate will be smaller than average. On the other hand, if R_b is larger, R_c will be also. Hence, the transistor saturation current will be smaller, and the smaller available base current will be

adequate to drive the transistor to saturation. Similarly if R_c is smaller, the saturation current will be larger. But the correspondingly smaller R_b will serve to increase the base current, as required. Finally we may note that if the resistors in a gate depart from the average, all the resistors in all the gates *on that same chip* depart from the average in the same direction.

Now let us consider the situation when the paralleled gates are on *different* chips. In this case the resistor on one gate may be high and on the other gate low. Thus, for example, in Fig. 4.10-1, consider that in gate A the collector resistor (call it R_{cA}) is high and in gate B, R_{cB} is low. Suppose that the paralleled gate is to be driven to logic level 0 by driving transistor TIA to saturation. Since R_{cB} is smaller than R_{cA} , the parallel combination of R_{cA} and R_{cB} is less than $R_{cA}/2$. Therefore, when gate B is paralleled with gate A, the current required to drive TIA to saturation is *more than doubled*. Hence, the input loading factor at the input to TIA is also more than doubled by the paralleling. Thus, the input loading factor must be increased above 6. To put the matter another way, we say that to drive the extra current required in R_b of TIA we must assure a higher voltage at the input to TIA . This result can be accomplished by restricting somewhat the allowed loading on the driving gate. If we specify a higher input loading factor for gate A, we shall have accomplished precisely this end.

Referring again to Fig. 4.10-1 and assuming again that $R_{cB} < R_{cA}$, if the drive is to be applied to the base of transistor TIB instead of TIA , the loading factor at this input might be set at less than 6. On the other hand, when gates are paralleled, unless we take special pains to investigate, we shall not know which gate has the higher resistors and which the lower. Hence, the only thing we can do is to allow an extra margin of input loading factor at *every* gate input.

In the matter of the extra margin of input loading factor we must seek guidance from the manufacturer, who will base his recommendations on what he knows his manufacturing tolerances to be. Typically, we find that in MRTL, when a gate on a first chip is to be paralleled with a gate on a second chip, it is recommended that the input loading factor be increased by 0.75 load. Thus, in Fig. 4.10-1 we would set the input loading factors at 6.75. Finally consider that a total of N gates are to be paralleled with N_A of the gates on chip A and N_B of the gates on chip B ($N_A + N_B = N$). Then, by an easy extension of the present discussion it would appear that the input loading factor on chip A is $3N + 0.75N_B$ and on chip B is $3N + 0.75N_A$.

4.11 SPECIFICATION OF OPERATING VOLTAGES

Figure 4.6-2 indicated the input-voltage-output-voltage variation of an RTL gate having a maximum fan-out of 5, a supply voltage $V_{cc} = 3$ V, and operating temperatures of -55 , $+25$, and $+125^\circ\text{C}$. However, the figure does not take account of the variability of transistor and resistor parameters due to manufacturing tolerances. To take account of such variability the manufacturer specifies

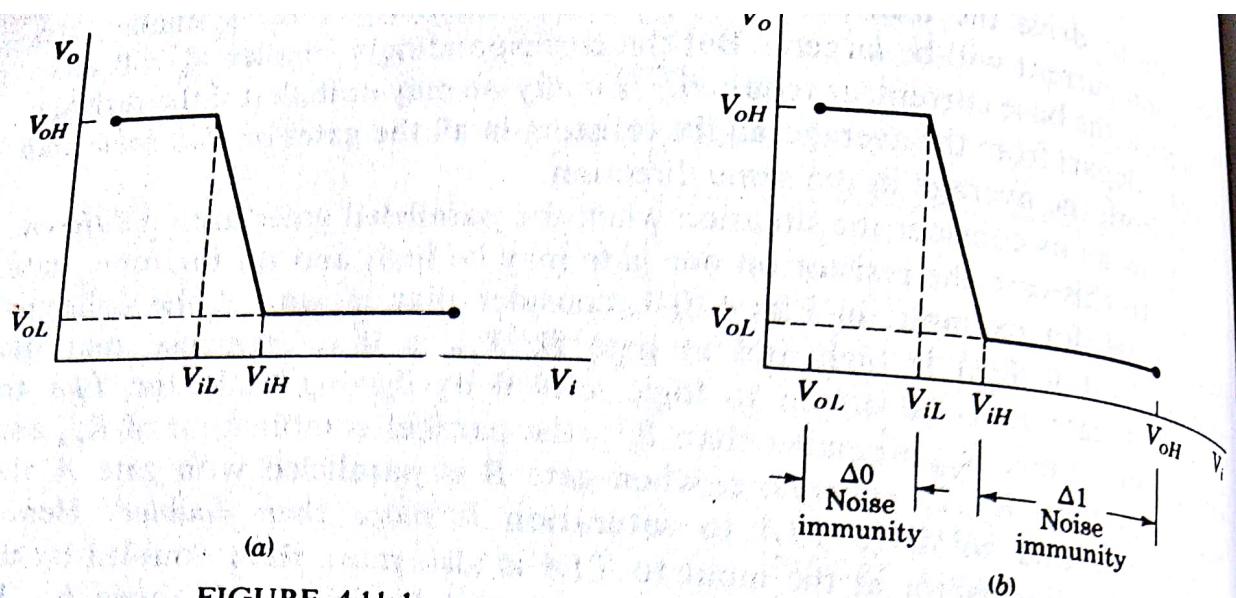


FIGURE 4.11-1

Input-output characteristic showing (a) worst-case parameters and (b) Δ_0 and Δ_1 noise immunities.

the worst-case parameters V_{oH} , V_{iH} , V_{oL} , V_{iL} shown in Fig. 4.11-1a. These parameters are specified at a given temperature, $V_{CC} = 3V \pm 10$ percent, maximum fan-out, and worst-case manufacturing tolerances. The definitions of these parameters are:

V_{oH} The minimum voltage which will be available at a gate output when the output is supposed to be at logic 1

V_{iH} The minimum gate input voltage which will unambiguously be acknowledged by the gate as corresponding to logic 1

V_{oL} The maximum voltage which will appear at a gate output when the output is supposed to be at logic 0

V_{iL} The maximum gate input voltage which will unambiguously be acknowledged by the gate as corresponding to logic 0

Thus, if V_i and V_o are gate input and output voltages, respectively, it is guaranteed that if $V_i \leq V_{iL}$, then $V_o \geq V_{oH}$ and if $V_i \geq V_{iH}$, then $V_o \leq V_{oL}$.

In Fig. 4.11-1b we have marked off the voltages V_{oL} and V_{oH} on the input voltage axis. It now appears that the noise immunities are

$$\Delta_0 = V_{iL} - V_{oL} \quad \text{and} \quad \Delta_1 = V_{oH} - V_{iH}$$

Since these four parameters V_{oH} , V_{iH} , V_{iL} and V_{oL} completely describe the worst-case input-output voltage characteristic and determine the Δ_0 and Δ_1 noise immunity, there is hardly any need for plotting the characteristic of Fig. 4.11-1. Instead, the same information is often presented in the manner shown in Fig. 4.11-2.

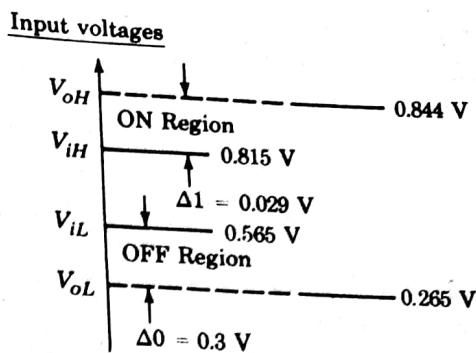


FIGURE 4.11-2
Manufacturer's specified noise margins.

EXAMPLE 4.11-1 For a given RTL gate operating at 25°C, the worst-case parameters as specified by the manufacturer are $V_{oH} = 844$ mV, $V_{iH} = 815$ mV, $V_{iL} = 565$ mV, and $V_{oL} = 265$ mV. Find the $\Delta 0$ and $\Delta 1$ noise immunity.

SOLUTION The worst-case parameter values are shown in Fig. 4.11-2. Thus, the worst-case $\Delta 0$ noise immunity is 300 mV, while the worst-case $\Delta 1$ noise immunity is 29 mV. These results are significantly poorer than those shown in Fig. 4.6-2, where the $\Delta 0$ noise margin is 450 mV and the $\Delta 1$ noise margin is 230 mV. These results seem worse than they really are. The manufacturer readily concedes that the results are extremely conservative and that larger noise margins actually exist.

4.12 PROPAGATION DELAY TIME

We have noted (Sec. 1.17) that there are propagation delays associated with logic gates. In RTL gates these delays are generally specified in terms of the parameters defined in Fig. 4.12-1. Here an input waveform (presumably the output of a preceding gate) is shown which makes a transition from logic 0 to logic 1 and thereafter a reverse transition. The corresponding output waveform is also shown. As is indicated, propagation delays are measured from the points on the waveform which are 0.5 V positive with respect to the logic 0 level. Since logic 0 is at about 0.2 V, the points on the waveform are at 0.7 V, which is very nearly the midpoint of the voltage range at which the transistors of the gates are passing through their active region (see Fig. 4.4-1). The time $t_{pd}(HL)$ is the propagation delay associated with a transition of the output waveform from its higher to its lower voltage while $t_{pd}(LH)$ is the corresponding delay as the output swings from its lower to its higher voltage level. The two propagation delays are not ordinarily equal.

Propagation delays result, in part, from the fact that, as voltages change, capacitors must be charged and discharged. The total capacitance with which the gate must contend depends on the fan-out and also on the fan-in (i.e., the number of inputs on the gate). Hence the propagation times are themselves

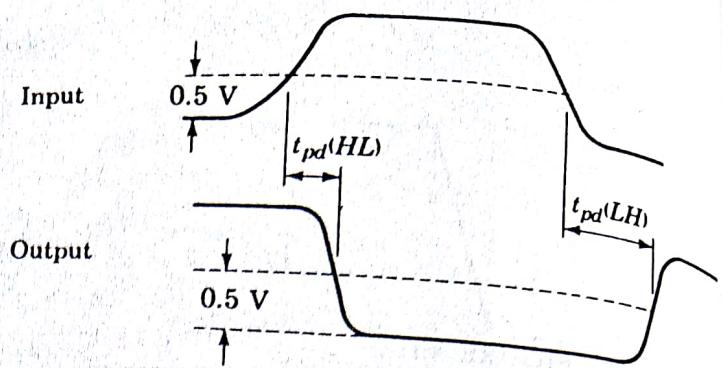


FIGURE 4.12-1
The propagation delay times $t_{pd}(HL)$ and $t_{pd}(LH)$.

functions of fan-out and fan-in. Typically in RTL gates propagation times are of the order of 10 ns. Such times compare favorably with propagation times associated with other types of gates yet to be considered. Unfortunately, in spite of the favorable propagation times, RTL gates are not widely used because of their relatively poor noise margins and fan-out capabilities.

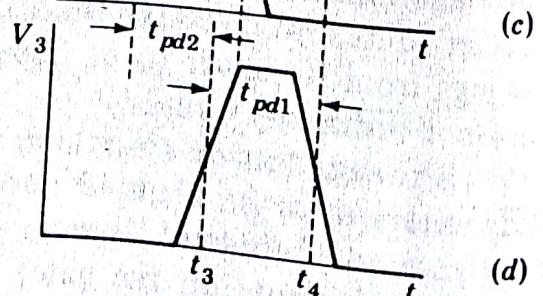
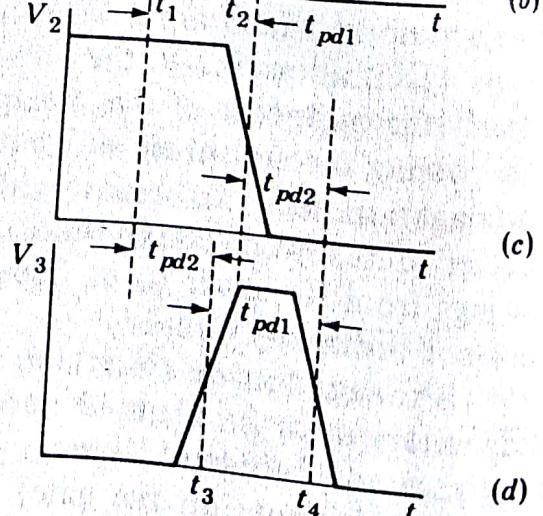
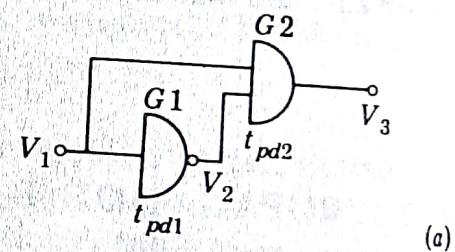


FIGURE 4.12-2
(a) A gate structure whose response is adversely affected by the propagation time delay t_{pd1} . (b) The input waveform. (c) The output of G1. (d) The output pulse from G2.

Propagation delay hazards As an example of the difficulty which may be caused by propagation delay in gates, consider the situation represented in Fig. 4.12-2. The NAND gate (used as an inverter) has a propagation delay t_{pd1} and the AND gate a delay t_{pd2} . It is intended that V_3 shall be in the 0 state independently of V_1 , as is indeed consistent with the logic of the circuit. However, as we may see from the waveforms in the figure, a transition in V_1 from logic 0 to logic 1 will result in a positive pulse of duration t_{pd1} as appears in (d). V_1 makes its transition at t_1 , taken, for simplicity, to be at the midpoint of the voltage excursion of the waveform V_1 , the waveform V_1 having a finite rise time since it is itself the output of some preceding gate (not shown). V_2 then makes an excursion from 1 to 0 after a time t_{pd1} at time t_2 . (We take the fall time of V_2 to be about the same as the rise time of V_2 .) Since now V_1 rises to 1 before V_2 falls from 1, there will be an interval when the AND gate output V_3 will be 1. V_3 rises to 1 at $t = t_3$ delayed by an interval t_{pd2} from t_1 . At $t = t_2$, after a delay t_{pd1} , V_2 falls back to 0 and finally, at $t = t_4$, after a delay again of t_{pd2} , V_3 will fall back to 0. In summary, it then appears that the step in V_1 has given rise to a pulse in V_3 . Note that the time of occurrence of the pulse is determined by t_{pd2} but that the width of the pulse is determined by t_{pd1} . Furthermore, the very existence of the pulse results from the delay t_{pd1} . Unintended results due to such gate propagation delays are referred to as *hazards*.

Charge compensation to reduce propagation time As noted, propagation delays result, in part, from the necessity to establish and remove base charge as transistors are turned ON and OFF. (See Sec. 1.17.) One way by which this process may be hastened is to provide for the flow of impulsive (very large albeit short-duration) currents into and out of the base. In RTL, such impulsive currents may be provided by bridging capacitors across the base resistors R_b , as shown in Fig. 4.12-3a.

Suppose $T1$ is in saturation because its input is at logic level 1. When V_1 drops to logic 0, $T1$ should cut off as the stored base charge is reduced to zero. In the absence of the capacitor C , this charge must dissipate in part through recombination in the base and in part by flowing out of the base through R_b . With the capacitor, however, an impulsive current can flow out of the base, removing the base charge much more rapidly. If the capacitor is adequately large it is possible, in principle at least, to transfer all the base charge to the capacitor instantaneously thereby turning the transistor OFF with limitless speed. The use of capacitors to draw charge abruptly out of a semiconductor is called *charge compensation*.

In integrated circuitry, conventional capacitors are used only infrequently because they take up a large amount of area on the IC chip. However, the junction capacitance of a transistor is sometimes employed when capacitors are required. In Fig. 4.12-3b such junction capacitors have been bridged across the resistors R_b through the addition of transistors $T3$ and $T4$. The capacitances of the base-emitter junctions of these added transistors bridge the resistors R_b .

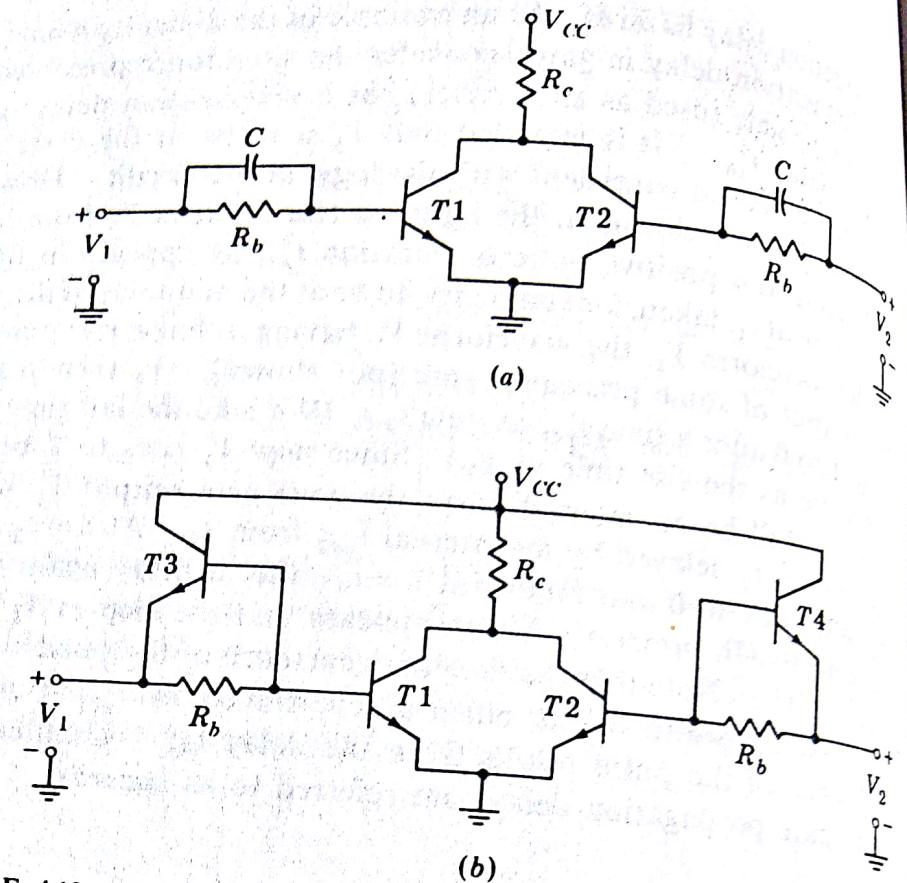


FIGURE 4.12-3

(a) An RTL gate with capacitors added to provide charge compensation. (b) A practical application of charge compensation using the capacitances across the base-emitter junctions of the added transistors.

A family of RTL gates as in Fig. 4.12-3b with $V_{CC} = 4.0$ V, $R_c = 1.9$ k Ω , and $R_b = 1.2$ k Ω is manufactured by the Western Electric Co. for use by the Bell System.

4.13 INTEGRATED-INJECTION LOGIC (IIL)

We have seen in Sec. 4.5 that when transistors are paralleled, as in RTL gates, the base current drawn by one transistor becomes inordinately large if one of its paralleling transistors goes to saturation. This increase in base current becomes progressively more pronounced as more of the paralleling transistors are turned ON and may be particularly pronounced in high fan-in gates. This feature of operation of paralleled transistors accounts, in large measure, for the relatively low fan-out of RTL gates. In addition DCTL suffers from the difficulty of current hogging, discussed in Sec. 4.3. For these reasons DCTL has never found any extensive applications. And while RTL did enjoy a brief period of popularity, it has now fallen into disfavor and is not presently incorporated into new digital systems.

In succeeding chapters we shall explore a number of other families of logic which do not have the limitations of DCTL and RTL. Some of these involve bipolar transistors, others use field-effect devices. These other bipolar transistor gates, particularly, have the disadvantage that they are appreciably more complicated than DCTL or RTL. Hence each such gate occupies more real estate on the integrated-circuit silicon chip than, say, DCTL would. This greater area requirement is, of course, a disadvantage in LSI and even in MSI. As we shall see, FET devices are more economical of area but unfortunately are appreciably slower than bipolar transistor gates.

RTL and DCTL were the first logic families commercially developed. Thereafter a number of other logic families were introduced; these families are described and analyzed in succeeding chapters more or less in the order of their development. *Integrated-injection logic (IIL or I²L)* is the most recent logic system to be introduced to commercial application. We discuss it at this point because it has a special relationship to DCTL. IIL has the elegant simplicity of DCTL. A typical gate uses very little real estate and consumes very little power. For these reasons IIL is eminently suited for medium- and large-scale integration applications.

When a logic family is to be used in medium- or large-scale integration, where gates are to be crowded as close together as possible, the power dissipation per gate is a matter of great concern. It is generally true, as we have already seen for RTL, that a trade-off can be made by sacrificing power dissipation to speed. Hence a figure of merit which is relevant in comparing one logic family with another is the *speed-power* product. Speed is measured by the propagation time and power by the power dissipation of a typical gate. It is impressive to compare the speed-power product of IIL with the corresponding product for other logic families. By way of example, consider the comparison between IIL and TTL (transistor-transistor logic, discussed in detail in Chap. 6). At the present time TTL is the most popular family of logic, certainly in small-scale integration, and it has extensive applications in medium-scale integration and some application in large-scale integration. We find that for TTL the speed-power product [dimensionally, $(\text{time} \times \text{energy})/\text{time} = \text{energy}$] is typically 100 pJ, while for IIL this product is in the range 0.1 to 0.7 pJ. And while TTL gates can be packed with a density of about 20 gates per square millimeter, IIL gates allow a packing density in the range from 120 to 200 gates per square millimeter.

At the present writing (summer 1976) IIL logic is not commercially available in small-scale integration. Packages containing one or several gates, as available in RTL and in other logic families, have not been marketed. On the other hand, medium- and large-scale-integration chips are available.

Basic configuration of IIL The DCTL gate shown in Fig. 4.2-1 and the RTL gate shown in Fig. 4.1-1 do indeed look like gates. Each exhibits multiple inputs and a single output, as expected of a gate. (The other families of logic discussed in succeeding chapters also look like gates.) On the other

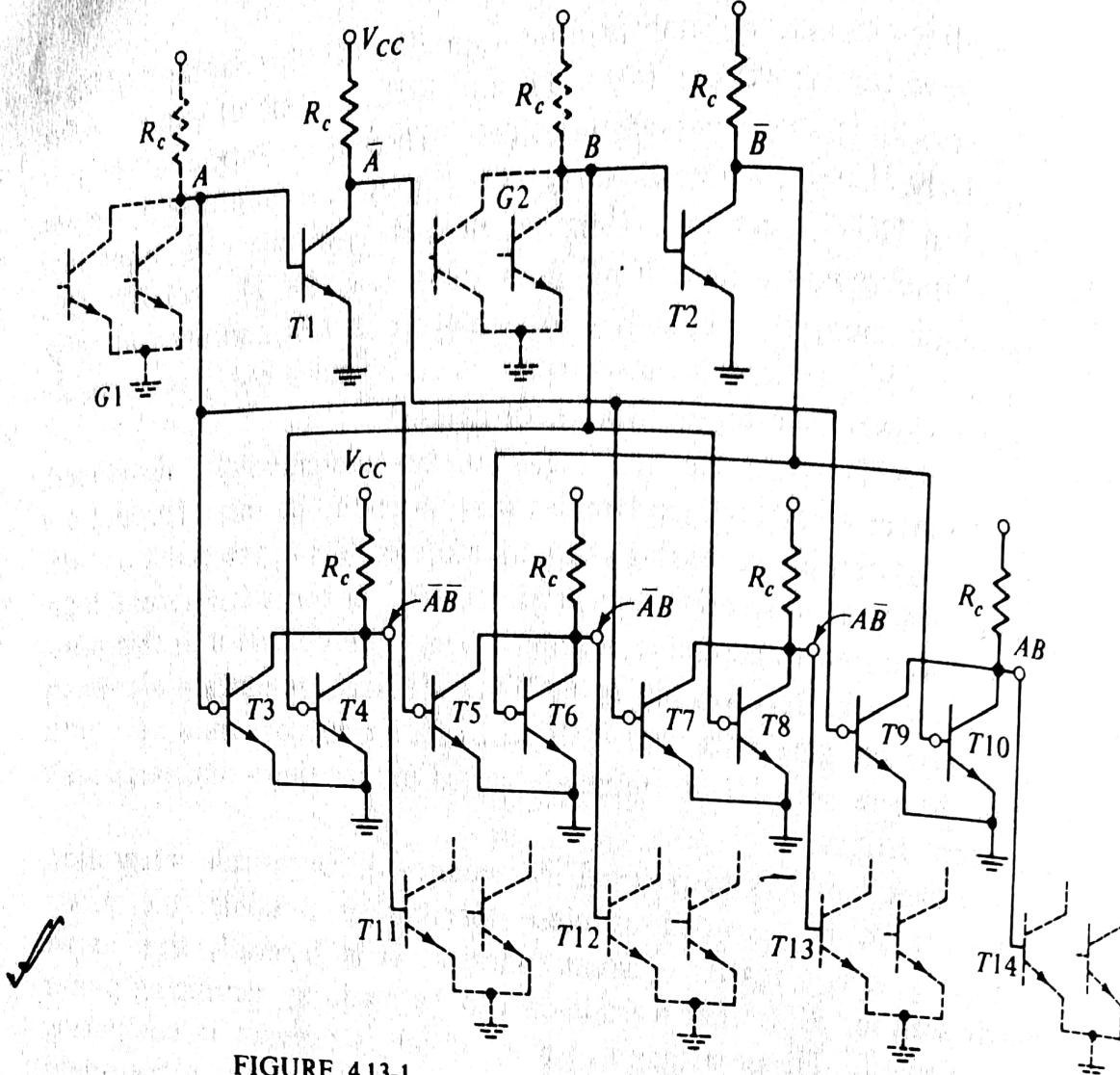


FIGURE 4.13-1
A DCTL gate structure which generates AB , $A\bar{B}$, $\bar{A}B$, and $\bar{A}\bar{B}$ from the logical variables A and B .

hand, the basic structure of an IIL exhibits a single input and multiple outputs, and some explanation is in order.

To pursue the matter, by way of illustration, let us consider that we have two logical variables to deal with, A and B , and that we need to generate the functions AB , $A\bar{B}$, $\bar{A}B$, and $\bar{A}\bar{B}$. We shall use DCTL logic. The variables A and B may themselves be functions of still other variables and hence will themselves be initially available as the outputs of other DCTL gates, $G1$ and $G2$, as shown in Fig. 4.13-1. Since these gates are external to the system we are to assemble, we have drawn them with dashed lines. (Two transistors are indicated in $G1$ and $G2$, but of course the number is arbitrary.)

We need \bar{A} and \bar{B} , and these functions of A and B are generated by the single-input gates involving transistors $T1$ and $T2$. Finally, with A , B , \bar{A} , and \bar{B} available, the functions required are generated by four two-input DCTL gates. The generated functions may themselves serve as inputs to other gates. To allow for this possibility we have connected the output $\bar{A}\bar{B}$ to the base of $T11$, the output $\bar{A}B$ to the base of $T12$, etc., these transistors, $T11$ through $T14$, providing one input of these other external gates.

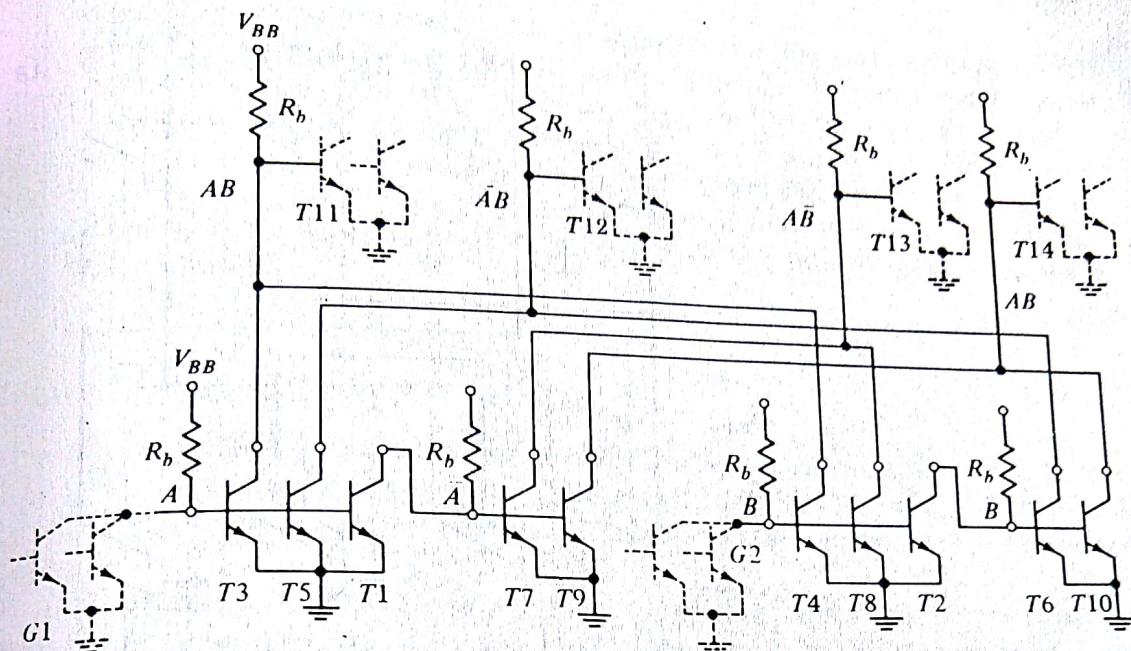


FIGURE 4.13-2

Figure 4.13-1 redrawn to group transistors with common base connections.

We have redrawn Fig. 4.13-1 to appear now as in Fig. 4.13-2. In redrawing that part of the figure of interest to us, i.e., the part drawn in solid lines, we have reorganized the drawing to group together transistors with common base connections. In Fig. 4.13-1 the transistors grouped together have common collector connections. Further, in going from Fig. 4.13-1 to Fig. 4.13-2 we have adopted a different interpretation of the function of the resistors. In Fig. 4.13-1 we view the resistors as common-collector resistors and accordingly label them R_c . In Fig. 4.13-2 the resistors are viewed as common-base resistors and are labeled R_b . Thus the resistor which was previously viewed as the common-collector resistor of the transistors of gate G_1 is viewed instead as the common-base resistor of transistors T_1 , T_3 , and T_5 . Correspondingly, in one case the voltage to which the resistor has been returned is called V_{cc} and in the other it is called V_{BB} .

We have redrawn Fig. 4.13-2 to appear as in Fig. 4.13-3. Here groups of transistors with common emitters and bases (such as T_3 , T_5 , and T_1) have been represented as a single multiple-collector transistor. The basic structure of the IIL gate is a transistor with multiple collectors and a single emitter together with a mechanism for supplying base current. The logic operation performed, as in DCTL, is the NOR operation. Thus, if a collector of a gate whose input is A is connected to a collector of a gate whose input is B and the joined collectors are in turn connected to the base of another gate, the logic that appears at the base is $\overline{A} + \overline{B}$.

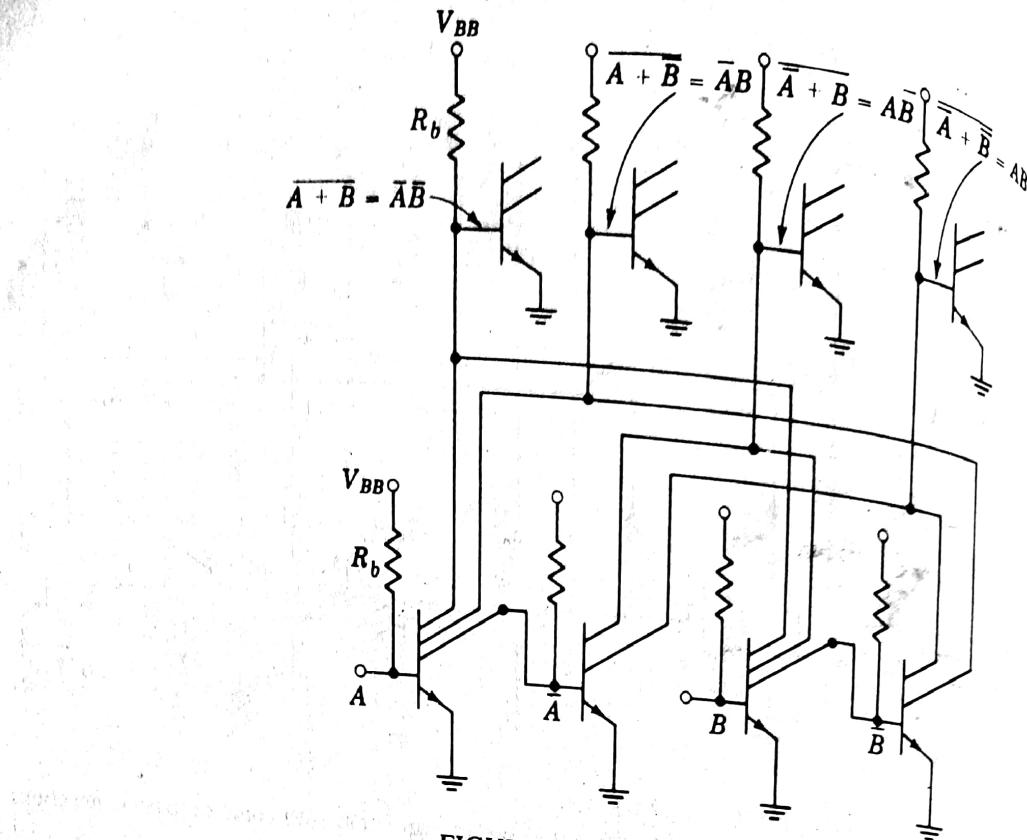


FIGURE 4.13-3

Figure 4.13-2 redrawn with multiple-collector transistors.

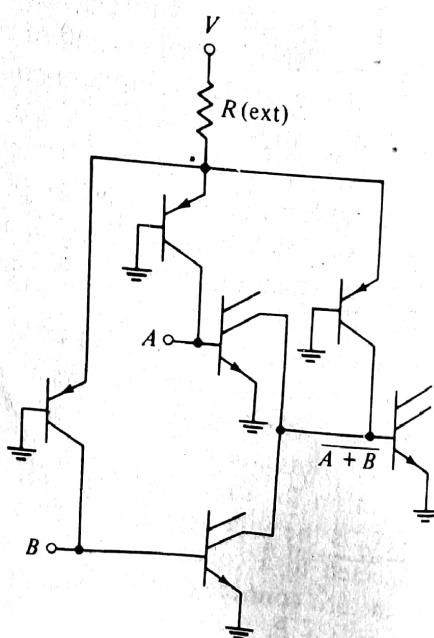


FIGURE 4.13-4

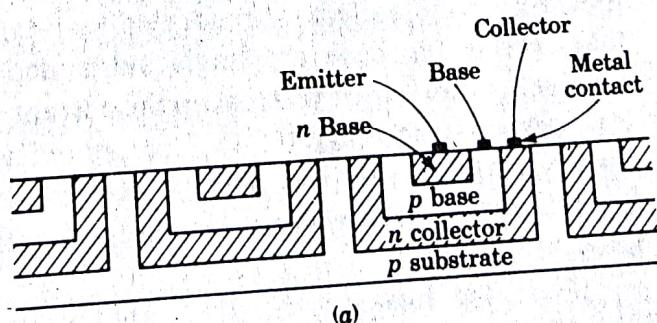
The basic configuration of IIL gates.

Up to this point we have made it appear that the base current of the multicollector transistors is supplied through a resistor. We now need to take note of the fact that actually this current is supplied through a transistor. Thus, finally, the basic configuration encountered in IIL appears as in Fig. 4.13-4. The transistor, it turns out, can be incorporated in the structure of the integrated circuit in a manner which uses much less chip area than would be required by a resistor. Observe that, for reasons to be discussed later, this added transistor is of the *pnp* type.

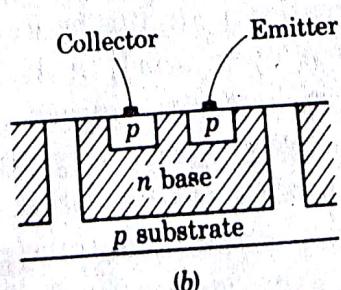
4.14 PHYSICAL LAYOUT OF IIL

In order to appreciate the features of IIL which account for its comparative merits, it is necessary to give some consideration to the physical construction of an IIL integrated circuit. We shall consider the matter in a simplified manner.

In integrated circuits, for reasons concerned with the technology of fabrication, transistors are of the *npn* type. The layout of an array of transistors is shown in Fig. 4.14-1a. (In Fig. 4.14-1 for simplicity we have deliberately omitted a number of features needed for the proper operation of the device but not essential to our discussion.) The substrate is *p*-type silicon, and the *p*-type material extends upward from the substrate to the integrated-circuit surface to provide isolation from one transistor to the next. The collector, base, and emitter are *n*-type, *p*-type, and again *n*-type, respectively, as shown. Isolation is effected by arranging that the substrate shall be always negative with respect to the collector. The various parts of the transistors are formed by diffusions of impurities from the surface of the integrated circuit. The collector is relatively lightly doped, the base doped more heavily, and the emitter doped quite heavily.



(a)



(b)

FIGURE 4.14-1
(a) The physical structure (simplified) of an integrated-circuit transistor. (b) The physical structure of a *pnp* lateral transistor.

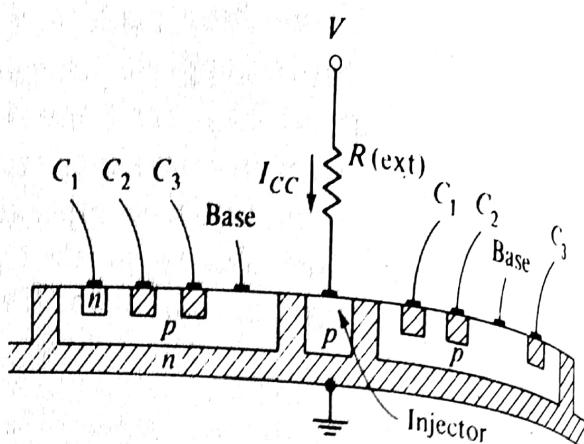


FIGURE 4.14-2
The physical structure of the basic gate configuration in IIL.

Both the geometry of the structure and the doping serve to ensure that the common-base gain α_N shall be close to unity and that $h_{FE} = \alpha_N/(1 - \alpha_N)$ shall be large. Since the emitter is doped much more heavily than the base, the carriers which cross the emitter junction are predominantly electrons. It is important that such be the case since holes crossing from base to emitter constitute an emitter current which will not be collected at the collector junction. Since the base is very thin, very few of the electrons injected into the base will be lost in the base as a result of recombination. Finally, we note that the emitter is almost surrounded by the collector, i.e., when viewed from the emitter, the collector subtends a large angle. As a consequence, an electron leaving the emitter, from no matter what point and in which direction, can hardly fail to reach the collector. For all these reasons we find $\alpha_N \approx 0.98$ or even higher. In the transistor configuration of Fig. 4.14-1a the axis of symmetry of current flow is in the vertical direction. Hence such a transistor is called a *vertical transistor*.

The transistor structure can be modified to allow a *pnp* transistor. Such a transistor is shown in Fig. 4.14-1b. The substrate is again *p* type. However the layer above the substrate becomes not the collector but the base. As shown, the emitter and collector are formed by *p*-type diffusions into the base. Observe that in the *pnp* case the angle subtended by the collector at the emitter is relatively small. For this reason the current gain h_{FE} of the *pnp* transistor is rather low, being in the range 0.5 to 5 compared with 50 to 150 for an *npn* transistor. Finally we note that the general direction of current flow is horizontal, i.e., to the side rather than vertical, hence the configuration of Fig. 4.14-1b, is called a *lateral transistor*.

Turning now to the IIL gate, we see the structure of such a gate in Fig. 4.14-2. (In this figure, we have again taken some liberties in the direction of simplification.) In this figure we display two three-collector gates side by side. The lower *n* layer, which in the conventional integrated-circuit transistor is the collector, is here the emitter. Since all the emitters in all the transistors operate at the same voltage (ground), a *p*-type isolation, necessary in Fig. 4.14-1a, is not required in the circuit of Fig. 4.14-2. In the conventional transistor the small *n* region, embedded in the *p*-type base, is the emitter. In the IIL transistor these small *n* regions are the multiple collectors. However, in the IIL transistor

the relative doping is geometrically but not functionally the same as in the conventional transistor; i.e., while in the conventional transistor the emitter is most heavily doped and the collector least heavily doped, in the IIL transistor the situation is reversed. Hence the IIL transistor operates in a mode which we would describe as the *inverse* mode if we were dealing with a conventional transistor. Accordingly we expect that the current gain for the IIL transistor will be low. Such is indeed the case. Yet it turns out to be possible to get current gains as large as 5 and even higher. A current gain of this magnitude is entirely adequate; for, as can be seen in Fig. 4.13-1, each collector needs to provide for a fan-out of only 1.

As indicated in Fig. 4.14-2, the location of the base connection for the *npn* transistor is not the same from transistor to transistor. This feature is useful in that it allows base connections and collector regions to be located as required to accommodate the necessary interconnections.

Figure 4.14-2 also shows the *pnp* transistor which supplies base current to the *npn* transistor (see Fig. 4.13-4). The *p* region marked "injector" is the emitter of this transistor, its collector is the *p*-type base of the *npn* transistors, and its base is the *n*-type emitter of the *npn* transistor. Altogether the two transistors, one *npn* and one *pnp*, are formed with only four separate regions, the two transistors using two regions in common. For this reason IIL is also called *merged-transistor logic* (MTL).

Observe that the *pnp* transistor through which base current is injected into the *npn* transistor is pictured in Fig. 4.14-2 as serving two transistors on each side. Note also that the *pnp* transistors are *lateral* transistors. Current I_{cc} is supplied for the injector from a supply source V through an external resistor R . The voltage from the *p*-type injector region to ground is the voltage across a forward-biased junction and turns out in the present case to be about 0.85 V. Fortunately this injector-to-ground voltage tracks very well from injector to injector throughout the integrated-circuit chip. Hence it turns out to be possible to operate all the injectors in parallel so that all the injector current required by a chip can be supplied through a single external resistor.

Adjustability of speed We have seen that in RTL gates it is possible to sacrifice power dissipation for the sake of an improvement in speed. This trade-off is effected by changing the sizes of the resistors. Small resistors allow larger currents, so that capacitances can charge more rapidly albeit at the expense of greater power dissipation. What is to be noted here is that different speeds are associated with *different* integrated-circuit chips. In IIL, as we shall now see, it turns out that the trade-off between speed and power can be effected on a single chip by the simple expedient of changing the current I_{cc} injected into the chip.

Since the voltage at the injector is constant (≈ 0.85 V), the input power is proportional to the average input current I_{cc} . (On a large-scale-integration chip we may reasonably expect that a nominally fixed fraction of the transistors will be conducting at any one time and hence that I_{cc} will be rather constant.)

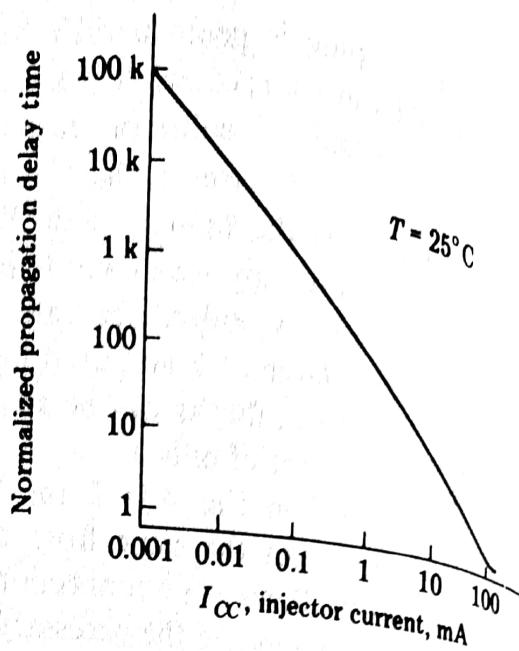


FIGURE 4.14-3
Normalized propagation delay time versus
injector current.

A fraction I_{cc}/n of this current will be available, on the average, to operate a gate, n being the average number of gates which are conducting. At low current levels the propagation-delay time is principally the time required to charge junction and parasitic capacitors. The time required to charge these capacitors is *inversely proportional* to the available charging current I_{cc}/n . Accordingly the speed-power product is constant independently of I_{cc} . Increasing I_{cc} (by increasing V or decreasing R in Fig. 4.14-2), we can decrease the propagation delay at the expense of a proportionate increase in dissipation.

At medium current levels the principal source of propagation delay is the need to establish and remove the excess minority-carrier base charge in the transistors (see Sec. 1.17). This charge is proportional to the transistor current available to establish or remove it, and hence the propagation delay is independent of the current. Thus, in this current range, an increase in I_{cc} will increase the dissipation without reducing the delay.

At high current levels the transistors are driven into saturation. As discussed in Sec. 1.18, in saturation the stored base charge increases more than in proportion to transistor current. Hence, in this current range an increase in I_{cc} will not only increase the dissipation but will also increase the delay.

Figure 4.14-3 shows a plot of the normalized propagation delay time as a function of I_{cc} for the Texas Instrument (SBPO400) IIL chip. In the range of I_{cc} from 0.001 to 100 mA we can trade off dissipation and speed. Beyond about 100 mA an increase in dissipation yields no continuing decrease in speed. While the plot is not carried to the high-current region, at such high currents the plot would no doubt have a positive slope.

4.15 AN IIL DECODER

In Fig. 4.14-2 we show an injector serving two transistors. Actually a single injector can serve many transistors. When this is intended, the injector is

extended into a long strip parallel to the surface of the chip and is referred to as an *injector rail*. The transistors are fabricated on both sides of the rail and extend perpendicular to the rail.

As an example of an alternative layout we have the 3-bit decoder shown in Fig. 4.15-1. The function of decoders and their logic is discussed in Sec. 12.9. It will be sufficient here to note that the present decoder has as input the three logic variables A , B , and C and is intended to make available on eight separate output lines the eight minterms (see Sec. 3.17) of the input variables. Hence, at any time, only one output line will be at logic 1; all others will be at

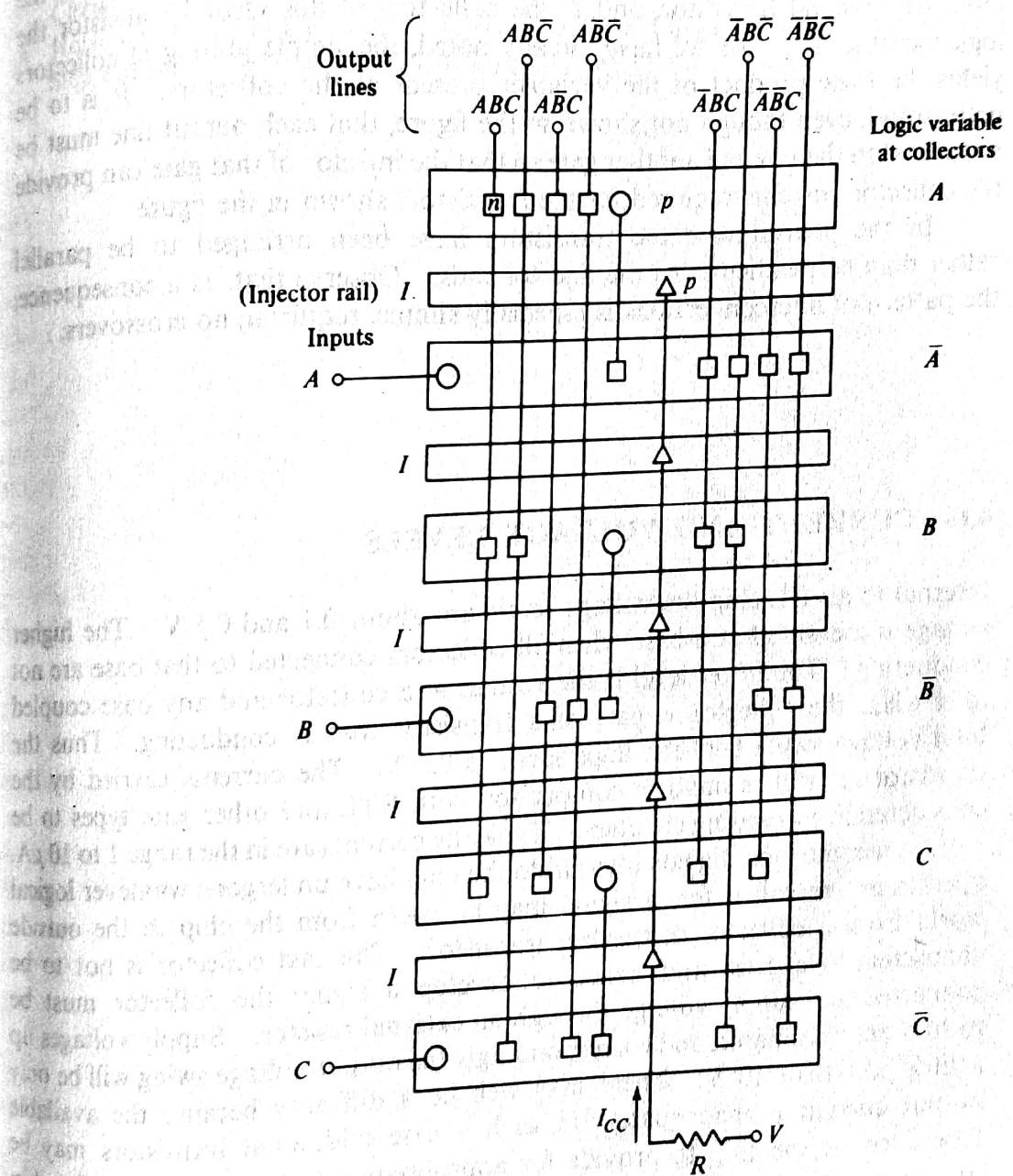


FIGURE 4.15-1
A 3-bit IIL decoder.

logic 0. The line selected to be at logic 1 is determined by the logic levels of the inputs.

The view shown is seen looking down at the surface of the chip. The common *n*-type emitter of the *npn* transistors (see Fig. 4.14-2) (which is also the base of the injector transistor) is not explicitly shown. We do see the *p*-type injector rail and the *p*-type base of the *npn* transistors (which is also the base of the injector transistor). Connections for the injected current are shown as triangles on the injector rail. The base connections are shown as circles and the collectors as squares. To the right of the figure are specified the logic variables present at the collector on each multicollector transistor. Thus the transistor whose input is *A* has \bar{A} at each collector. One of these collectors provides \bar{A} at the input to a second transistor, and at the collectors of this second transistor the logic variable is *A*. As we have already noted, the simple joining of collectors yields the logic product of the variables present at the collectors. It is to be understood, even though not shown in the figure, that each output line must be connected to the input of another gate so that the injector of that gate can provide the collector currents required for the transistors shown in the figure.

In the present case the transistors have been arranged to be parallel rather than perpendicular to the injector rails. Observe that, as a consequence, the pattern of interconnections is especially simple, requiring no crossovers.

4.16 CURRENT AND VOLTAGE LEVELS

Internal to an IIL chip the voltage levels are about 0.7 and 0.1 V. The higher voltage is measured at a base when all collectors connected to that base are not conducting. The lower level is the voltage at a collector and any base coupled to it when the collector is part of a transistor that is conducting. Thus the total voltage swing between logic levels is 0.6 V. The currents carried by the transistors are rather small in comparison with RTL and other gate types to be considered in succeeding chapters. Typically currents are in the range 1 to 10 μ A.

When the logic signals internal to the chip have undergone whatever logical operations are called for, a signal may be taken from the chip to the outside world from a collector of the last transistor. This last collector is not to be connected to a base and hence to develop a signal the collector must be connected to a supply voltage through an external resistor. Supply voltages up to 10 V are reasonable, and correspondingly the output-voltage swing will be only a little less than 10 V. There may well be a difficulty because the available output current is inadequate. In such a case additional transistors may be fabricated on the chip to provide for appropriate interfacing between the chip and its external load.