VLSI Systems

First Class Test BCSE 4th year Full marks: 30

1. What is difference between verification and testing in VLSI design?
2. For an npn transistor with emitter grounded draw the I_c versus V_{CE} characteristics. Show the saturation region. Generally the term 'saturation' implies something becoming constant, which one is becoming constant here and with respect to whom?
3. What are the advantages of CMOS over MOSFET? What are the disadvantages of CMOS design?
4. As in static condition no current flows through CMOS, how do the power dissipation occur?
5. In a NMOS transistor find out the current at different conditions- cutoff, liner, satuaration.

Deduce the characteristics of an NMOS enhancement mode transistor for t_{ox} = 100 Å, μ= 350 cm^2 /V sec, V_t = 0.7 V, V_{gs} = 5V, W/L = (last digit of your roll number) mod 2 +1.

6. What are its advantages and disadvantages of single complex cell designs?
7. What is the significance of stick diagram, as applicable in the design of VLSI? What is its advantage and limitation?
8. Compare silicon versus Germanium in fabrication. What is the role of silicon dioxide in fabrication?

4+3+4+2+7+2+4+4