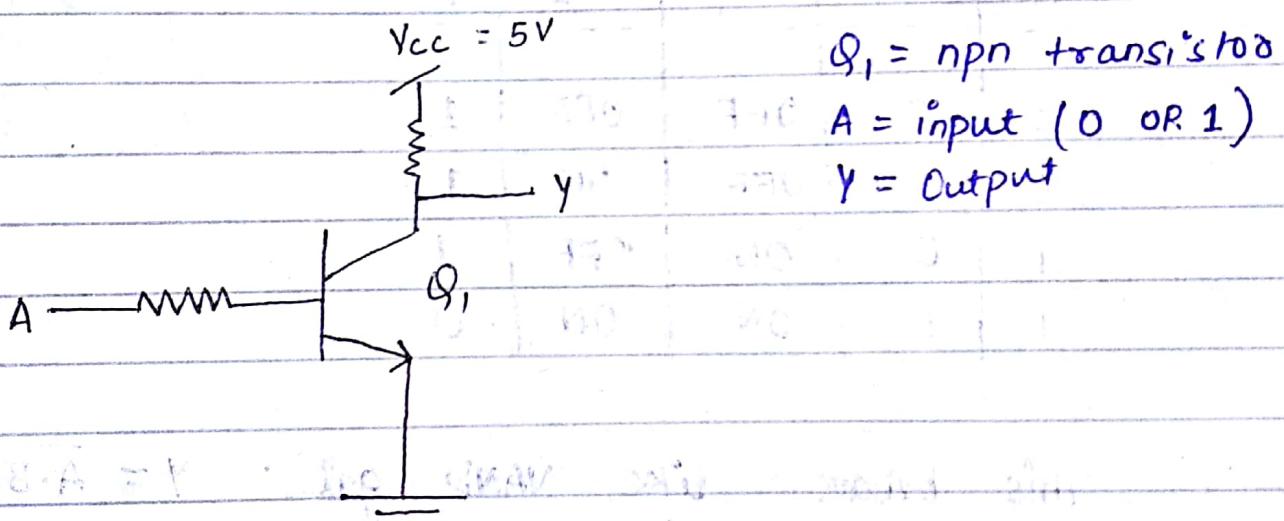


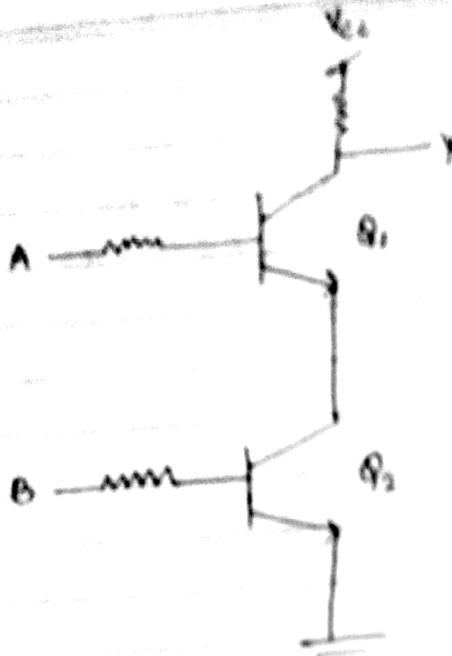
Logic Family

1. RTL : Resistor Transistor Logic



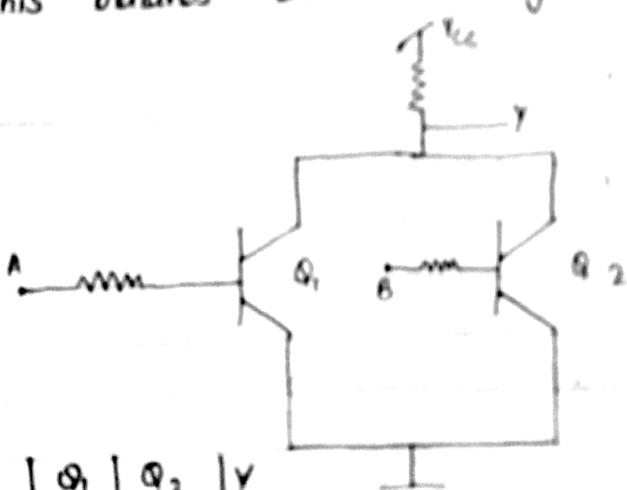
A	Q_1	y
0	OFF	1
1	ON	0

This circuit behave like NOT gate or inverted circuit.



A	B	Q_1	Q_2	Y
0	0	OFF	OFF	1
0	1	OFF	ON	1
1	0	ON	OFF	1
1	1	ON	ON	0

This behaves like NAND gate $Y = \overline{A \cdot B}$



A	B	Q_1	Q_2	Y
0	0	OFF	OFF	1
0	1	OFF	ON	0
1	0	ON	OFF	0
1	1	ON	ON	0

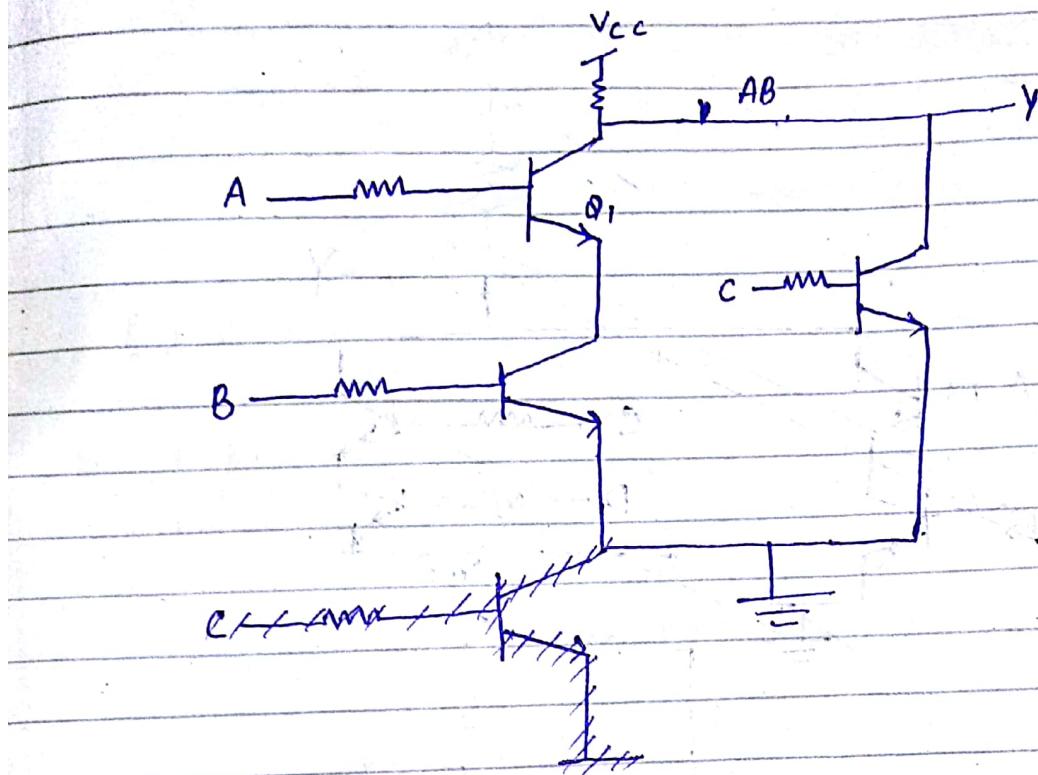
This circuit will behave like NOR gate

$$Y = \overline{A + B}$$

Series : $A \cdot B \cdot \dots \cdot x_n$

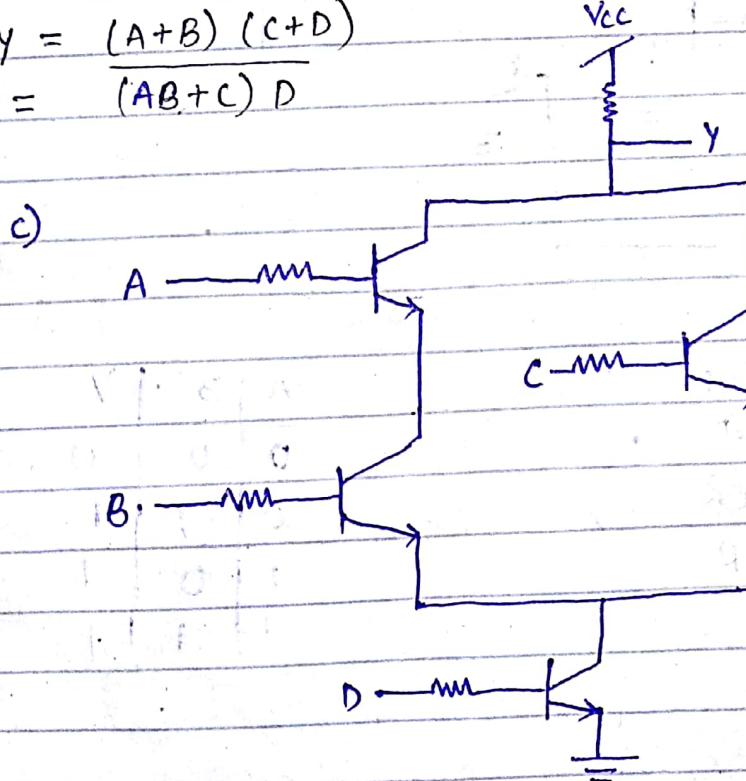
parallel: $A + B + \dots + x_n$

1. Draw the circuit if a) $y = \overline{AB} + C$
= $\overline{AB} \cdot \overline{C}$



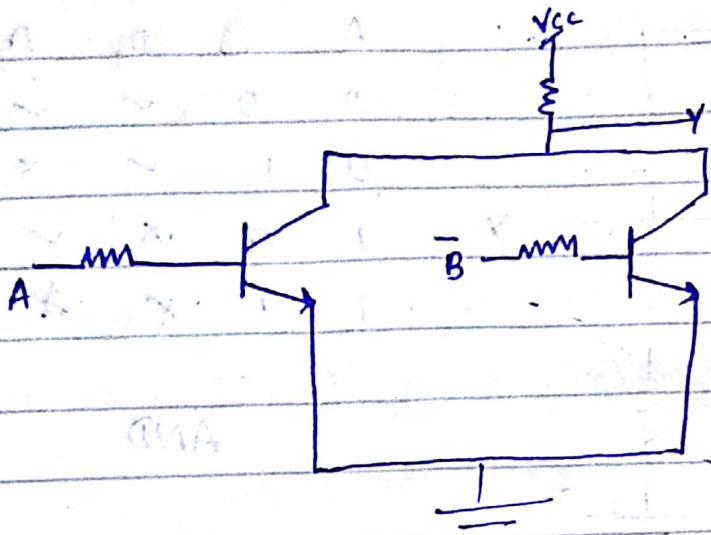
b) $y = \overline{(A+B)} \cdot (C+D)$

c) $y = \overline{(AB+C)} \cdot D$

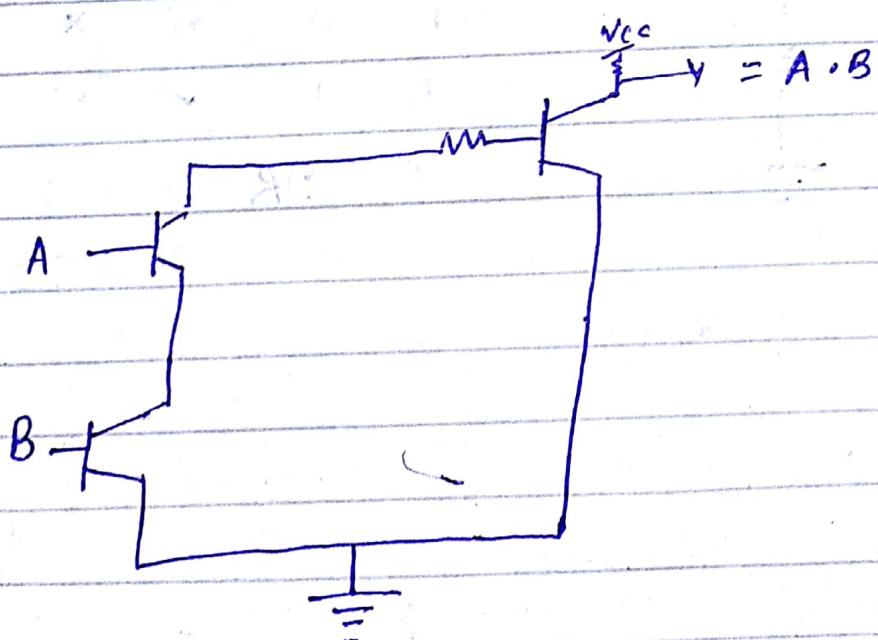
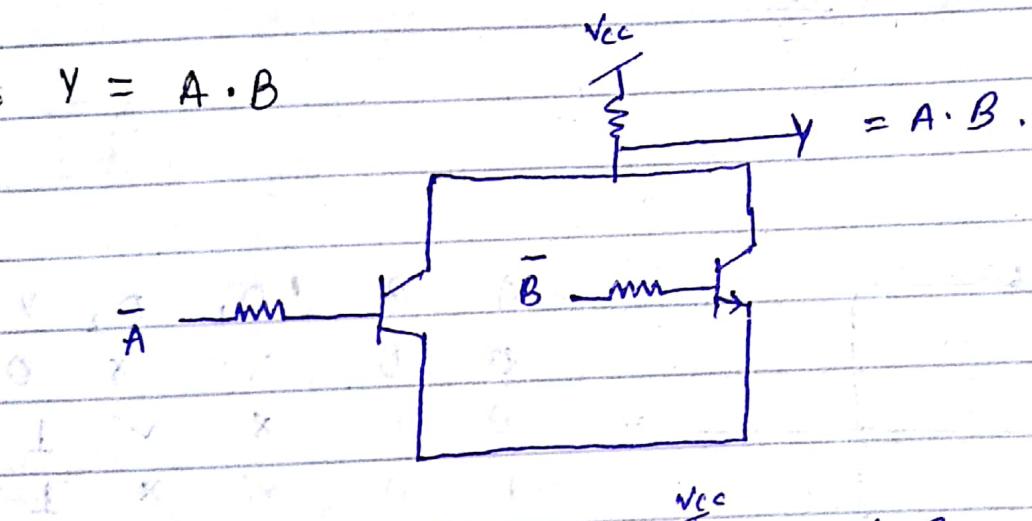


$$2. \quad Y = \bar{A}B$$

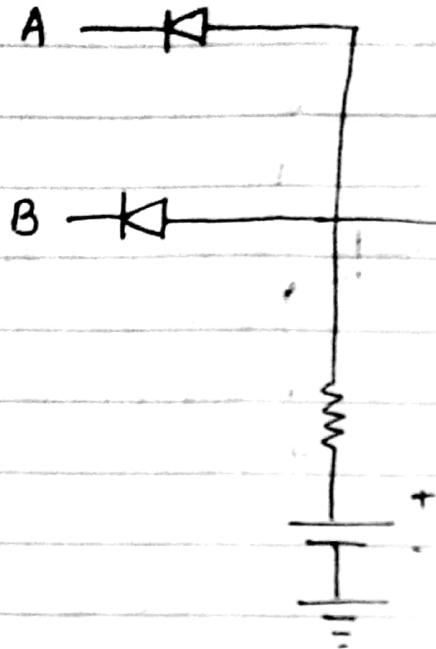
$$\bar{Y} = \cdot \overline{\bar{A}B} = \bar{\bar{A}} + \bar{B} = A + \bar{B}$$



$$3. \quad Y = A \cdot B$$

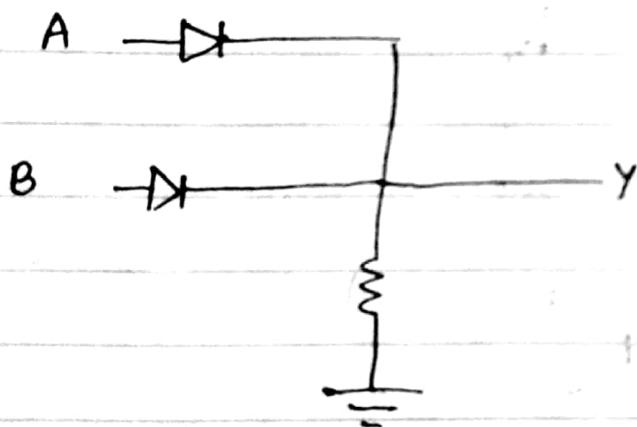


Diode Logic



A	B	D ₁	D ₂	Y
0	0	✓	✓	0
0	1	✓	✗	0
1	0	✗	✓	0
1	1	✗	✗	1

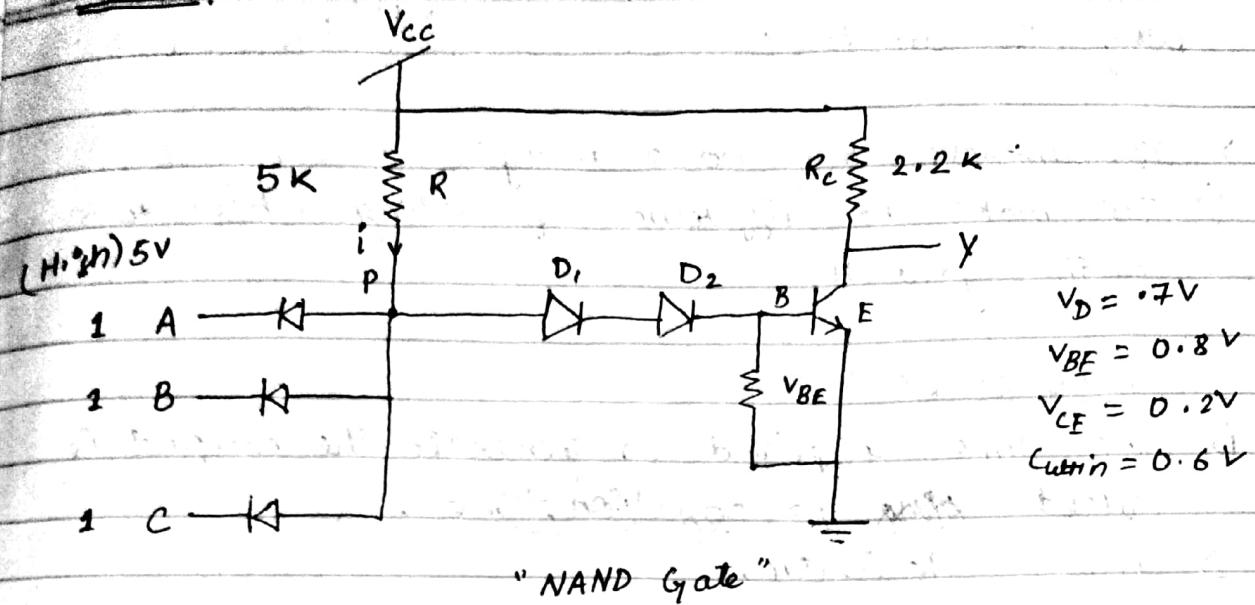
AND



A	B	D ₁	D ₂	Y
0	0	✗	✗	0
0	1	✗	✓	1
1	0	✓	✗	1
1	1	✓	✓	1

OR

DTL. (Diode transistor).



Noise immunity feature is very low in diode.
 " " " high in DTL

$$V_{D1} = 0.7 \text{ V} \quad \text{Minimum voltage required}$$

$$(0.7 + 0.7 + 0.8) \text{ V} = \text{to ON the transistor}$$

$$V_p = 2.2 \text{ V}.$$

H High

$$I = \frac{V_{cc} - V_p}{5k}$$

$$= \frac{5 - 2.2}{5k} = \frac{2.8}{5k} = 0.56 \times 10^{-3}$$

$$= 0.56 \text{ mA}$$

$$V_{CE} = V_o = 0.2 \text{ V.}$$

H low, the $V_o = 0.2$

$$V_p = 2.2$$

$$V_o = 5 \text{ V} \approx 5 \text{ V.}$$

$$\begin{aligned} A + B &= 0.2 + 0.7 = 0.9 \\ &= 0.2 + 0.7 \end{aligned}$$

Why Two diode ??

→ KJF

- 1) To improve the noise margin.
- 2) To make the difference of voltage b/w two path greater.

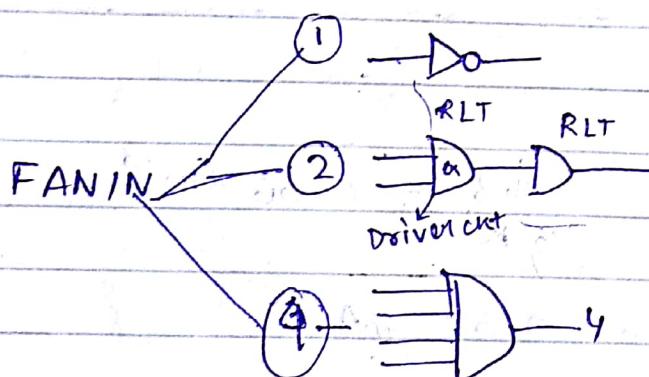
Parameters :

- 1) The time required to generate the output is called ~~time~~ propagation time.
- 2) Power decipation:

FAN IN and FAN OUT

The no. of similar gates which can be driven by a gate.

FAN IN:



(Maximum, it can hold)

No number of logic gate can be connected at the output of any logic gate

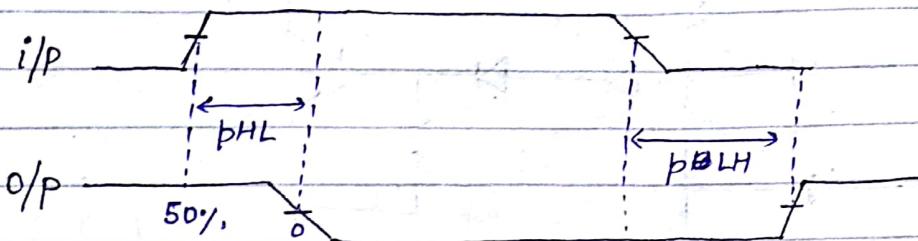
160 mA = Total current / output

16 mA = Each load current.

$$\text{Fan out} = \frac{160 \text{ mA}}{16 \text{ mA}} = 10$$

The propagation delay or speed of operation.

The speed of a digital ckt is specify in term of propagation time. The I/O waveform of logic gates are shown in Fig. A. The delay times are measured b/w the 50% voltage level of input and output waveform.



Power dissipation.

This is the amount of power dissipated in an IC. Determined by the current I_{cc} i.e. drawn from V_{cc} . And given by, $V_{cc} \times I_{cc}$

Figure of merit

Figure of merit = Propagation delay time * Power

The unit of figure of merit is picosecond (ps). Propagation delay is measured in nanosecond (ns). Power dissipation milliwatt (mW).

Bipolar : BJT (Bipolar devices)

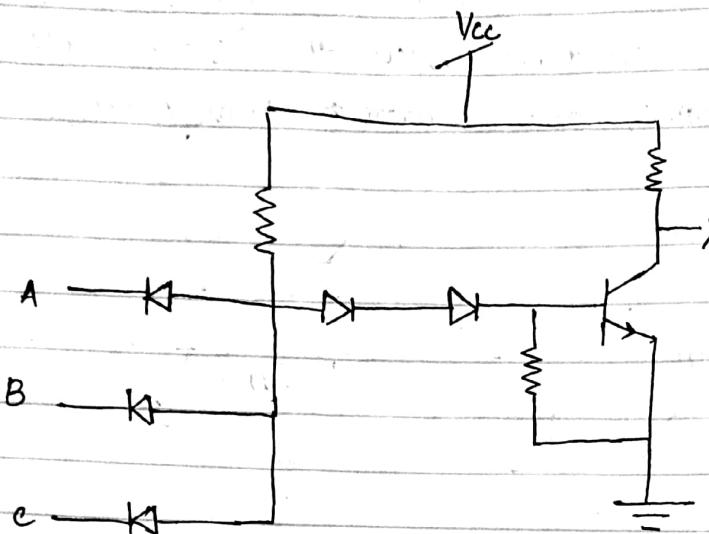
Unipolar : N-MOS, P-MOSFET, CMOS

Bipolar → Saturated
→ Unsaturated

The saturated bipolar logic families are :

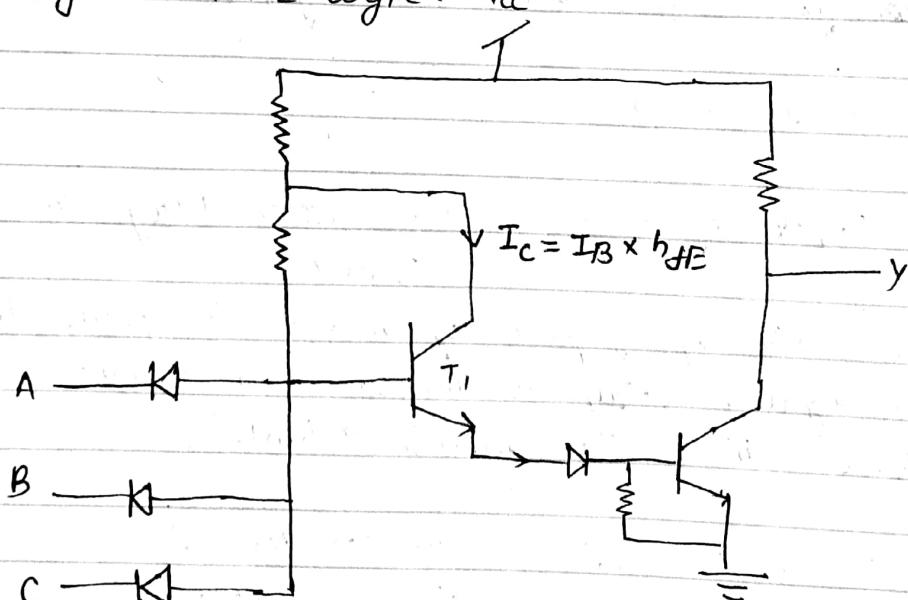
RTL, DCTL, IIL, DTL, HTL, TTL

Bipolar logic families are : ECL, SchotTKy TTL
(Emitter coupled logic)



$$h_{FE} = \frac{I_C}{I_B} \quad I_C = I_B \times h_{FE}$$

Modified DTL logic: Vcc

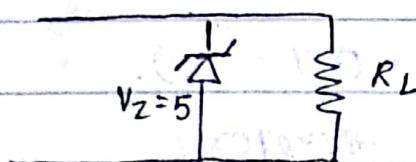


In Modified DTL logic,

Fan Out is better than DTL logic.

HTL (High threshold logic) (High Power devices)

Due to presence of electric motto, all ON-OFF control CKT ~~are~~ and high voltage switch in an industrial ~~department~~ environment, the noise level is quite high and logic families like DTL, RTL and diode family are not perform properly.

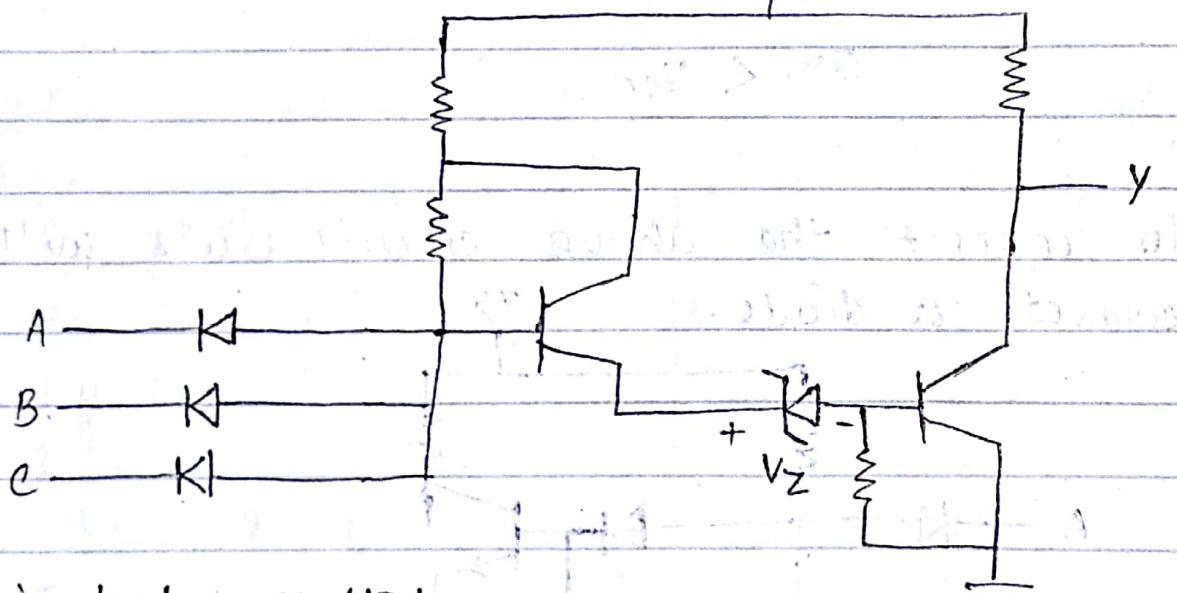


First,

$$V_{in} < 5 \text{ V}$$

$$V_{in} > 5 \text{ V}$$

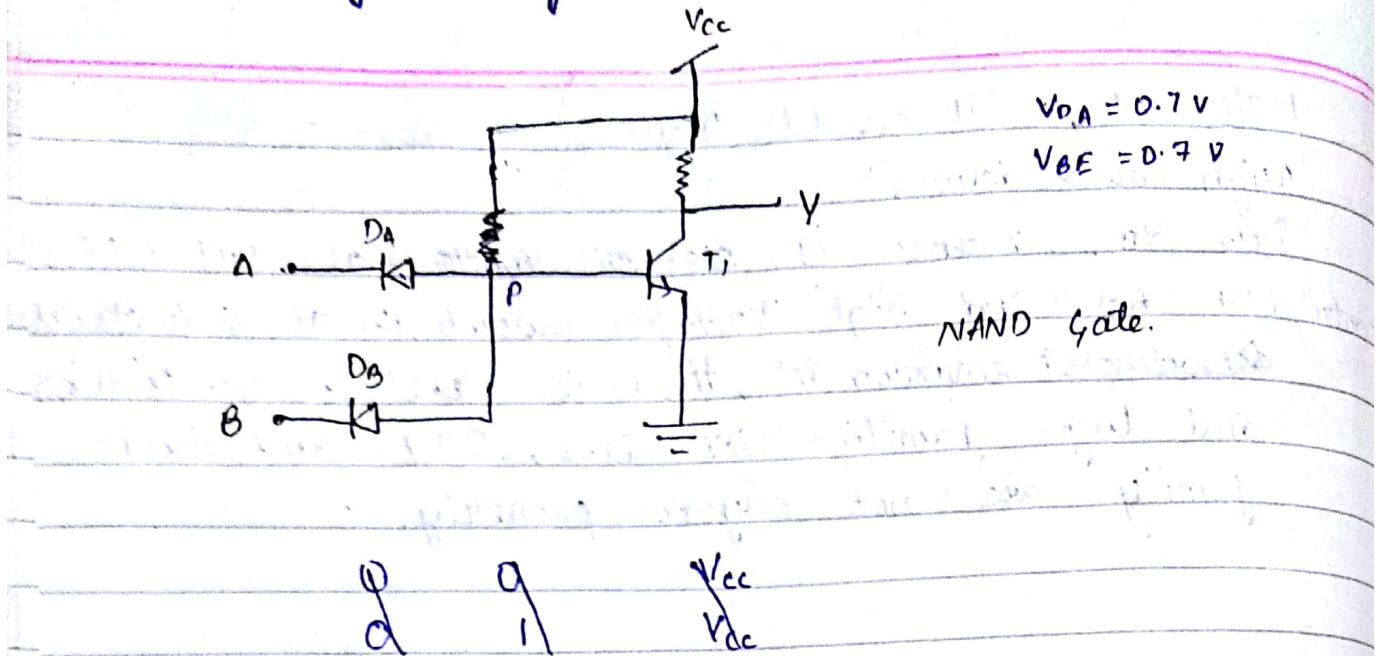
Then the voltage across R_L is 5V



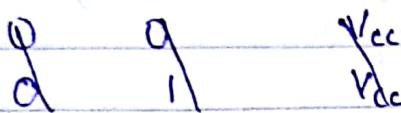
Disadvantage of HTL

1. The propagation delay time is affected due to large resistance value.

Practically wrong Ideally correct.



NAND Gate.



At Low Voltage (0.2)

At pt. p. Voltage drop = $0.2 + 0.7 = 0.9$.

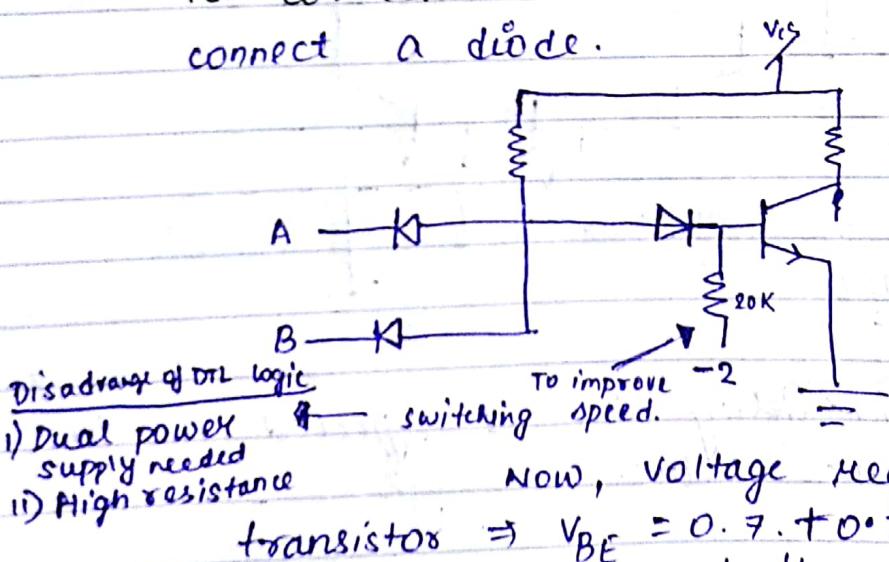
which is always > 0.7 therefore

T_1 is always ON. and it will give $V_{CE} = 0V$.

At high voltage

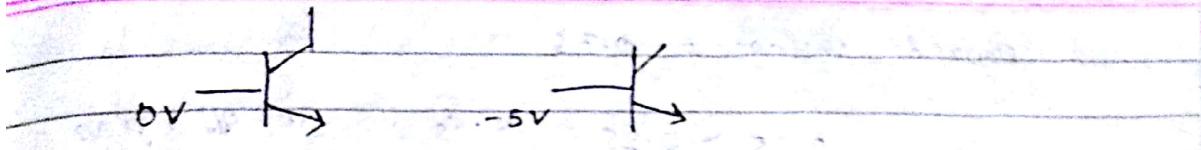
$$5V < V_{CE}$$

To correct the above circuit: We will connect a diode.



NOW, voltage req. to ON the

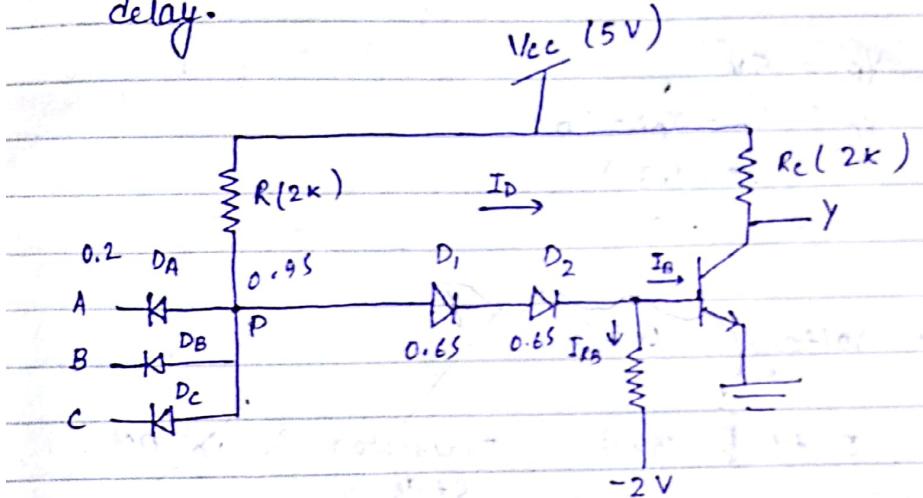
$$\text{transistor} \Rightarrow V_{BE} = 0.7 + 0.7 \\ = 1.4$$



-5V will take less time and will be faster.

The propagation delay of DTL circuit

The propagation delay in DTL's gate are of the order of 30 - 80 ns (nanosecond). The turn OFF delay is generally larger than turn ON delay.



Find out the output voltage when inputs are

- 0
- 1

i) The voltage drop across the diode is 0.65 V

$$\text{Value of } V_{CE} = 0.2$$

$$\text{Value of } V_{BE} = 0.75 \text{ V}$$

$$V_{DA} = V_{BB} = 0.75$$

~~$$V_P = 0.2 + 0.2 + 0.2 + 0.75 + 0.65 + 0.65$$~~

$$\begin{array}{r} 0.2 \\ + 0.75 \\ + 0.65 \\ + 0.65 \\ \hline 2.3 \end{array}$$

At low V_{OI} ,

$$V_P = 0.2 + 0.75 \text{ V} = 0.95 \text{ V}$$

$$\begin{aligned} (\text{Base terminal of transistor}) \quad V_B &= V_P - V_{D1} - V_{D2} \\ &= 0.95 - 0.65 - 0.65 \\ &= -0.35 \text{ V} \end{aligned}$$

Required Voltage = 0.75

$0.75 > 0.35$ It is in cut-off region
or off state.

$$I_{RB} = \frac{-0.35 + 2}{20k}$$

$$\cancel{20k} = 0.08 \text{ mA}$$

output : v_{cc}

A high voltage,

$$V_p = 5V$$

$$\begin{aligned} v_o &= V_p - V_{D1} - V_{D2} \\ &= 5 - 1.3 \\ &= 3.7 \end{aligned}$$

Required Voltage = 0.75

$$0.75 < 3.7$$

Transistor is in ON state.

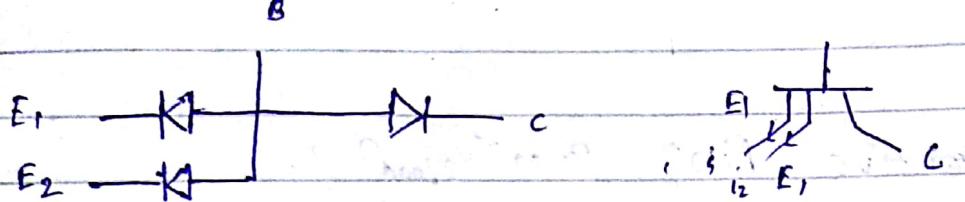
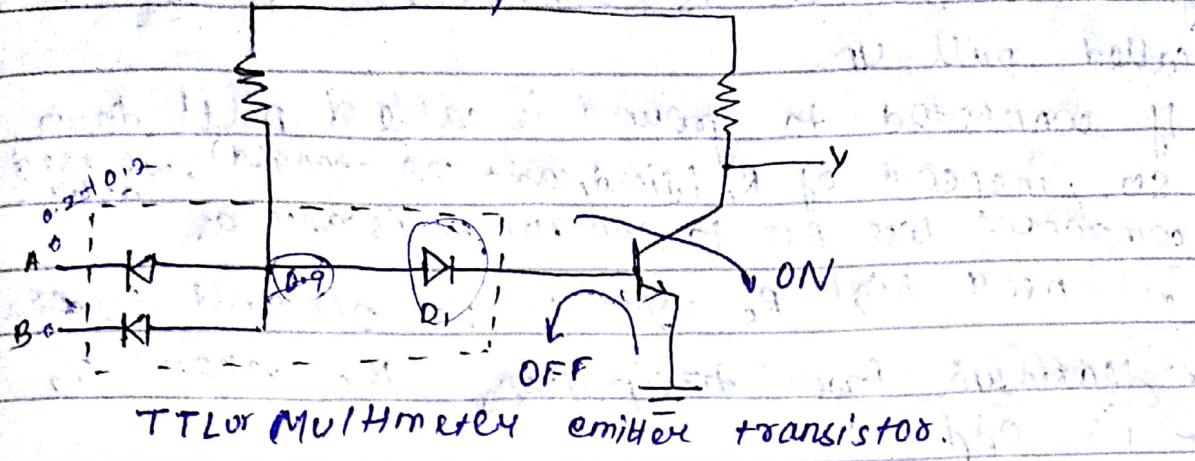
$$I_{RB} = \frac{3.7 + 2}{20k}$$

$$\begin{aligned} &= \frac{5.7}{20,000} = 2.85 \times 10^{-4} \text{ A} \\ &= 0.65 + 0.65 + 2.05 = 0.28 \text{ mA} \end{aligned}$$

$$I_{RB} = \frac{0.75 + 2}{20k} = 0.14 \text{ mA}$$

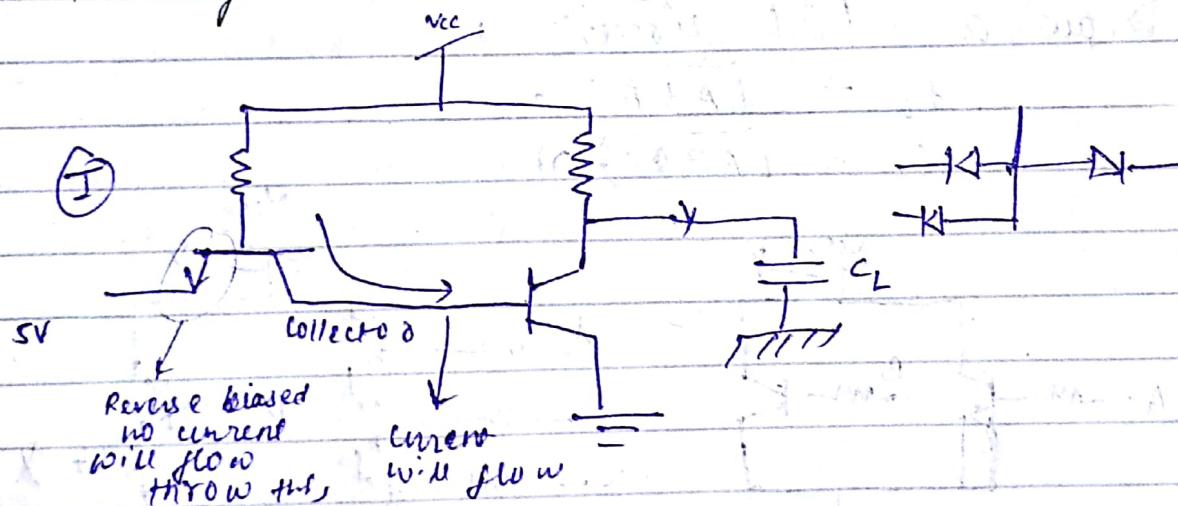
$$I_D = \frac{V_{cc} - V_p}{R} = \frac{5 - 2.05}{2k} \approx 0.14 \text{ mA}$$

$$I_B = I_D - I_{RB} = 0.26 \text{ mA}$$



Transistor ON = Collector current = Emitter

Reversely active transistor



From (i) when T_1 is high T_1 is reversely active transistor.

From (f), C_L is from load, $\tau = R_C C_L$

If R_C is reduced, I_C increases rapidly and (ii) T_2 cannot work properly in saturation mode

* Need to reduce R_C . So, C_1 is fixed.

~~Transistor~~



If a compound is connected to V_{CE} it is called pull up.

If connected to ground is called pull down so, instead of R_C (fixed, can't be changed), we used active component like BJT to control resistance as we need high R_C when T_2 is ON and low R_C when T_2 is OFF.

~~Maximize power dissipation~~ R_C when T_2 is OFF.

why active. Not Passive load??

Bcz we cannot change the value of resistance but active we can modify the resistance.

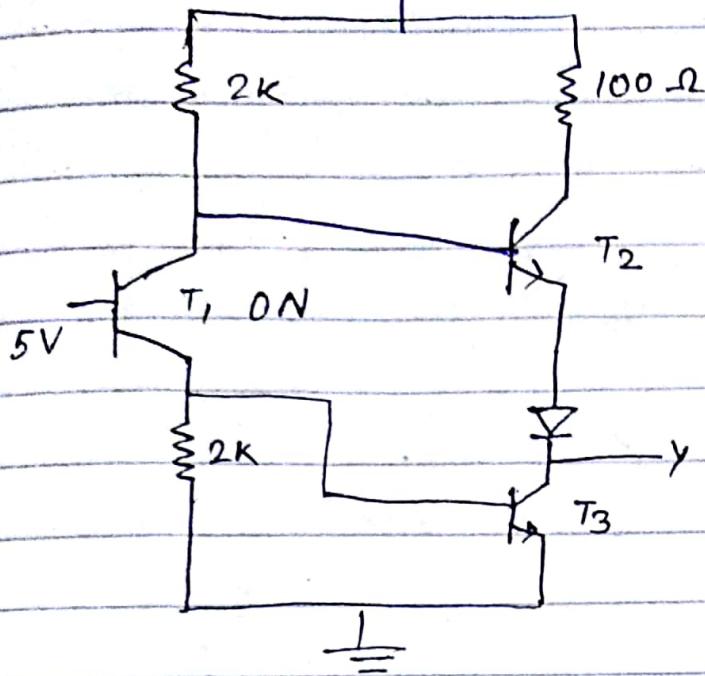
1. Draw a RTL circuit :

$$f_L = (A + B) C$$

$$f_L = \overline{(AB \bullet C \bullet D)}$$

V_{CE}
Y

V_{CE}
T Y



← Adv. of DTL

i) Improve charging / discharging

ii) Improve power dissipation

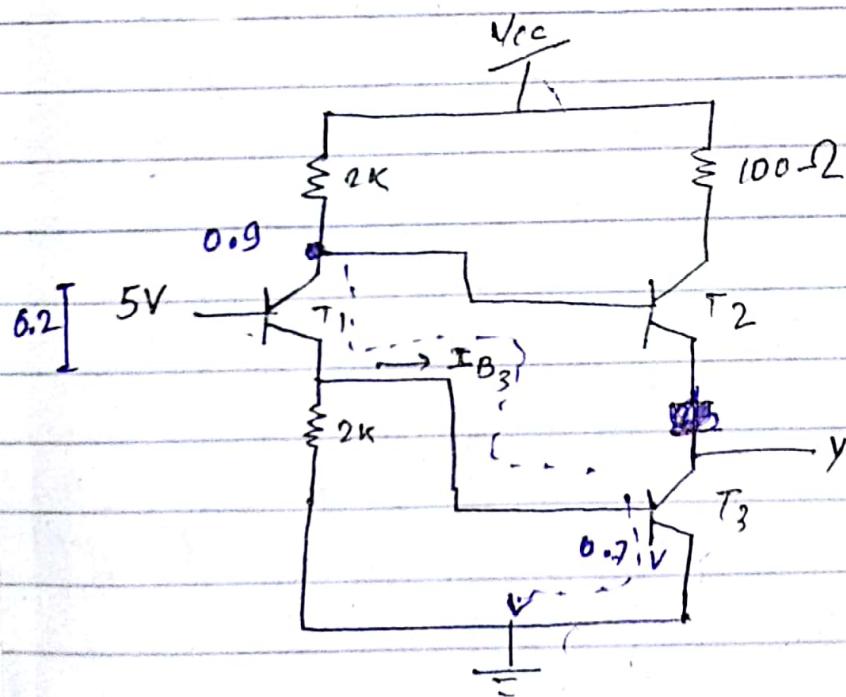
iii) Propagation time improve.

iv) speed improvement

v) size reduce, performance increase,

	T ₁	T ₂	T ₃	y
5V	ON	OFF	ON	0 (0.2V)
0.2V	OFF	ON	OFF	$1 \left(5 - V_{CE} - 0.75 = 4.01V \right)$ (0.2)

T₁ is called face-splitter g-to-en-poh network



V.V.I. //

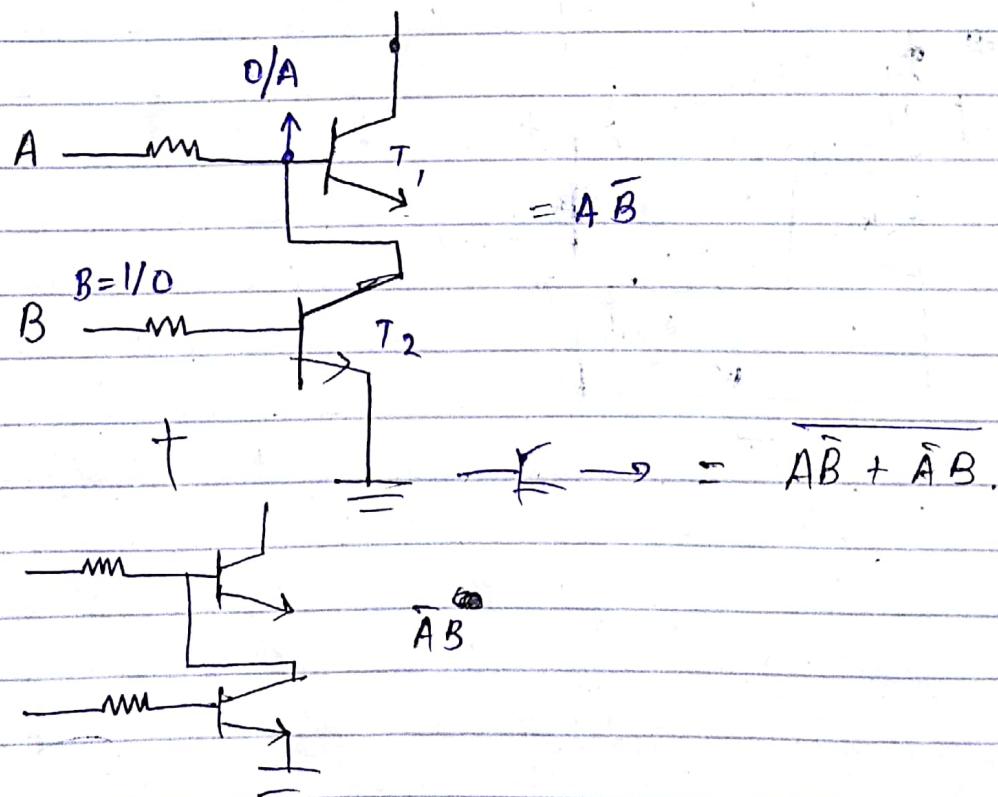
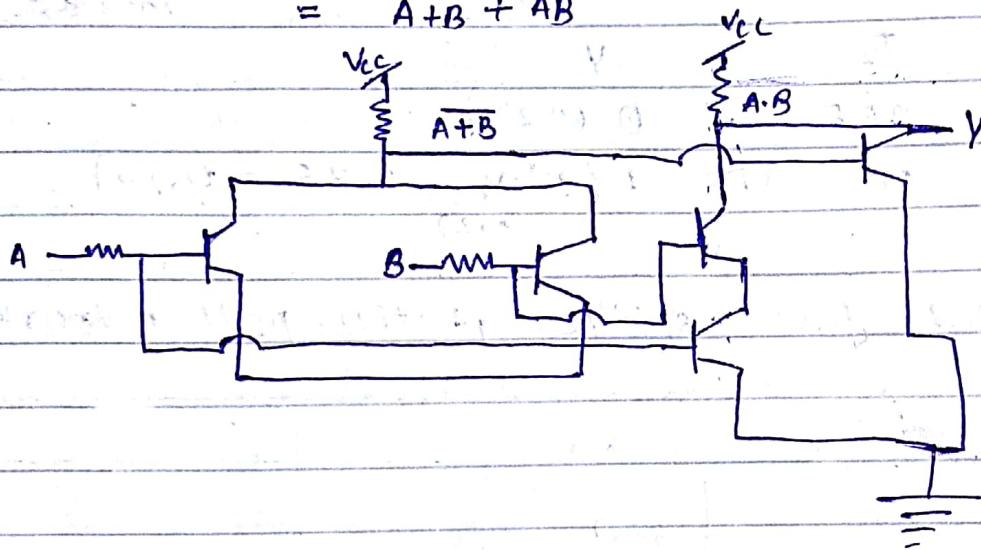
Design using RTL logic family with minimum number of transistors. $Y = \overline{AB} + \overline{A}\overline{B}$ (XOR gate)

$$Y = \overline{AB} + \overline{A}\overline{B}$$

 ~~$= (\overline{A} + B)(\overline{A} + \overline{B})$~~
 $= (A + \overline{B})(\overline{A} + B)$

$$Y = \overline{\overline{AB} + A\overline{B}} \quad (\text{XOR})$$

 $= \overline{\overline{AB} + AB}$
 $= \overline{A + B + AB}$



Disadvantage of RTL

- 1) No. of Resistances is more
- 2) Area. A

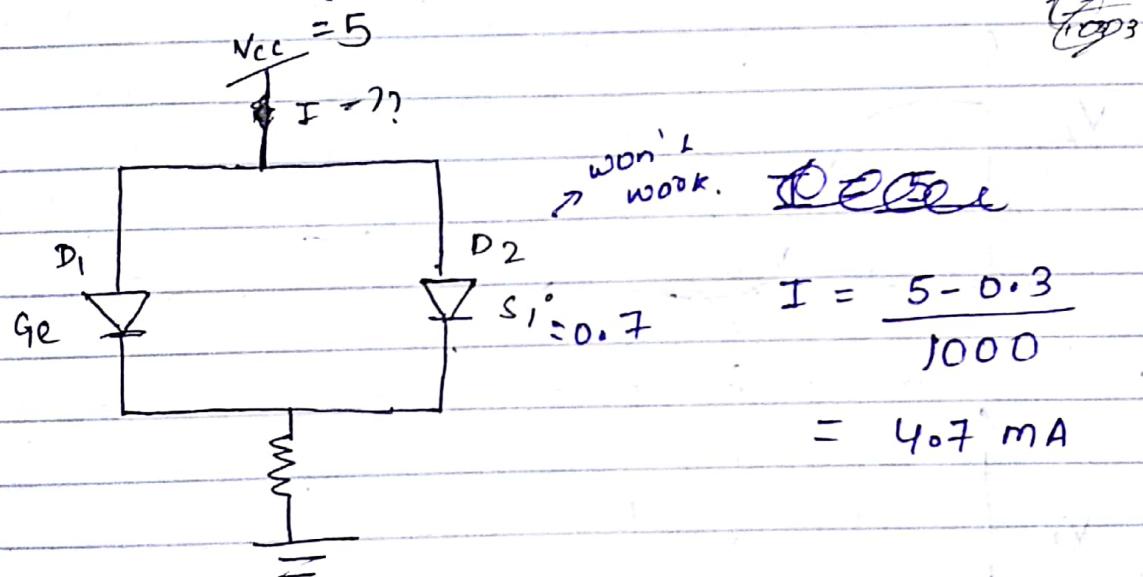
DCTL (Direct Coupling Transistor logic)

Disadvantage:

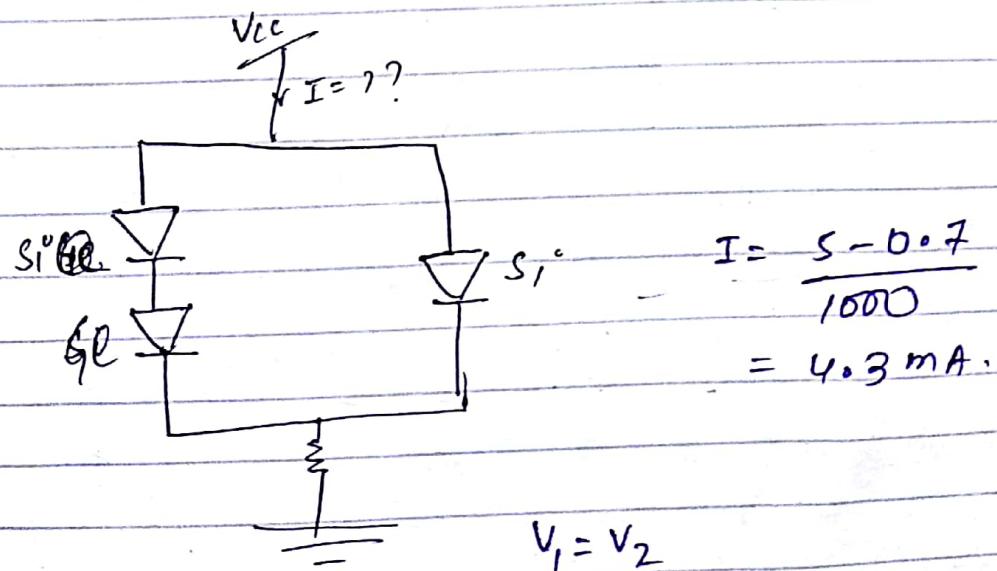
- 1) Problem of current hogging problem
not properly distributed.

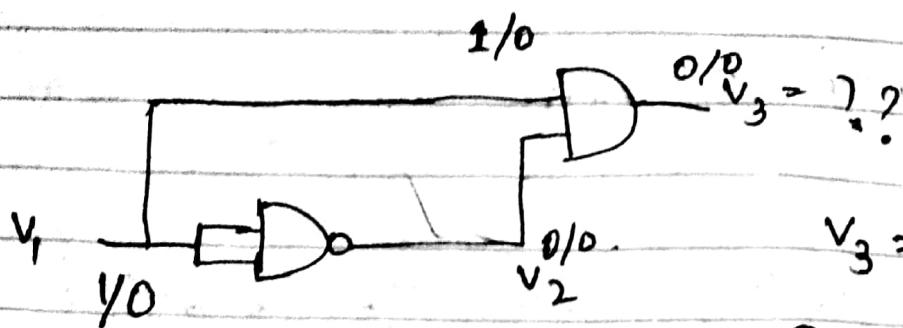
Advantage:

- 1) less resistor
- 2) less area.



If two voltage source in parallel,
~~total voltage drop~~ $V_1 = 0.3$ and $V_2 = 0.7$.



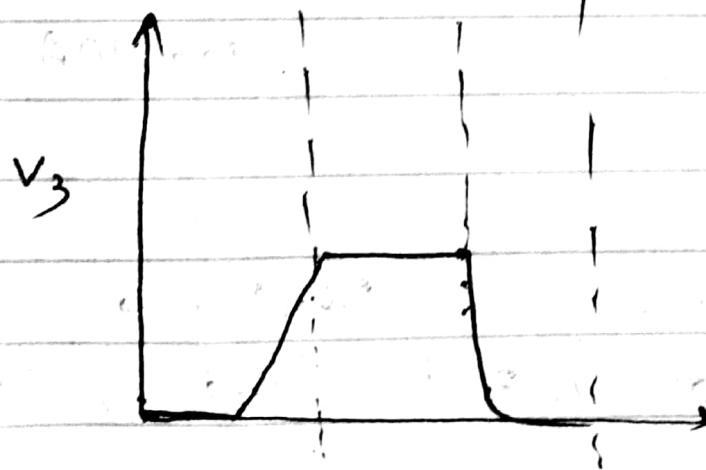
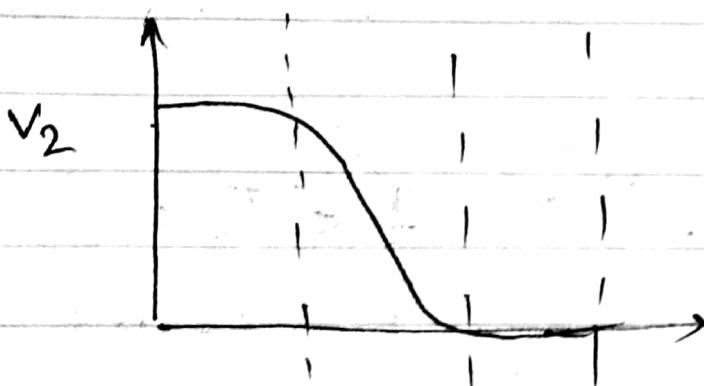


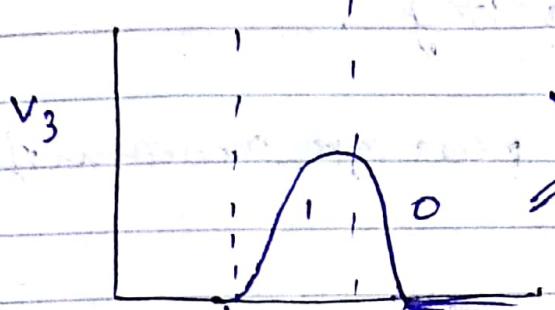
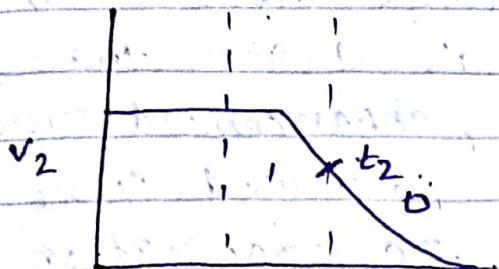
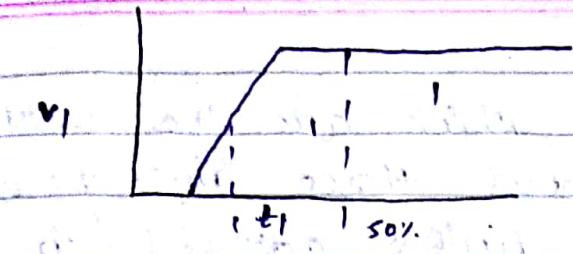
$$v_3 = 0.$$

Propagation delay.



Draw the waveform of v_2 and v_3 .



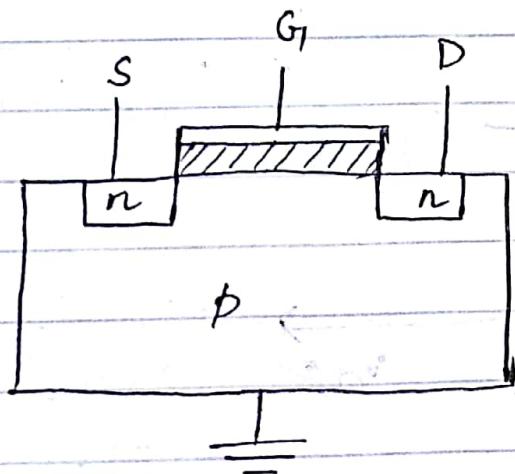


For cascading ckt
disadvantages

- 1) Noise will be there
- 2) Time delay is going to add
- 3).

Imp Propogation delay
Hazard

n - MOS



~~enhancement~~ type is ~~more~~ more better than Depletion enhancement.

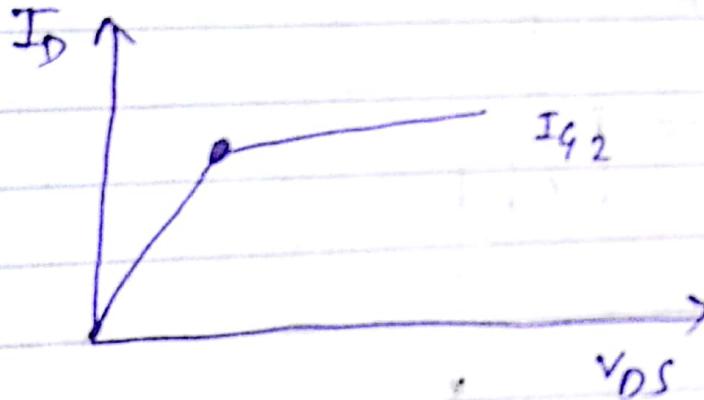
Dis adv of Depletion

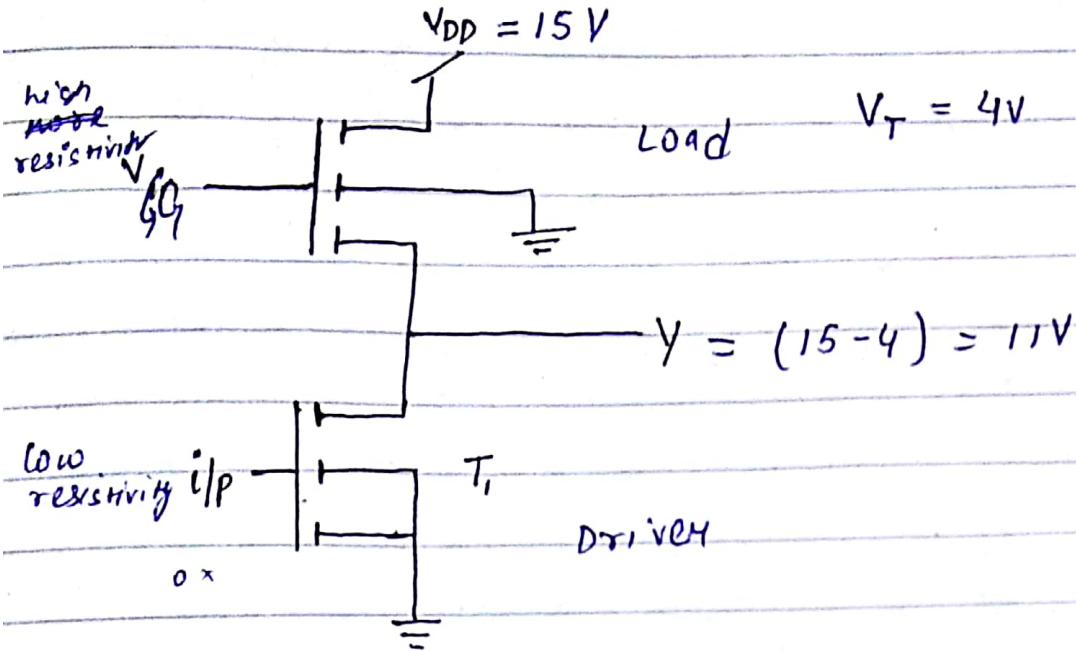
- 1) At OV, p depletion also works. ~~no connection b/w source and drain.~~

- 1) The mobility of e's which are the carriers in an n-MOS is about three times greater than the mobility of holes carrier in p-MOS. Hence, n-MOS is faster than p-MOS.
- 2) The digital circuit using enhancement mode transistors is generally preferred since it is a great convenience that the transistor be cutoff at 0 gate voltage.

gate current almost ~~plus~~ picamper

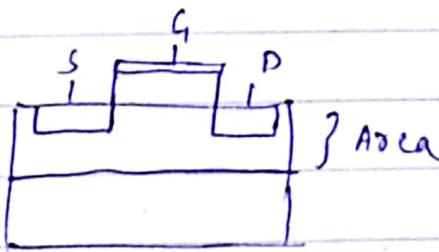
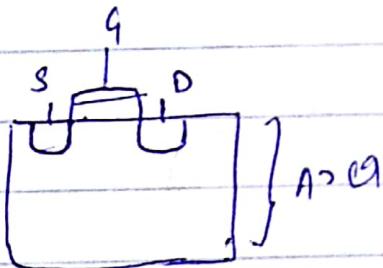
when both regions are overlapped the region is pinch-off. After that we get constant current.





~~If resistance is low~~

channel less, more conductivity.



conductivity fast

Resistivity decreases

- 1) The Driver transistors should have relatively high conductance while load should have low conductance.
- 2) In the bipolar trans. switch ckt, use of load resistance of order of some thousands of ohm but for the MOSFETs Switch ckt's, load resistance will be off many 10×10^3 of ohms even upto $100k\Omega$