Bachelor of Instrumentation and Electronics Engineering, 2017-18
2nd year, 2nd semester
DIGITAL ELECTRONICS

Time : Three hours **Full Marks : 100**

ALL MODULES ARE COMPULSORY.

Module – I (5 Marks)

(Answer Either Q1 or Q2.)

Q1. What decimal number corresponds to the binary pattern **10110110**, when it is in (a) Excess-3 BCD format. (b) 2's complement format, (c) unsigned binary format, (d) Gray format, and (e) sign-magnitude format. (5)

Q2. (a) Convert $(408.26)_9$ to **base-3** system. (b) Convert the Gray pattern **10110110** into binary. (c) State the advantage of Gray code. (2+1+2)

Module – II (5 Marks)

(Answer Either Q3 or Q4.)

Q3. Perform the following arithmetic operations :

(a) **(-39) + (+21)** using **8-bit 2's** complement number system.

(b) **(+28) + (+99)** using **8-bit 1's** complement number system. (2+3)

Q4. Realize the logic circuit for detecting **overflow in 1's complement addition**. (5)

Module – III (40 Marks)

(Answer Any TWO from Q5, Q6 and Q7)

Q5. (a) Using a suitable **PROM** realize a **Full-adder**. What is the dimension of this PROM ? Draw both AND plane and OR plane.

(b) Draw the **CMOS** circuit which realizes the following function :

$$F(A, B, C) = AC' + A'BC' + BC$$

(c) Outputs of two standard TTL gates **should never be shorted** together. Explain.

(10 + 6 + 4)

Q6. (a) Use Karnaugh Map technique to obtain the minimized expressions for the following functions as indicated :

(i) F(W, X, Y, Z) = WX'Z + W'X'Z' + WX' + X'Y; in **minimized POS** form

(ii) F(A, B, C, D) = ∏M(3, 5, 6, 7, 12, 14); in **minimized SOP** form

(iii) F(A, B, C, D) = ∑m(0, 1, 2, 6, 8, 10, 11, 12); in **minimized NOR-NOR** form

(b) In **Positive Logic** certain logic circuit corresponds to the function

f = A'B'C + ABC+ AB'

What will be the expression of the output from the same logic circuit in **Negative Logic** ?

(3 x 5 + 5)

Q7. (a) Using **one** 8:1 Multiplexer and **one** 2:1 Multiplexer **(if needed)** realize the following function :

F(W, X, Y, Z) = WX'Z' + W'X'' + W'X + XY'

(b) Realize a **4-input Priority Encoder.** (12 + 8)

Module – IV (50 Marks)

(Answer Q8 **and** Any TWO from Q9, Q10 and Q11)

Q8. Realize a **JK-FF using one T-FF** as the memory element. (10)

Q9. Design a **MOD-6** synchronous **lockout-free Gray code counter** which counts from 0 to 5 repeatedly in Gray format. Use **D-FFs** as memory elements. (20)

Q10. (a) Design a sequence generator which generates the sequence "**100110**" repeatedly. Use minimum number of D-FFs.

(b)What do you mean by **synchronizer failure** ? Which technique is used to reduce the chance of such failure ?

Q11. (a) Using **SR-FF** as memory element, realize a sequential **Gray to Binary** code converter. The input Gray bits are coming serially starting from the MSB.

(b) Discuss the **merits and demerits** of a **Ring-counter**.

(c) What is the **race-around problem** in JK-Latch ? How is it avoided ?

(10+5+5)