BACHELOR OF COMPUTER SCIENCE ENGINEERING EXAMINATION, 2012

(2nd Year, 1st Semester)

DIGITAL CIRCUITS

Time : Three Hours | Full Marks - 100

Answer any **Five** questions

1. a) Explain the operations of a RTL NOR gate. 4

   b) Estimate its fan-out capabilities. 6

   c) Draw its transfer characteristics. 4

   d) How can the fan-out of the same be increased? Explain. 2+4

2. a) What are the disadvantages of a DTL gate? How can they be resolved in TTL gates? 2+6

   b) Draw and explain the transfer characteristic of a standard TTL NOT gate. 12

3. a) Explain the operations of an nMOS Inverter. 6

   b) Draw its transfer characteristics. 4

   c) How can NAND and NOR gates be iplemented by using nMOS devices? What are their relative merits and demerits? 4+2

d) Realise $X = \overline{A \cdot (B + C) + D \cdot E}$ by using a single MOS gate. 4

4. a) Explain the operation of an Astable multivibrator using an 555 IC timer. 6

b) Deduce the expressions of the Time-period and duty cycle. 4+2

c) Design a clock working 1 KHz with 30% duty cycle using a 0.01 μf capacitor. 4

d) How can the duty cycle of 50% be achieved? 4

5. a) With the help of a circuit diagram explain the operations of a 3 Tr/Cell memory. 8

b) How can the stored information be maintained is such a memory cell? 8

c) How does it differ from a 1 Tr/Cell memory? 4

6. a) Explain the operation of a 4 bit DAC using weighted resistors. 10

b) What are the problems of a weighted resistor DAC? 2

c) How can a two digit BCD converter be designed by using 4 bit DAC's? 8

7. a) Explain the operation of stair-case type ADC. 14

b) Why is it also called a Ramp-type ADC? 2

c) What are its relative merits and demerits? 4

8. Write notes on any **four** of the following : 4x5=20

a) Problems of DCTL

b) HTL gates

c) Tristate gates

d) ECL gates

e) CMOS gates

f) Multiplication of an input frequency by a factor of π

g) Classifications of memories

h) EPROM's.