

Exam Roll - CSE218056

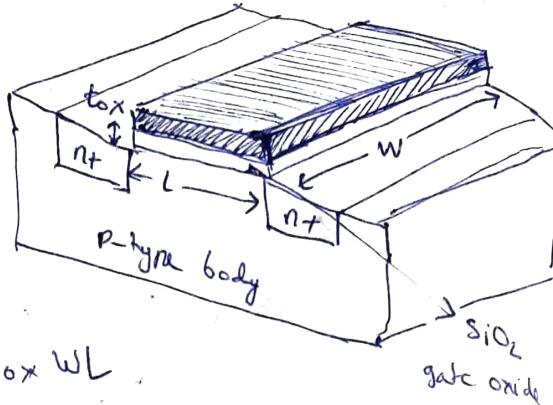
Class Roll - 001710801029

BCSE-IV Sem-2

Sub:- VLSI Systems.

1.

b). For an NMOS transistor



Approximate channel connected to Source.

$$C_{gs} = \epsilon_0 \epsilon_{\infty} WL / t_{ox} = C_{ox} WL$$

Calculating channel charge

$$Q_{\text{channel}} = C_{gs} V_{gc}$$

Here V_{gc} depends on position of the channel.Taking average value, as $\frac{V_{ds}}{2}$ Effective gate voltage = $V_{gs} - V_t$, $V_t \Rightarrow$ threshold voltage.

$$V_{gc} = (V_{gs} - V_t) - \frac{V_{ds}}{2}$$

Then,

$$Q_{\text{channel}} = C_{ox} WL \left\{ (V_{gs} - V_t) - \frac{V_{ds}}{2} \right\}$$

Time taken by carriers to cross channel is

$$t = \frac{L}{4} / u V_{ds} \quad \left[t = \frac{L}{u} = \frac{L}{u E_{ds}} = \frac{L \times L}{u V_{ds}} = \frac{L^2}{u V_{ds}} \right]$$

where u is mobility.

Now the current is given as

$$I_{ds} = \frac{Q_{\text{channel}}}{t} = u C_{ox} \left(\frac{W}{L} \right) \left\{ (V_{gs} - V_t) - \frac{V_{ds}}{2} \right\} V_{ds}$$

$$I_{ds} = \beta \left[(V_{gs} - V_t) - \frac{V_{ds}}{2} \right] V_{ds} \quad \text{--- (1)}$$

$$\text{where } \beta = u C_{ox} \frac{W}{L}$$

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The three conditions for eq of I_{ds} is given as - ②

i) Cutoff: when $V_t > V_{gs}$, in such a case there is no flow of charge, Hence, $Q_{drain} = 0$.

$$I_{cutoff} = 0.$$

ii) linear: when V_{ds} is very small as $V_{gs} > V_t$, the transistor is ON and the term $V_{ds}/2$ is negligible in comparison to $V_{gs} - V_t$.

Thus eq① becomes:

$$I_{linear} = \beta(V_{gs} - V_t)V_{ds}, \text{ where } \beta = \mu C_o x \frac{W}{L}$$

↳ linear equation.

3). Saturation:-

If $V_{gd} < V_t$; the channel pinches off near drain.
i.e. when $V_{ds} > V_{dsat} = V_{gs} - V_t$. $\left[V_{dsat} = \text{saturation voltage} \right]$

Thus at saturation :-

$$I_{ds} = \beta \left[(V_{gs} - V_t) - \frac{V_{dsat}}{2} \right] V_{dsat}$$

$$= \beta \left[(V_{gs} - V_t) - \frac{(V_{gs} - V_t)}{2} \right] \cdot \left(\frac{V_{gs} - V_t}{2} \right)$$

$$I_{saturation} = \beta (V_{gs} - V_t)^2 / 2. \text{ when } \beta = \mu C_o x \frac{W}{L}$$

ii)

Given

$$l_{ox} = 100 \text{ nm}$$

$$u = 350 \text{ cm}^2/\text{V s}$$

$$V_t = 0.7 \text{ V}$$

$$V_{gs} = 5 \text{ V}$$

$$V_{ds} = 4 \text{ V}$$

$$\frac{w}{L} = 2.$$

$$\beta = u C_{ox} \frac{w}{L} = 350 \times \frac{39 \times 8.85 \times 10^{-14}}{100 \times 10^{-8}} \times 2 \\ = 240 \text{ mA/V}^2$$

$$I_{ds} = \beta \left\{ (V_{gs} - V_t) - \frac{V_{ds}}{2} \right\} V_{ds}$$

$$= 240 \left\{ (5 - 0.7) - \frac{4}{2} \right\} \times 4 \text{ mA}$$

$$= 240 \times (4.3 - 2) \times 4 \text{ mA}$$

$$= 240 \times 2.3 \times 4 \text{ mA}$$

$$= 2,208 \times 10^3 \text{ mA}$$

$$I_{ds} = 2.208 \text{ mA}$$

Hence the current in the transistor is 2.208 mA

2. i) Problems of VLSI design :-

• problems with technology :

- High power consumption (power density, leakage)
- Process variation - larger as a fraction of feature size.
- Increased noise sensitivity.

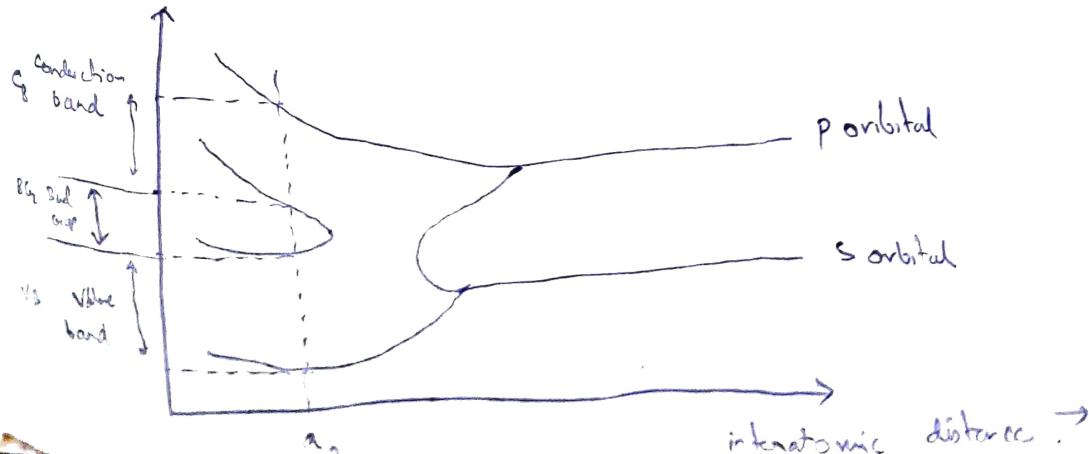
• Problems with design :

- verification of correctness - logic and timing
- Ensuring reliable operation
- Testing.

ii) Design synthesis is the development of a procedure to manufacture a device using ~~unknow~~ unknown materials and processes when given an I/O function.

Synthesis transforms the RTL design into a gate-level netlist with all the constraints as specified by the designers.

iii) ~~The given~~ The given observation can be explained by energy band theory of crystals. If we consider the group of Si, then the energy vs interatomic distance curve will be as follows :-



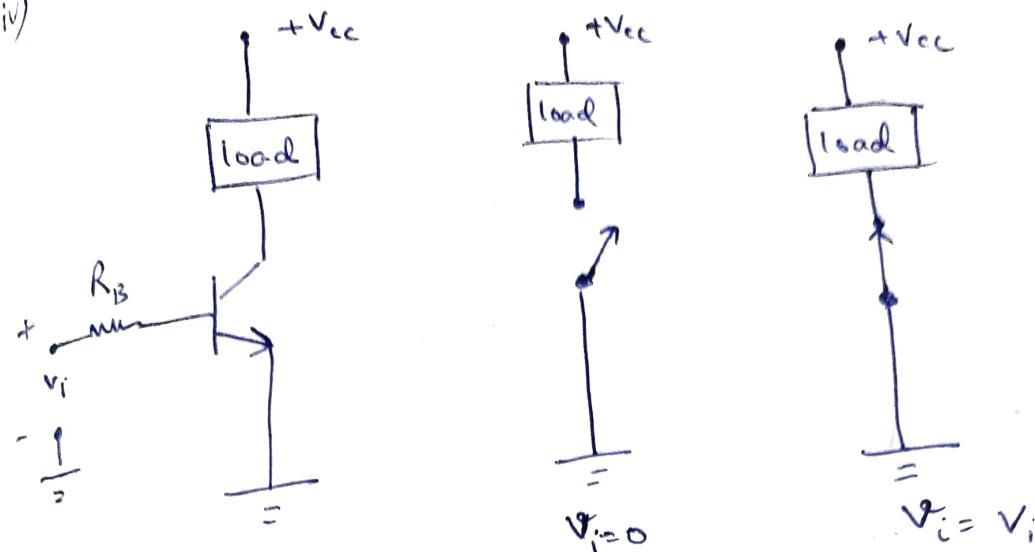
In general, the electrons are present in the outermost s and p orbitals are of interest because they contribute to the flow of charge in a crystal ~~to~~ lattice. In general, the electrons moving around in the conduction band cause the flow of charge. There is however an energy difference between the valence and conduction bands called the band gap - which decides the transfer of electrons from the valence band to the conduction band, and hence the nature of the element.

If, band gap is high : C, we get an insulator ($\sim 5\text{ eV}$) with no movement of electrons in conduction band.

If band gap is ~~less~~ low : Sn, Pb, we get conductors with free movement of electrons in CB.

3. If band gap is moderate : Si, Ge, we get a semiconductor due to the controlled flow of electrons in CB.

iv) Transistor as switch:



The above diagram represents an npn transistor as a switch when gate voltage v_i is 0, no charge flows across the transistor and it acts as open switch.

When $v_i = V_i$; the transistor allows flow of charge, and it acts as a closed switch.

3.

a)

$$i) f = ab + bc + cd$$

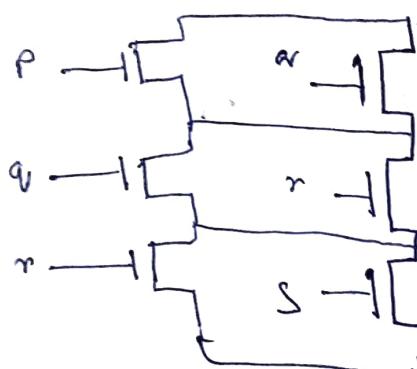
$$f = \overline{f} = \overline{(ab + bc + cd)} = \overline{(\overline{a} + b)(\overline{b} + c)(\overline{c} + d)}$$

$$= \overline{(p+q)(q+r)(r+s)}$$

where $p = \overline{a}$, $q = \overline{b}$, $r = \overline{c}$, $s = \overline{d}$.

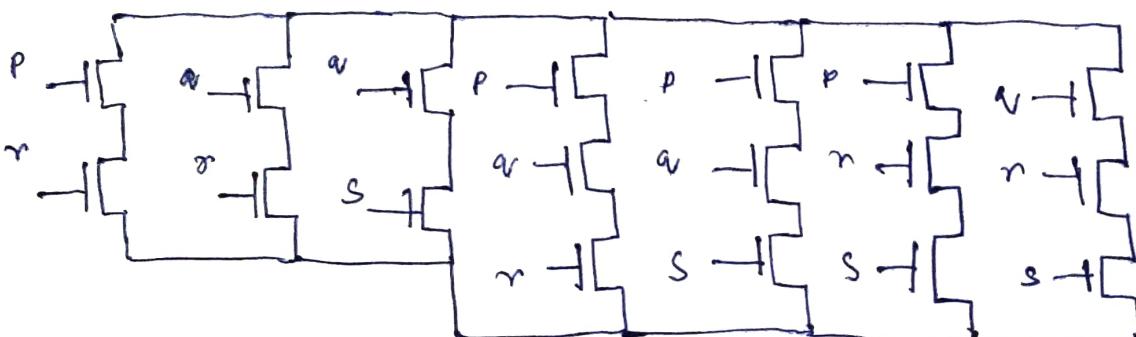
Let's implement \overline{f} using NMOS.

PS form:-



$$\begin{aligned}\overline{f} &= (p+q)(q+r)(r+s) \\ &= (pq + pr + qr + qrs)(r+s) \\ &= pqr^2 + pqrs + pr^2 + prs \\ &\quad + qqr^2 + qrs + qr^2 + qrs \\ &= pr + qr + qs \\ &\quad + pqr^2 + pqs + prs + qrs\end{aligned}$$

SP form:-

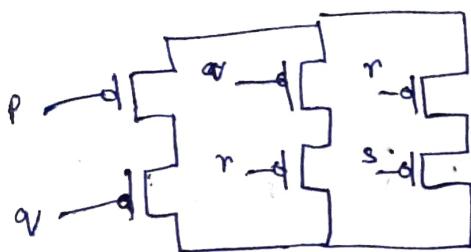


lets implement f using PMOS

$$\bar{f} = (p+a)(q+r)(r+s)$$

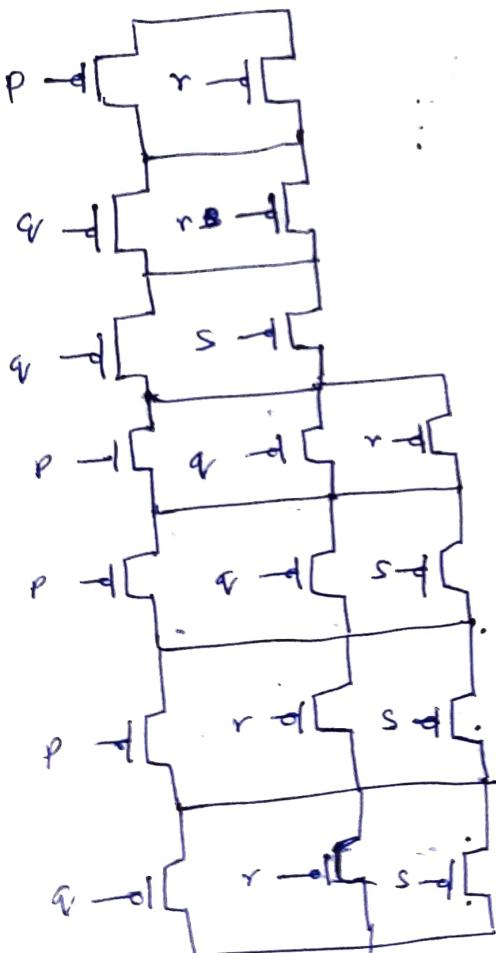
$$\begin{cases} p = \bar{a}, & r = \bar{c} \\ q = \bar{b}, & s = \bar{d} \end{cases}$$

8P form



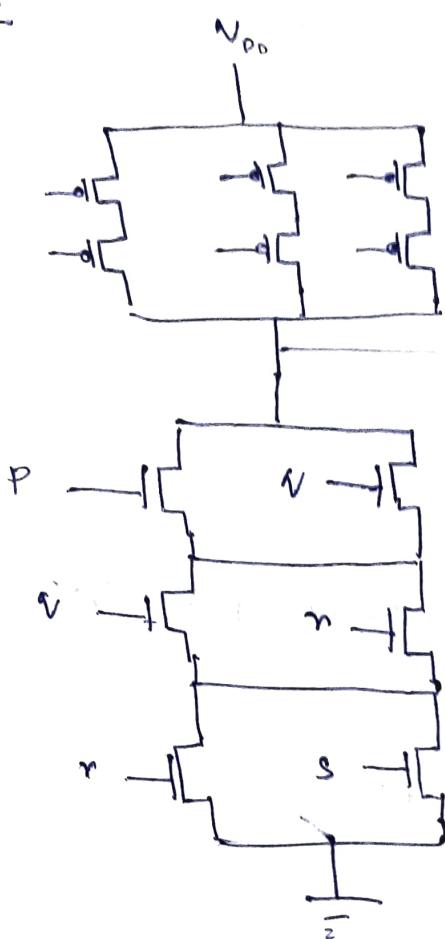
ps form

$$\bar{f} = pr + qrr + qrs + pqr + pqrs + prs + qrs$$



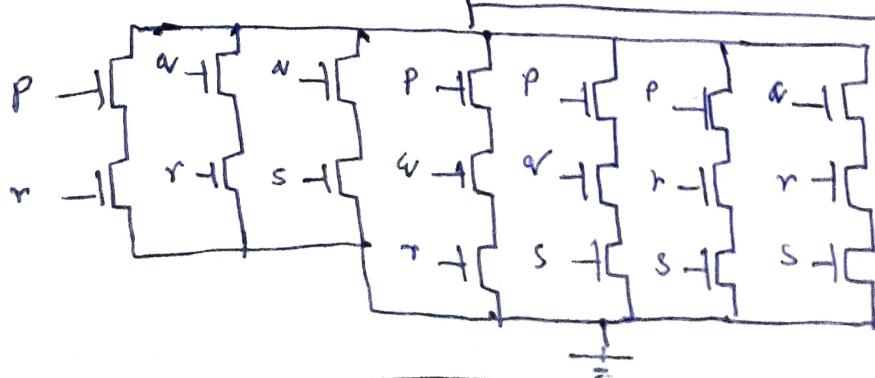
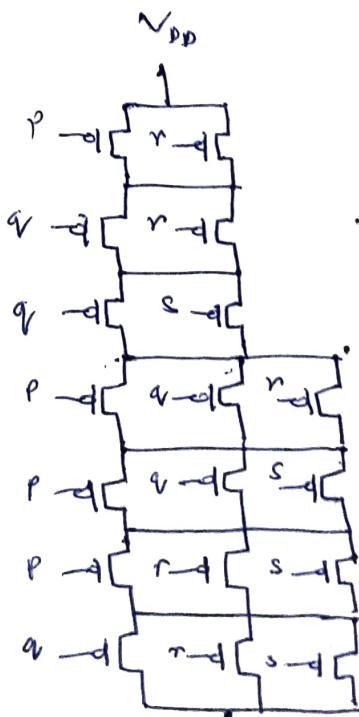
Different single complex cell design implementation of f one:-

 SP - PS
1.



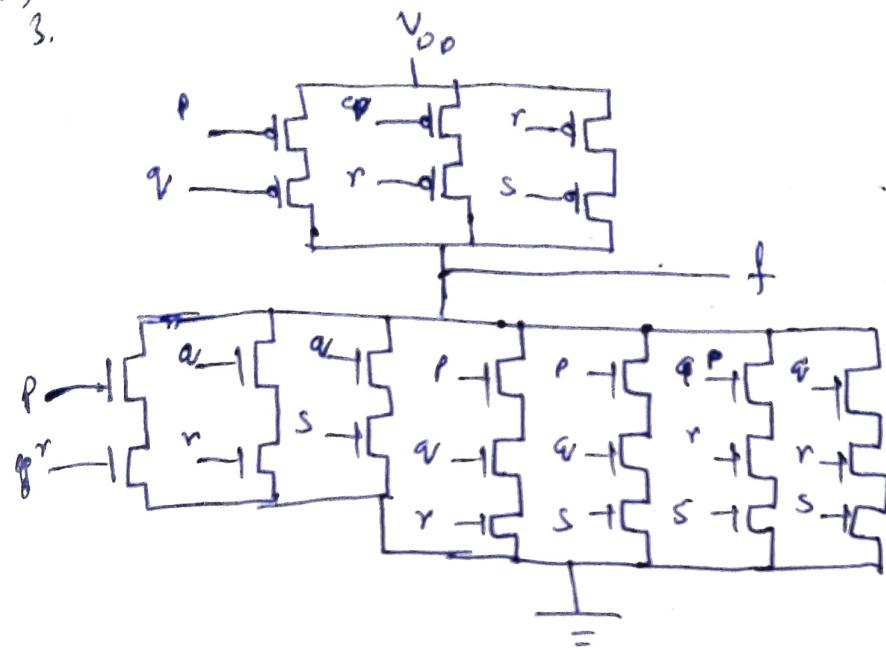
$$\begin{aligned}f &= \overline{(P+q)} (\overline{B} \overline{q} + r) (\overline{t} + q) \\&= ab + bc + cd\end{aligned}$$

 PS - SP
2.

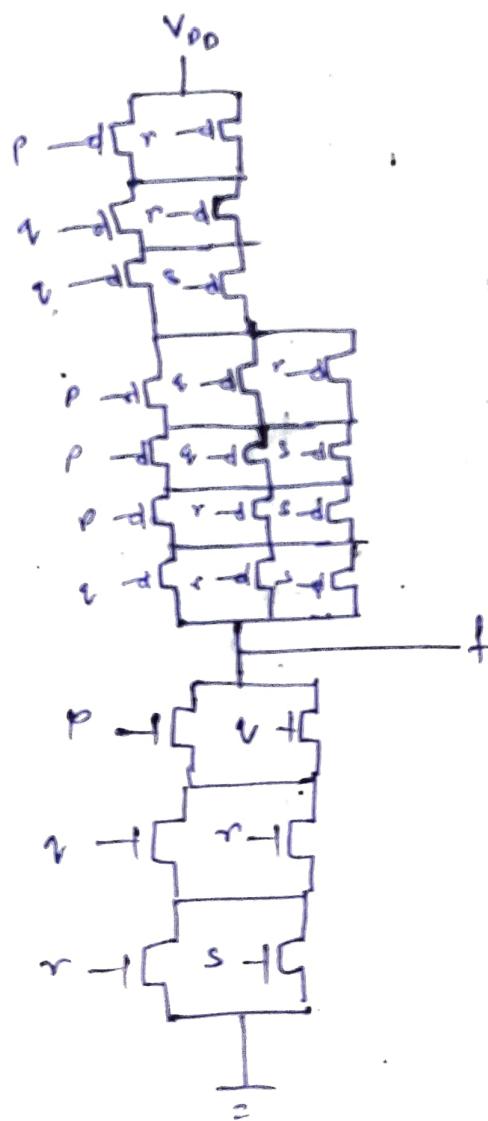


$$f = ab + bc + cd$$

(2) 3. SP - B SP

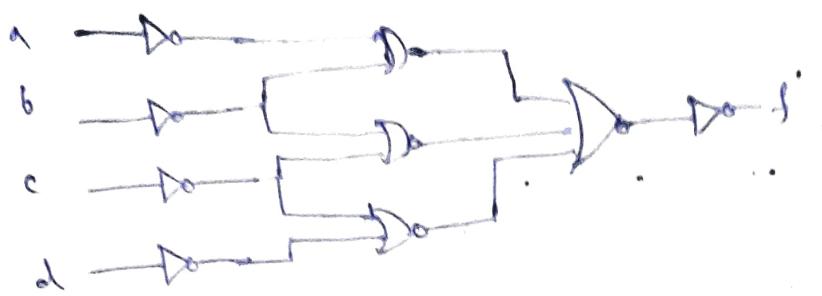


(2) 4. PS - PS

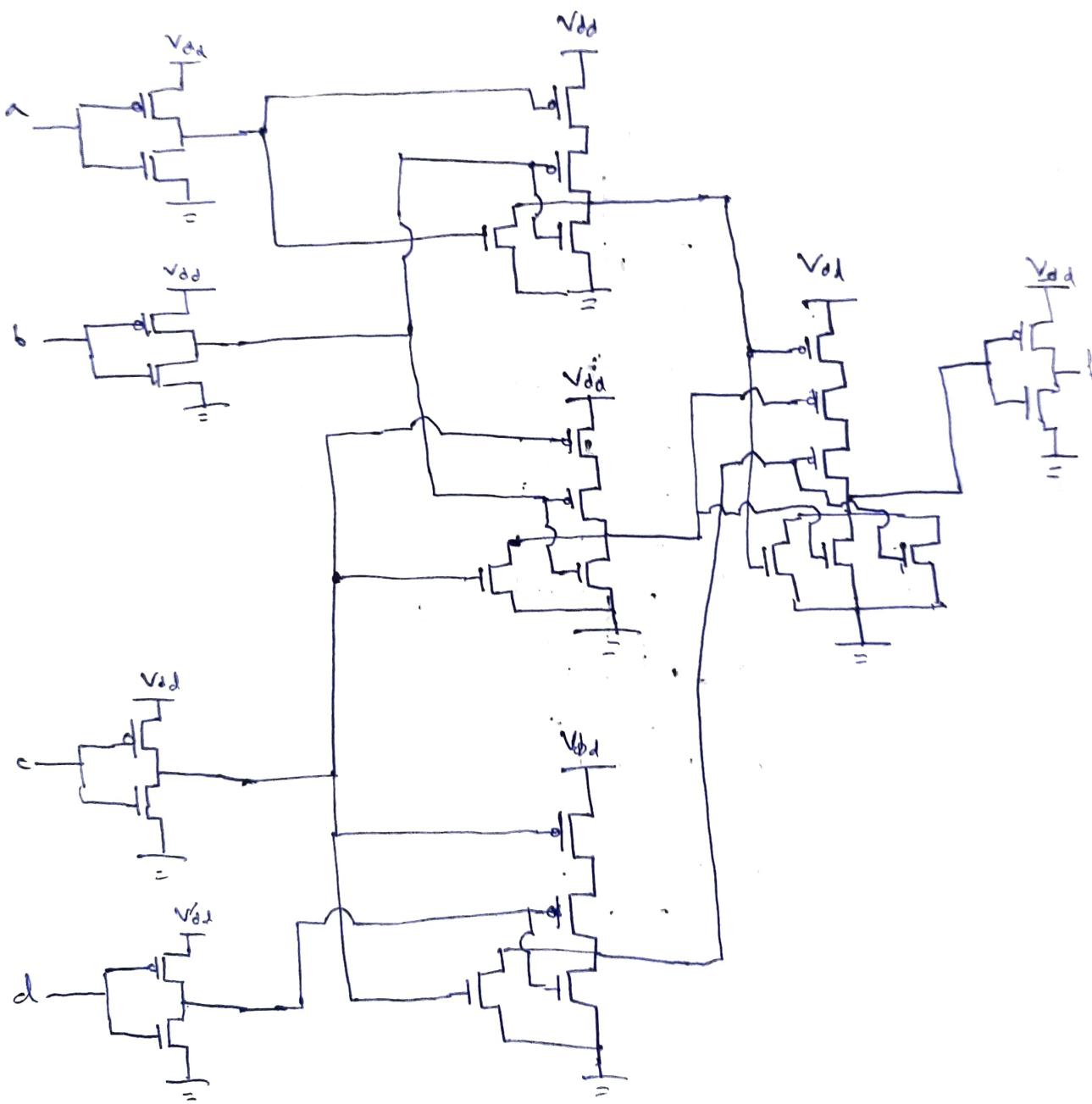


ii) $f = ab + bc + cd$

equivalent logic circuit



Equivalent CMOS NOR gate circuit.



3. c) i) λ -based design rules:-

lambda based design rules are rules that are based on a single parameter i.e. λ .

- The ~~minimum~~ minimum feature size is depicted as 2λ . This is to allow for shape contraction.
- Along with that the minimum separation of features are a layer of 2λ , to ensure adequate continuity of the intervening materials.

Advantages of λ -based design rules:-

1. Simple for the designer
2. wide acceptance
3. provides feature size independent way of setting out mask.
4. preserves topological features on a chip.
5. Prevents shorting, opens, contacts from slipping out of area to the contacted.

Disadvantages of λ -based design rules:-

1. limited linear scaling.
2. Too conservative.

NMOS - Design Rules:-

1. Minimum width of diffusion region and polysilicon region = 2λ
2. minimum width of metal line = 3λ
3. Diffusion - Diffusion spacing = 3λ
4. poly poly spacing = 2λ
5. Polysilicon gate extension = 2λ
6. contact extension = λ .

It is sometimes advantageous to convert polysilicon to diffusion.

The two types of contact are :-

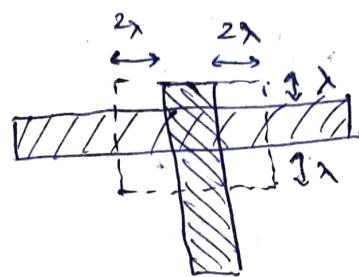
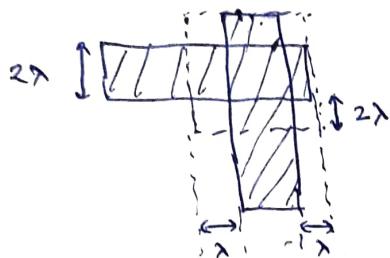
- Butting contact • Buried contact.

3.

9)

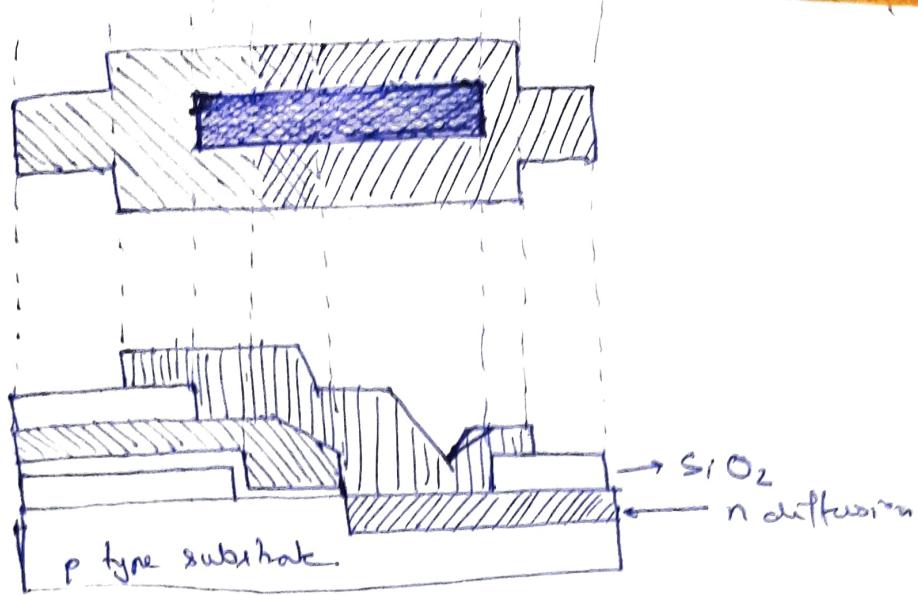
i) Buried contact :-

In buried contact layers join over a $2\lambda \times 2\lambda$ area with the ~~the~~ buried contact cut extending 1λ in all directions around the contact area except that the contact cut extension is extended to 2λ . This contacts poly silicon layer to diffusion region.



Butting contact :-

- This contacts poly silicon layer to diffusion layer using metal
- In butting contact, a $2\lambda \times 2\lambda$ cut is made down to ~~over~~ each of the layers to be joined. The layers are butted together in such a way that these two contact cuts become contiguous.
 - Since the poly silicon and diffusion ~~and~~ sections overlap and then oxide under poly silicon acts as a mask in the diffusion process, the layers are also butted together.
 - The contact b/w the two butting layers is then made by a metal overlay as shown :-



4.

a)

- i) Comparison of silicon and germanium in fabrication :-
- a large variety of processes are possible in Si without the problem of decomposition as in case of compound semiconductor of germanium.
 - Silicon has a higher band gap than germanium, hence it has higher ~~operat~~ operating temperatures.
 - $\text{Si} \rightarrow 125^\circ - 175^\circ$
 - $\text{Ge} \rightarrow \sim 85^\circ$
 - Silicon readily forms a ~~natural~~ native oxide $\rightarrow \text{SiO}_2$ which is a high quality insulator, protects and passivates the underlying circuitry, helps in ~~resist~~ patterning and is useful for daping masking.
 - Silicon is abundant and cheap as compared to Germanium.
 - Silicon has lower mobility (μ) than Ge.
- These silicon circuits are slower :

Material
Si

Mobility :- ($\text{cm}^2/\text{V}\cdot\text{s}$)

$$n_s = 1500 \quad \mu_p = 960$$

Ge

$$n_s = 3900 \quad \mu_p = 1900$$

- Silicon has indirect bandgap which makes it weak for absorption and emission of light.

Due to its cheap cost, abundance, stable oxide, higher operating temperature, reduced leakage current, Silicon is preferred over Germanium for fabrication.

Q. a)

- i) Basic processing steps of fabrication are:-

Starting material :- lightly doped p-type Si substrate.

1. Oxide silicon-Surface:

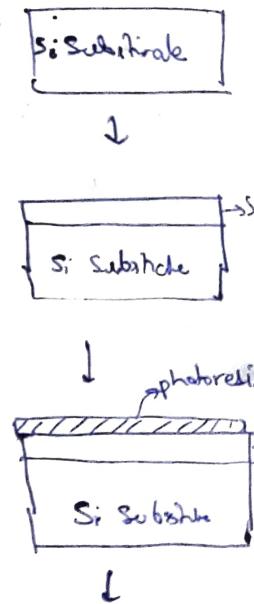
- A small layer of Si substrate, about 1μm thick is oxidized.

2. Deposit photoresist:-

- photo resist, a light sensitive and acid resistant organic polymer, is placed on top of the SiO_2 .

3. Mount mask.

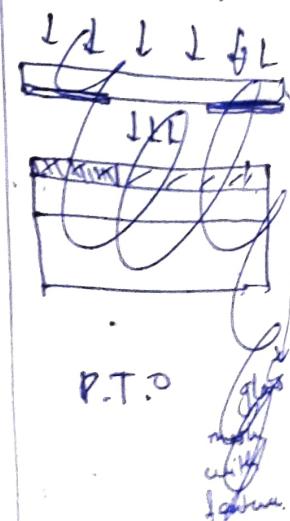
- A ~~mask~~ mask (pattern) is placed above photoresist. The mask defines the regions into which diffusion is to take place together with channel.



4. Expose to UV light

- The photoresist through is made is exposed to the UV ~~light~~ light.

- The areas where UV light strikes becomes soluble in certain solvents.



S. Etch photoresist and SiO₂

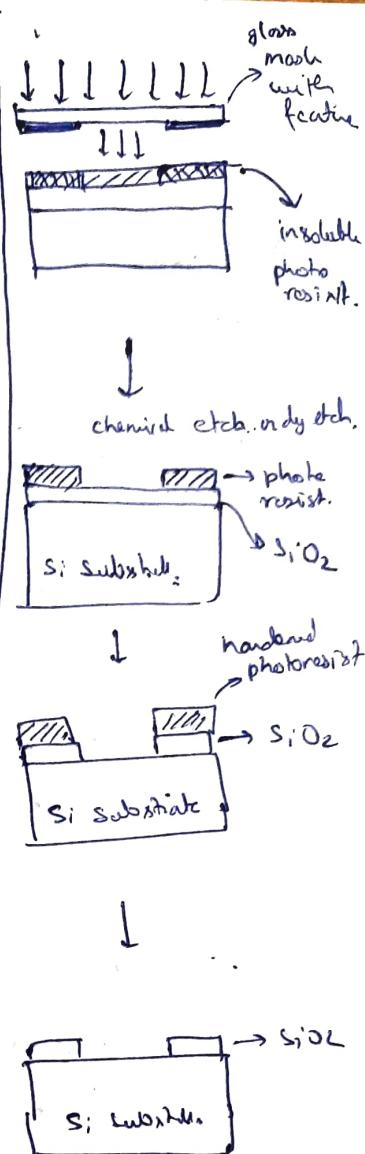
The exposed photoresist regions are etched out.

- The SiO₂ which are not covered by the photoresist, can now be etched away \leftrightarrow using a chemical solvent (HF acid) or dry etch process (using plasma).

6). Removal of photoresist :-

- After the last step, we have an oxide window that reaches down to the silicon layer.
- The remaining, unexposed and hardened, photoresist is not stripped from SiO₂ surface using another solvent.
- This leaves a patterned silicon dioxide feature on the surface

The fabrication process of semiconductor devices, requires several such patterns to be performed on SiO₂ polysilicon.



[5] b)

- i) A sliceable floor-plan is a floorplan that can be obtained by recursively partitioning a rectangle into two parts, either by a horizontal or vertical line. Any floor plan that cannot be obtained by that method are called non-sliceable floor plans.

For example,

Sliceable:-

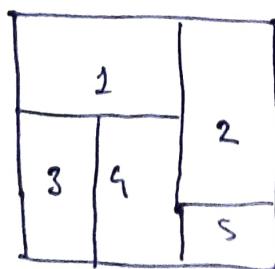


non sliceable :-

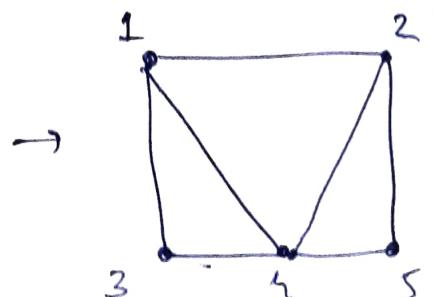


- ii) An adjacency graph of a rectangular floor plan is a planar graph $G_1 = (V, E)$ where V is the set of modules and $(M_i, M_j) \in E$ if and only if modules M_i & M_j are adjacent in the floor plan.

Ex -



Floor plan



adjacency graph

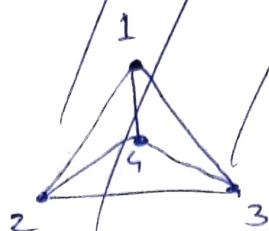
An adjacency graph cannot admit a rectangular dual iff it contains a complex triangle as a sub-graph.



complex triangle.

(18)

If the adjacency graph contains a complex triangle
 then it cannot be transformed into a rectangular floor plan.



complex triangle

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Advantage of having a rectangular deal :-

Hence a deal with an adjacency graph

representation of a floor plan it can be easily represented in computer memory, thus iterative algorithms can be run using it on a computer.

iv)

Notation:-

 w_i, h_i : width & height of module M_i . (x_i, y_i) : coordinates of the lower left corner of module M_i w, y : width & height of floor plan. a_i, b_i : min & max values of aspect ratio w_i/b_i of module M_i .

Given a set of modules M , each module M_i , has an unknown $w_i \& h_i$, and a prescribed aspect ratio

$a_i \leq w_i/h_i \leq b_i$. The solution is to find $x_i, y_i, w_i \& h_i$, for each module such that all constraints are satisfied & xy is minimized.

The constraints are as follows:-

→ No overlap constraint:

~~if M_i is to the left of M_j -~~

$$\begin{array}{l} x_i + w_i \leq x_j \\ x_j + w_j \leq x_i \\ y_i + h_i \leq y_j \end{array}$$

$x_i + w_i \leq x_j$ if M_i is to the left of M_j

$x_j + w_j \leq x_i$ if M_i is to the right of M_j

$y_i + h_i \leq y_j$ if M_i is to the bottom of M_j

$y_j + h_j \leq y_i$ if M_i is to the top of M_j

(1)

for any pair of adjacent modules only one of them must be satisfied. to obtain a legal solution.

For each pair of modules $M_i \& M_j$ we introduce 2 binary variables $p_{ij} \& q_{ij}$. We also introduce $w \& h$ as the upperbound of width & height of the possible solution region.

$$x_i + w_i \leq x_j + w(p_{ij} + q_{ij})$$

$$x_j + w_j \leq x_i + w(1 - p_{ij} + q_{ij})$$

$$y_i + h_i \leq y_j + h(1 + p_{ij} - q_{ij})$$

$$y_j + h_j \leq y_i + h(2 - p_{ij} - q_{ij})$$

} — (2)

here $p_{ij} \& q_{ij}$ are binary variables & can only hold the values 0 or 1.

Module size constraint :

Introduce a lower bound on the size of a module.

$$\therefore w_i h_i \geq A_i$$

$$a_i \leq w_i/h_i \leq b_i$$

$$\therefore \text{on } w_{\min} = \sqrt{A_i/a_i} \quad \text{on } h_{\min} = \sqrt{A_i/b_i}$$

$$w_{\max} = \sqrt{A_i/b_i}$$

$$h_{\max} = \sqrt{A_i/a_i}$$

$$\text{Q) } w_i \in [w_{\min}, w_{\max}] \& h_i \in [h_{\min}, h_{\max}]$$

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The constraint $w_i \geq h_i$ is a non-linear constraint. We use the first order approximation of the equation i.e., a straight line passing through (w_{\min}, h_{\max}) & (w_{\max}, h_{\min}) .

$$h_i = \Delta_i w_i + c_i$$

$$\Delta_i = (h_{\max} - h_{\min}) / (w_{\max} - w_{\min})$$

$$c_i = h_{\max} - \Delta_i w_{\min}$$

~~The equation & their approximation~~

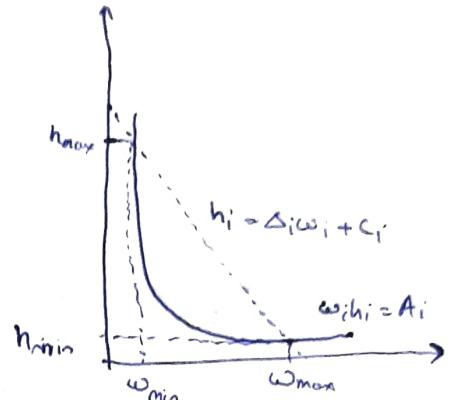
The linear constraint can now be incorporated into eqn (1) giving:

$$x_i + w_i \leq u_j$$

$$x_j + w_j \leq u_i$$

$$y_i + \Delta_i w_i + c_i \leq y_j$$

$$y_j + \Delta_j w_j + c_j \leq y_i$$



→ cost function: The function to be minimized is ~~the~~ the total area of floor plan. $A = \sum y_i$. Again this is a non-linear constraint. However it is possible to fix a width W and minimize height of floor plan.

$$\therefore \min y$$

$$x_i + w_i \leq W$$

$$y \geq y_i + h_i$$

∴ Complete LP formulation:-

$$\min y$$

$$x_i, w_i, y_i \geq 0$$

$$p_{ij}, q_{ij} = 0 \text{ or } 1$$

$$x_i + w_i \leq W$$

$$y \geq y_i + h_i$$

$$x_i + w_i \leq x_j + w (p_{ij} + q_{ij})$$

$$x_i + w_j \leq x_i + w (1 - p_{ij} + q_{ij})$$

$$y_i + \Delta_i w_i + c_i \leq y_j + H(1 + p_{ij} - q_{ij})$$

$$y_j + \Delta_j w_j + c_j \leq y_i + H(2 - p_{ij} - q_{ij})$$

5.

b)

- (iii) Let n be the number of vertices of an arbitrary extended dual $G_{\text{e}}(n)$. By induction, it is hypothesized that it is possible to generate a floorplan for any dual graph $G_{\text{e}}(k)$ for $k \leq n$. If the external vertices r, u, l, b have degree 3 or if external vertices r, u, l, b of graph G_{e} are examined, there are 2 possible cases: a) some of the vertices of r, u, l, b have degree 3 or b) none of the vertices have degree 3.

Consider the first case, without loss of generality, it can be assumed that vertex r has degree 3. Since $(r, u), (r, b) \in G_{\text{e}}(n)$, there is exactly one edge (r, v) where $v \notin \{r, u, l, b\}$.

The configuration of the graph is shown in figure 1a. Remove vertex r from $G_{\text{e}}(n)$ and replace vertex v as r . The resulting graph $G_{\text{e}}(n-1)$ satisfies the hypothesis, as a floorplan $F(n-1)$ can be obtained. The floorplan

$F(n)$ of $G_{\text{e}}(n)$ is obtained by placing $F(n-1)$ on the left and node v on the right, as shown in figure. (id)

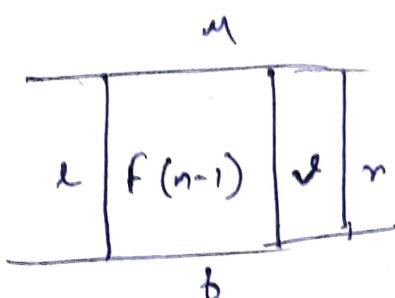
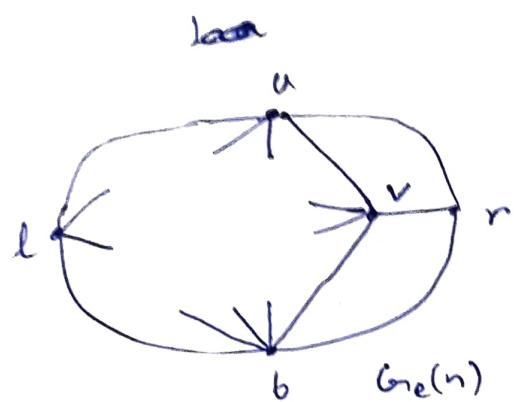
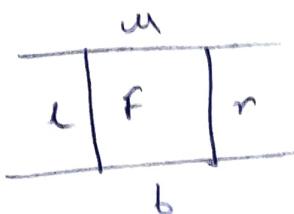
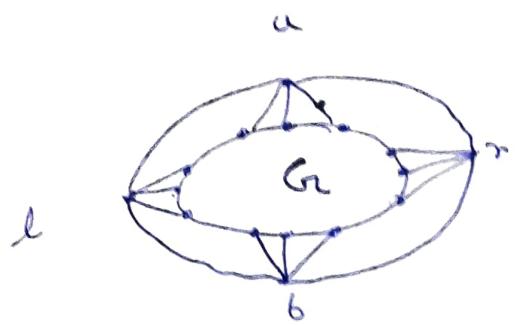


Fig. 1.(a)

Fig. 1.(b)

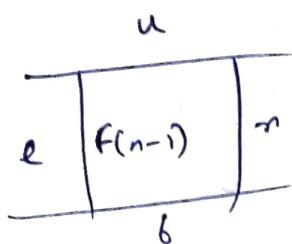
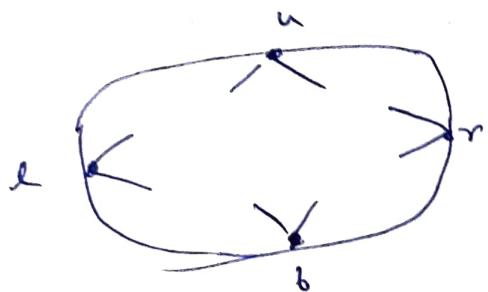


Fig. 1.(c)

Fig. 1.(d)

Now comes the case where none of r, u, l, b has degree 3, we find path $P_r = \{u = p_1, p_2, \dots, p_k = b\}$ in $G_c(n)$ from u to b with the following properties.

1. $p_2, \dots, p_{k-1} \notin \{r, u, l, b\}$

2. $(p_i, p_j) \notin G_c(n)$, for all distinct i, j and

3. $(p_i, l) \notin G_c(n)$, for some i , and $(p_j, r) \notin G_c(n)$ for some j .

Such path P_r is called vertical splitting. Similarly we can have horizontal splitting. One such path always exists if $G_c(n)$ consists of no complex triangles.

$G_{e(C_n)}$ decomposes along P_V to produce subgraphs

G_L & G_R , with vertices of Path P_V are duplicated

so they appear in both subgraphs. A vertex

v' and edges (P_i, v') ; $1 \leq i \leq n$; are added to

get obtain $\& G_{eL}$ and similarly a

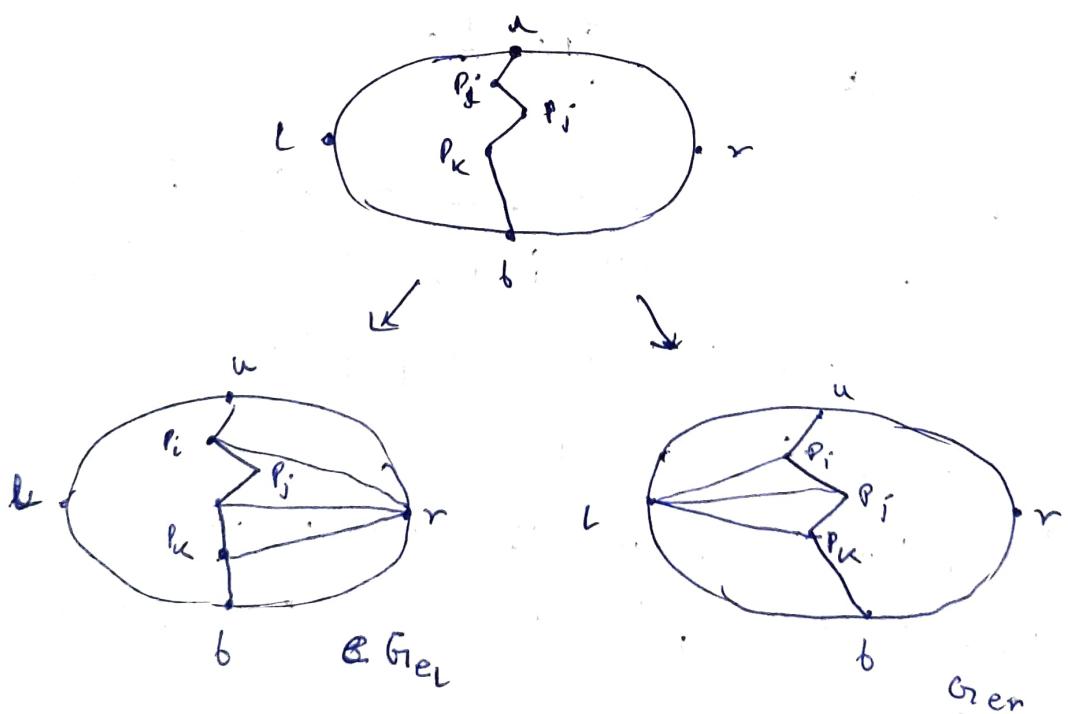
(or use vertex r' and edges (P_i, r')); $1 \leq i \leq n$,

are added to obtain G_{eR} . The ~~decomps~~

decomposition is illustrated in ~~Figure 2~~.

the figure below. From the properties of P_V , it can be shown that graph G_{eL} & G_{eR} both contain fewer than n vertices. Thus, the hypothesis applies and floorplan F_L and F_R are produced.

The floorplans F_L & F_R are merged to obtain the ~~two~~ floorplan G_{eF} .



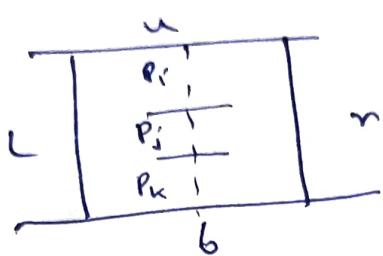
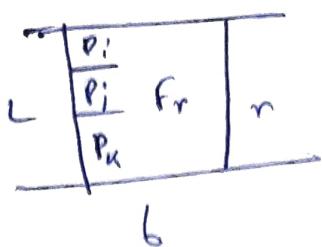
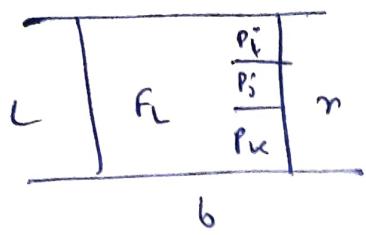


Fig: merger of F_L & F_r

5.

c)

i) Placement Cost Components :-

→ Area

- Would like to pack all the modules very tightly

→ Wire length (half-perimeter of the net boundary box)

- Minimize the average wire length.

- Would result in ~~tight packing~~ packing of the modules with high connectivity.

→ Overlap

- Cannot be prohibited by the mous, or used as penalty.
- Keep the cells from overlapping (mous cells apart)

→ Timing

- Not in 1-1 correspond with wire length minimization, but consist in the average.

→ ~~Percept~~ Congestion

- measure of reusability

- Want like to move the cells apart.

ii) Approaches for top ~~top-down~~ placement :-

→ Top-down

- partition-based placement

- Recursive bi-partition or quadrisection

- Here we try to partition the entire set into smaller subsets based on ~~new~~ some heuristics.

→ Iterative approach

- Simulated annealing or force directed (based on physical systems)

- Here we start with an initial placement (may be random) and iteratively apply the algorithm to improve the ratios like area to wire length.

→ Construction

- Here we start with a cross cells in the center, and place highly connected adjacent nodes in the form. This is similar to a bottom up approach.

iii) Force directed algorithm:

This utilizes the ~~or~~ similarity between the placement problem and the classical mechanics problem of a system of bodies attached to springs blocks connected by ~~are~~ nets are assumed to exert mutually attractive forces,

magnitude ~~are~~ dist b/w 2. blocks.

magnitude ~~are~~ weighted ~~is~~ sum of the nets b/w 2 blocks.
if the blocks are allowed to move freely, they would move freely ~~not~~ until equilibrium state is reached

- find equilibrium configuration of placement of blocks.

→ force considered in either horizontal or ~~and~~ vertical directions.

Model:-

- uses simulated springs

$$\text{Force}_{ij} = \text{weight}_{ij} \times \text{distace}_{ij}$$

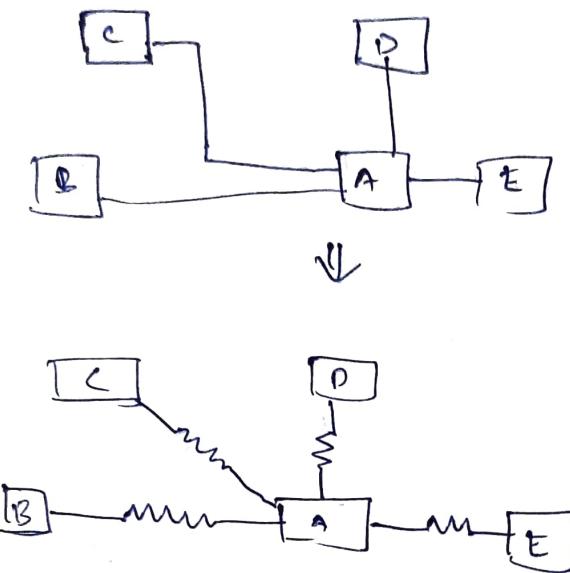
- cell size as repellent forces

- "vacat" regions work as "attracting" forces.

"overcrowded" regions work as "repelling" forces.

Algorithm :-

- solve a set of linear equations to find an intermediate solution (module/block locations)
- Repeat the process until equilibrium

Constructive Force-Directed Algorithm:-

- First, an initial placement is constructed by placing the modules so that they are in equilibrium with respect to the forces acting on them.
- That is, for any module M_j , $\sum_i k_{ij} (x_j - x_i) = 0$ and $\sum_i k_{ij} (\gamma_j - \gamma_i) = 0$ for all module M_i .
- How ever, trivial solution: $x_j = x_i$ for all i, j .
Everything placed on the same position.
- Need to have some way to avoid overlapping.
 - receive forces
 - connecting to fixed I/O pins on the boundary of the placement region
 - not really move to the equilibrium position, but a nearby position with out introducing overlapping.

Iterative Force Directed Algorithm:-

- Start with an initial position of modules
- The module M with maximum force acting on it is identified.
- Place M at its ideal position (x, y), where no force is acting on it.
- If it causes overlap with another module M' .
 - Move M' to where M was previously placed, or *
 - The resulting overlap may be tackled off at later stage.
- The above process is repeated for all badly placed modules.
- Each module can be displaced a constant number of times.

Simulated Annealing (SA) Placement:-

Stage 1:

- Models are moved between different rows as well as within the same row.
- module overlaps are allowed (to reduce running time).
- when temperature is reduced below a certain value, stage 2 begins.

Stage - 2 :

- Removes overlaps
- Annealing process continues, but only interchanges adjacent modules within the same row.

Algorithm SA.

begin

temp := INIT_TEMP

place := INIT_PLACEMENT

while (inner-loop-criterion = false) do

new-place := PERTURB(place);

 $\Delta C' := \text{cost}(\text{new-place}) - \text{cost}(\text{place}),$ if ($\Delta C < 0$) then place := new-place;else if ($\text{RANDOM}(0, 1) > e^{\Delta C / \text{temp}}$) then

place := new-place;

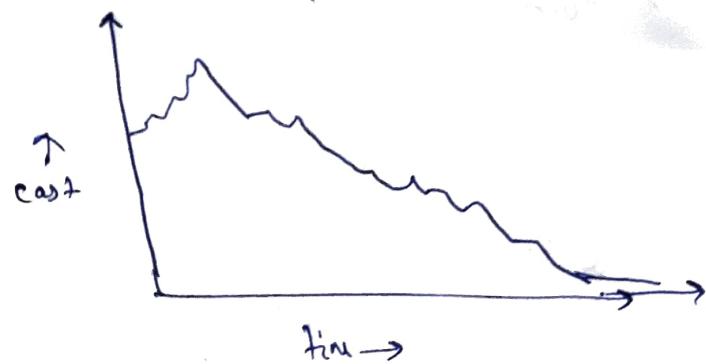
temp := SCHEDULE(-temp),

end;

Initial placement Improved through swaps and Moves.

Accept a swap/Move if it improves cost.

Accept a swap/Move that degrades cost under some probability condition.

All Possiblesolution space:- All possible arrangements of modules into rows possibly with ~~one~~ ~~one~~ overlaps.

Neighboring solutions :-

- 3 types of move \rightarrow Displace a module to a new location (M1)
- \rightarrow Interchange two modules (M2)
- \rightarrow Change the orientation of a module (M3)

Move Selection :-

→ Select between M1, M2 & M3 based on probability.

→ If a move of type M1 is chosen (for certain module) and it is rejected, then a move of type M3 (for the same module) will be chosen with probability 1/10.

Restriction on:

- How far a module can be displaced
- what pair of modules can be interchanged

Cost function :-

$$\Psi = C_1 + C_2 + C_3$$

$$C_1 = \sum_i (x_i w_i + R_i h_i) \text{ wire cost.}$$

x_i & R_i are horizontal ad vertical weights,
respectively.

C₂ = penalty for overlaps.

$$C_2 = \sum_{i+j} (O(i,j) + \alpha)^2$$

α - offset parameter to ensure $C_2 \rightarrow 0$ when $O \rightarrow 0$.

C₃ : Penalty function that controls the row length.

Desired row length = $d(r)$

$l(r)$ = sum of widths of the module in row r.

$$C_3 = \sum R |l(r) - d(r)|$$

Schedule :-

$$T_k = r(f_k) \cdot T_{k-1}, \quad f_k = 1, 2, 3, \dots$$

$r(f_k)$ increases from 0.8 to max value 0.94 at then
decreases to 0.1.

at each temp. $K \cdot n$ attempts σ is made

n = no. of modules

K = user specified const.