Bachelor of Technology in Instrumentation and Electronics Engineering, 2017-18
1st year, 2nd semester

DIGITAL ELECTRONICS

Time : Three hours | Full Marks : 100

Answer *ANY FIVE*

Q1. (a) Using JK-FF as memory element, realize a sequential **Binary to Gray** code converter. The input Gray bits are coming serially starting from the MSB.

(b) Draw the **p-MOS** circuit which realizes the following function :

F(A, B, C) = A'C + AB'C + B'

(c) Outputs of two CMOS gates should never be shorted together. Explain.

(10 + 6 + 4)

Q2. (a) Design a sequence generator which generates the sequence "**101110**" repeatedly. Use minimum number of **D-FFs**.

(b) Briefly explain the problem of **decoding spikes** and how it can be avoided ?

(15 + 5)

Q3. Realize a lock-out free **Div-by-6** synchronous counter using **T-FFs** as the memory elements.

(20)

Q4. (a) Use **Karnaugh Map** technique to obtain the minimized expressions for the following functions as indicated :

(i) ,F(W, X, Y, Z) = ∏M(1, 4, 6, 7, 9); **in minimized SOP form**

(ii) F(A, B, C, D) = AB'D + A'B'D' + AB' + B'C; **in minimized POS form**

(iii) F(A, B, C, D) = ∏M(3, 4, 5, 6, 7, 9, 13, 15); **in minimized NAND-NAND form**

(b) Realize a **T-FF** using **one SR-FF** as the memory element.

(4 x 3 + 8)

Q5. (a) Realize a **2:1** multiplexer using logic gates.

(b) Cascading the 2:1 multiplexers realize one **8:1** Multiplexer.

(c) Using two 2:1 multiplexers realize one **2-input XOR** function.

(d) Implement the following function using **one 8:1** multiplexer and **one 2:1** multiplexer **(if needed)** :

F(W, X, Y, Z) = WX'Z' + W'XZ' + WX' + YZ

(2 + 2 + 2 + 14)

Q6. Write short technical notes on : (4 x 5)

(a) Use of CMOS **transmission gates**.

(b) **Floating inputs** in TTL logic gates.

(c) Merits and demerits of **ring-counter**.

(d) **Difference** between Latch and Flip-Flop.

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