Ex/CSE/T/214/18/2015

BACHELOR OF COMPUTER SCIENCE AND ENGINEERING EXAMINATION, 2015

(2nd Year, 1st Semester)

DIGITAL CIRCUITS

Full Marks : 100 Time : Three Hours

The figures in the margin indicate full marks.

Answer any *five* questions.

1. With the help of circuit diagram explain the operations of DCTL and DTL gates. Compare their performances. 8+8+4

2. Draw the Transfer characteristics of a standard TTL gate. Justify the diagram. 4+16

3. (a) Explain the operation of a CMOS inverter. Why does it perform better than a MOS gate? 8+4

   (b) How can NAND and NOR gates be realised with CMOS ? 4

   (c) Discuss the issues related to the interfacing between CMOS and TTL gates. 4

[*Turn over*]

4. (a) An 555 IC Timer is connected in Astable mode of operation. Deduce expressions for the frequency of oscillations and duty cycle. 4+6+2

(b) In the above circuit oscillates at a frequency of 100 KHz with a duty cycle of 40%, design the circuit. The circuit is working at 15 Vdc. Use a 50 pf capacitor. 8

5. (a) With the help of a circuit diagram explain the operation of a 3tr/cell Memory. 8

(b) How can the stored information be maintained in such a memory ? 8

(c) How does it differ from a 1tr/cell memory ? 4

6. (a) How can you convert a single digit BCD data to Analog Voltage using weighted resistors ? 10

(b) What are the difficulties encounter with weighted resistors DAC ? When does it arise ? 4

(c) The output of a two digit BCD counter is to be converted to the corresponding Analog Voltages. How can it be implemented by using two of the above mentioned DAC's? 6

[*Turn over*]

7. (a) Why would one prefer using a Successive Approximation type ADC ? Justify your answer with the help of a diagram for a 3 bit ADC. 4+12

   (b) Discuss the functions of various interfacing signals in connection with the above ADC. 4

8. Write notes on any *four* of the following : 4×5

   (a) ECL ;

   (b) Tristate Buffer ;

   (c) nMOS inverter ;

   (d) Frequency Multiplication ;

   (e) EPROM ;

   (f) 2's complement DAC ;

   (g) Delta Modulation ;

   (h) Sample / Hold circuits.

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