Ref. No. : Ex/MECE 512/2018

M.TECH. VLSI AND MICRO ELECTRONICS
SECOND YEAR SECOND SEMESTER EXAM 2018

EMC/EMI AND SYSTEM TESTING AND TESTABLE DESIGN

Time: Three hours Full Marks: 50

[PART - I]

[Use separate answer scripts for each part]
Answer Q.1 and *any two* questions form the rest part

1. a) Determine a simple expression to convert (RMS) voltage in dBμV to dBm. [3]

   b) A 50-Ω source is connected to a 50-Ω receiver using 300 ft of RG58U coaxial cable. If the source output is 100 MHz and -30 dBm, determine the voltage at the receiver in mV and dBμV. The coaxial cable has 4.5 dB/100 ft loss at the frequency of the incident wave. [5]

   c) "What do you understand by - "CISPR 22 conducted emission limit for Class B digital devices is 56 dBmV QP ."? [2]

2. a) Discuss the effect of rise/fall time, repetition rate and duty cycle on spectral content of a trapezoidal pulse train. [10]

   b) A 5-V, 10-MHz oscillator having a rise/fall time of 10 ns and a 50% duty cycle is applied to a gate as shown in Fig. 1. Determine the value of the capacitance such that the fifth harmonic is reduced by 20 dB in the gate voltage $V_G(t)$. [10]

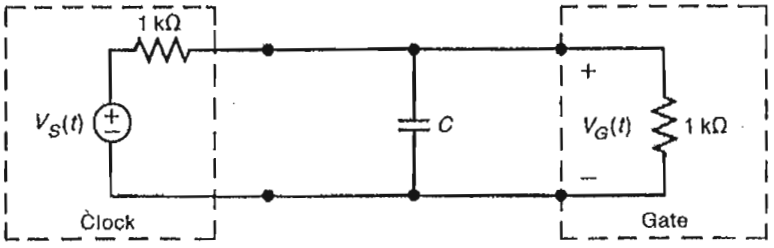
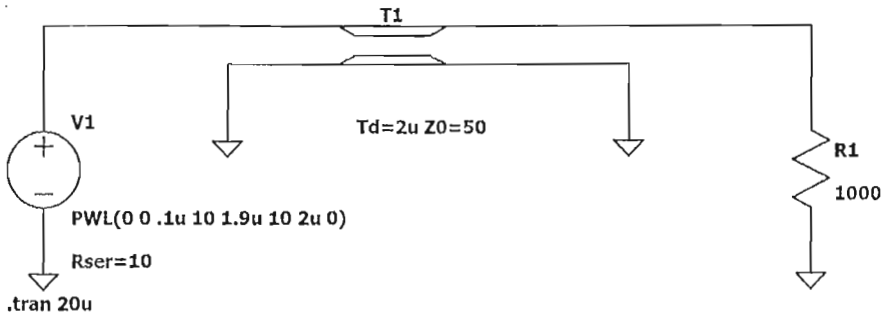


Fig. 1

3. Draw the input voltage vs time and output voltage vs time plot for 0 to 20 μs for the circuit shown in Fig.2. The source in the circuit can be represented by PWL function as shown in figure. Here the source is a trapezoidal pulse with delay = 0 and holds voltage sequence 0 V, 10 V, 10 V and 0V at 0 s, 0.1 μs, 1.9 μs and 2 μs, respectively. The source and load resistances are 10 Ω and 1k Ω, respectively. T1 represents a transmission line with characteristic impedance of 50 Ω and the path delay is 2μs.



[20]

Fig.2

4. a) Draw a simplified equivalent circuit of a non-ideal inductor including the effects of lead inductance and package capacitance showing Bode plots of the impedance magnitude and phase. Explain these plots. [6+2]

   b) A common-mode choke has self-inductance of 'L' and a coupling coefficient of 'M'. Determine its series effective impedances for common and differential-mode currents. [4]

   c) Draw the circuit diagram of typical power supply filter and briefly explain its operation in electromagnetic compatible designs. [8]

5. Write short notes on: [4x5=20]

   a) Line impedance stabilization network (LISN)
   b) Human body model for ESD and its use
   c) Shielding effectiveness and effects of apertures on it
   d) Arc suppression techniques

Ex/MECE 512/2018

M.Tech. VLSI And Micro Electronics Second Year Second Semester-2018

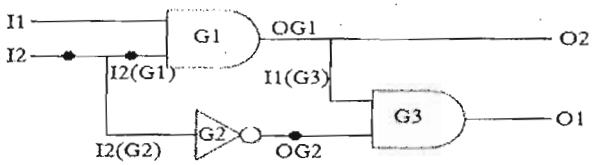
EMC/EMI & System Testing & Testable Design

Time : 1:30 Hr **Full Marks : 50**

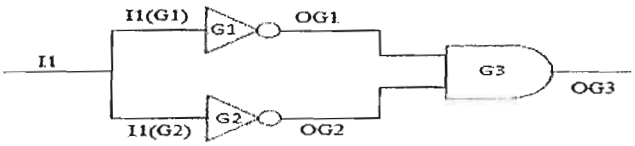
Part B: System Testing & Testable Design

[Question No 5 is compulsory and answer any 3 from the rest]

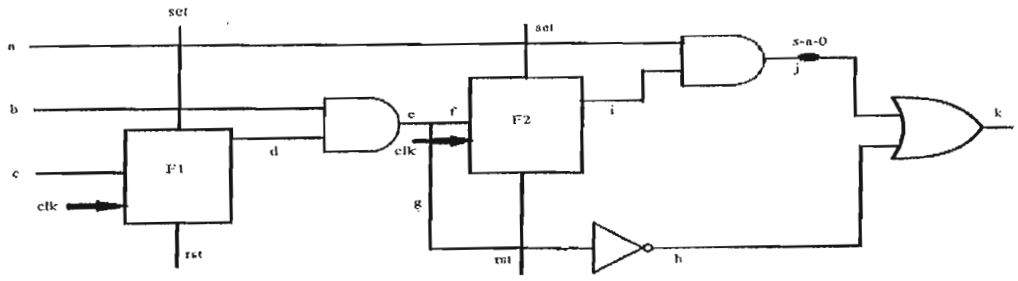
1. (a) Explain Parallel fault simulation through the following circuit for the faults, s-a-0 at I2, s-a-0 at I2(G1) and s-a-1 at OG2 respectively.



(b) Enlist the faults, which could be simulated in a single scan by deductive fault simulation process, providing '0' as an input at I1 node in the following circuit. State the rules of deductive fault simulation. [7+8]



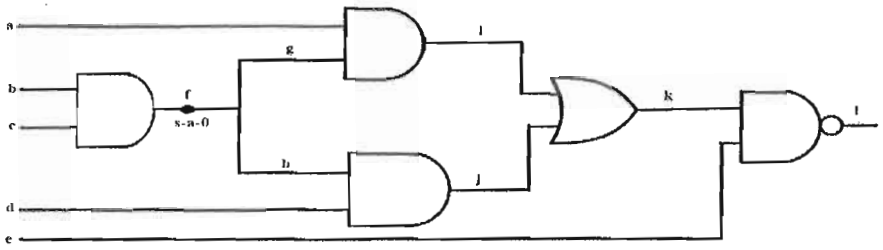
2. (a) For the circuit given below and the given fault, find out the test vector by using full scan chain based ATPG.



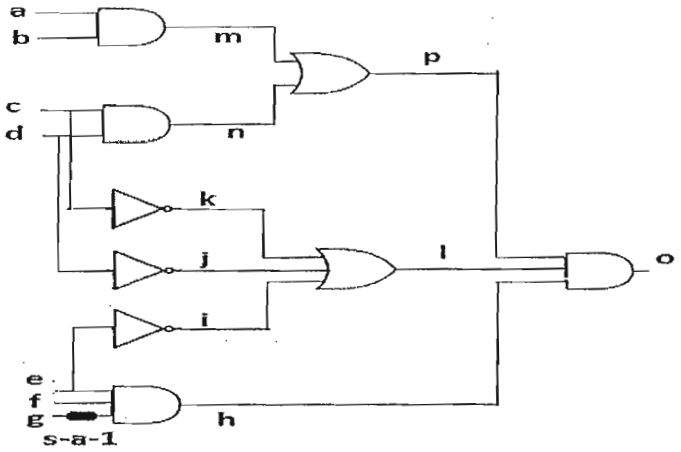
(b) Explain how the scan chain output itself reduces the complexity of the algorithm in finding the test vector.

(c) Draw the schematic diagram of an edge triggered muxed – D cell. [7+5+3]

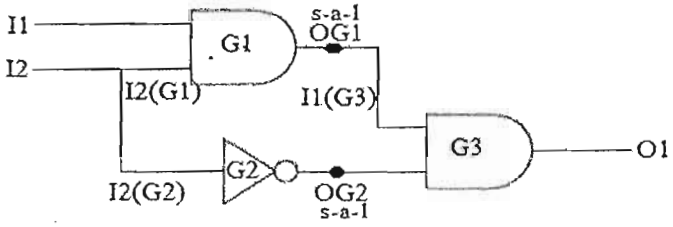
3.(a) Find the test vector for the following circuit for the given fault. Define D frontier. What are the D frontier gates for the given circuit? [8]



(b) Explain the line justification problem for this circuit and find the test vector for the given fault. Define J frontier. [7]



4. (a) Compare the difficulty levels of s-a-1 faults in the 2 nets given below [7]



(b) Derive the expression for controllability and observability for a 2 input AND gate and 2 input XOR gate [2x4=8]

5. Short notes [any one] [5]

(a) Redundant hardware

(b) Boolean difference based ATPG

(c) Flowchart of D algorithm