No. Ex/MECE 518/2018

M.TECH. VLSI AND MICRO ELECTRONICS FIRST YEAR SECOND SEMESTER-2018

Subject : EMBEDDED AND REAL TIME SYSTEM

Time : 3 Hrs **Full Marks :**

Use Separate Answer scripts for each Part

PART - I

Answer any five questions

1. Identify the key difference between hard real-time, soft real-time and firm really-time systems. Give at least one example in each category.
   Identify and represent the timing constraints in the following air-defence system by means of EFSM. An incoming missile must be detected within 0.2 seconds of its entering the radar coverage area. The intercept missile should be engaged within 5 seconds of detection of target missile. The intercept missile should be fired after 0.1 seconds of its engagement but no later than 1 Sec. 3+2+5

2. Design a 8 bit GCD calculator system consisting of Data path and schematic of the controller with the relevant control signals. 7+3

3. A cyclic scheduler is to be used to run the following set of periodic tasks on a uniprocessor. Select an appropriate frame size.

Task	Start Time (m Sec)	Execution Time (m Sec)	Period (m Sec)	Relative Deadline (m Sec)
T1	0	25	100	150
T2	0	10	30	50
T3	0	50	150	200

   What are advantages of cyclic scheduler over table driven scheduler . 7+3

4. Consider the following of four independent real-time periodic tasks.

Tas k	Start Time (m Sec)	Execution Time (m Sec)	Period (m Sec)
T1	20	25	150
T2	40	10	50
T3	20	15	50
T4	60	50	200

   Assume that task T3 is more critical than task T2. Check whether the task set can be feasibly scheduled using RMA. Show all the intermediate steps. 10

5. Consider the following set of three independent real-time periodic tasks.

Tas k	Start Time (m Sec)	Execution Time (m Sec)	Period (m Sec)	Relative deadline(m sec)
T1	20	25	150	100
T2	60	10	50	30
T3	40	50	200	150

Determine whether the task set is schedulable on a uniprocessor using EDF. Show all intermediate steps in your computation. 10

6. What is high level synthesis? State the steps involved in the process.
Convert the following code segment to a suitable Data path using high level synthesis process with the constrained of one operation per schedule.

```
x = a + b ;
y = c – d ;
z = x * d ;
```

10

7. How the task behaviour can be described in terms of Task states? Give a brief idea of the architecture of Real time operating system and discuss its relative merits and demerits.

3+5+2

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EMBEDDED AND REAL TIME SYSTEM

PART-II

(50 Marks for each part)

Use separate Answer Script for each part

Answer any *five* of the following questions

1.
a) What do you mean by embedded systems? Explain with example.
b) Briefly explain design methodologies of an Embedded System.
c) Describe technological aspects of Embedded System.

3+4+3

2.
a) Describe memory distribution of an Embedded System.
b) Why cache memory is required in an Embedded System.
c) Describe various cache memory mapping techniques.

4+2+4

3.
a) Describe embedded DSP architecture.
b) Briefly explain various cache memory replacement techniques.

5+5

4.
How do you interface a LED with PIC16F877 microcontroller? Draw the circuit connection diagram.
Write appropriate program for it in PIC C. 5+5

OR

a) What do you mean by 'Thumb' instruction in ARM?
b) Describe in brief advance features of ARM processor.
c) Content of register R1=0xEF00DE12. Find the result in the destination register, after the following instruction is executed.
LSL R1, #8

3+4+4

5.
a) Briefly explain about the various flags of an ARM7 processor.
b) Write an assembly language program to find the sum 4X+3Y+7Z (X=3, Y=5, Z=4) for ARM-7.

4+6

6. Write short note on
a) I^2C
b) IEEE 802.11

5+5