MASTER OF ENGINEERING EXAMINATION, 2018

(1st Year, 2nd Semester)

(ELECTRICAL, E.T.C.E., BIO-MEDICAL)

EMBEDDED SYSTEMS

Time: 3 Hours Full Marks: 100

Answer any FOUR questions.

1. a) Design an *Application Specific Integrated Circuit* (ASIC) for the following sequential state machine:

   "An output pulse z is to be coincident with the first x_2 pulse immediately following two or more consecutive x_1 pulses." [13]

   b) Design an automaton capable of recognizing a string: a-a-a-b by two or more ways. Label the transitions (arcs/edges) by symbols: x, y, z and w arbitrarily. Select a lattice diagram with nodes symbolized by 1, x, y, z, w and 0 as you wish. Now using the lattice diagram, determine the lattice belief that the automaton will recognize the string: a-a-a-b. [12]

2. a) Develop a VHDL program for your own state machine with at least 2 states and 4 state-transitions. [13]

   b) Construct a *Programmable Array Logic* (PAL) to realize the following switching functions.

   $Y_1 = A\,B'C' + AB'$

   $Y_2 = ABC' + A'C'$ [6]

   c) Design a *Programmable Logic Device* (PLD) to realize the following switching function with feedback.

   $Y_1 = AB'C' + AB'\,Y_1'$ [6]

3. a) Draw the timing diagrams for the signals used in the Centronix bus of a Dot Matrix Printer. [8]
   b) Develop an interfacing of the dot matrix printer to transfer a block of data bytes from system RAM to printer. [5]

c) Write an *Assembly Level Program* (ALP) to transfer 10 bytes of data from users' RAM to the printer. [12]

4. a) Construct a Task Graph with the following precedence relationships: $T_1 \rightarrow T_2$, $T_1 \rightarrow T_3$, $T_2 \rightarrow T_4$, $T_3 \rightarrow T_4$, $T_3 \rightarrow T_5$, $T_5 \rightarrow T_6$, $T_6 \rightarrow T_7$, $T_4 \rightarrow T_7$. [3]

b) Given two hardwares: H_1 and H_2, and 2 software platforms: S_1 and S_2. Prepare a Table to represent the timing required for each task on each piece of hardware or software. Using only time-criteria determine the minimum time required to execute the complete job comprising 7 tasks, introduced in Part (a). [10]

c) Write down the main steps of an *Ant Colony Optimization* (ACO) algorithm. Explain how you can solve the Hardware/Software partitioning problem by the ACO algorithm. [12]

5. a) Graphically illustrate the fuzzy reasoning technique with the rule:
If x is A_1 Then y is B_1,
Else If x is A_2 Then y is B_2,
where the parameters have their usual meanings. Presume that the observation is "x is A'". [8]

b) Show the realization of the above reasoning on a VLSI engine. [9]

c) State Dinning Philosophers' problem and solve it by a Petri Net. [8]

6. a) Explain the RST hardware interrupt-handling mechanism in 8085A microprocessor system. [6]

b) Using RST 7.5 and RST 5.5 interrupts, design a scheme for set-point changing in a process control loop without shutting down the plant. Develop necessary Assembly Level Program to explain your solution. [9]

c) With a neat diagram, explain how you will interface 4KB RAM chips to develop a 16 KB RAM memory in an embedded system. Show the interconnection of the address decoder with the CPU and the memory chips, and also narrate the Hex beginning and end addresses of the RAM memory chips. If the processor has 64 K address space, how many possible addresses can be used to access each memory location? [10]

7. Write notes on any TWO of the following:

a) FPGA realized with p-ASIC architecture,
b) PROM-PLA-PAL-PLD-CPLD development,
c) Hierarchical State Machine with application,
d) Stochastic Automaton. [12 ½ × 2]