

AD 0332

## TRANSISTOR-TRANSISTOR LOGIC (TTL)

The usefulness of a DTL gate is limited by its speed of operation. A principal source of this limitation can be appreciated by considering the circuit of Fig. 6.1-1, where a single-input gate is shown. With a view toward the TTL gate shortly to be introduced, we have explicitly shown the input diode as a diode-connected transistor, i.e., a transistor with collector and base connected.

Consider, now, that the input to the gate is at logic level 1. Then current flows through  $T_2$  and diode  $D$  and into the base of  $T_3$ . The transistor  $T_3$  is driven to saturation, and the gate output is at logic level 0. Now change the input to logic level 0. Then the output of the gate should go to logic level 1. However, this transition to logic level 1 will not take place until transistor  $T_3$  comes out of saturation, passes through the active region, and eventually goes to cutoff. Cutoff however, will not be reached until the stored base charge of  $T_3$  has been removed (see Sec. 1.20). During this removal of the stored base charge, transistor  $T_1$  is ON, but transistor  $T_2$  and diode  $D$  are cut off. Hence, there is no alternative: the base charge must leak off through the resistor  $R_b$ .

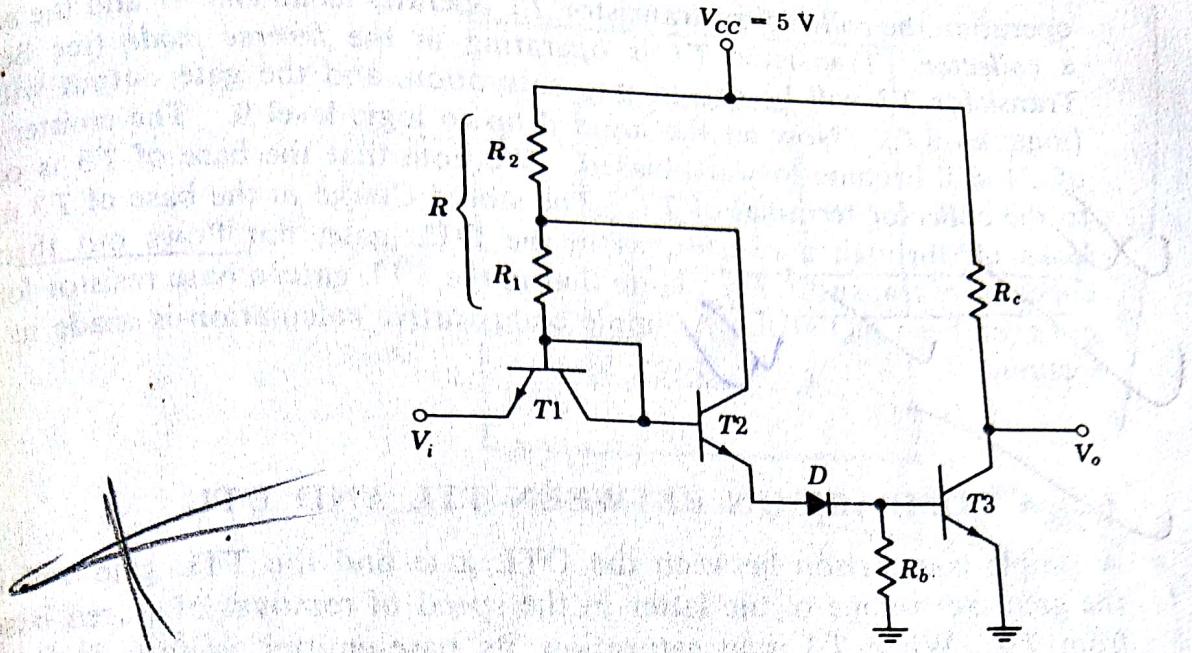


FIGURE 6.1-1  
The basic DTL gate.

or dissipate by recombination. This relatively slow mechanism for the removal of stored charge establishes the essential speed limitation of the DTL gate.

The DTL speed limitation is overcome in the transistor-transistor-logic gate (TTL). In its simplest and most elemental form this gate appears as shown in Fig. 6.1-2. (For the moment, we picture a single input gate.) There is a certain similarity between the TTL gate of Fig. 6.1-2 and the DTL gate of Fig. 6.1-1. In the TTL gate the input transistor  $T_1$  is connected as a transistor, the collector-base connection being removed. Transistor  $T_2$  and diode  $D$  of the DTL gate are removed, and the collector of  $T_1$  is connected directly to the base of  $T_3$ .

When, in the TTL gate, the input is high, the emitter-base junction of  $T_1$  will be back-biased and current will flow, through  $R$  and through the forward-biased base-collector junction of  $T_1$  into the base of  $T_3$ . In this mode of

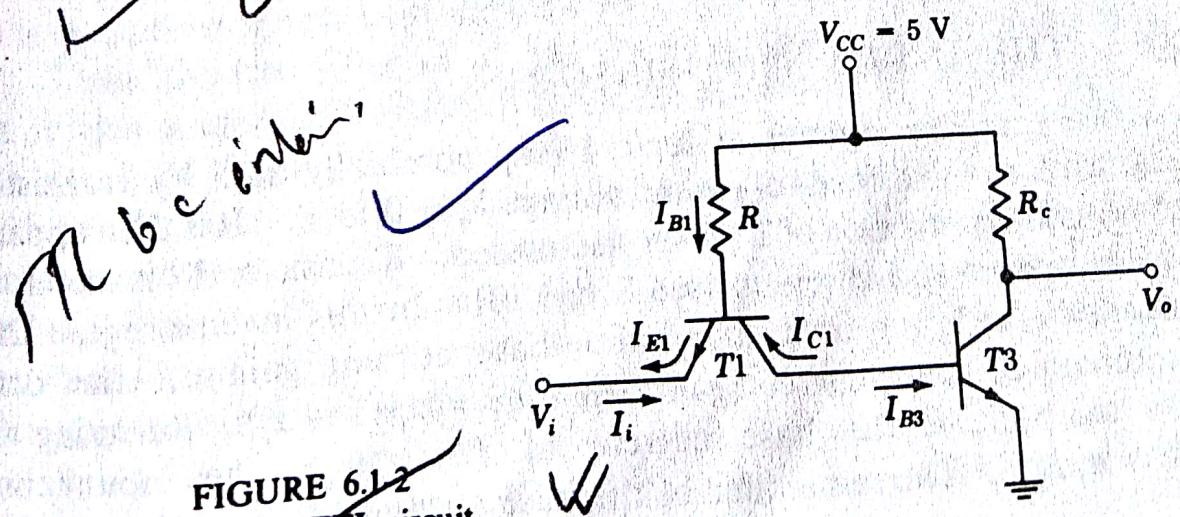


FIGURE 6.1-2  
A basic TTL circuit.

operation the *collector* of transistor  $T_1$  operates as an *emitter* and the *emitter* as a *collector*. Transistor  $T_1$  is operating in the *inverse mode* (see Sec. 1.10). Transistor  $T_3$  will be driven into saturation, and the gate output will be low (logic level 0). Now let the input drop to logic level 0. The emitter junction of  $T_1$  will become forward-biased. We note that the base of  $T_3$  is connected to the collector terminal of  $T_1$ . The stored charge in the base of  $T_3$  no longer leaks off through a resistor, as in the DTL gate, but flows out through the collector of transistor  $T_1$ . Note that in the TTL gate, a base resistor for  $T_3$  has not even been included. A simple comparative calculation is made in the next section.

## 6.2 A COMPARISON BETWEEN TTL AND DTL

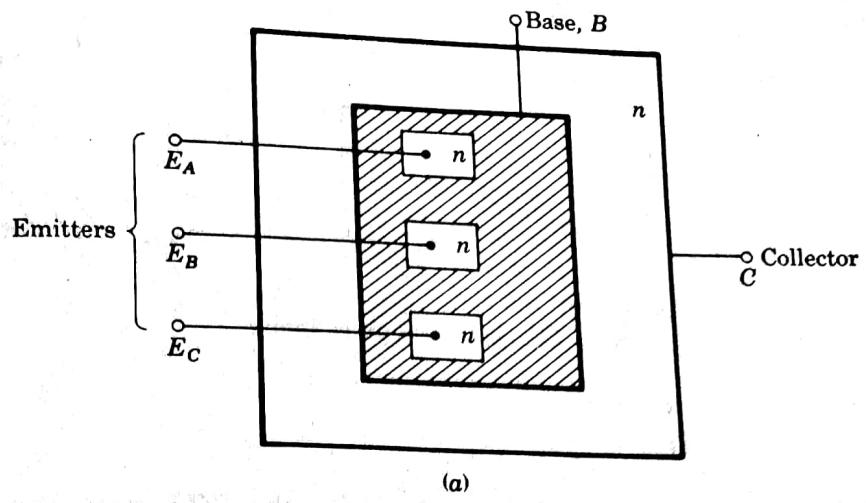
A simple comparison between the DTL gate and the TTL gate will illustrate the great advantage of the latter in the speed of removal of stored base charge from  $T_3$ . When  $T_3$  is in saturation, its base-emitter voltage is  $V_\sigma = 0.75$  V. When, in Fig. 6.1-1, diode  $D$  is cut off, the initial current out of the base of  $T_3$  is  $V_\sigma/R_b = 0.75/2 \text{ k}\Omega \approx 0.38 \text{ mA}$ .

On the other hand, in the TTL gate, consider that the input is grounded. Then the base-emitter junction of  $T_1$  is forward-biased, and we shall assume that the voltage across the junction is 0.75 V. As we shall see, in a typical case the resistor  $R$  in Fig. 6.1-2 is  $R = 4 \text{ k}\Omega$ . Then the base current in  $T_1$  is  $I_{B1} = (5 - 0.75)/4 \text{ k}\Omega \approx 1.1 \text{ mA}$ . Initially, transistor  $T_1$  is operating in its active region, since the base-to-ground voltage of  $T_3$ , which is also the collector-to-ground voltage of  $T_1$ , is initially  $V_\sigma = 0.75$  V and therefore  $V_{CE1} = 0.75$  V. We then observe that the initial collector current in  $T_1$ , which is also the rate at which the stored base charge of  $T_3$  is being removed, is  $h_{FE} I_{B1}$ , where  $h_{FE}$  is the current gain of  $T_1$ . Even if we allow an  $h_{FE}$  no larger than  $h_{FE} = 20$ , we find the discharge rate to be  $h_{FE} I_{B1} = 20(1.1) = 22 \text{ mA}$ , which is to be compared with 0.38 mA in the DTL case.

This faster removal of the charge stored in  $T_3$  results in TTL gates which operate at propagation delay times that are one-tenth those of DTL gates.

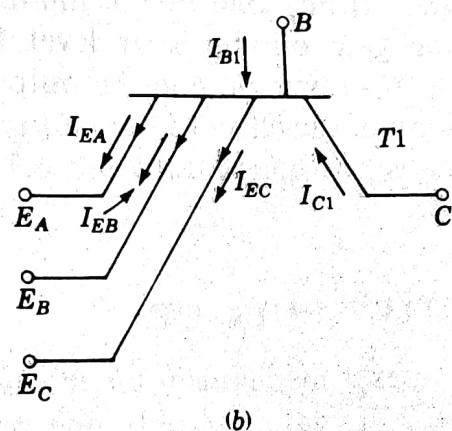
## 6.3 THE INPUT TRANSISTOR

When the gate input is at logic 1 (say nominally at 5 V), transistor  $T_3$  is in saturation with a base-to-ground voltage  $V_\sigma = 0.75$  V. It is then apparent that the base-emitter junction of  $T_1$  is reverse-biased. Transistor  $T_1$  is therefore operating in its inverse active region (see Sec. 1.10). In this inverse region the transistor operates with an inverse common-base current gain  $\alpha_I$ , the corresponding common-collector current gain being  $h_{FC} = \alpha_I/(1 - \alpha_I)$ . Referring to Fig. 6.1-2, we see that if the base current of  $T_3$  is  $I_{B3}$ , the input current  $I_1$ , is  $I_1 = \alpha_I I_{B3}$ . The remainder of the base current for  $T_3$  is supplied by the base



(a)

*multi emitter  
transistor*



(b)

FIGURE 6.3-1  
(a) Pictorial representation and (b) symbol of multiemitter transistor.

current  $I_{B1}$  of  $T1$ , so that  $I_{B1} = (1 - \alpha_I)I_{B3}$ . In a TTL gate, the input transistor  $T1$  is deliberately designed to have a very low value of inverse current gain. Values in the range  $\alpha_I \approx 0.02$  or even lower are typical of TTL gates. With such a value of  $\alpha_I$  only 2 percent of the required base current of  $T3$  need be supplied by the input driving source, while the other 98 percent is supplied through  $R$  from  $V_{cc}$ . Thus, the low value of  $\alpha_I$  has the advantage of minimizing the loading on a driving source, at least when the input is at logic level 1.

For the circuit of Fig. 6.1-2 to serve as a gate, additional inputs must be provided. These additional inputs may be made available by paralleling  $T1$  with additional input transistors. All such input transistors would then have their collectors tied together and their bases similarly joined. In practice we do not parallel input transistors but construct a transistor with a single common collector, a single common base, and multiple emitters. The physical structure of such a *multiple-emitter transistor* is shown in Fig. 6.3-1a, and its circuit symbol is shown in Fig. 6.3-1b. A three-input TTL gate using such a multiple-emitter

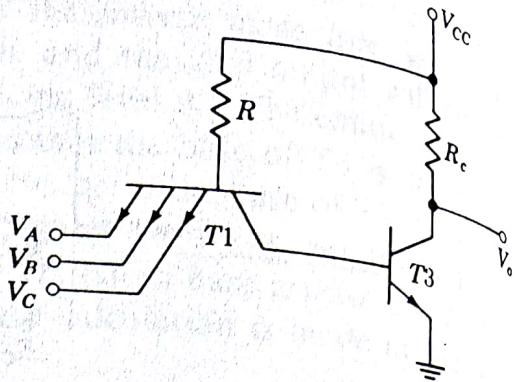


FIGURE 6.3-2  
A basic TTL gate with three inputs.

transistor is shown in Fig. 6.3-2. Like the DTL gate, the TTL gate of Fig. 6.3-2 is a NAND gate. If any one of the inputs is at logic level 0, transistor  $T_3$  is cut off and the gate output is at level 1. If all the inputs are at logic 1, transistor  $T_3$  is in saturation and the output is at logic 0.

A discussion of the effect of the multiple-emitter transistor on the operation of the TTL gate is postponed until Sec. 6.7.

#### 6.4 THE ACTIVE PULL-UP

Providing as it does a mechanism for the rapid removal of the output transistor base charge, the TTL gate has only one principal remaining limitation on the gate speed. This results from the effects of capacitance which appears across the output of the gate, from the collector of  $T_3$  to ground. This capacitance is composed of the capacitance of the output transistor itself, of the capacitance to ground of wires which connect the gate output to other gates, and of the input capacitances of these other gates or other devices which are being driven. When  $T_3$  is driven to cutoff, this output capacitance must charge from  $V_{CC}$  through the pull-up resistor  $R_c$ . If the output capacitance is  $C_o$ , the capacitance charges and the output rises from logic 0 to logic 1 with a time constant  $R_c C_o$ . This time constant can be reduced by reducing the resistance of  $R_c$ . Such a reduction, however, would increase the power dissipation in  $R_c$  and, of course, in transistor  $T_3$  while  $T_3$  is conducting. In addition, the reduction in  $R_c$  would make it more difficult to saturate  $T_3$ .

The expedient used in TTL gates to hasten the charging of output capacitance substantially without introducing an unacceptable increase in power dissipation is shown in Fig. 6.4-1. Here, the pull-up resistor  $R_c$  in Fig. 6.3-2 is replaced with the active devices, transistor  $T_2$  and diode  $D$ . This circuit is recognized to be an *active pull-up* similar to the active pull-up used in RTL gates (Fig. 4.7-1) as well as in DTL gates. We now discuss, qualitatively, the operation of the circuit of Fig. 6.4-1.

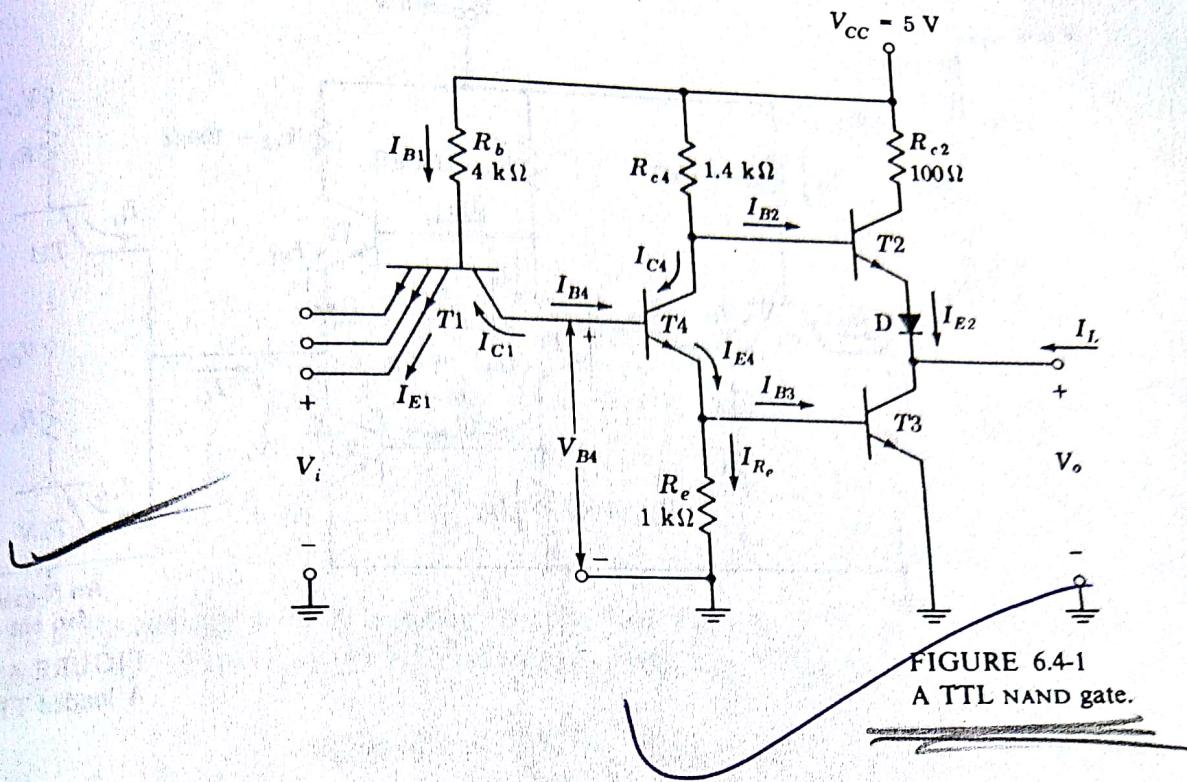


FIGURE 6.4-1  
A TTL NAND gate.

It is intended, in the active pull-up circuit of Fig. 6.4-1, that when the output  $V_o$  is at logic 0, transistor  $T_3$  will be in saturation and  $T_2$  cut off. Alternatively, when the output goes from logic 0 to logic 1,  $T_3$  is to cut off,  $T_2$  is to go ON, and the output capacitance is to charge through the series combination of the emitter-follower transistor  $T_2$  and diode  $D$ . This switching of transistors  $T_3$  and  $T_2$  is accomplished by transistor  $T_4$ , which is a *phase splitter* used to provide the bases of  $T_3$  and  $T_2$  with voltages which swing in opposite directions so that when one transistor of the  $T_3$ - $T_2$  *totem-pole* pair is being driven ON, the other is being driven OFF and vice versa.

To appreciate the need for the diode  $D$  located between the output transistor pair, consider the situation when the inputs are all at logic 1, in which case the output should be at logic 0. With all inputs at logic 1, transistors  $T_4$  and  $T_3$  will both be in saturation (we shall verify later that such is indeed the case). Then the collector voltage of  $T_3$  is  $V_{CE}(\text{sat}) \approx 0.2$  V while the collector voltage of  $T_4$  is  $V_{CE4}(\text{sat}) + V_{BE3} \approx 0.2 + 0.75 = 0.95$ . In this case, if diode  $D$  were not present, the base-emitter voltage of  $T_2$  would be  $V_{C4} - V_{C3} = 0.95 - 0.2 = 0.75$  V, and  $T_2$  would also be in saturation. We require however that at the logic 0 output  $T_2$  be cut off. With the diode  $D$  present, the 0.75 V drop between the collectors of  $T_4$  and  $T_3$  must divide between diode  $D$  and the base-emitter junction of  $T_2$ . In this case neither diode  $D$  nor transistor  $T_2$  will be forward-biased sufficiently to pass any appreciable current.

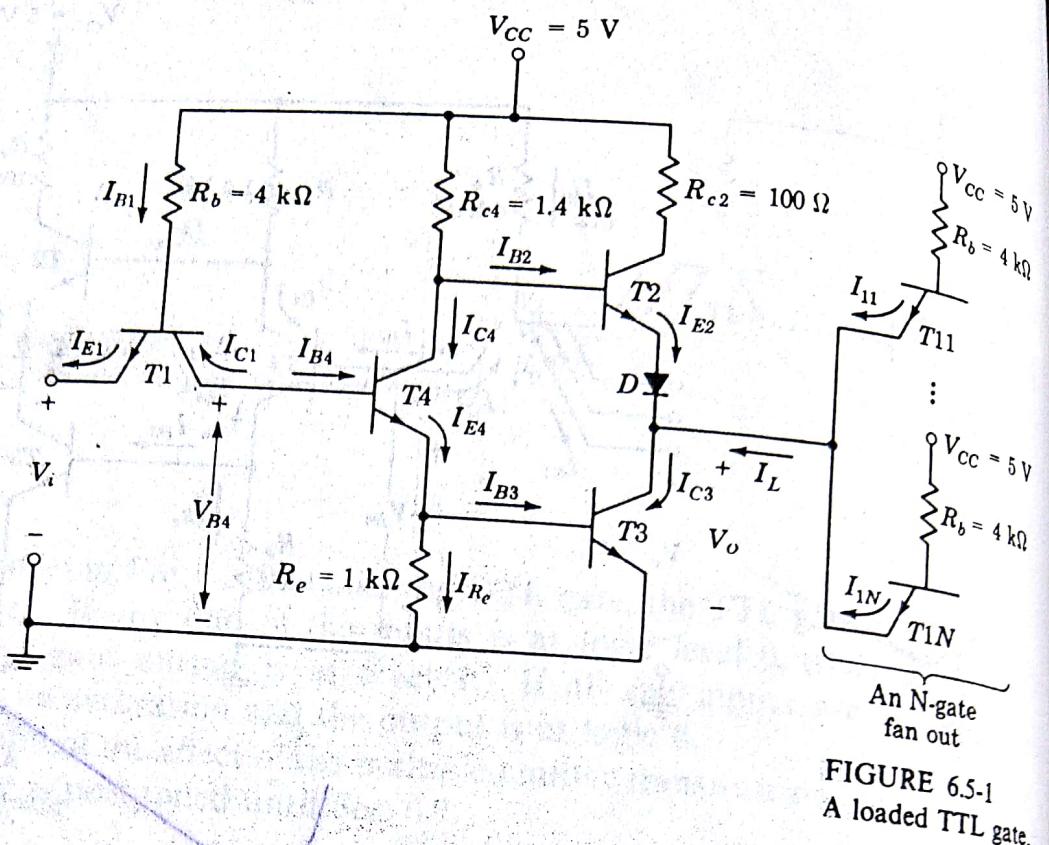


FIGURE 6.5-1  
A loaded TTL gate.

## 6.5 INPUT-OUTPUT CHARACTERISTIC NEGLECTING THE INPUT TRANSISTOR

We shall now undertake to describe and make calculations concerning the operation of the TTL gate shown in Fig. 6.5-1. Since this gate is substantially more complicated than either the RTL gate or the DTL gate, we find it convenient to consider at the outset not the overall input-output characteristic but the characteristic relating the gate output voltage  $V_o$  to the base voltage  $V_{B4}$  of transistor  $T4$ . In Sec. 6.6 we shall consider the relation between  $V_{B4}$  and the input voltage  $V_i$ ; and by combining these two characteristics, we shall deduce the overall characteristic.

Let us start with  $V_{B4} = 0$  V. In this case  $T4$  and  $T3$  are cut off. Transistor  $T2$  supplies a current  $I_{E2}$  to the  $N$  driven gates. The emitter current  $I_{E2}$  is equal to the current  $-I_L$ ,  $I_L$  being the load current. Following common convention, the positive direction of  $I_L$  is taken into the gate.

The circuit from which to calculate the output voltage  $V_o$  is given in Fig. 6.5-2. The output voltage  $V_o$  is given by

$$V_o = V_{cc} - R_{c4} I_{B2} - V_{BE2} - V_D \quad (6.5-1)$$

where  $V_{cc}$  ( $= 5$  V) is the supply voltage,  $R_{c4} I_{B2}$  is the drop across  $R_{c4}$ ,  $V_{BE2}$  is the base-emitter voltage of  $T2$ , and  $V_D$  is the drop across the diode. Assuming

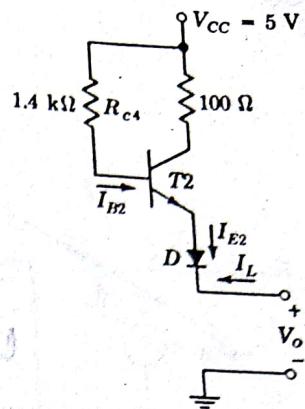


FIGURE 6.5-2  
Output circuit used to calculate  $V_o$  when  
 $T_3$  and  $T_4$  are cut off.

that  $T_2$  is operating in its active region, the base current is  $I_{B2} = I_{E2}/(h_{FE} + 1) = -I_L/(h_{FE} + 1)$ . Equation (6.5-1) becomes, since  $h_{FE} \approx h_{FE} + 1$ ,

$$V_o = V_{CC} + \frac{R_{c4} I_L}{h_{FE}} - V_{BE2} - V_D \quad (6.5-2)$$

When  $T_3$  is cut off,  $V_o$  is at its logic 1 level. To calculate the load current  $I_L$  we observe that the input transistors of the  $N$  driven gates in Fig. 6.5-1 are each operating in their inverse mode, just as for the input transistor in the basic circuit shown in Fig. 6.1-2. In each of the *driven* gates (only the input transistors of which are shown in Fig. 6.5-1) transistors  $T_3$  and  $T_4$  are in saturation. Hence,  $V_{B4} = V_{BE3} + V_{BE4} = 0.75 + 0.75 = 1.5$  V. The base current of  $T_4$  is being supplied almost entirely through the collector junction of the input transistor. This input transistor is operating in its active (albeit inverse) mode, and so we shall allow a drop of 0.7 V across its base-collector junction. Altogether the voltage at the base of the input transistor is  $1.5 + 0.7 = 2.2$  V. The drop across each base resistor  $R_b$  is therefore  $5.0\text{ V} - 2.2\text{ V} = 2.8$  V. The current through  $R_b$  is  $2.8/(4\text{ k}\Omega) = 0.70\text{ mA}$ . Assuming that the input transistors  $T_{11} - T_{1N}$  each have  $h_{FC} = 0.02$ , the input current to each driven gate, is  $0.70(0.02) = 14\text{ }\mu\text{A}$ .

If the driving gate  $T_2$  were fanned out to a single gate, with the emitter junction and diode carrying so small a current ( $14\text{ }\mu\text{A}$ ) we could reasonably take  $V_{BE2} = V_D = V_\gamma = 0.65$  V. In this case also, the drop across  $R_{c4}$  [the second term in Eq. (6.5-2)] is negligible, and we have

$$V_o \approx V_{CC} - 2V_\gamma = 5.0 - 2(0.65) = 3.7\text{ V} \quad (6.5-3)$$

Suppose, on the other hand, we drive 10 gates (as we shall see, a fan-out of 10 is the conservative figure generally specified by manufacturers) and suppose we allow as a worst case that  $h_{FC}$  may be as large as 0.1. In this case the load current would be of the order of 1 mA. Even with this current the drop across

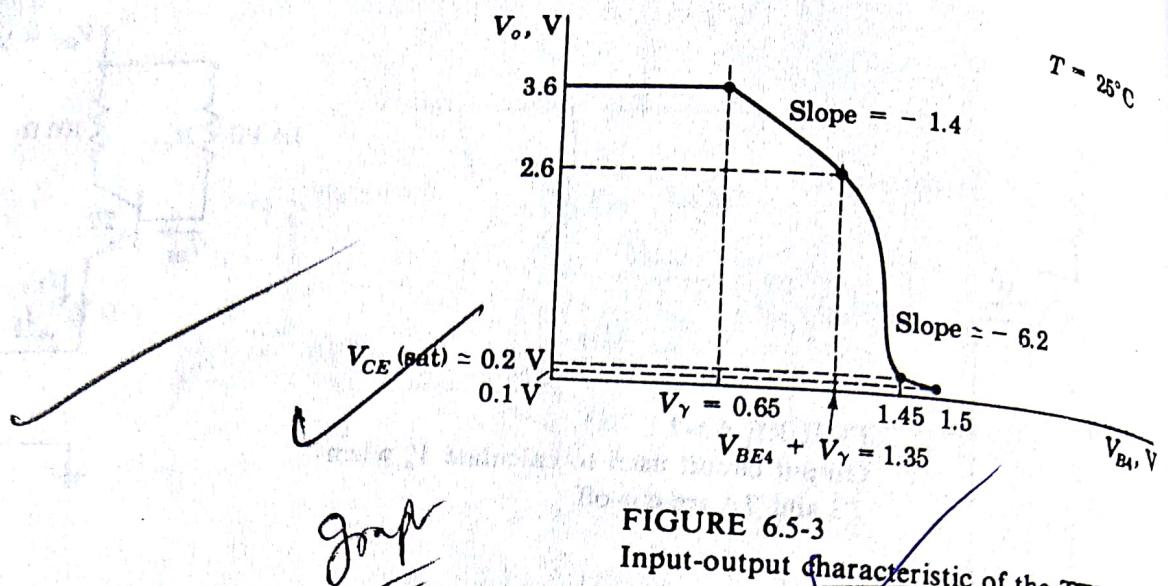


FIGURE 6.5-3

Input-output characteristic of the TTL gate.

$R_{c4}$  would continue to be negligible, but it would be more reasonable to take  $V_{BE2} = V_D = 0.75$  V. The output voltage would then be

$$V_o = V_{cc} - 2V_o = 5.0 - 2(0.7) = 3.6 \text{ V} \quad (6.5-4)$$

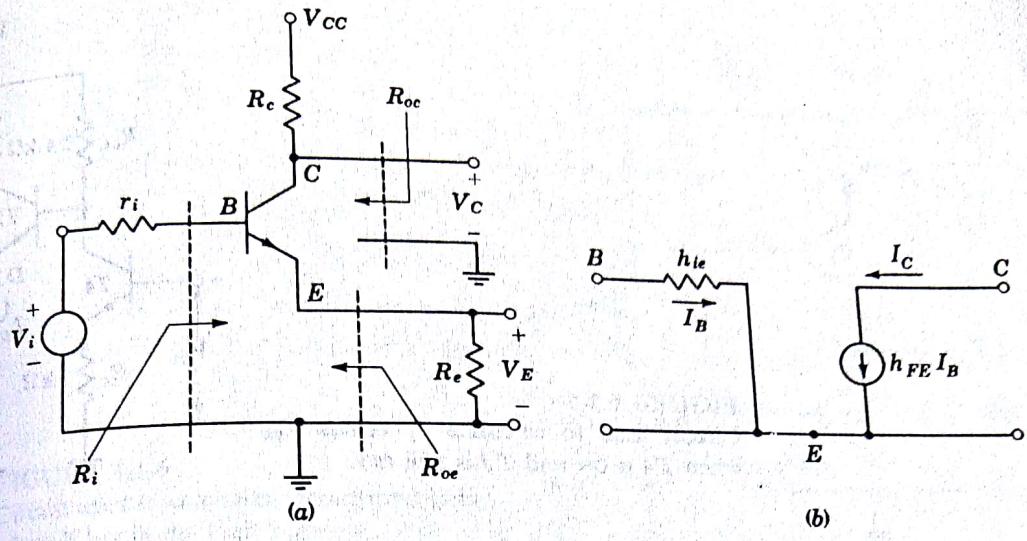
We therefore see that when  $V_o$  is in the 1 state, the value of  $V_o$  is only slightly dependent on the load current and hence on the fan-out. We shall accordingly simplify matters by assuming that when  $T4$  (and hence  $T3$ ) are cut off, the output voltage  $V_o$  is as given in Eq. (6.5-4). This value of the output voltage is given in the plot of the input-output characteristic shown in Fig. 6.5-3.

**Phase splitter** Before continuing, it will be well to digress briefly to review some of the gain and impedance characteristics of a phase splitter. Such a stage is shown in Fig. 6.5-4a. The transistor is assumed to be biased into its active region, although the biasing arrangements are not explicitly shown. The stage has a collector resistor  $R_c$  and an emitter resistor  $R_e$  and is driven by a source of impedance  $r_i$ . We assume that, in the active region, the transistor can be represented by the equivalent circuit involving hybrid parameters, as shown in Fig. 6.5-4b. We then find that the impedances and the voltage gains are given by the equations in Fig. 6.5-4. Rather typically we might assume that  $h_{FE} = 50$  and  $h_{ie} = 1 \text{ k}\Omega$ . If  $h_{FE} R_e \gg h_{ie} + r_i$ , these equations for impedances and gains can be simplified to the useful approximations

$$R_i \approx h_{FE} R_e \quad (6.5-5a)$$

$$A_E = \frac{V_E}{V_i} \approx 1 \quad (6.5-5b)$$

$$A_C = \frac{V_C}{V_i} = -\frac{R_c}{R_e} \quad (6.5-5c)$$



$$R_i = h_{ie} + (h_{FE} + 1) R_e$$

$$A_E = \frac{V_E}{V_i} = 1 - \frac{h_{ie} + r_i}{R_i}$$

$$R_{oe} = \frac{h_{ie} + r_i}{h_{FE}}$$

$$A_C = \frac{V_C}{V_i} = -\frac{R_c}{R_e} A_E$$

$$R_{oc} = R_c$$

FIGURE 6.5-4

(a) A phase splitter. (b) Equivalent circuit of a transistor.

Returning to the circuit of Fig. 6.5-1, let us allow \$V\_{B4}\$ to increase from zero. When \$V\_{B4}\$ attains a value of about \$V\_{B4} = V\_y = 0.65\$ V, transistor T4 will begin to enter its active region. However, because of the drop across the base-emitter junction of T4, T3 will remain cut off. Hence, at this point, the circuit used to calculate the response of the output voltage \$V\_o\$ to \$V\_{B4}\$ is as shown in Fig. 6.5-5.

We now calculate the slope of the transfer characteristic in the region where T3 is cut off. The gain \$A\_2 \equiv \Delta V\_o / \Delta V\_{B2}\$ from the base of T2 to the output is the gain of an emitter-follower and, hence, as in Eq. (6.5-5b) is \$A\_2 \approx 1\$. The gain provided by T4 is [from Eq. (6.5-5c)] \$A\_4 = -R\_{c4}/R\_e = -1.4\$. The overall gain \$A = \Delta V\_o / \Delta V\_{B4}\$ is \$A\_2 A\_4 = -1.4\$, as indicated in Fig. 6.5-3.

With further increase in \$V\_{B4}\$, T3 will eventually reach the cut-in point. At this point T4 is in the active region, and we shall correspondingly assume a base-emitter voltage drop of \$V\_{BE4} = 0.7\$ V. Assuming, as usual, that T3 comes out of cutoff when the voltage drop across its base-emitter junction is \$V\_{BE3} = V\_y = 0.65\$ V, we estimate that T3 begins to turn on when \$V\_{B4} = V\_{BE4} + V\_{BE3} = 0.7 + 0.65 = 1.35\$ V. At the point where T3 just turns ON, the current through \$R\_{c4}\$ is \$V\_y/R\_e = 0.65/1 \text{ k}\Omega = 0.65 \text{ mA}\$. The corresponding drop through \$R\_{c4} = 1.4 \times 0.65 = 0.9\$ V. Hence,

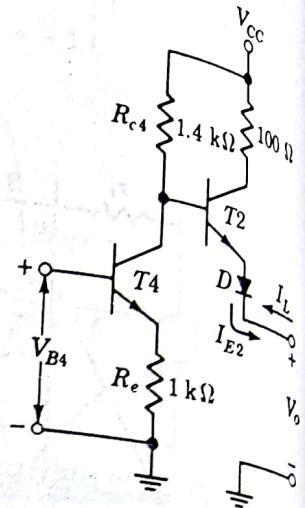


FIGURE 6.5-5

Circuit used to calculate  $V_o$  versus  $V_{B4}$  when  $T4$  is ON and  $T3$  is still OFF.

as appears in Fig. 6.5-3, when  $V_i = 1.35$  V,  $V_o$  is 0.9 V lower than the value in Eq. (6.5-4), that is  $V_o = 3.5 - 0.9 = 2.6$  V.

When  $T3$  turns ON, the incremental gain  $A = \Delta V_o / \Delta V_{B4}$  increases and the output voltage  $V_o$  begins to drop more sharply with increasing  $V_{B4}$  than when  $T3$  was OFF. This increase in gain has a twofold source. On the one hand  $V_o$  drops, simply because  $T3$  begins to conduct. On the other, with  $T3$  ON, the emitter resistor  $R_e$  is shunted by the impedance seen looking into the base of  $T3$ . The resistance in the emitter circuit of  $T4$  is thereby decreased, and, as indicated in Eq. (6.5-5c), the gain of  $T4$  increases. The following illustrative calculation will display these two sources of increased gain.

**EXAMPLE 6.5-1** In the circuit of Fig. 6.5-1, let  $T3$ ,  $T2$ , and  $T4$  be assumed to be in the active region, each with parameters  $h_{ie} = 1$  kΩ and  $h_{FE} = 50$ . Calculate the incremental gain  $A = \Delta V_o / \Delta V_{B4}$ .

**SOLUTION** With  $h_{ie} = 1$  kΩ shunting  $R_e = 1$  kΩ, the equivalent resistor in the emitter of  $T4$  is  $R'_e = 500$  Ω. The condition  $h_{FE} R'_e \gg h_{ie}$  continues to apply. Hence, the gain from base to emitter of  $T4$ , which is also the gain from the base of  $T4$  to the base of  $T3$ , continues to have the value unity. In Fig. 6.5-1 we have redrawn the relevant portion of Fig. 6.5-1, with  $R_e$  replaced by  $R'_e$ , the connection from the emitter of  $T4$  to the base of  $T3$  removed, and with a generator  $\Delta V_{B3} = \Delta V_{B4}$  applied at the base of  $T3$ .

Let us now apply the principle of superposition and calculate separately the output voltage  $\Delta V_o$  due individually to each of the generators  $\Delta V_{B4}$  and  $\Delta V_{B3}$ . The gain, referring to the generator  $\Delta V_{B4}$ , is calculated as before, except that  $R_e$  is now replaced by  $R'_e$ . We then have

$$A_4 = \frac{\Delta V_{C4}}{\Delta V_{B4}} = -\frac{R_{c4}}{R'_e} = -\frac{1.4}{0.5} = -2.8 \quad (6.5-6)$$

Next we calculate the gain due to  $\Delta V_{B3}$ . Referring to Fig. 6.5-4, we can readily verify

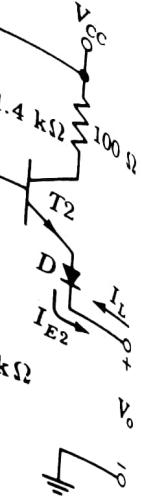
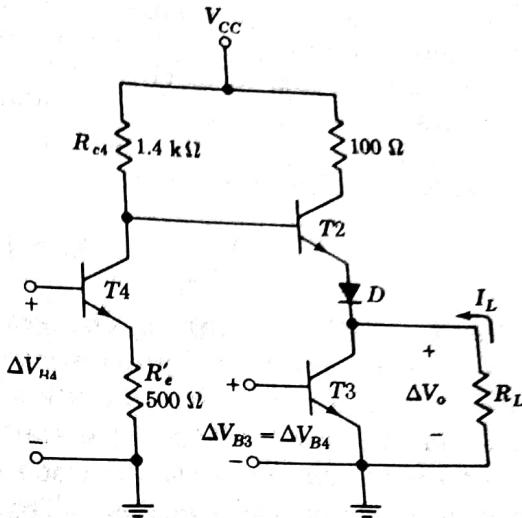


FIGURE 6.5-6  
Circuit used to calculate incremental gain when  $T_3$  is in the active region.



that a common-emitter amplifier stage operating without an emitter resistor and with a collector resistor  $R_c$  has a gain

$$A_3 = \frac{\Delta V_o}{\Delta V_{B3}} = -\frac{h_{FE}}{h_{ie}} R_c \quad (6.5-7)$$

The equivalent collector resistor  $R_c$  with which  $T_3$  operates is the incremental impedance seen looking back into the diode  $D$  and the emitter of  $T_2$ . The transistor impedance  $\Delta V_{BE}/\Delta I_E \equiv h_{ie}$ . The impedance  $\Delta V_{BE}/\Delta I_E = \Delta V_{BE}/h_{FE} \Delta I_E = h_{ie}/h_{FE}$ . Since the same current flows in the diode as in  $T_2$ , we let the diode impedance equal the transistor impedance  $h_{ie}/h_{FE}$ . To find  $R_c$  we add the diode impedance to the impedance seen looking into the emitter of  $T_2$ , as given by the equation for  $R_{oe}$  in Fig. 6.5-4. We have

$$R_c = \frac{h_{ie}}{h_{FE}} + \frac{h_{ie} + R_{c4}}{h_{FE}} = \frac{10^3}{50} + \frac{(1.4 + 1) \times 10^3}{50} = 68 \Omega \quad (6.5-8)$$

a value small enough in comparison with any load the gate will encounter to permit us to ignore the load. From Eqs. (6.5-7) and (6.5-8) we have

$$A_3 = \frac{\Delta V_o}{\Delta V_{B3}} \approx -\frac{h_{FE}}{h_{ie}} R_c = -\frac{1.4 + 2}{1} = -3.4 \quad (6.5-9)$$

The total incremental output voltage  $\Delta V_o$  is therefore  $\Delta V_o = A_4 \Delta V_{B4} + A_3 \Delta V_{B3}$ . However,  $\Delta V_{B3} = \Delta V_{E4} \approx \Delta V_{B4}$  since  $T_4$  is an emitter follower. Hence,  $\Delta V_o = (A_4 + A_3) \Delta V_{B4}$ , and the overall gain is

$$A = \frac{\Delta V_o}{\Delta V_{B4}} = A_4 + A_3 = -2.8 - 3.4 = -6.2 \quad (6.5-10)$$

The calculation in Example 6.5-1 indicates an abrupt change in the magnitude of the gain from 1.4 to 6.2 when  $T_3$  turns on. Actually we

assumed an abrupt change in the input impedance  $h_{ie}$  of  $T_3$  from  $h_{ie}$  infinite below cutoff to  $h_{ie} = 1 \text{ k}\Omega$  above cutoff. It is the finite value of  $h_{ie}$  that yields the nonzero gain  $A_3$  as given in Eq. (6.5-7), and it is the finite value of  $h_{ie}$  that increases the gain  $A_4$  above its initial value of 1.4. However, the parameter  $h_{ie}$  depends on the emitter current of  $T_3$  and the extent to which the transistor has been driven into saturation. It is readily established that

$$h_{ie} \approx (1 + \sigma h_{FE}) \frac{V_T}{I_E} \quad (6.5-11)$$

Hence, as  $T_3$  turns ON,  $h_{ie}$  changes gradually from an extremely large value to a value which gets progressively smaller as  $T_3$  draws more and more current and tends toward saturation. Thus, the magnitude of the incremental gain in the circuit of Fig. 6.5-6 starts at 1.4 when  $T_3$  is OFF, increases when  $T_3$  turns ON, has the value 6.2 when  $h_{ie} = 1 \text{ k}\Omega$ , and increases still more as the current in  $T_3$  increases further. These features appear in the plot of the input-output characteristic shown in Fig. 6.5-3.

Referring once more to Fig. 6.5-1, we see that with still further increases of  $V_{B4}$ ,  $T_3$  is driven eventually to saturation. Assuming, as we have, that at saturation the base-to-emitter voltage of a transistor is  $V_\sigma = 0.75 \text{ V}$ , we would have saturation  $V_o \approx 0.2 \text{ V}$  when

$$V_{B4} = V_{BE4} + V_\sigma = 0.7 + 0.75 = 1.45 \text{ V} \quad (6.5-12)$$

This estimate has been included on the plot of Fig. 6.5-3.

When  $V_{B4}$  is increased beyond 1.45 V to 1.5 V both transistors  $T_4$  and  $T_3$  are saturated and  $T_2$  is cut off. In this case  $T_3$  is deeply saturated and  $V_o \approx 0.1 \text{ V}$ . Then collector current  $I_{C3} = I_L$ , and the load current is now positive. This current is calculated in Sec. 6.9.

## 6.6 INPUT-OUTPUT CHARACTERISTIC OF THE INPUT TRANSISTOR

The plot of Fig. 6.5-3 relates the output voltage  $V_o$  to the base voltage  $V_{B4}$ . Of much greater interest is the input-output characteristic that relates  $V_o$  to the input voltage  $V_i$ , shown in Fig. 6.6-1. We now study the operation of transistor  $T_1$  to enable us to determine the relation between  $V_i$  and  $V_o$ .

As we have noted, when  $V_i$  is at a high voltage corresponding to logic 1, the input transistor  $T_1$  operates in the active inverse mode. The collector current  $I_{C1}$  which is the base current  $I_{B4}$  of  $T_4$  is supplied principally by the base current  $I_{B1}$  of  $T_1$ . The current gain  $h_{FC}$  in this inverse mode is extremely low by deliberate transistor design ( $h_{FC} \approx 0.02$ ), so that the input source  $V_i$  supplies only about 2 percent of the base current of  $T_4$ . Under these circumstances  $T_4$  and  $T_3$  are in saturation,  $V_{B4} = 0.75 + 0.75 = 1.5 \text{ V}$ , and the gate output  $V_o$  is at logic 0. This situation prevails so long as  $V_i$  is sufficiently positive with respect to  $V_{B4}$  ( $2V_o = 1.5 \text{ V}$ ) to maintain  $T_1$  in the active inverse region.

(6.5-11)

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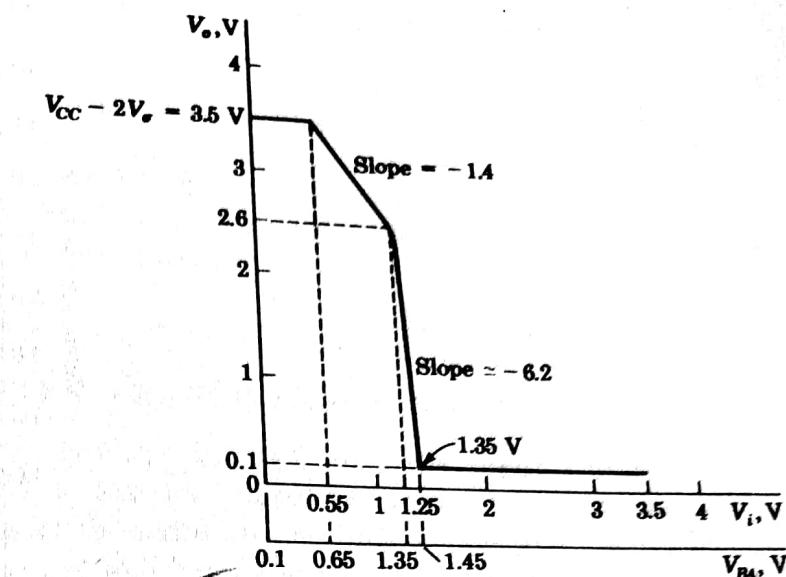


FIGURE 6.6-1  
Input-output characteristic of a loaded TTL gate.

We shall now show that as  $V_i$  falls, then, at least up to the point where  $V_i = 2V_o$  ( $= 1.5$  V), the transistors  $T_4$  and  $T_3$  remain in saturation and consequently  $V_o$  remains at logic 0. With  $V_i = 2V_o$ ,  $V_{CE1} = 0$  V, and  $T_1$  is in saturation. From Eq. (1.10-11) we find that when  $V_{CE1} = V_{CE}(\text{sat}) = 0$ ,  $\sigma = -1/(h_{FE} + h_{FC}) \approx -1/h_{FE}$  since  $h_{FE} \gg h_{FC}$ . Applying the definition of  $\sigma$  to transistor  $T_1$ , we have that  $\sigma = I_{C1}/h_{FE} I_{B1}$ . Substituting in this definition the value  $\sigma = -1/h_{FE}$ , we find that  $-I_{C1} = I_{B1}$ . Hence, the emitter current of  $T_1$  is now zero. However, the emitter current of  $T_1$  supplied only 2 percent of the base current of  $T_4$ , and this small loss of base current will hardly affect  $T_4$  or  $T_3$ . Hence,  $V_o$  remains at logic 0.

As  $V_i$  falls to voltages lower than  $2V_o = 1.5$  V, the base current  $I_{B1}$  will be diverted away from the base-collector junction of  $T_1$  into its base-emitter junction. Eventually, the base current of  $T_4$  will be reduced to a value where the transistor  $T_4$  will be at the verge of coming out of saturation. We calculate now the voltage  $V_i$  corresponding to this situation. We have often noted that when a transistor is comfortably inside the saturation region, its collector-emitter voltage is  $V_{CE}(\text{sat}) = 0.2$  V. At the very edge of saturation a more reasonable number is  $V_{CE}(\text{sat}) = 0.3$  V. Referring to Fig. 6.5-1, since  $T_2$  is OFF when  $T_3$  is ON, we have

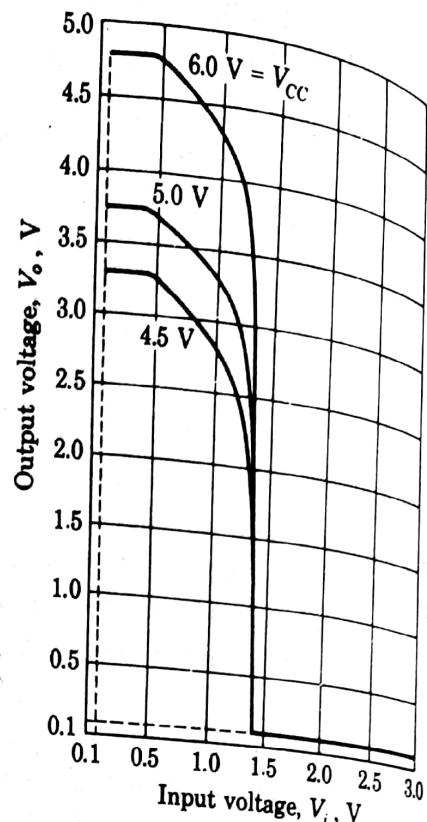
$$V_{CC} = R_{c4} I_{C4} + V_{CE4}(\text{sat}) + V_{BE3} \quad (6.6-1)$$

or

$$5 = 1.4 \times 10^3 I_{C4} + 0.3 + 0.75 \quad (6.6-2)$$

from which

$$I_{C4} = 2.8 \text{ mA} \quad (6.6-3)$$



**FIGURE 6.6-2**  
Medium-speed TTL transfer characteristics  $V_{cc} = 4.5, 5.0$ , and  $6.0\text{ V}$ ;  $T_A = 25^\circ\text{C}$ .

Since  $T_4$  is at the edge of saturation,  $I_{C4} = h_{FE} I_{B4}$ ; therefore using  $h_{FE} = 50$ ,

$$-I_{C1} = I_{B4} = \frac{I_{C4}}{h_{FE}} = \frac{2.8\text{ mA}}{50} = 56\text{ }\mu\text{A} \quad (6.6-4)$$

The base voltage  $V_{B4}$  is 1.5 V. We allow a voltage drop of 0.7 V across the collector junction of  $T_1$  since this junction is carrying only  $56\text{ }\mu\text{A}$ . The base-to-ground voltage of  $T_1$  is  $1.5 + 0.7 = 2.2\text{ V}$ . Consequently the base current of  $T_1$  is  $I_{B1} = (5 - 2.2)/(4\text{ k}\Omega) = 0.7\text{ mA}$ . We can now calculate the parameter  $\sigma$  for transistor  $T_1$ ; we find

$$\sigma = \frac{I_{C1}}{h_{FE} I_{B1}} = \frac{-56 \times 10^{-6}}{50(0.7) \times 10^{-3}} = -1.6 \times 10^{-3} \quad (6.6-5)$$

This value of  $\sigma$  is so close to  $\sigma = 0$  that we shall make no error in assuming  $\sigma = 0$ . In this case  $V_{CE}(\text{sat})$  is given by Eq. (1.10-4), and we have

$$V_{CE1} \approx V_T \ln \frac{1}{\alpha_I} \quad (6.6-6)$$

For  $\alpha_I = 0.02$ ,  $V_{CE} \approx 100\text{ mV}$ . Thus, the voltage  $V_i$  at which  $T_4$  comes out of saturation is about 0.1 V lower than the corresponding voltage  $V_{B4}$ . Hence, while in Fig. 6.5-3, the saturation region begins at  $V_{B4} = 1.5\text{ V}$ , in Fig. 6.6-1 it begins at  $V_i = 1.4\text{ V}$ .

As  $V_i$  continues to decrease, the current  $I_{B4} = -I_{C1}$  continues to decrease, becoming zero when  $T_4$  cuts off and remaining zero thereafter. Hence,  $\sigma$ , which has the value given by Eq. (6.6-5) when  $T_4$  is in saturation, falls to  $\sigma = 0$  when

$T_4$  cuts off and remains at zero thereafter. Hence, again  $V_i$  is 0.1 V lower than  $V_{B4}$ . It is now apparent that a plot of the overall input-output characteristic ( $V_o$  versus  $V_i$ ) of the TTL gate is the same as the plot of  $V_o$  versus  $V_{B4}$  shifted along the voltage axes to the left by amount 0.1 V. Such an overall characteristic is shown in Fig. 6.6-1 and is to be compared with the characteristics shown in Fig. 6.6-2. These latter characteristics are typical measured characteristics supplied by manufacturers.

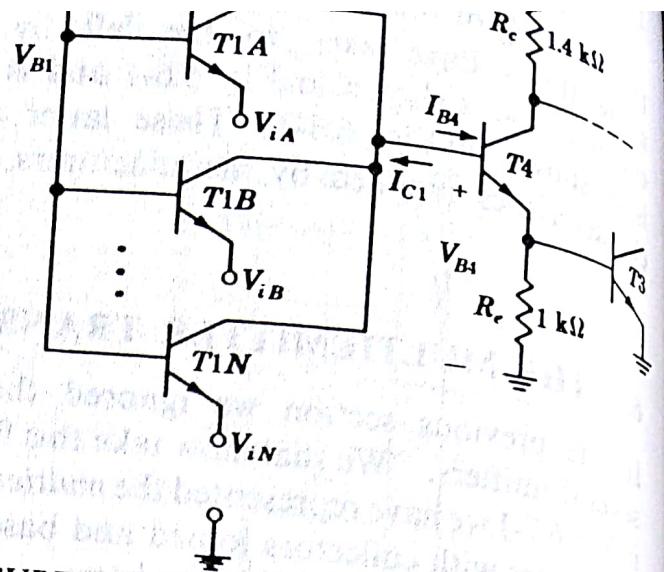
## 6.7 THE MULTIEmitter TRANSISTOR

In the previous section we ignored the fact that the input transistor has several emitters. We shall now take this feature into account. For convenience, in Fig. 6.7-1 we have represented the *multiemitter transistor* as an array of individual transistors with collectors joined and bases joined. The inputs  $V_{iA}, V_{iB}, \dots, V_{iN}$  are applied to the individual emitters.

Suppose now that all inputs are at the logic level 1, corresponding nominally to  $V_{iA} = V_{iB} = \dots = V_{iN} = V_{CC} - 2V_\sigma = 3.5$  V. All input transistors  $T_1$  are now operating in the inverse active region. We assume tentatively that transistors  $T_3$  and  $T_4$  are in saturation. Thus, the voltage  $V_{B4} = V_\sigma + V_\sigma = 1.5$  V while  $V_{B1} = 0.7 + 1.5 = 2.2$  V. The current through  $R$  is then  $I_{B1} = (5.0 - 2.2)/(4 \text{ k}\Omega) = 0.7$  mA. In this mode of operation the combined emitter current  $I_E = -h_{FC} I_{B1}$ , where  $h_{FC}$  is the inverse current gain corresponding to  $\alpha_I$ . Now  $h_{FC} = \alpha_I/(1 - \alpha_I) \approx \alpha_I$  since  $\alpha_I \ll 1$ . Using  $\alpha_I = 0.02$ , we have  $I_{E1} = -0.02(0.7)$  mA = -0.014 mA. Thus, the total base current of  $T_4$  is  $I_{B4} \approx 0.7$  mA. This is the same result calculated in Sec. 6.6 for a single-emitter input transistor  $T_1$ .

We note again that the base current required to drive  $T_4$  comes almost entirely from  $V_{CC}$  through  $R_b$ . The total current required from the gate driving  $T_{1A}, T_{1B}, \dots, T_{1N}$  is 2 percent of the base current  $I_{B4}$ . If there are  $N$  inputs, each driving gate need supply only  $2/N$  percent of this current.

Next, let us consider that one of the input emitters, say the emitter of  $T_{1A}$ , is at logic level 0, which corresponds to about 0.2 V, the saturation voltage of the driving gate. Then, as we have seen in Sec. 6.6,  $T_{1A}$  will be in saturation, and  $V_{B4} = V_{iA} + V_{CE}(T_{1A}) \approx 0.2 + 0.1 = 0.3$  V. Transistors  $T_4$  and  $T_3$  are therefore cut off, as required. Now, while  $T_{1A}$  is operating in saturation with its emitter junction forward-biased and carrying an emitter current very large in comparison with its collector current, let us assume that the emitters of each of the other "transistors"  $T_{1B}, \dots, T_{1N}$  are in the logic 1 state, with  $V_i = 3.5$  V. These transistors are operating in the inverse active mode with their base-collector junctions forward-biased and their emitters reverse-biased. We note further that since  $V_{iA} = 0.2$  V and  $T_{1A}$  is saturated,  $V_{B1} = V_{iA} + V_{BE}(T_{1A}) = 0.2 + 0.75 = 0.95$  V. Also, the collector voltages of transistors  $T_{1B}, \dots, T_{1N}$  are equal to  $V_{B4}$ , where  $V_{B4} = 0.3$  V. Hence, the voltage drops across the



**FIGURE 6.7-1**  
Circuit to show operation of the multiemitter transistor.

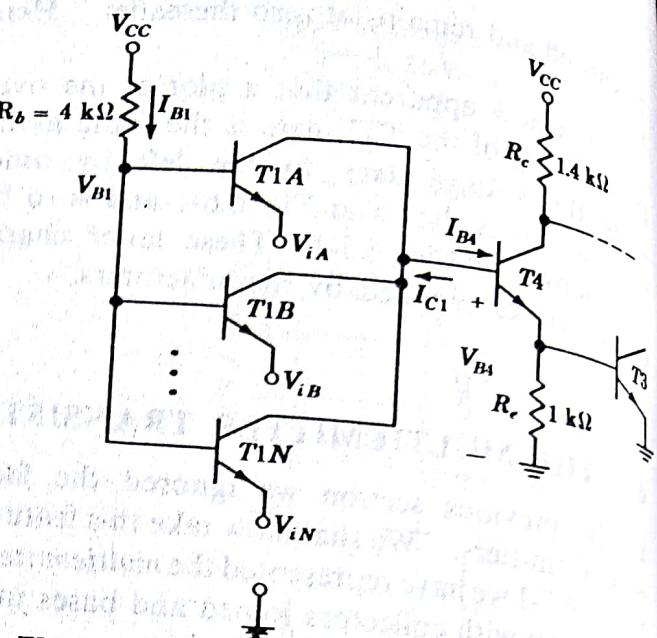
forward-biased base-collector junctions of  $T1B, \dots, T1N$  are 0.65 V, which is 0.1 V less than the forward bias across the base-emitter junction of  $T1A$ . On many occasions, we have noted that a change of 0.1 V in voltage will carry a transistor from saturation to the edge of cutoff. Hence, in Fig. 6.7-1, we may estimate that when one (or more) inputs are set at the logic level 0, the other transistors are, to all intents and purposes, cut off.

One additional characteristic of the multiemitter transistor should be mentioned. Referring to Fig. 6.3-1, we see that transistors are formed not only between each of the three emitters and the collector but also between the emitters  $E_A$  and  $E_B$ ,  $E_A$  and  $E_C$ , and  $E_B$  and  $E_C$  since they also are *n*p*n* structures. However, because of the geometry of the "transistors," their current gains are very small (less than 0.01) and the presence of these transistors may be neglected.

## 6.8 INPUT VOLT-AMPERE CHARACTERISTIC OF THE TTL GATE

Because of the relative complexity of TTL logic, it is useful to consider the input and the output volt-ampere characteristic in addition to the transfer characteristic. We consider here the input characteristic. The output characteristic is discussed in Sec. 6.9.

In Fig. 6.8-1a we are interested in the input volt-ampere characteristic at one emitter input. Other emitter inputs (only one additional input is shown in the figure) are assumed to be at logic level 1. For the reasons presented in Sec. 6.7 we neglect the effect of these other emitter terminals.



**FIGURE 6.7-1**  
Circuit to show operation of the multiemitter transistor.

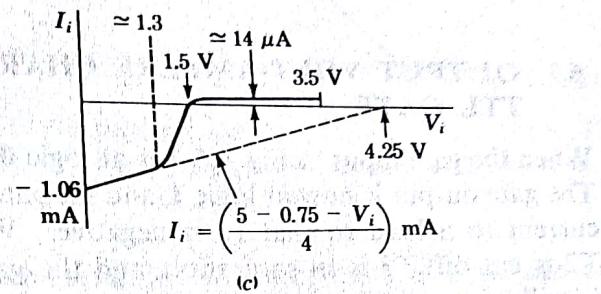
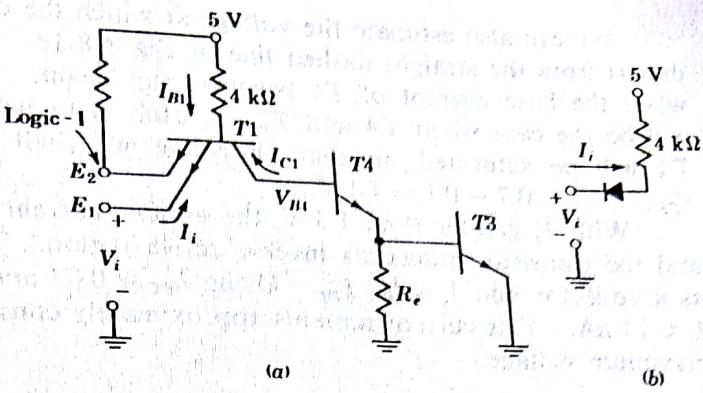
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**FIGURE 6.8-1**  
Input volt-ampere characteristic.

When  $V_i = 0$ ,  $T4$  is cut off and therefore the collector current  $I_{C1} = 0$ . In this case, neglecting the current contribution from  $E_2$  (see Sec. 6.7), we can represent  $T1$  as a diode. An equivalent circuit for calculating the current  $I_i$  is then shown in Fig. 6.8-1b. When we assume the usual 0.75 V junction voltage,  $I_i = -(5 - 0.75)/(4 \text{ k}\Omega) = -1.06 \text{ mA}$ , as noted in the plot of Fig. 6.8-1c. As long as all the current through the 4-k $\Omega$  resistor flows through the  $E_1$  junction, the volt-ampere characteristic is a straight line with current intercept  $-1.06 \text{ mA}$  and voltage intercept  $5 - 0.75 = 4.25 \text{ V}$ . This straight line is indicated (dashed) in the plot.

(dashed) in the plot. As  $V_i$  increases, the  $V_i$ - $I_i$  plot departs from the straight line as  $T4$  begins to turn on. When  $I_i = 0$ , all the current through the 4-k $\Omega$  resistor flows into the collector of  $T1$  and into the base of  $T4$ . At this point both  $T4$  and  $T3$  will be in saturation, and the voltage  $V_{B4}$  will be 1.5 V. Since  $I_i = 0$ , the emitter current in  $T1$  is zero and the collector-emitter voltage is given by Eq. (1.10-9):

$$V_{CE1} = -V_T \ln \frac{1}{\alpha_N} \quad (6.8-1)$$

With  $V_T = 25$  mV and  $\alpha_N = 0.98$ , we have  $V_{CE1} \approx -0.5$  mV. Thus, the input voltage  $V_i$  is 0.5 mV less than  $V_B = 1.5$  V. Hence, we can approximate  $V_i \approx 1.5$  V when  $I_i = 0$ . This point  $V_i = 1.5$  V and  $I_i = 0$  is noted in the plot of Fig. 6.8-1c.

We can also estimate the voltage at which the characteristic will begin to depart from the straight dashed line in Fig. 6.8-1c. This departure will begin when the base current of  $T_4$  becomes significant. We may judge that such will be the case when  $T_4$  and  $T_3$  are each in its active region. At this time  $T_1$  will be saturated, so that altogether we shall have  $V_i = V_{BE3} + V_{BE4}$ .

With  $V_i$  greater than 1.5 V, the emitter current in  $T_1$  reverses direction as a collector and  $I_i = h_{FE} I_{B1}$ . Using  $h_{FE} \approx 0.02$  and  $I_{B1} = 0.7$  mA, we have  $I_i \approx 14 \mu\text{A}$ . This current remains approximately constant as  $V_i$  increases to its maximum voltage.

## 6.9 OUTPUT VOLT-AMPERE CHARACTERISTIC OF THE TTL GATE

When the gate input in Fig. 6.5-1 is at logic 0, transistors  $T_4$  and  $T_3$  are cut off. The gate output is now at logic 1, and the gate is sourcing current, i.e., furnishing current to a load so that  $-I_L$  is negative. When the gate input is at logic 1,  $T_2$  is cut off,  $T_3$  is in saturation, and the gate will be sinking current, that is,  $I_L$  will be positive.

Consider first the case where the input is at logic level 0,  $T_3$  is cut off, and the gate is sourcing current. Then the output characteristic of the gate can be deduced from Fig. 6.9-1, where  $-I_L = I_S$  is the source current. Since, in this mode, transistor  $T_2$  is in the active region, the base current is  $I_S/(h_{FE} + 1)$ . Starting at the 5 V supply and taking account of the voltage drops across  $R_{e4}$  across the base-emitter junction of  $T_2$  (0.65 V), and across the diode  $D$  (0.65 V), we find

$$V_o = 3.7 - \frac{R_{e4}}{h_{FE} + 1} I_S \quad (6.9-1)$$



FIGURE 6.9-1  
Equivalent circuit to find output voltage characteristic when  $T_3$  is cut off.

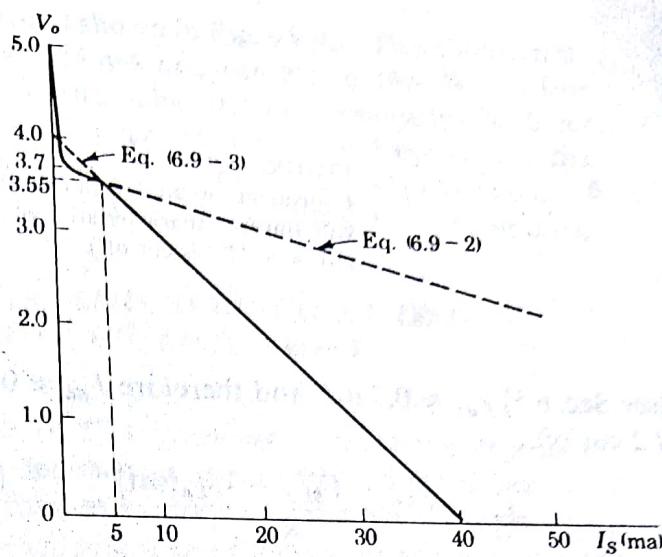


FIGURE 6.9-2  
Output-input characteristics when \$T\_3\$ is cut off.

Thus, the output has a Thevenin representation which consists of a voltage of 3.7 V in series with an output impedance \$R\_{c4}/(h\_{FE} + 1)\$. With \$R\_{c4} = 1.4 \text{ k}\Omega\$ and using \$h\_{FE} + 1 = 50\$, we find that the output impedance is \$28 \Omega\$, so that

$$V_o = 3.7 - 28 I_s \quad (6.9-2)$$

When transistor \$T\_2\$ is in saturation, \$V\_{BE2} = 0.75\$ and \$V\_{CE2} = 0.2\$ V. Also \$V\_D = 0.75\$ V. In this case \$I\_{B2} = (3.5 - V\_o)/1,400\$ and \$I\_{C2} = (4.05 - V\_o)/100\$. Since \$I\_s = I\_{C2} + I\_{B2}\$ and \$I\_{B2} \ll I\_{C2}\$, we have

$$V_o \approx 4.05 - 100 I_s \quad (6.9-3)$$

The straight-line plots for Eqs. (6.9-2) and (6.9-3) intersect at \$I\_s \approx 5\$ mA. Hence, for \$I\_s > 5\$ mA the transistor is in saturation, and Eq. (6.9-3) applies, while for \$I\_s < 5\$ mA the transistor is in the active region, and Eq. (6.9-2) applies. The output characteristic is then given by the solid-line plot of Fig. 6.9-2. At very low currents that plot must depart from the straight line of Eq. (6.9-2). For at \$I\_s = 0\$, there need be no drop across \$R\_{c2}\$ nor any drop across the base-emitter junction of \$T\_2\$ or the diode \$D\$, and, in principle, \$V\_o\$ should become equal to \$V\_{CC} = 5.0\$ V.

When all the inputs to the gate of Fig. 6.5-1 are at logic level 1, \$T\_2\$ is cut off while \$T\_3\$ and \$T\_4\$ are in saturation. The output looks back directly across the saturated transistor \$T\_3\$, as in Fig. 6.9-3, which now sinks a current \$I\_L\$. The volt-ampere characteristic at these output terminals is now precisely the common-emitter collector characteristic of the transistor corresponding to the base current \$I\_{B3}\$. This characteristic is similar to that shown in Fig. 1.10-1, the difference being that we now plot \$V\_o = V\_{CE3}(\text{sat})\$ as a function of \$I\_L = \sigma h\_{FE} I\_{B3}\$ rather than as a function of \$\sigma\$. We calculate \$I\_{B3}\$ as follows. Referring to Fig. 6.5-1, we have

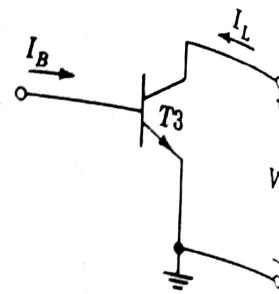


FIGURE 6.9-3

Equivalent circuit for calculating output volt-ampere characteristic when  $T_3$  is saturated ( $T_2$  is cut off).

(see Sec. 6.5)  $I_{B1} \approx 0.7 \text{ mA}$  and therefore  $I_{B4} \approx 0.7 \text{ mA}$ . With  $T_4$  saturated and  $T_2$  cut off,

$$I_{C4} = \frac{V_{CC} - V_{BE3} - V_{CE4}(\text{sat})}{R_{c4}} = \frac{5 - (0.75 + 0.2)}{1.4 \text{ k}\Omega} \approx 2.9 \text{ mA} \quad (6.9-4)$$

Hence

$$I_{E4} = I_{B4} + I_{C4} = 0.7 + 2.9 = 3.6 \text{ mA}$$

Since the current in resistor  $R_e$  is  $(6.9-5)$

$$I_{R_e} = \frac{0.75}{1 \text{ k}\Omega} = 0.75 \text{ mA} \quad (6.9-6)$$

we have

$$I_{B3} = I_{E4} - I_{R_e} = 3.6 - 0.75 = 2.85 \text{ mA} \quad (6.9-7)$$

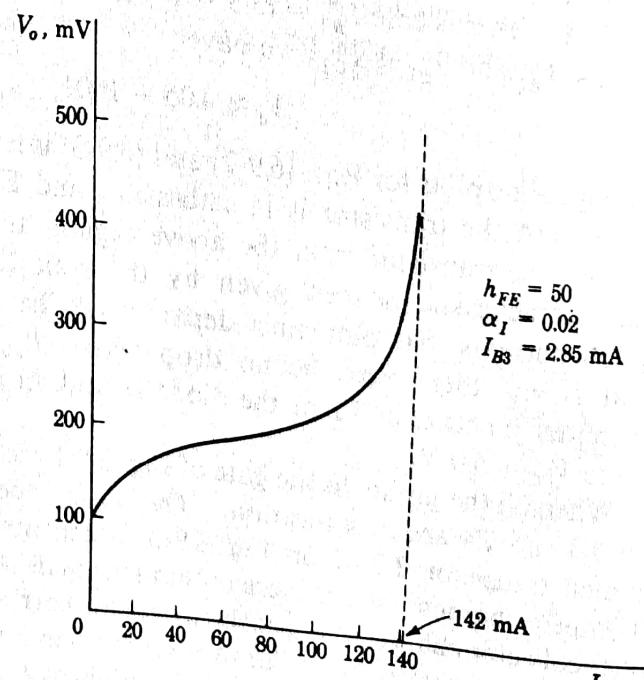


FIGURE 6.9-4

Output volt-ampere characteristic when all inputs to a TTL gate are in state 1.

A typical TTL output characteristic is shown in Fig. 6.9-4. This characteristic corresponds to a base current  $I_{B3} = 2.85 \text{ mA}$  as given by Eq. (6.9-7). At low currents the output is  $V_{CE}(\text{sat}) \approx 0.1 \text{ V}$ , the value we have associated with an unloaded transistor in saturation. At higher currents the drop across the saturated transistor increases. Finally, at a current in the neighborhood of  $I_L = h_{FE} I_{B3} = 50(2.85 \times 10^{-3}) = 142 \text{ mA}$ , transistor  $T_2$  comes out of saturation.

### 6.10 MANUFACTURER'S DATA AND SPECIFICATIONS; TEMPERATURE DEPENDENCE AND NOISE IMMUNITY

As with other gates, the characteristics of TTL gates are temperature-dependent. As before, the principal source of this dependence is the temperature dependence of the base-emitter and base-collector junction voltages. Because of the similarity with calculations already made, these calculations of temperature effects are left for the problems. Instead we shall take note of this temperature dependence as it is evidenced in typical average characteristics published by manufacturers.

Figures 6.10-1 to 6.10-4 all apply to the Texas Instrument type 54/74 gate. The type 74 gates are intended for the ambient temperature range 0 to  $70^\circ\text{C}$  and allow for a supply-voltage range from 4.75 to 5.25 V. The type 54 are held to tighter tolerances, are intended for a temperature range  $-55$  to  $125^\circ\text{C}$ , and allow a supply range from  $-4.5$  to  $5.5$  V. This gate is a "standard" type TTL NAND gate and represents a useful compromise between good speed and modest power dissipation. Figure 6.10-1 gives typical transfer characteristics for a variety

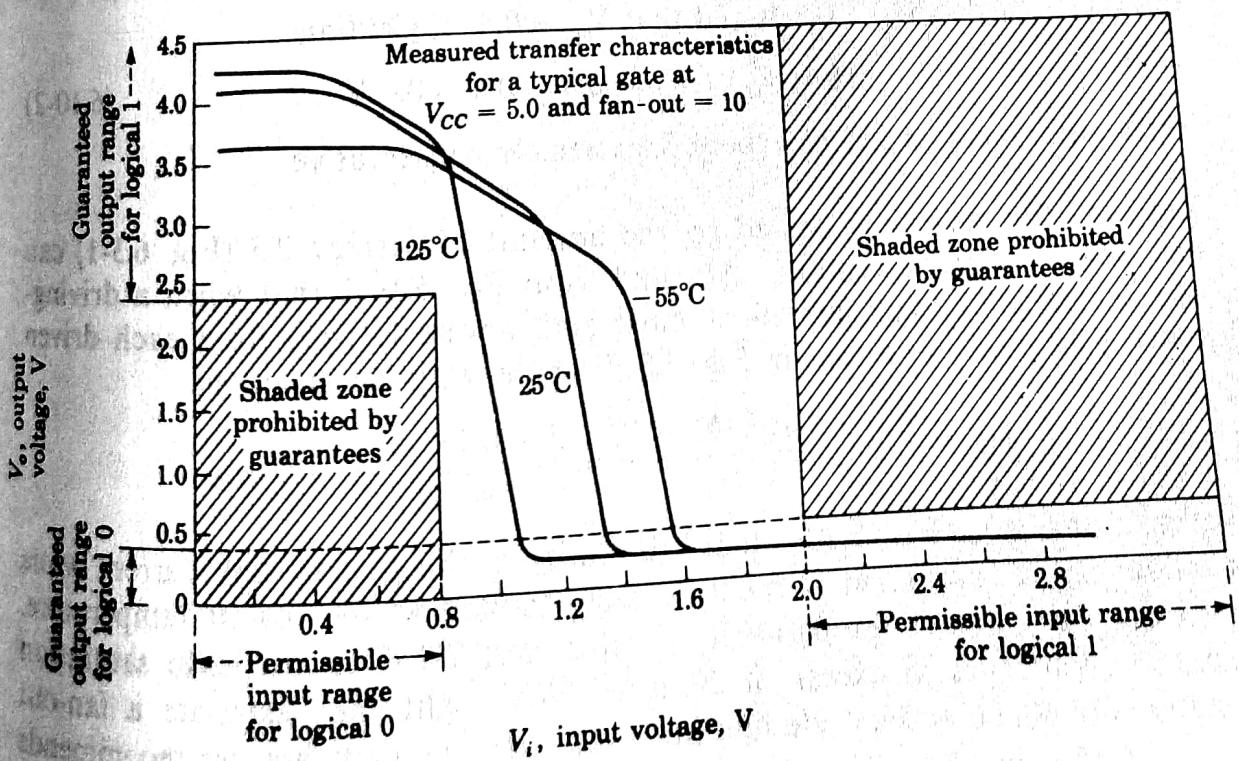


FIGURE 6.10-1  
Voltage transfer characteristics for typical SN54/74 TTL NAND gate.

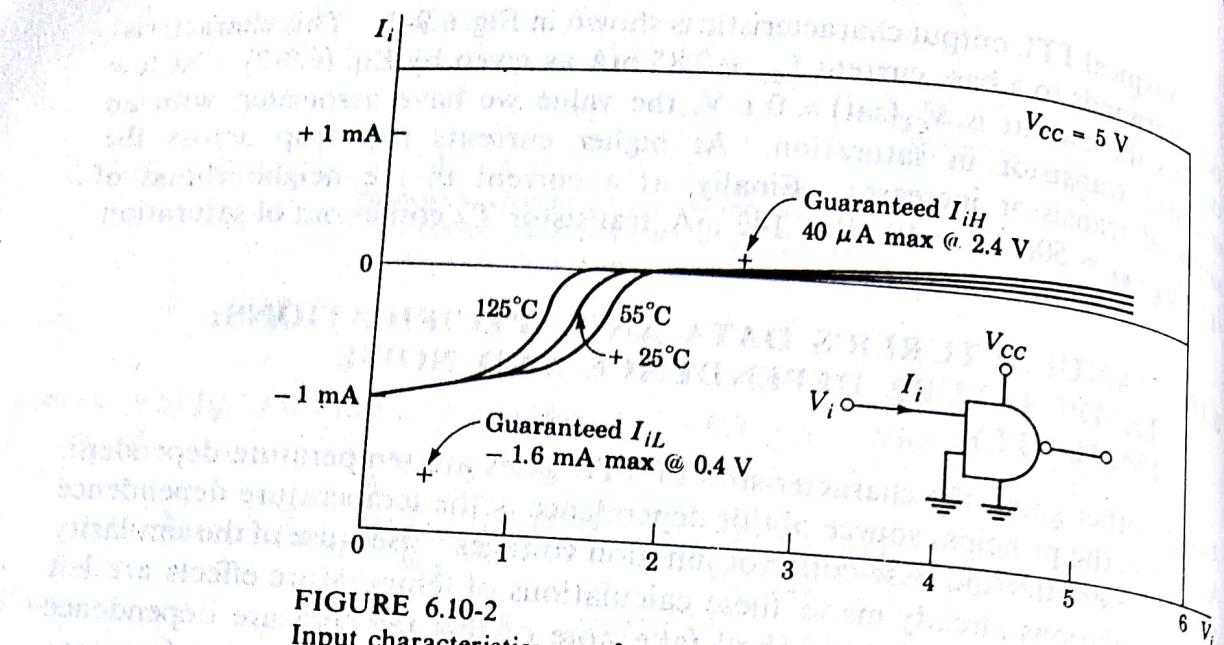


FIGURE 6.10-2

Input characteristics as a function of temperature for standard series SNS5475.

of temperatures and for a fan-out of 10. Note that the manufacturer guarantees that any input voltage greater than 2.0 V will be acknowledged by the gate to correspond to the logic level 1; that is,  $V_{iH} = 2.0$ . Similarly it is guaranteed that the gate output at logic level 1 will never be less than 2.4 V; that is,  $V_{oH} = 2.4$  V. Thus, the  $\Delta 1$  noise margin is

$$\Delta 1 = V_{oH} - V_{iH} = 2.4 - 2.0 = 0.4 \text{ V} \quad (6.10-1)$$

We also note that  $V_{iL} = 0.8$  V and that  $V_{oL} = 0.4$  V, yielding

$$\Delta 0 = V_{iL} - V_{oL} = 0.8 - 0.4 = 0.4 \text{ V} \quad (6.10-2)$$

These noise margins are, as expected, extremely conservative.

**Fan-out** The fan-out is limited by the amount of current  $T_3$  (Fig. 6.5-1) can sink when it is in saturation. We find from Fig. 6.10-2 that when a driving-gate output is at logic level 0, it must sink about 1.0 mA from each driven gate. This result is verified in Fig. 6.5-1, where, with  $T_3$  saturated,

$$I_{11} = \frac{V_{CC} - V_{BE}(T11) - V_o}{R_b} = \frac{5 - 0.75 - 0.2}{4 \text{ k}\Omega} \approx 1 \text{ mA}$$

We note also from Fig. 6.10-3 that the ability of the gate to sink current while keeping  $T_3$  in saturation is most severely limited at the lowest temperature,  $-55^\circ\text{C}$ . Even at this temperature we note that  $T_3$  does not leave saturation except for currents in excess of 30 mA. We might then estimate a fan-out capability of  $30/1.0 = 30$ . We find however, that the manufacturer recommends a fan-out of only 10 to keep  $V_{oL}$  well below 0.4 V. Further the fan-out affects propagation delay time as well as saturation.

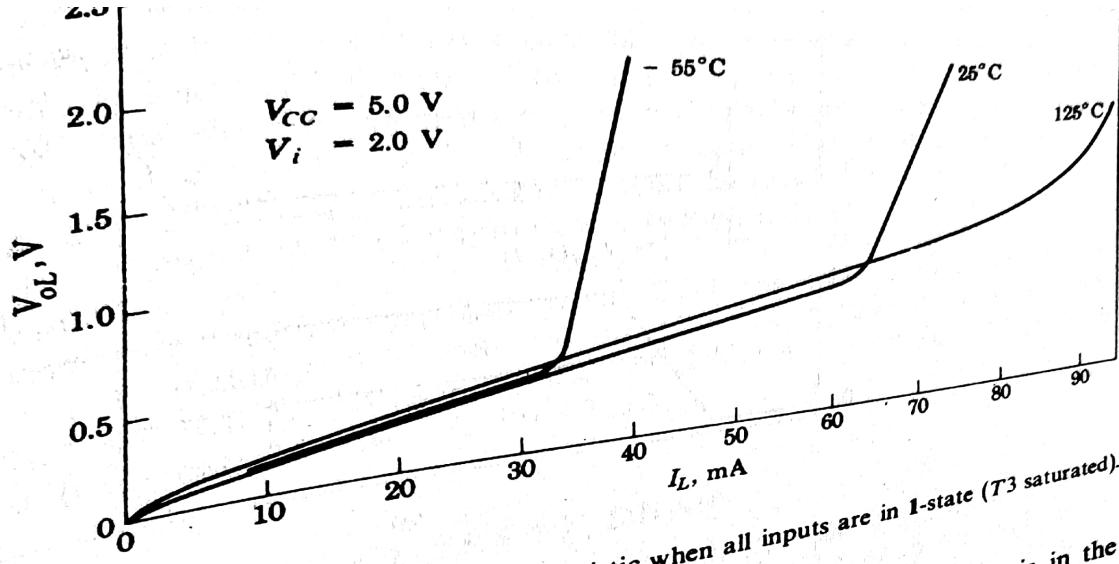
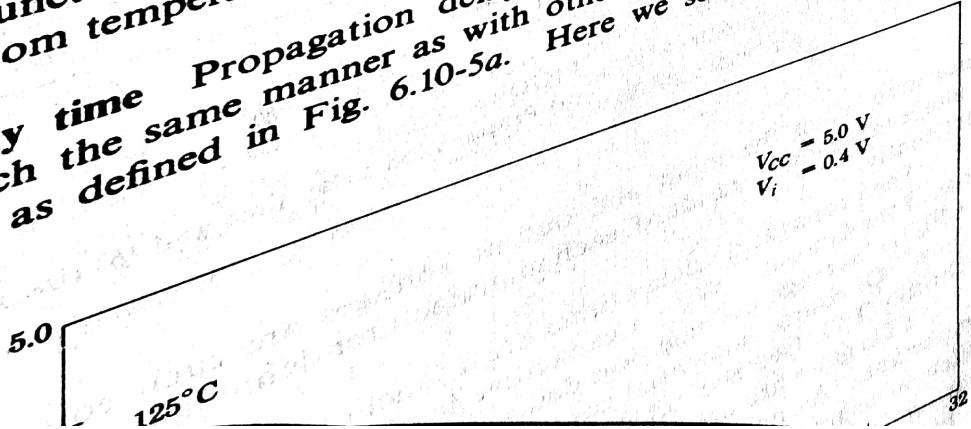


FIGURE 6.10-3  
Output volt-ampere characteristic when all inputs are in 1-state ( $T_3$  saturated).

Figure 6.10-4 is a plot of the output voltage  $V_{oH}$  when the gate is in the high state, as a function of the output current  $I_S$ . Note that if  $V_{oH} > 2.5$  V and  $I_S < 11$  mA at room temperature. Propagation delay time measured in much the same manner as with other gates. Here we see that the times  $t_{pd}(HL)$  and  $t_{pd}(LH)$  are as defined in Fig. 6.10-5a. Here we see that the times  $t_{pd}(HL)$



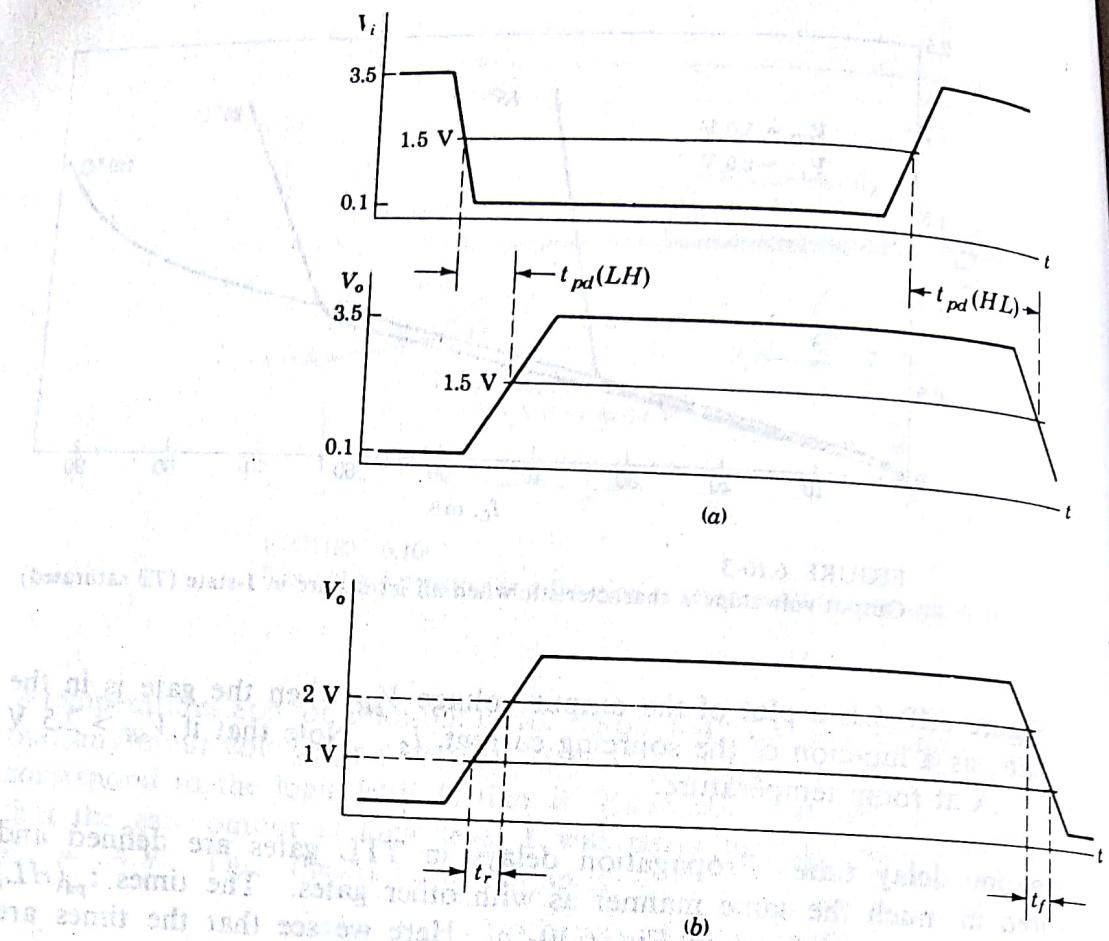


FIGURE 6.10-5

(a) Propagation delay time and (b) rise and fall time in TTL.

measured when the input and output voltages are each equal to 1.5 V. The voltage value is not standard, each manufacturer defining the delay time somewhat differently.

The propagation delay times are a function of capacitive loading and therefore of the fan-out. With a capacitive load of the order of 15 pF and a fan-out of 10, the average propagation delay time  $t_{pd} \equiv \frac{1}{2}[t_{pd}(HL) + t_{pd}(LH)]$  is typically 10 ns. Of course, increased capacitive loading increases the propagation delay. Schottky TTL (see Sec. 6.13) gates have propagation delay times of 2 to 4 ns.

TTL gates are used at high speeds, where the *rise time* and the *fall time* are important. As noted in Fig. 6.10-5b, the rise and fall times of TTL gates are often measured between the 1- and 2-V points of the output voltage. Alternatively, sometimes the rise and fall times are defined as the time of transition between the 10 and 90 percent points of the output waveform. Typical values for a high-speed TTL gate are  $t_r = 8$  ns and  $t_f = 5$  ns for a medium-speed TTL gate and 4 to 8 ns for a high-speed TTL gate. Schottky TTL gates have rise and fall times of about 3ns.

Because of its active pull-up, the TTL, like the RTL buffer (see Sec. 4.7), can accommodate a heavy capacitive load like that presented by 10 driven gates. When  $V_o$  drops to logic 0,  $T_4$  cuts off and the base voltage of  $T_2$  rises abruptly. The capacitive load due to the fan-out keeps the output voltage  $V_o$  initially at 0.1 V. Hence, as is easily verified,  $T_2$  saturates and the current initially flowing out of the emitter of  $T_2$ ,  $I_{E2} \approx 38.5$  mA. This large transient current (current spike) rapidly changes the load capacitance bringing  $V_o$  abruptly to the logic 1 level.

Unfortunately, it turns out that, when  $T_2$  turns ON and saturates, it will do so before  $T_3$  comes out of saturation. As a consequence a substantial portion of the current  $I_{E2}$  which should be available to charge the loading capacitance will instead be diverted into  $T_3$ .

### 6.11 POWER-SUPPLY CURRENT DRAIN

The current drain from the power supply used with TTL gates is not the same in the two logic levels. The drain is larger for logic level 0 than for logic level 1. In a typical case, say in the gate of Fig. 6.5-1, the steady-state drain is roughly 3 mA in one level and roughly 1 mA in the other (see Prob. 6.11-1). The difference depends principally on the fact that in one case  $T_4$  conducts and in the other is cut off. Of much more importance, however, is the fact that the current spike in  $I_{E2}$ , discussed in the preceding section, must be supplied by the power supply.

The exact waveform of the supply current depends both on the type of TTL gate involved and on the capacitive loading. Spikes range in amplitude up to about 40 mA, as noted, and have durations from several nanoseconds to many tens of nanoseconds in the case of heavy capacitive loading. A typical current waveform is shown in Fig. 6.11-1.

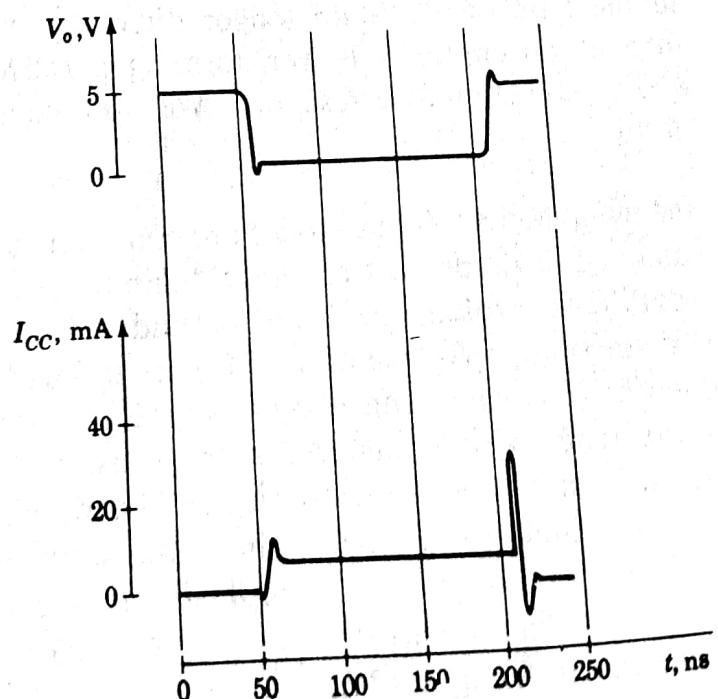


FIGURE 6.11-1  
Output-voltage and current-supply spike.

These current spikes occur as frequently as the gate makes transitions, and hence the average current drawn is a function of the frequency at which the gate is being operated. It is not unusual for the average current drain to increase by a factor of 2 or 3 when the gate is being operated at some tens of megahertz. If permitted to flow through the internal impedance of the power supply, these spikes of current would produce spikes of voltage, which would then be distributed throughout the system being serviced by the power supply. To avoid such a situation, it is necessary to provide capacitive bypassing to ground at the point where the power-supply lead is connected to the integrated-circuit chip.

## 6.12 TYPES OF TTL GATES

A number of types of TTL gates are available, differing principally in the compromise made between speed and power dissipation. Thus, the gate of Fig. 6.5-1 is considered a medium-speed gate and has an average power dissipation of about 10 mW and, as noted, a propagation delay of about 10 ns. The power dissipation can be decreased, at the expense of speed, by increasing the resistor values. Thus, we find that a commercially available gate with (see Fig. 6.5-1)  $R_b = 40 \text{ k}\Omega$ ,  $R_{c4} = 20 \text{ k}\Omega$ ,  $R_e = 12 \text{ k}\Omega$ , and  $R_{c2} = 500 \Omega$  has a power dissipation of only 1 mW, but its average propagation time is 33 ns.

The speed of a gate can be increased by lowering resistor values. However, when speed is at a premium, additional changes are incorporated into the gate. A typical high-speed TTL gate is shown in Fig. 6.12-1. We note that  $R_b$  has been reduced to 2.4 k $\Omega$ ,  $R_{c4}$  to 800  $\Omega$ , and  $R_{c2}$  to 60  $\Omega$ . We note three additional changes as well: (1) Diodes shunt each input to ground; (2) the emitter resistor of  $T_4$  has been replaced by a circuit consisting of an additional transistor  $T_5$  and two resistors; and (3) the connection from the collector of  $T_4$  to the base of  $T_2$  is no longer direct, as in Fig. 6.5-1, but is made instead through an emitter follower, forming a *Darlington amplifier*, composed of  $T_6$  and a 3.5-k $\Omega$  emitter resistor. We now consider each of these modifications in turn.

**The input diodes** Input diodes are common to all TTL gates, except the slowest gates. The diodes act as input "clamps" to suppress the ringing that results from the fast voltage transitions found in TTL systems. Consider, for example, that the output voltage of a TTL gate suddenly changes from the 1 level to the 0 level. The wire connecting this gate to a driven gate now carries this signal. If the wire, which acts like a transmission line, is not terminated properly, ringing results (see Appendix A), as illustrated in Fig. 6.12-2a.

The input diodes clamp the negative undershoot at approximately -0.75 V and absorb enough of the applied signal energy to prevent a large positive overshoot which might turn the gate ON again. This suppression of the ringing is illustrated in Fig. 6.12-2b.

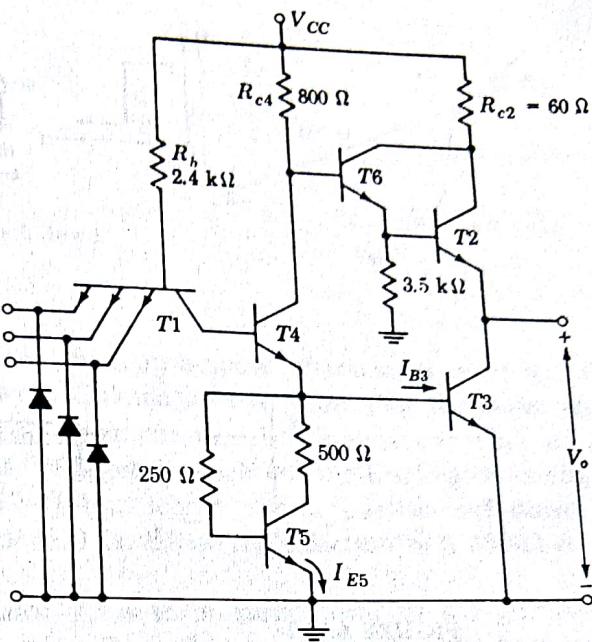


FIGURE 6.12-1  
A high-speed TTL gate.

**The Darlington circuit** We consider now the effect of  $T_6$  in the circuit of Fig. 6.12-1. First, we may note, as a matter of incidental interest, that the diode  $D$  encountered in the circuit of Fig. 6.5-1 is not used in Fig. 6.12-1. It will be recalled that the diode was included to ensure that  $T_2$  will be cut off when  $T_4$  and  $T_3$  are saturated. In the configuration shown here the voltage drop across the base-emitter junction of  $T_6$  serves the same function provided by the diode voltage drop, and  $T_2$  remains cut off when  $T_3$  is ON.

Returning for a moment to the circuit of Fig. 6.5-1, we recall that when  $T_2$  is in its active region, the output resistance seen at the gate output terminal is approximately  $R_{c4}/h_{FE}$ , for which, in Sec. 6.9 [see Eq. (6.9-2)] we estimated the value  $28 \Omega$ . In Fig. 6.12-1, we would calculate the output resistance as follows. First the output resistance, seen looking back into the emitter of  $T_6$ , is  $R_{c3}/h_{FE} = 800/50 = 16 \Omega$ . Then, repeating the calculation for  $T_2$ , we find that the gate output resistance is  $16/h_{FE} = 16/50 \approx 0.3 \Omega$ . We have neglected the resistance of the transistor in these calculations. As a result, we find that in the gate of Fig. 6.12-1 the measured output resistance is more nearly  $10 \Omega$ . In any event, the important characteristic of the gate of Fig. 6.12-1, is that when  $T_6$  and  $T_2$  are conducting, the gate output resistance is substantially lower than in the circuit of Fig. 6.5-1. (We recognize, of course, that transistors  $T_6$  and  $T_2$  are in a Darlington configuration, one characteristic of which is precisely this reduced output resistance.) This lowered output impedance increases

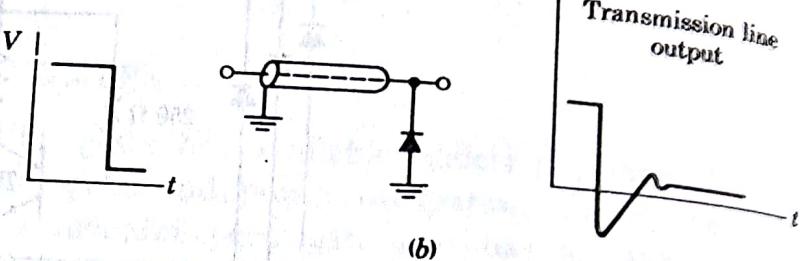
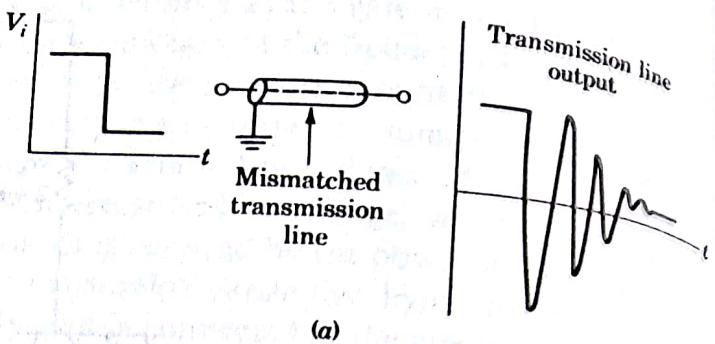


FIGURE 6.12-2

(a) Output of a transmission line to a negative-transition step, showing ringing.  
 (b) Output of the transmission line loaded by a diode.

the speed of operation of the gates. For with the lowered output resistance, any capacitance shunting the gate output will be able to charge more rapidly.

Of course, these considerations concerning output resistance do not apply when transistors  $T_6$  and  $T_2$  are cut off or in saturation. However, over a considerable range of the transition region from one logic level to the other, both transistors are in the active region, and the above discussion does apply. In this connection it is of interest to note that while in Fig. 6.5-1 transistor  $T_2$  goes to saturation when the gate output goes to logic level 1, such is not the case in the circuit of Fig. 6.12-1. In a Darlington circuit only the input transistor ( $T_6$  in Fig. 6.12-1) and not the output transistor ( $T_2$ ) can be driven to saturation. For no matter whether  $T_6$  is saturated or in its active region,  $V_{CE6}$  is positive. Since  $V_{CB2} = V_{CE6}$ , the collector-base junction of  $T_2$  can never be forward-biased. Hence  $T_2$  can never saturate.

**The active pull-down** The emitter resistor  $R_e$  in Fig. 6.5-1 provides the connection to ground for the base of the output transistor  $T_3$ . Thus,  $R_e$  is the *pull-down* resistor which pulls the base of  $T_3$  down to ground when  $T_4$  cuts off. This terminology is analogous to use of the term *pull-up* resistor used in connection with collector resistors which are returned to the supply voltage. Extending the analogy, we shall refer to the circuit associated with  $T_5$  in Fig. 6.12-1 as an *active pull-down*. We consider now the advantages which accrue from the use of such an active pull-down.

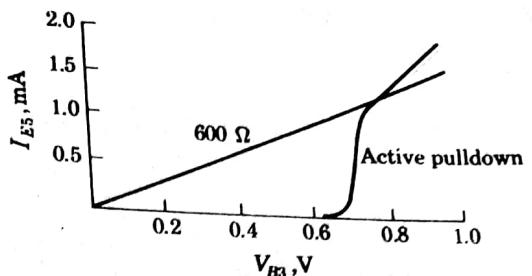


FIGURE 6.12-3  
The effect of the active pull-down.

In Fig. 6.12-3, we compare the volt-ampere characteristics of a  $600\text{-}\Omega$  resistor and the active pull-down. Calculations to show that the curve representing the active volt-ampere pull-down characteristic is reasonable are left as a student exercise. In high-speed TTL gates which use the Darlington configuration ( $T_6$  and  $T_2$  in Fig. 6.12-1) but which use a passive pull-down, the pull-down resistor has the value  $600\text{ }\Omega$ ; hence the selection of a  $600\text{-}\Omega$  resistor for comparison.

Now consider that transistor  $T_3$  is to be turned ON. It will go ON when its base voltage exceeds  $0.65\text{ V}$  and will reach saturation when the base voltage is  $0.75$ . We note from Figs. 6.12-1 and 6.12-3 that over this range of voltages the active pull-down diverts less current from the base of  $T_3$  than it would with a passive  $600\text{-}\Omega$  pull-down resistor. Hence, in this mode of operation  $T_5$  appears as a "resistor" which is larger than  $600\text{ }\Omega$ . As a result we have as a first advantage that  $T_3$  turns on faster.

To see a second advantage we note that when  $T_3$  is ON and the fan-out is small, the base current in  $T_3$  is substantially larger than is required to bring it to saturation. This excessive base current prolongs the storage time and delays the turnoff of the transistor. It also develops that  $T_3$  can be driven so far into saturation that its base-emitter voltage may well exceed even  $0.8\text{ V}$ . In such a case, again to be noted in Fig. 6.12-3, the active pull-down diverts more current from the base than a passive pull-down would. Hence, in this mode the active pull-down appears as a smaller resistor than the  $600\text{-}\Omega$  resistance. Thus, excessive base current is somewhat suppressed.

In considering the turnoff of  $T_3$ , we might imagine, however, that once the base voltage drops below  $0.8\text{ V}$ , the active pull-down would be at a disadvantage, since it draws less current than a  $600\text{-}\Omega$  resistor out of the base of  $T_3$ . Such, however, is not the case. We must keep in mind that the active pull-down characteristic plotted in Fig. 6.12-3 applies only in steady state. Actually, at turnoff, the active pull-down continues to draw the larger current for some few nanoseconds until the charge distribution within  $T_5$  itself has adjusted to the change.

The active pull-down also offers an important advantage in connection with the operation over a wide range of temperature. In a TTL gate without active pull-down, the turnoff time for  $T_3$  increases with increasing temperature because  $T_3$  is driven further into saturation. The reasons for the increases are twofold:

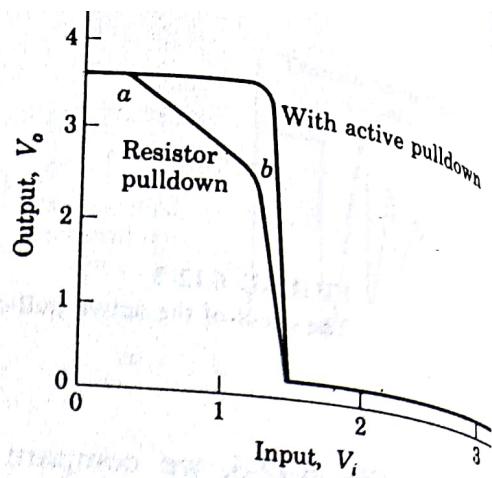


FIGURE 6.12-4

Comparison of transfer characteristics of TTL gates: resistor pull-down versus active pull-down.

(1) since junction voltages decrease with increasing temperature, with an increase in temperature more current will flow into the base of  $T_3$ ; (2) the current gain of a transistor increases with temperature. Hence, even a fixed base current will drive a transistor farther into saturation as the temperature increases. With higher temperature, however, the active pull-down shown in Fig. 6.12-1 actually draws more current, thereby keeping  $I_{B3}$  fairly constant. This compensation results since an increase in temperature decreases  $V_{BE5}$ , thereby increasing  $I_{B5}$  and  $I_{C5}$ . A calculation to determine the change in  $I_{B3}$  resulting from a change in temperature is left as a student exercise.

A final advantage of the active pull-down is to be seen in its effect on the input-output voltage characteristic of the TTL gate. Characteristics with active pull-down and resistor pull-down are compared in Fig. 6.12-4. With resistor pull-down the plot exhibits a region (between  $a$  and  $b$ ), as discussed in Sec. 6.5, where the slope has a magnitude equal to the ratio of collector to emitter resistors of  $T_4$ . In this region  $T_4$  is in its active region and provides gain. Point  $a$  marks the turn-on of  $T_4$ , and point  $b$  marks the turn-on of transistor  $T_3$ .

In the circuit of Fig. 6.12-1, until such time as  $T_3$  turns on, the active pull-down provides no path for the emitter current of  $T_4$ . Thus,  $T_4$  and  $T_3$  go on simultaneously, and the region  $a-b$  is absent, with active pull-down. As a result the characteristic exhibits the much more abrupt change between levels, as indicated. The fact that the transition between logic levels is achieved with much smaller change in input voltage is, of course, of advantage in the matter of noise immunity.

## 6.13 SCHOTTKY TTL

In all TTL gates, transistors are driven into saturation and diodes are turned on. A good part of the speed limitation of the gates results from the storage time delay associated with turning off and allowing transistors to recover from

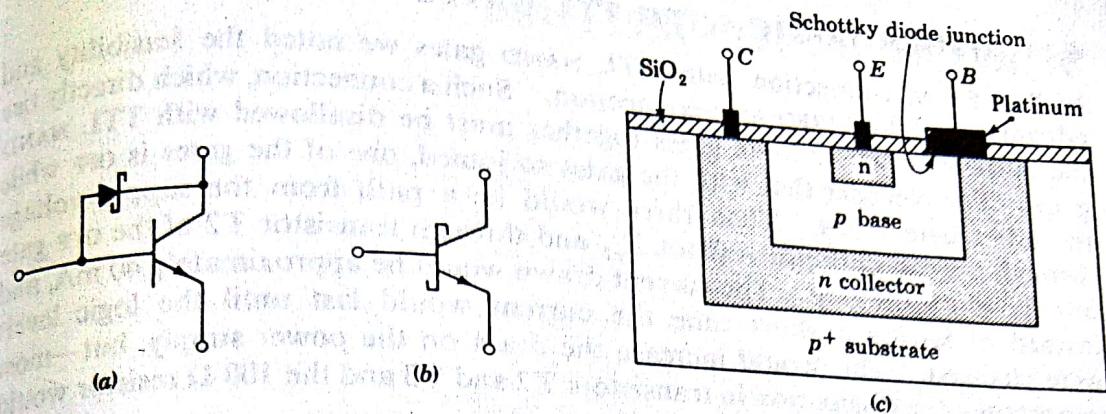


FIGURE 6.13-1

(a) Schottky diode connected from base to collector. (b) Schottky transistor.  
(c) Fabrication of the Schottky transistor.

saturation. The use of Schottky diodes (Sec. 1.19) reduces the transistor turnoff time to negligible proportions.

In Sec. 1.19 we considered how a diode bridged between collector and base of a transistor can serve to restrain a transistor from entering saturation (see Fig. 1.19-1). To review the matter, we note again that a transistor in saturation operates with a collector junction forward-biased to the extent of about 0.55 V or more. The transistor may therefore be kept out of saturation by the addition of a *diode clamp*, which does not allow the collector junction to become adequately forward-biased.

A transistor with a Schottky-diode clamp is indicated in Fig. 6.13-1a. Such a diode-transistor combination is referred to as a *Schottky transistor* and generally represented by the figure shown in Fig. 6.13-1b. The geometry (simplified and idealized) of an integrated-circuit Schottky transistor is shown in Fig. 6.13-1c. Observe that the metal contact to the n-type collector has been allowed to overlap the p-type base, thereby creating a metal-semiconductor (Schottky) diode junction between the metal and the collector. As discussed in Sec. 1.19, the base doping is graded so that the junction of the base and the metal is not rectifying.

There is available a family of high-speed TTL gates of which the schematic is as given in Fig. 6.12-1 but in which the input diodes are Schottky diodes and all transistors, except T2, are Schottky transistors. An exception is made of T2 since, as we have noted, T2 does not saturate. This Schottky family of gates has propagation times as low as 2 ns and rise and fall times in the range 2 to 3 ns. The power-supply current spikes are also reduced, being about 20 percent as large as those encountered in TTL gates that do not use Schottky transistors. In these gates the improved speed results, in part, from the fact that Schottky transistors have areas which are roughly one-half the areas used in conventional TTL transistors.

### 6.14 OTHER LOGIC WITH TTL GATES

In Sec. 5.6 in connection with DTL NAND gates we noted the feasibility and advantages of the WIRED-AND connection. Such a connection, which directly ties the outputs of two or more gates together must be disallowed with TTL NAND gates. For consider that with the gates so joined, one of the gates is OFF while the other gate is ON. Then there would be a path from the supply voltage through a small collector resistor  $R_{c2}$  and through transistor  $T_2$  of the OFF gate into  $T_3$  of the ON gate. The current drawn would be approximately 40 mA, and instead of lasting a short time the current would last until the logic levels were changed. This would increase the drain on the power supply, but—most important—the dissipation in transistors  $T_2$  and  $T_3$  and the 100- $\Omega$  resistor would be excessive.

Still, the economy possible with the WIRED-AND connection is such that manufacturers find it advantageous to make available a modified TTL gate which allows such a connection. The modification consists in deleting the upper totem-pole transistor; i.e., these gates are intended to be used with an external passive pull-up, (resistor), and, of course, the advantages of an active pull-up are thereby relinquished.

While it is possible to perform all logic functions, it is often very convenient and economical to have available an AND gate. Of course, two NAND gates may be cascaded to achieve the AND function. However, gates are available in which a second inversion is incorporated within the gate itself and at low power level.

NOR gates and gates which perform the AND-OR-INVERT (AOI) function are also available in TTL logic. The circuitry of these gates is somewhat different from the circuitry of NAND gates (see Probs. 6.14-1 to 6.14-4).

### REFERENCE

- 1 Morris, R. L., and J. R. Miller, eds.: *Designing with TTL Integrated Circuits*, McGraw-Hill, New York, 1971.