Ex./CSE/T/214/18/2013

BACHELOR OF COMPUTER SCIENCE & ENGINEERING EXAMINATION, 2013

(2nd Year, 1st Semester)

DIGITAL CIRCUITS

Full Marks : 100 Time : Three Hours

Answer *any five* questions.

1. (a) Explain the operation of a positive logic AND gate using Diodes. 4

   (b) Has can this be modified to implement a universal logic gate ? 4

   (c) Explain the operation of the same. 6

   (d) From the transfer characteristics estimate the Noise Margins of the same at 25°C. 6

2. (a) What do you understand by the Transfer characteristics of a logic family ? 4

   (b) Draw and explain the Transfer characteristics of a TTL Not gate. 16

3. (a) How can an Inverter be implemented by using MOSFET. Explain its operation. 6

[*Turn over*]

(b) Estimate the voltage rise time in an MOSFET inverter in terms of the circuit parameters. 6

(c) Calculate t_r ; when $c_L = 6p_f$, $k_L = 16\mu A/v^2$ and $v_f = 12V$. 4

(d) Realise $X = \overline{(A + B)C + D.E}$ using a single Mos gate. 4

4. (a) What are the various building blocks of a PLL ? Explain their operations. 12

(b) How does a PLL track an input frequency. 4

(c) How can an input frequency be multiplied by π ? 4

5. (a) Explain the operation of a 3tr/cell MOS memory cell. 8

(b) How can the stored information be retained in such a Memory cell ? 8

(c) How does it differ from a 1tr/cell RAM. 4

6. (a) Explain the operation of a buffered weighted register type DAC. 8

(b) How can offsets be introduced in such converters? 4

(c) How can a 3 bit signed binary number in 1's complement representation be converted to analog voltages ? 8

[*Turn over*]

7. (a) Explain the operation of a 3 bit direct comparison type ADC. 8

   (b) Design the encoder circuit. 4

   (c) How can a 6 bit ADC be implemented by using above mentioned converters. 6

   (d) What are its advantages and disadvantages ? 2

8. Write notes on *any four* of the following : 5×4

   (a) HTL gates ;

   (b) Tristate gates ;

   (c) C MOS gates ;

   (d) Square wave generation ;

   (e) Implementation of Non-Volatile RAM ;

   (f) Over-driven Emitter follower switches for DAC's ;

   (g) Dual Slope ADC ;

   (h) Sample and Hold circuits.

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