MCA 1st Year 2nd Semester Examination 2018

Subject: Computer Organization and Architecture

Time: 3hrs **Full Marks:** 100

Answer any **five**

Answer all the sub-parts of a question in *adjacent* location

1 Compare the following (any **four**): 5x4

a. Address Bus vs. Control Bus

b. Horizontal Microinstructions vs. Vertical Microinstruction

c. Absolute addressing vs. Relative addressing

d. RISC vs. CISC

e. Write Back vs. Write Through

f. SDRAM vs. DDR-SDRAM

2 a. How does interrupts help when you have *write* command in the code? Show with an example. 6

b. What are the merits of *mezzanine* architecture? 2

c. State Amdahl's law. Keeping this law in mind, discuss the effect of parallelism of the code on the performance of the system. 4

d. Briefly discuss about the evolution of Intel x86 architecture. 8

3 a. Concisely write down the different aspects of disk data layout. 6

b. Mention the different fields present in the *Winchester* disk format. 4

c. Consider the example: Z = A x C + A x C; implement this using 1-address and 0-address machines respectively. 5

d. Pictorially show how stack can be designed using shift registers. 3

e. Define the purpose of base and limit registers in designing stack. 2

4 a. What are the advantages of Micro-programmed Control Unit over Hardwired Control Unit? 2

b. With the help of a diagram, discuss the working principle of *Wilkes'* design. Assume 3-bit address fields, and required number of control signals. Consider 8

[Turn over

that the external source provides the starting address of a microprogram stored in the control memory (CM). Keep the facility when control unit can suitably respond to external signals or conditions.

c. Mathematically prove that while designing the control unit using nanoprogramming, it can save more memory than microprogramming. 7

d. Mention few ways to improve the processor organization. 3

5 a. Write down the policies adopted by the RAID levels 1, 3 and 5 for data storing, replication, and recovery. 9

b. Draw the circuit diagram of a Static RAM (SRAM) cell. 3

c. Discuss its working principle. 3

d. Pictorially show that a 16-bit bit-sliced ALU can be made of four 4-bit slices. 5

6 a. Diagrammatically show the different register organization of CPU. 5

b. Explain the different steps of an instruction cycle with interrupts. 5

c. Describe the read and write operations when synchronous timing is used in bus. 4

d. What are the major functions of different layers of Intel QPI Interconnect? 6

7 a. What are the merits and demerits of associative mapping in cache memory? 4

b. 'Shortcomings of associative mapping in cache memory can be solved by set-associative mapping' – justify this statement. 4

c. Take a data of 8 bits long. Assume the required number of check bits. Compute the syndrome word. Suppose its (a) 2^{nd} bit and (b) 4^{th} bit (separately) get flipped due to error. Use Hamming error detection and correction method to rectify it. 12

8 Write short note on the following (any two) 2x10

a. PCIe Configuration

b. State-table method and Delay-element method

c. Peripheral processor and Co-processor

d. Direct mapping in cache memory