Ref. No.: Ex/MECE 518(A)/2018

M.Tech Intelligent Automation and Robotics, 1st Year 2nd Semester, 2018

EMBEDDED SYSTEMS AND TECHNOLOGIES

Time: 3 Hours. Full Marks: 100

Answer any **four** questions.

1. (a) Design an ASIC for a Fibonacci sequence generator to count 1st N numbers in the sequence. Draw the state diagram, data flow path and necessary pin configuration of the designed ASIC. 12

   (b) Design a comparator to supplement the design in part (a) for $i \leq N-1$ realization. 8

   (c) Write the comparison between RISC and CISC architecture. 5

2. (a) Explain the essence of a hierarchical state machine with reference to an elevator control logic design as an example. 8

   (b) Design a pulse divider ASIC, that produces a pulse x after receiving four pulses at terminal 'a'. 10

   (c) For the lattice automaton, given in Fig. 1(a), determine the lattice belief to recognize the string: 'ab'. Use the lattice shown in Fig. 1(b) for your computation. 7

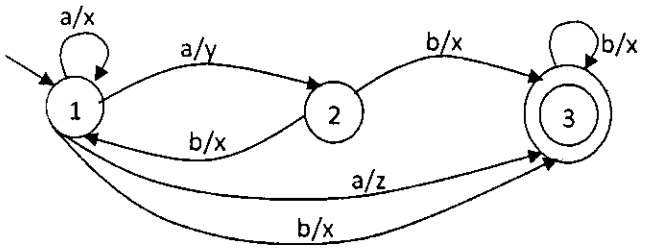


Fig. 1(a)

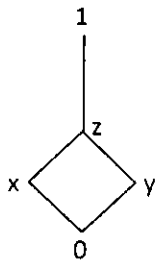


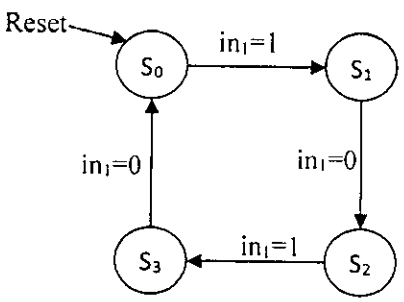
Fig. 1(b)

3. (a) Draw the schematic architecture of an ARM processor and state its fundamental features. Explain how the instruction STR $r_0,[r_1]$ is executed by the ARM processor. 8

   (b) What is hardware/software partitioning problem? What is task graph? What are task splitting and task merging? 5

   (c) Presume that given a table showing time required for execution on different software and hardware units of task T_1 to T_6. Also presume that given a task graph for the same tasks. How will you solve the hardware/software partitioning problem? 12

4. (a) Construct a VHDL model for the state machine shown in the following figure. 10



(b) Design a hypothetical two address line PROM to store the following four bit data. 10

Adress		Data			
A_1	A_0	d_3	d_2	d_1	d_0
0	0	0	0	1	1
0	1	1	0	0	1
1	0	1	1	1	1
1	1	1	0	1	0

(c) Write a short note on CPLD. 5

5. (a) Design an all MOS PAL for the following switching functions. 8

$$Y_1 = AB'C + A'B$$

and $Y_2 = A'BC + AC$.

(b) Realize a half-adder on the Quick logic p-ASIC architecture. Justify your realization. 10

(c) Design an all MOS PLD for the following logic function: 7

$$y_1 = AB'C + A'B\ y_1$$

6. (a) Draw a block diagram of a dot-matrix printer. Explain how the printer CPU functions in controlling data transfer from the data buffer to the print-head. 9

(b) Show an interface between the user's microcomputer with a dot-matrix printer for data transfer. 10

(c) Draw a flowchart to transfer data to a dot-matrix printer from the user's buffer area. 6

7. Write short notes on any two: $12.5 \times 2 = 25$

(a) Comparison between PROM, PLA and PAL.

(b) Concurrency handling in VHDL using NAND-XOR system.

(c) Stochastic vs. Fuzzy automaton.

(d) Ant Colony Optimization Principle.