

5

DIODE-TRANSISTOR LOGIC

In this chapter we consider a logic family, *diode-transistor logic* (DTL), whose circuitry is somewhat more involved than RTL. Although DTL has the advantage of greater fan-out and improved noise margins, it suffers from somewhat slower speed.

5.1 DIODE-TRANSISTOR-LOGIC (DTL) GATE

A diode-transistor-logic gate as realized with discrete components is shown in Fig. 5.1-1. Transistor T_0 is the output transistor (corresponding to T_2) of a preceding gate. Three inputs are indicated, but, of course, more can be added by adding more diodes to the array of diodes DA , DB , and DC .

The gate performs the NAND operation for positive logic. Consider that the driving gate T_0 is at logic level 0. Then T_0 is in saturation, and the corresponding collector voltage is $V_i \approx 0.2$ V or lower. We can verify that when the input in Fig. 5.1-1 is $V_i = 0.2$ V, T_2 is cut off and the output at the

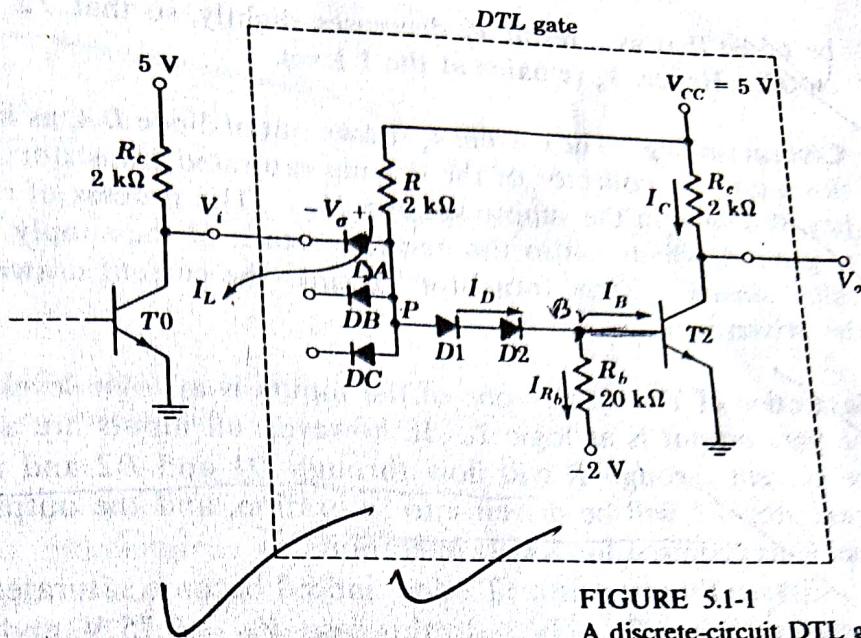


FIGURE 5.1-1
A discrete-circuit DTL gate.

collector is $V_{cc} = 5$ V, which corresponds to logic level 1. For, with the input at 0.2 V, the voltage at point P is

$$V_p = V_{CE}(\text{sat}, T0) + V_{DA} = 0.2 + 0.75 = 0.95 \quad \text{at } T = 25^\circ\text{C} \quad (5.1-1)$$

Here we have assumed that the current in diode DA, which is approximately 2 mA, is adequate to produce a voltage drop of 0.75 V across diode DA. The base-to-ground voltage of T2 is then

$$V_{B2} = V_p - V_{D1} - V_{D2} = 0.95 - 0.65 - 0.65 = -0.35 \text{ V} \quad (5.1-2)$$

Here we have taken $V_{D1} = V_{D2} = 0.65$ since, as will appear, the currents in D1 and D2 are very small. This voltage V_{B2} is less than the cut-in voltage $V_y = 0.65$ V of transistor T2, and therefore T2 is cut off. Thus, the current in diodes D1 and D2 continues through resistor R_b , and this current is

$$I_{R_b} = I_D = \frac{V_{B2} + 2}{R_b} = \frac{-0.35 + 2}{20 \times 10^3} = 0.08 \text{ mA} \quad (5.1-3)$$

This result confirms our initial assumption that the diode current is indeed quite small. Finally, since T2 is cut off, the output voltage $V_o = 5$ V, corresponding to logic level 1.

We have shown that if V_i is at logic level 0, V_o is at logic level 1. Similarly we can show that if all of the inputs are at logic level 0, V_o remains at logic level 1. For, if all the inputs are simultaneously at logic level 0, the current through resistor R will divide among the diodes DA, DB, DC, ... With a smaller current through, say, DA, the drop across this diode will decrease slightly. It should

be noted that as a result V_p decreases slightly, so that T_2 is forced further into cutoff. Hence, V_o remains at the 1 level.

Current sinking The current I_L drawn out of diode DA , as indicated in Fig. 5.1-1, flows into the collector of the driving saturated transistor T_0 . This current I_L has its source in the supply voltage V_{cc} . The process of returning this current to ground, which is also the negative return of the supply source, is commonly called *sinking*. Thus, transistor T_0 sinks the current drawn out of the input of the driven gate.

Saturation of T_2 If any one of the inputs is at logic level 0, T_2 is cut off and the gate output is at logic 1. If, however, all inputs are at logic level 1 (5 V), the current through R will flow through D_1 and D_2 and into the base of T_2 . Transistor T_2 will be driven into saturation, and the output will drop to logic level 0, as required for NAND operation.

To see that transistor T_2 does indeed become saturated let us calculate the base current $I_B = I_D - I_{R_b}$. In this case, $V_{B2} = 0.75$ V, and the current in R_b is

$$I_{R_b} \approx \frac{0.75 + 2}{20 \times 10^3} \approx 0.14 \text{ mA} \quad (5.1-4)$$

The voltage at point P is now $V_p = V_{D1} + V_{D2} + V_{B2} \approx 2.25$ V, where we have assumed that I_D and I_B are sufficiently large to cause the diode and base-emitter voltage to be approximately 0.75 V. Thus, the diode current I_D , which is also the current in resistor R , is

$$I_D = \frac{V_{cc} - V_p}{R} = \frac{5 - 2.25}{2 \times 10^3} \approx 1.4 \text{ mA} \quad (5.1-5)$$

The base current of transistor T_2 is the difference between the currents I_D and I_{R_b} and is

$$I_B = I_D - I_{R_b} \approx 1.26 \text{ mA} \quad (5.1-6)$$

which is clearly sufficient to saturate transistor T_2 , since with $V_{ce}(\text{sat}) \approx 0.2$ V, $I_c = 2.4$ mA. Assuming that $h_{FE} = 50$, this collector and base current corresponds to $\alpha = 0.04$. Referring to Fig. 1.10-1, we find that $V_{ce}(\text{sat})$ is more nearly 0.1 V than 0.2 V.

Base resistor R_b If transistor T_2 is in saturation, and if then one or more of the gate inputs returns to logic level 0, point P falls to $V_p = 0.95$ V. The equivalent circuit of the gate at this instant is as shown in Fig. 5.1-2. Note that the voltage drop across both diodes D_1 and D_2 is 0.2 V and therefore these diodes are cut off. Hence, $I_D = 0$, and there is no current source to supply I_B .

If there were no charge storage in the system, I_B would instantly drop, causing the base-emitter voltage to fall below its cut-in voltage, and therefore T_2 would immediately cut off. The steady-state base-emitter voltage would then be -0.35 V [see Eq. (5.1-2)]. However, there is charge stored in the transistor.

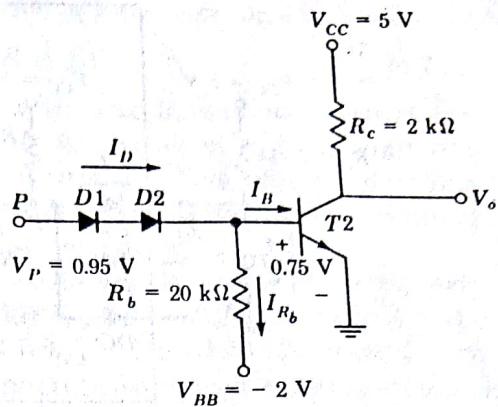


FIGURE 5.1-2
Equivalent circuit of the DTL gate at the instant that V_P is decreased to 0.95 V

When point P drops, momentarily cutting off diodes $D1$ and $D2$, this stored charge leaves through resistor R_b . Thus, resistance R_b provides a discharge path for the charge stored in the transistor. Resistor R_b is connected to the -2 V supply to increase the rate of discharge.

The selection of $R_b = 20 \text{ k}\Omega$ and $V_{BB} = -2 \text{ V}$ (rather than, say, $R_b = 1 \text{ k}\Omega$ and $V_{BB} = -4 \text{ V}$) is the result of a compromise. Many values of resistance and supply voltage are possible, and most will result in satisfactory operation. To increase the rate of charge removal and therefore decrease the time needed to cut off $T2$, we would like R_b to be small and V_{BB} to be very negative. However, when $T2$ is cut off and we attempt to turn it on quickly, we would like all the diode current I_D to flow into the base of $T2$. In this case we would like R_b to be very large and V_{BB} to be positive. Typical values of R_b range from 5 to 30 $\text{k}\Omega$, and values of V_{BB} vary from 0 to -5 V .

5.2 FAN-OUT

Figure 5.2-1 shows the DTL gate driving N other gates. When the gate output transistor $T0$ is sinking the current of a gate $G1$ that it is driving, it encounters its heaviest loading when all the other inputs of the driven gate are at logic level 1 (or equivalently when all other inputs are left floating). For, in this case all the current through R continues through DA and into the collector of $T0$. On the basis of the previous discussion [see Eq. (5.1-1)] this current is

$$I_L = \frac{5 - 0.95}{R} = \frac{4.05}{2 \text{ k}\Omega} \approx 2 \text{ mA} \quad (5.2-1)$$

In any event, it is clear that to minimize the input loading due to DTL gate $G1$ it is advantageous to make R a large resistance.

On the other hand, consider that all inputs of gate $G1$ are at logic level 1. In this case current I_D flows from V_{CC} , through R and the diodes $D1$ and $D2$, and finally divides between R_b and the base of $T2$. Transistor $T2$ should now

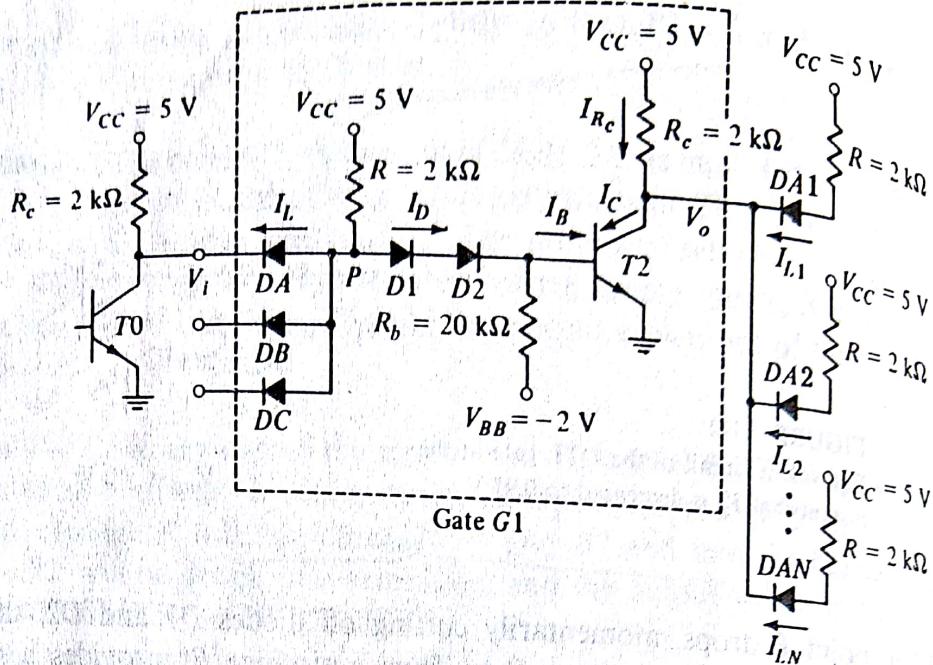


FIGURE 5.2-1
A DTL gate with fan-out.

be in saturation. Now, to see the relationship between the fan-out N of gate G_1 and the resistor R , let us assume that the collector voltage of T_2 , when saturated, is $V_o = 0.2$ V. Then the current in each of the N loading gates is

$$I_{L1} = I_{L2} \cdots = I_{LN} \approx \frac{V_{cc} - V_{DA1} - V_o}{R} = \frac{5 - 0.75 - 0.2}{R} \approx \frac{4}{R} \quad (5.2-2)$$

To arrive at this result we have assumed that all the current flowing in R , in each of the driven gates, flows into T_2 . We are therefore neglecting the current flow in diodes D_1 and D_2 of these driven gates. This neglected current is approximately 0.08 mA [see Eq. (5.1-3)] and is negligible.

The total collector current in T_2 is then

$$I_C = I_{R_c} + NI_{L1} = \frac{V_{cc} - V_o}{R_c} + \frac{4N}{R} = 2.4 \text{ mA} + \frac{4N}{R} \quad (5.2-3)$$

The base current in T_2 is I_B and is found, as before, by noting that $V_P = 2.25$ V when T_2 is saturated. Again, neglecting the current in R_b , we have

$$I_B \approx I_D = \frac{V_{cc} - V_P}{R} = \frac{2.75}{R} \quad (5.2-4)$$

Since we require that T_2 be driven to saturation, we also have

$$I_C = \sigma h_{FE} I_B \quad (5.2-5)$$

in which the value of σ can be estimated from Fig. 1.10-1 after we have decided what value we want for $V_{CE}(\text{sat})$, that is, how deeply T_2 is to be driven to saturation.

Combining Eqs (5.2-3) to (5.2-5) and solving for N , the fan-out, we find

$$N \approx 0.7\sigma h_{FE} - 0.6R \times 10^{-3} \quad (5.2-6)$$

Observe that to increase N we must increase σ ; that is, we must restrict the extent to which T_2 is driven into saturation. As we increase N , a point will be reached where $\sigma = 1$ and T_2 is no longer saturated. This situation develops because each additional load on the driving gate requires T_2 to sink an additional 2 mA without a compensating increase in base current in T_2 .

Assume $h_{FE} = 50$, $R = 2 \text{ k}\Omega$, and that $\sigma = 0.85$. This value of σ corresponds to a modest excursion into saturation and yields $V_{CE}(\text{sat}) = 0.2 \text{ V}$ (see Fig. 1.10-1). In this case the first term in Eq. (5.2-6) is $0.7\sigma h_{FE} = 30$, while the second term is $0.6(2) = 1.2$. Thus if we decide that the output transistor need be but moderately saturated, the fan-out $N = 29$. This result would not change appreciably if R were doubled or halved. Hence, we may neglect this second term and estimate that $N = 0.7\sigma h_{FE}$, depending only on h_{FE} and not on R . This relative independence of N from R is to be anticipated on the basis of the following consideration. If R changes, say decreases, the base current of T_2 increases. However, the current which T_2 must sink for each additional load increases correspondingly, so that there is no net increase in allowable fan-out. It should be noted that if we decided that $V_{CE}(\text{sat}) = 0.1 \text{ V}$ under maximum fan-out, then $\sigma = 0.1$ and $N = 2$. Now the fan-out depends on σh_{FE} and R .

In the next section, when we consider the DTL gate in integrated-circuit form, we shall see how a modification of the circuitry devises to increase the base drive of the output transistor without a corresponding increase in the current load imposed by each additional gate. As a result the fan-out is significantly increased.

5.3 INTEGRATED-CIRCUIT DTL GATES

The DTL gate in integrated form is shown in Fig. 5.3-1. It is commercially available with either $R_c = 2 \text{ k}\Omega$ or $R_c = 6 \text{ k}\Omega$. In the former case the power dissipation is higher than in the latter case. However, all capacitance shunting the collector of T_2 to ground must charge through R_c when T_2 goes off. Hence, with $R_c = 2 \text{ k}\Omega$ the propagation delay time is smaller than with $R_c = 6 \text{ k}\Omega$.

We observe that in the integrated circuit of Fig. 5.3-1 transistor T_1 , whose collector is connected to a tap on R , is used in lieu of diode D_1 in the discrete circuit of Fig. 5.1-1. It is to be recalled, however, that in integrated circuitry a diode is normally a transistor with its collector tied to its base. Hence, the change involved is not so much the replacement of a diode by a transistor as simply a new connection for the collector. This new transistor T_1 operates in its active region and provides current gain between its base and emitter. Hence, it makes available more current for the base of T_2 without requiring a reduction in the resistance R .

We now explain the effect of this new transistor and the tap position. Let

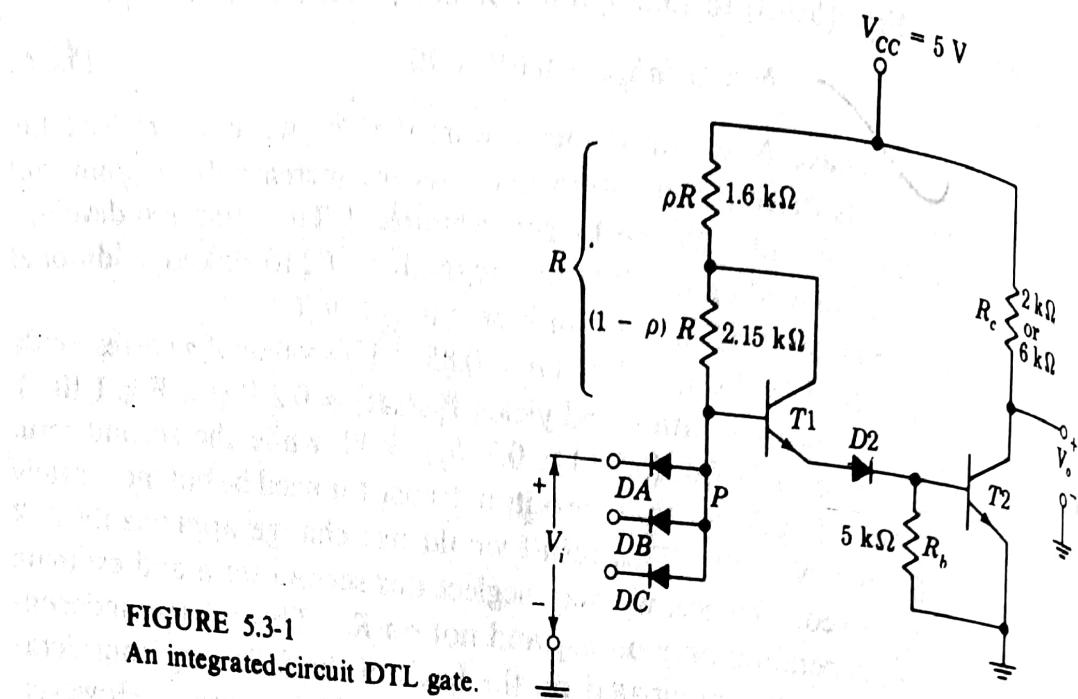


FIGURE 5.3-1
An integrated-circuit DTL gate.

us begin by calculating the fan-out of the gate shown in Fig. 5.3-2. Let us assume, as before, that when T_2 is saturated, $V_o = 0.2$ V. Then, if the gate is fanned out to N loading gates, the load currents which must sink through T_2 are given, as in Eq. (5.2-2), as

$$I_{L1} = I_{L2} = \dots = I_{LN} \approx \frac{5 - 0.95}{R} \approx \frac{4}{R} \quad (5.3-1)$$

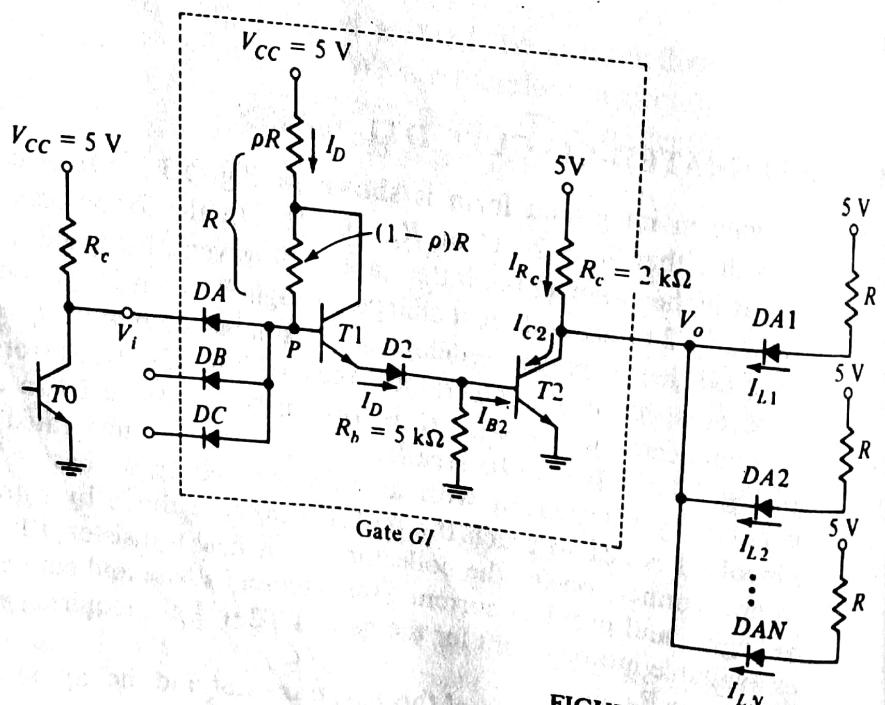


FIGURE 5.3-2
DTL gate with a fan-out of N .

Since the current in resistor R_c is $4.8/(2 \times 10^3) = 2.4 \text{ mA}$, the collector current is

$$I_{C2} = 2.4 \times 10^{-3} + \frac{4N}{R} \quad (5.3-2)$$

This result, of course, is identical to that obtained in Eq. (5.2-3).

We now calculate the base current I_{B2} , again assuming that the current in R_b is negligibly small. First, we note that the voltage at point P is

$$V_P = V_{BE1} + V_{D2} + V_{BE2} = 0.75 + 0.75 + 0.75 = 2.25 \text{ V} \quad (5.3-3)$$

The calculation of $I_{B2} = I_D$ can now be easily performed with the help of Fig. 5.3-3. Let the base current in $T1$ be called I . Then $I_{B2} = (h_{FE} + 1)I$. Hence

$$V_{CC} - V_P = \rho R(h_{FE} + 1)I + (1 - \rho)RI \quad (5.3-4)$$

Solving for $(h_{FE} + 1)I = I_{B2}$ yields

$$I_{B2} = (h_{FE} + 1)I = \frac{V_{CC} - V_P}{R[\rho + (1 - \rho)/(h_{FE} + 1)]} \quad (5.3-5)$$

in which $V_{CC} - V_P = 2.75 \text{ V}$.

Since $\sigma h_{FE} I_{B2} = I_{C2}$, we have, combining (5.3-2) and (5.3-5),

$$\frac{2.75\sigma h_{FE}}{R[\rho + (1 - \rho)/(h_{FE} + 1)]} = 2.4 \times 10^{-3} + \frac{4N}{R} \quad (5.3-6)$$

Solving for the fan-out N yields

$$N \approx \frac{0.7\sigma h_{FE}}{\rho + (1 - \rho)/(h_{FE} + 1)} - 0.6R \times 10^{-3} \quad (5.3-7)$$

When $\rho = 1$, Eq. (5.3-7), as required, reduces to Eq. (5.2-6). As ρ decreases, the fan-out increases. In typical commercial DTL integrated-circuit gates $1/\rho$ is in the range 2 to 10. With $h_{FE} \approx 50$ and assuming, as in the previous section,

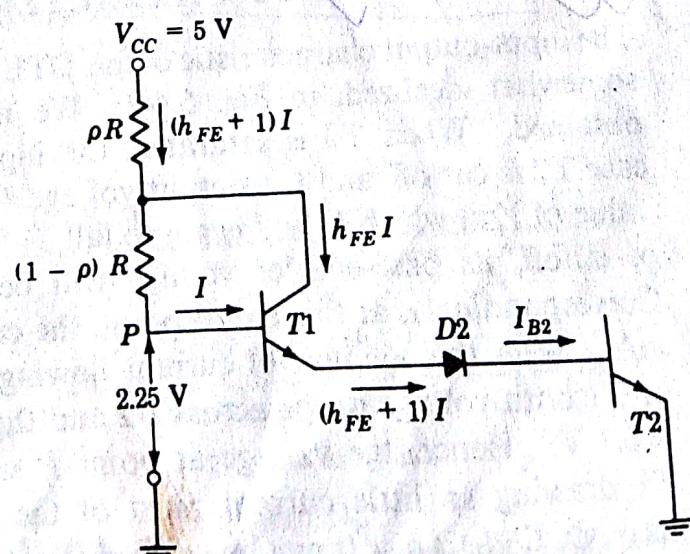


FIGURE 5.3-3
Circuit to show the effect of splitting the base resistor R .

that σ is in the range $\sigma \approx 0.85$, we have approximately that

$$N = \frac{0.7\sigma h_{FE}}{\rho} \quad (5.3.8)$$

Thus, we conclude that the new circuit increases the fan-out by the factor $1/\rho$ or, equivalently, that if we keep N fixed, we may drive the output transistor further into saturation by decreasing σ by the factor $1/\rho$.

The mechanism of increase in fan-out is the following. When the gate input V_i in Fig. 5.3-2 is at logic 0, T_1 is OFF and the driving gate sees the same load as in the circuit of Fig. 5.2-1. When, however, V_i is at logic 1, T_1 is ON and provides current gain. Hence the base current available for the output transistor is larger (by the factor $1/\rho$) than it would be if all the base current had to be furnished directly through the entire resistor R .

Equation (5.3-8) suggests that it might be advisable in Fig. 5.3-1 to move the tap on R closer to V_{CC} (letting $\rho \rightarrow 0$), thereby increasing the base drive of T_2 and the fan-out. The difficulty with such a procedure is that increasing the base current will result in an increase in the power dissipated in T_2 . Furthermore, if the gate is operated with a fan-out which is less than maximum, T_2 will be heavily saturated, thereby increasing the propagation delay time required to remove T_2 from saturation. The component values employed in the DTL gate represent a compromise, taking account of fan-out, propagation delay, and power dissipation.

A last feature to be noted in the gate on Fig. 5.3-1 is that the negative supply return of R_b has been eliminated. It is, of course, a great convenience to be able to operate the gate with a single supply voltage. We observe, however, that since we require that the stored charge in the base be drawn out of T_2 through R_b , the resistor R_b is much smaller in the integrated-circuit gate than in the discrete circuit.

5.4 INPUT-OUTPUT CHARACTERISTIC

The input-output characteristic of the DTL gate of Fig. 5.4-1 has the form shown, somewhat idealized, in Fig. 5.4-2. We now show how this characteristic is obtained. When T_0 is saturated, the input voltage V_i is $V_i \approx 0.2$ V. In this case T_2 is cut off, and the output voltage $V_o = V_{CC} = 5$ V. We can estimate the value of V_i at which V_o will begin to fall as follows. When T_2 is just at the edge of cutoff, its base-emitter voltage will be about $V_y = 0.65$ V (at $T = 25^\circ\text{C}$). Correspondingly, at this cut-in point, the current $I_{D2} \approx 0$ and $I_D = V_y/R_b \approx 0.13$ mA. With this amount of current flowing in diode D_2 and out of the emitter of T_1 both voltage drops across D_2 and the base-emitter junction of T_1 will be ≈ 0.7 V. Hence, the voltage at point P will be $2(0.7) + 0.65 = 2.05$ V. With T_1 drawing so little current most of the current through R will be flowing through diode D_A . It can be verified (Prob. 5.4-1) that at this point the current

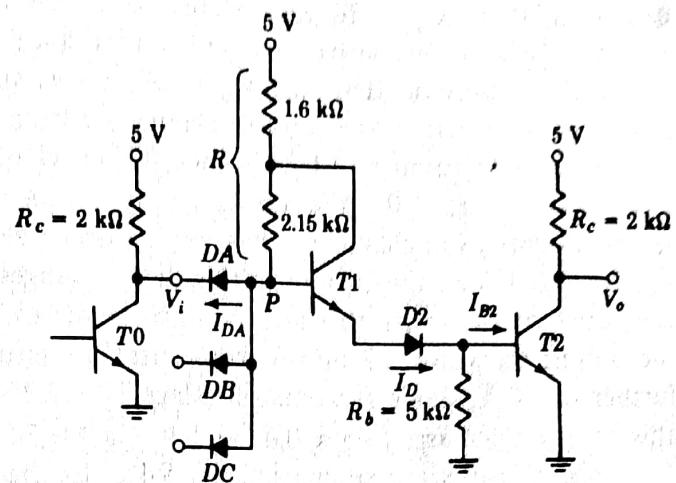


FIGURE 5.4-1
Circuit used to calculate the unloaded input-output characteristic.

$I_{DA} \approx 0.75$ mA. With this current, the drop across the input diode DA will be more nearly $V_{DA} \approx 0.75$ V. Hence (at $T = 25^\circ\text{C}$) the input voltage is $V_i = 2.05 - 0.75 = 1.3$ V, as indicated in Fig. 5.4-2.

We now calculate the minimum value of V_i needed to saturate T_2 . When T_2 switches from the edge of cutoff, $V_{BE2} = V_y = 0.65$ V, to saturation, $V_{CE2} = 0.2$ V, the collector current I_{C2} changes by approximately $\Delta I_{C2} \approx 2.4$ mA and the base current changes by $\Delta I_{B2} = \Delta I_{C2}/\sigma h_{FE} \approx 60 \mu\text{A}$ ($\sigma \approx 0.85$). Furthermore, since V_{BE2} changes by 0.1 V, from V_y to V_o , the change in the current

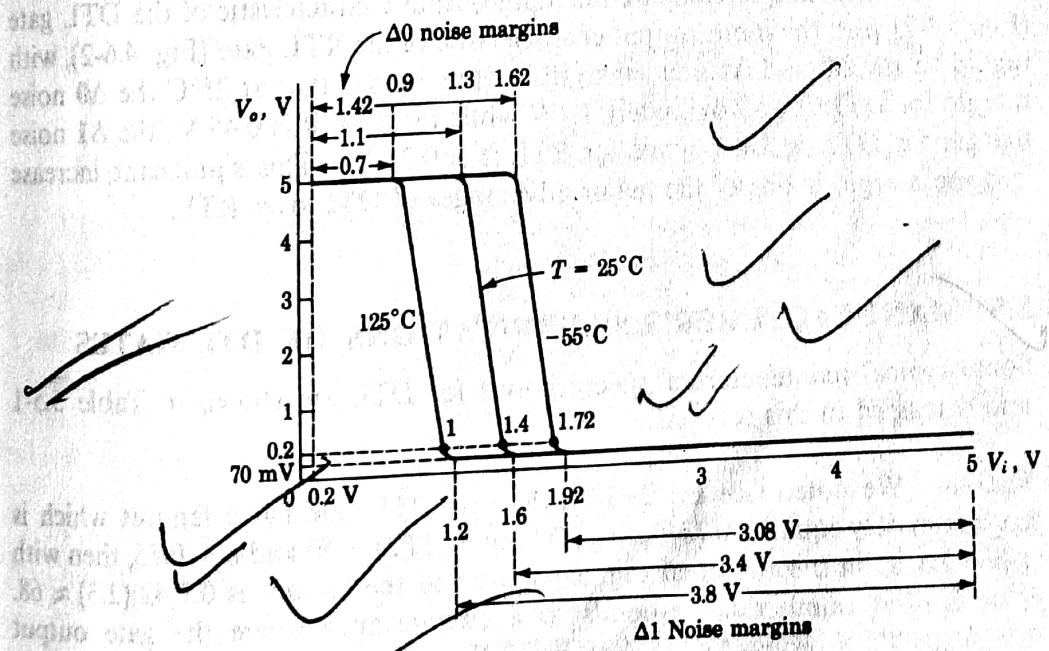


FIGURE 5.4-2
The unloaded input-output characteristic.

flowing in R_b is $\Delta I_{R_b} = 20 \mu\text{A}$. Hence, $\Delta I_{E_1} = 80 \mu\text{A}$ and $\Delta I_{B_1} \approx \Delta I_{E_1}/h_{FE} = 1.6 \mu\text{A}$. This increase in base current results in a decrease in diode current I_{D_1} which is also approximately $1.6 \mu\text{A}$. Hence, a very small change in the current in diode D_A is all that is necessary to change T_2 from cutoff to saturation.

Since the current in T_1 and diode D_2 has changed by $80 \mu\text{A}$, from $130 \mu\text{A}$ when $V_{BE2} = V_i$ to $210 \mu\text{A}$ when $V_{BE2} = V_\sigma$, we can assume that V_{BE1} and V_{D_2} remain essentially unchanged. This assumption is certainly valid when considering diode D_A since the current in this diode changes by only $1.6 \mu\text{A}$. Thus, we can conclude that when the input voltage increases by 0.1 V from 1.3 V to 1.4 V , the output transistor T_2 moves from cutoff to saturation. When V_i increases further to 1.6 V , diode D_A cuts off (since $V_p = 2.25 \text{ V}$) and $I_{B_2} \approx 1.5 \text{ mA}$. At this point σ decreases to $\sigma \approx 0.03$ and $V_{CE}(\text{sat}) \approx 70 \text{ mV}$ (see Fig. 1.10-1).

These results are shown in Fig. 5.4-2. In the plots for $T = -55^\circ\text{C}$ and $T = +125^\circ\text{C}$, also given in this figure, we have assumed, as usual, that the temperature sensitivity of a junction voltage is $-2 \text{ mV}/^\circ\text{C}$. However, as before, we have ignored the temperature dependence of $V_{CE}(\text{sat})$. The details of the calculations leading to the input-output characteristics are left as problems.

The input-output characteristic shown in Fig. 5.4-2 is somewhat idealized inasmuch as we performed the calculation for the case where T_2 is unloaded, i.e., has a fan-out of 0. A typical fan-out for a DTL gate is 8. If we had taken the fan-out into account, as illustrated in Fig. 5.3-2, we would see that when T_2 is cut off, V_o is still equal to 5 V since $D_{A1}, D_{A2}, \dots, D_{AN}$ are also cut off. As discussed in Sec. 5.3, the effect of too large a fan-out is to increase the collector current in T_2 , thereby raising T_2 out of saturation and increasing V_o above 0.2 V when $V_i = 5 \text{ V}$. For the maximum fan-out of 8 specified by the manufacturer this problem does not arise.

It is interesting to compare the input-output characteristic of the DTL gate (Fig. 5.4-2) with the input-output characteristic of the RTL gate (Fig. 4.6-2), with regard to the $\Delta 0$ and $\Delta 1$ noise margins. Here we see that at 25°C the $\Delta 0$ noise margin for DTL is approximately 1.2 V while for RTL it is 0.45 V ; the $\Delta 1$ noise margin for DTL is 3.4 V while for RTL it is 0.24 V . This significant increase in noise margin is one of the major advantages of DTL over RTL.

5.5 MANUFACTURER'S SPECIFICATIONS OF DTL GATES

Some typical manufacturers' specifications for DTL are shown in Table 5.5-1 and discussed in this section.

Fan-out We noted [see Eq. (5.3-7)] that the DTL gate has a fan-out which is approximately equal to $0.7\sigma h_{FE}/\rho$. Taking $h_{FE}(T_2) = 50$ and $\sigma = 0.85$, then with $1/\rho = 2.3$, as in the circuit of Fig. 5.4-1, we find the fan-out is $0.7(42)(2.3) \approx 68$. This fan-out number corresponds to a circumstance where the gate output transistor T_2 is brought to $V_{CE}(\text{sat}) = 0.2 \text{ V}$. If we assume that $V_{CE}(\text{sat}, T_2) = 0.1 \text{ V}$, then $\sigma = 0.1$ and the maximum fan-out is reduced to 8.

The manufacturer specifies a typical fan-out of 8 for the DTL gate and 25 for the buffer. The buffer employs an active pull-up similar to that employed in RTL. A detailed analysis of the DTL buffer is left for Prob. 5.4-6. Furthermore, each gate loading the driving gate appears as a 10-pF capacitor. Thus, a load of eight gates acts like a 80-pF capacitor and therefore affects the propagation delay time of the loaded gate. Thus, the specified fan-out of 8 ensures that the propagation delay time requirement of 30 to 40 ns is satisfied and that the collector-emitter voltage of the output transistor is approximately 0.1 V.

Voltage levels The specified voltage levels V_{oH} , V_{IH} , V_{IL} , and V_{oL} are shown in Fig. 5.5-1 for $T = 25^\circ\text{C}$. The voltage V_{oH} is the minimum output voltage of a gate corresponding to the logic 1 state. The value of the load current I_L when $V_o = V_{oH}$ is called I_{oH} . The value of 2.6 V shown in Table 5.5-1 is recommended by one manufacturer. Another manufacturer lists $V_{oH} = 4.3$ V. To estimate V_{oH} we refer to Fig. 5.4-1 and let $T2$ be cut off. Then assuming $V_{CC} = 5$ V \pm 10 percent, $R_c = 2 \text{ k}\Omega$, a leakage current $I_L = 50 \mu\text{A}$, and $I_{oH} = -0.12$ mA, we find

$$V_o = V_{oH} = 4.5 - 2,000(50 + 120) \times 10^{-6} = 4.16 \text{ V} \quad (5.5-1)$$

If V_{oH} is calculated for $I_{oH} = 0$, that is, no load, we find

$$V_{oH} = 4.4 \text{ V} \quad (5.5-2)$$

This is similar to the value presented by one manufacturer.

Table 5.5-1 TYPICAL MANUFACTURERS SPECIFICATIONS AT 25°C FOR DTL NAND GATE AND BUFFER

	Gate	Buffer
Output loading factor (fan-out)	8	25
Input loading factor	1	1
Power dissipation, mW	11	42
Input voltage, $V: V_{IL}$	1.1	1.1
V_{IH}	2	2
Output voltage, $V: V_{oL}$	0.4	0.4
V_{oH}	2.6*	2.6†
Output leakage current $I_L, \mu\text{A}$	50	50
Reverse diode current $I_R, \mu\text{A}$	2	2
Forward current of input diodes I_F for a unit input load, mA	1.6	1.6
Propagation delay time $t_{pd}(HL)$	30	40
$t_{pd}(LH)$	80	80

* $I_{oH} = -0.12$ mA

† $I_{oH} = -2.5$ mA.

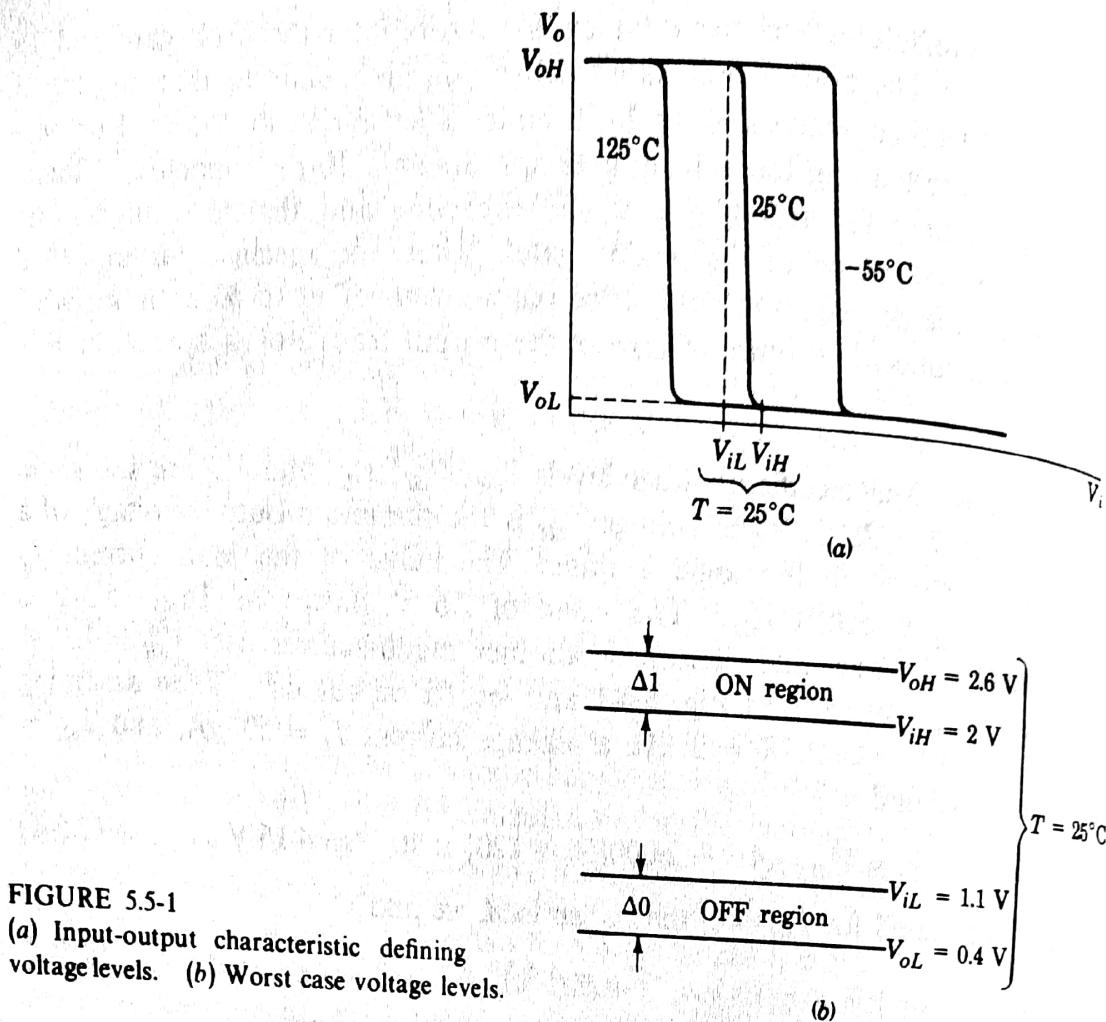


FIGURE 5.5-1
 (a) Input-output characteristic defining voltage levels. (b) Worst case voltage levels.

The maximum output voltage of the gate corresponding to the logic level 0 is V_{oL} . We have estimated that at a fan-out of 8, $V_{oL} = V_{CE}(\text{sat}) = 0.1\text{ V}$. The manufacturer, in order to be extremely conservative, will only say that the collector-emitter voltage V_{oL} will never exceed 0.4 V.

The maximum allowable input voltage which will reliably be recognized as corresponding to logic level 0 is V_{iL} , and the minimum allowable input voltage which will reliably be recognized as corresponding to logic level 1 is V_{iH} . The temperature dependence of these parameters is brought out in Fig. 5.5-1. Our calculations indicate that, at 25°C , $V_{iL}(\text{max})$ should be approximately 1.3 V and $V_{iH}(\text{min})$ about 1.6 V. We find (see Table 5.5-2) that the manufacturer's

Table 5.5-2

	-55°C	25°C	125°C
V_{iH}, V	2.1	2	1.9
V_{iL}, V	1.4	1.1	0.8
$\Delta 0$	1.0	0.7	0.4
$\Delta 1$	0.5	0.6	0.7

specification on V_{IL} is 1.1 V, while the specification on V_{IH} is 2 V. Again, we note that these specified values represent worst-case conditions.

Noise immunity The $\Delta 0$ and the $\Delta 1$ noise immunity are given by

$$\Delta 0 = V_{IL} - V_{oL} \quad (5.5-3)$$

$$\Delta 1 = V_{oH} - V_{IH} \quad (5.5-4)$$

The parameters V_{IH} and V_{IL} as specified by the manufacturer are summarized in Table 5.5-2. Using $V_{oH} = 2.6$ V and $V_{oL} = 0.4$ V (since these values do not change significantly with temperature), we can calculate $\Delta 0$ and $\Delta 1$, which are also tabulated in Table 5.5-2. The value $V_{oH} = 2.6$ V seems unreasonably conservative. It may have been selected by the one manufacturer in order simply to arrange that the noise margins $\Delta 0$ and $\Delta 1$ be nearly equal to one another. Note the significant increase in the noise immunity of DTL compared with that of RTL.

Propagation delays Propagation delays in DTL gates are of the order of 30 to 80 ns. The delay associated with turning on the output transistor [the turn-on delay $t_{pd}(HL)$] is smaller than the delay associated with driving that transistor back to cutoff [the turn-off delay $t_{pd}(LH)$]. The turnoff delay is generally substantially larger than the turn-on delay, often by a factor of 2 or 3. For, at turn-on, any capacitance shunting to ground the output of the gate can discharge rapidly through the low impedance of a transistor in saturation. At turnoff, however, this shunt capacitor must charge through the relatively large pull-up resistor R_c . In addition, at turnoff, there is a storage-time delay in the output transistor T_2 which is not encountered at turn-on.

5.6 THE WIRED-AND CONNECTION

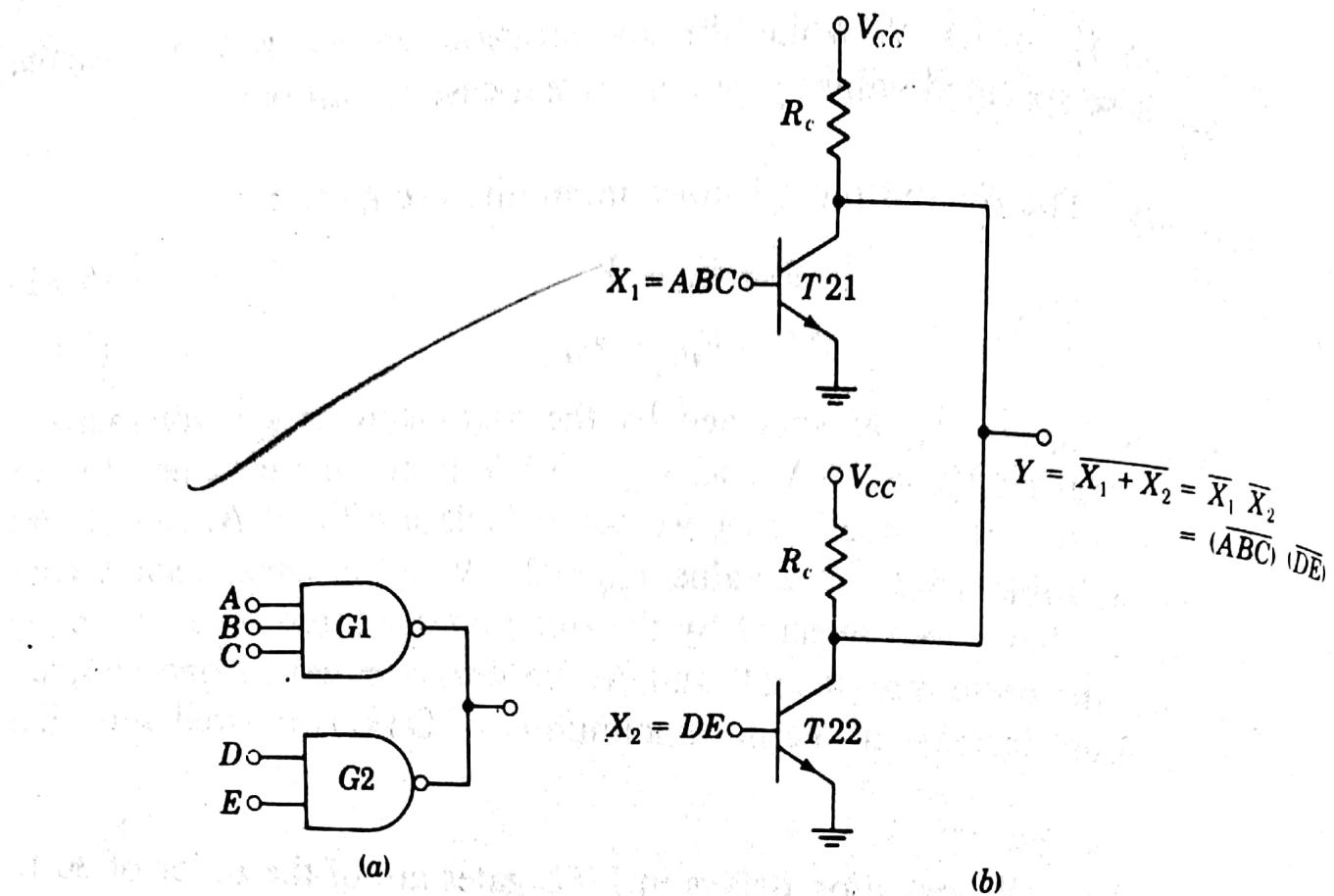
A useful extension of the logic capability of DTL gates can be achieved by joining the outputs of two DTL gates. Such a connection of outputs into a single common output is indicated in Fig. 5.6-1a. In Fig. 5.6-1b is shown the output transistor of each of the two gates with their collectors tied together to a common output Y . For the inputs given in Fig. 5.6-1a the logic variables which appear at the bases of these two transistors are $X_1 = ABC$ and $X_2 = DE$, as shown in Fig. 5.6-1b. Additionally, it is readily verified (compare with the RTL gate of Fig. 4.4-1) that $Y = \overline{X_1 + X_2} = \overline{ABC + DE}$. Hence, altogether we have

$$Y = \overline{X_1 + X_2} = \overline{ABC + DE} \quad (5.6-1)$$

or, using De Morgan's theorem,

$$Y = \overline{X_1} \overline{X_2} = (\overline{ABC})(\overline{DE}) \quad (5.6-2)$$

From Eq. (5.6-1) it appears as though tying the outputs together resulted in a NOR operation. On the other hand, from Eq. (5.6-2) we can interpret the result



(b)

FIGURE 5.6-1
The WIRED-AND connection.

as what would be obtained if the outputs of the individual DTL gates, when not joined, were combined in an AND gate. This result applies as well if more than two gates are connected at their outputs. This consideration leads to the description of the arrangement of Fig. 5.6-1 as a WIRED-OR or a WIRED-AND connection of DTL gates. In this text we shall use the terminology WIRED-AND.

To appreciate the usefulness of the WIRED-AND connection, consider that we did indeed want to generate the logical function Y given in Eq. (5.6-1) or (5.6-2); and suppose that we were restricted to using the DTL NAND gates in the conventional manner. Then, as already noted, we should have to combine the DTL-gate outputs \overline{ABC} and \overline{DE} in an AND gate. An AND gate, when constructed from NAND gates, requires two such NAND gates. Hence, altogether, the equivalent of the gating circuit of Fig. 5.6-1a would appear as shown in Fig. 5.6-2 and require a total of four gates.

Loading rules In the WIRED-AND connection of a number of DTL gates, it may happen that only one output transistor is conducting while the others are

all cut off. Then this transistor must not only sink the current of the loading gates and the current due to its own pull-up resistor but must also sink the current in the pull-up resistor of the other output transistors. To allow for this situation it is necessary to reduce the allowable fan-out of each gate in the WIRED-AND connection. This fan-out reduction is calculated in the following example.

EXAMPLE 5.6-1 A number K of DTL gates are connected in a WIRED-AND connection. Calculate the reduction required in the output loading factor as a function of K .

SOLUTION Refer to Fig. 5.6-3. Here we see the outputs T_1, T_2, \dots, T_K of K gates connected in a WIRED-AND configuration and driving N DTL gates. The driven gates are represented by their input diodes and series resistors R since the load affects the operation of the driving gate only when the driving gates are saturated, in which case all the current in R flows through its series diode.

Now assume that X_1 is in logic level 1 while X_2, \dots, X_K are in logic level 0. Then T_1 is saturated. Let $V_{CE}(\text{sat}) \approx 0.2 V. If the current in each diode, D_1, D_2, \dots, D_N , is called I_L , we have$

$$I_L = \frac{V_{CC} - V_D - V_{CE}(\text{sat})}{R} = \frac{5 - 0.75 - 0.2}{3.75 \times 10^3} = 1.08 \text{ mA} \quad (5.6-3)$$

The currents flowing in the collector resistors of the WIRED-AND output transistors are each equal to I_1 , which is

$$I_1 = I_2 = \dots = I_K = \frac{V_{CC} - V_{CE}(\text{sat})}{R_c} = \frac{5 - 0.2}{2 \times 10^3} = 2.4 \text{ mA} \quad (5.6-4)$$

Thus, the collector current in T_1 is

$$I_{C1} = KI_1 + NI_L = 2.4K + 1.08N \text{ mA} \quad (5.6-5)$$

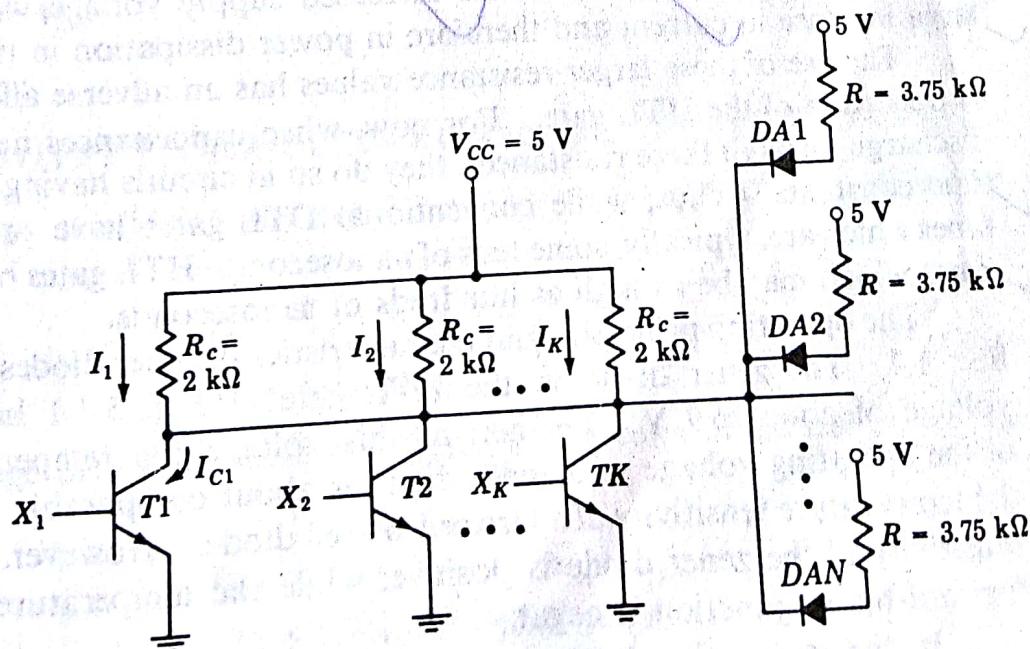


FIGURE 5.6-3
The WIRED-AND connection for K gates.

We see from this expression that increasing K by 1 gate is equivalent, as far as the increase in collector current is concerned, to increasing the fan-out by $\Delta N = 2.4/1.08 = 2.2$ gates.

Thus, for each gate connected in parallel with T_1 to form a WIRED AND, we must reduce the maximum output loading factor by 2.2 gates. This results in leaving the collector current fixed, and therefore T_1 remains saturated. The manufacturer specifies a load reduction of 2.5 gates.

It is of great practical importance to note that DTL gates using an active pull-up, as in the buffer shown in Fig. P5.4-6, should not be used in the WIRED-AND mode. The reason for this restriction is made clear in Sec. 6.14.

5.7 HIGH-THRESHOLD LOGIC (HTL)

There are circumstances where logic circuits must operate in environments which are very noisy electrically. For operation in such surroundings there is available a line of DTL logic circuits with thresholds, i.e., noise immunities Δ_0 and Δ_1 , which are quite high in comparison with the thresholds of conventional DTL circuitry.

A high-threshold-logic (HTL) gate is shown in Fig. 5.7-1. Comparing Fig. 5.7-1 with the conventional gate of Fig. 5.4-1, we note that in the HTL gate the supply voltage has been raised from 5 to 15 V. This feature, as we shall see, accounts for the increased noise immunity. Because of the higher supply voltage, the diode D_2 in Fig. 5.3-1 must sustain a higher voltage and has hence been replaced by a zener diode. We note, additionally, that in the HTL gate the resistance values are appreciably larger than in the conventional gate. This increase in the resistance values is necessary because of the increased supply voltage; for, otherwise, the increased supply voltage would result in a large increase in current and therefore in power dissipation in the HTL gate.

The use of these larger resistance values has an adverse affect on the speed of operation of the HTL gate. For now, when capacitances need to charge or discharge through these resistances, they do so in circuits having relatively larger time constants. Thus, while conventional DTL gates have propagation delay times which are, typically, some tens of nanoseconds; HTL gates have propagation times which may be as high as hundreds of nanoseconds.

The operating principles and characteristics of zener diodes are discussed in Sec. 1.4. The zener diode in the HTL gate of Fig. 5.7-1 has an operating voltage of about 6.9 V. Further, at this voltage the temperature sensitivity of the operating voltage of a zener diode is about comparable in magnitude to the temperature sensitivity of a forward-biased diode. However, the temperature sensitivity of the zener diode is positive, while the temperature sensitivity of a forward-biased junction is negative.

In the conventional DTL gate we noted, as in Fig. 5.4-2, that the input voltage at which the gate makes its transition between logic levels is dependent

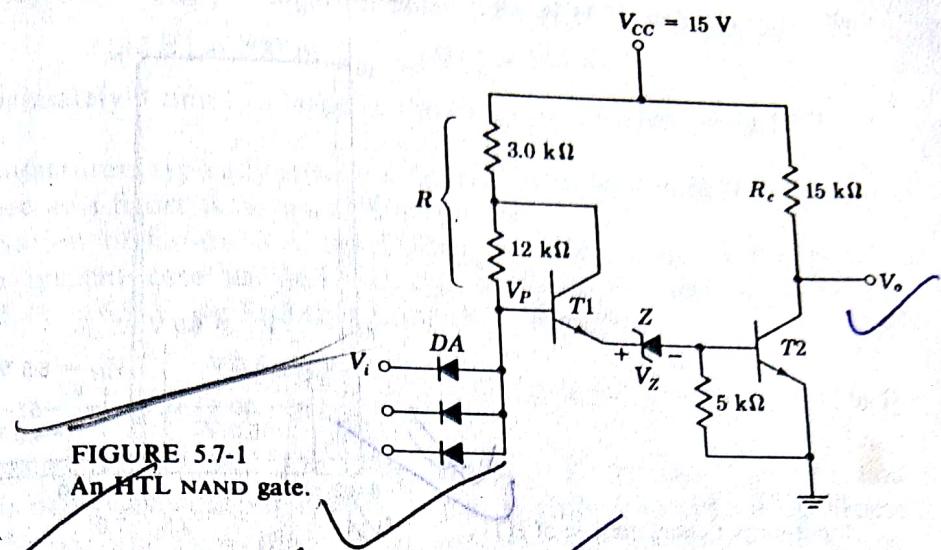


FIGURE 5.7-1
An HTL NAND gate.

on temperature. The temperature sensitivity of this voltage is equal to the temperature sensitivity of two diodes in series. For, in Fig. 5.4-1, since the input diode and the base-emitter junction of T_1 are in polarity opposition, the temperature sensitivities of these two junctions cancel. We are then left with the combined temperature sensitivities of D_2 and the base-emitter junction of T_2 . In the HTL gate of Fig. 5.7-1 the input diode and the junction of T_1 cancel, as before. But now we also have a cancellation of the temperature sensitivities of the zener diode and the junction in T_2 since the temperature sensitivities of these two are approximately equal and are also in opposite directions. The result is that the temperature sensitivity of the HTL gate is significantly less than that indicated in Fig. 5.4-2 for the DTL gate. We therefore ignore temperature effects.

~~5.8 INPUT-OUTPUT CHARACTERISTIC OF THE HTL GATE~~

The input voltage at which transistor T_2 begins to come out of cutoff is (see Prob. 5.8-1)

$$\begin{aligned} V_i &= V_{BE2} + V_z + V_{BE1} - V_{DA} \\ &= 0.65 + 6.9 + 0.7 - 0.75 = 7.5 \text{ V} \end{aligned} \quad (5.8-1)$$

The input voltage at which transistor T_2 is at the edge of saturation is (see Prob. 5.8-2)

$$\begin{aligned} V_i &= V_{BE2} + V_z + V_{BE1} - V_{DA} \\ &= 0.75 + 6.9 + 0.7 - 0.75 = 7.6 \end{aligned} \quad (5.8-2)$$

Using the results in Eqs. (5.8-1) and (5.8-2), we can draw the input-output characteristic shown in Fig. 5.8-1.

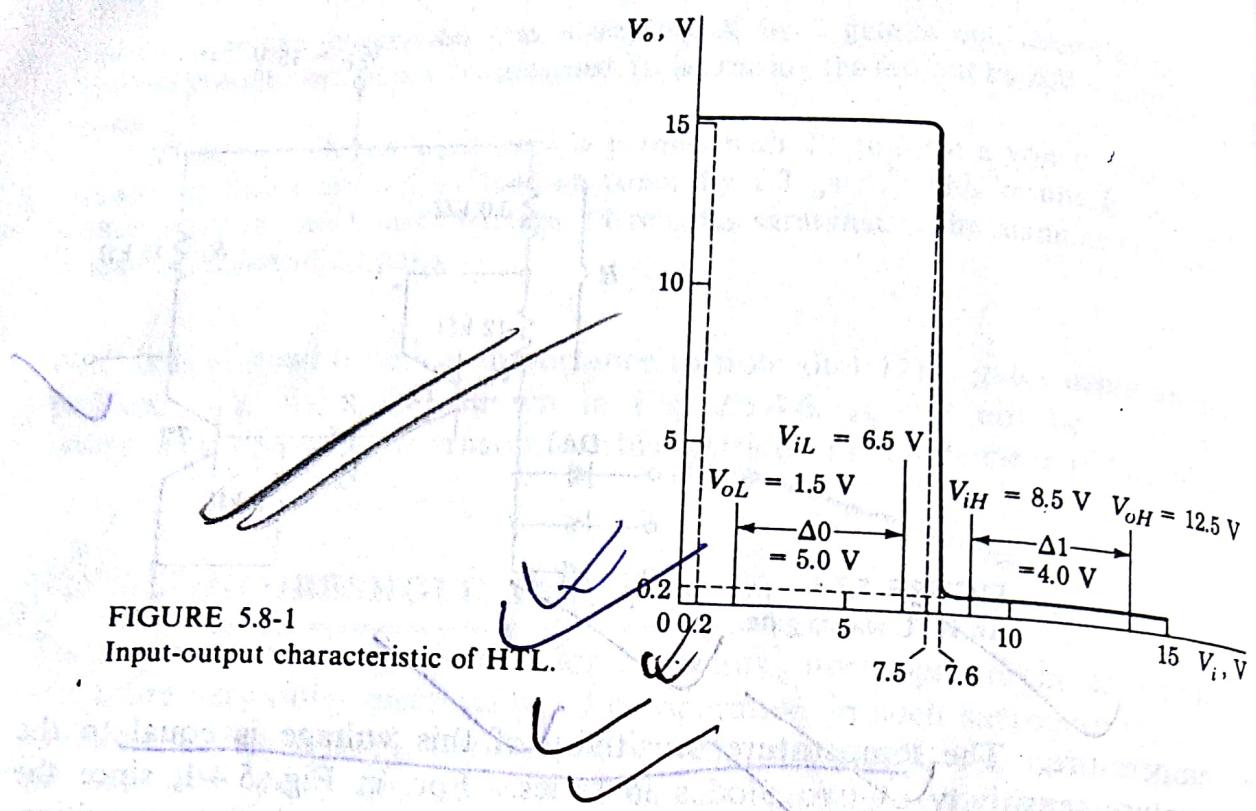


FIGURE 5.8-1
Input-output characteristic of HTL.

5.9 MANUFACTURER'S SPECIFICATIONS

Manufacturer's voltage specifications for HTL are typically

$$\begin{aligned} V_{iL} &= 6.5 \text{ V} & V_{oL} &= 1.5 \text{ V} & I_{oL} &= 12 \text{ mA} \\ V_{iH} &= 8.5 \text{ V} & V_{oH} &= 12.5 \text{ V} & I_{oH} &= -30 \mu\text{A} \end{aligned} \quad (5.9-1)$$

These voltages have been marked on the plot of Fig. 5.8-1. The voltage range V_{iL} to V_{iH} bridges the transition region rather symmetrically and leaves a reasonable margin of safety. The voltage $V_{oH} = 12.5 \text{ V}$ is also rather reasonable. For, with a $15\text{-k}\Omega$ pull-up resistor, as in Fig. 5.7-1, a leakage current in the output transistor of $100 \mu\text{A}$, and with $I_{oH} = -30 \mu\text{A}$, the output voltage of the gate is $V_o = V_{CC} - 15 \times 10^3 \times (130 \times 10^{-6})$. Letting $V_{CC} = 14 \text{ V}$ (the manufacturer assumes that V_{CC} can vary by $\pm 1 \text{ V}$ from the nominal value of 15 V), we have $V_o = 12 \text{ V}$, which is actually somewhat less than the value of V_{oH} given.

The voltage $V_{oL} = 1.5 \text{ V}$ seems artificially high. The manufacturer states that even if 12 mA enters the output transistor $T2$ from an outside source, $V_o \leq 1.5 \text{ V}$. Presumably, if a gate is operating properly, the output transistor should be in saturation and the gate output should be 0.2 or at most, 0.4 V (see Fig. 1.10-1). This value of V_{oL} is specified, we may surmise, to make the noise immunities Δ_1 and Δ_0 more nearly comparable. For we find that the noise margins Δ_1 and Δ_0 are

$$\Delta_1 = V_{oH} - V_{iH} = 12.5 - 8.5 = 4.0 \text{ V} \quad (5.9-2)$$

and

$$\Delta_0 = V_{iL} - V_{oL} = 6.5 - 1.5 = 5.0 \text{ V} \quad (5.9-3)$$

Propagation delay time The propagation delay time of HTL gates is typically

$$t_{pd}(LH) = 200 \text{ ns} \quad t_{pd}(HL) = 100 \text{ ns}$$

which is approximately 3 times as large as the delay found when using DTL.

Fan-out Manufacturers typically specify a fan-out of 10 for the HTL gate. As we shall now see, this figure is, as usual, conservative.

The derivation of fan-out for the DTL gate which leads to Eq. (5.3-7) applies to the present case as well. Using, in the derivation $V_{cc} = 15 \text{ V}$, $R = 15 \text{ k}\Omega$ and $V_z = 6.9 \text{ V}$, we find that Eq. (5.3-7) becomes

$$N = \frac{0.5\sigma h_{FE}}{\rho + (1 - \rho)/(h_{FE} + 1)} - 0.07R \times 10^{-3} \quad (5.9-4)$$

In the HTL gate, $\rho = 0.2$, so that $N \approx 2.5\sigma h_{FE}$. If we use $h_{FE} = 50$ and $\sigma = 0.85$, which brings the output transistor just slightly into saturation, where $V_{CE}(\text{sat}) = 0.2 \text{ V}$, we find $N = 106$. If we require that the output transistor be driven well into saturation [$\sigma = 0.1$, $V_{CE}(\text{sat}) = 0.1 \text{ V}$], we find $N \approx 12$. Thus, $N = 10$ seems conservative yet reasonable.

REFERENCES

- 1 Bohn, R., and R. Seeds: Collector Tap Improves Logic Gating, *Electronic Design*, August 3, 1964, pp. 51-55.