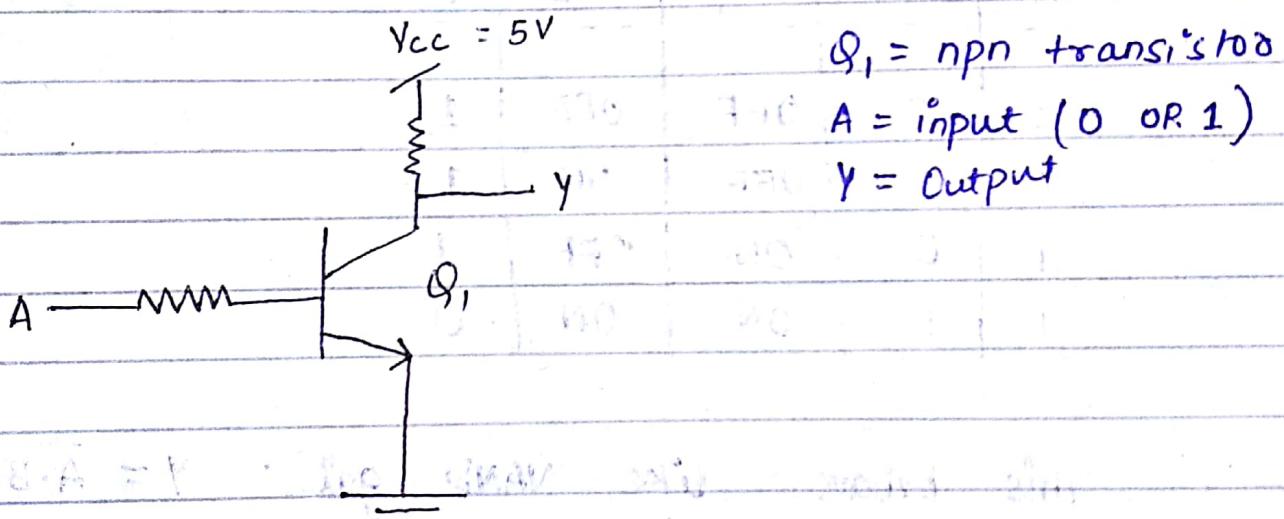


## Logic Family

### 1. RTL : Resistor Transistor Logic



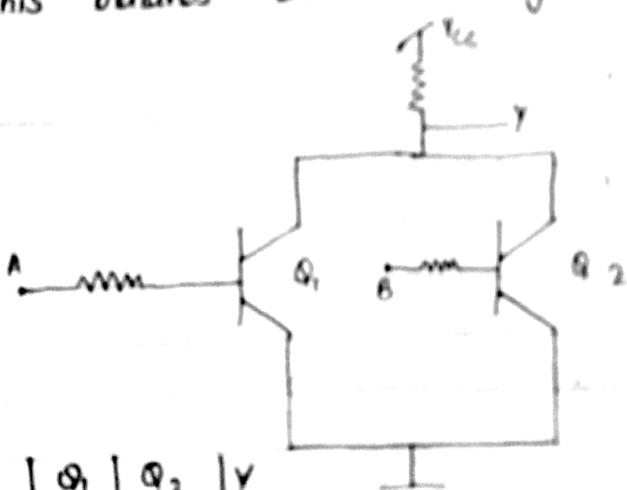
$A$	$Q_1$	$y$
0	OFF	1
1	ON	0

This circuit behave like NOT gate or inverted circuit.



A	B	$Q_1$	$Q_2$	Y
0	0	OFF	OFF	1
0	1	OFF	ON	1
1	0	ON	OFF	1
1	1	ON	ON	0

This behaves like NAND gate  $Y = \overline{A \cdot B}$



A	B	$Q_1$	$Q_2$	Y
0	0	OFF	OFF	1
0	1	OFF	ON	0
1	0	ON	OFF	0
1	1	ON	ON	0

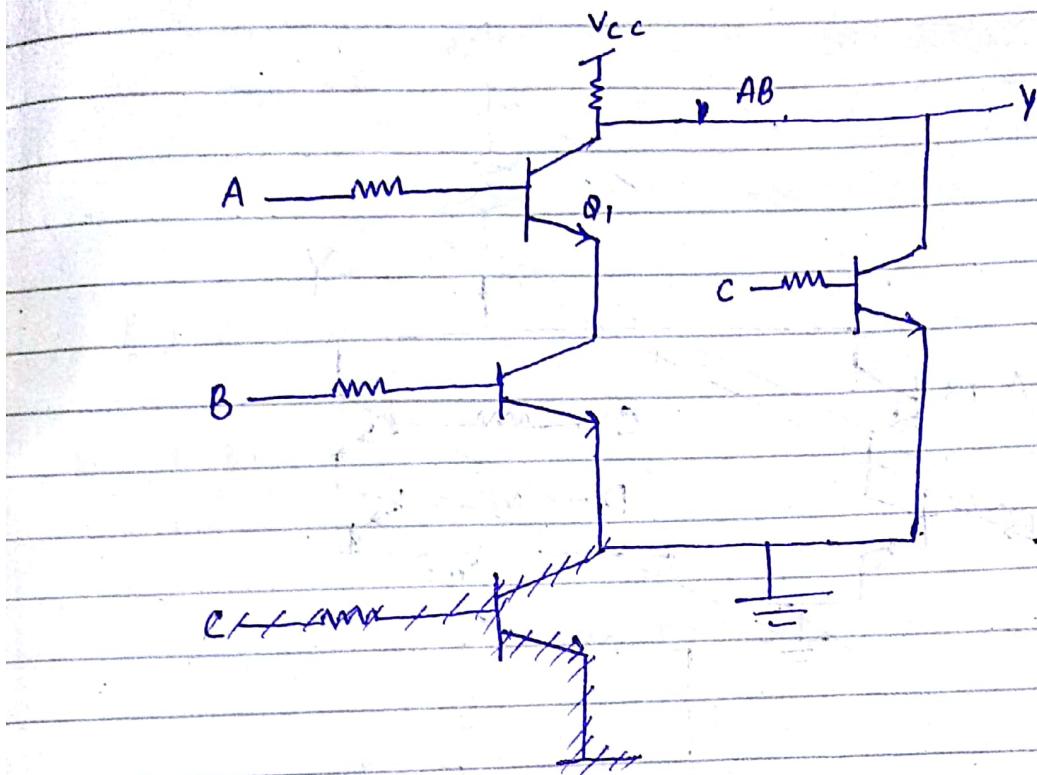
This circuit will behave like NOR gate

$$Y = \overline{A + B}$$

Series :  $A \cdot B \cdot \dots \cdot x_n$

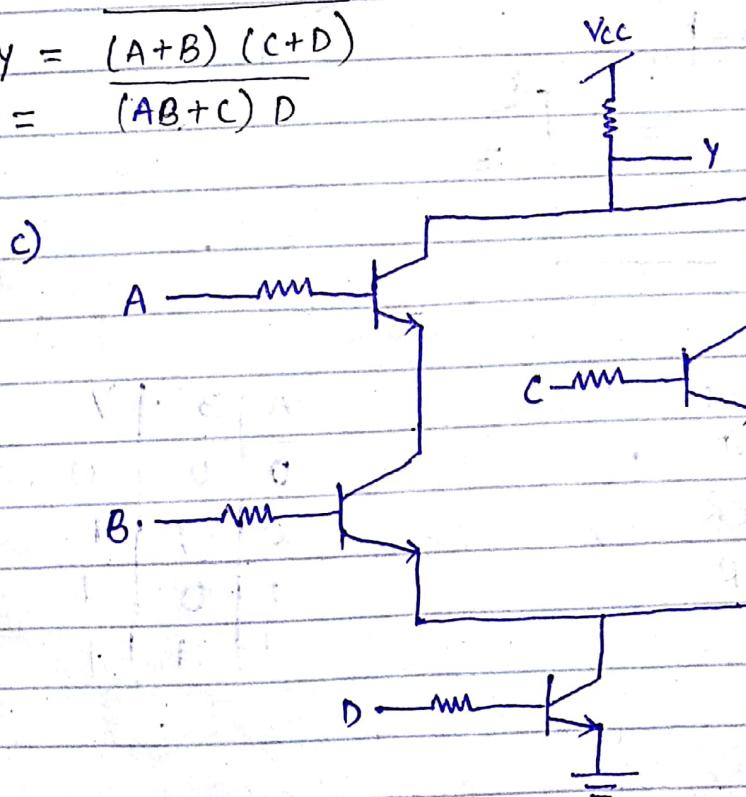
parallel:  $A + B + \dots + x_n$

1. Draw the circuit if a)  $y = \overline{AB} + C$   
=  $\overline{AB} \cdot \overline{C}$



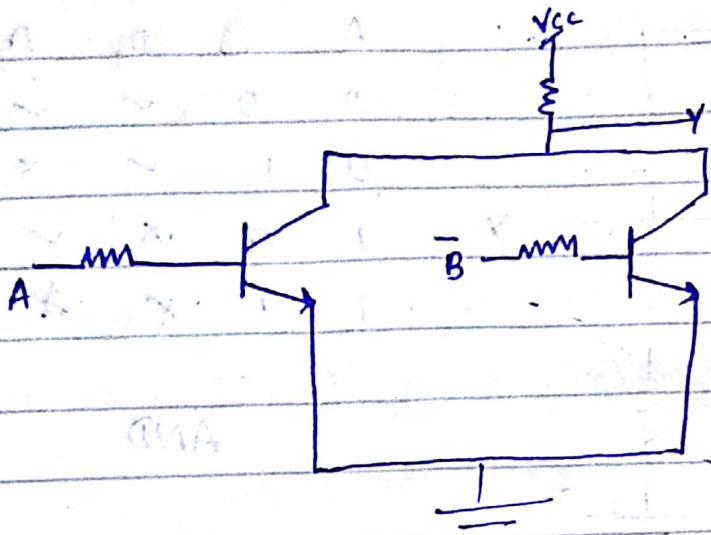
b)  $y = \overline{(A+B)}(C+D)$

c)  $y = \overline{(AB+C)}D$

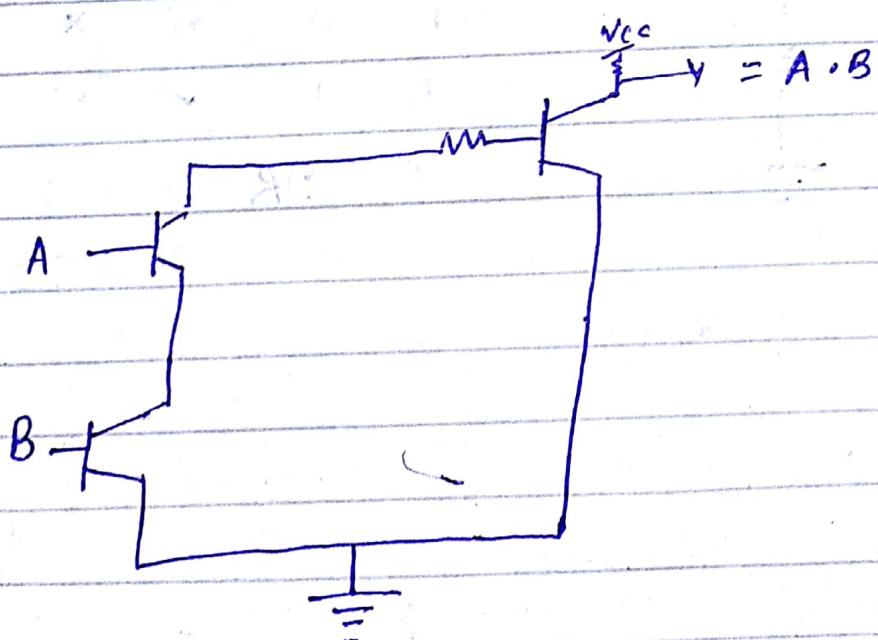
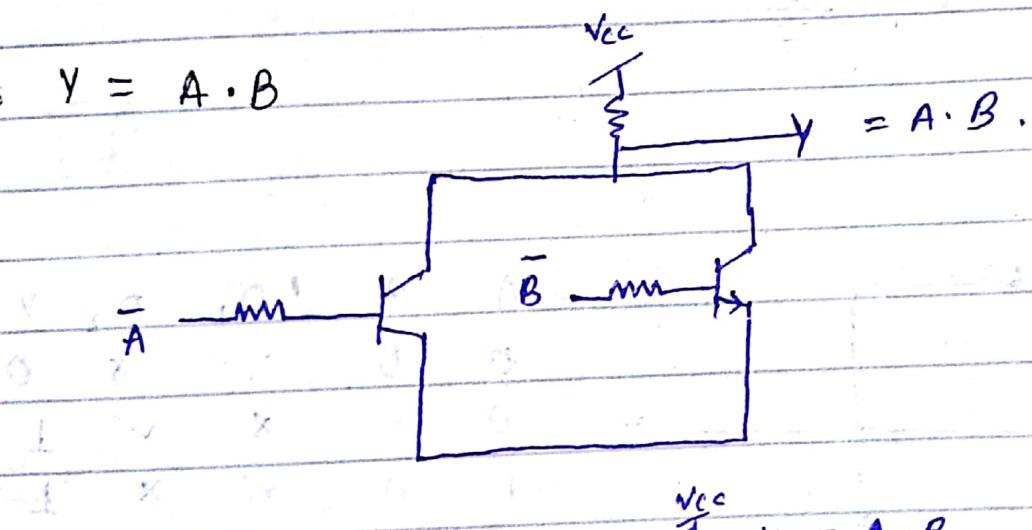


$$2. \quad Y = \bar{A}B$$

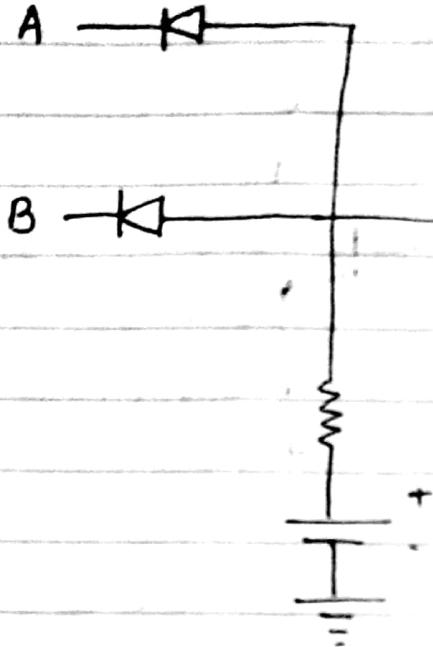
$$\bar{Y} = \cdot \overline{\bar{A}B} = \bar{\bar{A}} + \bar{B} = A + \bar{B}$$



$$3. \quad Y = A \cdot B$$

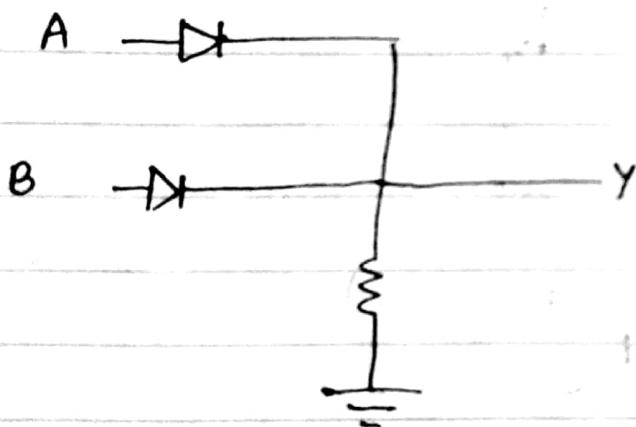


# Diode Logic



A	B	D <sub>1</sub>	D <sub>2</sub>	Y
0	0	✓	✓	0
0	1	✓	✗	0
1	0	✗	✓	0
1	1	✗	✗	1

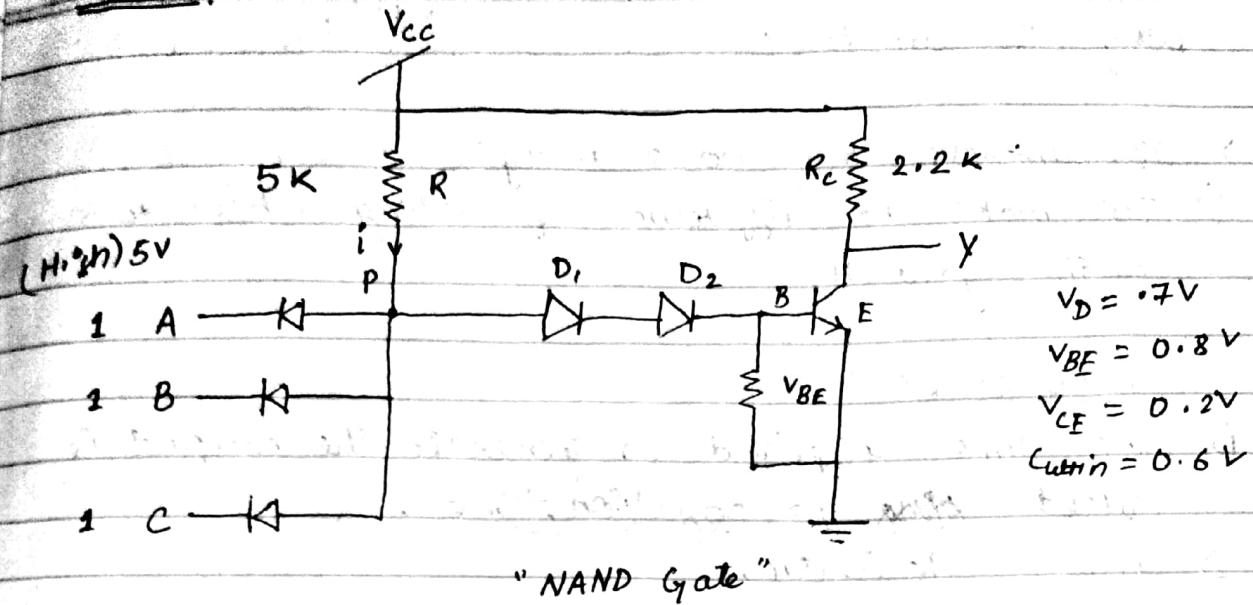
AND



A	B	D <sub>1</sub>	D <sub>2</sub>	Y
0	0	✗	✗	0
0	1	✗	✓	1
1	0	✓	✗	1
1	1	✓	✓	1

OR

## DTL. (Diode transistor).



Noise immunity feature is very low in diode.  
 " " " high in DTL

$$V_{D1} = 0.7 \text{ V} \quad \text{Minimum voltage required}$$

$$(0.7 + 0.7 + 0.8) \text{ V} = \text{to ON the transistor}$$

$$V_p = 2.2 \text{ V}.$$

H High

$$I = \frac{V_{cc} - V_p}{5k}$$

$$= \frac{5 - 2.2}{5k} = \frac{2.8}{5k} = 0.56 \times 10^{-3}$$

$$= 0.56 \text{ mA}$$

$$V_{CE} = V_o = 0.2 \text{ V.}$$

H low, the  $V_o = 0.2$

$$V_p = 2.2$$

$$V_o = 5 \text{ V} \approx 5 \text{ V.}$$

$$\begin{aligned} A + B &= 0.2 + 0.7 = 0.9 \\ &= 0.2 + 0.7 \end{aligned}$$

Why Two diode ??

→ ~~Two diodes~~

- 1) To improve the noise margin.
- 2) To make the difference of voltage b/w two path greater.

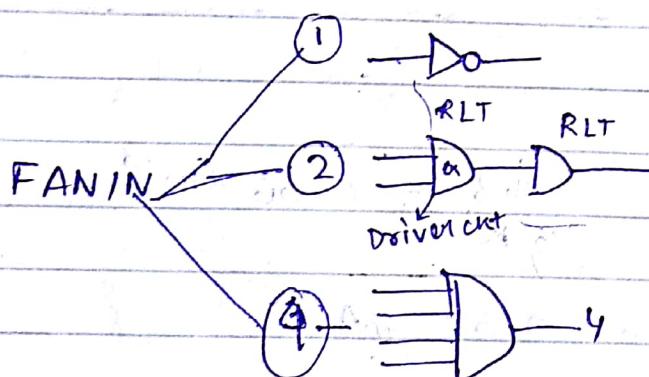
Parameters :

- 1) The time required to generate the output is called ~~time~~ propagation time.
- 2) Power decipation:

FAN IN and FAN OUT

The no. of similar gates which can be driven by a gate.

FAN IN:



(Maximum, it can hold)

No number of logic gate can be connected at the output of any logic gate

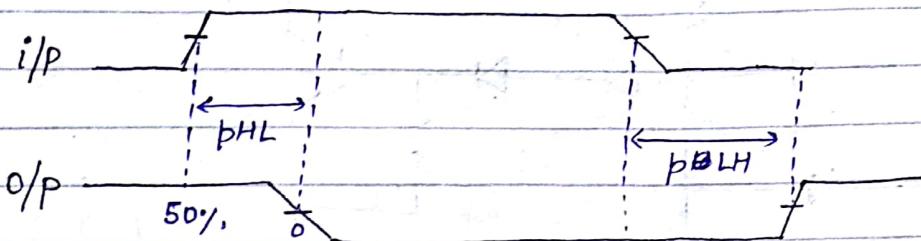
160 mA = Total current / output

16 mA = Each load current.

$$\text{Fan out} = \frac{160 \text{ mA}}{16 \text{ mA}} = 10$$

The propagation delay or speed of operation.

The speed of a digital ckt is specify in term of propagation time. The I/O waveform of logic gates are shown in Fig. A. The delay times are measured b/w the 50% voltage level of input and output waveform.



Power dissipation.

This is the amount of power dissipated in an IC. Determined by the current  $I_{cc}$  i.e. drawn from  $V_{cc}$ . And given by,  $V_{cc} \times I_{cc}$

Figure of merit

Figure of merit = Propagation delay time \* Power

The unit of figure of merit is picosecond (ps). Propagation delay is measured in nanosecond (ns). Power dissipation milliwatt (mW).

Bipolar : BJT (Bipolar devices)

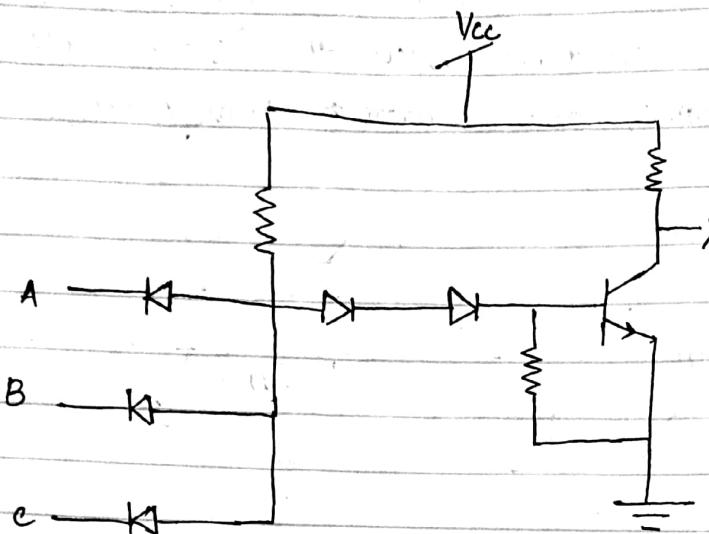
Unipolar : N-MOS, P-MOSFET, CMOS

Bipolar → Saturated  
→ Unsaturated

The saturated bipolar logic families are :

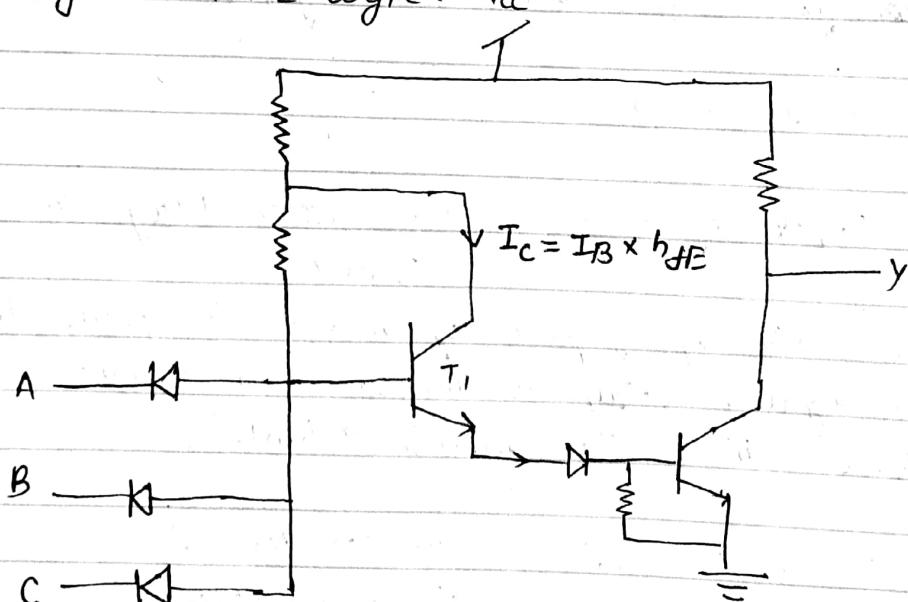
RTL, DCTL, IIL, DTL, HTL, TTL

Bipolar logic families are : ECL, SchotTKy TTL  
(Emitter coupled logic)



$$h_{FE} = \frac{I_C}{I_B} \quad I_C = I_B \times h_{FE}$$

Modified DTL logic: Vcc

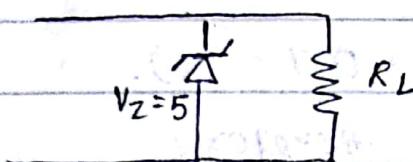


In Modified DTL logic,

Fan Out is better than DTL logic.

## HTL (High threshold logic) (High Power devices)

Due to presence of electric motto, all ON-OFF control CKT ~~are~~ and high voltage switch in an industrial ~~department~~ environment, the noise level is quite high and logic families like DTL, RTL and diode family are not perform properly.

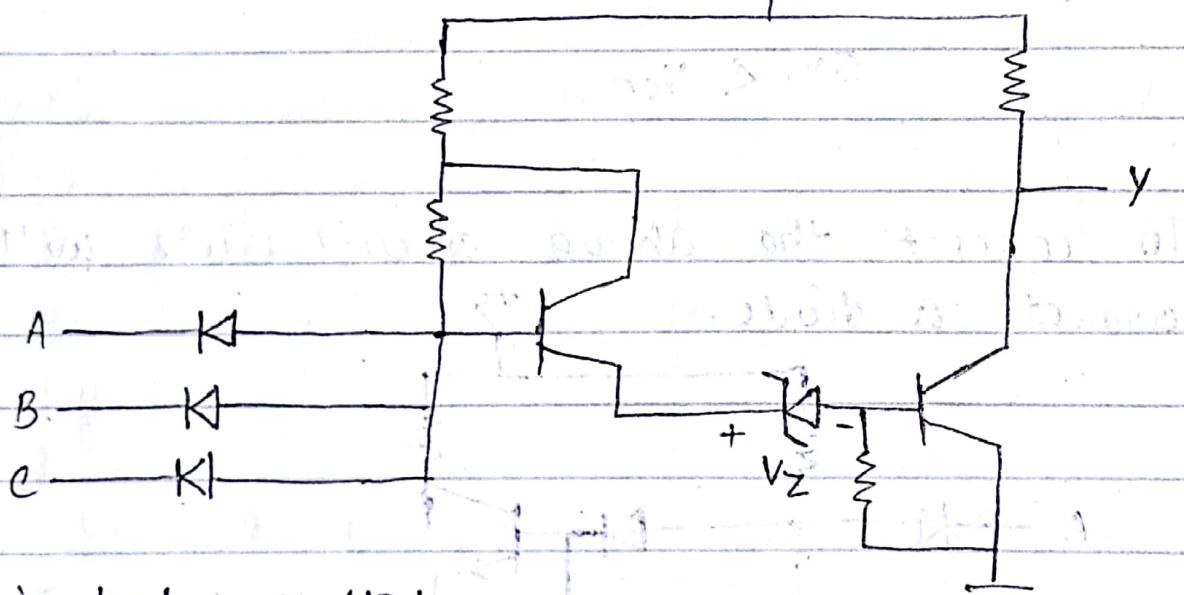


First,

$$V_{in} < 5 \text{ V}$$

$$V_{in} > 5 \text{ V}$$

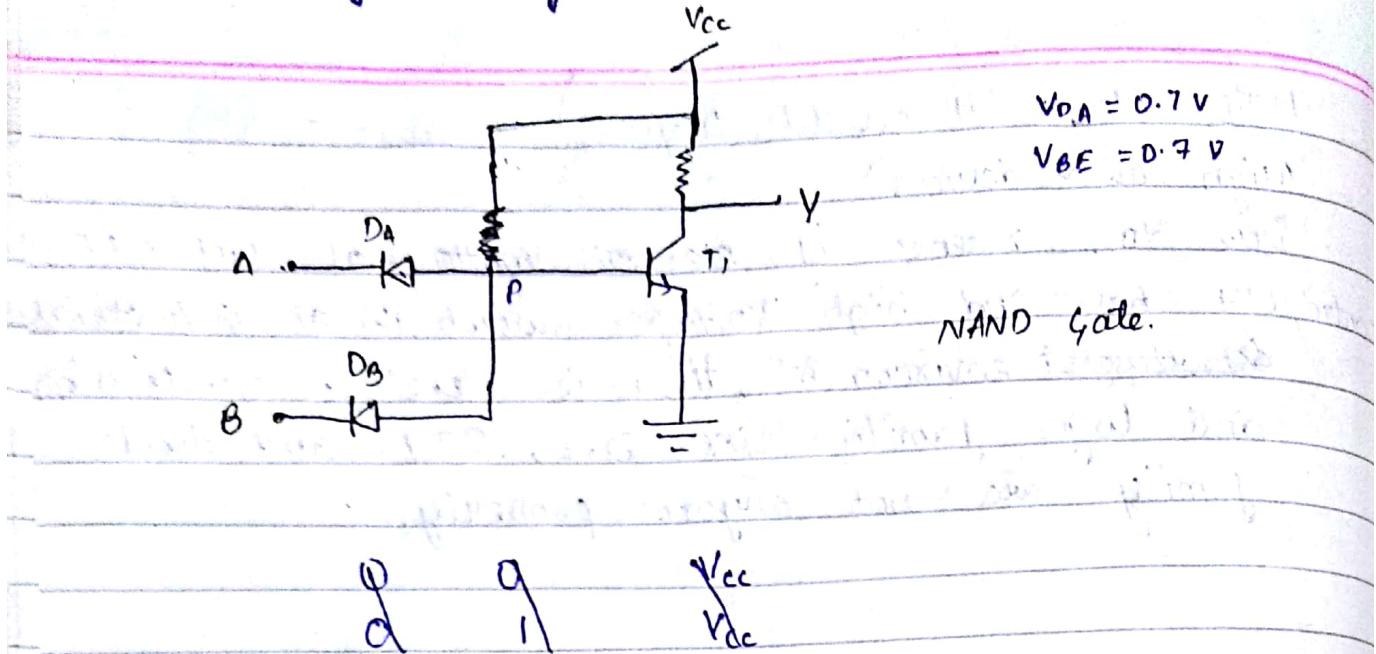
Then the voltage across  $R_L$  is 5V



Disadvantage of HTL

1. The propagation delay time is affected due to large resistance value.

Practically wrong Ideally correct.



At Low voltage (0.2)

At pt. p. Voltage drop =  $0.2 + 0.7 = 0.9$ .

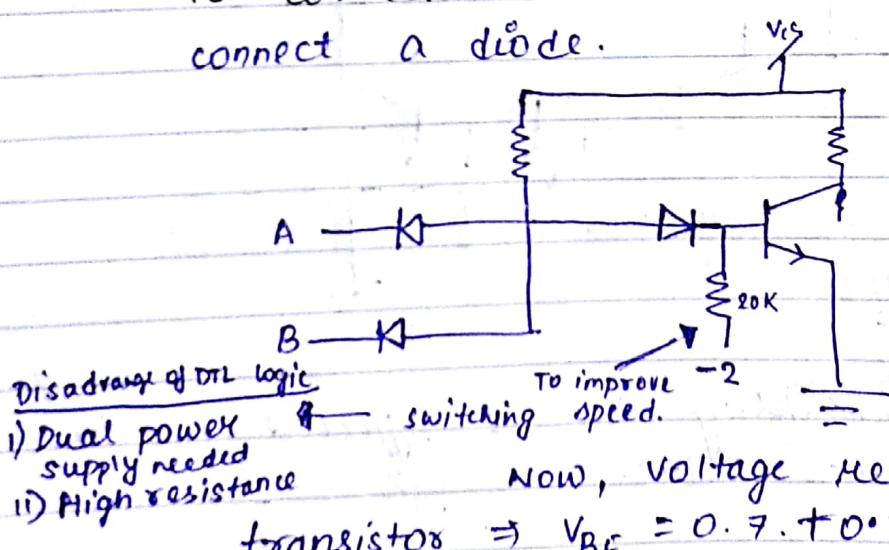
which is always  $> 0.7$  therefore

$T_I$  is always ON. and it will give  $V_{CE} = 0V$ .

At high voltage

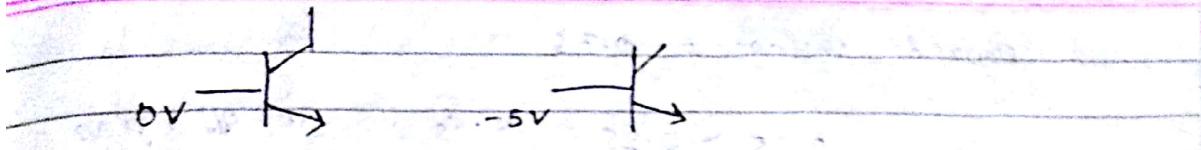
$$5V < V_{CE}$$

To correct the above circuit : We will connect a diode.



- i) Dual power supply needed
- ii) High resistance

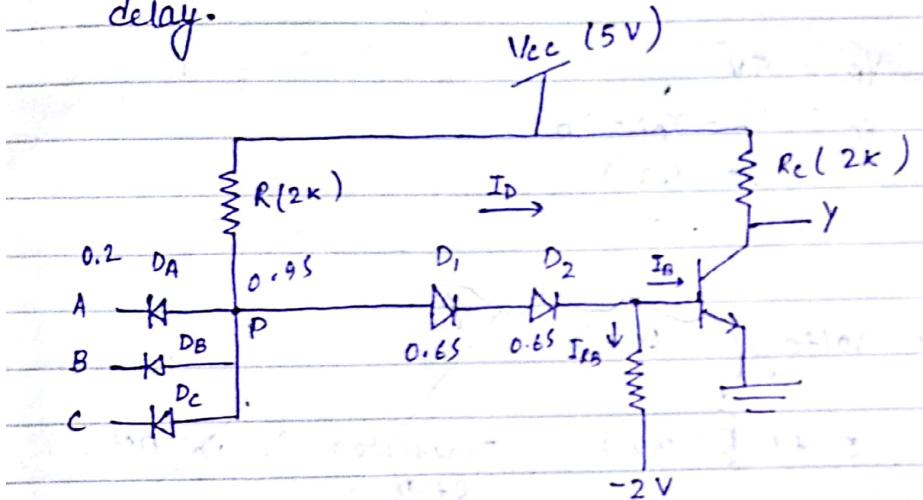
NOW, voltage req. to ON the transistors  $\Rightarrow V_{BE} = 0.7 + 0.7 = 1.4$



-5V will take less time and will be faster.

The propagation delay of DTL circuit

The propagation delay in DTL's gate are of the order of 30 - 80 ns (nanosecond). The turn OFF delay is generally larger than turn ON delay.



Find out the output voltage when inputs are

- 0
- 1

i) The voltage drop across the diode is 0.65 V

$$\text{Value of } V_{CE} = 0.2$$

$$\text{Value of } V_{BE} = 0.75 \text{ V}$$

$$V_{DA} = V_{BB} = 0.75$$

$$V_P = 0.2 + 0.75 + 0.65 = 1.60 \text{ V}$$

At low  $V_{OI}$ ,

$$V_P = 0.2 + 0.75 \text{ V} = 0.95 \text{ V}$$

$$\begin{aligned} (\text{Base terminal voltage}) \quad V_B &= V_P - V_{D1} - V_{D2} \\ &= 0.95 - 0.65 - 0.65 \\ &= -0.35 \text{ V} \end{aligned}$$

2.3  
0.65  
1.95  
0.6  
2.55

Required Voltage = 0.75

$0.75 > 0.35$  It is in cut-off region  
or off state.

$$I_{RB} = \frac{-0.35 + 2}{20k}$$

$$= 0.08 \text{ mA}$$

output :  $v_{cc}$

A high voltage,

$$V_p = 5V$$

$$\begin{aligned} v_o &= V_p - V_{D1} - V_{D2} \\ &= 5 - 1.3 \\ &= 3.7 \end{aligned}$$

Required Voltage = 0.75

$$0.75 < 3.7$$

Transistor is in ON state.

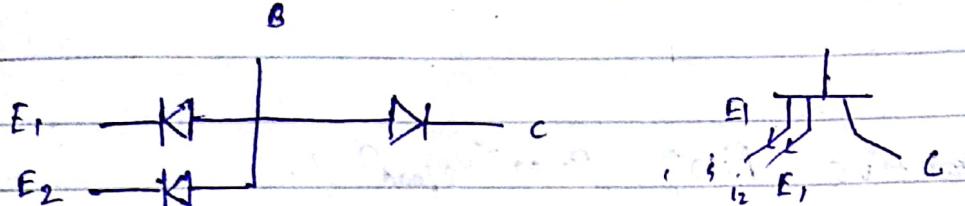
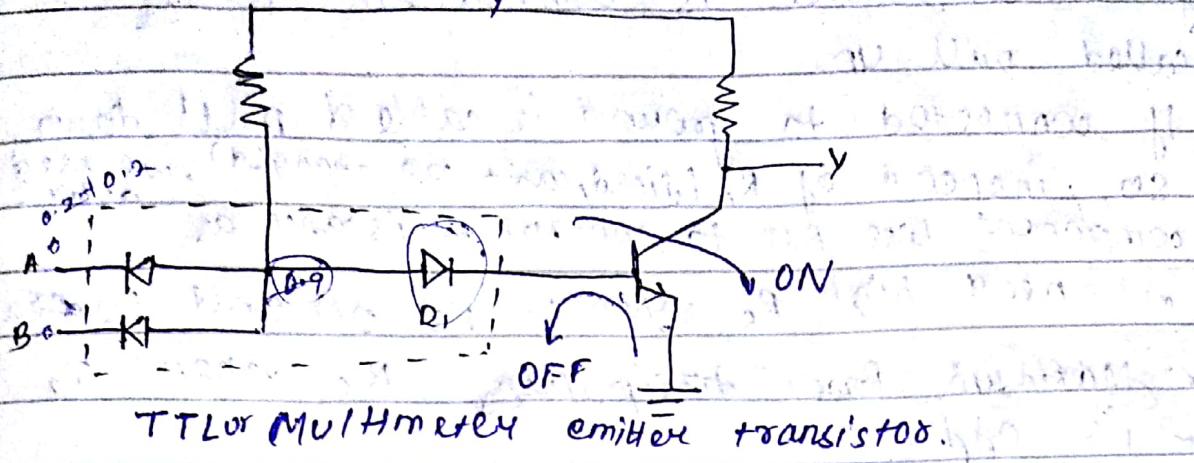
$$I_{RB} = \frac{3.7 + 2}{20k}$$

$$\begin{aligned} &= \frac{5.7}{20,000} = 0.28 \text{ mA} \\ &= 0.00028 \text{ A} \\ &= 0.28 \text{ mA} \end{aligned}$$

$$I_{RB} = \frac{0.75 + 2}{20k} = 0.14 \text{ mA}$$

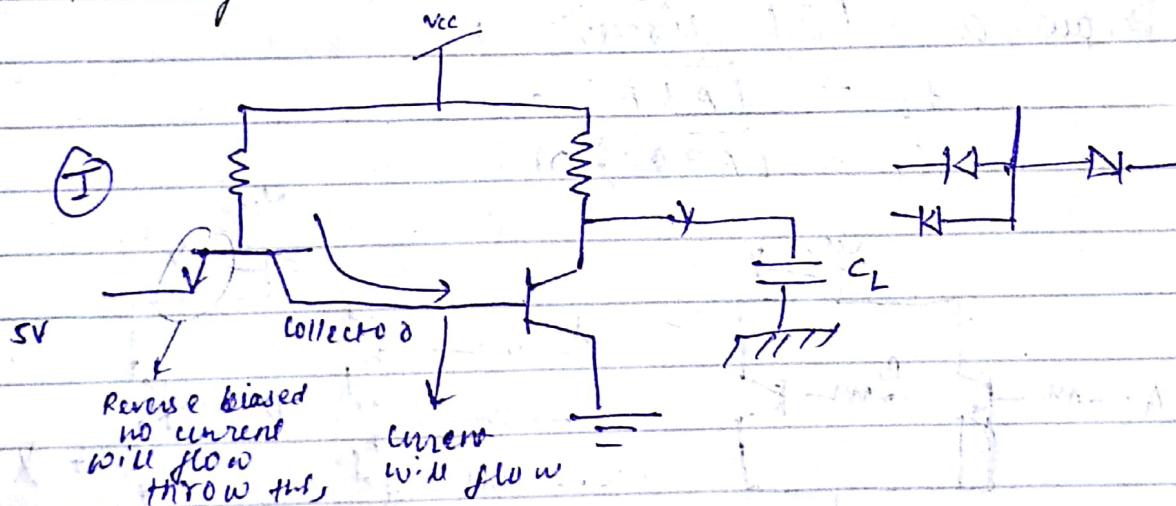
$$I_D = \frac{V_{cc} - V_p}{R} = \frac{5 - 2.05}{2k} \approx 0.14 \text{ mA}$$

$$I_B = I_D - I_{RB} = 0.26 \text{ mA}$$



Transistor ON = Collector current = Emitter

Reversely active transistor



From ①; when  $T_1$  is high  $T_2$  is reversely active transistor.

From ②,  $C_L$  is from load,  $\tau = R_C C_L$

If  $R_C$  is reduced,  $I_C$  increases rapidly and  $T_2$  cannot work properly in saturation mode

Need to reduce  $R_C$ , so  $C_1$  is fixed.

~~Transistor~~



If a compound is connected to  $V_{CE}$  it is called pull up.

If connected to ground is called pull down so, instead of  $R_C$  (fixed, can't be changed), we used active component like BJT to control resistance as we need high  $R_C$  when  $T_2$  is ON and low  $R_C$  when  $T_2$  is OFF.

~~Maximize power dissipation~~  $R_C$  when  $T_2$  is OFF.

why active. Not Passive load??

Bcz we cannot change the value of resistance but active we can modify the resistance.

1. Draw a RTL circuit :

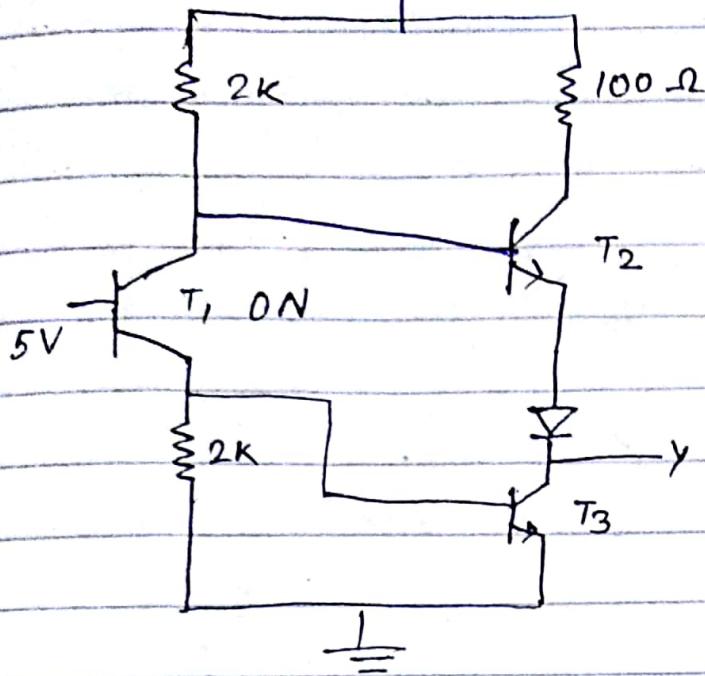
$$f_L = (A + B) C$$

$$f_L = \overline{(AB \bullet C \bullet D)}$$

$V_{CE}$

$V_{CE}$

$T_Y$



← Adv. of DTL

i) Improve charging / discharging

ii) Improve power dissipation

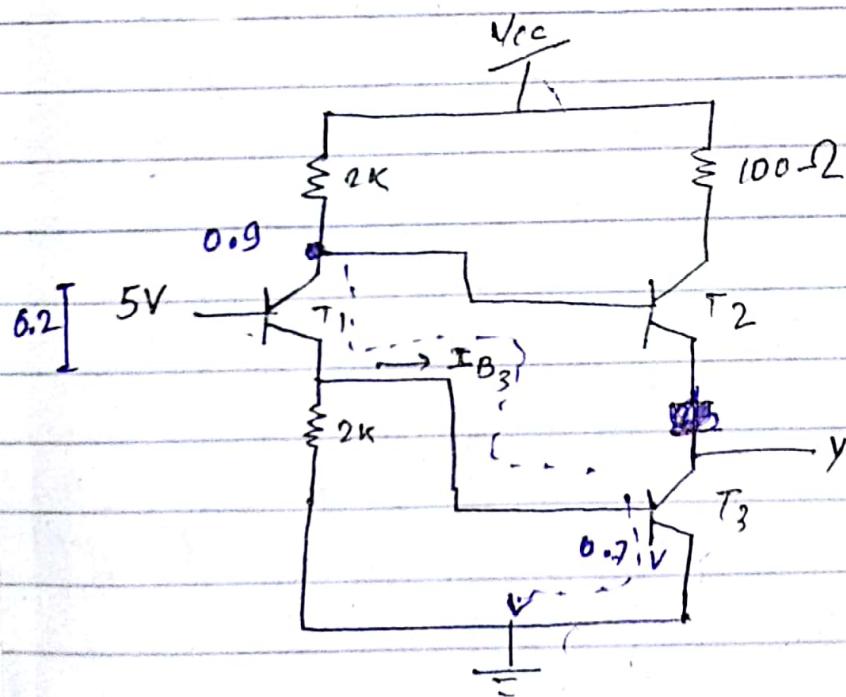
iii) Propagation time improve.

iv) speed improvement

v) size reduce, performance increase,

	T <sub>1</sub>	T <sub>2</sub>	T <sub>3</sub>	y
5V	ON	OFF	ON	0 (0.2V)
0.2V	OFF	ON	OFF	$1 \left( 5 - V_{CE} - 0.75 = 4.01V \right)$ $(0.2)$

T<sub>1</sub> is called face-splitter g-to-en-poh network

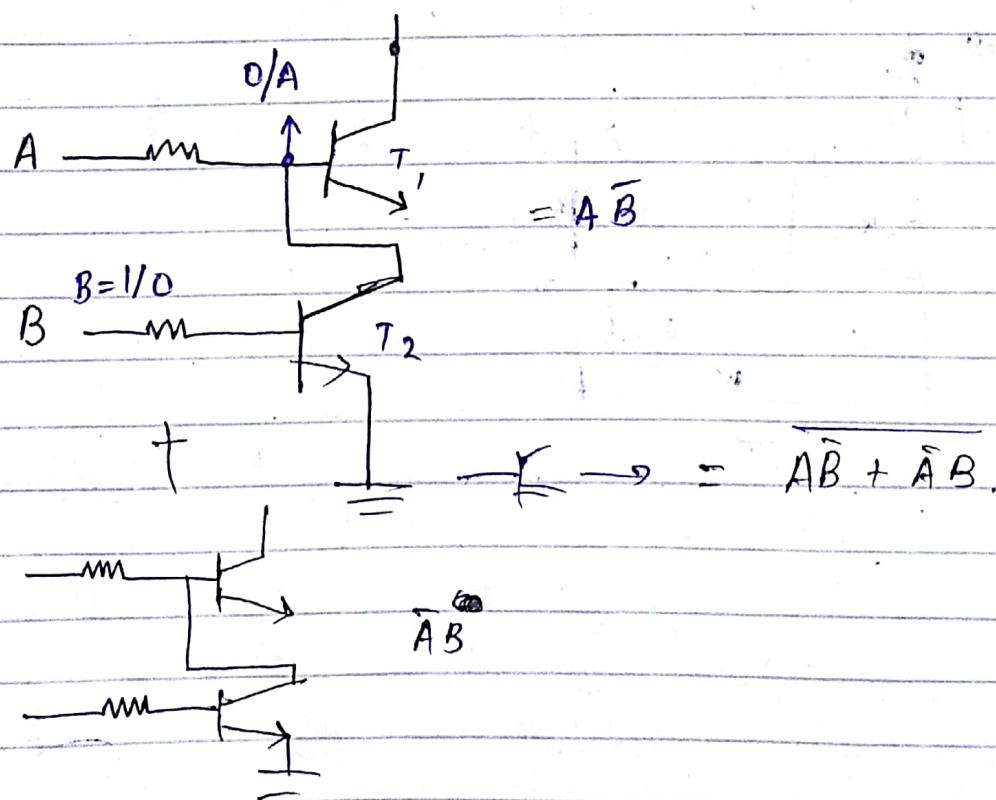
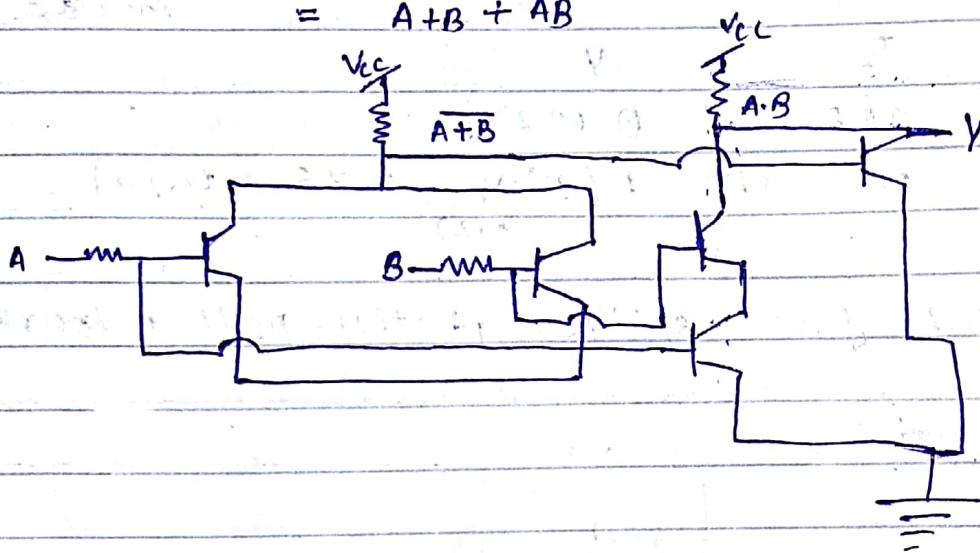


V.V.I. //

Design using RTL logic family with minimum number of transistors.  $Y = \overline{AB} + \overline{A}\overline{B}$  (XOR gate)

$$Y = \overline{AB} + \overline{A}\overline{B}$$
  
 ~~$= (\overline{A} + B)(\overline{A} + \overline{B})$~~   
 $= (A + \overline{B})(\overline{A} + B)$

$$Y = \overline{\overline{AB} + A\overline{B}} \quad (\text{XOR})$$
  
 $= \overline{\overline{AB} + AB}$   
 $= \overline{A + B + AB}$



## Disadvantage of RTL

- 1) No. of Resistances is more
- 2) Area. A

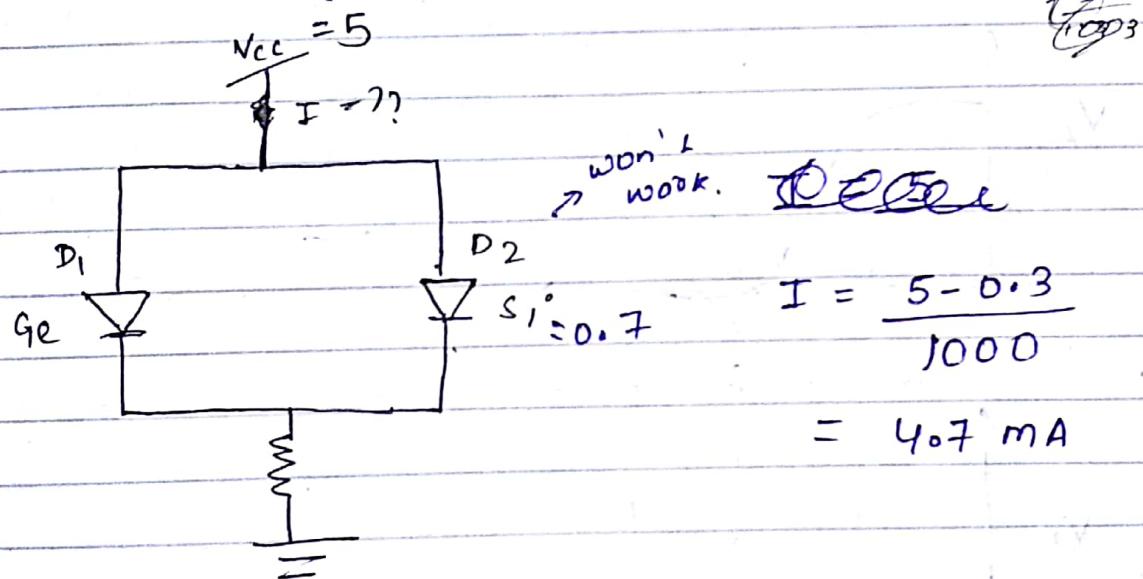
DCTL (Direct Coupling Transistor logic)

Disadvantage:

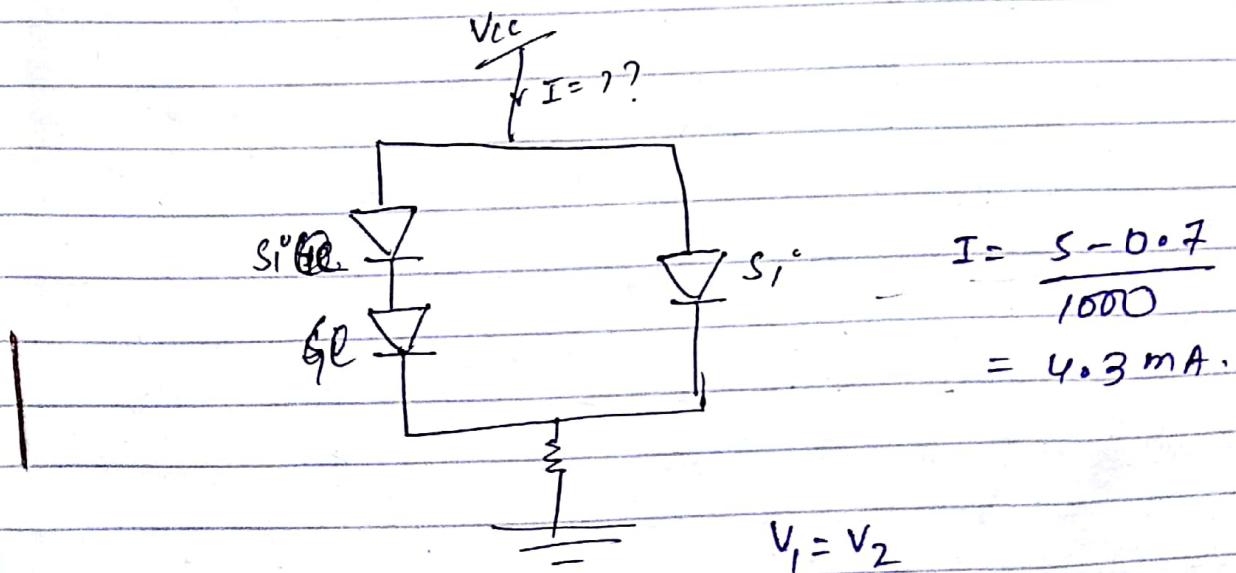
- 1) Problem of current hogging problem  
not properly distributed.

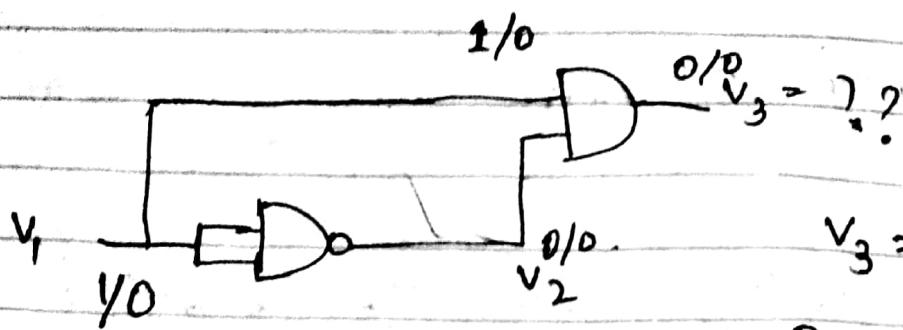
Advantage:

- 1) less resistor
- 2) less area.



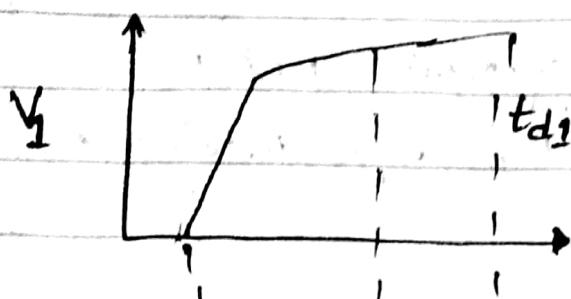
If two voltage source in parallel,  
~~total voltage drop~~  $V_1 = 0.3$  and  $V_2 = 0.7$ .



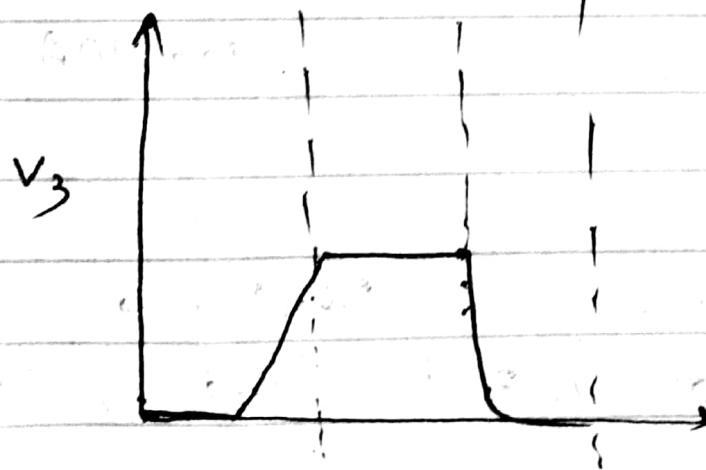
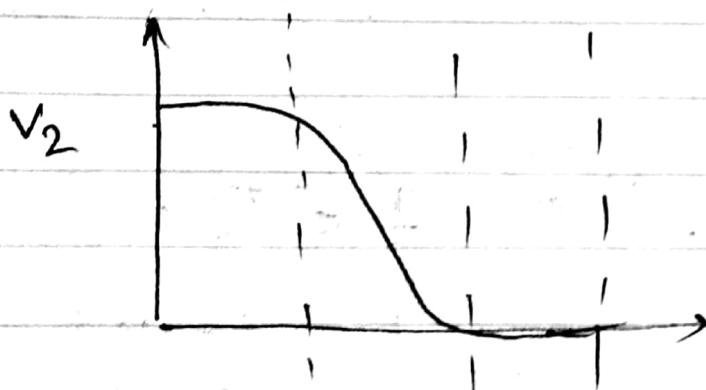


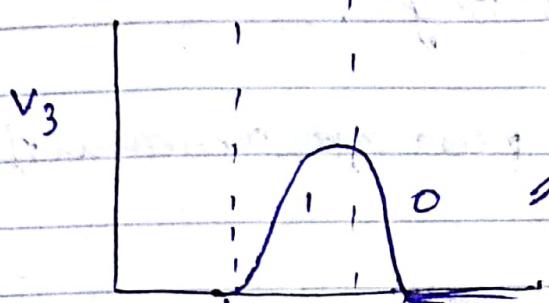
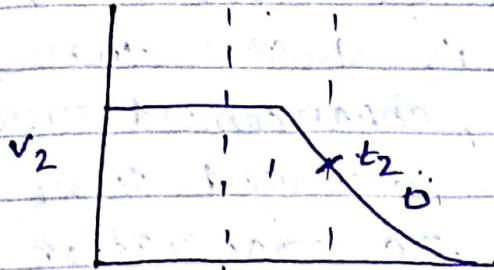
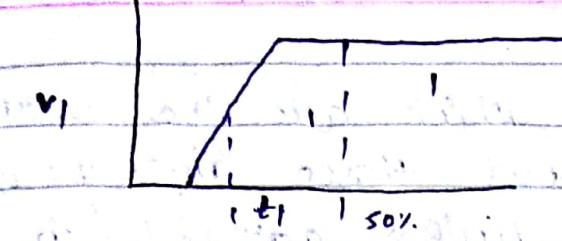
$$v_3 = 0.$$

Propagation delay .



Draw the waveform of  $v_2$  and  $v_3$ .



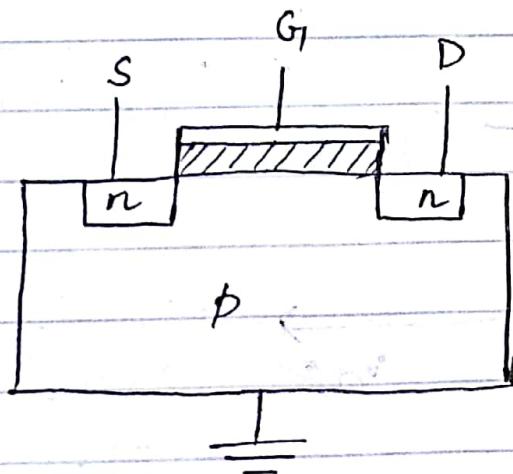


For cascading ckt  
disadvantages

- 1) Noise will be there
- 2) Time delay is going to add
- 3).

Imp Propogation delay  
Hazard

### n - MOS



~~enhancement~~ type is ~~more~~ more better than Depletion enhancement.

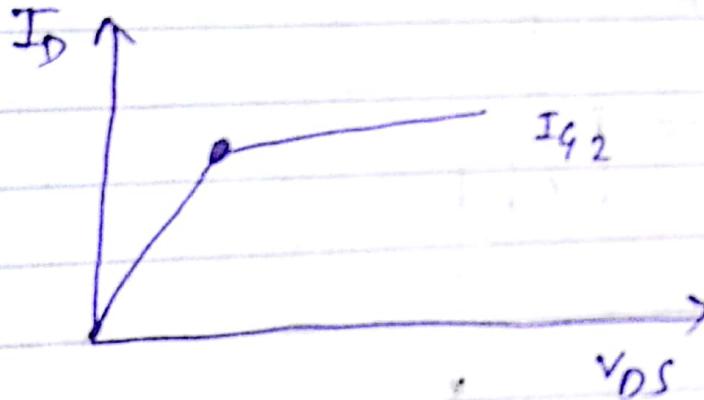
### Dis adv of Depletion

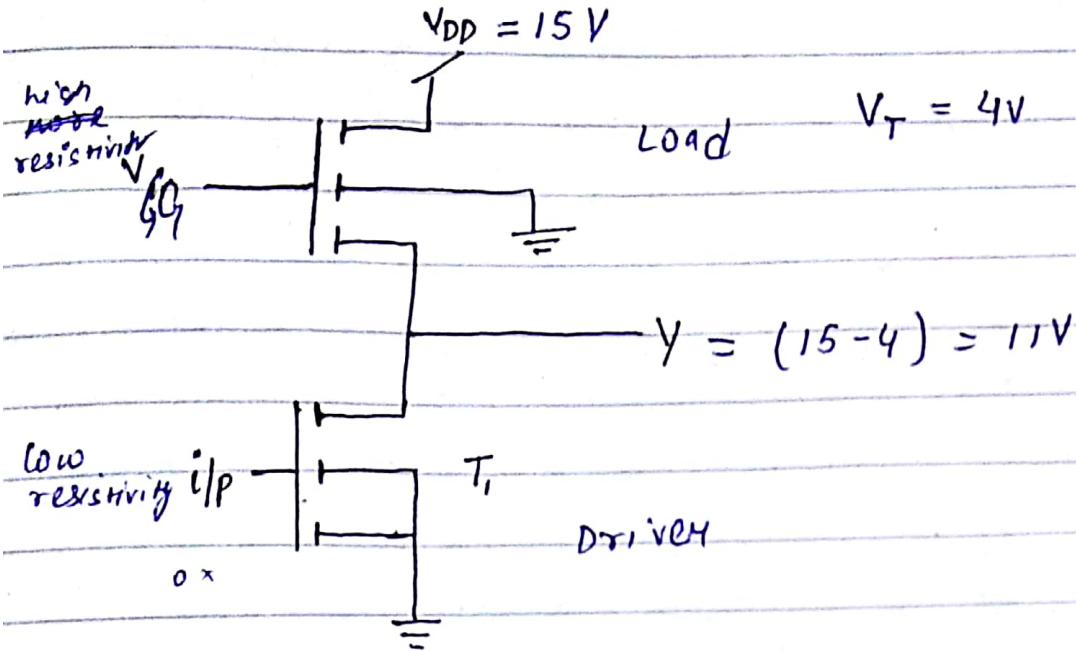
- 1) At OV, p depletion also works. ~~no connection b/w source and drain.~~

- 1) The mobility of e's which are the carriers in an n-MOS is about three times greater than the mobility of holes carrier in p-MOS. Hence, n-MOS is faster than p-MOS.
- 2) The digital circuit using enhancement mode transistors is generally preferred since it is a great convenience that the transistor be cutoff at 0 gate voltage.

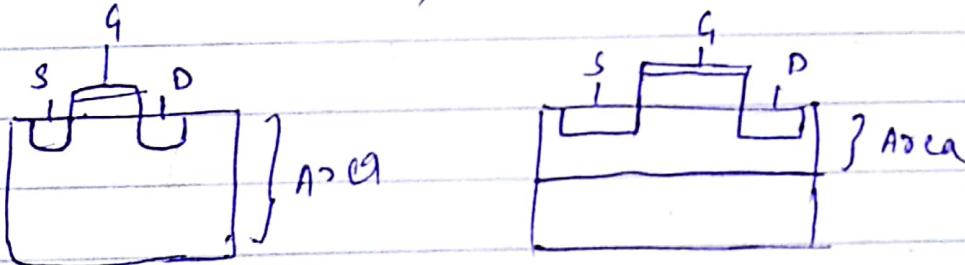
gate current almost ~~plus~~ picamper

when both regions are overlapped the region is pinch-off. After that we get constant current.





~~If resistance is low~~  
channel less, more conductivity.



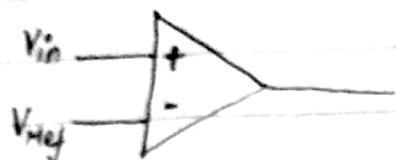
conductivity fast  
Resistivity decreases

- 1) The Driver transistors should have relatively high conductance while load should have low conductance.
- 2) In the bipolar trans. switch ckt, use of load resistance of order of some thousands of ohm but for the MOSFETs Switch ckt's, load resistance will be off many  $10 \times 10^3$  of ohms even upto  $100k\Omega$

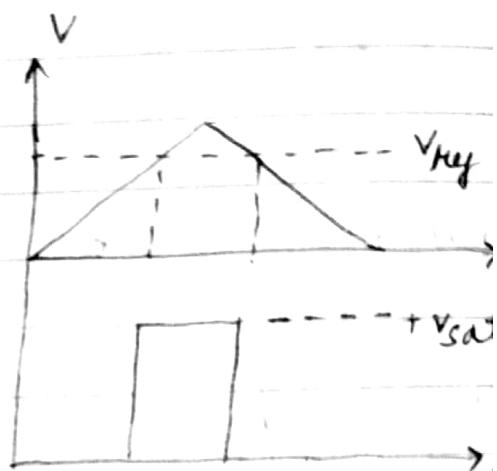
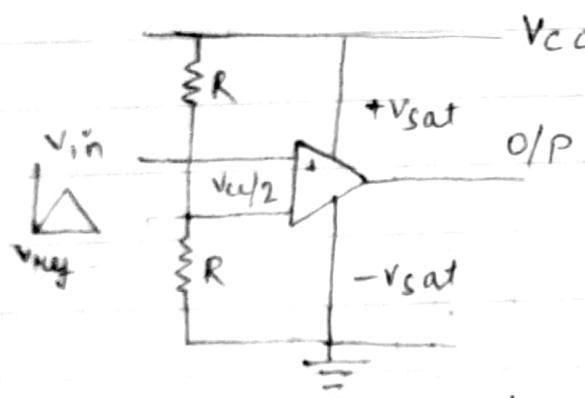
# comparator Circuit

## 1) Non-Inverting

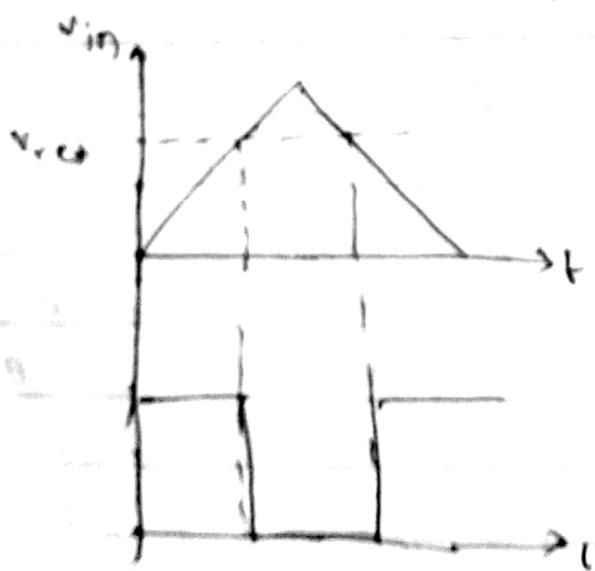
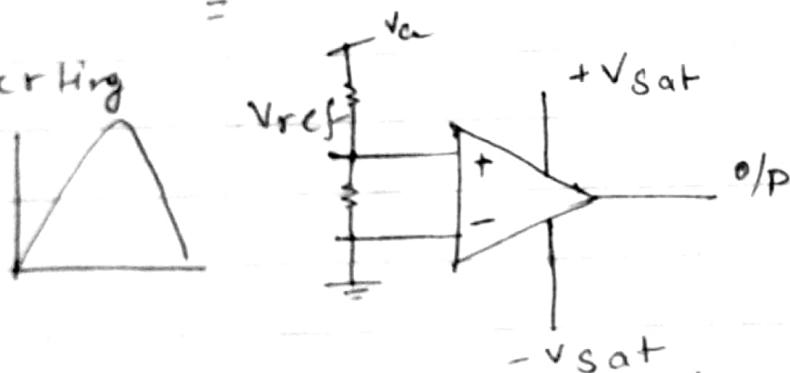
homework

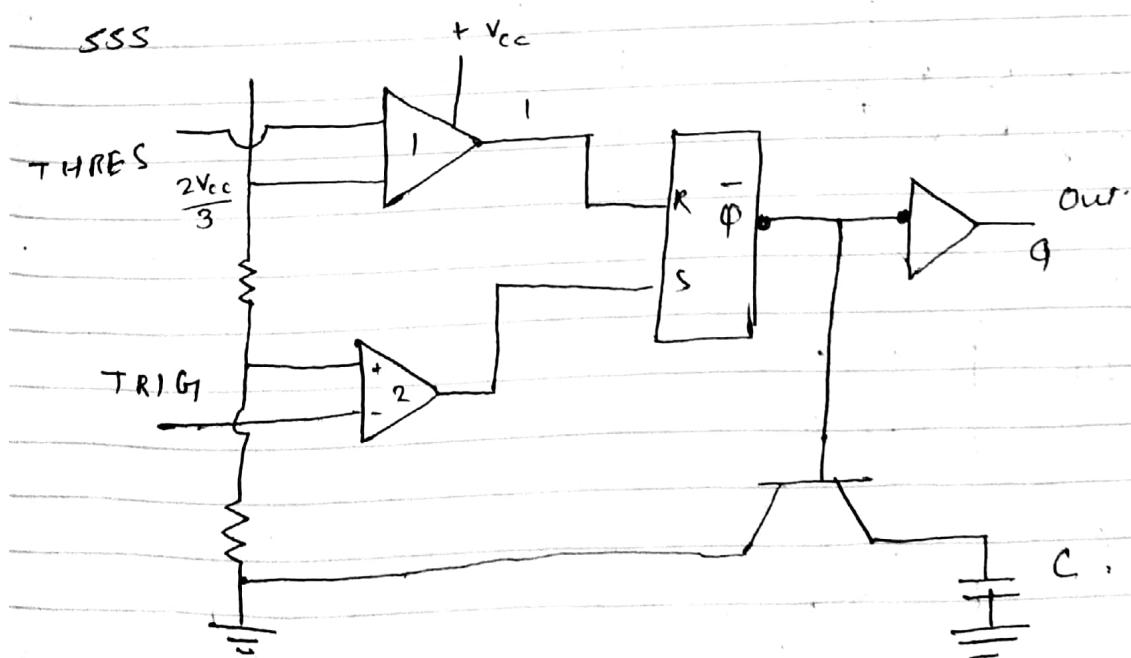
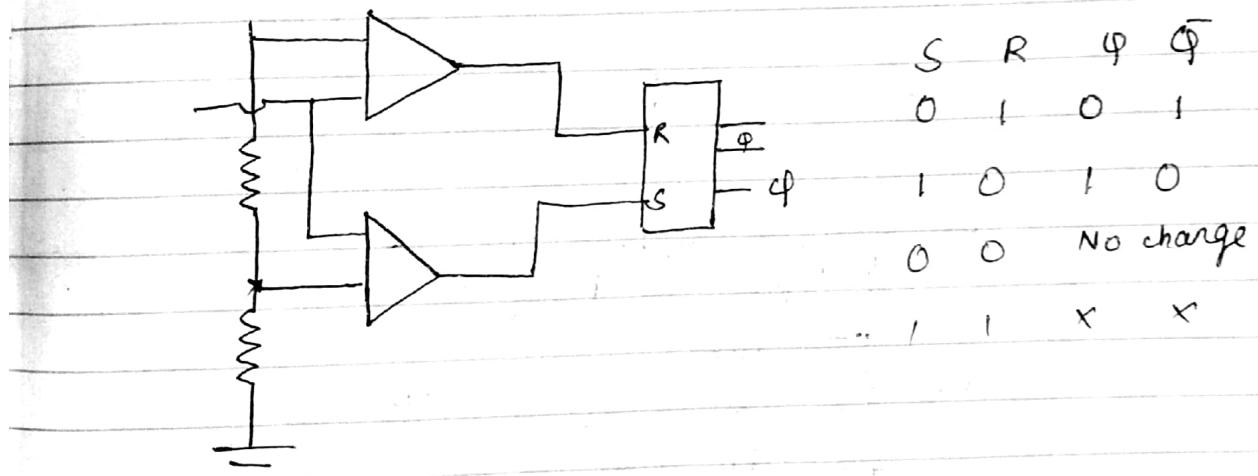
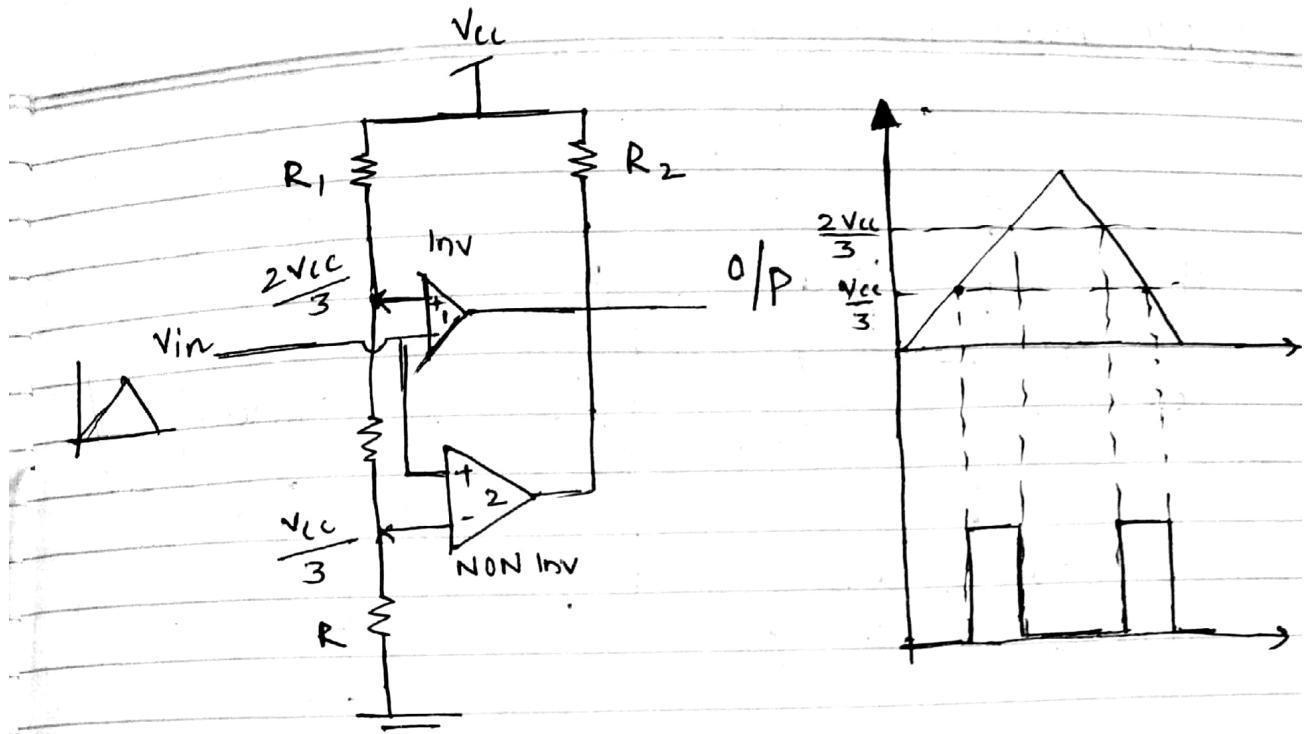


(-)ve terminal = Inverting  
(+)ve terminal = Non Inverting

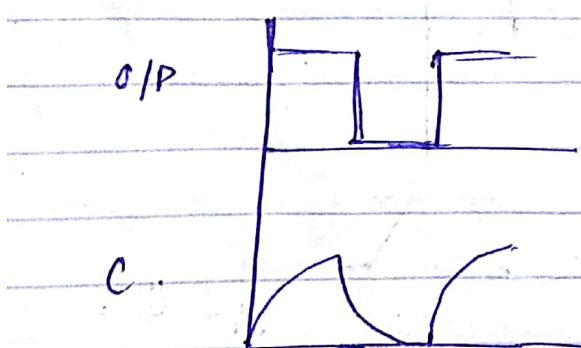
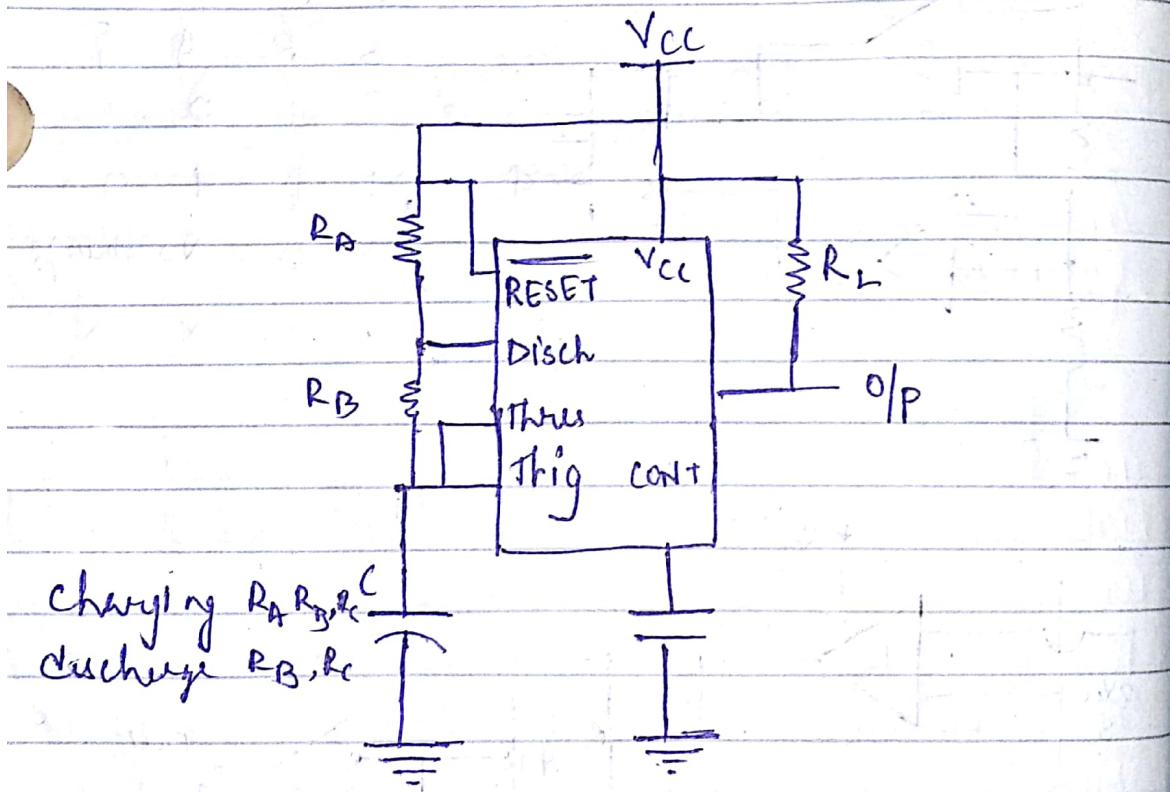
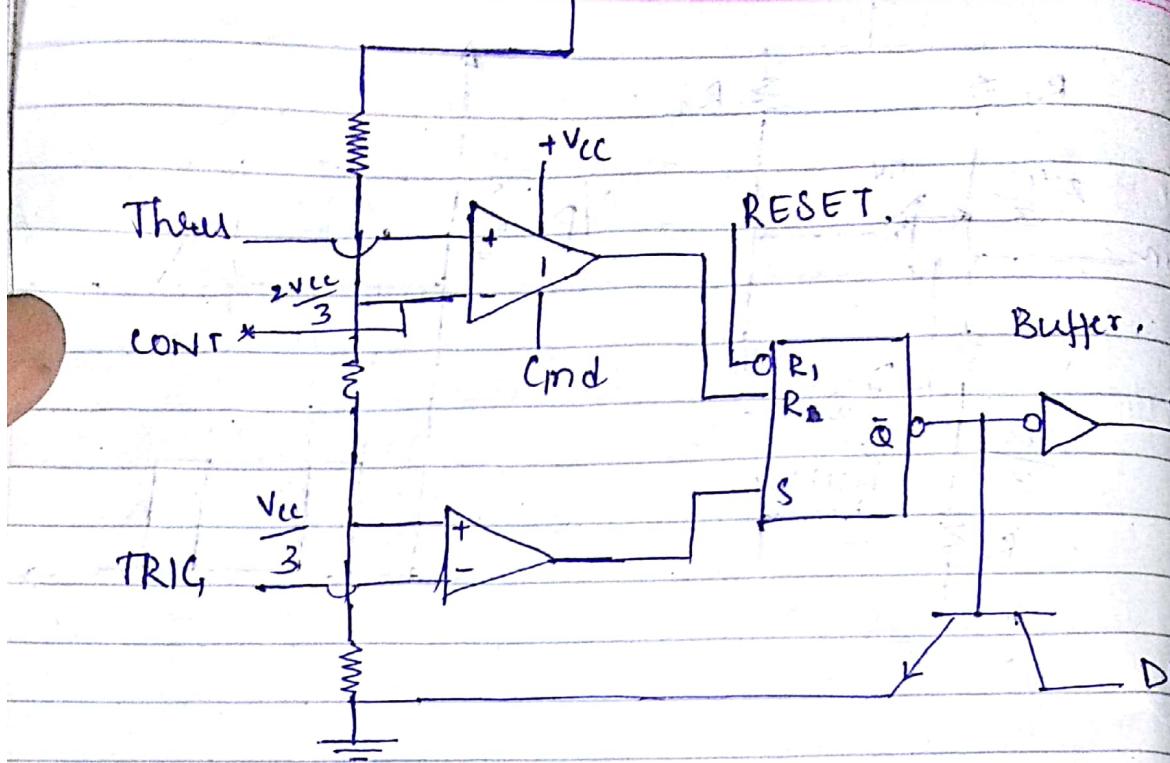


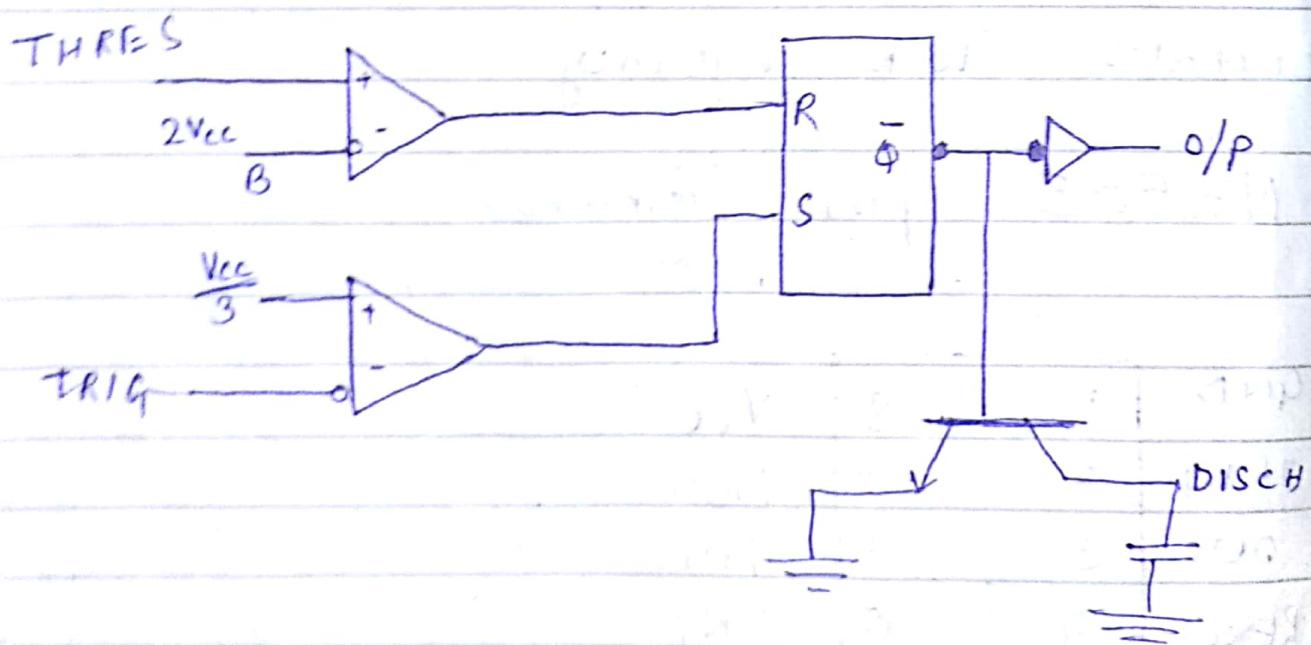
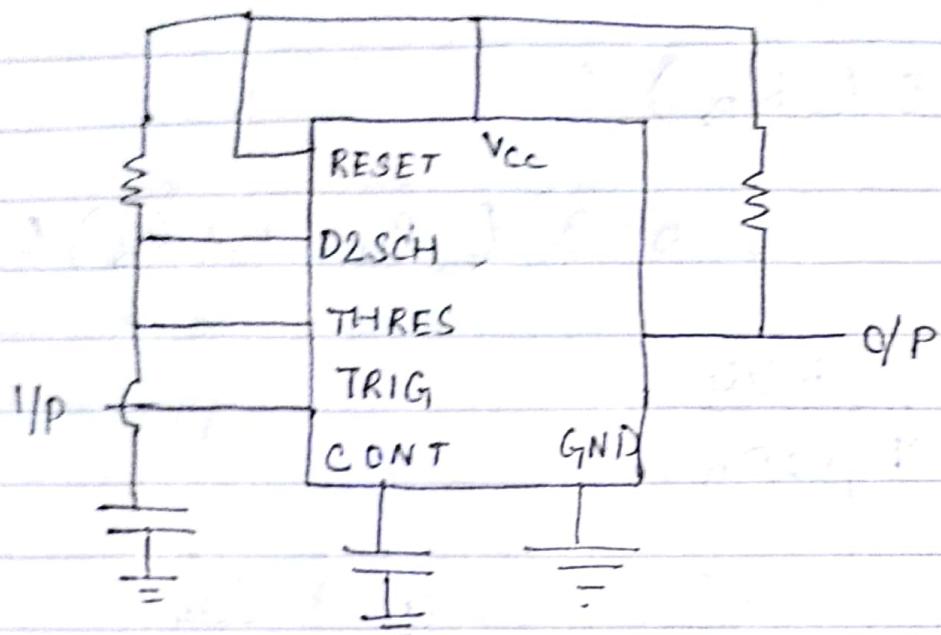
inverting

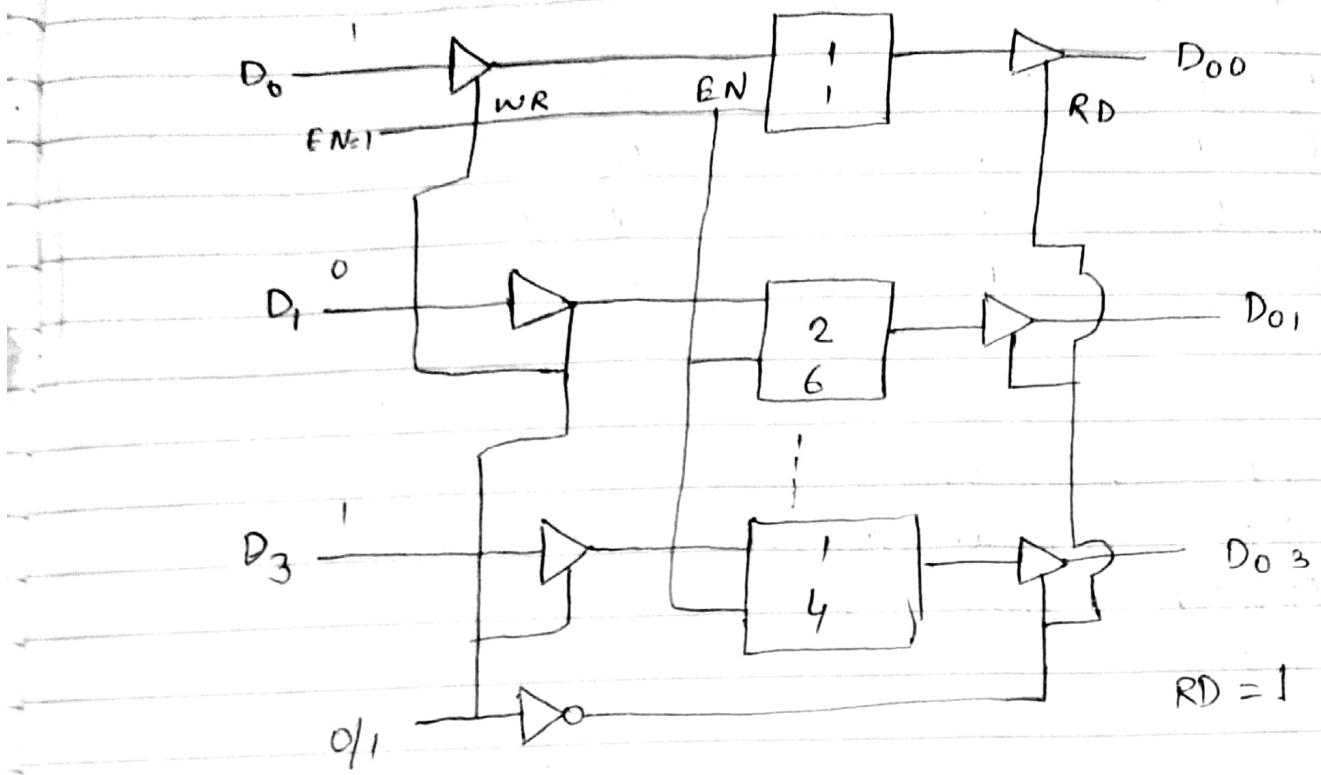




# Astable multivibrator V<sub>cc</sub>







$$T = 1s$$

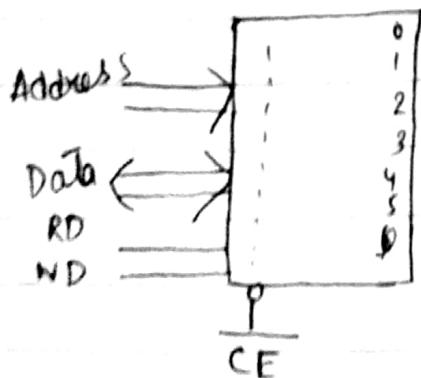
$$RD = 0$$

$$WR = 1$$

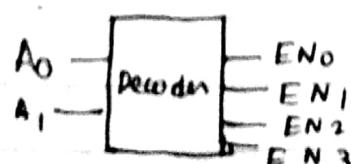
$R/W$

$N/\bar{R}$

- Multiplexing :-
- Reduce the pin count (Adv.)
- chip size will be reduced
- Power dissipation will also be reduced



$$8 \times 4 = 32 \text{ digits}$$



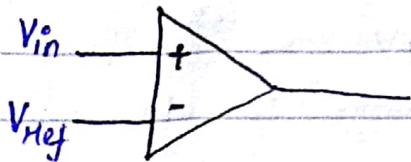
a

$A_1$	$A_0$	$EN_0$	$EN_1$	$EN_2$	$EN_3$
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

# comparator Circuit

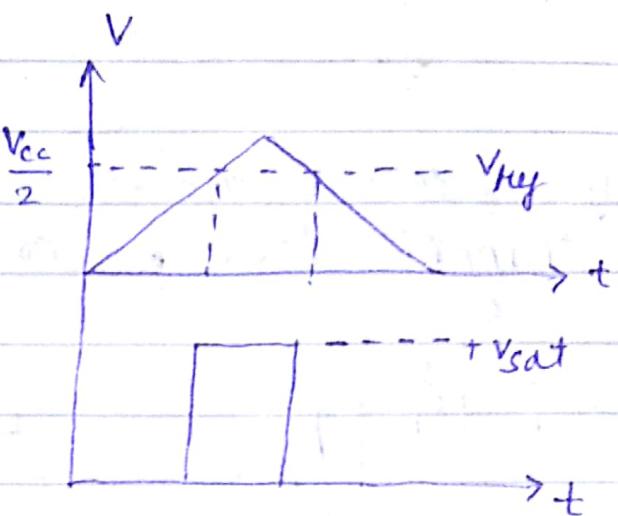
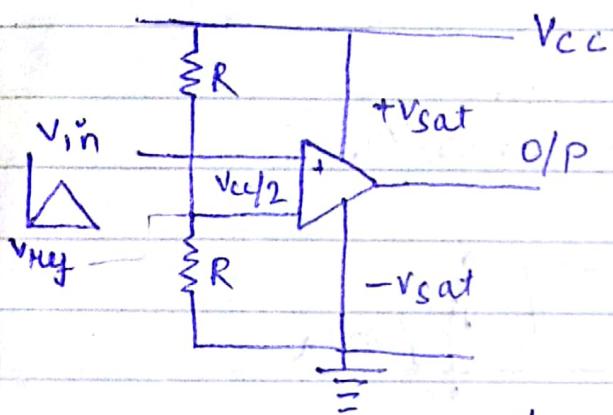
## 1) Non-Inverting

handwriting

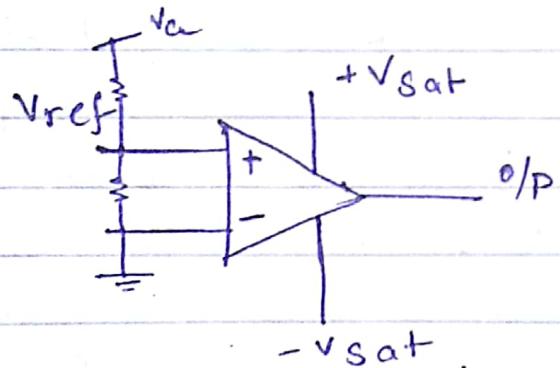


(-)ve terminal = Inverting

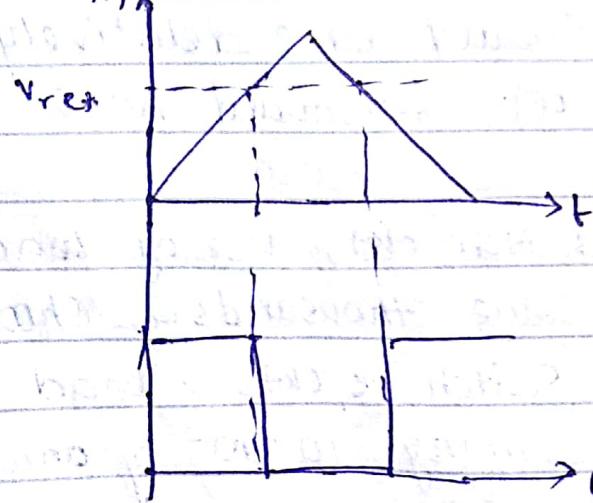
(+)ve terminal = Non Inverting

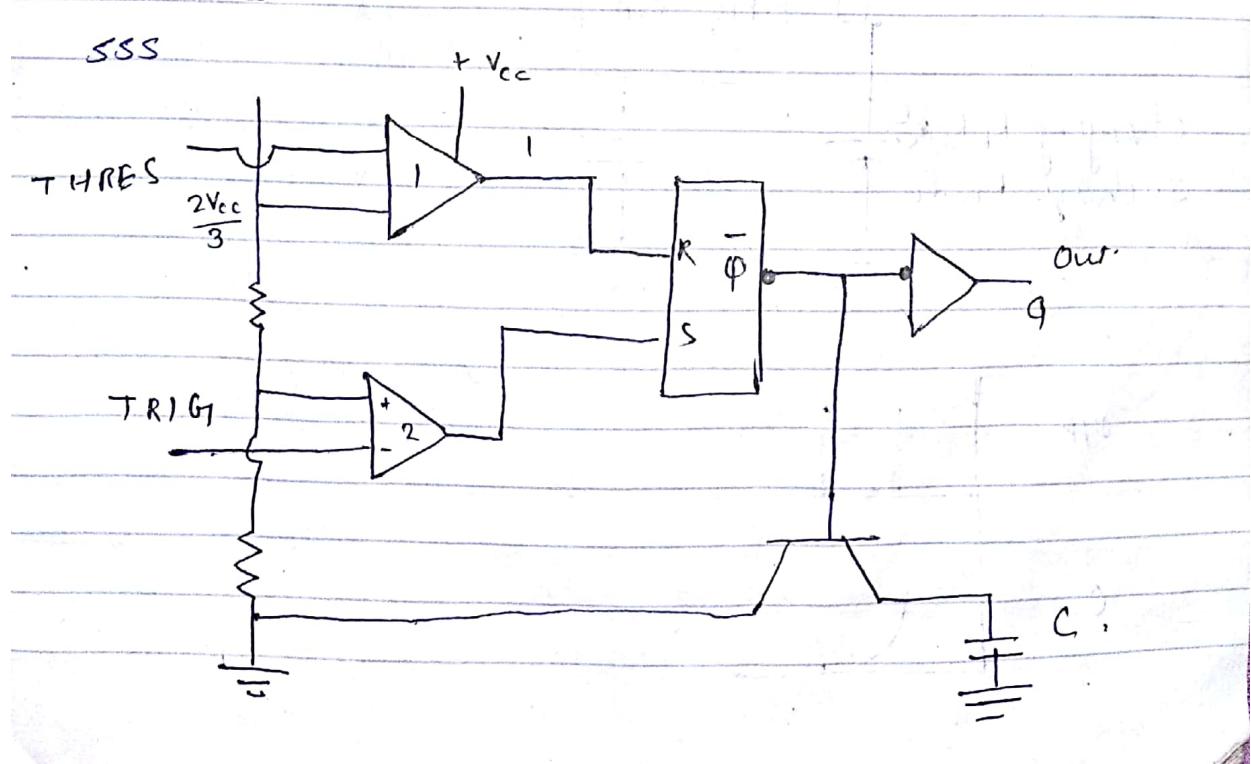
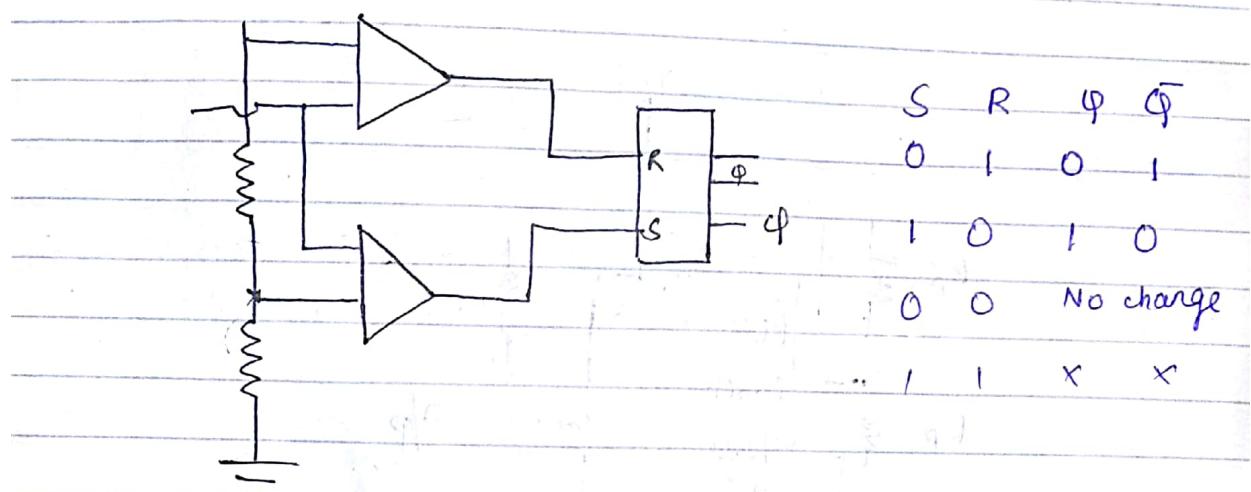
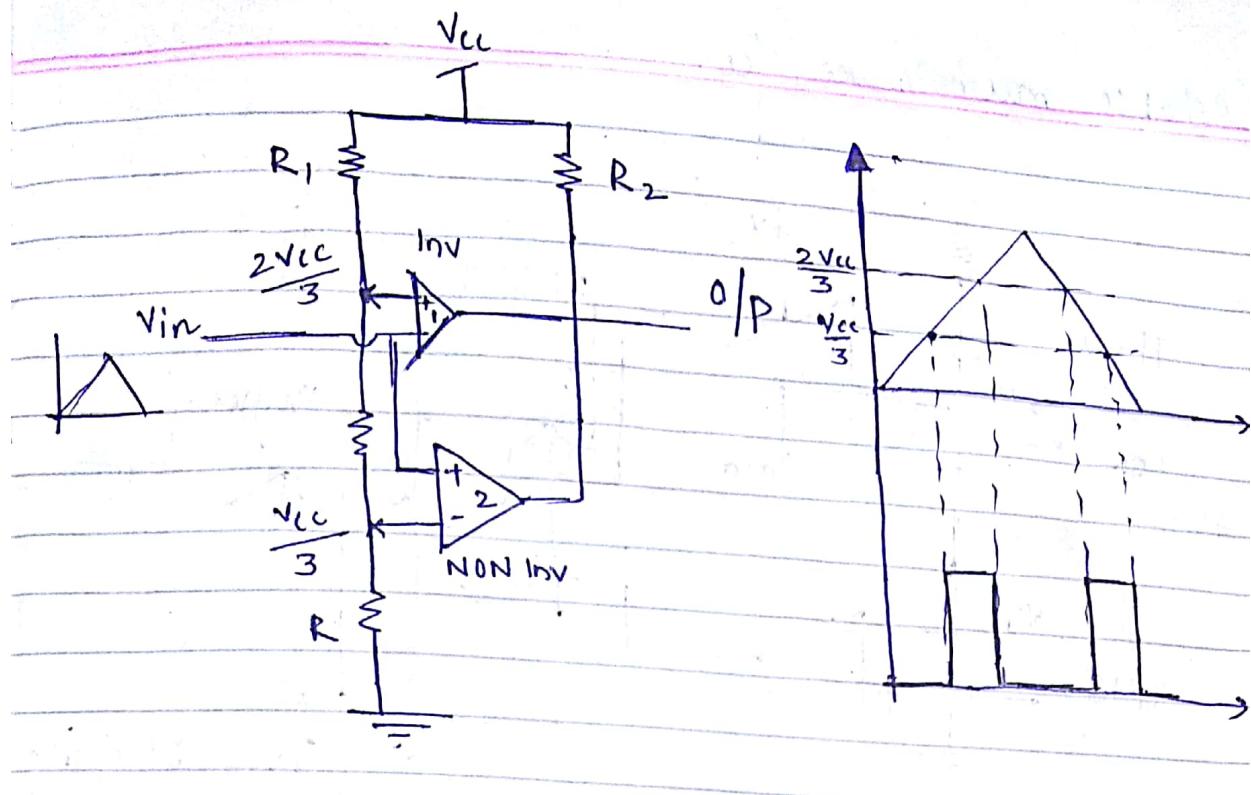


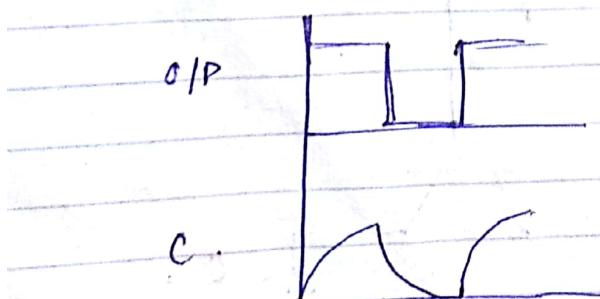
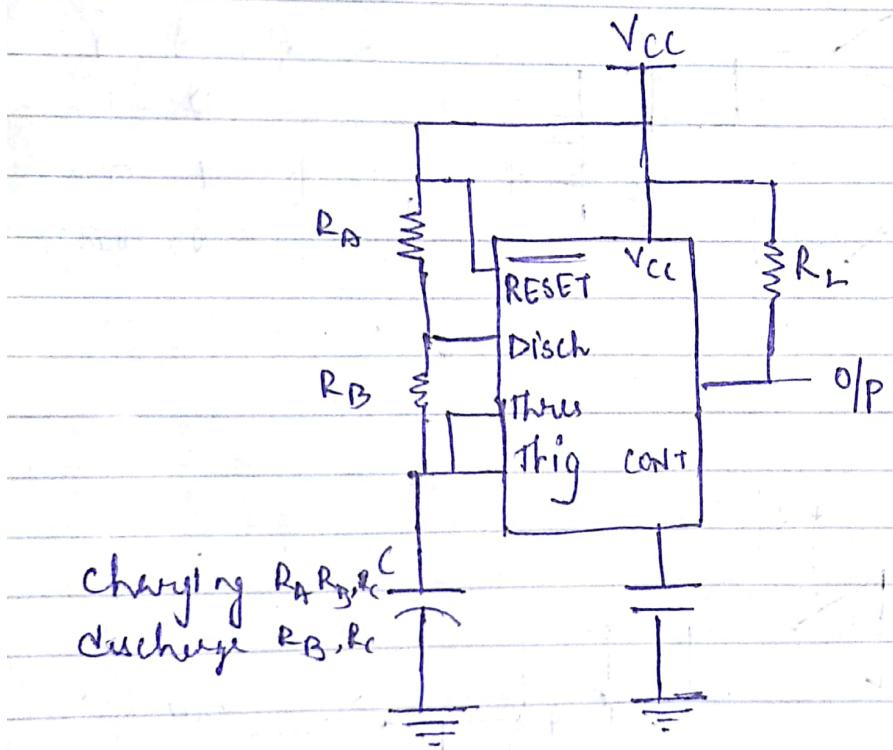
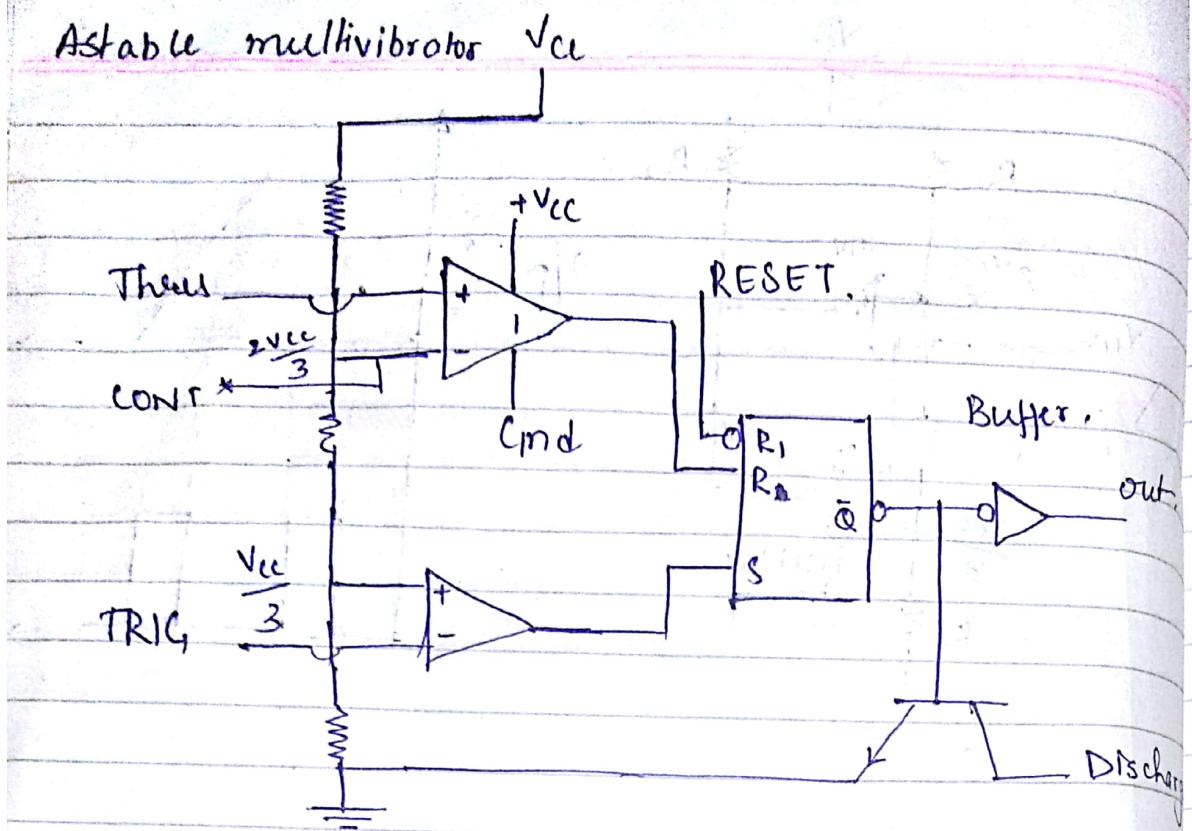
Inverting



$V_{in}$







$$t_H = 0.693 (R_A + R_B)C$$

$$t_L = 0.693 (R_B)C$$

$$\text{Time period} = 0.693 (R_A + 2R_B)C$$

$$\text{Frequency} = \frac{1.44}{(R_A + 2R_B)C}$$

$$\text{Duty cycle} = \frac{T_H}{T_H + T_L} \quad \text{or} \quad \frac{T_L}{T_H + T_L}$$

Generates clock frequency

for NE555 pin diagram.

GND	1	8	V <sub>cc</sub>
TRIG	2	7	Disch
OUT	3	6	Thres
RESET	4	5	CONT

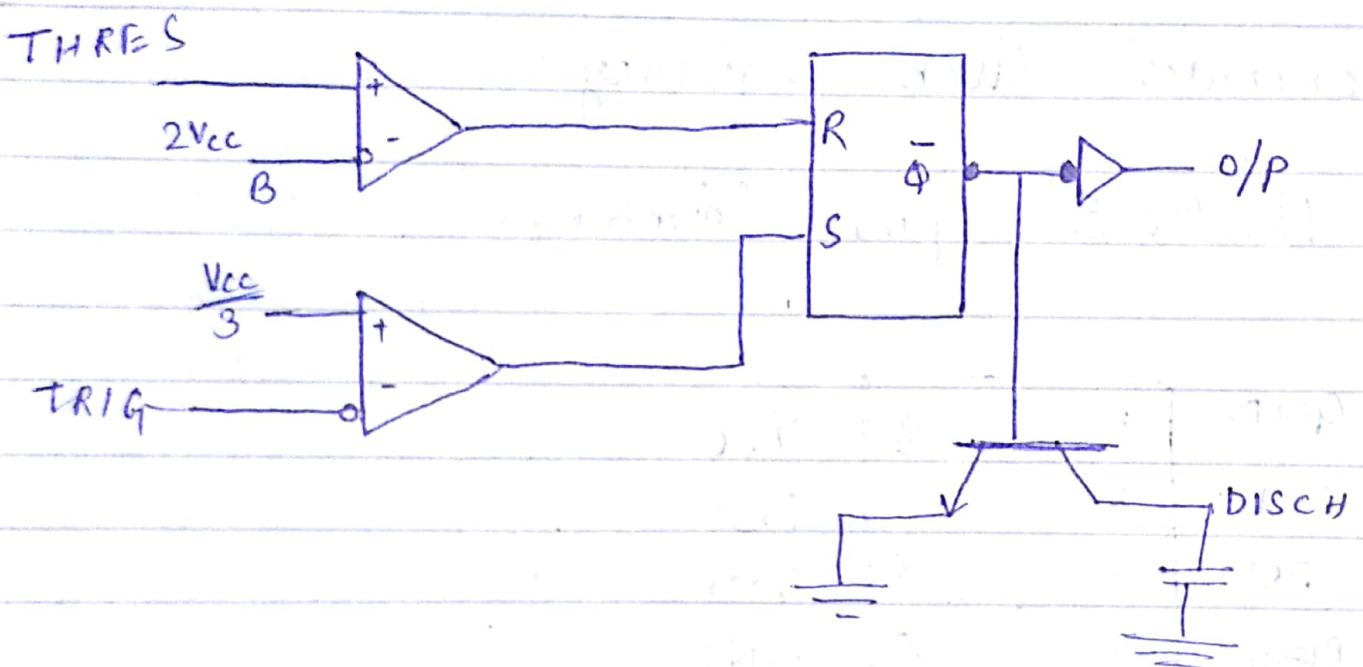
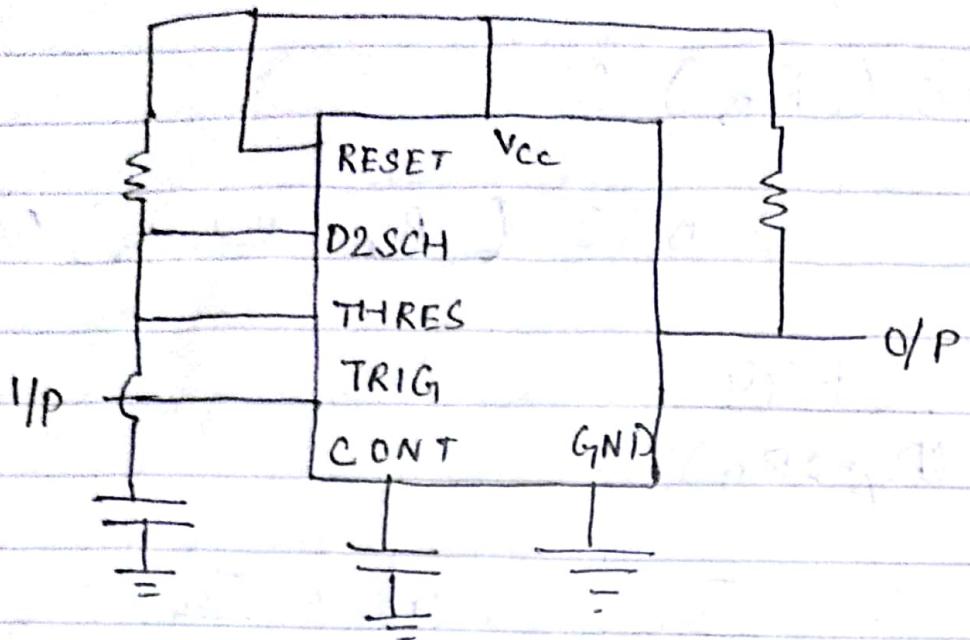
V<sub>cc</sub> max limit 16V.

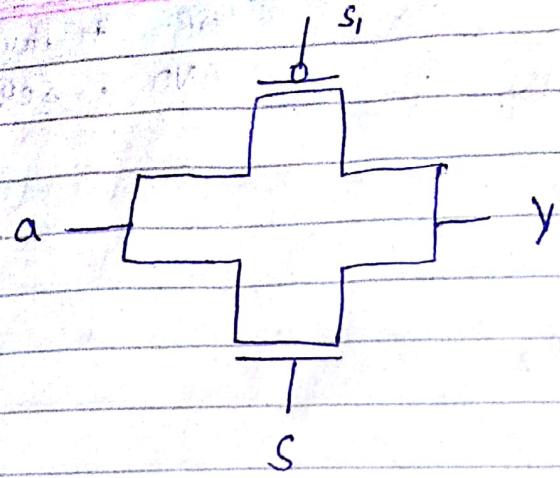
Trig → Start timing input when Trig voltage < V<sub>cc</sub>/2. (control voltage)

threshold → end of timing input when Thres > V<sub>cc</sub> (control).

Disch → open collector o/p to discharge timing capacitor.

cont → control pin bidirectional comparator threshold, o/p voltage is  $\frac{2V_{cc}}{3}$ .



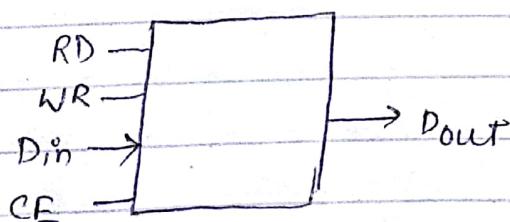
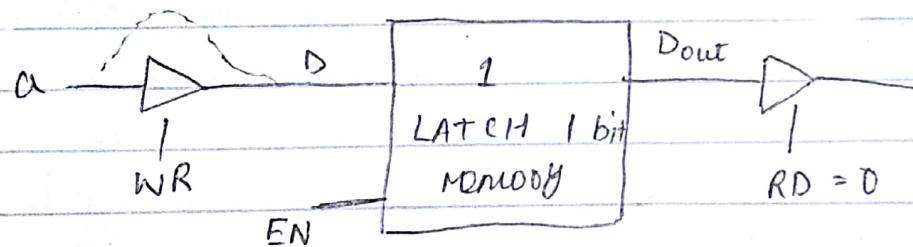


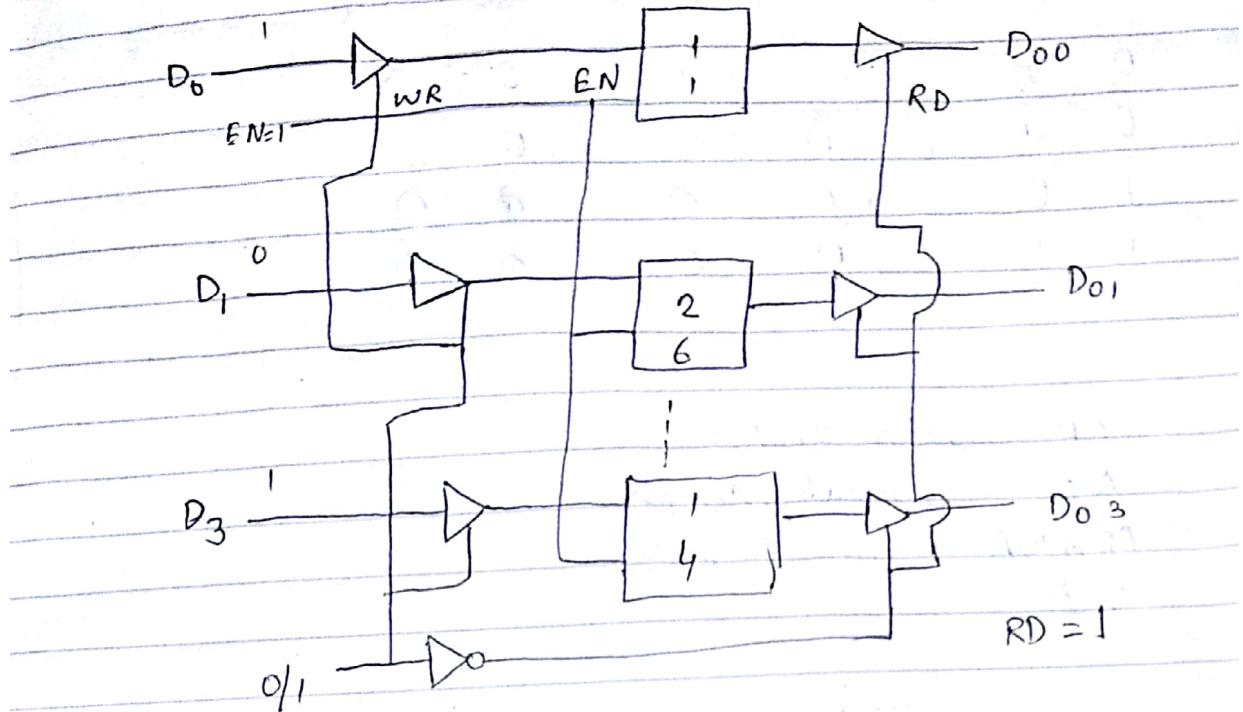
Tristate switch/  
transmission gate

$S$	$a$	$y$
1	$a$	$a$
0	$a$	$z$
1		
1		

$z = z$  is the high  
impedance output w

—x—





$$T = 1S$$

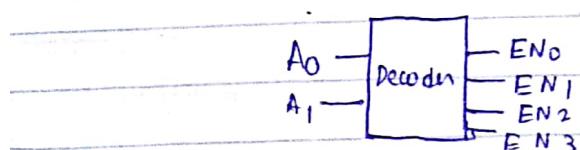
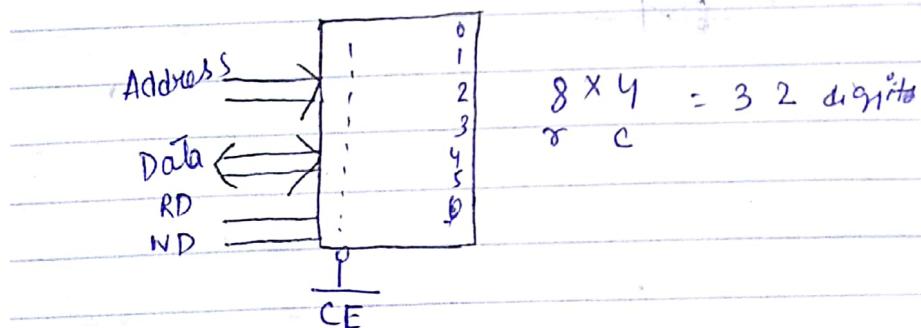
$$RD = 0$$

$$WR = 1$$

$R/W$

$W/R$

- Multiplexing :
- Reduce the pin count (Adv.)
  - chip size will be reduced
  - Power dissipation will also be reduced



a

$A_1$	$A_0$	$EN_0$	$EN_1$	$EN_2$	$EN_3$
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

CE = cheap Enable

ADDR = generate Address

RD or WR = Read or Write

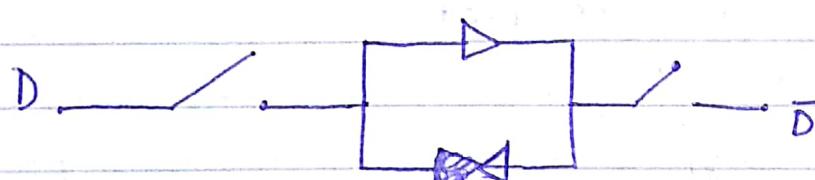
Data

- x -

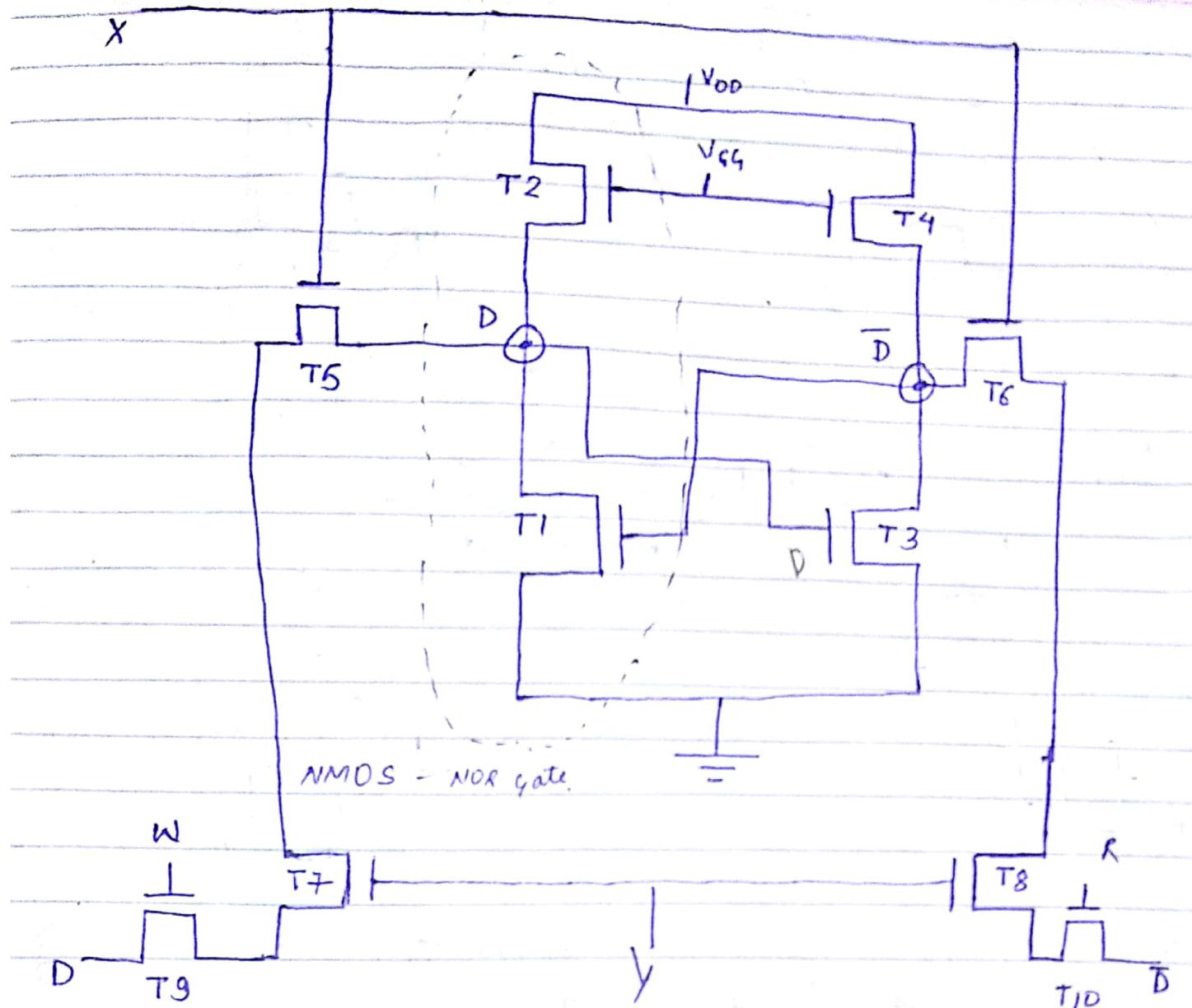
RAM

→ Static RAM (faster than DRAM)

→ Dynamic RAM



# SRAM (6 transistor SRAM design)

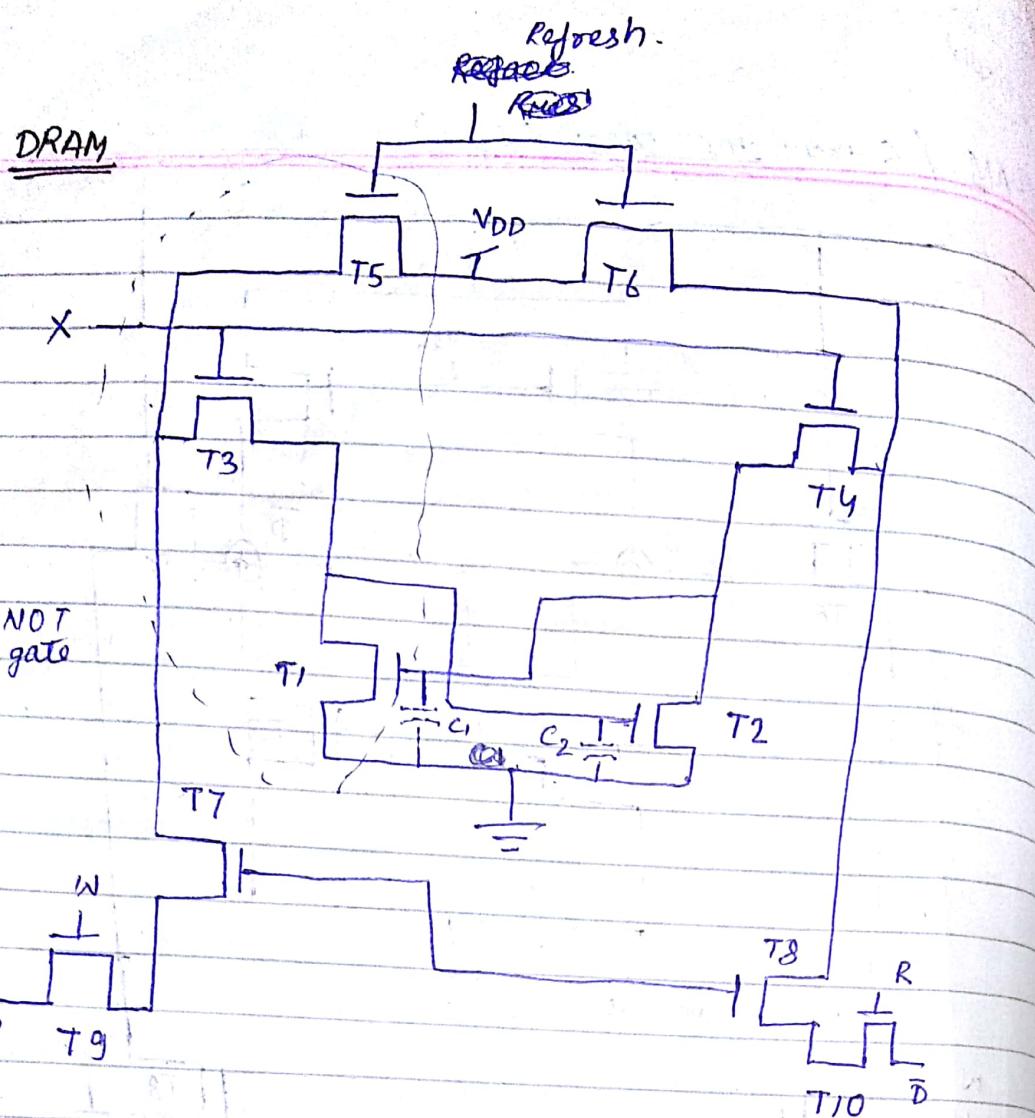


X, y = addressed

- ① Address
- ② Din
- ③ R/W

$V_{GG}$  function = helps to maintain  
the resistance of load  
Driver = T<sub>1</sub> and T<sub>3</sub>.

∴ switching time of SRAM is much better  
than DRAM



$C_1, C_2$  = capacitors store data.

$V_T$  = threshold voltage

Driver gate = T1

- ~~DISB~~
- ~~COSB~~
- 1) Refresh the data after some interval of time.
  - 2) Data R/W time is higher than the SRAM.

Pros :

No. of transistors less

Why MOS transistor not BJT?

- 1) Area less
- 2) Scaling of MOS is very easy than the BJT

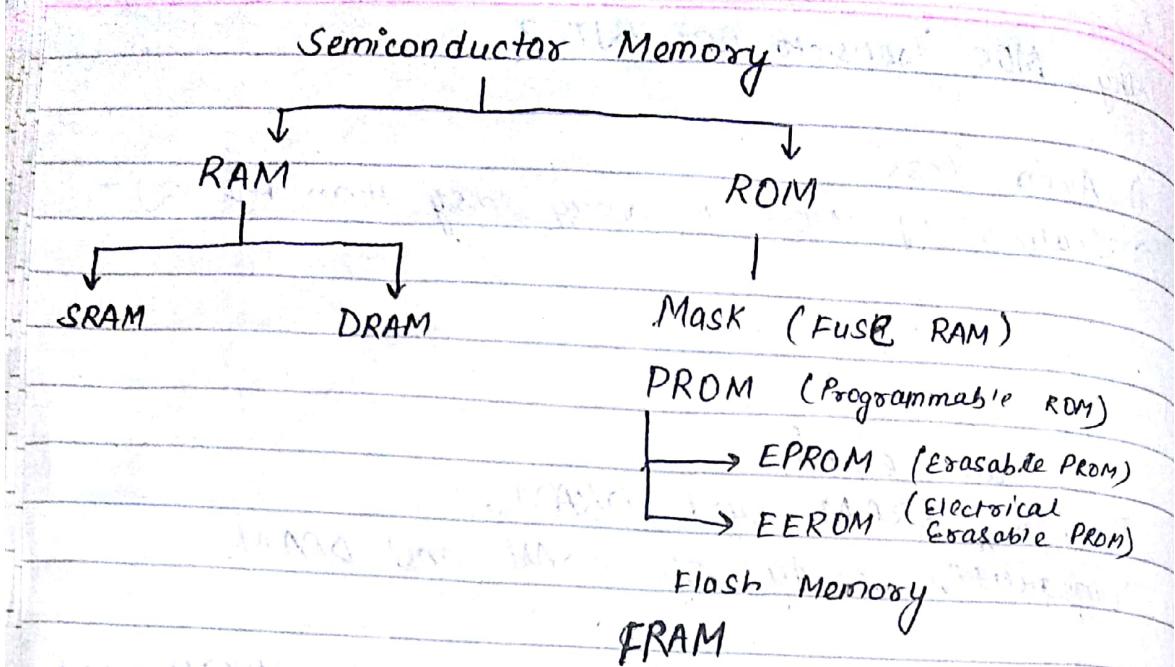
Imp

and explain

1. Design SRAM and DRAM.
2. Comparative study of SRAM and DRAM.
3. The area efficiency of the memory array, i.e. the no. of stored data bits per unit area (This is the main problem), is one of the key design criteria that determine the overall storage capacity and hence, the memory cost per bit.

Cost / bit of SRAM is higher than the DRAM.

- another important issue is the memory access time, i.e., the time required to store and/or retrieved a particular data bit in memory array.
- The access time determine the memory speed which is an important performance criteria of the memory array.
- Finally, the static and dynamic power consumption of the memory array is a significant factor to be considered in a design, because of the increasing power of the low power application



### MASK ROM

In which data are reading during chip fabrication by using a photomask

### PROM

In which data are ~~re~~written electrically after chip fabrication.

Depending on data erasing characteristic PROM are further classified into FUSE ROM, EPROM, EEPROM.

EPROM and EEPROM can be rewritten ~~re~~

but re write operation is limited to  $10^4 - 10^5$  times.

The drawback of EEPROM is slower write speed.

## DRAM

1. The DRAM cell consists of a capacitor to store binary information, 1 - high voltage 0 - low voltage power is turned ON. The cell information (voltage) is degraded mostly due to junction leakage current at the storage node.
  2. DRAM is widely used for main memory & main frame computers.
1. The SRAM cell consists of a latch, therefore, the cell is kept as long as the 1 - high voltage 0 - low voltage power is turned ON. The refresh operation is not required.
2. SRAM is used for cache memory in microprocessors, main frame computers.
3. SRAM works fast
4. " costly and uses less power.

## SRAM