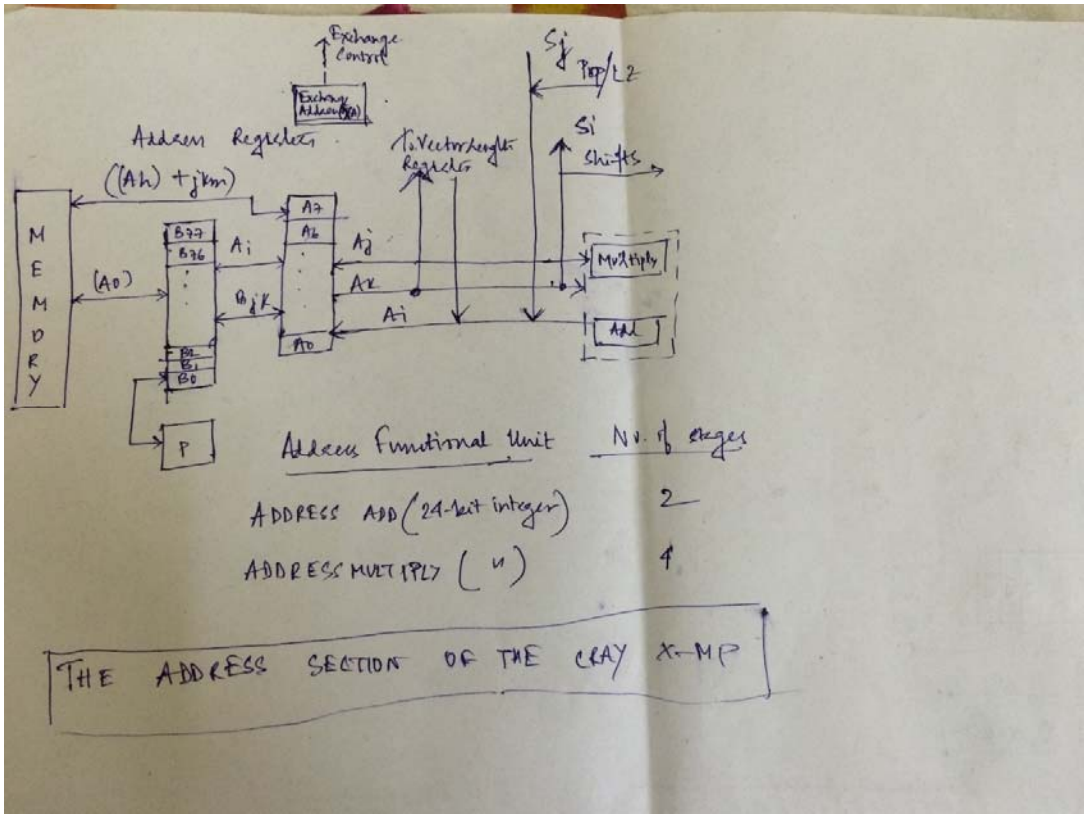
LECTURE 6



(FIGURE 1: THE ADDRESS SECTION OF THE CRAY X-MP)

Address register (A0 – A7) → 8 24 bit registers:

- They hold addresses referenced in memory operations.
- They are also used as index registers and for short integer computations.

B registers (B0 – B77) → 64 24-bit registers:

- They are not connected directly to the functional units.
- They are used for saving registers during subroutine linkage or for temporary storage of addresses.

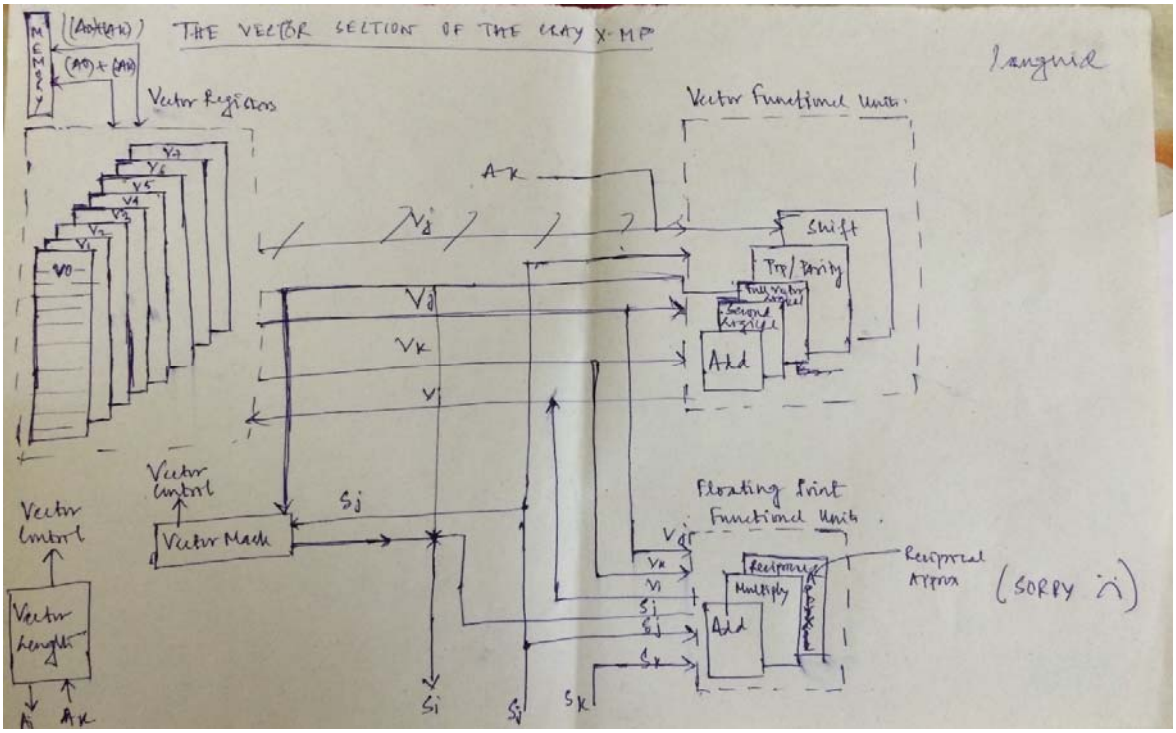
Addresses on the CRAY X-MP:

All memory data is stored in words of 64 bits and word addresses are specific by 22 bits. Instructions take up either 16 bits (one parcel) or 32 bits (2 parcels) and parcel addresses are 24 bit wide.

A and B register addresses are either interpreted as 22-bit word addresses or as 24-bit parcel addresses depending on the instruction in which they occur.

h, I , j, k, m → octal digit

INSTRUCTION	DESCRIPTION	OCTAL CODE
Ai exp, Ah	Read Ai from location Ah + exp	10hijkm m is 16 bit h, i, j, k is 3 bit exp is coded as jkm
Exp, Ah Ai	Store Ai at location Ah + exp	11hijkm
J Bjk	Branch to address in Bjk	0050jk
R exp	Branch to address exp = ijkm, after setting B00 to P + 2	007ijkm
Ai Bjk	Set Ai to Bjk	024ijk
Bjk Ai	Set Bjk to Ai	025ijk
Ai Sj	Copy lower 24-bits of Sj into Ai	023ij0
Ai VL	Set Ai to VL	023i01
Ai ZSj	Set Ai to leading zerocount of Sj Ai = 64 if Sj = 0	027ij0
Ai Aj + Ak	Set Ai to Aj + Ak	030ijk
Ai Aj * Ah	Set Ai to Aj * Ah	032ijk
Ai PSj	Set Ai to number of ones in Sj (population count)	026ij0



(FIGURE 2: VECTOR SECTION OF THE CRAY X-MP)

A vector is defined as a collection of values which are stored in memory locations spaced a fixed distance apart.

1. The spacing of the elements is called the stride of the vector.
2. Parallelism and computational efficiency achieved in a vector processor when a significant portion of a programs data can be mapped into vectors.

The same operations can be performed on all of the elements of a vector with results becoming available on consecutive clock cycles.

<u>Basic Operations of Vector Section:</u>

1. Each processor of the Cray X-MP has 8 octal registers V0...V7. Each register in 64-bit words long.
2. Since there are no direct connections from main memory to the vector functional units, all vector arithmetic operations are performed through the vector registers.
3. A vector is processed by reading its components into the consecutive elements of the vector registers starting with element 0 and going through element VL-1. VL is the value of the vector length register when the instruction is issued.
4. The source and destination vector registers and the functional units are reserved during vector operations.
5. All of the vector functional units are pipelined. The units are designed to perform the same operation on each element of a vector.

6. Once the pipeline of a functional unit is filled, the unit will produce a result on every clock cycle.

There are 3 phases of the pipelined operation:

The 1st phase is called the setup phase. During this phase, the functional unit is set to perform the appropriate operation and the source and destination routes to the vector registers are established. The setup time for all the vector functional units is 3 clock cycles.

The 2nd phase is called the execution phase. During each clock cycle in this phase one pair of source elements enters the first stage of the pipeline and the result computed for the previous pair is sent to the next stage.

Vector Functional unit	*No of Clock Cycles*
Vector ADD(64-bit integer)	3
Vector SHIFT(64-bit)	3
Vector SHIFT(128-bit)	4
Full vector logical(64-bit)	2
2nd vector logical(64-bit)	4
Vector pop or parity	5
Floating add	6
Floating mul	7
Reciprocal approximation	14

One cycle after the last pair of input elements has elements has entered the pipeline the functional unit can be used for another operation. Thus the functional unit will be available is

3*VL + 1 = VL + 4 clock cycles

Here VL is the value of the vector length register during the issuing of the instruction.

The source operands become available immediately after the last pair of input elements has entered the pipeline. Vector source registers are therefore reserved for VL + 3 clock cycles.

The 3rd phase of the pipeline operation is the **shutdown phase.** Shutdown time is the difference between the time when the last individual result emerges from the pipeline and the time when the destination vector register becomes available for another operation. Shutdown time is 3 clock cycles so the destination register becomes also available in:

$$3 + n + (VL - 1) + 3 = n + VL + 5$$

Where n is the number of stages in the pipeline and VL is the number of components operations to be performed (chaining is an exception to this rule).