BACHELOR OF COMPUTER Sc. ENGG. EXAMINATION, 2009

(2nd Year, 1st Semester)

DIGITAL CIRCUITS

Time : Three hours | Full Marks : 100

Answer any ***five*** questions.

1. a) With the help of a circuit diagram explain the operation of a DTL gate. 8

   b) Estimate the reverse recovery current and output impedances of the same. 4+4

   c) Hence discuss its merits and demerits. 4

2. a) Explain the operation of a TTL gate. 10

   b) What are the open collector and Tristate gates ? Why are they required ? 4+4+2

3. a) How can an Inverter be implemented using MOSFET ? Explain. 8

   b) Explain the drawbacks of the same. 8

   c) Estimate the rise time of an MOS inverter assuming C_L = 5 pf, K_L = 12 $\mu A/v^2$ and V_f = 10 V. 4

4. a) Explain the operation of a clock generator using an 555 IC. 8

[TURN OVER]

b) Deduce the expressions for the frequency and duty cycle. 6+2

c) Design a clock woring at 1 KHz with 40% duty cycle using a .01μf capacitor. 4

5. a) Explain the operation of a static MOS memory cell. 10

b) Design a 4 K × 8 bit memory system using 1 K × 4 bit memory chips. 6

c) How can Non-volatile RAM be implemented ? 4

6. a) Explain the operation of a Ladder Type DAC. 12

b) How can the effect of R_L be eliminated ? 4

c) What are its relative merits and demerits ? 4

7. a) How can an Analog input voltage be converted to Digital form ? 4

b) Explain the operation of a counter type ADC. 10

c) What are its demerits and how can they be resolved ? 6

8. Write short notes on any *four* of the followings : 5×4

a) HTL ;

b) ECL ;

c) C MOS ;

d) Frequency Multiplication ;

e) EP ROM's ;

f) 1's Complement DAC ;

g) Sample / Hold Circuits ;

h) Analog Multiplexers.

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