

# EMITTER-COUPLED LOGIC

## 7.1 INTRODUCTION

All the other logic forms considered (RTL, DTL, TTL) suffer from a common and fundamental limitation on their speed of operation. This limitation occurs because in all these logic types transistors are driven into saturation, resulting in an increased propagation delay time. This consideration prompts us to inquire whether a logic form is possible in which transistors are switched from cutoff to an operating point in the active region. Certainly the forms so far considered cannot be operated in this way; for the range of base-emitter voltages in the active region extends over only some tens of millivolts, and there are so many variable factors (temperature variations, variability due to manufacture, etc.) to contend with. Suppose we arranged that at one logic level a transistor stage is operating in its active region. Then a small drift of the applied input voltage would be enough to drive the transistor either to cutoff or saturation with a correspondingly large change in the stage output voltage.

It is possible to establish a transistor in its active region, with stability, by introducing negative feedback through the simple expedient of using a large emitter resistor. This is precisely what is accomplished when using an emitter

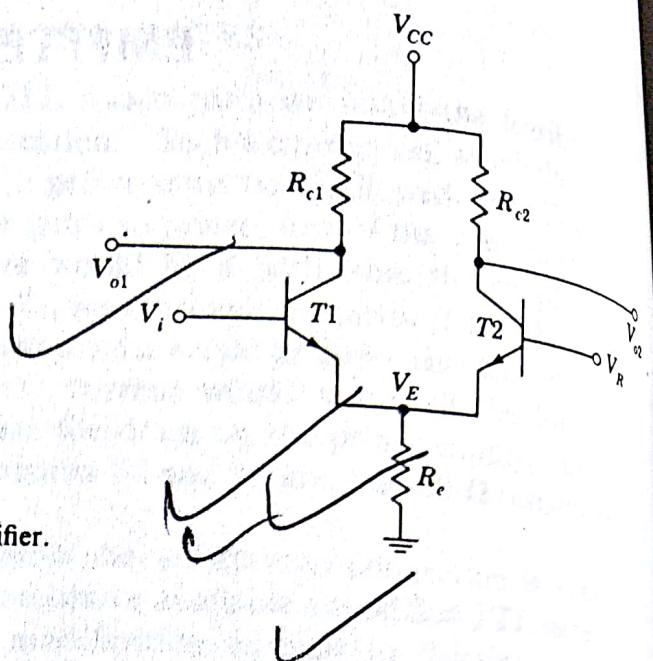


FIGURE 7.1-1  
The difference amplifier.

~~follower or a phase splitter. The difficulty with this arrangement is that with a large emitter resistor, a large input-voltage swing at the base is required to carry the transistor from cutoff well into the saturation region. We can achieve both ends, however, i.e., active-region operation with stability and switching between this region and cutoff with a small input-voltage swing. These ends are accomplished by devising a circuit which will not turn a transistor current ON and OFF but will rather switch a current from one transistor to another.~~

~~The basic circuit configuration employed in the logic type under consideration, shown in Fig. 7.1-1, will, of course, be recognized as the *difference amplifier*, which was discussed in Sec. 2.1 in connection with its use in operational amplifiers and comparators. Since in this difference amplifier the emitters of the two transistors are connected, the logic family based on this circuit is referred to as *emitter-coupled logic*.~~

~~In the present application as a logic gate, the base of transistor  $T_2$  is held at a fixed reference voltage  $V_R$  while an input voltage  $V_i$  is applied to the base of transistor  $T_1$ . When  $V_i$  is sufficiently lower than  $V_R$ , transistor  $T_1$  will be cut off and current will flow through  $T_2$ . The reference voltage  $V_R$  and the resistors  $R_{c2}$  and  $R_e$  are selected to assure that  $T_2$  operates in its active region and is not saturated. When  $V_i$  rises to equal  $V_R$ , the currents in the two transistors will be nominally equal. Finally, as  $V_i$  continues to increase, the emitter voltage  $V_E$  increases, since  $V_E = V_i - V_{BE1}$  and  $V_{BE1}$  is approximately constant, and eventually  $T_2$  will cut off. We now have  $T_1$  operating in its active region. In summary, then, it appears that a variation of  $V_i$  will switch the current from one transistor to the other. As a matter of fact, we shall show that as  $V_i$  changes from the point where  $T_1$  is cut off to the point where  $T_2$  is just cut off, the total emitter current through  $R_e$  changes less than 2 percent. Thus, the mechanism of operation consists in switching a nominally fixed emitter current from one transistor to the other.~~

## 7.2 THE ECL GATE

An ECL gate, incorporating the basic structure of Fig. 7.1-1, is shown in Fig. 7.2-1. The input transistor  $T_1$  in Fig. 7.2-1 is shown here paralleled by a number of transistors to provide for multiple gate inputs.

Outputs are taken at the collectors through emitter followers. The emitter followers provide buffering and low impedance at the output terminals. An accurate, temperature-controlled reference voltage  $V_R = -1.175$  V (at room temperature) is employed at the base of  $T_2$ . The supply voltage employed is  $-V_{EE} = -5.2$  V. Note that, contrary to the usual pattern, the collector resistors of the transistors are grounded and the emitter transistors are connected to a negative supply voltage. Thus, all the voltages encountered here will be negative. The reason for this reversal is discussed in Sec. 7.11.

As with other gates, ECL gates are commercially available in a number of types differing largely in the values of resistor components. Higher-resistance units dissipate less power and operate at a lower speed. Lower-resistance units dissipate more power but are faster. The gate with components and reference voltage in Fig. 7.2-1 is a Motorola unit of medium speed and power dissipation, designated as MECL II.

The ECL gate can operate as either a NOR gate or as an OR gate. It can be readily verified that if  $V_{o1}$  is taken as the output, a NOR gate is realized, while if  $V_{o2}$  is used, an OR gate results. In many an application either one or the other output will be used, while in some applications it is a great convenience to have available both outputs, which are, of course, complements of one another.

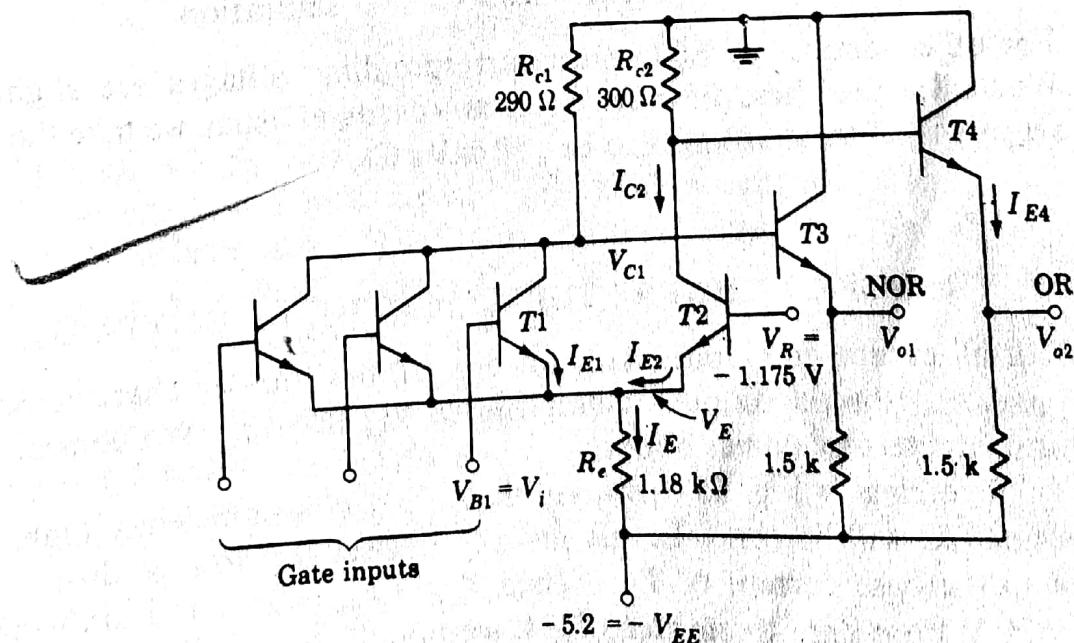


FIGURE 7.2-1  
An ECL gate.

### 7.3 ECL-TRANSISTOR VOLTAGES

The saturation current of a transistor is  $I_{\text{sat}} = [V_{CC} - V_{CE}(\text{sat})]/R$ , in which  $V_{CC}$  is the supply voltage and  $R$  is the total resistance in series with the transistor. If, as usual,  $V_{CE}(\text{sat}) \ll V_{CC}$ , then  $I_{\text{sat}} \approx V_{CC}/R$  rather independently of any transistor characteristic. The base-emitter voltage  $V_{BE}$  ( $= V_\sigma$ ) required to cause this current  $I_{\text{sat}}$  to cross the emitter junction depends on the cross-sectional area of the emitter junction. That is, at least at the onset of saturation,

$$I_{\text{sat}} = I_C \approx I_E = I_{E0} e^{V_\sigma/V_T}$$

Here  $I_C$  and  $I_E$ , are the collector and emitter currents, respectively, and  $I_{E0}$  is the emitter-junction reverse saturation current, which is proportional to the area of the emitter junction. Hence, altogether  $V_\sigma$  depends on  $V_{CC}$ ,  $R$ , and the emitter junction area.

For the gates considered so far it has turned out that the supply voltages, resistor values, and the geometry of the integrated transistor have been such that using  $V_\sigma \approx 0.75$  V gives reasonable agreement with measured voltages. For ECL gates, however, a better value is  $V_\sigma = 0.8$  V. This higher voltage value is a result principally of the smaller physical dimensions of the ECL transistor, a feature which serves as well to reduce capacitance and hence improve speed.

Consistent with previous procedures we may again consider that cutoff is at a voltage about 100 mV lower than  $V_\sigma$ . On this basis we have  $V_y = 0.70$  V. And, as has been our practice, we shall assume that when the transistor is in its *active* region, the base-emitter voltage, which we shall call  $V_{BEA}$ , is  $V_{BEA} = 0.75$  V, that is, midway between  $V_y$  and  $V_\sigma$ . In summary, at room temperature, for the transistors in the ECL circuit of Fig. 7.2-1 we shall use

$$V_{BE} = \begin{cases} V_y = 0.70 \text{ V} & \text{cut-in} \\ V_{BEA} = 0.75 \text{ V} & \text{active region} \\ V_\sigma = 0.80 \text{ V} & \text{saturation} \end{cases} \quad (7.3-2)$$

For other families of ECL gates corresponding voltages are slightly different. We shall neglect these differences. In any event, as usual, we take the temperature sensitivity of these voltages to be  $-2$  mV/ $^{\circ}\text{C}$ .

### 7.4 TRANSFER CHARACTERISTIC: THE OR OUTPUT

With all except one input transistor cut off, the transfer characteristic between  $V_i$  and  $V_{o2}$  (the OR output) is as given in Fig. 7.4-1a. We consider now how this characteristic comes about.

Referring to Fig. 7.2-1, we see that when  $V_i$  is sufficiently high,  $T1$  will be ON and  $T2$  will be OFF. Let us initially neglect the voltage drop through  $R_{c2}$  due to the base current of  $T4$ . Then  $V_{c2} = V_{b4} = 0$  V, and allowing a voltage of 0.75 V from base to emitter of  $T4$ , we find  $V_{o2} = -0.75$  V. However, as we shall now see, the neglect of the drop through  $R_{c2}$  is not entirely justifiable, and a small correction is in order.

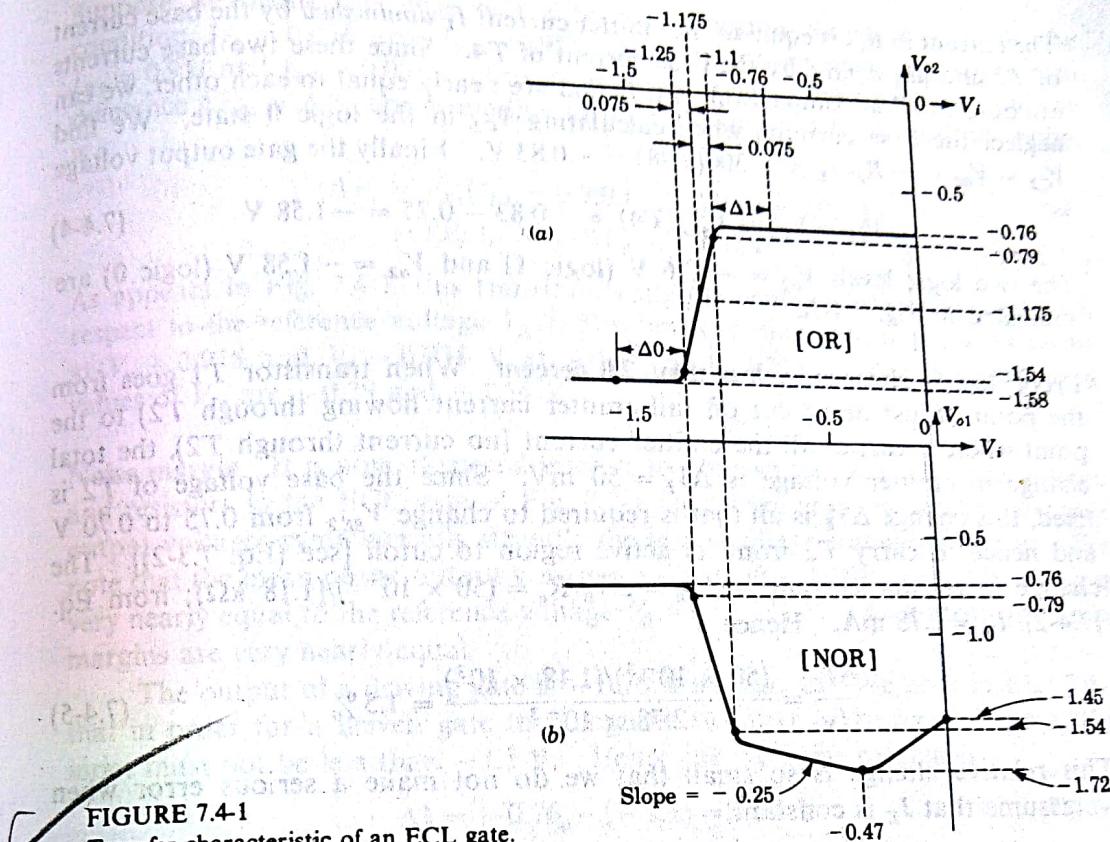


FIGURE 7.4-1  
Transfer characteristic of an ECL gate.

The emitter current of  $T_4$  is

$$I_{E4} = \frac{-0.75 + 5.2}{1.5} \approx 3 \text{ mA} \quad (7.4-1)$$

Transistors in ECL gates have current gains  $h_{FE}$  in the range from about 40 to 150. We use  $h_{FE} = 100$  as a typical value. The base current of  $T_4$  is  $I_{B4} = I_{E4}/(h_{FE} + 1) = 3/101 \approx 0.03 \text{ mA}$ . This base current flows through  $R_{c2} = 300 \Omega$  and produces a voltage drop  $300(-0.03 \times 10^{-3}) \approx 0.01 \text{ V}$ . Hence  $V_{C2} = V_{B4} \approx -0.01 \text{ V}$  rather than 0 V, and correspondingly  $V_{o2} \approx -0.76$ , as indicated in Fig. 7.4-1a.

Now let  $V_i$  decrease so that  $T_1$  turns OFF and  $T_2$  enters its active region. The emitter-to-ground voltage  $V_E$  is then

$$V_E = V_R - V_{BEA}(T2) = -1.175 - 0.75 = -1.925 \text{ V} \quad (7.4-2)$$

The emitter current is

$$I_E = \frac{V_E - (-V_{EE})}{R_e} = \frac{-1.925 + 5.2}{1.18} = 2.78 \text{ mA} \quad (7.4-3)$$

The current in  $R_{c2}$  is equal to the emitter current  $I_E$  diminished by the base current of  $T_2$  and augmented by the base current of  $T_4$ . Since these two base currents are both small in comparison with  $I_E$  and are nearly equal to each other, we can neglect the base currents when calculating  $V_{C2}$  in the logic 0 state. We find  $V_{C2} = V_{B4} = -R_{c2} I_E = -300(2.78) = -0.83$  V. Finally the gate output voltage is

$$V_{o2} = V_{B4} - V_{BEA}(T4) = -0.83 - 0.75 = -1.58 \text{ V} \quad (7.4-4)$$

The two logic levels  $V_{o2} = -0.76$  V (logic 1) and  $V_{o2} = -1.58$  V (logic 0) are indicated in Fig. 7.4-1a.

**Proof that  $I_E$  changes by less than 2.0 percent** When transistor  $T_1$  goes from the point of just being cut off (all emitter current flowing through  $T_2$ ) to the point where it carries all the emitter current (no current through  $T_2$ ), the total change in emitter voltage is  $\Delta V_E = 50$  mV. Since the base voltage of  $T_2$  is fixed, this change  $\Delta V_E$  is all that is required to change  $V_{BE2}$  from 0.75 to 0.70 V and hence to carry  $T_2$  from its active region to cutoff [see (Eq. 7.3-2)]. The change in emitter current is  $\Delta I_E = \Delta V_E/R_e = (50 \times 10^{-3})/(1.18 \text{ k}\Omega)$ ; from Eq. (7.4-2),  $I_E = 2.78$  mA. Hence

$$\frac{\Delta I_E}{I_E} = \frac{(50 \times 10^{-3})/(1.18 \times 10^3)}{2.78 \times 10^{-3}} = 1.5\% \quad (7.4-5)$$

This relative change is so small that we do not make a serious error when we assume that  $I_E$  is constant.

**Transition width** As  $V_i$  increases,  $V_{o2}$  changes from -1.58 V (logic 0 assuming positive logic) to -0.76 V (logic 1). This change in logic level occurs as the input  $V_i$  swings through a transition region, which, as we shall now show, is 150 mV in width. We have

$$I_{E1} + I_{E2} = I_E = I = \text{const} \quad (7.4-6)$$

Over the transition region,  $T_1$  and  $T_2$  are both in their active regions; hence

$$I_{E1} \approx I_{E0} e^{V_{BE1}/V_T} = I_{E0} e^{(V_{B1} - V_E)/V_T} \quad (7.4-7)$$

and

$$I_{E2} \approx I_{E0} e^{(V_R - V_E)/V_T} \quad (7.4-8)$$

The ratio of emitter currents is

$$\frac{I_{E1}}{I_{E2}} = e^{(V_{B1} - V_R)/V_T} \quad (7.4-9)$$

Combining Eq. (7.4-9) with Eq. (7.4-6), we have

$$I_{E1} = \frac{I}{1 + e^{(V_R - V_{B1})/V_T}} \quad (7.4-10a)$$

and

$$I_{E2} = \frac{I}{1 + e^{(V_{B1} - V_R)/V_T}} \quad (7.4-10b)$$

Suppose we define one edge of the transition region to correspond to the condition  $I_{E1} = 0.05I$  and  $I_{E2} = 0.95I$  while the other edge corresponds to  $I_{E1} = 0.95I$  and  $I_{E2} = 0.05I$ . Then, as is easily verified, the total input voltage difference  $\Delta V_{B1} = \Delta V_1$ , corresponding to the total width of the transition region, is

$$\begin{aligned}\Delta V_1 &= V_{B1}(I_{E1} = 0.95I) - V_{B1}(I_{E1} = 0.05I) \\ &\approx 2V_T \ln 20 = 6V_T = 150 \text{ mV}\end{aligned}\quad (7.4-11)$$

As appears in Fig. 7.4-1, this transition range is symmetrically disposed with respect to the reference voltage  $V_R$ . The limits of the transition region occur at  $V_R + 0.075$  and  $V_R - 0.075$  V at  $-1.1$  and  $-1.25$  V. The corresponding values of  $V_{o2}$  are  $-0.79$  and  $-1.54$  V.

**Noise margin** It is now of special interest to observe that the reference voltage and resistors in the ECL gate of Fig. 7.2-1 have been selected so that the gate output voltages symmetrically straddle the input-voltage transition region. We note that the mean of the output voltages is  $\frac{1}{2}(-0.76 - 1.58) = -1.170$ . This is very nearly equal to the reference voltage  $V_R = -1.175$  V. As a result the noise margins are very nearly equal.

The output of a driving gate is  $-0.76$  V at logic 1. We note in Fig. 7.4-1 that in order for a driven gate to recognize an input as being at logic 1, this input must not be less than  $-1.1$  V. Hence the  $\Delta 1$  noise margin is

$$\Delta 1 = -0.76 - (-1.1) = 0.34 \text{ V} \quad (7.4-12)$$

Similarly the  $\Delta 0$  noise margin is

$$\Delta 0 = -1.25 - (-1.58) = 0.33 \text{ V} \quad (7.4-13)$$

It is to be noted that these noise margins are typical and not worst-case margins.

## 7.5 THE NOR OUTPUT

We have defined the edges of the transition region of the OR output as being the points where  $I_{C2} \approx I_{E2} = 0.05I$  and  $0.95I$ , where  $I$  is the nominally constant current through  $R_e$ . Since the current  $I = I_{E1} + I_{E2}$  is constant,  $I_{C1} \approx I_{E1} = 0.05I$  when  $I_{C2} \approx I_{E2} = 0.95I$  and vice versa. Hence, the transition points for the OR and NOR output occur for the same values of input  $V_i$  as shown in Fig. 7.4-1b. Further, if we neglect the small difference between  $R_{c1}$  and  $R_{c2}$ , the corresponding output voltages are also the same for OR and NOR outputs.

When  $V_i$  is low enough for  $T1$  to be cut off, the output voltage is  $V_{o1} = -V_{BEA}(T3) - I_{B3}R_{c1} = -0.75 - 0.01 = -0.76$  V, just as for the logic 1 level of the OR output. When, however,  $V_i$  has increased to the point where all the emitter current has transferred to  $T1$ , a further increase in  $V_i$  will result in a

(7.4-6)

(7.4-7)

(7.4-8)

(7.4-9)

(7.4-10a)

(7.4-10b)

further increase in  $I_{C1}$  and the output  $V_{o1}$  will continue to fall. With  $T_2$  cut off, the gain  $A$  from input to collector of  $T1$  is (see Sec. 6.5)

$$A = \frac{\Delta V_{C1}}{\Delta V_i} = -\frac{R_{c1}}{R_e} = -\frac{0.290}{1.18} = -0.25 \quad (7.5.1)$$

Hence, as indicated in Fig. 7.4-1,  $V_{o1}$  falls with this negative slope, until transistor  $T1$  begins to approach saturation.

We now estimate the input voltage  $V_i$  at which saturation begins to make itself felt. A transistor which is well into saturation has, as we have frequently noted, a collector-emitter voltage in the range 0.1 to 0.2 V. However, as shown in Fig. 1.10-1, when a transistor is just entering the region of saturation, the collector-emitter voltage is more nearly about 0.3 V. With 0.3 V between collector and emitter, the voltages  $V_{C1}$  and  $V_E$  are

$$V_{C1} = -(5.2 - 0.3) \frac{R_{c1}}{R_{c1} + R_e} = -\frac{4.9(0.290)}{1.47} = -0.97 \text{ V} \quad (7.5.2)$$

and

$$V_E = -0.97 - 0.3 = -1.27 \text{ V} \quad (7.5.3)$$

The output voltage  $V_{o1}$  and its corresponding input voltage are then

$$V_{o1} = V_{C1} - V_{BE3} = -0.97 - 0.75 = -1.72 \text{ V} \quad (7.5.4)$$

and

$$V_i = V_E + V_o = -1.27 + 0.8 = -0.47 \text{ V} \quad (7.5.5)$$

in which we have used 0.75 and 0.8 V, respectively, as the base-emitter drop for  $T3$  (in the active region) and  $T1$  (in saturation).

With a still further increase in  $V_i$ , the output  $V_{o1}$  begins to rise because additional emitter current in  $T1$  is diverted to the base and away from the collector. When  $V_i = 0$  V,  $T1$  is deeply in saturation. Using 0.8 and 0.1 V, respectively, as the base-emitter voltage and the collector-emitter voltage of  $T1$ , we have  $V_E = -0.8$  V and  $V_{C1} = -0.8 + 0.1 = -0.7$  V. The output voltage is

$$V_{o1} = -0.7 - 0.75 = -1.45 \text{ V} \quad (7.5.6)$$

as indicated in Fig. 7.4-1b.

When in Fig. 7.2-1,  $T1$  and some of its paralleling transistors conduct, the current in  $R_{c1}$  may be somewhat larger than the current in  $R_{c2}$  when  $T2$  is ON. To reduce the corresponding difference in the logic 0 levels of OR and NOR outputs,  $R_{c1}$  is made smaller than  $R_{c2}$ .

## 7.6 MANUFACTURER'S SPECIFICATIONS: TRANSFER CHARACTERISTIC

The ECL circuit shown in Fig. 7.2-1 corresponds in all respects, component values, supply and reference voltages, etc., to the line of ECL logic manufactured by Motorola and designated MECL II. The plots of Fig. 7.6-1 are published by

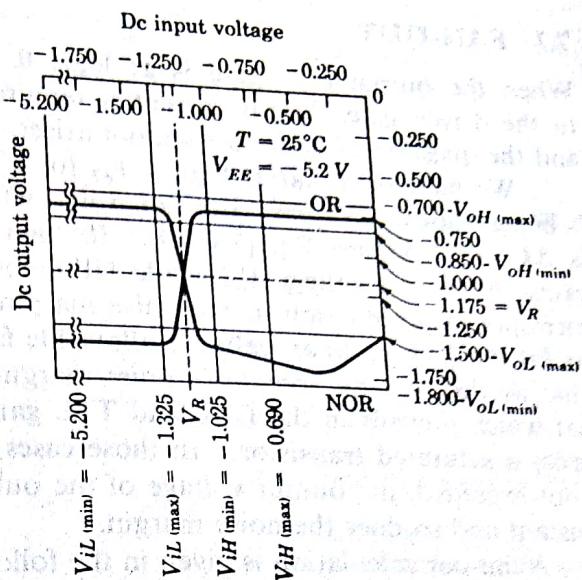


FIGURE 7.6-1  
Typical ECL transfer characteristics.

Motorola as typical, average transfer characteristics for the gate. There is generally good agreement between the plots of Fig. 7.6-1 and the derived transfer characteristic given in Fig. 7.4-1.

The maximum range of variability to be anticipated in these gates is indicated in Fig. 7.6-1. Thus, while the available output voltage  $V_{oH}$  is nominally  $-0.76$  V, the actual output may range from  $V_{oH}(\text{max}) = -0.70$  V to  $V_{oH}(\text{min}) = -0.85$  V. Similarly the output voltage  $V_{oL}$  ranges from  $V_{oL}(\text{max}) = -1.5$  V to  $V_{oL}(\text{min}) = -1.8$  V. The manufacturer specifies that an input voltage not more negative than  $V_{iH}(\text{min}) = -1.025$  V is guaranteed to be to the right of the transition region and hence to be acknowledged by the gate as corresponding to a logic 1 input. The  $\Delta 1$  margin, allowing for worst-case possibilities, is

$$\Delta 1 = V_{oH}(\text{min}) - V_{iH}(\text{min}) = -0.85 + 1.025 = 0.175 \text{ V} \quad (7.6-1)$$

rather than the typical value  $0.34$  V given in Eq. (7.4-10). Similarly, the worst-case  $\Delta 0$  margin is

$$\Delta 0 = V_{oL}(\text{max}) - V_{iL}(\text{max}) = 1.500 - 1.325 = 0.175 \text{ V} \quad (7.6-2)$$

The  $V_{iL}(\text{min}) = -5.2$  V is specified just to indicate that even if the most negative voltage available should happen to be impressed on the input, no disadvantage would result. The voltage  $V_{iH}(\text{max}) = -0.690$  V is so specified to indicate that a voltage in excess of this value will cause transistor  $T_1$  to carry an unnecessarily large current which will eventually produce saturation.

Notice again that it is required (to assure equal noise margins  $\Delta 0 = \Delta 1$ ) that the midpoints of the transition regions of the OR and NOR outputs occur at the coordinates  $V_i = V_R$  and  $V_{o2} = V_{o1} = V_R$ .

## 7.7 FAN-OUT

When the output of a gate is at logic 0, it need furnish no input current to the driven gate. Input current is required when the logic level is logic 1, and the question of allowable fan-out arises.

We have seen that at logic 1  $V_{o2}$  (or  $V_{o1}$ ) is at  $-0.76$  V when *no current* is being drawn. We have also noted that with  $V_i = -0.76$  the  $\Delta I$  noise margin is  $\Delta I = 0.34$  V [see Eq. (7.4-12)]. If, then, we fanned out to a number of gates, the output voltage  $V_{o2}$  would fall below  $-0.76$  V and there would be a corresponding reduction in the noise margin. Thus, in the present ECL case (as for the RTL gates as well) the allowable fan-out is a continuous function of what we decide is an acceptable noise margin. This situation is different from that which prevails in the DTL and TTL gates, where the outputs were taken across a saturated transistor. In those cases, as long as the allowable fan-out is not exceeded, the output voltage of the output transistor remains essentially constant and so does the noise margin.

A fan-out calculation is given in the following illustrative example.

**EXAMPLE 7.7-1** The output  $V_{o2}$  of the gate of Fig. 7.2-1 is to be fanned out to  $N$  similar gates, as shown in Fig. 7.7-1. Find  $N$  at room temperature if the  $\Delta I$  noise margin is to be 0.3 V. Assume the following worst-case conditions. The resistors of the driving stage are 20 percent higher than typical,  $R_{e2} = 300(1.2) = 360 \Omega$ , the emitter resistor  $= 1.5(1.2) = 1.8 \text{ k}\Omega$ ; the resistors of the driven stages are 20 percent lower than typical,  $R_e = 1.18(0.8) = 940 \Omega$ . The supply voltage is 10 percent high,  $V_{EE} = 5.2(1.1) = 5.7$  V. The transistors have current gains  $h_{FE} = 40$ . (These departures from typical values are all in the direction to reduce the fan-out.)

**SOLUTION** Refer to Fig. 7.7-1. At the edge of the transition region  $V_i = V_{o2} = -1.1$  V, as indicated in Fig. 7.4-1. This voltage value is not affected by the change in the value of  $R_e$ . If the noise margin is to be 0.3 V, we require that  $V_i = V_{o2} = -1.1 + 0.3 = -0.8$  V. Assuming, as usual, that  $V_{BEA} = 0.75$ , we have  $V_E = -0.8 - 0.75 = -1.55$  V,  $I_E = [-1.55 - (-5.7)]/940 = 4.4 \text{ mA}$  and

$$I_i = \frac{I_E}{h_{FE} + 1} = \frac{4.4}{41} = 107 \mu\text{A}$$

Turning now to the driving stage, we have  $V_{B4} = V_{o2} + 0.75 = -0.8 + 0.75 = -0.05$  V,  $I_{B4} = 0.05/360 = 139 \mu\text{A}$ ,  $I_{E4} = (h_{FE} + 1)I_{B4} = 41(139) = 5.7 \text{ mA}$ ,  $I_4 = [-0.8 - (-5.7)]/1.8 = 2.7 \text{ mA}$ , so that

$$I_o = I_{E4} - I_4 = 5.7 - 2.7 = 3 \text{ mA}$$

The fan-out is

$$N = \frac{I_o}{I_i} = \frac{3,000}{107} = 28$$

The number  $N = 28$  calculated in Example 7.7-1 is to be compared with  $N = 25$  given by the manufacturers as a "dc fan-out." On the other hand, if

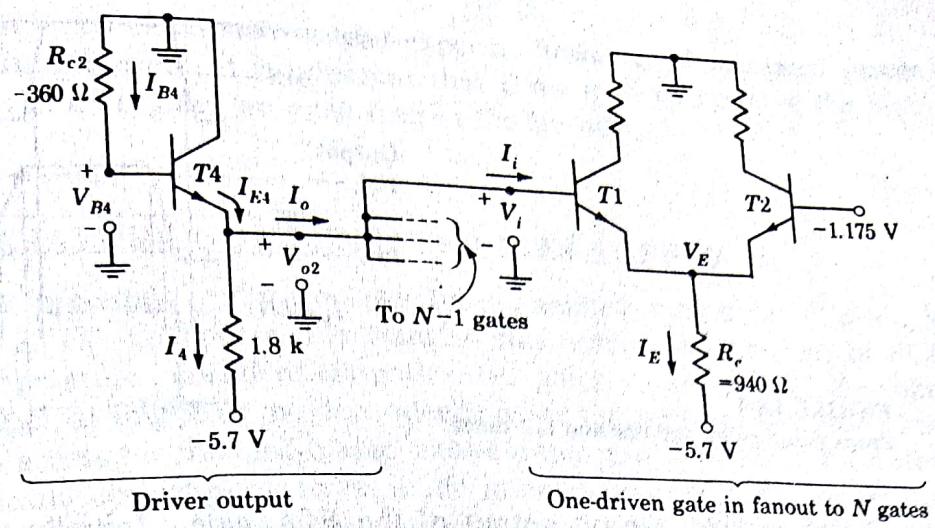


FIGURE 7.7-1  
A calculation of fan-out.

we allow  $\Delta V$  to fall to 0.1 V, then, as can be verified (Prob. 7.7-1),  $N$  becomes  $N \approx 250$ . In any event, it is apparent that fan-out in ECL gates is no problem if our only concern is the availability of enough driving current. However, the principal merit of ECL logic is its high speed. This speed is adversely affected by increasing the fan-out since each additional loading gate increases the loading capacitance correspondingly. Hence, the manufacturer specifies as well an "ac fan-out." This fan-out, usually about 15, is the fan-out recommended to keep rise and fall times and propagation times below specified limits.

## 7.8 SPEED OF OPERATION

Of all the gates considered, ECL is the fastest. When unloaded, a MECL II gate will exhibit a propagation delay time of the order of 4 ns. An even faster gate (MECL III) has a typical propagation delay time of about 1 to 2 ns. However, the speed of an ECL gate is adversely affected by capacitive loading. This situation is a result of the characteristic of the emitter followers used at the gate outputs. For, when the base voltage of an emitter follower changes sharply in the direction to increase emitter current, the emitter follows. Any capacitance hanging across the output charges rapidly through the low output impedance ( $\approx 6 \Omega$  in MECL II) of the emitter follower. When, however, the input changes in the reverse direction, the emitter voltage remains fixed momentarily due to the coupled capacitor. Since the base voltage has dropped, the emitter follower cuts off and the capacitance must discharge through the relatively large emitter resistance ( $-1.5 \text{ k}\Omega$  in Fig. 7.2-1). However, as we can now see, in the present ECL case, if the capacitive loading is moderate, the discharge time need not be excessively large because the logic levels are separated by a voltage difference which is small in comparison with the separation between the logic levels and the supply voltage.

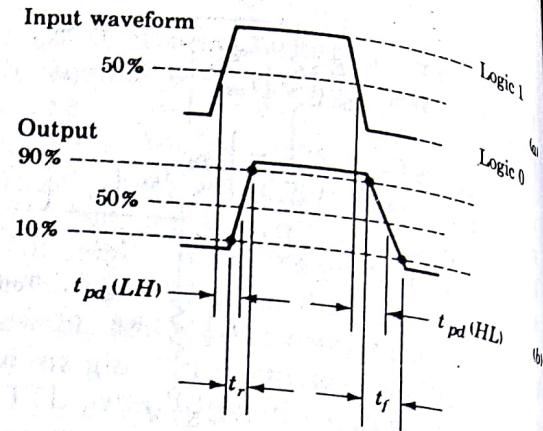


FIGURE 7.8-1  
Propagation delay and rise and fall times.

For consider the OR output of the ECL gate. Initially the output is at logic level 1 at  $V_{o2}(1) = -0.76$  V. When the emitter follower ( $T_4$  in Fig. 7.2-1) cuts off, the output starts to fall, heading asymptotically toward  $-V_{EE} = -5.2$  V. Logic level 0 is reached when the output voltage becomes  $V_{o2}(0) = -1.58$  V. The time  $T$  required to make the transition between logic levels can be shown to be

$$T = RC \ln \left[ \frac{V_{o2}(1) - (-V_{EE})}{V_{o2}(0) - (-V_{EE})} \right] \quad (7.8-1)$$

Using the values given above, we find that

$$T \approx 0.2RC \quad (7.8-2)$$

Assuming a capacitive load  $C = 5$  pF, we find  $T = 1.5$  ns.

Consider then a gate input as in Fig. 7.8-1a. With a substantial capacitive load on the gate output, the OR output would exhibit the characteristic to be noted in Fig. 7.8-1b, where the output falls more slowly than it rises. Propagation times in ECL gates are measured at a voltage midway between the two logic levels, the 50 percent point noted in the figures. We observe that the propagation time for a negative-going output  $t_{pd}(HL)$  is longer than  $t_{pd}(LH)$ , the propagation time for a positive-going output.

In MECL II, it turns out that the input capacitance of a gate averages about 3.3 pF. Allowing for the capacitance associated with wired interconnections, we reasonably consider that each added fan-out contributes 5 pF. At no fan-out, we find that  $t_{pd}(HL)$  and  $t_{pd}(LH)$  are about equal, each being approximately 3.5 ns. However, at a fan-out of 20, corresponding to a capacitive load of  $5(20) = 100$  pF, the manufacturer informs us that  $t_{pd}(LH)$  has increased to only about 5 ns while  $t_{pd}(HL)$  has increased to about 18 ns. Similarly, we find that at no fan-out, the rise and fall times  $t_r$  and  $t_f$  (see Fig. 7.8-1) are 6 and 4 ns, respectively. At a fan-out of 20,  $t_r$  increases to about 8 ns while  $t_f$  increases to about 30 ns. The times  $t_{pd}(HL)$  and  $t_f$  can be reduced, of course, by shunting the emitter resistor of the output emitter

follower by an external resistor, at the expense, however, of increased power dissipation. In any event, it is apparent that if we wish to preserve the high speed inherent in ECL gates we must restrict the fan-out.

### 7.9 TEMPERATURE-COMPENSATED BIAS SUPPLY

In all of the preceding discussion we have assumed operation at a single temperature, 25°C. Of course, the transfer and other characteristics of ECL gates are temperature-dependent, as with other gates. And, as with the other gates, the principal source of the dependence is the temperature variation of the voltage drop across the forward-biased base-emitter junctions of the transistors.

There is one special point to be made in connection with the temperature variation of an ECL gate, which we shall now consider. We noted earlier that the ECL gate was designed so that the  $\Delta 1$  and  $\Delta 0$  noise margins should be approximately equal. If the reference voltage  $V_R$  is kept fixed, this condition can apply at only a single temperature. It is possible, however, to supply a reference voltage which is itself temperature-dependent so as to ensure that the symmetry of the noise margins is maintained over a wide range of temperatures. The bias supply circuit which accomplishes this for MECL II gates, and which is often incorporated directly on the integrated-circuit chip, is shown in Fig. 7.9-1. The operation of the circuit is analyzed below.

Assuming that diodes  $D_1$  and  $D_2$  operate at a forward bias of 0.75 V, at a temperature  $T = 25^\circ\text{C}$ , we find (neglecting the base current in  $T_5$ ) that the base voltage of  $T_5$  is  $-0.425$  V. Assuming also a drop of 0.75 V from the base to emitter of  $T_5$ , we find that  $V_R = -0.425 - 0.75 = -1.175$  V, as expected.

Let us now assume a temperature change  $\Delta T$ . In this case each forward-biased junction voltage changes by the amount  $\delta = -k \Delta T$  ( $k = 2 \text{ mV}/^\circ\text{C}$ ). We calculate now the effect of such a change on the reference voltage  $V_R$  and on the output voltage levels  $V_o(1)$  and  $V_o(0)$  corresponding to logic 1 and logic 0

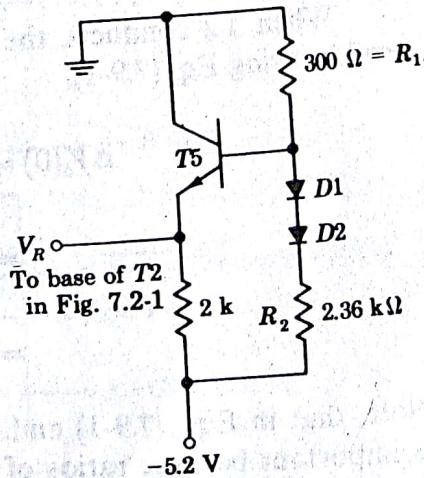


FIGURE 7.9-1  
Reference supply circuit for ECL gates.

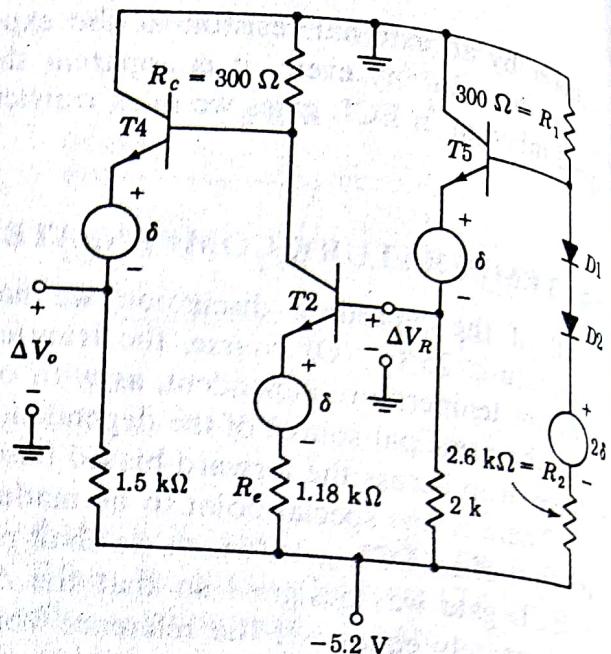


FIGURE 7.9-2

Equivalent circuit for calculating effect of temperature variation.

levels of the OR output (a calculation for the NOR output is left for the problems). The circuit of Fig. 7.9-2 includes the bias supply of Fig. 7.9-1 and that part of the gate circuit of Fig. 7.2-1 which generates the OR output. For ease of identification, the transistors in Fig. 7.9-2 have been given the same designations as in Figs. 7.2-1 and 7.9-1. Generators ( $\delta$  and  $2\delta$ ), representing the *voltage increments* introduced into the circuit due to a temperature change, have also been included.

Assuming that the gain through the emitter follower ( $T_5$ ) is unity, we calculate the change in reference voltage  $V_R$  to be

$$\begin{aligned}\Delta V_R &= \frac{2\delta R_1}{R_1 + R_2} - \delta = \delta \left( -1 + \frac{2}{1 + R_2/R_1} \right) \\ &= \delta \left( -1 + \frac{2}{1 + 2.36/0.3} \right) \approx -0.77\delta\end{aligned}\quad (7.9-1)$$

When  $T_2$  conducts, the output is at logic level 0. The increment in this level is, using Eq. (7.9-1),

$$\begin{aligned}\Delta V_o(0) &= -\Delta V_R \frac{R_c}{R_e} + \delta \frac{R_c}{R_e} - \delta \\ &= (0.77\delta + \delta) \frac{R_c}{R_e} - \delta \\ &= \left( 1.77 \frac{0.3}{1.18} - 1 \right) \delta = -0.55\delta\end{aligned}\quad (7.9-2)$$

Note, that in Eqs. (7.9-1) and (7.9-2) only resistor ratios appear. This feature is important because ratios of resistors can be held to much tighter tolerances

( $\approx 2$  percent) than the absolute values of resistors ( $\approx 20$  percent). Finally when  $T_2$  is cut off and the output is at logic level 1, the corresponding increment is

$$\Delta V_o(1) = -\delta \quad (7.9-3)$$

From Eqs. (7.9-2) and (7.9-3) we can now calculate that the average increment of the two logic levels is

$$\frac{\Delta V_o(1) + \Delta V_o(0)}{3} = \frac{-\delta - 0.55\delta}{2} \approx -0.77\delta \quad (7.9-4)$$

which is equal to the increment  $\Delta V_R$  given by Eq. (7.9-1). Thus, as the temperature changes, the midpoint of the range from logic 0 to logic 1 changes by the same amount as the reference voltage  $V_R$ .

Since the reference voltage lies midway between the two output-voltage levels, independently of the temperature variation, the  $\Delta 1$  and  $\Delta 0$  noise immunities are the same. This therefore maximizes the noise immunity. However, the noise immunity does change with temperature (Prob. 7.9-2). Further, the above analysis neglected the effect of fan-out. It can be shown (see Prob. 7.9-3) that the result is relatively independent of fan-out.

The bias supply of Fig. 7.9-1 also provides a measure of compensation for variations in the supply voltage  $-V_{EE}$ . However, the compensation is not as exact as for temperature variations (see Prob. 7.9-5).

## 7.10 LOGIC VERSATILITY OF ECL GATES

As with DTL logic, it is possible to extend the logic capabilities of ECL gates simply by connecting the gate outputs together. For example, it can readily be verified that two or more emitter followers, operating into a common load,

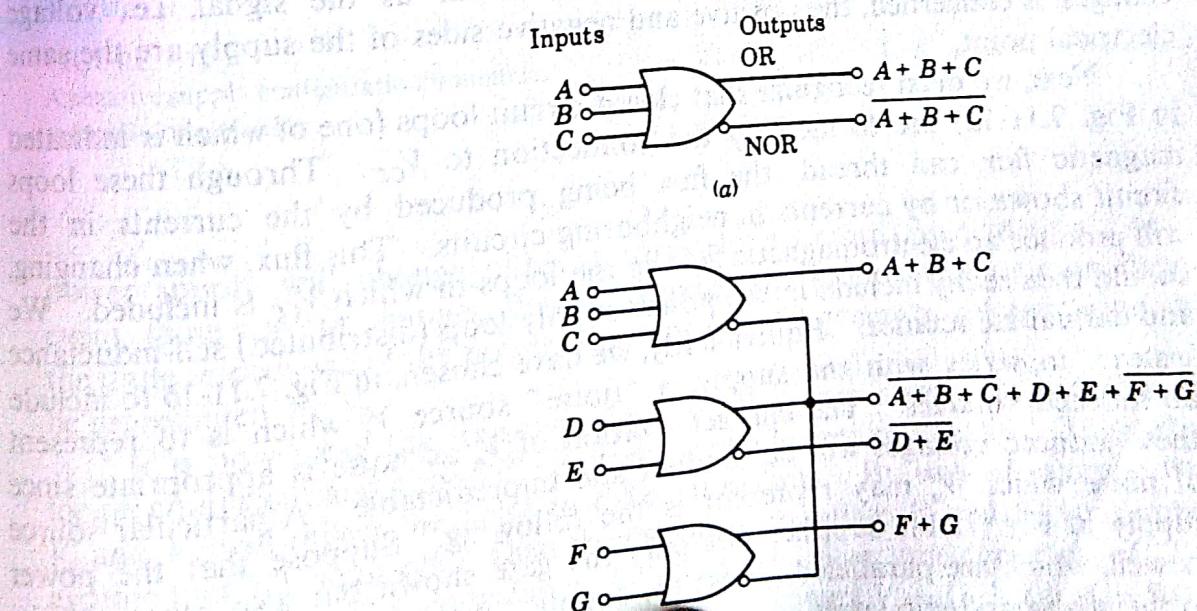


FIGURE 7.10-1  
The WIRED-OR connection

constitute an OR gate for positive logic. Hence, if the outputs of ECL gates are joined, this connection provides the logical sum (OR operation) of the outputs that would otherwise appear at the individual gates. Such a connection is therefore referred to as the WIRED-OR connection.

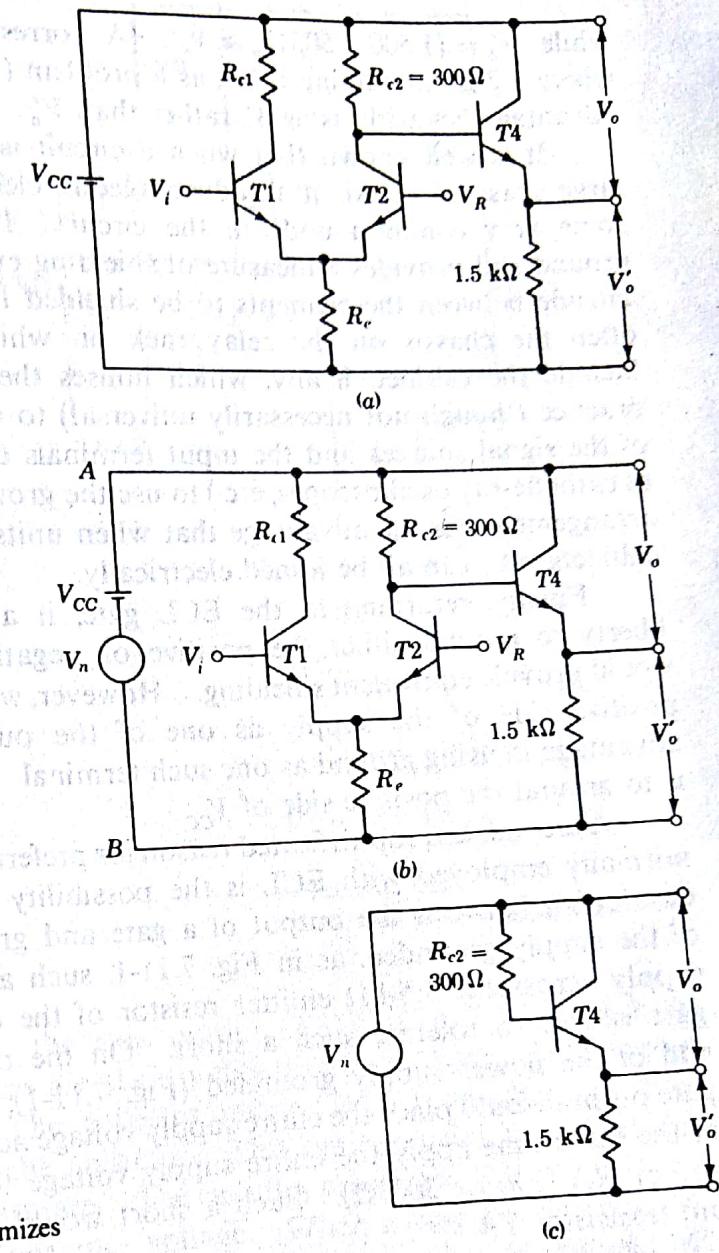
An example of the WIRED-OR connection is shown in Fig. 7.10-1. In Fig. 7.10-1a is shown the symbol for the ECL gate. Two outputs are shown. However, as a matter of convenience and to allow greater fan-out, some commercially available gates are provided with multiple OR and multiple NOR outputs. On the other hand, some gates are provided with only one OR and one NOR output. Figure 7.10-1b shows a WIRED-OR connection involving both OR and NOR outputs.

## 7.11 THE NEGATIVE SUPPLY VOLTAGE

In RTL, DTL, and TTL gates, the negative end of the power-supply voltage is grounded. In ECL gates, as we have noted, it is common practice to ground the positive end of the supply. We consider now the advantages of such an arrangement with ECL gates.

Let us initially put aside the question of grounding entirely and address ourselves to another matter. In Fig. 7.11-1 we have drawn an ECL gate. (To simplify the drawing we have omitted the part of the gate that provides the NOR output. This simplification will have no bearing on our discussion.) A supply voltage  $V_{cc}$  has been bridged across the gate. It has been our practice to consider that the output voltage of the gate is the voltage  $V_o$  taken between the emitter of  $T_4$  and the positive side of the power supply. But it readily appears that no fundamental change would be involved if we had chosen instead to take as the output voltage the voltage  $V'_o$  between emitter and negative side of the supply. As a matter of fact, as far as the signal, i.e., voltage changes, is concerned, the positive and negative sides of the supply are the same electrical point.

Next, we must recognize that closed-circuit loops (one of which is indicated in Fig. 7.11-1a) are formed by the connection to  $V_{cc}$ . Through these loops magnetic flux can thread, the flux being produced by the currents in the circuit shown or by currents in neighboring circuits. This flux, when changing, will produce an electromagnetic field in the loops in which  $V_{cc}$  is included. We should then really include in the power-supply loop (distributed) self-inductance and mutual inductance. Equivalently, we have chosen, in Fig. 7.11-1b to include instead, in series with the supply, a "noise" source  $V_n$  which is to represent all induced voltages. The characterization of  $V_n$  as noise is appropriate since these induced voltages will be random and unpredictable. A particular source of noise which  $V_n$  may represent is the following. Suppose that the power supply in Fig. 7.11-1 supplies not only the gate shown but also other circuits as well, which are paralleled across the supply. As these other circuits respond to the changing logic levels of their input signal, the current they draw from the



**FIGURE 7.11-1**  
A negative supply configuration minimizes external-noise transfer.

power supply will change either transiently or more permanently. In any event, these current changes, flowing through the inductances or even through the finite impedance of the power supply itself, will generate voltages which may be represented by  $V_n$ .

It is now clear that the two sides of the power supply  $A$  and  $B$  are no longer equivalent and  $V_o$  and  $V'_o$  similarly are no longer equivalent. The voltages  $V_o$  and  $V'_o$  will reflect the noise to different extents. By way of example let us assume that  $T_2$  is cut off. Then the circuit to calculate  $V_o$  and  $V'_o$  is as appears in Fig. 7.11-1c. The impedance between collector and emitter of  $T_4$  is  $R_{c2}/(h_{FE} + 1) = 300/100 = 3\Omega$  for  $h_{FE} = 99$ . Hence,  $V_o = (3/1,500)V_n = 0.002V_n$

$$R_{c2}/(h_{FE} + 1) = 300/100 = 3\Omega \text{ for } h_{FE} = 99$$

while  $V'_o = (1,500/1,503)V_n \approx V_n$ . [A corresponding calculation for the case where  $T2$  is conducting is left as a problem (Prob. 7.11-2).] It is clear that the advantage lies with using  $V_o$  rather than  $V'_o$ .

It is well known that when a circuit is to operate in the proximity of a large mass of metal, it is advantageous electrically to connect this mass to some very common node in the circuit. The metal is then referred to as ground and provides a measure of shielding even though it need not physically intrude between the elements to be shielded from each other. This ground is often the chassis on the relay rack on which the circuit is built and will include the cabinet, if any, which houses the unit. It is also very common practice (though not necessarily universal) to arrange for the output terminals of the signal sources and the input terminals of signal-measuring devices (such as cathode-ray oscilloscopes, etc.) to use the ground as one signal terminal. This arrangement has the advantage that when units are interconnected, the chassis, cabinets, etc., can all be joined electrically.

Finally, returning to the ECL gate, it appears that we are initially at liberty to ground either the positive or negative side of the supply. Either would provide equivalent shielding. However, we find an advantage in using the positive side of the supply as one of the output terminals and a further advantage in using ground as one such terminal. Hence, altogether the practice is to ground the positive side of  $V_{CC}$ .

A second, less sophisticated reason for preferring the grounding arrangement normally employed with ECL is the possibility of an accidental short circuit developing between the output of a gate and ground. With the positive end of the supply grounded, as in Fig. 7.11-1, such a short places the entire 5.2-V supply across the 1.5-k $\Omega$  emitter resistor of the output emitter follower. The gate is able to tolerate such a short. On the other hand, with the negative end of the power supply grounded (Fig. 7.11-1), a short to ground from the gate output would place the entire supply voltage across the output transistor and at the same time apply the entire supply voltage to the transistor base through  $R_{c1}$  or  $R_{c2}$  (290 or 300  $\Omega$ ). Such a short would promptly overheat and burn out transistor  $T4$ .

## 7.12 LEVEL TRANSLATION

It is often necessary to interconnect two different logic systems such as ECL and TTL (or DTL). One such application is the time-division multiplexing of  $M$  digital signals to form a single digital signal. Although the bit rate of each of the  $M$  signals may be handled using TTL, the bit rate of the composite signal is  $M$  times faster and may require ECL to process it.

**Saturated logic to ECL translation** The circuit of a commercial unit used to translate from saturated logic (TTL or DTL) to ECL is shown in Fig. 7.12-1. The circuit involving  $T1$ ,  $T2$ , and  $T4$  is recognized as the ECL gate in which

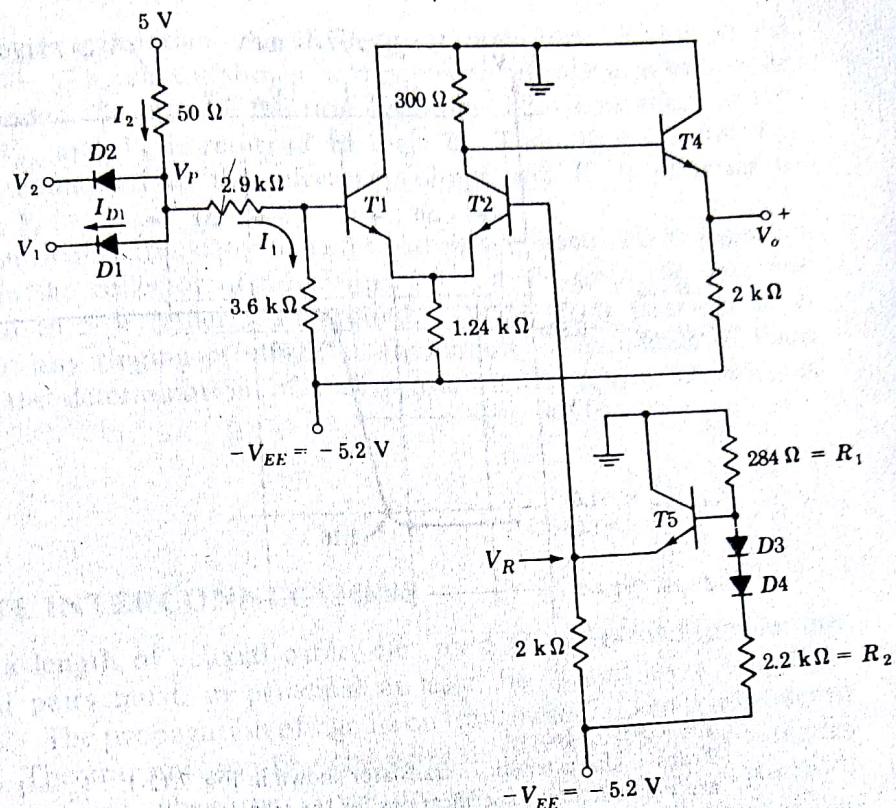
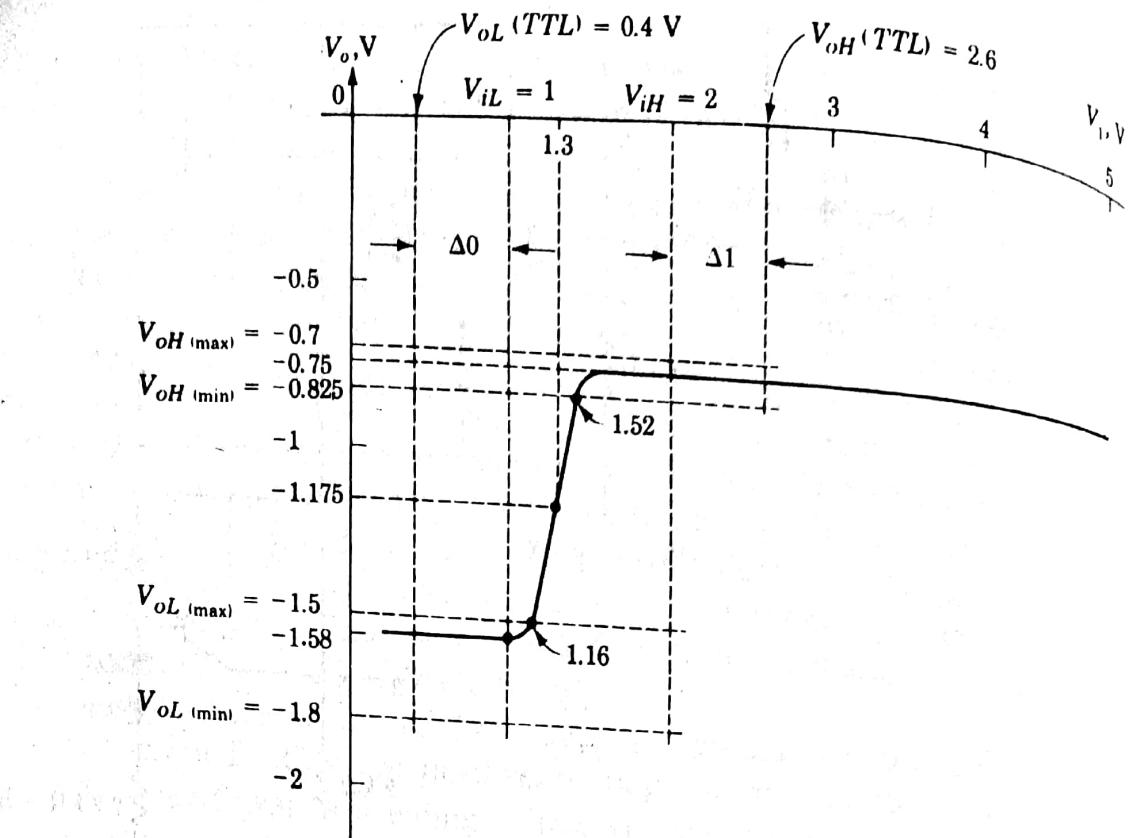


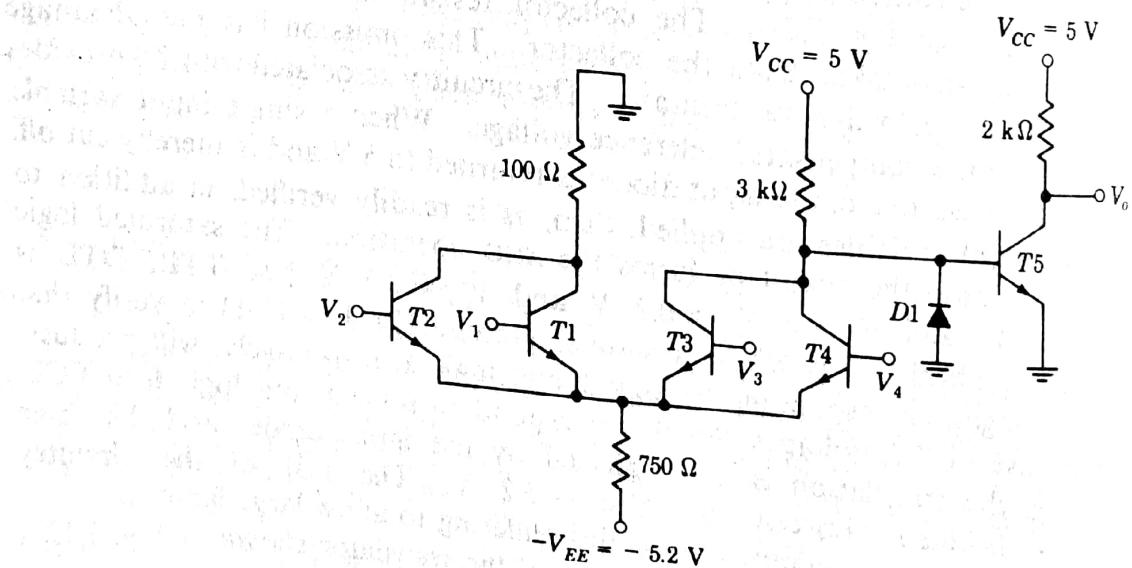
FIGURE 7.12-1  
Saturated logic-to-ECL translator.

the transistor used to provide the NOR output ( $T_3$  in Fig. 7.2-1) has been omitted. The component values are slightly different from those which appear in the circuit of Fig. 7.2-1. The collector resistor of  $T_1$  has been omitted since no signal is taken from the collector. This omission has the advantage of assuring that  $T_1$  will never saturate. The circuitry associated with  $T_5$  provides the temperature-compensated reference voltage. When a single input variable is to be handled, one of the input diodes is returned to 5 V and is thereby cut off. If two logical variables are applied, then, as is readily verified, in addition to level translation the circuit performs the AND operation. The saturated logic levels of  $V_1$  and  $V_2$  are  $V_{oL} \approx 0.2$  V and  $V_{oH} \approx 3.5$  V (for TTL; DTL is generally higher). It is left as a student exercise (Prob. 7.12-1) to verify that these voltages, corresponding to logic 0 and logic 1, respectively, will produce, at the base of  $T_1$ , voltages, which correspond to logic 1 and logic 0 in ECL. Actually, the translation is accomplished by the input diodes and the three resistors bridged between +5 and -5.2 V. The rest of the circuitry provides temperature compensation and buffering to allow large fan-out.

The resulting transfer characteristic of the translator shown in Fig. 7.12-1 is given in Fig. 7.12-2.

**FIGURE 7.12-2**

Transfer characteristic of translator shown in Fig. 7.12-1.  $V_{iL} = 1$  V and  $V_{iH} = 2$  V are manufacturer's specifications for the translator.

**FIGURE 7.12-3**  
ECL-to-saturated-logic translator.

**ECL-to-saturated-logic translation** An ECL-to-saturated-logic translator is shown in Fig. 7.12-3. The circuit shown is capable of operating in either the OR or NOR logic mode. To provide the NOR operation  $V_4$  is connected to the reference voltage  $V_R$ , and  $V_3$  is returned to logic 0. Then  $V_0 = V_1 \text{ NOR } V_2$ . Similarly, if  $V_2$  is connected to the reference voltage and  $V_1$  is returned to logic 0,  $V_0 = V_3 \text{ OR } V_4$ .

The operation of this translator is rather straightforward, the translation being performed in the collector of transistors  $T3$  and  $T4$  since the collector resistor is returned to 5 V rather than ground. Diode  $D1$  is inserted, as in TTL, to damp out any ringing produced in the circuit. The details of these calculations and the determination of the transfer function are left for the problems.

### 7.13 ECL-GATE INTERCONNECTIONS

A pair of wires, a length of coaxial cable, etc., used to make interconnections between terminal pairs must, in principle at least, be viewed as a length of transmission line. The propagation of signals on transmission lines is considered in Appendix A. The transmission-line character of the interconnection makes itself especially apparent when the waveforms encountered make transitions between levels in times which are comparable to the time of propagation along the line. When the transition times are long in comparison to the time of propagation along the line, the line can be approximated by lumped-circuit elements.

Consider, then, the connection of the output of a driving ECL gate to the input of a driven gate. The emitter-follower driver has a low output impedance ( $< 10 \Omega$ ) while the input impedance of the driven gate may well be of the order of many thousands of ohms. In Appendix A, we consider the characteristic impedance of interconnecting wires of geometries such as might reasonably be found in electronic circuitry. We estimate that such impedance would be in the range of some tens to some hundred of ohms. Hence, as indicated in Fig. 7.13-1a, the interconnection between gates may reasonably be represented by a line of one-way delay  $t_d$  and characteristic impedance  $R_0$ . The sending-end termination is  $R_s \ll R_0$ , and the receiving-end termination is  $R \gg R_0$ .

If the input to the line  $V_i$  makes an abrupt transition between voltage levels, as indicated by the dashed waveform in Fig. 7.13-1b, the output  $V_o$  has the damped oscillatory waveforms shown by the solid plot. It is thus apparent that a transition at the driver-gate output from logic 0 to logic 1 might be interpreted at the driven gate as a sequence of several such transitions. If, on the other hand, the input waveform makes its transition in a time which is rather long in comparison with  $t_d$ , then, as shown in Fig. 7.13-1c, the output follows the input more closely; the oscillations of  $V_o$  about  $V_i$  are not nearly so pronounced.

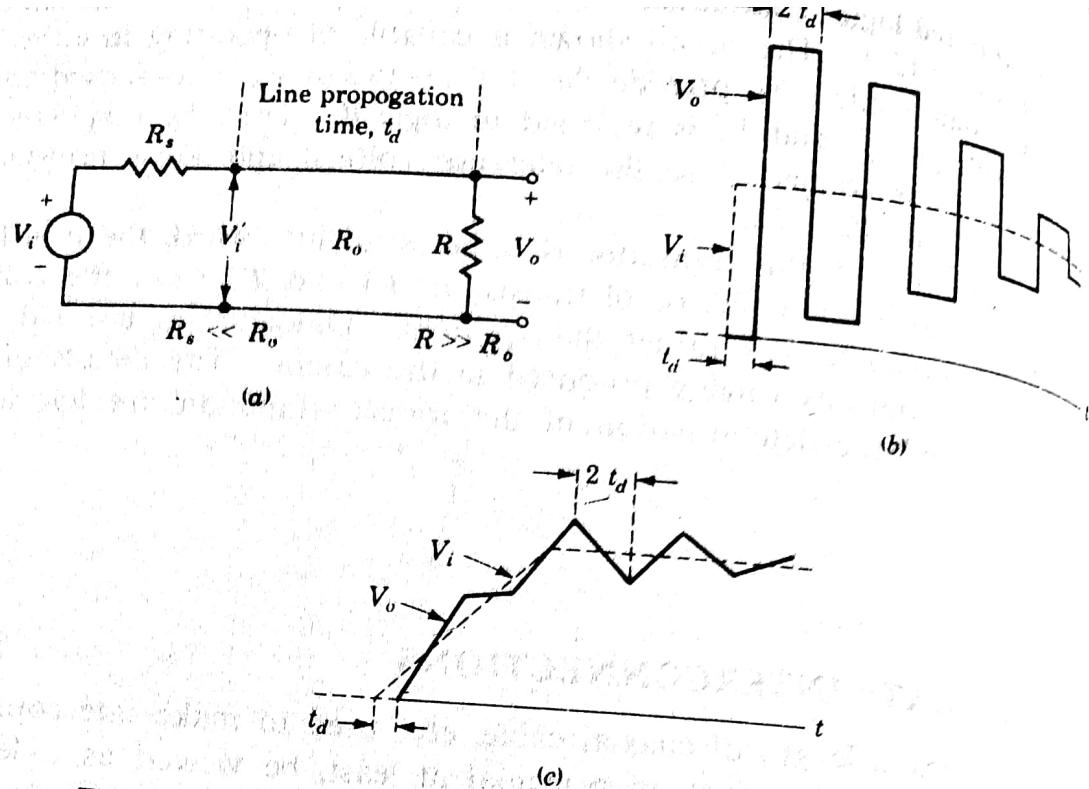


FIGURE 7.13-1

(a) A line of delay time  $t_d$  and characteristic impedance  $R_0$ . It is terminated at its sending end in  $R_s \ll R_0$  and at its receiving end in  $R \gg R_0$ . (b) The response at the output for a step input. (c) The response for an input ramp which rises in a time long in comparison with  $t_d$ .

We have already noted oscillations of the type indicated in Fig. 7.13-1b in connection with TTL gates (see Sec. 6.12). In ECL the problem is even more urgent because of its higher speed. Transition times between logic levels of the order of 1 ns may occur in ECL. Depending on the dielectric constant of the insulation used to support the lines, 1-ns delays may occur in lines only 4 to 6 in long.

The oscillations can be suppressed by terminating the line at its receiving end in its characteristic impedance. In the absence of such termination, for an input logic swing of fixed rise time, the oscillation becomes more pronounced as the line gets longer. For this reason manufacturers generally provide guidance concerning the maximum allowable unterminated line lengths. This allowable length depends on the rise time, the fan-out, the characteristic impedance of the line, and the propagation time delay per unit length of line. By way of example, for Motorola type MECL 10,000, which has a rise time of 3.5 ns, using a microstrip line with  $R = 50 \Omega$ , and with a fan-out of 1, the allowable length is 8.3 in. For Motorola type MECL III, which has a rise time of 1 ns, using again a microstrip line except with  $R_0 = 100 \Omega$  and with a fan-out of 8, the allowable length is only 0.1 in.

A transmission-line interconnection between gates is indicated in Fig. 7.13-2.

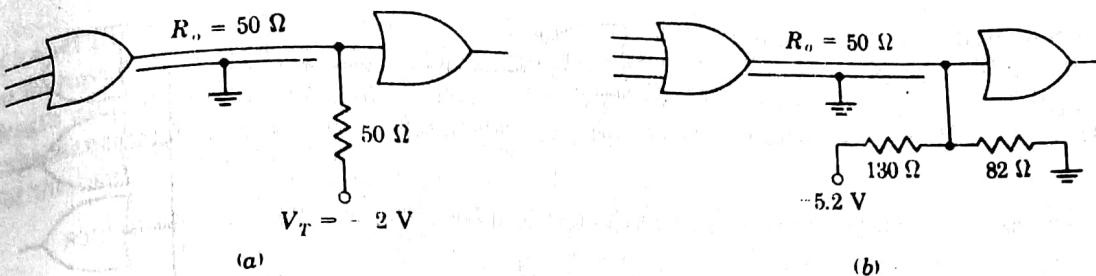
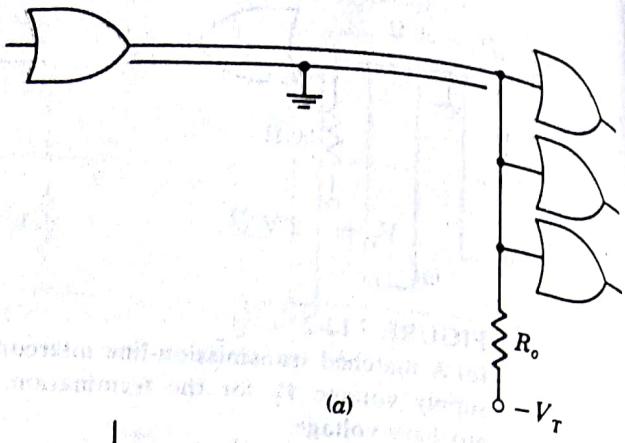


FIGURE 7.13-2

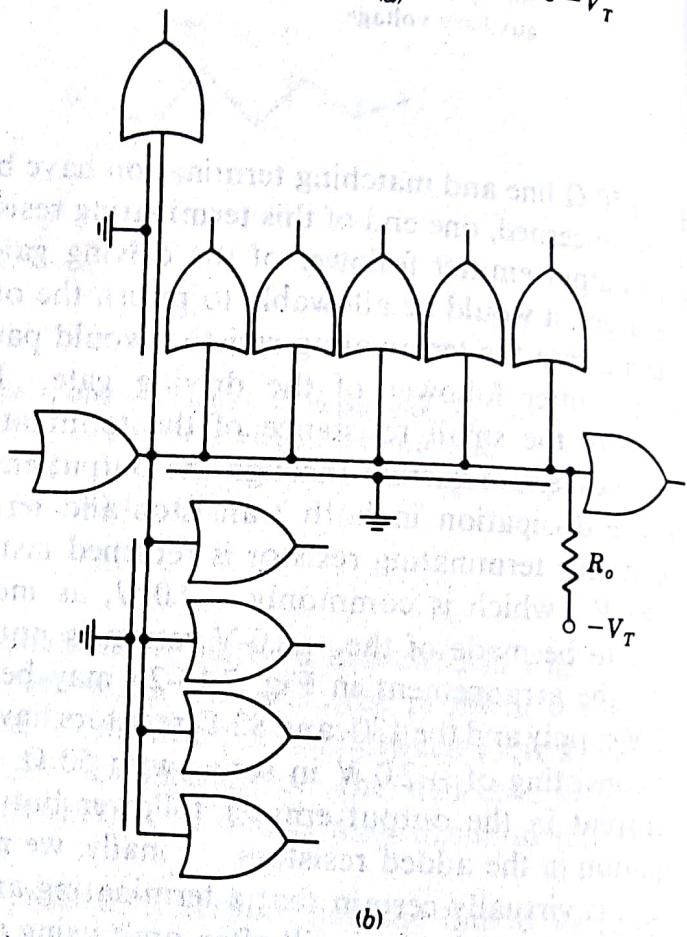
(a) A matched transmission-line interconnection between gates using an auxiliary supply voltage  $V_T$  for the termination. (b) An arrangement which avoids the auxiliary voltage.

Here a 50- $\Omega$  line and matching termination have been used. As far as dc operation is concerned, one end of this terminating resistor is connected to the emitter of the output emitter follower of the driving gate. If this terminating resistor were larger, it would be allowable to return the other end to the -5.2-V supply. In such a case the terminating resistor would parallel the emitter resistor of the output emitter follower of the driving gate. In the present case, however, because of the small resistance of the termination, such a connection would result in excessive current through the output emitter follower, with consequent excessive dissipation in both transistor and termination. To circumvent this difficulty the terminating resistor is returned instead to an auxiliary terminating voltage  $V_T$ , which is commonly -2.0 V, as indicated in Fig. 7.13-2a. When the use to be made of the -2.0-V return is not adequate to justify a separate supply, the arrangement in Fig. 7.13-2b may be used. As can be verified, the -5.2-V supply and the 130- and 82- $\Omega$  resistors have a Thevenin equivalent replacement consisting of -2.0 V in series with 50  $\Omega$ . This latter arrangement limits the current in the output emitter follower but at the expense of considerable dissipation in the added resistors. Finally, we may note that in fast ECL gates, where it is virtually certain that a terminating arrangement as in Fig. 7.13-2 will be used, the manufacturer will often omit using an emitter resistor in the driving gate. In any event the output current diverted into the termination, and hence not available to drive gates, must be taken into account in estimating the allowable fan-out.

In Fig. 7.13-3 are shown a number of ways in which we can arrange the geometry of fan-out. In Fig. 7.13-3a all the driven gates are physically mounted very close to one another and are paralleled at the receiving end of a matched transmission line. In Fig. 7.13-3b the driving gate drives three transmission lines, two unmatched and one matched. The unmatched lines must be restricted in length in accordance with manufacturer's recommendations. In a representative case in an arrangement as in Fig. 7.13-3b we find with Motorola MECL III logic, using 50- $\Omega$  microstrip lines, the unterminated line with a fan-out of 1 may be no longer than 1.6 in. The other unterminated line, with a fan-out of 4 and



(a) Driven gates lumped at the end of a matched line.



(b)

FIGURE 7.13-3

Fan-out arrangements for ECL gates: (a) the driven gates lumped at the end of a matched line; (b) gates distributed along matched and unmatched lines.

the load gates distributed nominally uniformly along the length of the line, the total length of the line may be no longer than 0.7 in.

In Fig. 7.13-3b the loads supplied by the matched line are distributed along the length of the line. A special consideration to be taken into account in connection with such an arrangement is discussed in the following illustrative example.

**EXAMPLE 7.13-1** The matched line in Fig. 7.13-3b is 9 in long and drives 6 gates spaced at multiples of 1.5 in from the input end of the line. The line has capacitance per unit length and inductance per unit length  $C = 2 \text{ pF/in}$  and  $L = 0.02 \mu\text{H/in}$ . The input capacitance of a gate is 5 pF. Estimate the value of the resistive termination required for the line.

**SOLUTION** Using Eq. (A.1-4), we find that the characteristic impedance of the line is

$$R_0 = \sqrt{\frac{L}{C}} = \sqrt{\frac{0.02 \times 10^{-6}}{2 \times 10^{-12}}} = 100 \Omega$$

The six gates have a total input capacitance of  $6(5) = 30 \text{ pF}$ . Since the length of the line is 9 in, the gates add a capacitance per unit length  $C' = 30/9 = 3.3 \mu\text{F/in}$ . If this added capacitance were uniformly distributed along the line, the line impedance would be given exactly by Eq. (A.1-4) with  $C$  replaced by  $C + C'$ . While such is not the case, we may well expect that this replacement will nonetheless yield a good approximation. We then find

$$R_0 = \sqrt{\frac{0.02 \times 10^{-6}}{5.3 \times 10^{-12}}} = 61 \Omega$$

The propagation delay per unit length [the inverse of the velocity in Eq. (A.1-5)] is

$$t_{pd} = \sqrt{L(C + C')} = \sqrt{(0.02 \times 10^{-6})(5.3 \times 10^{-12})} \approx 0.3 \text{ ns/in}$$

**Series termination** A line terminated at its receiving end is referred to as a *parallel-terminated line* since, as can be seen in Fig. 7.13-1, the matching resistor  $R$  is bridged across the line. A line may alternatively be matched at its input end by selecting  $R_s = R_0$  in Fig. 7.13-1, in which case the line is referred to as a *series-terminated line*. It is feasible to provide such input matching, for the output impedance of a gate (see Fig. 7.2-1) is approximately  $R_{c2}/h_{FE} = \frac{300}{50} = 6 \Omega$ . We have noted that the line impedances are in the range 50  $\Omega$  to several hundred ohms. Hence, matching allows for the insertion of an additional resistor  $R_s$  in series with the output of the driving gate, as indicated in Fig. 7.13-4. Observe that series matching has the advantage that no auxiliary supply voltage is required. On the other hand, the series resistor limits the available output current and thereby restricts the fan-out to about 10.

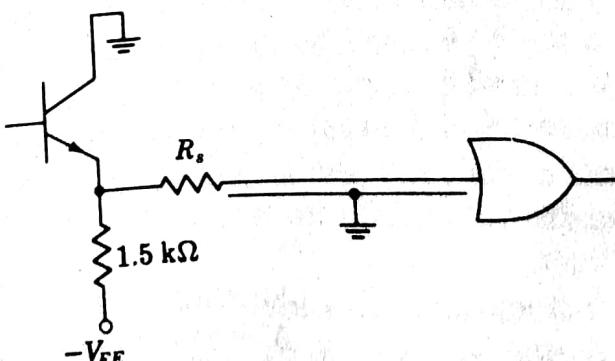


FIGURE 7.13-4  
A line matched at its input end.

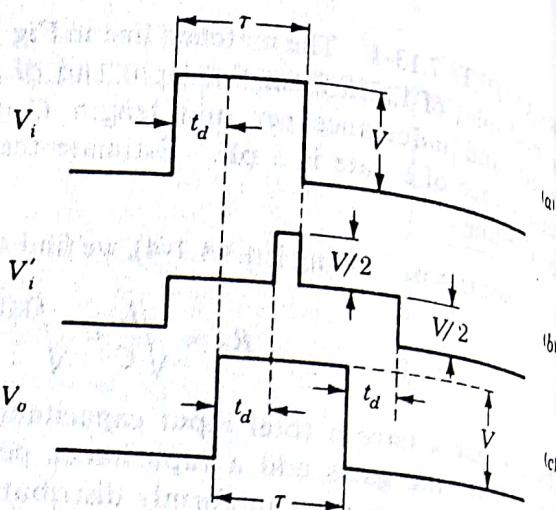


FIGURE 7.13-5

(a) A pulse of duration  $\tau$  is applied to a line matched at its input end and open at its receiving end. Also shown is the waveform (b) at the input end and (c) at the receiving end of the line.

When driven gates are strung out on a parallel-terminated line, some difficulty may arise because signals from the driver arrive at different gates at different times. In series-terminated gates, of course, a similar situation prevails. However, an additional difficulty arises when employing the series-terminated line which does not occur in the parallel-terminated gate. Consider that in Fig. 7.13-1a,  $R_s = R_0$ ,  $R = \infty$ , and  $V_i$  has the form indicated in Fig. 7.13-5a; that is, the driving gate changes its logic level, but the change persists only for a time  $\tau$ . Suppose further that one of the driven gates is located at the input side of the

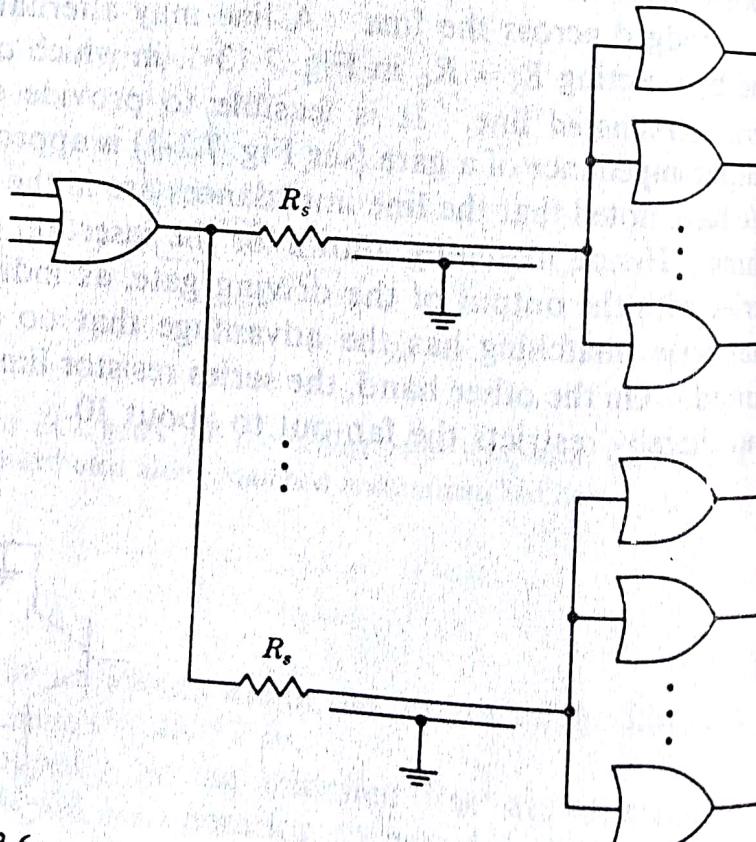


FIGURE 7.13-6

A number of series-matched lines used to accommodate a large fan-out.

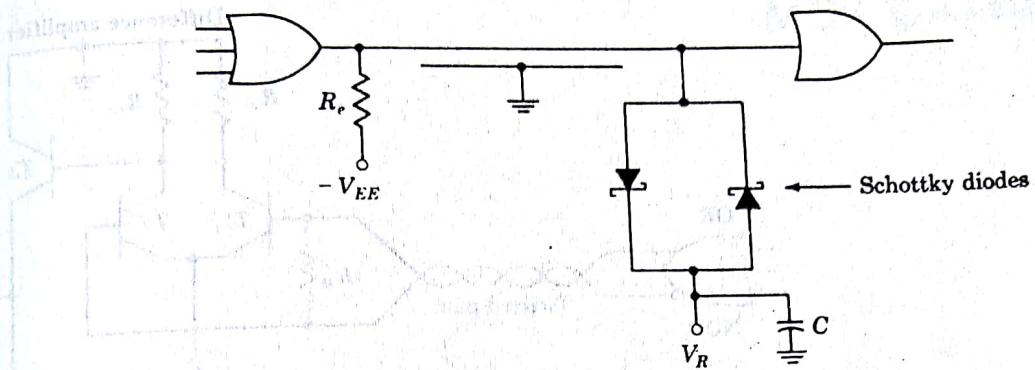


FIGURE 7.13-7  
Diode termination of a line.

line, where the voltage is  $V'_i$ . It is left as a problem (Prob. 7.13-3) to verify that the input waveform and the waveform at the end of the line are given as in Fig. 7.13-5. We have drawn the waveforms for  $\tau = 2.5t_d$ ,  $t_d$  being the one-way delay of the line. Note that the change in level in  $V_o$  persists for the same time  $\tau$  as in  $V_i$  although there is a relative delay  $t_d$ . On the other hand, in  $V'_i$ , the full change persists only for a time  $\tau - 2t_d$  and develops only after a time delay  $2t_d$ . If then it should happen that  $\tau \leq 2t_d$ , the full change in level would never appear in  $V'_i$ . The difficulty can be relieved by arranging the spacing between driven gates to be small in comparison with the spacing of the gates from the input side of the line. When many driven gates must be accommodated, the configuration of Fig. 7.13-6 is effective. Here a number of parallel lines are used, each with its own series termination.

**Diode termination** An additional method of suppressing oscillations is indicated in Fig. 7.13-7. This method is a rather natural extension of the use of input diodes, encountered earlier in connection with TTL gates. Of course, Schottky diodes are called for. We have noted that the ECL levels symmetrically straddle the reference voltage (see Fig. 7.6-1). Hence, the diodes are returned to this reference voltage  $V_R$ . Schottky diodes which have a cut-in voltage  $V_y \approx 0.3$  V would allow the line voltage to swing freely through the range  $V_R \pm V_y$ , while oscillations outside this range would be sharply damped.

**Twisted pair lines** A second difficulty associated with the transmission of ECL waveforms is *crosstalk*, or unintended coupling of signals between circuits. Because of the speed of the signals, a large signal may be coupled from one signal path to another by a small stray capacitance or mutual inductance. Crosstalk can, of course, be minimized by using coaxial cables, but such cables are bulky and certainly do not readily allow a distribution of taps for driven gates.

A feature of ECL gates which is of great use in suppressing crosstalk is the fact that gates have two outputs (OR and NOR) which are of opposite polarity.

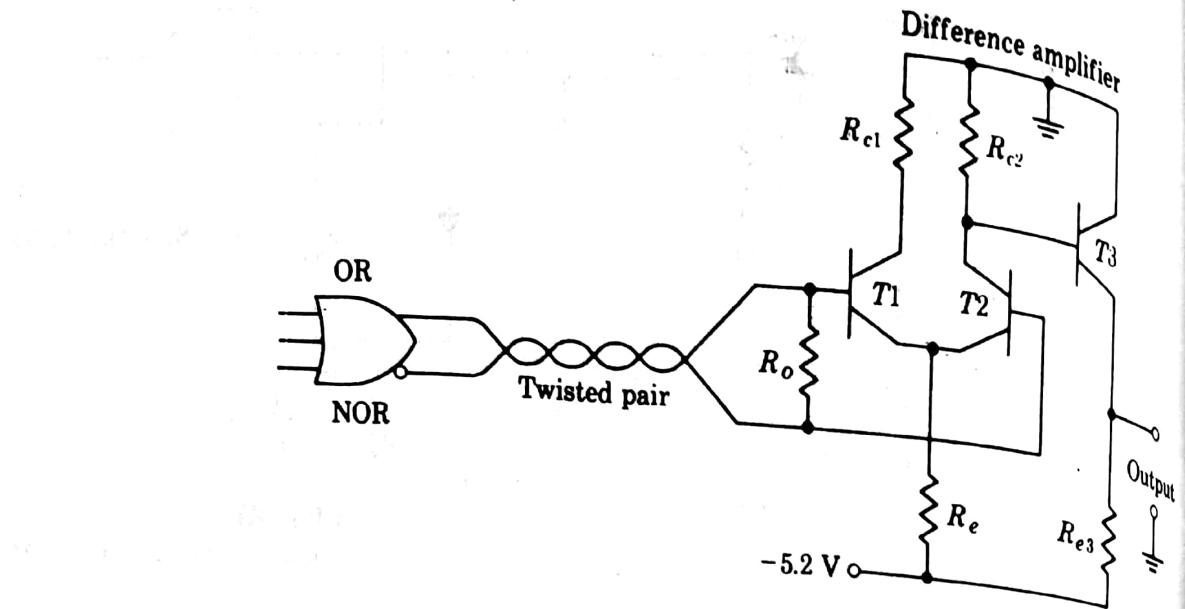


FIGURE 7.13-8  
Twisted-pair transmission in ECL

Whatever the change in voltage at one output, the change at the other output is equal and opposite. We take advantage of this feature as indicated in Fig. 7.13-8. The *difference* in output between OR and NOR output is transmitted over a twisted pair of wires to a *difference amplifier*. This difference voltage is nominally twice as large in amplitude as the signal available from the OR or the NOR output separately. The difference amplifier is normally made available by manufacturers for the present purpose and is generally referred to as a *receiver*. The twisting of the transmission wires keeps the wires together and also regularly reverses their relative positions. Hence, any signal path which might have induced in it a signal from one of the wires in the pair may well be expected to have an equal and opposite signal induced by the other wire. Hence, crosstalk from the twisted pair to other signal paths may be expected to be minimal. Similarly, crosstalk of other signals to the twisted pair will be introduced into the difference amplifier as a *common-mode* signal and hence will largely be restrained from appearing at the single-ended output. Of course, as appears, the twisted pair must be matched at its receiving end. A twisted pair may be used for transmission over many feet and may be used to distribute commonly used signals (such as clock waveforms) to many points. Generally, at each point when the signal is to be picked off the pair, a receiver will be required.

## REFERENCE

- 1 Blood, W. R., Jr.: "MECL System Design Handbook," Motorola Semiconductor Products, Inc, Phoenix, Ariz., October 1971.