VSLI Lab Report

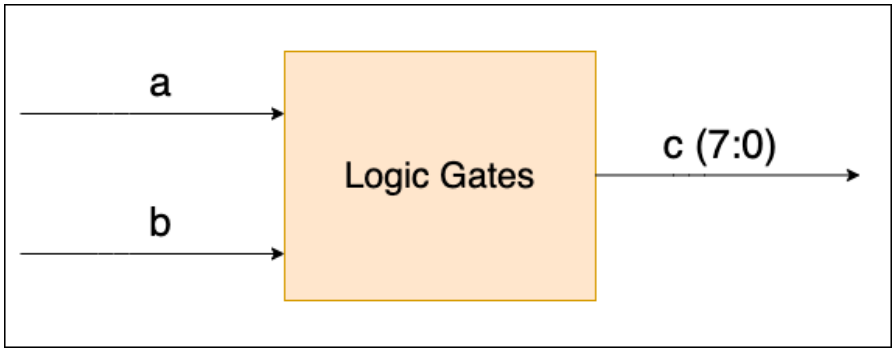
Assignment 1

Md Sahil
Roll- 001710501029

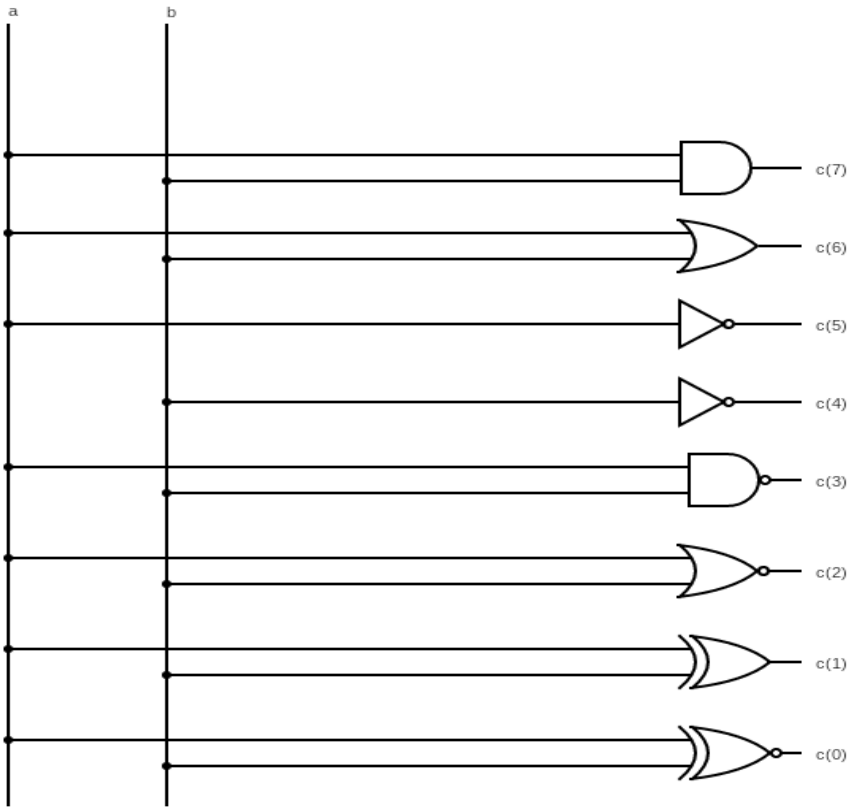
Description

The following circuit has two inputs *a* and *b*, 1 bit each. *c* is the output bus which is of 8 bits. If we consider most significant bit as the first output bit of the output bus, then first bit is the AND of a and b, the second output bit is the OR of *a* and *b*, the third output bit is the INVERTER of *a*, the fourth output bit is the INVERTER of *b*, the fifth output bit is the NAND of *a* and *b*, the sixth output bit is the NOR of *a* and *b*, the seventh output bit is the XOR of *a* and *b*, and the eighth(least significant bit) output bit is the XNOR of *a* and *b*.

Block Diagram



Circuit Diagram



Truth Table

a	b	c(7)	c(6)	c(5)	c(4)	c(3)	c(2)	c(1)	c(0)
		AND	**OR**	**NOT a**	**NOT b**	**NAND**	**NOR**	**XOR**	**XNOR**
0	0	0	0	1	1	1	1	1	0
0	1	0	1	1	0	1	0	0	1
1	0	0	1	0	1	1	0	0	1
1	1	1	1	0	0	0	0	1	0

Code

Entity

```
entity a1 is
    Port ( a : in  STD_LOGIC;
           b : in  STD_LOGIC;
           c : out  STD_LOGIC_VECTOR (7 downto 0));
end a1;
```

Architecture

```
architecture Behavioral of a1 is

begin
   c(0) <= a xnor b;
   c(1) <= a xor b;
   c(2) <= a nor b;
   c(3) <= a nand b;
   c(4) <= not b;
   c(5) <= not a;
   c(6) <= a or b;
   c(7) <= a and b;
end Behavioral;
```

Test Bench

```
ENTITY a1_test_bench IS
 END a1_test_bench;
 ARCHITECTURE behavior OF a1_test_bench IS
    COMPONENT a1
    PORT(
        a : IN  std_logic;
        b : IN  std_logic;
        c : OUT  std_logic_vector(7 downto 0)
       );
    END COMPONENT;

   signal a : std_logic := '0';
   signal b : std_logic := '0';
   signal c : std_logic_vector(7 downto 0);
BEGIN
   uut: a1 PORT MAP (
         a => a,
         b => b,
         c => c
       );
   stim_proc: process

 begin
      a<='0';
       b<='0';
       wait for 1 ps;
       a<='0';
       b<='1';
       wait for 1 ps;
       a<='1';
       b<='0';
       wait for 1 ps;
       a<='1';
       b<='1';
       wait for 1 ps;
   end process;
 END;
```

Timing Diagram